INTEGRATED CIRCUITS

Semiconductors for Wireless Communications

1997

Data Handbook IC17

Philips Semiconductors

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DEFINITIONS

Data Sheet Identification	Product Status	Definition (Note)
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.
Short-form specification	—	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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Preface

Wireless Communications

Thank you for your interest in Wireless Communications products from Philips Semiconductors. As a leading supplier to the Wireless market, we offer a wide range of discrete and integrated semiconductor components.

This Wireless Communications handbook includes information on current Wireless integrated circuits from Philips Semiconductors. The products are used in a wide range of Wireless transmitter and receiver electronics. These applications include: Cellular radio, cordless telephones, high performance receivers, two-way communications and LANs.

Selected products from this handbook can be used to build a complete wireless system. The system diagrams located in the Wireless System Solutions Section can help you determine which products are best suited for your application.

Philips Semiconductors also offers discrete Wireless components through the Discrete Semiconductor Group. For information on this product line, please contact Philips Semiconductors.

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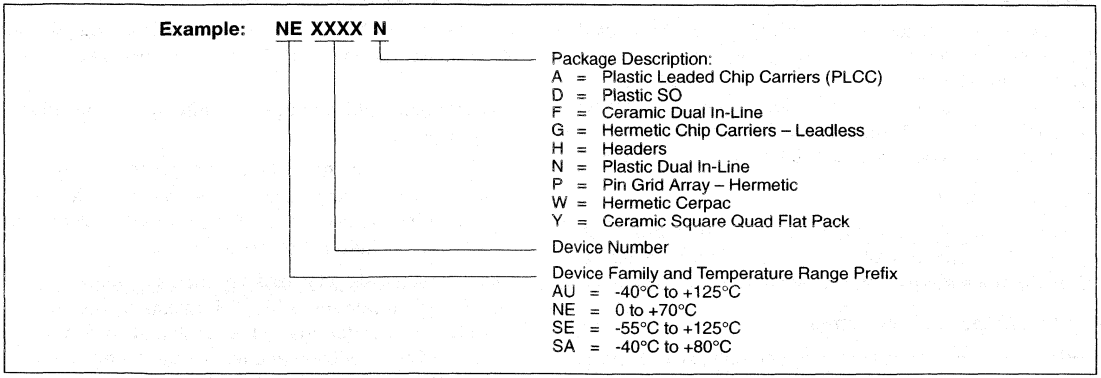
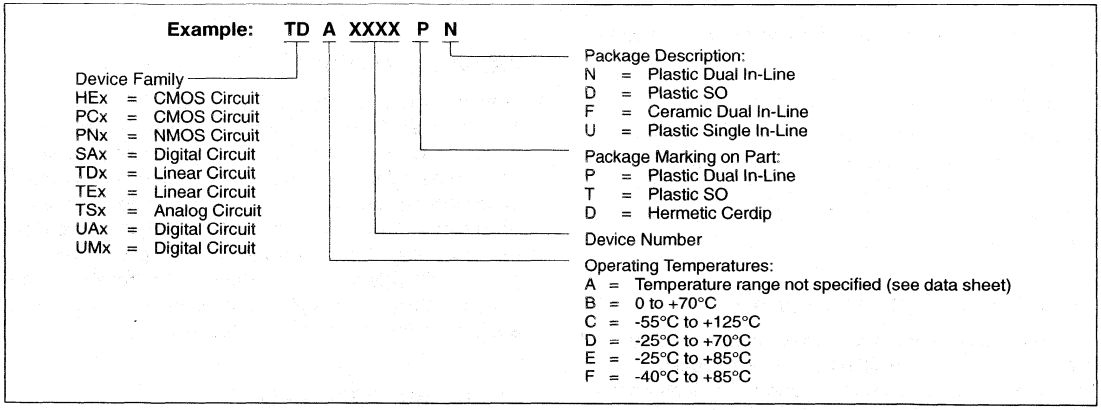
Ordering Information

LINEAR PRODUCTS PART NUMBERING SYSTEM



PHILIPS PRODUCTS PART NUMBERING SYSTEM
PREFIXES HE, PC, PN, SA, TD, TE, TS, UM



TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, components reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the product reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

Section 2
Guides

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System Standard—Product Selector Guide

PRODUCTS			TARGET SYSTEMS														
Function	Type	Description	Cellular							Cordless					Wireless Data		
			(N)AMPS /(E) TACS	IS–54/–136 TDMA	IS–95 CDMA	GSM	DCS1800	PCS	PDC	CTO	CT1	SS	DECT	PHS	802.11	CDPD	PAGERS
RF Amplifiers											X	X					
	SA5200	Gain block–1 GHZ										X				X	
RF Front End																	
	SA600	LNA/Mixer–1 GHz	X	X													
	SA601	LNA/Mixer–1 GHz	X	X							●	●					
	SA611	1 GHz low volt LNA and mixer	X	X	X				X			●			●		
	SA2420	2.45GHz low voltage RF transceiver										●			●		
	SA621	1GHz low volt LNA, mixer and VCO	●	●	●				X			●					
	SA1620	Low voltage GSM RF transceiver				●											
	UAA2072M	Image reject GSM front–end				X											
	UAA2073M	Image reject GSM front–end				X											
	UAA2077AM	Image reject front–end for DECT											X				
	UAA2077BM	2GHz image reject front–end															
	UAA2067G	Image reject 1.8GHz for DECT											●				
	UAA2080T	Advanced pager receiver															X
	UAA2082	Advanced pager receiver															●
Synthesizers/Prescalers																	
	UMA1014T	Synthesizer, 1GHz	X								X					X	
	UMA1015M	Low–voltage, dual–1GHz	●								●					●	
	UMA1017M	Low–voltage, single loop–1 GHz				X						X					
	UMA1018M	Low–voltage, single loop–2 GHz	X		●	●											
	UMA1019M	Low–voltage, single loop–2 GHz				●							●				
	UMA1020M	Low–voltage, low noise–2.2 GHz						X					●	X	●		
	UMA1021M	Low–voltage, very low noise–2.2 GHz				X	X	X	X			●	●	●	●		
	UMA1022	Low voltage, very low noise–2.2 GHz				X	X	X	X			●	●	●	●		
	UMA1005T	Synthesizer, Fractional–N		X		X											
	SA7025	Low–votlage, Fractional–N—1.04 GHz		●		X			●			●					
	SA8025A	Low–voltage, Fractional–N—1.8 GHz		●	●			●	●			●					
Mixer/IF/Demod																	
	SA605	High perf/wide BW mixer FM/IF	X	X								X	X	X	X	X	
	SA606/7/8	Low–voltage, high perf mixer FM/IF	●	●						●	●					●	
	SA626	Low–voltage/Wide BW/fast RSSI										●		●			
	SA636	SA626 with Wideband data output											X		●	●	

System Standard—Product Selector Guide

PRODUCTS			TARGET SYSTEMS														
			Cellular							Cordless					Wireless Data		
Function	Type	Description	(N)AMPS /(E) TACS	IS–54/–136 TDMA	IS–95 CDMA	GSM	DCS1800	PCS	PDC	CTO	CT1	SS	DECT	PHS	802.11	CDPD	PAGERS
	SA637	SA626 with Digital IF		●				●									
	SA639	Low–votlage mixer FM/IF w/switch										X	●		●		
	SA1630	Low voltage transceiver w/74 dB VGA							X			X			●		
	SA1638	Low–voltage GSM IF transceiver				●											
Transmitter																	
	SA900	I/Q transmit modulator		●								X					
	SA910	Variable gain RF predriver amplifier	●									X					
	SA2410	2.45 GHz PA and T/R Switch													●		
	CGY2011					●											
	CGY2012					●											
	CGY2013					●											
	CGY2020						●										
	CGY2021	DCS/PCS 2W power amplifier		●			●										
	CGY2023						●										
	CGY2030												●				
	CGY2032												●				
	PAT1906												●				

The Philips Family Of High Performance Front End Systems

	Description	V_{CC}	I_{CC}	Pins	Pkg	Input Frequency	Gain (power)	Noise Figure	Input IP3	1dB Comp.	Input Imped.	Output Imped.	Feature Highlights
Image Reject Front–end Systems							f_{RF}=2 GHz						
UAA2067G	LNA+IRM+Mod+VCO	3–5.5V	24mA (rx) 45MA (T_X)	32	BE	1.8–2.2 GHz	32 dB	6 dB	–25 dBm	–32dBm	50Ω	50Ω	—Image reject Mixing —DECT, DCS1800, GSM and US PCS
UAA2077AM	LNA+IRM	3.15–5.3V	27mA @4V	20	DK	1.8–2.2 GHz	20 dB	4.3 dB	–17 dBm	–22dBm	35Ω	1κ Ω	
UAA2077BM		3.6–5.3V	27mA @4V	20	DK	1.8–2 GHz	20 dB	4.3 dB	–17 dBm	–23dBm	35Ω	1κ Ω	
Image Reject Front–End Systems							f_{RF}=900 MHz						
UAA2072M	LNA+IRM+Mixer	4.5–5.3V	31.5mA@5V	20	DK	LNA+IRM 960 MHz	26 dB	4 dB	–15 dBm	–24.5dBm	200Ω	High	—Image reject mixer (30dN min) —T_x down–convert mixer
UAA2073M	Integrated Front–end	3.6–5.3V	26mA@3.75V	20	DK	960 MHz	23 dB	3.25 dB	–15 dBm	–23 dBm	150Ω	1kΩ	—30 dB min image rejection
Integrated Front–End Systems							f_{RF}=900 MHz						
NE/SA600	LNA+IRM+Mixer	4.5–5.5V	13mA/4.2mA* @5V	14	D	LNA 1/2 GHz	16/–7.5 dB*	2.2 dB	–10/+26dBm	–20 dBm	50Ω	50Ω	—LLNA Overload Mode —Excellent Noise Figure
						Mixer 1.2 GHz	–2.6 dB	14 dB	+6 dBM	–14 dB	50Ω	High	
NE/SA601	LNA+IRM+Mixer	42.7–5.5V	7.4mA@3V	20	DK	LNA 1/2 GHz	11.5 dB	1.6 dB	–2 dBm	–16 dBm	50Ω	50Ω	—Low voltage —Excellent Noise Figure
						Mixer 1.2 GHz	+6 dB	10 dB	–2 dBm	–13 dBm	50Ω	High	
SA620	LNA+Mixer+VCO	2.7–5.5V	10.4mA/7.2mA* @3V	20	DK	LNA 1/2 GHz	11.5/–7.5 dB*	1.6 dB	–3/+25 dBm*	–16 dBm	50Ω	50Ω	—Low voltage —Excellent Noise Figure —LNA Overload Mode —Internal VCO
						Mixer 1.2 GHz	+3dB	9 dB	–6 dBm	–13 dBm	50Ω	High	
SA611	LNA+Mixer	2.7–5.5V	8mA@3V	20	DK	LNA 1 GHz	15 dB	1.9 dB	–7 dB	–16 dBm	50Ω	50Ω	—Low voltage
						Mixer 1 GHz	9 dB	0.5 dB	4 dB	–9 dBm	50Ω	High	—Excellent system perf
SA621	LNA+Mixer+VCO	2.7–5.5V	13.3mA/10mA* @3V	20	DK	LNA 1 GHz	15dB	1.9 dB	–7 dB	–16 dB	50Ω	50Ω	—Low voltage
						Mixer 1 GHz	9 dB	10.5 dB	4 dB	–9 dB	50Ω	High	—Excellent system perf
Integrated Front–End Transceiver							f_{RF}=900 MHz						
SA1620	Rx: 2 LNAs w/atten.+mixer T_x: P_{OUT}=+8.5 dBm@2.7V+mixer	2.7–5.5V	R_x:28 mA T_x: 59 mA	48	BE	<1800 MHz	LNA 20 dB 8.5 dB	1.9 dB 10 dB	–5 dB 2 dB	–15 dBm –7.3 dBm	50Ω 50Ω	50Ω High	—LNA gain control range=59dB —Excellent noise Figure —T_x power adjustable
SA2420	Rx: LNA w/atten.+mixer T_x: Predriver+mixer	2.7–5.5V	R_x:21 mA T_x: 34 mA	24	DH	2.4–2.5 GHz	LNA 14 dB Mixer 8 dB	2.5 dB 11 dB	–6dBm 1 dBm	–17dBm –10 dBm	50Ω 50Ω	50Ω High	—low voltage —LNA gain atten. range=22dB —T_x P_{OUT}=0dBm
Mixer Systems							f_{RF}=45 MHz						
NE/SA602A	Mixer+Oscillator	4.5–8.0V	2.4mA@6V	8	N,D	500 MHz	17dB	5.0 dB	–13cBm	–25dBm	1.5kΩ	1.5kΩ	—Excellent Noise Figure —High Gain
NE/SA602A	Mixer+Oscillator	4.5–8.0V	2.4mA@6V	8	N,D	500 MHz	17dB	5.0 dB	–13cBm	–25dBm	1.5kΩ	1.5kΩ	—Excellent Noise Figure —High Gain

Temperature Range
NE: 0 to 70°C
SA: –40 to +85°C

D: Small Outline–14
Small Outline–16
Small Outline–20

Package Descriptions
DK: Shrink Small Outline Package (SSOP)–20
BE: Low Qaud Flat Paackage (LQFP)

N: Dual In–Line Plastic

*Amplifier: Enabled/Disabled

Discrete Front–End Selector Guide

FUNCTION	SYSTEM FREQUENCY (MHZ)	SOT23	SOT323	SOT143(1)	SOT343(1)	SOT353(2)	SOT363(2)
LNA	900;1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505
	900:1900	BFR520	BFS520	BFG520	BFG520W	BFC520	BFM520
MIXER	900	BFR93A	BFR93AW	BFG83A	BFG83AW		
	900;1900	BFR505	BFS505	BFG505	BFG505W	BFE505	BFM505
	900;1900	BFR520	BFS520	BFG520	BFG520W	BFE520	BFM520
BUFFER AND VCO	900	BFR92A	BFR92AW	BFG92A	BFG92AW		
	900	BFR93A	BFR93AW	BFG93A	BFG93AW		
	900	BFQ67	BFQ67W	BFG87	BFG87W		
	900;1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505
	900;1900	BFR520	BFS520	BFG520	BFG520W	BFC520	BFM520
IF	40 TO 100	BF547	BF547W				
		BFS17	BFS17W	BFG17A			
		BFR92A	BFR92AW	BFG92A	BFG92AW		

1. Also available in /X and /XR versions.
2. Under development.

RF Amplifier Family Overview

	NE/SA5200	NE/SA5204A	NE/SA5205A	NE/SA5209	NE/SA5219
Description	**Dual Gain Stage**	**Wideband Amp**	**Wideband Amp**	**Variable Gain Amp**	**Variable Gain Amp**
V_{CC}	4 – 9V	5 – 8V	5 – 8V	4.5 – 7.0V	4.5 – 7.0V
I_{CC}	4.2mA/95μA*@5V (per amplifier)	25mA @ 6V	25mA @ 6V	43mA @ 5V	43mA @ 5V
Bandwidth (3dB)	DC - 1.2GHz	DC - 350MHz	DC - 550MHz	DC - 850MHz	700MHz
Gain (power)	7.5dB/–13.5dB* (per amplifier)	19dB	19dB	25dB (voltage)	25dB (voltage)
Noise Figure	3.6dB	6.0 dB 50Ω 4.8 dB 75Ω	6.0 dB 50Ω 4.8 dB 75Ω	9.3dB	9.3dB
1dB Compression	+3.2dBm	+4dBm	+4dBm	–3dBm	–3dBm
3rd Order Intercept (input)	–1.8dBm	–2dBm	–2dBm	+13dBm (output)	+13dBm (output)
Input Impedance	50Ω	50Ω	50Ω	1.2kΩ	1.2kΩ
Output Impedance	50Ω	50Ω	50Ω	60Ω	60Ω
Package	SO8	DIP8 SO8	DIP8 SO8	DIP16 SO16	DIP16 SO16
Features	+DC to 1.2GHz operation +Power-Down mode	+DC to 350MHz operation	+DC to 550MHz operation	+DC to 850MHz operation +Gain control pin	+DC to 700MHz operation +Gain control pin

*Amplifier: Enabled/Disabled

The Philips Family of High Performance IF Systems

	V_{CC}	I_{CC}	Pins	Package	Input Freq	IF Freq	f_{RF}=45MHz			RSSI Range	Fast RSSI	Freq Check Pin	IF Filter Match	Output Op Amps	Feature Highlights
							Input Sensitivity	Mixer Gain	Input IP3						
FM IF															
NE/SA604A	4.5–8V	3.3mA@6V	16	D,N	25MHz	25MHz	0.22μV[1]	–	–	90dB	–	–	455kHz	–	–High Sensitivity
NE/SA614A	4.5–8V	3.3mA@6V	16	D,N	25MHz	25MHz	0.22μV[1]	–	–	80dB	–	–	455kHz	–	
NE/SA624	4.5–8V	3.3mA@6V	16	D,N	25MHz	25MHz	0.22μV[1]	–	–	90dB	✓	–	455kHz	–	–Wide IF BW
MIxer/FM IF															
NE/SA605	4.5–8V	5.7mA@6V	20	D,DK,N	500MHZ	25MHz	0.22μV[1]	13dB	–10dBm	90dB	–	–	455kHz	–	–High Sensitivity
NE/SA615	4.5–8V	5.7mA@6V	20	D,DK,N	500MHZ	25MHz	0.22μV[1]	13dB	–10dBm	80dB	–	–	455kHz	–	–High Input Frequency
NE/SA625	4.5–8V	5.7mA@6V	20	D,DK,N	500MHZ	25MHz	0.22μV[1]	13dB	–10dBm	90dB	✓	–	455kHz	–	
NE/SA627	4.5–8V	5.7mA@6V	20	D,DK,N	500MHZ	25MHz	0.22μV[1]	13dB	–10dBm	90dB	✓	✓	455kHz	–	–Wide IF BW
LowVoltage Mixer/FM IF															
SA606	2.7–7V	3.5mA@3V	20	D,DK,N	150MHZ	2MHz	0.31μV[1]	17dB	–9dBm	90dB	–	–	455kHz	Audio Op Amp RSSI Op Amp	–High Sensitivity –Low Power –Audio/RSSI output Op Amps –Power–Down Mode (SA626/636/639)
SA616	2.7–7V	3.5mA@3V	20	D,DK,N	150MHZ	2MHz	0.31μV[1]	17dB	–9dBm	80dB	–	–	455kHz	Audio Op Amp RSSI Op Amp	
SA607	2.7–7V	3.5mA@3V	20	D,DK,N	150MHZ	2MHz	0.31μV[1]	17dB	–9dBm	90dB	–	✓	455kHz	Audio Op Amp RSSI Op Amp	
SA617	2.7–7V	3.5mA@3V	20	D,DK,N	150MHZ	2MHz	0.31μV[1]	17dB	–9dBm	80dB	–	✓	455kHz	Audio Op Amp RSSI Op Amp	
SA608	2.7–7V	3.5mA@3V	20	D,DK,N	150MHZ	2MHz	0.31μV[1]	17dB	–9dBm	90dB	–	✓	455kHz	Audio Op Amp RSSI Op Amp	
SA626	2.7–5.5V	6.5mA@3V	20	D,DK,N	500MHZ	2MHz	0.54μV[2]	11dB[2]	–16dBm	90dB	✓	–	10.7MHz	RSSI Op Amp	
SA636	2.7–5.5V	6.5mA@3V	20	D,DK,N	500MHZ	2MHz	0.54μV[2]	11dB[2]	–16dBm	90dB	✓	–	10.7MHz	RSSI OP AMP	
SA639	2.7–5.5V	8.5mA@3V	24	DH	500MHZ	25MHz	2.24μV[4]	12dB[4]	–12.5dBm[4]	90dB	✓	–	10.7MHz	Audio Buffered RSSI Op Amp Post–detect Amp Data Switch	
SA676	2.7–5.5V	3.5mA@3V	20	D,DK	100MHZ	25MHz	0.45μV	17dB	–10dBm	70dB	–	–	455kHz		
Low Voltage Mixer/Digital IF															
SA637	2.7–5.5V	3.5mA@3V	20	D,DK	200MHZ	2MHz	$\frac{-117dBm^3}{0.31\mu V}$	15dB	–10dBm	90dB	✓		455kHz	RSSI Op Amp	

Part	Description	V_{CC}	I_{CC}	Pins	Pkg	Input Freq	Gain (power)	Noise Figure	Input IP3	1dB Comp	Input Imped.	Out Imped.	Features
IF Transceiver													
SA1638	R_X: IF amp+I/Q mixers+buffers T_X: I/Q Mixers+buffers+IF Synthesizer	3.3–5.5V	R_X: 16mA T_X: 19.5mA	48	BE	70–400MHz				In–Band –53dBv Other –47dBv		1kΩ	–Internal IF PLL –Tunable IF BW=50–850 kHz –Two DC regulators
SA1630	R_X: 74dB VGA+I/Q mixers+buffers T_X: I/Q mixers+buffers	2.7–5.5V	Rx: 33.5mA Tx: 26.5mA	48	BE	70–400MHz							–Internal IF PLL 74dB VGA

Temperature Ranges
NE: 0 to 70°C
SA: –40 to +85°C

Package Descriptions
D: Small Outline–16
Small Outline–20
DK: Shrink Small Outline Package (SSOP)–20
N: Dual In–Line Plastic–16, 20

IF Filter Match
455kHz=1.5kΩ
10.7MHz=330Ω

The Philips Family of High Performance Frequency Synthesizers

	V_{CC}	I_{CC}	Pins	Pkg	Max RF/Input Frequency	Channel Spacing	Fractional–N Divider	Auxiliary Synthesizer	Applications
Fractional–N Frequency Syntesizer									
SA7025DK	2.7 to 5.5V	7.5mA@3V	20	SSOP20	1.0GHz (main) 150MHz (aux) 40MHz(aux)	10–5000kHz (main) 40–20,000kHz (aux) 10–5000kHz (aux)	✓	✓	IS–54/–136, IS–95, PDC, GSM digital cellular
SA8025ADK	2.7 to 5.5V	11 mA@3V	20	SSOP20	1.8GHz (main) 150MHz (aux) 40MHz(aux)	10–5000kHz (main) 40–20,000kHz (aux) 10–5000kHz (aux)	✓	✓	PHS digital cordless, U.S. PCS, PDC digital cellular
UMA1005T	2.9 to 5.5V	5mA@3V	20	SSOP20	30GHz (main) 90MHz (aux) 30MHz(aux)	10–20,000kHz (aux) 40–20,000kHz (aux) 10–5000kHz (aux)	✓	✓	IS–54/–136, IS–95, PDC, GSM digital cellular
Frequency Synthesizers									
UMA1014T	4.5 to 5.5V	13mA@5V	16	SO16	1.1GHz	5–100kHz			AMPS/TACS cellular, cordless
UMA1015M	2.7 to 5.5V	9.6mA@3V	20	SSOP20	1.1GHz 1.1GHz	8.5–375kHz		✓ (dual)	CT1/CT1+ cordless AMPS/TACS, NMT cellular
UMA1017M	2.7 to 5.5V	6.5mA@3V	20	SSOP20	1200MHz	10–200kHz			GSM digital cellular, spread spectrum
UMA1018M	2.7 to 5.5V	8.5mA@3V	20	SSOP20	1200MHz (main) 300MHz (aux)	10–2000kHz (main) 10–1000kHz (aux)		✓	GSM digital cellular
UMA1019M	2.7 to 5.5V	9.5mA@3V	20	SSOP20	2200MHz	10–2000kHz			DECT digital cordless DCS 1800
UMA1020M	2.7 to 5.5V	12mA@3V	20	SSOP20	2200MHz (main) 300MHz (aux)	10–2000kHz (main) 10–2000kHz (aux)		✓	DECT digital cordless, dcs1800, phs
UMA1021M	2.7 to 5.5V	9mA@3V	20	SSOP20	2200MHz	10–2000kHz			WLAN DECT digital cordless DCS 1800, PHS
UMA1022M	2.7 to 5.5V	13mA@3V	20	SSOP20	2200MHz (main) 500MHz (aux)	10–2000kHz		✓	WLAN DECT digital cordless DCS 1800, PHS

	V_{CC}	I_{CC}	Pins	Pkg	Max Input Frequency	Max Compare Frequency	Input Sensitivity	Divide Ratio
Prescalers								
SA701N,D	2.7 TO 6V	4.5mA@3V	8	DIP, S08	1.1GHz	65kHz/270kHz	–35 dBm	128/129,64/65
SA702N,D	2.7 TO 6V	4.5mA@3V	8	DIP, S08	1.1GHz	1000kHz	–35 dBm	64/66/72
SA703N,D	2.7 TO 6V	4.5mA@3V	8	DIP, S08	1.1GHz	335kHz	–35 dBm	128/129/144

RF Power Modules For Portable Equipment

TYPE NUMBER	APPLICATION	FREQUENCY BAND (MHZ)	SUPPLY VOLTAGE (V)	LOAD POWER (W) MIN.	DRIVE POWER (inW)	POWER GAIN (DB) MIN.	EFFICIENCY (%) MIN.	EFFICIENCY (%) TYP.	PACKAGE	PACKAGE THICKNESS (min)
ANALOG CELLULAR										
BGY115A	AMPS	824–849	6.0	1.2	2	27.8	45	50	SOT321	4
BGY115B	(E) TACS	872–905	6.0	1.2	2	27.8	45	50	SOT321	4
BGY115D	Spread Spectrum	902–928	6.0	1.2	2	27.8	45	50	SOT321	4
BGY118A	AMPS	824–849	4.8	1.2	2	27.8	50	55	SOT321	4
BGY118B	(E)TACS	872–905	4.8	1.2	2	27.8	50	55	SOT321	4
BGY118D	SPREAD SPEC-TRUM	898–928	4.8	1.2	2	27.8	50	55	SOT321	4
BGY119A	AMPS	824–849	4.8	1.2	2	27.8	50	55	SOT359	3
BGY119B	(E)TACS	872–905	4.8	1.2	2	27.8	50	55	SOT359	3
BGY119D	Spread Spectrum	902–928	4.8	1.2	2	27.8	50	55	SOT359	3
BGY122A	AMPS	824–849	4.8	1.2	2	27.8	50	55	SOT388	2
BGY122B[1]	(E)TACS	872–905	4.8	1.2	2	27.8	50	55	SOT388	2
BGY122D[1]	Spread Spectrum	898–928	4.8	1.2	2	27.8	50	55	SOT388	2
BGY120A	AMPS	824–829	3.6	1.2	2	27.8	50	55	SOT388	2
BGY120B[2]	(E)TACS	872–905	3.6	1.2	2	27.8	50	55	SOT388	2
BGY120D[2]	Spread Spectrum	898–928	3.6	1.2	2	27.8	50	55	SOT388	2
DIGITAL CELLULAR										
BGY201	GSM	880–915	12.5	14	1	41.5	33	35	SOT278A	7
BGY202	GSM	890–915	6.0	1.4	2	28.5	45	50	SOT321	4
BGY203	GSM	880–915	6.0	3.5	1	35.5	40	–	SOT342	4
BGY205	GSM	880–915	6.0	3.5	2	32.5	–	45	SOT321B	3
BGY204[1]	GSM	880–915	4.8	3.2	2	32.5	–	45	SOT321B	3
BGY206[1]	GSM	880–915	4.8	3.0	5	27.8	–	45	SOT308	2
BGY207[1]	GSM	880–915	4.8	1.2	2	27.8	50	55	SOT359	3
BGY208[1]	GSM	880–915	6.8	3.5	10	30.7	–	45	SOT388	2

1. Preliminary specification
2. Objective specification

RF Power Transistors for Portable Equipment

TYPE NUMBER	FREQUENCY (MHZ)	SUPPLY VOLTAGE (V)	LOAD POWER (W)	POWER GAIN (DB) MIN.	EFFICIENCY (%) MIN.	EFFICIENCY (%) TYP.	RESISTANCE$_3$ (K/W)	THERMAL PACKAGE
ANALOG CELLULAR								
BLT80	900	7.5	0.8	6	60	67	22[4]	SOT223
BLT81	900	7.5	1.2	6	60	70	32[5]	SOT223
BLT80	900	6.0	0.8	6		70	22[4]	SOT223
BLT81	900	6.0	1.2	6		70	32[5]	SOT223
BLT70	900	4.8	0.6	6	60		38[6]	SOT223
BLT71	900	4.8	1.2	6	60		24[7]	SOT223
BLT71/81	900	4.8	1.2	10	55	63	50[11]	SOT86 (SO8pl)
BLT61	900	3.8	1.2	6	50	60	30[8]	SOT86 (SO8pl)
DIGITAL CELLULAR								
BFG540W	900	8.0	18 dBM	6	60	67	22[4]	SOT433
BFG540W	1900	3.6	14 dBm	6	60	67	22[4]	SOT433
BFG10W/x	900	6.0	28 dBm	6	60	67	22[4]	SOT433
BFG10W/x	1900	3.6	20 dBm	6	60	67	22[4]	SOT433
BFG11W/x	1900	3.6	26 dBm	6	60	67	22[4]	SOT433
BLT82	900	6.0	3.5	6	50	65	32[17]	SOT96 (S08pl)
BLT72[1]	900	4.8	3.0	6	50	55	30[8]	SOT96 (S08pl)
BLT62	900	3.6	3.0	9	50	65	30[8]	SOT96 (S08pl)
BLT13[1]	1800	6.0	2.0	6	50	55	45[10]	SOT96 (S08pl)
BLT14	1800	4.8	1.6	6	50	65	45[10]	SOT96 (S08pl)

APPLICATION	SUPPLY VOLTAGE	LOAD POWER	1ST STAGE	2ND STAGE	3RD STAGE
ANALOG	6.0	1.2	BFG540W/x	BLT80	BLT81*
	4.8	1.2	BFG540W/x	BLT70	BLT71
	4.8	1.2	BFG510W/x	BLT7118	–
	3.8	1.2	BFG540W/x	BFG10W/x	BLT61
GSM	6.0	3.5	BFG540W/x	BFG10W/x	BLT82
	4.8	3.0	BFG540W/x	BFG10W/x	BLT72
	3.6	3.0	BFG540W/x	BFG10W/x	BLT62
PCN/DCS1800	6.0	2.0	BFG540W/x	BFG10W/x	BLT13
	4.8	1.6	BFG540W/x	BFG10W/x	BLT14
DECT	3.6	0.4	BFG540/x	BFG10x	BFG11/x
			BFG540W/x	BFG10W/x	BFG11W/x

NOTES:

T_0 is the temperature at the soldering pointof the collector tab

1. Preliminary specification
2. Objective specification
3. Junction to soldering point
4. P_{tot} =2W, T_G=131°C
5. P_{tot} =2W, T_G=110°C
6. P_{tot} =2W, T_G=95°C
7. P_{tot} =3.5W, T_G=90°C
8. P_{tot} =2W, T_G=115°C
9. P_{tot} =2W, T_G=115°C
10. P_{tot} =1W, T_G=130°C
11. P_{tot} =1.7W, T_G=90°C
12. P_{tot} =1.9W, T_G=115°1

Baseband Processors

Part No.	Part Type	Application	V_{DD}	I_{DD}	Package
PCD5032	ADPCM Codec	DECT	2.7-6.0V 2.7-6.0V	7mA Typ. Active 20µA Typ. Stdby	28-Pin SO28 44-Pin QFP
PCD5041	BMC (Burst Mode Controller)	DECT	2.7-6.0V	15mA Typ. Active	64-Pin QFP
NE/SA5750	Audio Companding Amplifier	AMPS TACS	5.0V	8.4mA Typ. 1.8mA Stdby	24-Pin DIP 28-Pin SOL
NE/SA5751	Audio Filter and Control	AMPS TACS	5.0V	2.7mA Typ. 0.9mA Stdby	24-Pin DIP 28-Pin SOL
SA5752	Audio Companding VOX and Amplifier	AMPS TACS	2.7V	31mA Typ. 125µA Stdby	20-Pin SOL 20-Pin SSOP
SA5753	Audio Filter and Control	AMPS TACS	2.7V	2.7mA Typ. 600µA Stdby	20-Pin SOL 20-Pin SSOP
PCF5001	POCSAG Decoder	PAGERS	1.5-6.0V	60µA Typ.	28-Pin Mini-Pak 32-Pin QFP
PCD5003	Advanced POCSAG Decoder	PAGERS	1.5-6.0V	50µA Typ. (ON) 25µA Typ. (OFF)	32-Pin TQFP
UMA1000LT	Data Processor for Cellular Radio	AMPS TACS	3.0-5.5V	2.5mA Typ.	28-Pin SOL
UMA1002	Data Processor for Cellular Radio	AMPS TACS	2.7-5.5V	2.5mA Typ.	28-Pin SOL 32-Pin LQFP

*Amplifier: Enabled/Disabled

The Philips Family of High Performance Compandors

	V_{CC}	I_{CC}	Pins	Packages	ALC Voltage	Reference Gain	Unity Down	Power Features	Key	Applications
NE/SA570	6-24V	3.2mA	16	D, F, N	Both Channels	Fixed 1.8V	775mV_{RMS}	No	– Excellent Unity Gain Tracking Error – Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
NE/SA571	6-18V	3.2mA	16	D, F, N	Both Channels	Fixed 1.8V	775mV_{RMS}	No	– Excellent Unity Gain Tracking Error – Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
NE/SA572	6-2V	6mA	16	D, F, N	Both Channels	Fixed 2.5V	100mV_{RMS}	No	– Independent Attack & Release time – Good THD – Need an Ext Summing Op Amp	High Performance Audio Circuits "Hi-Fi Studio Quality"
NE/SA575	3-7V	3-5.5mA	20	D, DK, N	Right Channels	$V_{CC}/2$	100mV_{RMS}	No	– Two uncommitted On-chip Op Amps Available – Low Voltage	Consumer Audio Audio Circuits "Commercial Quality"
NE/SA576	2-7V	1-3mA*	14	D, N	Right Channels	$V_{CC}/2$	100mV_{RMS}	No	– Low Power – Low External Component Count	Battery Powered Systems "Commercial Quality"
NE/SA577	2-7V	1-2mA*	14	D, N	Right Channels	$V_{CC}/2$	10mV to 1mV_{RMS}	No	– Low Power – Programmable Unity Gain	Battery Powered Systems "Commercial Quality"
NE/SA578	2-7V	1-2mA*	16	D, N	Right Channels	$V_{CC}/2$	10mV to 1mV_{RMS}	Yes (170µA)	– Low Power – Programmable Unity Gain – Power Down – Mute Function Summing Capability (DTMF) – 600Ω Drive Capability	Battery Powered Systems "Commercial Quality"

NOTE: NE/SA5750 and SA5752/5753 are also Excellent Audio Processor Components for High Performance Cordless and Cellular Applications that include the Companding Function
*I_{CC} varies with V_{CC}
Packages include: NE: 0 to 70°C; SA: -40 to +85°C; N: Plastic DIP; D; Plastic SO; F: Ceramic DIP; DK: SSOP (Shrink Small Outline Package)
Applications include: Cordless Phones, Cellular Phones, Wireless Mics, Modems, Consumer Audio and Two-Way Communications.

MOSFETS Selector Guide

TYPE	DESCRIPTION	CHANNEL	GATE(S)	SUPPLY VOLTAGE (V_{DS})	PACKAGE
PHN205	Low ohmic battery switch	N&N	Dual	25	S08 (SOT96)
PHP212	Low ohmic battery switch	P&P	Dual	25	S08 (SOT96)
PHC20512	Low ohmic battery switch	N&P	Dual	25	S08 (SOT96)
PHN103	Low ohmic battery switch	N	Single	30	S08 (SOT96)
PHP109	Low ohmic battery switch	P	Single	30	S08 (SOT96)
BSP030	Low ohmic battery switch	N	Single	30	S08 (SOT96)
BSP090	Low ohmic battery switch	P	Single	30	S08 (SOT96)

TYPE	DESCRIPTION	CHANNEL	GATE(S)	SUPPLY VOLTAGE (V_{DS})	PACKAGE
BF904	Mixer/oscillator	N&P	Dual	3 to 7	SOT143
BF904WR	Mixer/oscillator	N&P	Dual	3 to 7	SOT343
BF909	Mixer/oscillator	N&P	Dual	3 to 7	SOT143
BF909WR	Mixer/oscillator	N&P	Dual	3 to 7	SOT343

TYPE	DESCRIPTION	CHANNEL	GATE(S)	SUPPLY VOLTAGE (V_{DS})	PACKAGE
BSN254	Line interrupter/ground switch	N	Single	250	SOT54
BSN304	Line interrupter/ground switch	N	Single	300	SOT54
BSP126	Line interrupter/ground switch	N	Single	250	SOT223
BSP130	Line interrupter/ground switch	N	Single	300	SOT223
VN2406L	Line interrupter/ground switch	N	Single	240	SOT54
BSP92	Line interrupter/ground switch	P	Single	240	SOT54
BSP225	Line interrupter/ground switch	P	Single	250	SOT223
BSP224	Line interrupter/ground switch	P	Single	250	SOT54
BSP304	Line interrupter/ground switch	P	Single	250	SOT223

Section 3
Wireless System Solutions

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SYSTEM SOLUTIONS FOR WIRELESS STANDARDS

As the fastest growing area in electronics, the wireless personal communications market is fiercely competitive for semiconductor, communication equipment and EDP vendors alike. As a market characterized by a multiplicity of standards, only vendors with resources, vision and a commitment to innovation will realize the standards of the future. Philips Semiconductors is such a vendor, with chipset solutions for virtually all current cellular, cordless and paging standards, and with roadmaps for the global systems of the future.

The following section contains information on chipsets for several cellular telephone, cordless telephone, and wireless data standards. The system solutions and block diagrams presented in this section represent Philips chipset solutions that are currently available. Detailed information on individual ICs can be found in the preceding sections of this or other referenced data handbooks.

The list of solutions presented is by no means exhaustive, and is intended to demonstrate Philips' products and capabilities in several important wireless markets. Philips is constantly moving forward with new solutions for existing, as well as emerging, standards. If you would like more information on current chipsets and standard ICs, or would like to see what we are planning for the future, please contact your local Philips sales engineer or Philips representative.

GSM (Global System for Mobile Communications) Digital Cellular Chipset

GSM Digital Cellular

Since the late 1980s, Philips Semiconductors has been involved in developing ICs for the GSM (Global System Mobile) Digital Cellular standard. As a major supplier for this rapidly growing market, Philips has all the competencies required for GSM systems.

Introducing the first GSM chipset working at 3V

With samples now available, this 3 V chip-set uses low-power, low-voltage technology, is highly integrated and is suitable for GSM systems. This 8-chip solution is the next milestone on the road to smaller digital phones. Key features include ICs fabricated in 0.5µm CMOS technology for the baseband and QUBiC (BiCMOS) technology for the RF ICs. The ICs are encapsulated in small TQFP and SSOP packages.

In the RF section, three new ICs complement the existing PCF5075: the SA1620 RF transceiver, the SA1638 IF transceiver and the UMA1019 RF synthesizer. The RF chip set supports high IF frequencies and allows simple, low-cost filters to be used for image-rejection.

The baseband and audio interface (PCD5072) is a new single-chip interface between the IF transceiver, the microphone & earpiece and the baseband processor. It integrates an audio Codec and auxiliary AD/DA converters for AGC, AFC and power management.

The new baseband DSP (PCF5083) includes the TDMA timer. An on-chip ROM contains firmware program modules to perform all necessary processing algorithms. Special attention has now been given to equalization to improve performance in hilly areas and fast-moving vehicles.

The following components have, in addition, board level support tools:

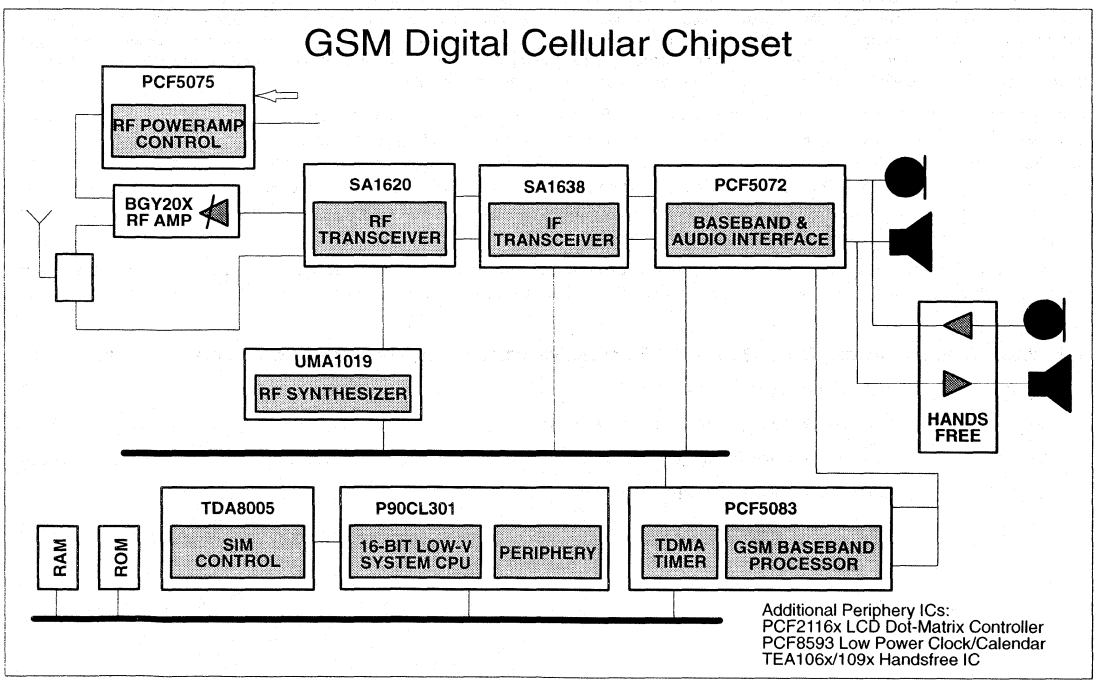
- **SA1620** GSM front-end transceiver
- **SA1638** IF I/Q transceiver
- **UMA1019AM** Frequency synthesizer
- **PCF5075** RF power amplifier Controller (OM4768 evaluation board)
- **P90CL301** Low-voltage 16-bit microcontroller (OM5040 evaluation board)
- **TDA8005** Smart Card Interface (CAKE 501-A evaluation board)
- LCD drivers and other Peripheral ICs: handsfree speakerphone IC (OM5027 evaluation board)
- Clock/calendar IC, etc.

GSM Digital Cellular

Philips Semiconductors offers a complete GSM chipset for mobile telephones and base-stations that consists of: **IC17 Page**

GSM Digital Cellular Chipset:

SA1620	Low-voltage GSM RF transceiver	4–147
SA1638	Low-voltage GSM IF transceiver	6–292
UMA1019AM	Low-voltage frequency synthesizer for radio telephones	7–199
PCF5075	Power amplifier controller for GSM systems	9–254
TDA8005	SIM interface	9–439
P90CL301	Low-voltage microcontroller	12–111
PCF5083	GSM baseband processor	9–271



IS-54/-136 TDMA Digital Cellular

North American Digital Cellular (NADC) IS-54/-136 TDMA RF Transceiver Chipset

IS-54/-136 (D-AMPS; TDMA) AND IS-95 (CDMA)

Designed to address the problem of using existing channels more efficiently, IS-54/-136 employs the same 30 kHz channel spacing and frequency bands (824-849 and 869-894 MHz) as the current North American analog cellular standard: AMPS. By using TDMA instead of FDMA, IS-54/-136 increases the number of users from 1 to 3 per channel (up to 10 with enhanced TDMA). The IS-54/-136 specification states that the digital handset and system must also support the analog AMPS system. Experience from the low power AMPS chip-set, together with customer inputs, were combined to produce a 4-chip solution for an IS-54/-136 RF/IF section.

IS-95 is another digital standard that uses the same frequency bands as AMPS and supports AMPS operation. This standard uses CDMA, employing spread-spectrum technology and a special coding scheme. This standard is at a very early stage but promises a threefold increase in user capacity over IS-54/-136.

IS-54/-136 transceiver chip-set

To compete with existing analog standards, a low power, highly integrated solution is a must for any digital standard to succeed. Our new chip-set for IS-54/-136 meets these criteria. The chip-set combines all of the necessary RF and IF functions into four integrated devices: the SA621 RF front end, the SA7025 dual frequency synthesizer, the SA900 I/Q transmit modulator and the SA637 digital IF receiver *or* SA606 FM IF receiver + external I/Q demodulator. These devices were designed as a system and therefore have interface levels which are matched, eliminating the need for additional buffers and interface devices. There is also a common high speed serial interface bus, making addressing the devices simpler. Additionally the frequency plan was designed to eliminate the need for an additional synthesizer and VCO loop. All of these features dramatically reduces the cost and size while improving the performance of the overall system.

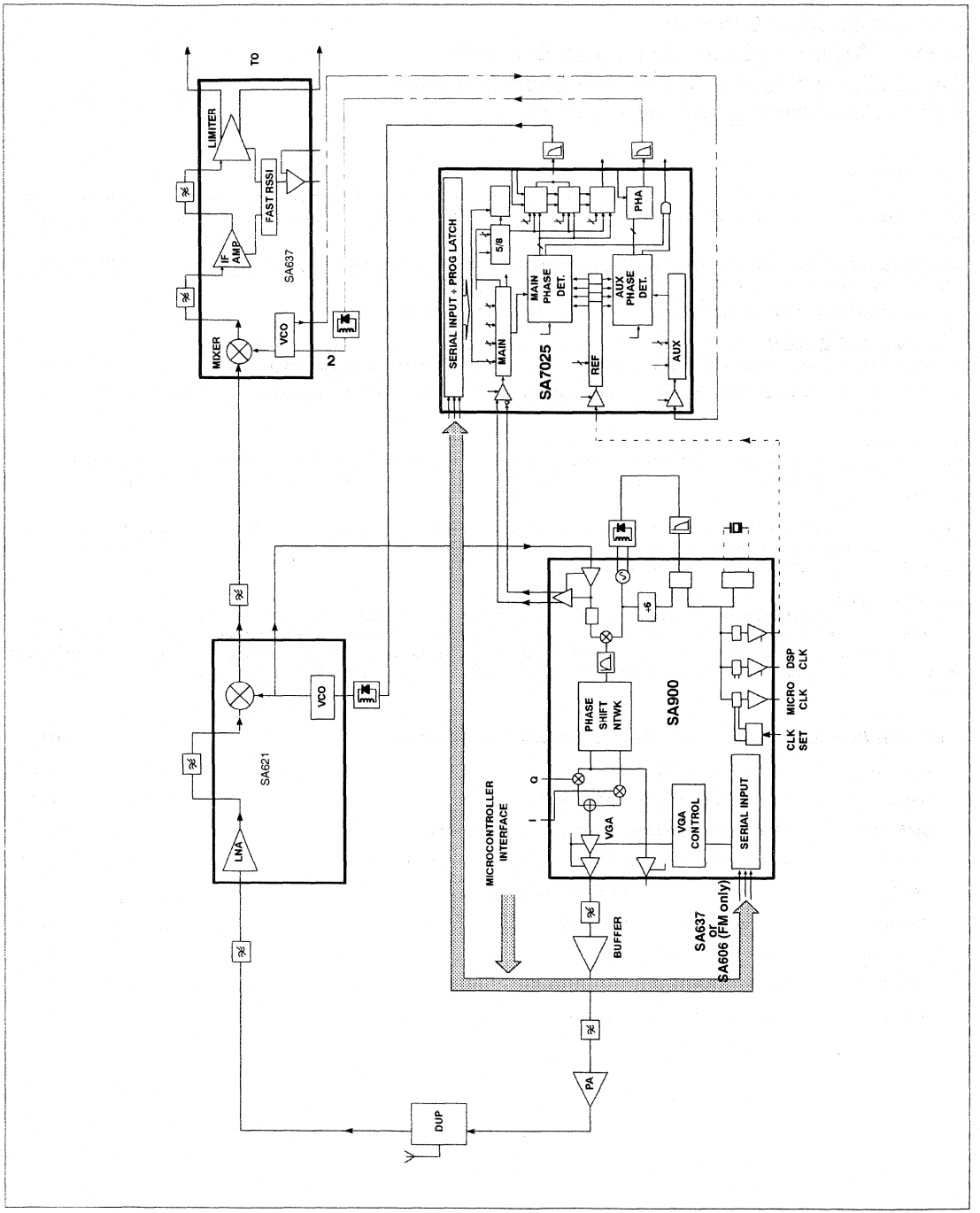
Although this is not the only IS-54/-136 solution, our 4-chip configuration is the most integrated and easy to use chip-set available today. For example, the SA900 provides I/Q modulators, the phase shifter, the VGA, a filter, control logic, clock distribution and more in a single IC. The need for two RF synthesizers was eliminated by closely coupling the SA7025 and the SA900 so it is possible to use the main synthesizer to simultaneously generate receive and transmit signals. The integration and connectivity of the chip-set promote significant cost reduction. In addition this integrated solution reduces the time to a final product by simplifying the design effort. The result is a smaller, cost effective, low-power phone that is ultimately more attractive to the end users.

Moving to a digital standard not only provides for increase in capacity, but offers the advantages of service integration. With the use of a digital modulation, other services such as data and fax can also be handled more easily over this system.

The Philips Semiconductors IS-54/-136 TDMA RF transceiver chipset consists of the following ICs: **IC17 Page**

SA621	1GHz low voltage LNA, mixer and VCO	4–147
SA606	Low voltage high performance mixer FM/IF system	6–97
SA637	Low-voltage digital IF receiver	6–249
SA7025	Low-voltage 1GHz fractional-N synthesizer	7–24
SA900	I/Q transmit modulator	8–13

IS-54/-136 TDMA Digital Cellular



AMPS/(E)TACS/CDPD Analog Cellular

Analog Cellular Chipset
AMPS (Advanced Mobile Phone Service)
TACS (Total Access Communication System)
CDPD (Cellular Digital Packet Data)

AMPS/ETACS

The analog cellular market is a consumer market with heavy price pressures on handsets and components. Analog cellular is still the worlds largest cellular system. Development in analog cellular handsets still continues at a faster pace, offering more features, lowering prices and more models.

Manufacturers of handsets face shorter product life cycles, faster Time–to–Market (TtM) and rapidly decreasing market prices. With Philips' long–time experience in analog cellular, our chipset presents a proven solution.

New ICs in the chipset are developed in order to meet market demand for lower cost and faster TtM.

Current AMPS/ETACS

Our chipset uses proven 3V technology to improve power–consumption of a hand–held phone, thus improving talk–time and standby–time.

The chipset is supported by a software package (source–code), consisting of protocol stack and examples for Man–Machine–Interface (MMI) and device drivers.

RF Transceiver

The transceiver section consists of 4 low–voltage, low–power ICs: For the Front–End, either the SA611 or SA621 can be used. Both have high–performance LNA and mixer on–chip. In addition, the SA621 contains an oscillator. With only an external resonator circuit, the SA621 can be configured as a VCO.

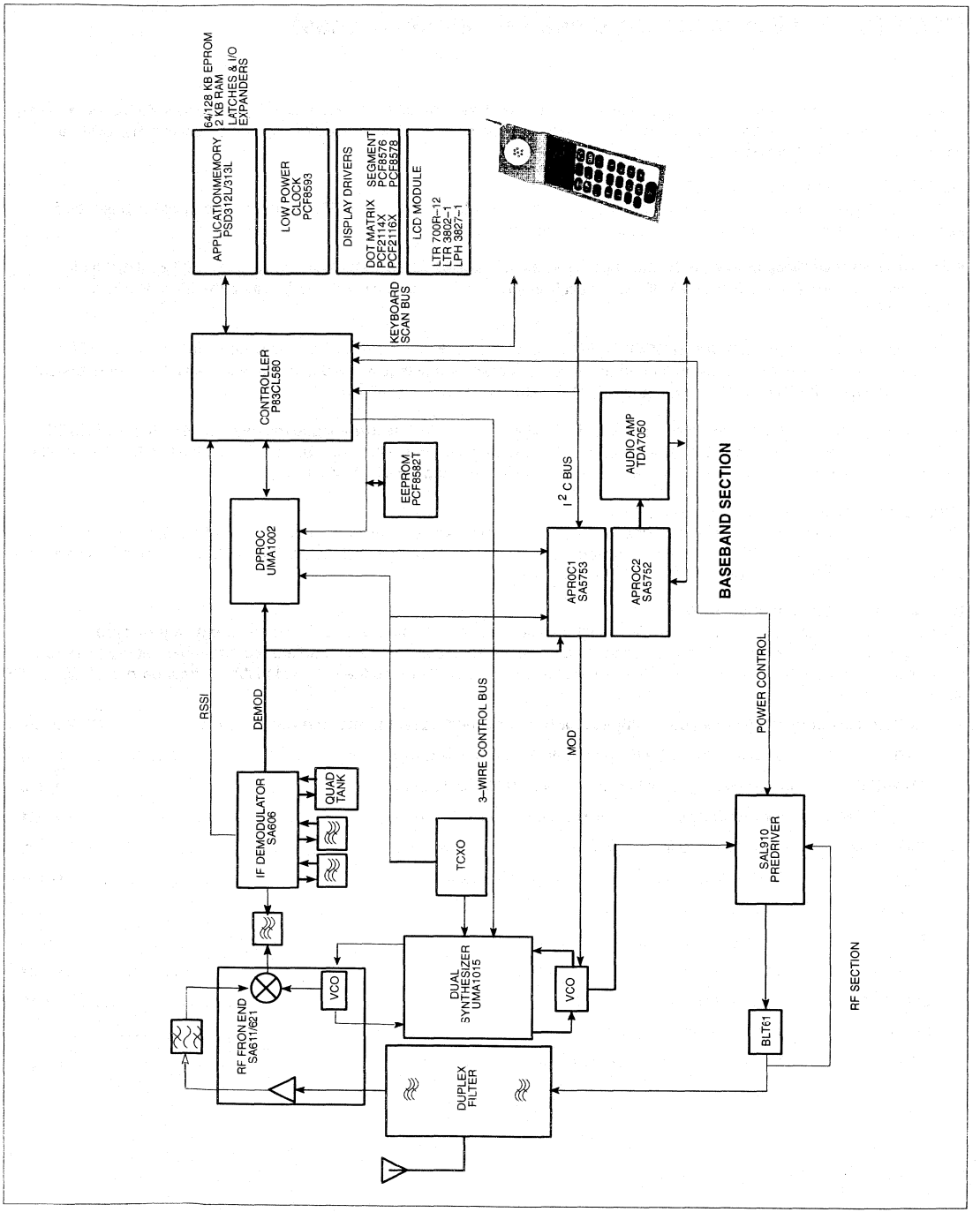
For the FM–IF, either the SA606 or the SA616 can be used. Both down–convert the 1st IF signal to provide the audio/data RSSI signals. The UMA1015 dual frequency synthesizer locks the receive and transmit VCOs. In the PA section, the SA910 is the low–voltage, high efficiency, pre–driver IC for the output power transistor (eg. BLT61).

Baseband Section

The AMPS/(E)TACS baseband solution handles all audio and data processing, control and memory functions. The SA5752, SA5753 audio processors and TDA7050 audio amplifier provide companding, VOX, filtering, amplification and control functions needed to meet AMPS and (E)TACS system requirements. The UMA1002 low voltage data processor incorporates all of the necessary data transceiving, processing and SAT functions. The P83CL580 8-bit microcontroller, PCF8582T EEPROM and PSD312L EPROM provide the control and memory for the entire handset.

The Philips Semiconductors AMPS/(E)TACS/CDPD chipset consists of:		IC17 Page
SA611/621	Low voltage LNA and mixer - 1GHz	4–30
SA606	Low-voltage high performance mixer FM IF system	6–97
UMA1015M	Low-power dual frequency synthesizer for radio communications	7–142
SA5752	Audio processor - companding, VOX and amplifier section	9–45
SA5753	Audio processor - filter and control section	9–55
UMA1002	Data processor for cellular radio (DPROC2)	9–537
P83CL580	8-Bit Microcontroller	12–74
TDA7050	Audio amplifier	8–81
SA910	Variabe gain RF predriver amplifier	8–43

AMPS/(E)TACS/CDPD Analog Cellular



DECT (Digital European Cordless Telephone) Chipset

DECT

The Philips Semiconductors chip-set for Digital European Cordless Telecommunication (DECT) is intended for use in a variety of wireless office and residential communications products. The chip-set is comprised of low-power ICs which provide a complete solution for both baseband and RF.

DECT office-communication chip-set

The Philips Semiconductors low-voltage DECT PCD504X Burst-Mode Controller (BMC) forms the heart of the baseband section in base-stations and handsets. It communicates with the:

- The RF transceiver incorporates a double superheterodyne receiver that is composed of the UMA1020 2 GHz double frequency synthesizer and SA639 FM IF. Our next front-end product, the UAA2067, will include the LNA, VCOs and preamplifier.
- The speech interface to our ADPCM CODEC (PCD5032) for encoding/decoding (G721) is in compliance with CCITT recommendations. Philips Semiconductors advanced bitstream technology is used to achieve the A/D & D/A conversion. The serial DSP interface can be connected to a DSP with echo control algorithms.
- The microcontroller interface is suited to one of the Philips Semiconductors low-voltage microcontrollers: the P80CL782 (8051-core), the P83CLXXX (8051-core), the P90CL301 (68K-core) and in the near future, the 16-bit P87C51XA (80C51XA core) microcontrollers. These execute the upper layer software of the DECT protocol.

Domestic and small-business systems

For this rapidly growing market, samples of a new IC family will be available by the end of 1994: the PCD509X series. A PCD509X combines the ADPCM, BCM and microcontroller in a single IC, hence its name, the "ABC chip". The RF interface will be upwardly compatible with the PCD504X family.

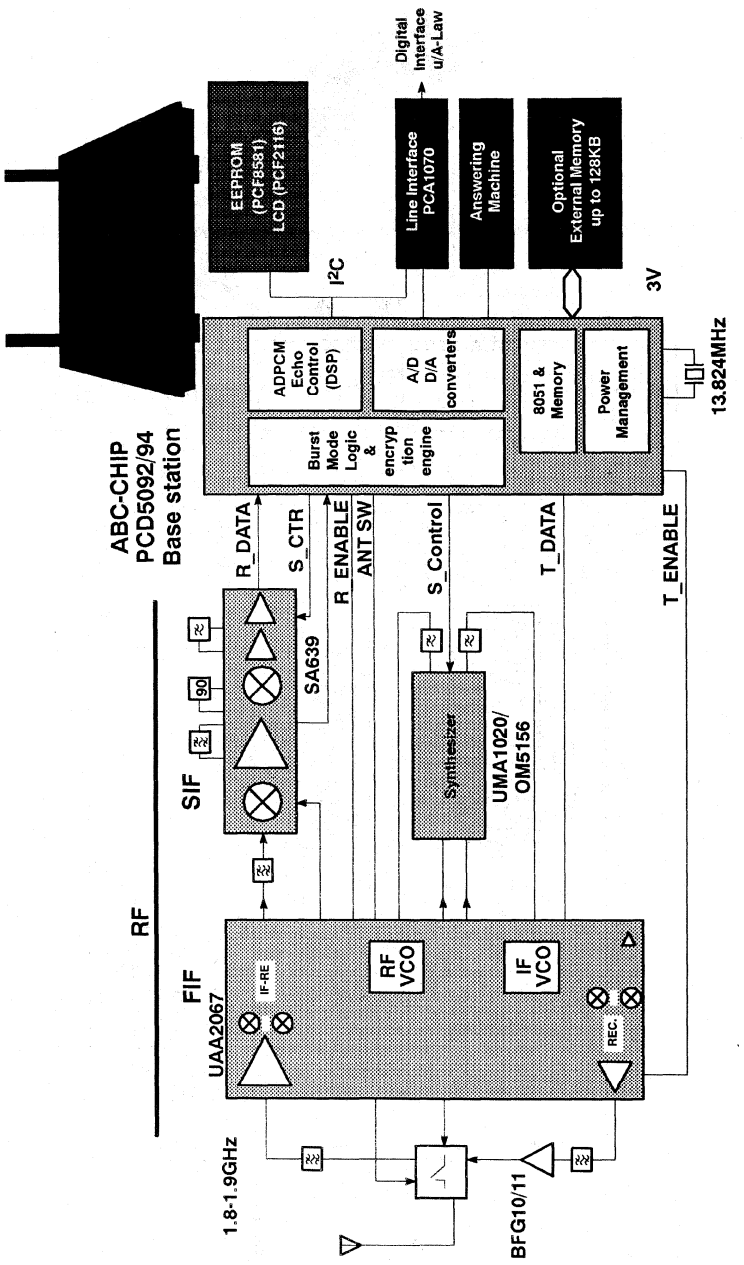
Evaluation kit supports design-in

Philips Semiconductors offers a kit (OM4756) which can be used to evaluate the DECT chip-set and as a prototype development tool. It includes an operating manual, a complete base-station and a complete rechargeable-battery-powered remote unit (hand-held). The latter comprises a baseband section built around the PCD5041 BMC, a keyboard, an LCD, an RF section and a handset.

Philips Semiconductors offers a DECT chipset for handsets and basestations that consists of:		IC17 Page
SA639	Low voltage mixer FM IF system with filter amplifier and data switch	6–260
UAA2067G	Image rejecting 1800MHz transceiver for DECT applications	4–173
UMA1020AM	Low-voltage dual frequency synthesizer for radio telephones	7–221
UMA1020M	Low-voltage dual frequency synthesizer for radio telephones	7–233
PCD5032	ADPCM (G721) codec for digital cordless telephone	9–191
PCD3311	DTMF Generator (basestation)	IC03
PCA1070	Line Interface (basestation)	IC03
PCD5041	DECT burst mode controller (handset)	9–202
BFG540/10/11	RF Power Amplifier	SC10
P80CLxxx	Low voltage microcontroller	IC20
PCD5042	DECT burst mode controller (base-station)	9–220

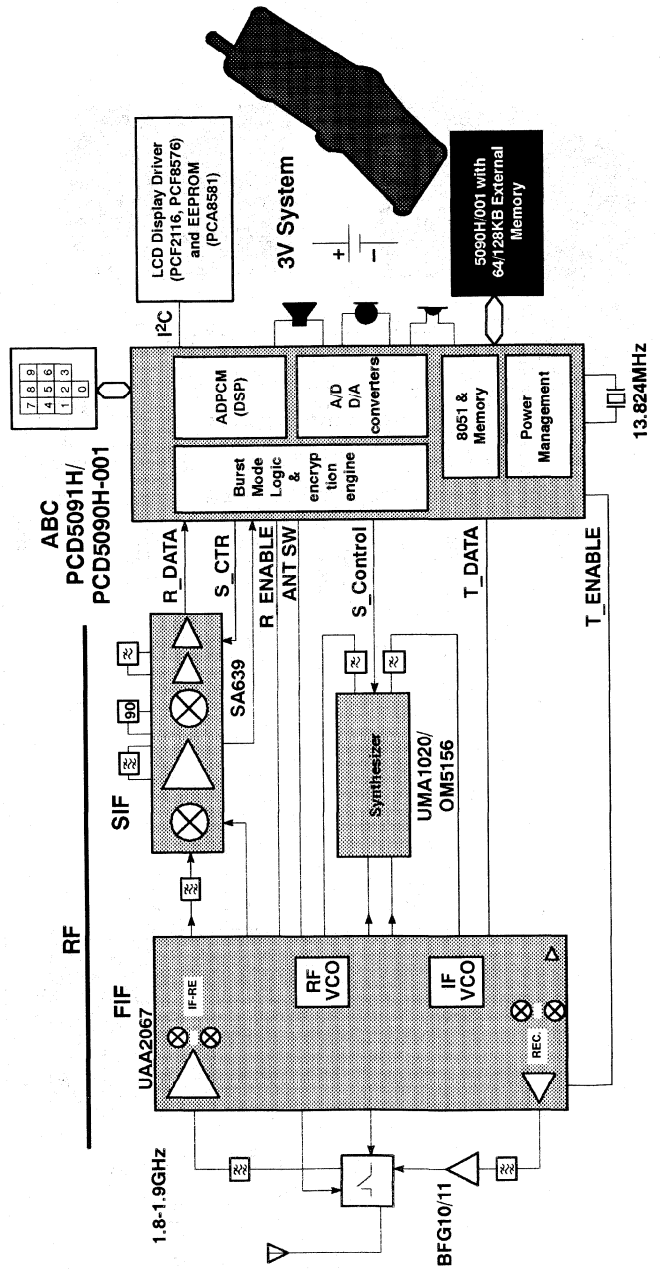
DECT Digital Cordless

DECT Base-station with a Double Superheterodyne RF Receiver



DECT Digital Cordless

DECT Handset with a Double Superheterodyne RF Receiver



CT0 Analog Cordless Chipset

CT0

This low-frequency analog cordless standard is established in many countries at various frequencies around 50MHz, including:

- France (26/41 MHz)
- Australia (30/39 MHz)
- The Netherlands & Spain (31/40 MHz)
- China, S. Korea, Taiwan, USA, Latin America (46/49 MHz)
- China (48/74 MHz).

As this market continues to grow (in terms of countries and increasing user density), our complete module/chip-set system approach to CT0 offers a low-cost solution with a number of advantages over competitors:

- It is an auto-scan, multiple-channel access (MCA) system: the base station and handset(s) automatically detect and select a free channel for incoming and outgoing calls
- 8 of the most commonly used CT0 frequency tables are incorporated in the standard chip-set, consequently software changes are not required
- One base-station unit can operate up to eight handsets.

System design is based on an advanced communication protocol using MSK (minimum shift keying) at 1200bps. This means high spectral efficiency and low-energy harmonics. Moreover, communication between base unit and handset features:

- A 20-bit security code (factory or user programmable)
- 2-way paging and 2-way intercom
- Call transfer between base unit & handset OR handset & handset
- Noise reduction for high audio performance
- DTMF/pulse dialling, or mixed-mode dialling.

The base-station unit offers a full-function speaker phone with keypad for use without handset, and a last number redial memory of 32 digits. It also includes a repertory dial memory (10 numbers of 24 digits, or 10 numbers of 16 digits + 3 emergency 28-digit numbers) and a music-on-hold facility.

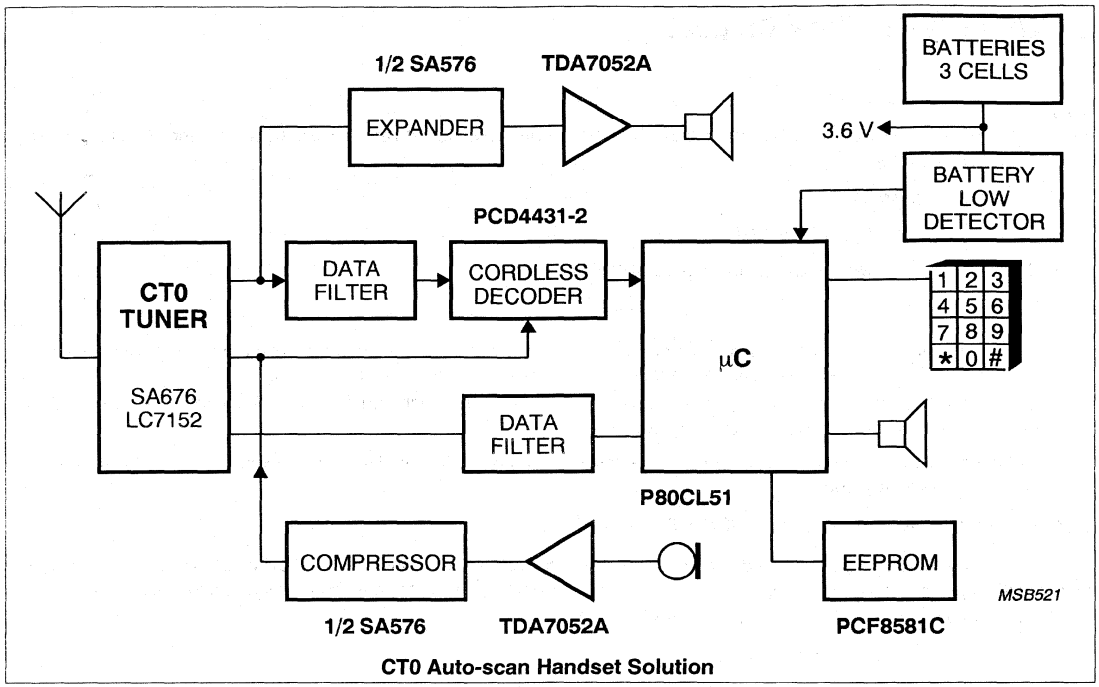
The handset design incorporates an advanced power-saving algorithm to achieve a *12-day standby time*. With the same number memory facilities as the base station, it also includes a low-battery warning, an out-of-range warning and a back-light for night use.

Evaluation kit

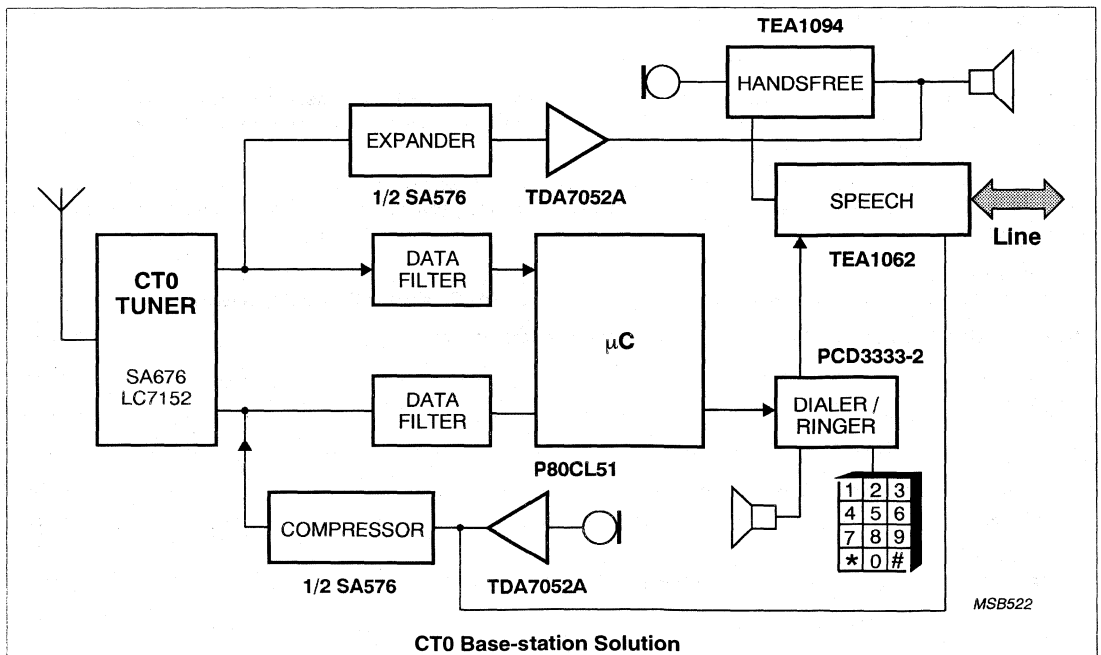
Demo/evaluation boards are available to cover all CT0 frequencies (type OM4760-X; X = country version).

The Philips Semiconductors CTO chipset consists of the following ICs:		IC17 Page
SA676	Low-voltage mixer FM IF system	6–129
NE/SA576	Low power compandor	10–45
PCD4431-2	Cordless Decoder (handset)	IC03
PCD3333-2	Cordless Decoder (basestation)	IC03
TEA1094	Handsfree Speaker Phone Amplifier (basestation)	9–464
TEA1062/ TEA1062A	Speech and Line Interface (basestation)	IC03
P80CL51	Microcontroller	IC20
TDA7052A/AT	1-Watt low voltage audio power amp with DC volume control	IC03

CT0 Analog Cordless



CT0 Auto-scan Handset Solution



CT0 Base-station Solution

CT1/CT1+ Analog Cordless Chipset

CT1/CT1+

CT1 and CT1+ have been chosen as the analog cordless standard by PTTs in several European countries. Their choice was based on the CT1/CT1+ multi-channel capability and 900MHz frequency. The high-frequency used and smaller market for this standard has made CT1/CT1+ sets inherently more expensive than CT0. However, as CT0 now features a multi-channel capability, consumer pressure is forcing CT1/CT1+ price-reductions. A low-voltage, auto-scan MCA solution for CT1/CT1+ offers a highly competitive package:

- A full solution for CT1 and CT1+ with software/hardware modifications available on request, and help in obtaining PTT approval
- One base-station can operate up to six handsets
- Advanced communication protocol
- 21-bit security code (factory or user programmable)
- 2-way paging and 2-way intercom
- Call transfer between base unit & handset OR handset & handset
- Noise reduction for high audio performance
- DTMF/pulse dialling, or mixed-mode dialling
- Programmable country settings, for all European countries.

The base-station unit offers a full-function speaker phone with keypad for use without handset, and a last number redial memory of 23 digits. It also includes a repertory dial memory (10 numbers of 23 digits), a music-on-hold facility and a fast battery charger (< 4 hrs).

The handset features the same number-memory facilities as the base-station unit, out-of-range warning and low battery warning. Battery management assures a standby time of more than 24 hours, with the handset supporting fixed or replaceable batteries.

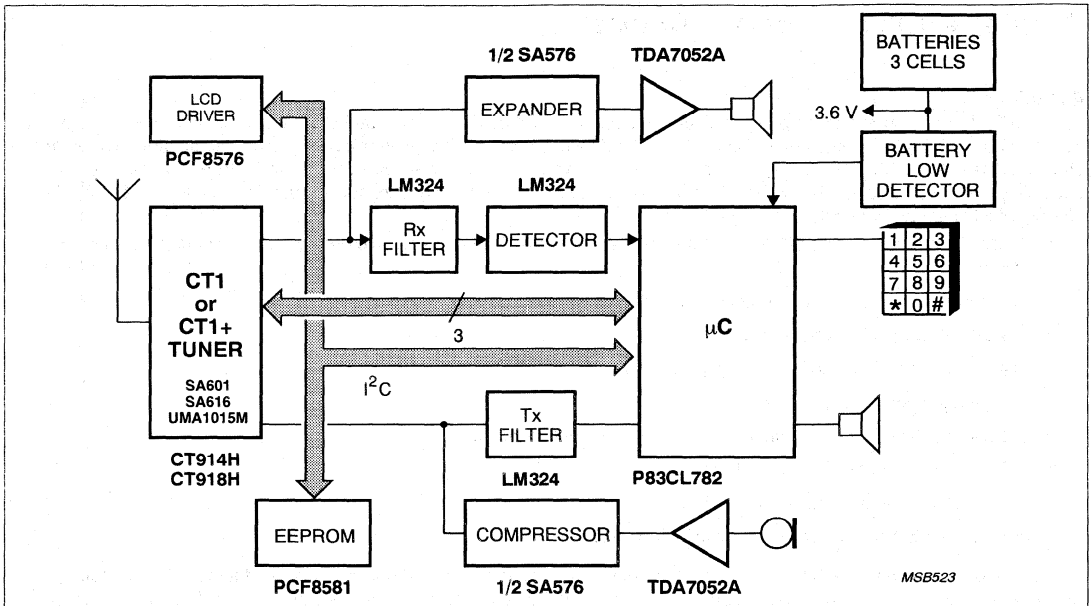
For CT1/CT1+, Philips also provide production-line testing software and service-engineer maintenance software.

Evaluation kits

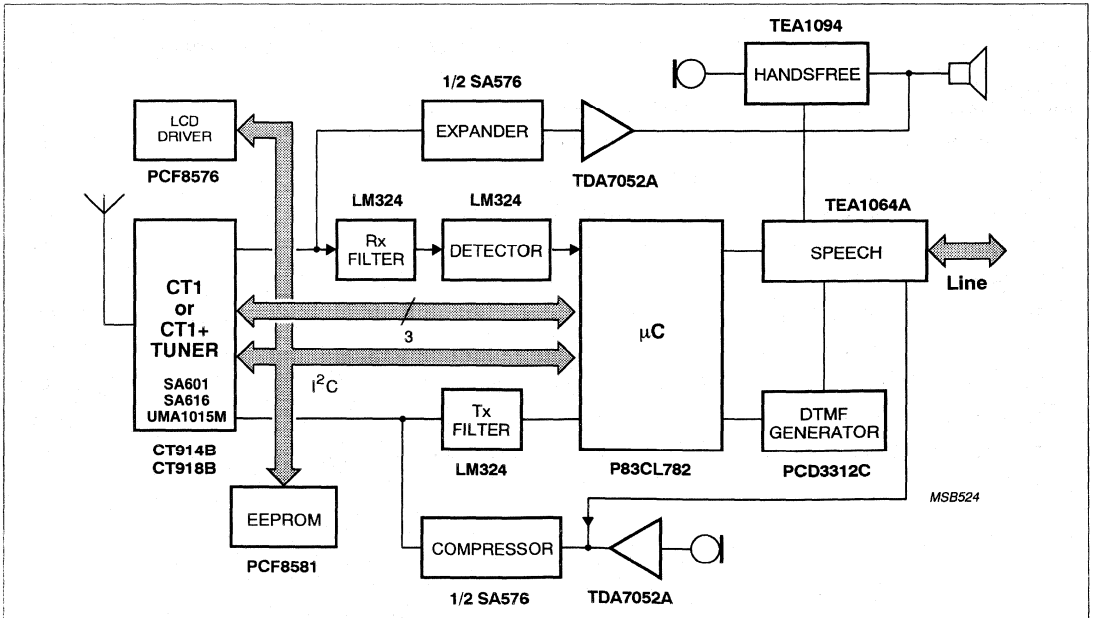
Demo/evaluation boards are available: type OM4743 for CT1 and type OM4744 for CT1+.

The Philips Semiconductors CT1/CT1+ chipset consists of:		IC17 Page
SA601	Low voltage LNA and mixer — 1GHz	4–19
SA616	Low voltage high performance mixer FM/IF system	6–113
UMA1015M	Low power dual frequency synthesizer for radio communications	7–142
NE/SA576	Low power compandor	10–45
PCD3312	DTMF generator	IC03
P83CL782	Low voltage microcontroller	IC20
TEA1064AT	Speech and Line Interface (base-station)	IC03
TEA1094	Handsfree Speaker Phone Amplifier (base-station)	9–464
TDA7052A/AT	1-Watt low voltage audio power amp with DC volume control	IC01

CT1/CT1+ Analog Cordless



CT1/CT1+ Handset Solution



CT1/CT1+ Base-station Solution

PAGERS

POCSAG

Because the pager market is characterized by customization, Philips Semiconductors does not offer a turnkey solution. However, Philips Semiconductors does provide two advanced chips for all the key functions of beep-only, numeric and alphanumeric pagers:

- The UAA2080 advanced pager receiver
- The PCF5001 POCSAG paging decoder.

Philips Semiconductors also provide application support on how to build complete pagers (the only extra components required are a microcontroller, memory, LCD module and real-time clock), and offer unrivalled application support, including evaluation kits.

UAA2080 advanced pager receiver

This is a high-performance low-power radio receiver circuit primarily intended for VHF and UHF (25 - 512MHz) wide-area (country-wide) digital pagers. With a high level of integration, this is currently the only chip available for use in very thin pagers (e.g., wrist-watch or credit card types). Employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK), the receiver is based on the direct conversion principle (zero IF). Operating up to 2400 baud, the UAA2080 is unique in its size, power consumption and performance advantages. Key features include:

- High integration level
- Wide frequency range
- Low power consumption
- High sensitivity
- High dynamic range
- Interfaces directly with the PCA5000A, PCF5001 and PCD5003 POCSAG decoders
- QFP32, SO28 package or naked chip.

The next generation UAA2082 will have two additional features: the low-battery detect voltage will be reduced from 2.05V to 1.1V; the internal oscillator will be disconnected when using direct injection from a frequency synthesizer, to further reduce current consumption.

PCF5001 POCSAG paging decoder

This is a fully integrated low-power decoder and pager controller. It decodes the CCIR radio paging Code No.1 at 512 and 1200 bits/s data rates and includes a digital input filter for high call success rates. Key features include:

- On-chip EEPROM storage
- Wide supply voltage range (1.5 - 6V)
- Very low supply current (60 mA with 76.8kHz crystal)
- Data rates up to 2400 bits/s possible
- Supports 4 user addresses (Receiver Identity Codes) in 2 independent frames
- Drives an LED, a magnetic or piezo ceramic beeper directly and offers optional vibrator type alerting
- Silent call storage (up to 8 calls).
- QFP32, SO28 package or naked chip.

PCF5003 new POCSAG paging decoder

The new PCD5003 is a very low power decoder and pager controller. It supports data rates of 512, 1200 and 2400 bps using a single 76.8kHz crystal. Its on chip EEPROM is programmable with a minimum supply of 2.5V. Key features are:

- Low operating current (50mA ON; 25mA OFF)
- 2-bit random and (optional) 4-bit burst address error correction
- Up to 6 user addresses (RICs), in 6 (max) different frames
- Standard POCSAG synchronization word, plus up to 4 user-programmable synchronization words

Pagers

- Received data inversion (optional)
- Synthesizer set-up and control interface (3-line serial)
- Separate power control or Receiver and RF oscillator for battery economy
- On-chip SRAM buffer for message data
- Direct and I²C-bus control of operating status (ON/OFF)
- Wake-up interrupt for microcontroller, programmable polarity
- Built-in data filter and bit clock recovery

Evaluation kits

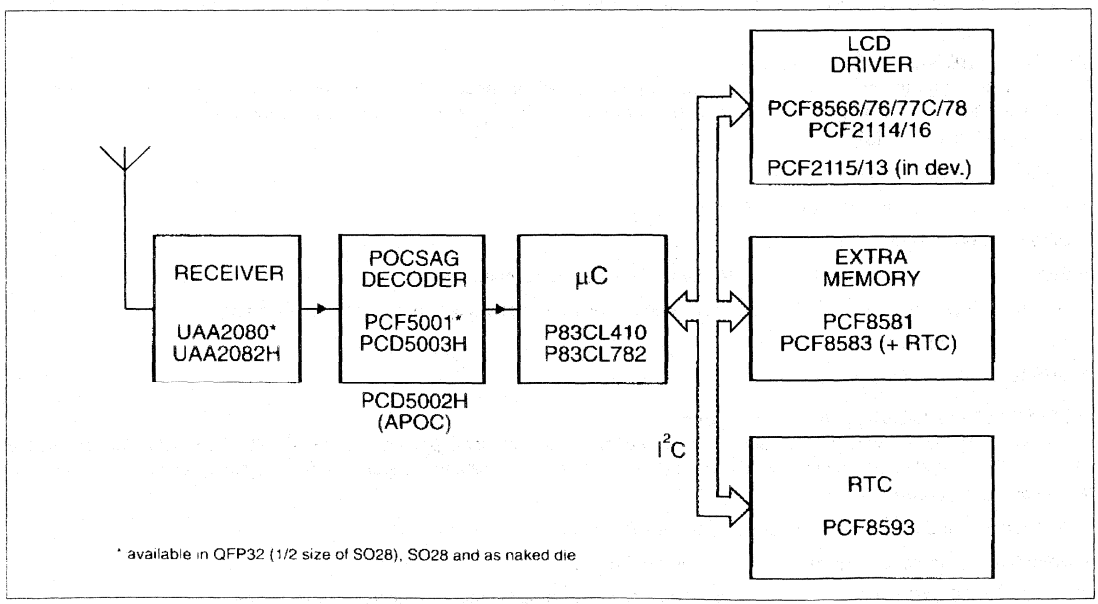
For the UAA2080 receiver, one may choose from four evaluation/demo boards:

- OM4745 for 173MHz
- OM4746 for 288MHz
- OM4747 for 470MHz
- OM4748 - frequency open.

For the PCF5001, Philips Semiconductors offers the OM4706 decoder evaluation/demo board and the OM4718 test program board. The latter allows monitoring of the decoder output from either a signal into the receiver, or a signal directly into the decoder.

Philips Semiconductors offers the following pager ICs: **IC-17 Page**

UAA2080T	Advanced pager receiver	4–288
UAA2082	Advanced pager receiver	4–293
PCD5003	Advanced POCSAG paging decoder	9–156
PCF5001	POCSAG paging decoder	9–84
P83CL410/782	Low voltage microcontroller	IC20



Section 4
Front–Ends and Paging

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SA601	1GHz low voltage LNA and mixer	4–20
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UAA2077AM	Image rejecting front-end for DECT applications	4–259
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UAA2077CM	2 GHz image rejecting front end	4–277
UAA2080	Advanced pager receiver	4–287
UAA2082	Advanced pager receiver	4–293

The Philips Family Of High Performance Front End Systems

	Description	V_{CC}	I_{CC}	Pins	Pkg	Input Frequency	Gain (power)	Noise Figure	Input IP3	1dB Comp.	Input Imped.	Output Imped.	Feature Highlights
Image Reject Front–end Systems								f_{RF}=2 GHz					
UAA2067G	LNA+IRM+Mod+VCO	3–5.5V	24mA (rx) 45MA (T_X)	32	BE	1.8–2.2 GHz	32 dB	6 dB	–25 dBm	–32dBm	50Ω	50Ω	—Image reject Mixing —DECT, DCS1800, GSM and US PCS
UAA2077AM	LNA+IRM	3.15–5.3V	27mA @4V	20	DK	1.8–2.2 GHz	20 dB	4.3 dB	–17 dBm	–22dBm	35Ω	1κ Ω	
UAA2077BM		3.6–5.3V	27mA @4V	20	DK	1.8–2 GHz	20 dB	4.3 dB	–17 dBm	–23dBm	35Ω	1κ Ω	
Image Reject Front–End Systems								f_{RF}=900 MHz					
UAA2072M	LNA+IRM+Mixer	4.5–5.3V	31.5mA@5V	20	DK	LNA+IRM 960 MHz	26 dB	4 dB	–15 dBm	–24.5dBm	200Ω	High	—Image reject mixer (30dN min) —T_x down–convert mixer
UAA2073M	Integrated Front–end	3.6–5.3V	26mA@3.75V	20	DK	960 MHz	23 dB	3.25 dB	–15 dBm	–23 dBm	150Ω	1kΩ	—30 dB min image rejection
Integrated Front–End Systems								f_{RF}=900 MHz					
NE/SA600	LNA+IRM+Mixer	4.5–5.5V	13mA/4.2mA* @5V	14	D	LNA 1/2 GHz	16/–7.5 dB*	2.2 dB	–10/+26dBm	–20 dBm	50Ω	50Ω	—LLNA Overload Mode —Excellent Noise Figure
						Mixer 1.2 GHz	–2.6 dB	14 dB	+6 dBM	–14 dB	50Ω	High	
NE/SA601	LNA+IRM+Mixer	42.7–5.5V	7.4mA@3V	20	DK	LNA 1/2 GHz	11.5 dB	1.6 dB	–2 dBm	–16 dBm	50Ω	50Ω	—Low voltage —Excellent Noise Figure
						Mixer 1.2 GHz	+6 dB	10 dB	–2 dBm	–13 dBm	50Ω	High	
SA620	LNA+Mixer+VCO	2.7–5.5V	10.4mA/7.2mA* @3V	20	DK	LNA 1/2 GHz	11.5/–7.5 dB*	1.6 dB	–3/+25 dBm*	–16 dBm	50Ω	50Ω	—Low voltage —Excellent Noise Figure —LNA Overload Mode —Internal VCO
						Mixer 1.2 GHz	+3dB	9 dB	–6 dBm	–13 dBm	50Ω	High	
SA611	LNA+Mixer	2.7–5.5V	8mA@3V	20	DK	LNA 1 GHz	15 dB	1.9 dB	–7 dB	–16 dBm	50Ω	50Ω	—Low voltage
						Mixer 1 GHz	9 dB	0.5 dB	4 dB	–9 dBm	50Ω	High	—Excellent system perf
SA621	LNA+Mixer+VCO	2.7–5.5V	13.3mA/10mA* @3V	20	DK	LNA 1 GHz	15dB	1.9 dB	–7 dB	–16 dB	50Ω	50Ω	—Low voltage
						Mixer 1 GHz	9 dB	10.5 dB	4 dB	–9 dB	50Ω	High	—Excellent system perf
Integrated Front–End Transceiver								f_{RF}=900 MHz					
SA1620	Rx: 2 LNAs w/atten.+mixer T_x: P_{OUT}=+8.5 dBm@2.7V+mixer	2.7–5.5V	R_x:28 mA T_x: 59 mA	48	BE	<1800 MHz	LNA 20 dB 8.5 dB	1.9 dB 10 dB	–5 dB 2 dB	–15 dBm –7.3 dBm	50Ω 50Ω	50Ω High	—LNA gain control range=59dB —Excellent noise Figure —T_x power adjustable
SA2420	Rx: LNA w/atten.+mixer T_x: Predriver+mixer	2.7–5.5V	R_x:21 mA T_x: 34 mA	24	DH	2.4–2.5 GHz	LNA 14 dB Mixer 8 dB	2.5 dB 11 dB	–6dBm 1 dBm	–17dBm –10 dBm	50Ω 50Ω	50Ω High	—low voltage —LNA gain atten. range=22dB —T_x P_{OUT}=0dBm
Mixer Systems								f_{RF}=45 MHz					
NE/SA602A	Mixer+Oscillator	4.5–8.0V	2.4mA@6V	8	N,D	500 MHz	17dB	5.0 dB	–13cBm	–25dBm	1.5kΩ	1.5kΩ	—Excellent Noise Figure —High Gain
NE/SA602A	Mixer+Oscillator	4.5–8.0V	2.4mA@6V	8	N,D	500 MHz	17dB	5.0 dB	–13cBm	–25dBm	1.5kΩ	1.5kΩ	—Excellent Noise Figure —High Gain

Temperature Range
NE: 0 to 70°C
SA: –40 to +85°C

D: Small Outline–14
Small Outline–16
Small Outline–20

Package Descriptions
DK: Shrink Small Outline Package (SSOP)–20
BE: Low Qaud Flat Paackage (LQFP)

N: Dual In–Line Plastic

*Amplifier: Enabled/Disabled

1GHz LNA and mixer NE/SA600

DESCRIPTION

The NE/SA600 is a combined low noise amplifier (LNA) and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 2dB noise figure at 900MHz with 16dB gain and an IM_3 intercept of -10dBm at the input. Input and output impedances are 50Ω and the gain is stabilized by on-chip compensation to vary less than ±0.5dB over the -40 to +85°C temperature range. The wide-dynamic-range mixer has a 14dB noise figure and IM_3 intercept of +6dBm at the input at 900MHz. Mixer input impedance is 50Ω with an open-collector output. The chip incorporates an option so the LNA can be disabled and replaced by a through connection. The amplifier IM_3 intercept increases to +26dBm in this mode; thus, large signals can be handled. The nominal current drawn from a single 5V supply is 13mA and 4.2mA in the LNA thru mode.

FEATURES

- Low current consumption: 13mA nominal, 4.2mA in the LNA thru mode
- Excellent noise figure: 2dB for the amplifier and 14dB for the mixer at 900MHz
- Excellent gain stability versus temperature
- Switchable overload capability
- Amplifier matched to 50Ω
- Mixer input matched to 50Ω
- Oscillator input matched to 50Ω

PIN CONFIGURATION

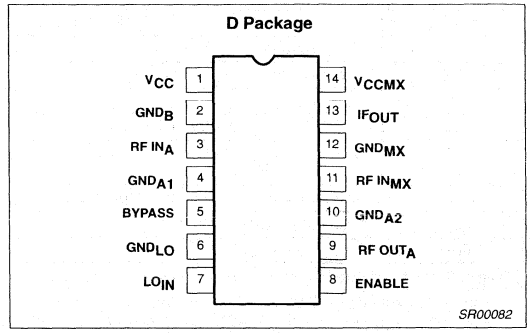


Figure 1. Pin Configuration

APPLICATIONS

- 900MHz front end for GSM/AMPS/TACS/ hand-held units
- RF data links
- UHF frequency conversion
- Portable radio
- Spread spectrum receivers
- 900MHz cordless phones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to +70°C	NE600D	SOT108-1
14-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA600D	SOT108-1

BLOCK DIAGRAM

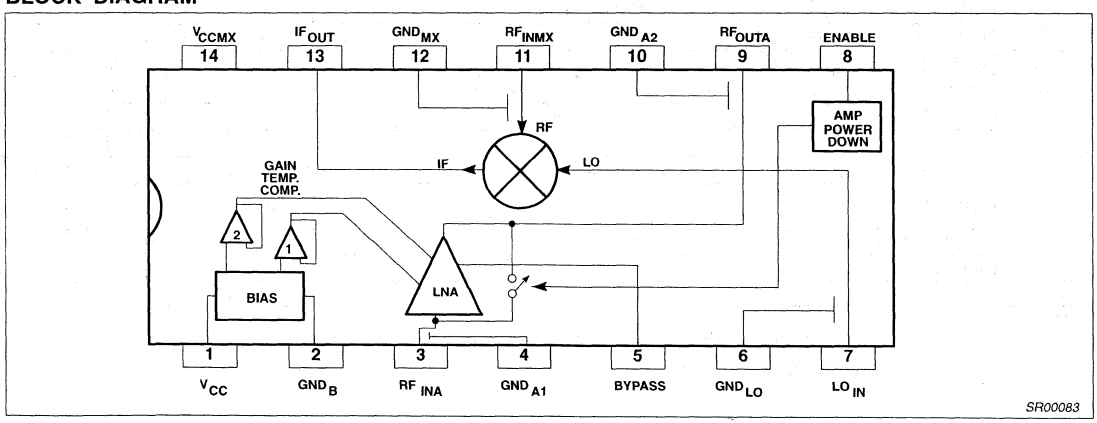


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}, V_{CCMX}	Supply voltage[1]	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC}+0.3)	V
ΔV	V_{CC} to V_{CCMX}	-0.3 to +0.3	V
ΔG	Any GND pin to any other GND pin	-0.3 to +0.3	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 14-Pin Plastic SO	 980	 mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 9V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   14-Pin SO: θ_{JA} = 125°C/W
3. CAUTION: The NE/SA600 is built on a BiCMOS process and is sensitive to electrostatic discharge.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}, V_{CCMX}	Supply voltage	4.5 to 5.5	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS[1,2]

V_{CC} = V_{CCMX} = +5V, T_A = 25°C; Test Figure 1, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
I_{CC}	Supply current (Pin 1, 13, 14)	Enable input high	10	11	13.0	15	16	mA
		Enable input low	3.2	3.6	4.2	4.8	5.2	
V_T	Enable logic threshold voltage		1.12	1.17	1.27	1.37	1.42	V
V_{IH}	Logic 1 level: LNA gain mode		2.0				V_{CC}	V
V_{IL}	Logic 0 level: LNA thru mode		–0.3				0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1		0		1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1		0		1	µA
V_{LNA-IN}	LNA input bias voltage	Enable input high			0.78			V
$V_{LNA-OUT}$	LNA output bias voltage	Enable input high			1.27			V
V_{BY}	LNA bypass bias voltage	Enable input high			1.05			V
V_{MX-IN}	Mixer RF input bias voltage				1.43			V
V_{LO-IN}	Mixer LO input bias voltage				3.35			V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the NE/SA600.
2. Standard deviations are estimated from design simulations to represent manufacturing variations over the life of the product.

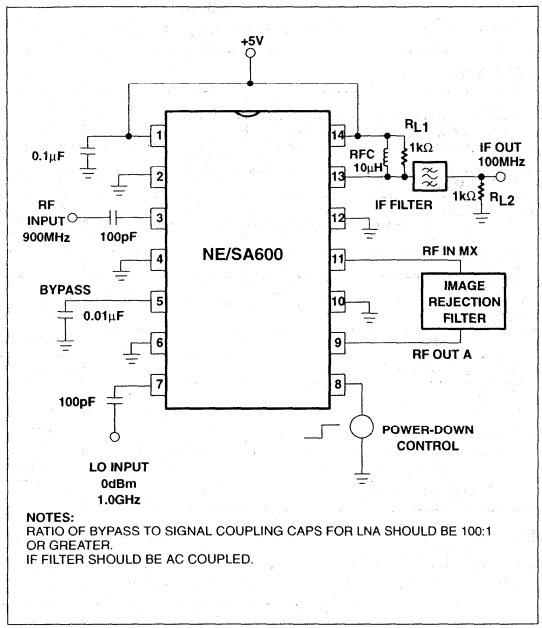
AC ELECTRICAL CHARACTERISTICS[1,2]

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNITS
				–3σ	TYP	+3σ	
LNA (V_{CC} = V_{CCMX} = +5V, T_A = 25°C; Enable = Hi, Test Figure 1, unless otherwise stated.)							
S_{21}	Amplifier gain	900MHz		14.9	16	17.1	dB
S_{21}	Amplifier gain in thru mode	Enable = LO, 900MHz		–9.0	-7.5	–6.0	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled	900MHz			-0.008		dB/°C
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity in thru mode	Enable = LO, 900MHz			-0.014		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz			-0.014		dB/MHz
S_{12}	Amplifier reverse isolation	900MHz		–47	-42	–37	dB
S_{11}	Amplifier input match[3]	900MHz		–11	-10	–9	dB
S_{22}	Amplifier output match	900MHz		–16.8	-15	–13.2	dB
P_{-1dB}	Amplifier input 1dB gain compression	900MHz		–21.2	-20	–18.8	dBm
IP_3	Amp input 3rd-order intercept	Test Fig. 2, 900MHz		–11.6	-10	–8.6	dBm
	Amp input 3rd-order intercept (thru mode)	Test Fig. 2, 900MHz, Enable = LO			+26		dBm
NF	Amplifier noise figure	900MHz		1.9	2.2	2.5	dB
	Amp noise figure w/shunt 15nH inductor at input	900MHz		1.7	2.0	2.3	dB
t_{ON}	Amplifier turn-on time	Enable Lo → Hi	Coupling = 100pF		30		µs
			Coupling = 0.01µF		3		ms
t_{OFF}	Amplifier turn-off time	Enable Hi → Lo	Coupling = 100pF		10		µs
			Coupling = 0.01µF		1		ms
Mixer (V_{CC} = V_{CCMX} = +5V, T_A = 25°C, Enable = Hi, f_{LO} = 1GHz @ 0dBm, f_{RF} = 900MHz, f_{IF} = 100MHz, Test Fig. 1, unless otherwise stated)							
VG_C	Mixer voltage conversion gain	R_{L1} = R_{L2} = 1kΩ		9.5	10.4	11.3	dB
PG_C	Mixer power conversion gain	R_{L1} = R_{L2} = 1kΩ		–3.05	–2.6	–2.15	dB
S_{11RF}	Mixer input match	900MHz		–23	-20	–17	dB
NF_M	Mixer SSB noise figure	Test Fig. 3, 900MHz, f_{IF} = 80MHz		12.2	14	15.8	dB
P_{-1dB}	Mixer input 1dB gain compression	900MHz		–5.3	-4	–2.7	dBm
IP_{3INT}	Mixer input third order intercept	900MHz		+5	+6	+7	dBm
IP_{2INT}	Mixer input second order intercept	900MHz		+18	+20	+22	dBm
G_{RFM-IF}	Mixer RF feedthrough	900MHz, C_{IF} = 3pF			–7		dB
G_{LO-IF}	Mixer LO feedthrough	900MHz, C_{IF} = 3pF			-10		dB
G_{LO-RFM}	Local oscillator to mixer input feedthrough	900MHz			-33		dB
S_{11LO}	LO input match	900MHz		–24	–20	–16	dB
G_{LO-RF}	Local oscillator to RF input feedthrough	900MHz			-46		dB
$G_{RFO-RFM}$	Filter feedthrough	900MHz			-39		dB
LNA + Mixer (V_{CC}=V_{CCMX}=+5V, T_A=25°C, Enable=Hi, f_{LO}=1GHz @ 0dBm, f_{RF} = 900MHz, f_{IF} = 100MHz, Test Fig. 1, unless otherwise stated)							
PG_C	Overall power conversion gain				13.4		dB
NF	Overall noise figure				3.5		dB
IP_3	Overall input 3rd-order intercept				–13		dBm

NOTE:

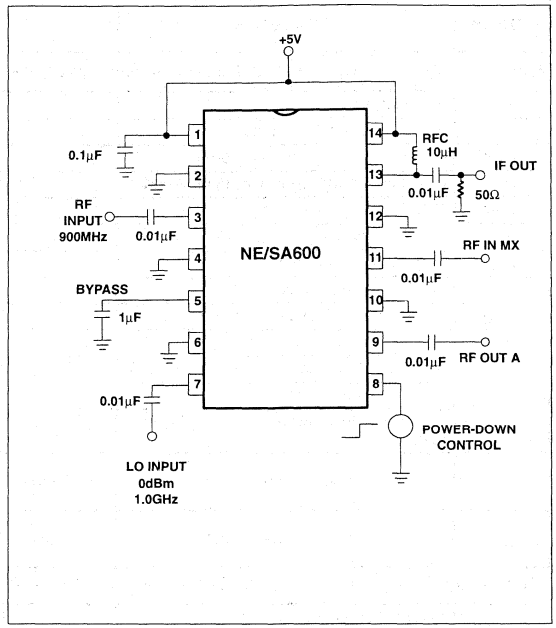
1. All meausrements include the effects of the NE/SA600 Evaluation Board (see Figure) unless otherwise noted. Measurement system impedance is 50Ω.
2. Standard deviations are estimated from design simulations to represent manufacturing variations over the life of the product.
3. With a shunt 15nH inductor at the input of the LNA, the value of S_{11} is typically –15dB.

TYPICAL APPLICATION

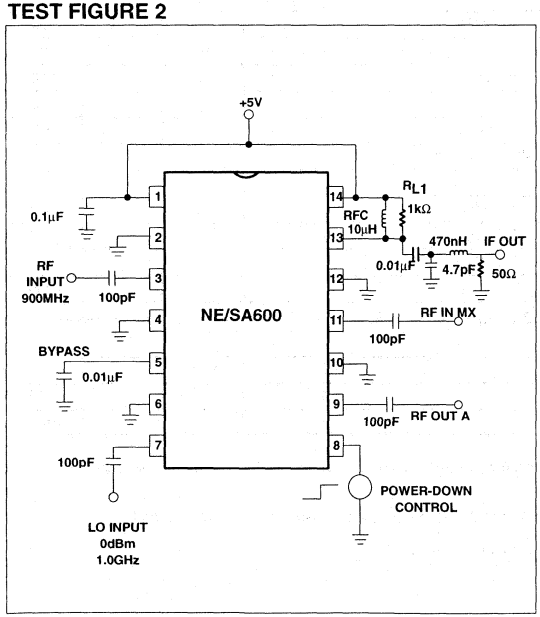


NOTES:
RATIO OF BYPASS TO SIGNAL COUPLING CAPS FOR LNA SHOULD BE 100:1 OR GREATER.
IF FILTER SHOULD BE AC COUPLED.

TEST FIGURE 1



TEST FIGURE 2



TEST FIGURE 3

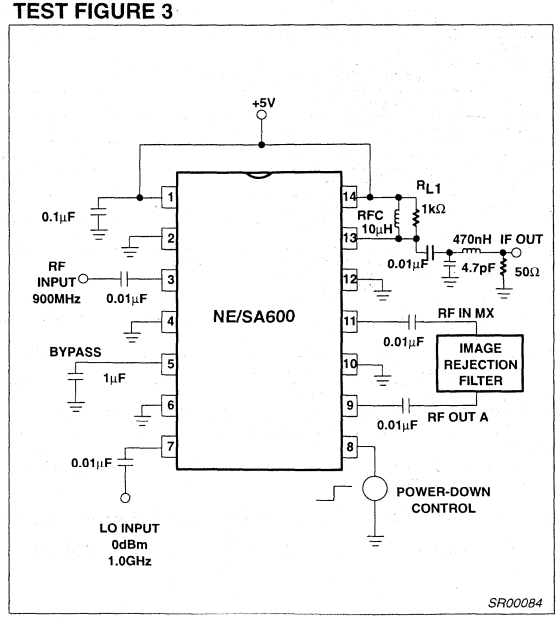


Figure 3. Test Application and Test Figures 1, 2 and 3

NOTE: All performance curves include the effects of the NE/SA600 evaluation board.

LNA S21 CHARACTERISTICS $4.5V \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Figure 1, unless otherwise specified.

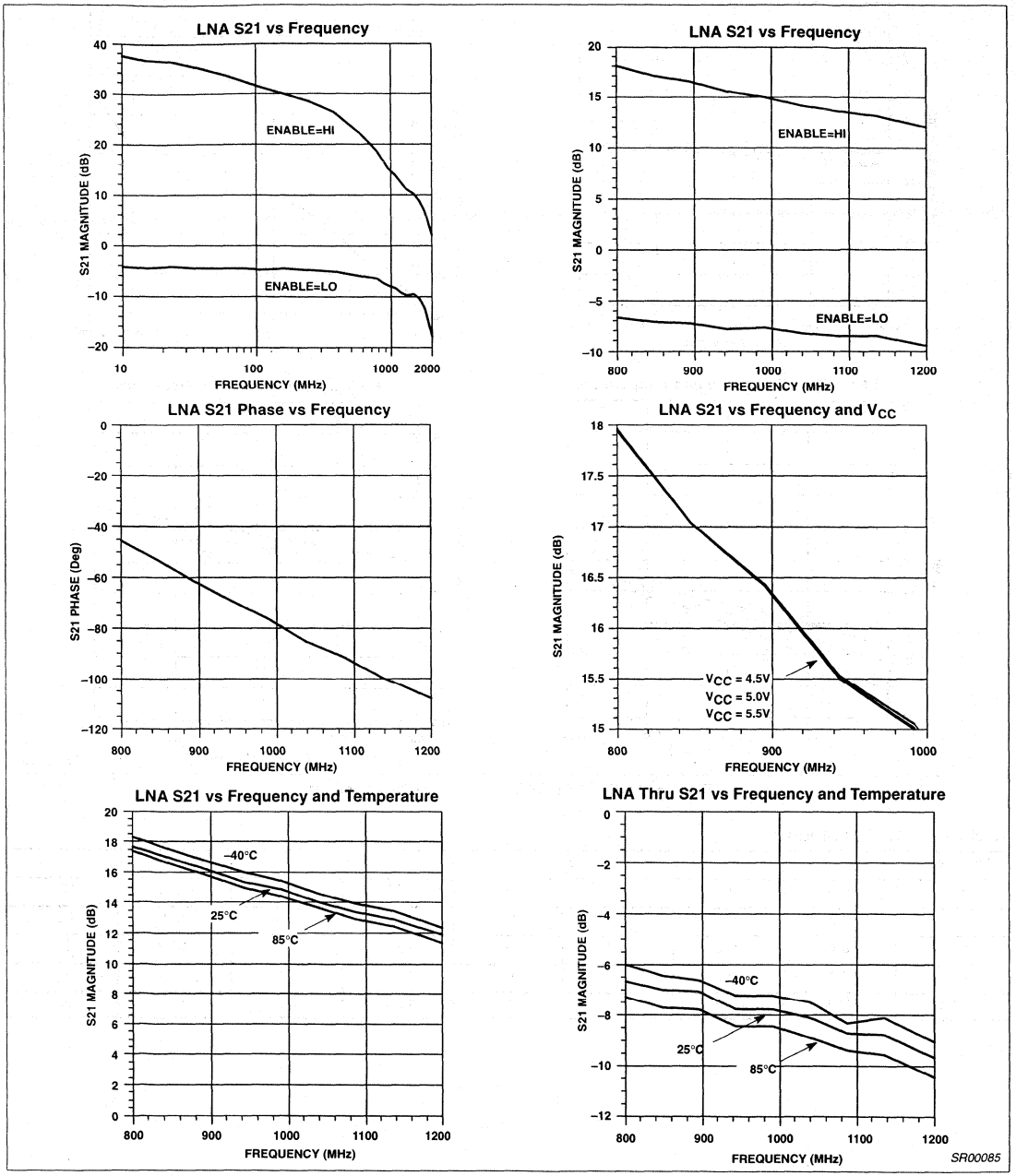


Figure 4. LNA S21 Performance Characteristics

LNA S11/S12/S22 CHARACTERISTICS $4.5V \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Figure 1, unless otherwise specified.

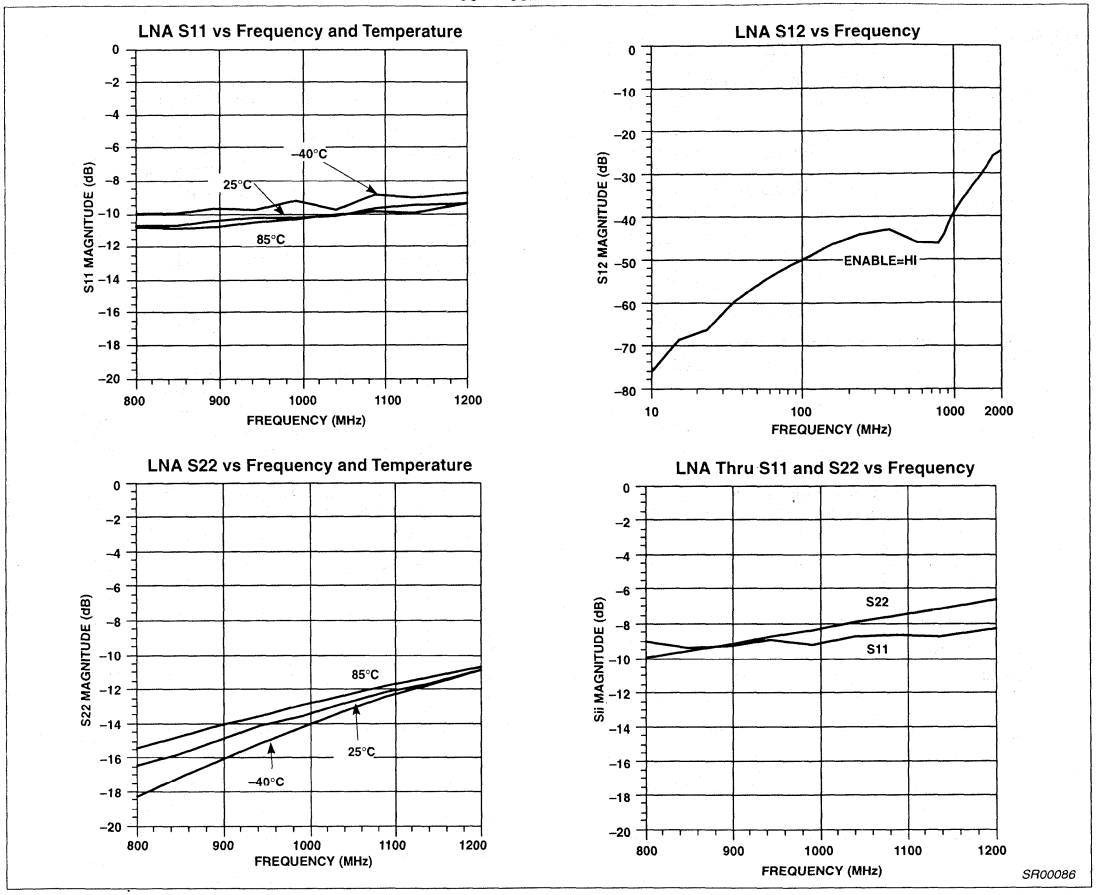


Figure 5. LNA S11/S12/S22 Performance Characteristics

Table 1. S-Parameters

Freq. MHz	S_{11}		S_{12}		S_{21}		S_{22}	
800	-9.5	-160	-46	8	17.9	125	-18.0	151
900	-9.5	-172	-43	19	16.4	105	-15.8	122
1000	-9.4	-173	-40	17	15.1	88	-14.0	98
1100	-9.1	-200	-37	12	13.8	70	-12.4	77
1200	-8.9	-216	-35	1	12.9	55	-11.1	58

LNA OVERLOAD/NOISE/DISTORTION CHARACTERISTICS

4.5V ≤ V_{CC} = V_{CCMX} ≤ 5.5V, Test Fig. 1, unless otherwise specified.

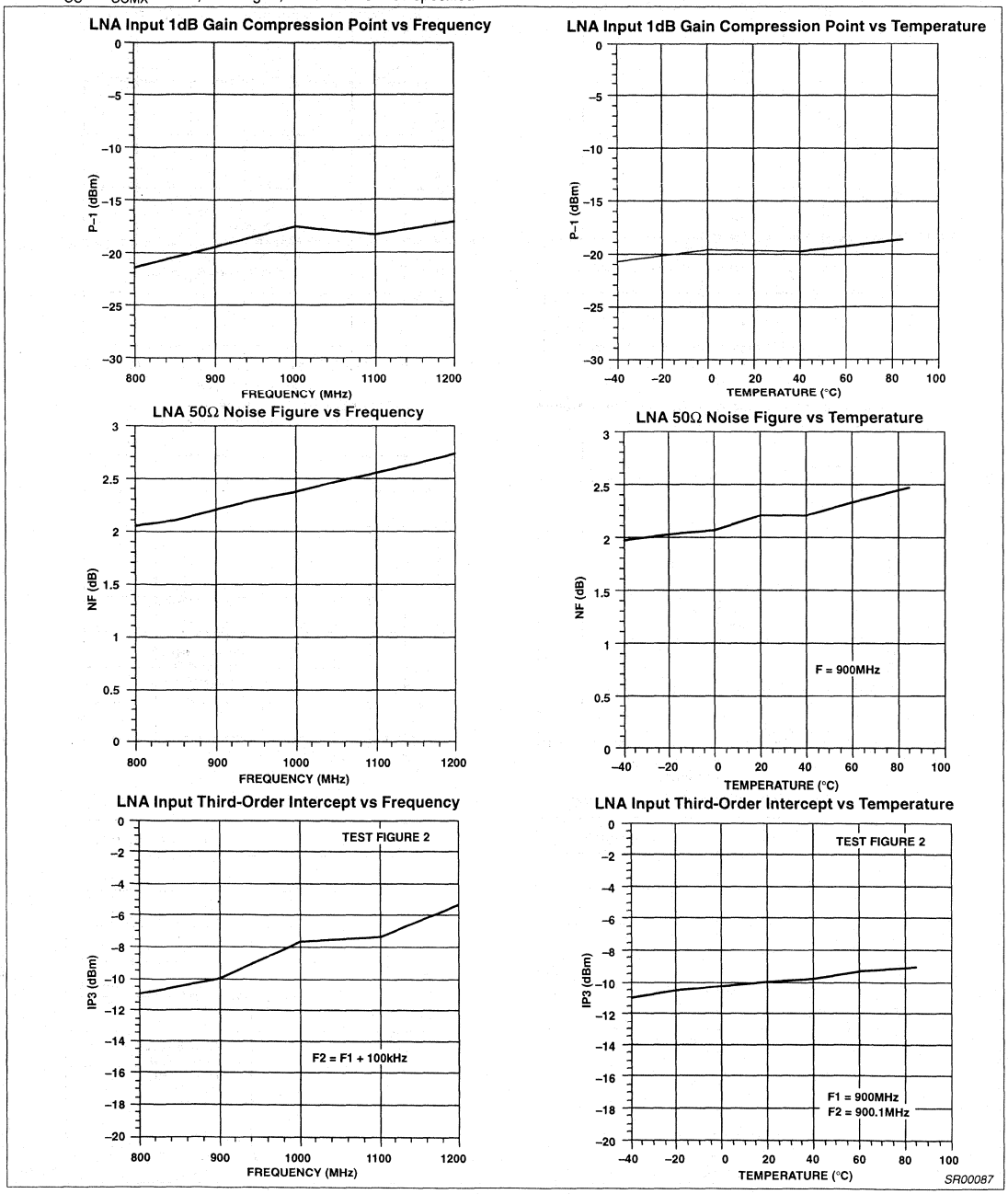


Figure 6. LNA Overload/Noise/Distortion Performance Characteristics

MIXER GAIN/NOISE CHARACTERISTICS $4.5V \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Figure 1, unless otherwise specified.

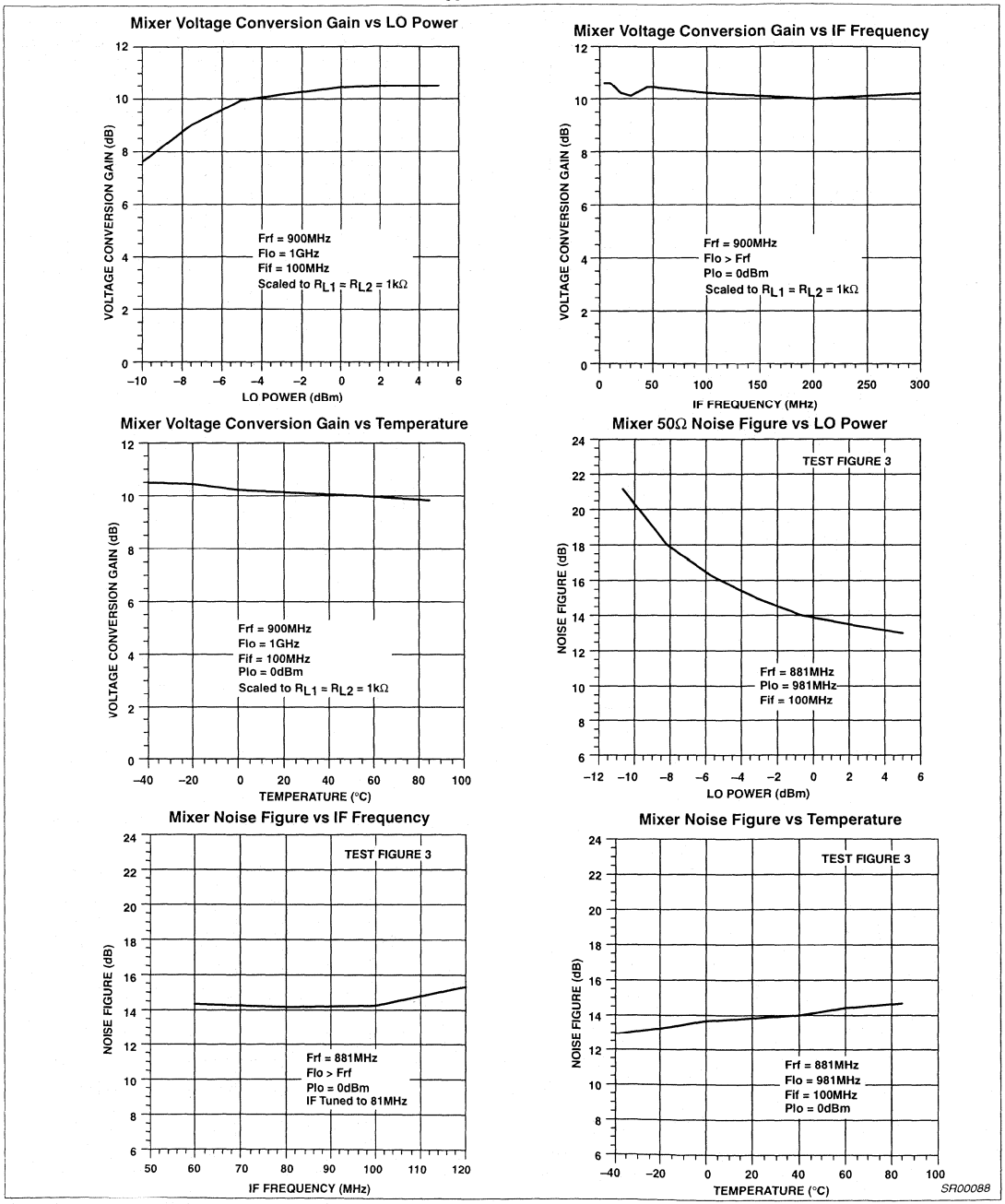


Figure 7. Mixer Gain/Noise Performance Characteristics

MIXER OVERLOAD/DISTORTION CHARACTERISTICS $4.5 \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Fig. 1, unless otherwise specified

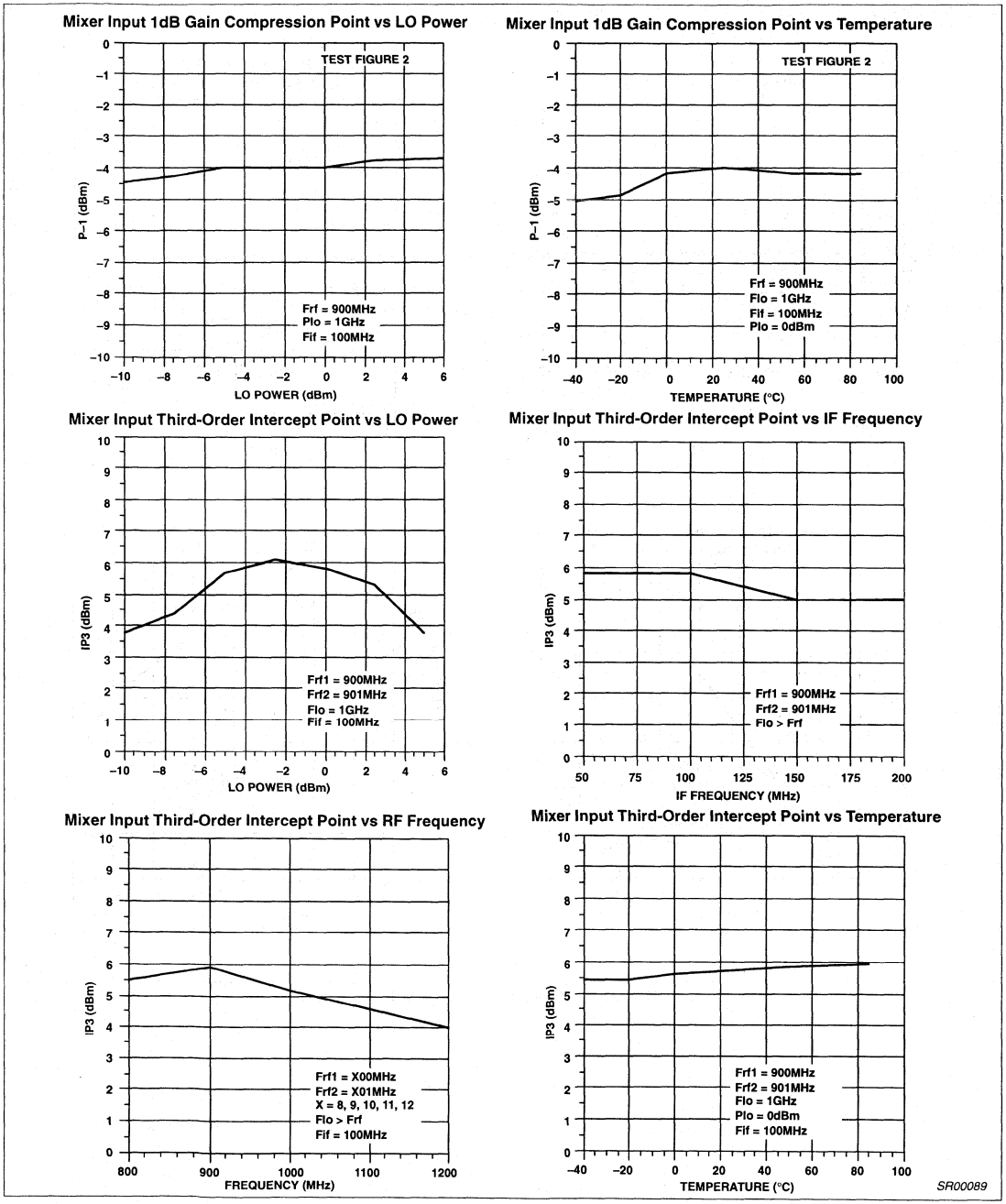


Figure 8. Mixer Overload/Distortion Characteristics

MIXER S11/ISOLATION/INTERFERENCE CHARACTERISTICS

$4.5 \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Fig. 1, unless otherwise specified

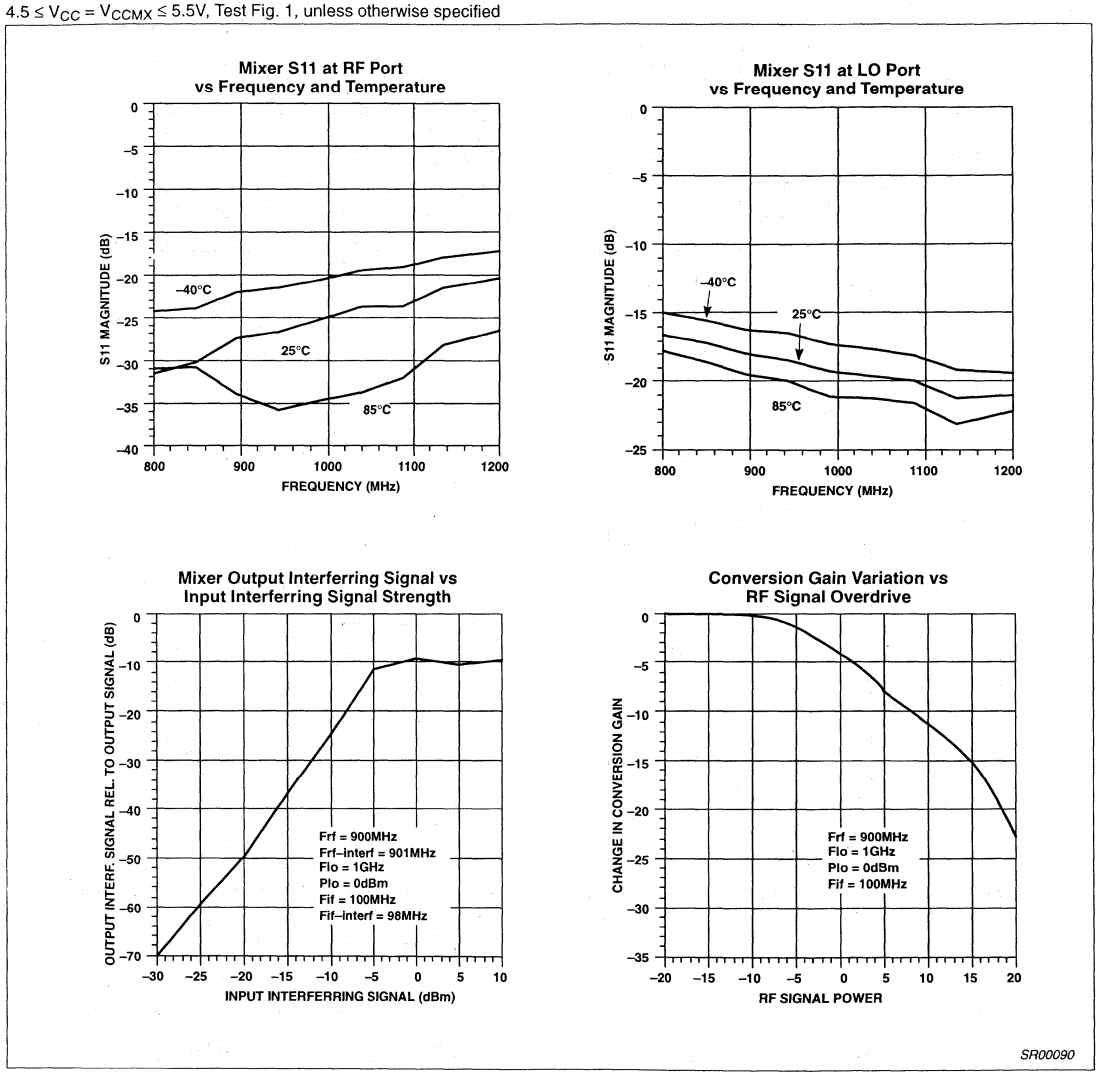


Figure 9. Mixer S11/Isolation/Interference Characteristics

OVERALL PERFORMANCE: ISOLATION CHARACTERISTICS

$4.5 \le V_{CC} = V_{CCMX} \le 5.5V$, Test Fig. 1, unless otherwise specified

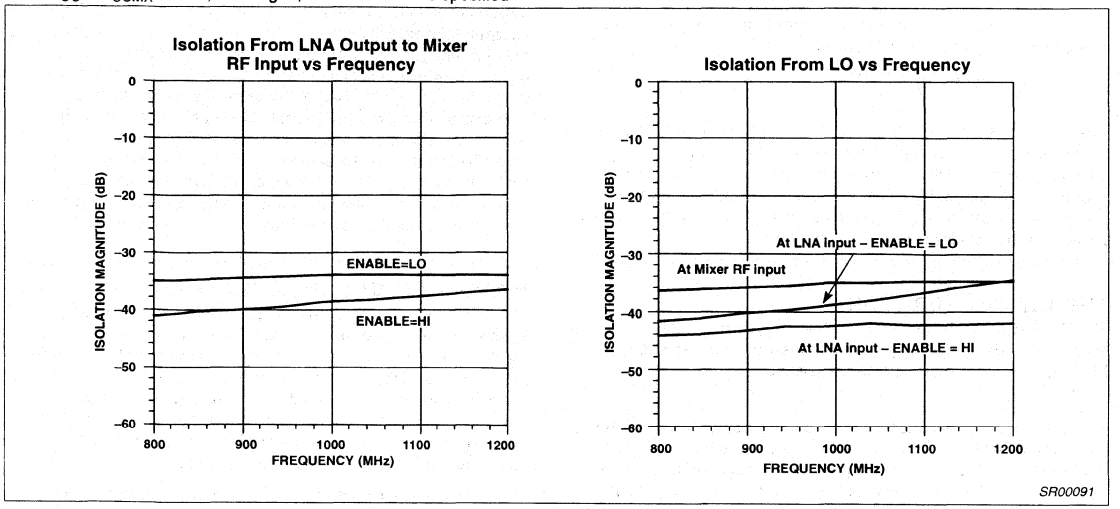


Figure 10. Overall Performance: Isolation Characteristics

SPECIFICATIONS

The goal of the Specifications section of the datasheet is to provide information on the NE/SA600 in such a way that the designer can estimate statistical variations, and can reproduce the measurements. To this end the high frequency measurements are specified with a particular PC board layout. Variations in board layout will cause parameter variations (sensitive parameters are discussed in the sections on the LNA and mixer below). For many RF parameters the ±3 sigma limits are specified. Statistically only 0.26% of the units will be outside these limits.

The LNA + mixer conversion gain is measured with an incident 900MHz signal and a 83MHZ SAW filter at the IF output. This measurement along with a gain measurement of the LNA ensure the correct operation of the chip and also allows a calculation of mixer conversion gain.

PIN DESCRIPTIONS AND OPERATIONAL LIMITS

RF_{INA}
Input of LNA, AC coupling required, DC = 0.78V, frequency range from DC to 2GHz, gain at low frequencies is 40dB — so be careful of overload, impedance below 50Ω, shunt 15-18nH inductor helps input match and noise figure.

RF_{OUTA}
Output of LNA, AC coupling required, DC = 1.27V, frequency range from DC to 2GHz, impedance above 50Ω.

BYPASS
Bypass capacitor should be 100 times larger than the largest signal coupling capacitor for the LNA, DC = 1.05V.

RF_{INMX}
Mixer RF port, AC coupling required, DC = 1.43V, frequency range from 100MHz to 2.5GHz, impedance close to 50Ω resistive.

LO_{IN}
Mixer LO port, AC coupling required, DC=3.35V, frequency range from 100MHz to 2.5GHz, impedance close to 50Ω resistive.

IF_{OUT}
Mixer IF port, open-collector output with 1.6mA DC, frequency range DC to 1GHz, impedance approximately 1pF capacitive.

Enable
TTL/CMOS compatible input. Bias current approximately zero.

CONVERSION GAIN DEFINITIONS

Referring to the figure above, we define the ratio of V_A (at the IF frequency) to V_I (at the RF frequency) to be the Available Voltage Conversion Gain, or more simply Voltage Conversion Gain,

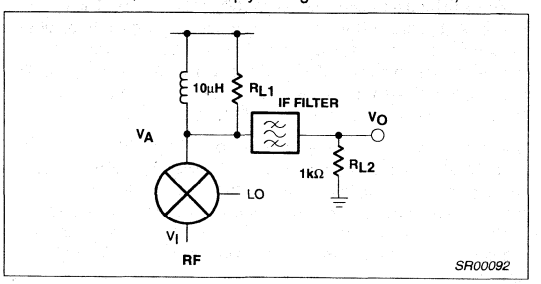


Figure 11.

$$VG_C = 20\log\left(\frac{V_A}{V_I}\right)$$

where V_A and V_I are expressed in similar voltage units (such as peak-to-peak). The voltage output V_A is decreased by the IF Filter

loss (and any other matching required). Typically, VG_C is 10.4dB for the NE/SA600 mixer with the net IF impedance equal to 500Ω.

It is more common to express the conversion gain in terms of power, so we have the Power Conversion Gain,

$$PG_C = 10\log\left(\frac{P_A}{P_I}\right) - 3dB$$

where $P_A = V_A^2 / R_{IF}$ and $P_I = V_I^2 / R_{RF}$. R_{IF} is the net resistance at the IF frequency at the IF port, and R_{RF} is the input impedance at the mixer RF port. With a 500Ω IF impedance and a 50Ω RF input impedance, the conversion gain works out to –2.6dB typically. The power delivered to the load is down 3dB with respect to the available power because of loss in R_{L1}.

THEORY OF OPERATION

The NE/SA600 is fabricated on the Philips Semiconductors advanced QUBiC technology that features 1µm channel length MOSFETs and 13GHz FT bipolar transistors.

LNA

The Low Noise Amplifier (LNA) is a two stage design incorporating feedback to stablize the amplifier. An external bypass capacitor of (typically) 0.01µF is used. The inputs and outputs are matched to 50Ω. The amplifier has two gain states: when the ENABLE pin is taken high, the amplifier draws 9mA of current and has 16dB of gain at 900MHz. When the ENABLE pin is low, the amplifier current goes to zero, and the amplifier is replaced by a thru. Typical loss for the thru is 7dB. This dual-gain state approach can be used in bang-bang control systems to achieve a low gain, high overload front-end as well as the more usual high gain, low overload front-end.

The amplifier has gain to frequencies past 2GHz, but a practical upper end is 1.6-1.7GHz. Both the input match and the noise figure (NF) can be improved with a shunt 15-18nH inductor at the input. Typically, the gain increases 0.4dB, the match improves to 13-16dB, and the noise figure drops to 1.95-2dB. Variations of any of the RF parameters with V_{CC} is negliglible, and variation with temperature is minimal.

Mixer

The mixer is a single-balanced topology designed to draw very low current, typically 4mA, and provide a very high input third-order intermodulation intercept point , typically IP3=+6dBm. The RF and LO ports impedances are nearly 50Ω resistive, and the IF output is an open collector. The open-collector output allows direct interfacing with high impedance IF filters, such as surface acoustic wave (SAW) filters without the need for external step-up transformers (which are needed for 50Ω output mixers).

The basic mixer is functional from DC to well over 2.5GHz, but RF and LO return losses degrade below 100MHz. The IF output can be used from DC to 500MHz or more, although typically the intermediate frequency is in the range 45-120MHz in many 900MHz receivers. To achieve the lowest noise, the LO drive level should be increased as high as possible, consistent with power dissipation limitations.

POWER SUPPLY ISSUES

V_{CC} bypassing is important, but not extremely critical because of the internal supply regulation of the NE/SA600. The Pin 1 V_{CC} supplies the LNA and powers overhead circuitry. Typical current draw is 9.8mA while enable is high (1mA powered down). The Pin 14 V_{CCMX} powers the mixer and typically has 3.2mA of current (assuming an inductor biasing the IFout back to V_{CCMX}). Care must be taken to avoid bringing any IC pin above V_{CC} by more than 0.3V, or below any ground by more than 0.3V. For example, this can occur if the enable pin is fed from a microcontroller that is powered up quicker than the NE/SA600. In this condition the internal electrostatic discharge (ESD) protection network may turn-on, possibly causing a part misfunction. Generally this condition is reversible, so long as the source creating the overstress is current limited to less than 100mA. To avoid the problem, make sure both V_{CC} pins are tied together near the IC, and install a 1kΩ resistor in series with the enable pin if it is likely to go above V_{CC}.

BOARD LAYOUT CONSIDERATIONS

The LNA is sensitive to mutual inductance from the input to ground. Therefore long narrow input traces will degrade the input match. Ideally, a top side ground-plane should be employed to maximize LNA gain and minimize stray coupling (such as LO to antenna). To avoid amplifier peaking, the output and input grounds should not be run together. Attach both grounds to a solid ground plane. A solid ground plane beneath the package will maximize gain. Top side to back side ground through holes are highly recommended.

The mixer is relatively insensitive to grounding. Care should be taken to minimize the capacitance on the RF port (Pin 11) for best noise figure. Also, the capacitance on the IFout pin must be kept small to avoid conversion gain rolloff when using high IF frequencies. The purpose of the inductor from IFout to V_{CC} is to set the midpoint of the IF swing to be V_{CC}. Without this inductor the part is sensitive to output overload under low V_{CC} (V_{CC} = 4.5V) and hot temperature conditions. The V_{CCMX} pin must be kept at the same potential as the V_{CC} pin.

APPLICATIONS INFORMATION

The NE/SA600 is a high performance, wide-band, low power, low noise amplifier (LNA) and mixer circuit integrated in a BiCMOS technology. It is ideally suited for RF receiver front-ends for both analog and digital communications systems.

There are several advantages to using the NE/SA600 as a high frequency front-end block instead of a discrete implementation. First is the simplicity of use. The NE/SA600 does not need any external biasing components. Due to the higher level of integration and small footprint (SO14) package it occupies less space on the printed circuit board and reduces the manufacturing cost of the system. Also the higher level of integration improves the reliability of the LNA and mixer over a discrete implementation with several components.

The LNA thru mode in NE/SA600 helps reduce power consumption in applications where the amplifiers can be disabled due to higher received signal strength (RSSI). Other advantages of this feature are described later in this section.

The mixer is an active mixer with excellent conversion gain at low LO input levels, so LO levels as low as -5dBm to -10dBm can be used depending on the applications requirement for mixer gain, mixer noise figure and mixer third order intercept point. This reduces the LO drive requirements from the VCO buffer, thus reducing its current consumption. Also, due to lower LO levels, the shielding requirements can be minimized or eliminated, resulting in substantial cost savings and weight and space reduction.

And last but not least, is the impedance matching at LNA inputs and outputs and mixer RF and LO input ports. Only those who have toiled through discrete transistor implementations for 50Ω input and output impedance matching can truly appreciate the elegance and simplicity of the NE/SA600 input and output impedance matching to 50Ω. Also, the mixer output impedance is high, so matching to a crystal or SAW IF filter becomes extremely easy without the need for additional IF impedance transformers (tapped-C networks with inductors or baluns).

The NE/SA600 applications and demo board features standard low cost 62mil FR-4 board. A top-side ground plane is used and 50Ω coplanar transmission lines are used. LO and RF_{INA} traces are perpendicular. Provisions for the image reject filter between RF_{OUTA} and RF_{INMX} are provided. A simple LC match for 80MHz IF is used so that 50Ω measurements can be made on the demo board.

The NE/SA600 applications evaluation board schematic is shown in Figure 1. The V_{CC} (Pin 1) and V_{CCMX} (Pin 14) are tied together and the power supply is bypassed with capacitors C5 and C6. These capacitors should be placed as close to the device as practically possible.

C1 is the DC blocking capacitor to the input of the LNA. L1 provides additional input matching to the LNA for an improved return loss (S11). This inductor can be a surface-mount component or can be easily drawn on the printed circuit board (small spiral or serpentine). This additional match improves the gain of the LNA by 0.4dB and lowers the noise figure to 2dB or less. If the typical gain of the LNA of 16dB is acceptable with 2.2dB of noise figure, then L1 can be eliminated. If the LNA input is fed from a duplexer or selectivity filter after the antenna, C1 can also be eliminated since the filter will also provide DC blocking. The LNA bypass capacitor C3 should be at least 100 times C1 or C9 for low frequency stability. Switch S1 toggles the LNA gain/through function. R1 is used only to limit the maximum current into the enable pin and only necessary if enable may power up before the V_{CC}.

C4 is a DC blocking capacitor for the LO input pin and may not be needed in actual applications if the VCO output is isolated and will not upset the internal DC biasing of the mixer. The image reject filter goes between the output of the LNA and the RF input to the mixer. Since the LO input, RF output and mixer input are all 50Ω matched impedances internally, there is no need for any external components. C8 and C9 are DC blocking capacitors to the connectors and will not be needed in an actual application.

R2 and L2 are the load to the mixer output which is typical of the IF crystal or SAW filters. C2 and L3 provide a match from the high impedance mixer output to a 50Ω test set-up (spectrum analyzer, etc.) and C7 is a DC blocking capacitor for the mixer output.

The printed circuit board layout for the schematic of Figure 1 is shown in Figure 14. It is a very simple printed circuit board layout with all the components on a single side. The layout also accomodates a two pole image reject filter between the LNA outupt and mixer input. All the input and output traces to the LNA and mixer should be 50Ω tracks with the exception of mixer output, which can be very narrow due to the higher impedances of the filter.

The NE/SA600 internal supply is very well regulated. This is seen from Figure 15 which shows the I_{CC} vs. V_{CC} for the NE/SA600. Table NO TAG shows the S11, S21, S22 and S21 for the LNA from 800-1200MHz. Typical measurements at 900MHz for the critical parameters such as gain, noise figure, IP_3, 1dB compression point, etc. as measured on an applications evaluation board are as follows :

LNA gain = 16.5dB
LNA through = –7dB
Mixer gain =–3dB (into a 50Ω load)
LNA noise figure = 2dB
Mixer noise figure = 14dB
LNA IP_3 = –10dBm (in gain mode)
LNA IP_3 = +26dBm (in through mode)
LNA 1dB compression point = –20dBm
Mixer 1dB compression point = –4dBm

The shunt inductor L1 for input match is optional. Figure 16 shows the effect of the inductor value from 8.2nH to 15nH on gain, noise figure and input match.

The total power gain for the LNA and mixer (excluding the image reject filter) in a system where the output of the mixer is loaded with 50Ω is about 14dB. In an actual system the output impedance of the mixer is usually much higher than 50Ω (more like 1kΩ or higher) and so it is more important to consider the voltage gain from the input at the LNA to the mixer output. The voltage gain in this case will be about 29.85V/V. The total noise figure for the LNA and mixer combination is be about 3.27dB. The input third order intercept point for the LNA and mixer is about -11dBm. In the LNA through mode, the intercept point for the combination is higher than +19dBm. This LNA through feature provides an additional boost to the total dynamic range of the system.

The NE/SA600 finds applications in many areas of RF communications. It is an ideal down converter block for high performance, low cost, low power RF communications transceivers. The front-end of a typical AMPS/TACS/NMT/TDMA/CDMA cellular phone is shown in Figure 13. This could also be the front-end of a VHF/UHF handheld transceiver, UHF cordless telephone or a spread spectrum system.

The antenna is connected to the duplexer input. The receiver output of the duplexer is connected to the RF input of the LNA. If the additional improvement in noise figure and gain are not needed to meet the system specifications then L1 and C1 can be eliminated. In TDMA systems, the NE/SA600 can be totally powered down by Q1 and the two resistors. In this mode the current consumption will be zero mA. Care should be taken in the software of the system to insure that the enable pin on NE/SA600 tied to the LNA gain control port is held low while the device is in total power down mode. L2 and C2 can be tuned to the IF frequency and to match to the IF filter impedance.

A complete analysis of the front-end shows that the total voltage gain from the antenna input to the mixer output is about 9.5V/V. This value includes a 3.2dB loss for the duplexer and a 1.8dB loss for the bandpass filter. The noise figure as referred to the antenna is 7dB and the input third order intercept point is about -7.5dBm. In LNA through mode the input third order intercept point increases to about +24dBm.

During normal operation of a handheld RF receiver the received signal strength (RSSI) is nominally greater than -100dBm. The signal only drops below this level due to severe multipath fading, shadow effect or when the receiver is at extreme fringes of cell coverage. The LNA through mode can be used here as a two step gain control such that when RSSI is below a certain threshold level (e.g. -90dBm), the LNA has a -7dB loss and the total current consumption of the NE/SA600 is only 4.3mA. The sensitivity of the system will not suffer because the received RF signal is much higher than the noise floor of the system. When the RSSI falls below a certain threshold (e.g. -95dBm) the LNA is enabled to give the full

16.5dB of gain with 2dB of noise figure. In this mode the current consumption is increased to 13mA. But for hand-held equipment, the average current consumption will be closer to 5-6mA. The other advantage of the LNA through mode besides power savings is the input overload characteristics. Due to the much higher input third order intercept point of the LNA (+26dBm), the receiver is immune to strong adjacent channel interference. Implementing this feature with an FM/IF device such as the NE625/7 with fast RSSI response and a window comparator toggling the LNA mode of NE/SA600, a fast two-step AGC with response time less than 10μs can be achieved.

This is a very useful feature to equalize multipath fading effects in a mobile radio system.

In conclusion, the NE/SA600 offers higher level of integration, higher reliability, higher level of performance, ease of use, simpler system design at a cost lower than the discrete multi-transistor implementations. In addition, the NE/SA600 provides unique features to enhance receiver performance which are almost unattainable with discrete implementations.

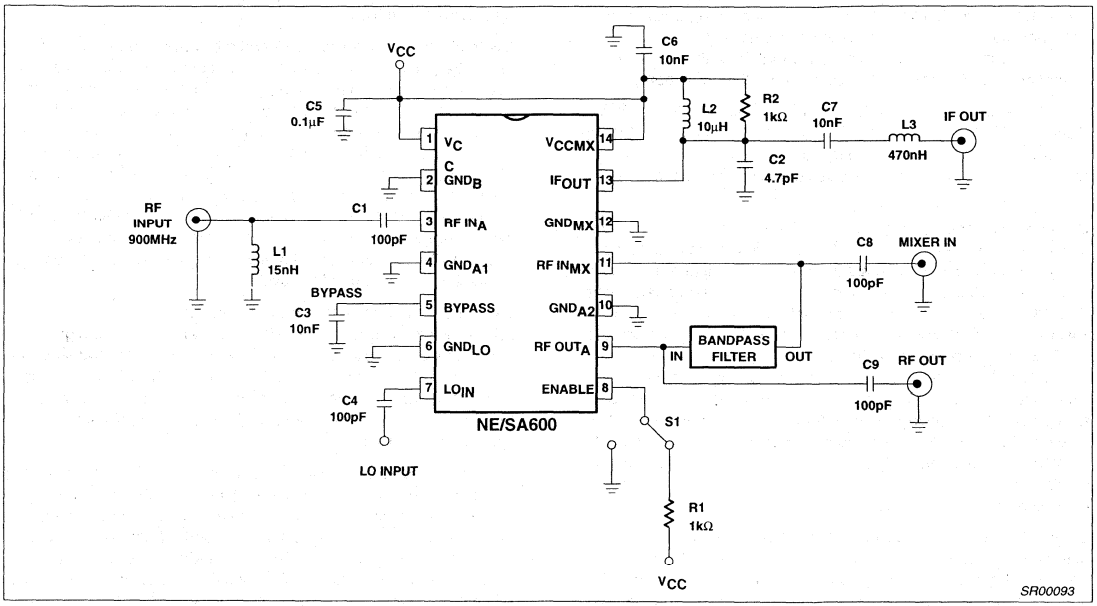


Figure 12.

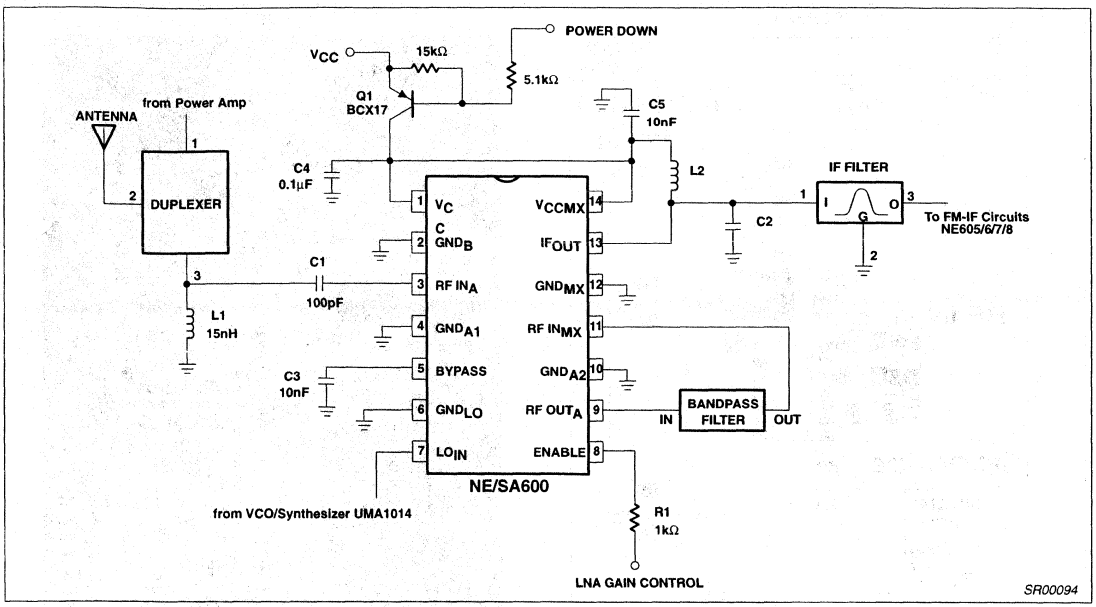

POWER DOWN
VCC
15kΩ
5.1kΩ
Q1
BCX17
C5
10nF
ANTENNA
from Power Amp
1
2
DUPLEXER
C4
0.1µF
L2
IF FILTER
1
I
G
O
3
2
To FM-IF Circuits
NE605/6/7/8
C2
C1
100pF
3
L1
15nH
C3
10nF
1 VC
2 C GNDB
3 RF INA
4 GNDA1
5 BYPASS
6 GNDLO
7 LOIN
14 VCCMX
13 IFOUT
12 GNDMX
11 RF INMX
10 GNDA2
9 RF OUTA
8 ENABLE
NE/SA600
IN
BANDPASS
FILTER
OUT
from VCO/Synthesizer UMA1014
R1
1kΩ
LNA GAIN CONTROL
SR00094

Figure 13.

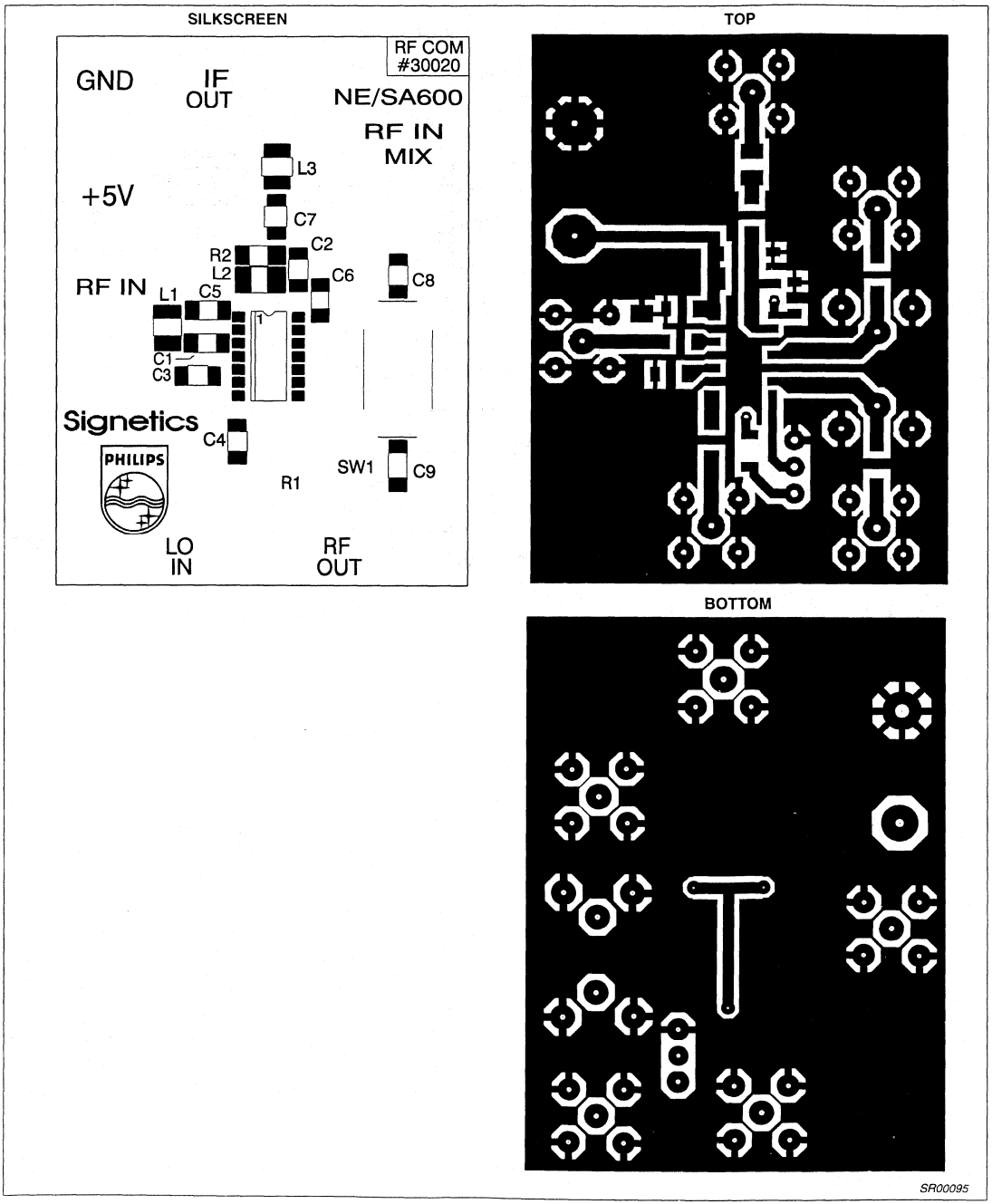


Figure 14. PC Board Layout

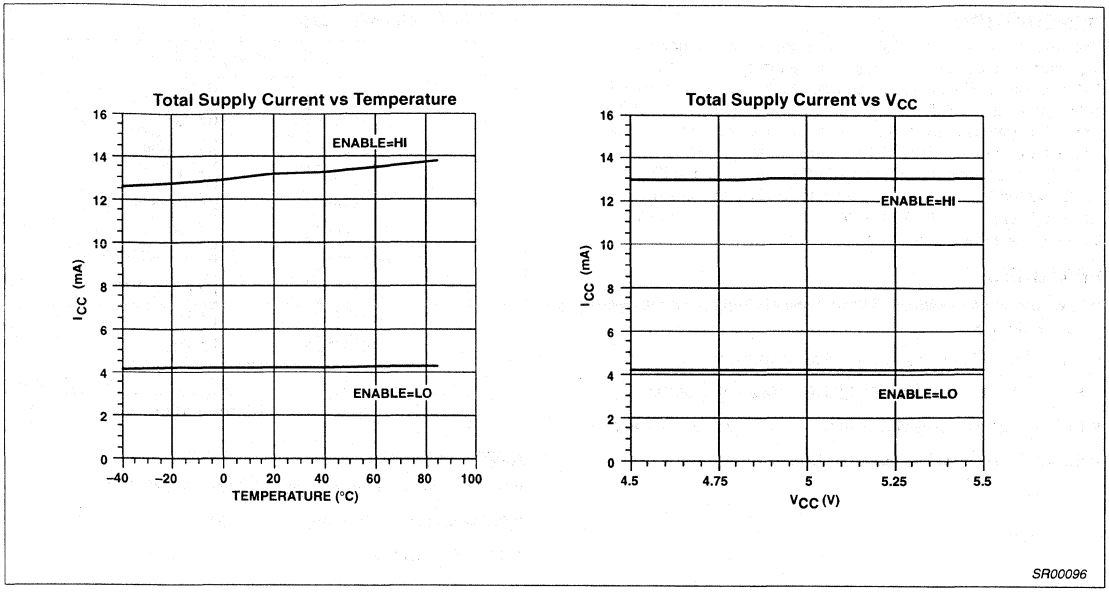


Figure 15.

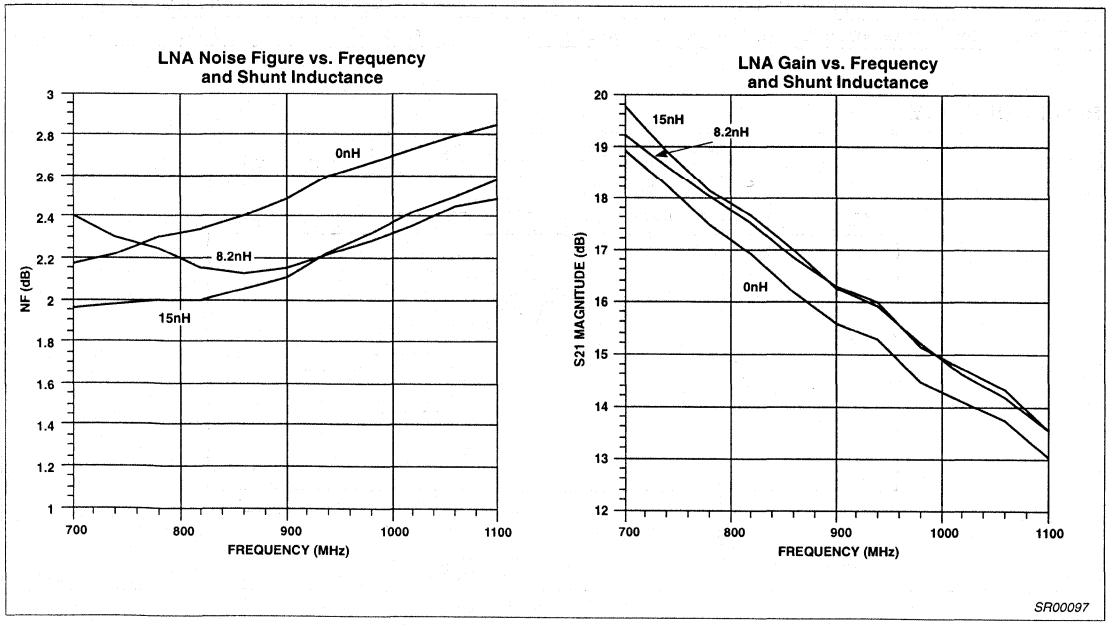


Figure 16.

1GHz low voltage LNA and mixer | SA601

DESCRIPTION

The SA601 is a combined RF amplifier and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 1.6dB noise figure at 900MHz with 11.5dB gain and an IP3 intercept of -2dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has a 9.5dB noise figure and IP3 of –2dBm at the input at 900MHz. The nominal current drawn from a single 3V supply is 7.4mA. The Mixer can be powered down to further reduce the supply current to 4.4mA.

FEATURES

- Low current consumption: 7.4mA nominal, 4.4mA with the mixer powered-down
- Outstanding LNA noise figure: 1.6dB at 900MHz
- High system power gain: 18dB (LNA + Mixer) at 900MHz
- Excellent gain stability versus temperature and supply voltage
- External >-7dBm LO can be used to drive the mixer

PIN CONFIGURATION

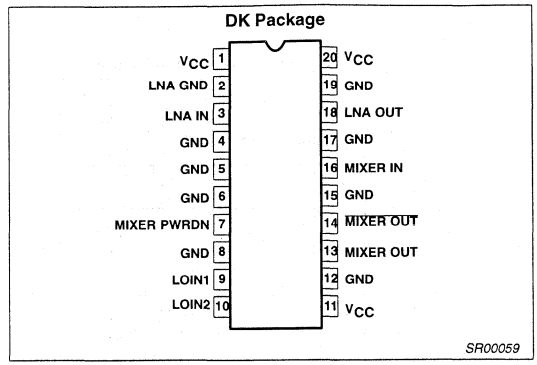


Figure 1. Pin Configuration

APPLICATIONS

- 900MHz cellular front-end (NADC, GSM, AMPS, TACS)
- 900MHz cordless front-end (CT1, CT2)
- 900MHz receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount, SSOP)	-40 to +85°C	SA601DK	SOT266-1

BLOCK DIAGRAM

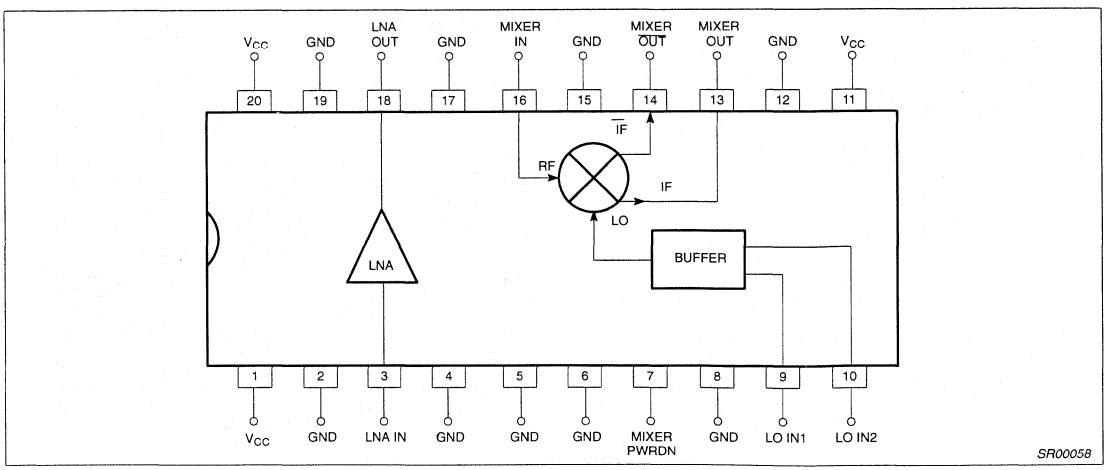


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS[3]

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}: 20-Pin SSOP = 110°C/W
3. Pins 9 and 10 are sensitive to electrostatic discharge (ESD).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current			7.4		mA
		Mixer power-down input low		4.4		
V_{LNA-IN}	LNA input bias voltage			0.78		V
$V_{LNA-OUT}$	LNA output bias voltage			2.1		V
V_{MX-IN}	Mixer RF input bias voltage			0.94		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; LO_{IN} = -7dBm @ 964MHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			-3σ	TYP	+3σ	
S_{21}	Amplifier gain	881MHz	10	11.5	13	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	881MHz		0.003		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz		0.01		dB/MHz
S_{12}	Amplifier reverse isolation	881MHz		-20		dB
S_{11}	Amplifier input match[1]	881MHz		-10		dB
S_{22}	Amplifier output match[1]	881MHz		-10		dB
P_{-1dB}	Amplifier input 1dB gain compression	881MHz		-16		dBm
IP3	Amplifier input third order intercept	$f_2 - f_1$ = 25kHz, 881MHz	-3.5	-2	-0.5	dBm
NF	Amplifier noise figure	881MHz	1.3	1.6	1.9	dB
VG_C	Mixer voltage conversion gain: $R_P = R_L$ = 1kΩ	f_S = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz	18.0	19.5	21.0	dB
PG_C	Mixer power conversion gain: $R_P = R_L$ = 1kΩ	f_S = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz	5.0	6.5	8.0	dB
S_{11M}	Mixer input match[1]	881MHz		-10		dB
NF_M	Mixer SSB noise figure	881MHz	8.0	9.5	11.0	dB
P_{-1dB}	Mixer input 1dB gain compression	881MHz		-13		dBm
$IP3_M$	Mixer input third order intercept	$f_2 - f_1$ = 25kHz, 881MHz	-3.5	-2	-0.5	dBm
IP_{2INT}	Mixer input second order intercept	881MHz		12		dBm
P_{RFM-IF}	Mixer RF feedthrough	881MHz		-7		dB
P_{LO-IF}	LO feedthrough to IF	881MHz		-25		dB
P_{LO-RFM}	LO to mixer input feedthrough	881MHz		-38		dB
P_{LO-RF}	LO to LNA input feedthrough	881MHz		-40		dB
$P_{LNA-RFM}$	LNA output to mixer input	881MHz		-40		dB
P_{RFM-LO}	Mixer input to LO feedthrough	881MHz		-23		dB
LO_{IN}	LO drive level	964MHz		-7		dBm

NOTE:
1. Simple L/C elements are needed to achieve specified return loss.

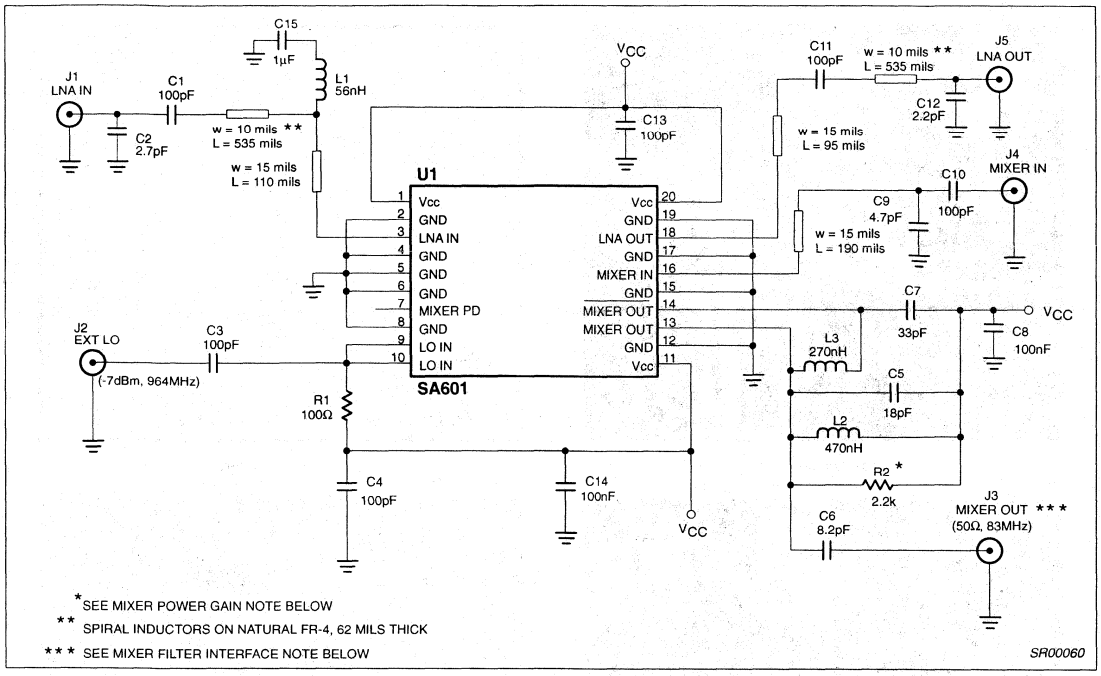


Figure 3. Application Circuit

CIRCUIT TECHNOLOGY

LNA

Impedance Match: Intrinsic return loss at the input and output ports is 7dB and 9dB, respectively. With no external matching, the associated LNA gain is ≈10dB and the noise figure is ≈1.4dB. However, the return loss can be improved at 881MHz using suggested L/C elements (Figure 5) as the LNA is unconditionally stable.

Noise Match: The LNA achieves 1.6dB noise figure at 881MHz when S_{11} = -10dB. Further improvements in S_{11} will slightly decrease the NF and increase S_{21}.

Temperature Compensation: The LNA has a built-in temperature compensation scheme to reduce the gain drift to 0.003dB/°C from –40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 3V to 5V.

LO Drive Level: Resistor R1 can be replaced by an inductor of 4.7nH and C3 should be adjusted to achieve a good return loss at the LO port. Under this condition, the mixer will operate with less than -10dBm LO drive.

IP3 Performance: C9 between Pin 16 and ground can be removed to introduce 3dB mismatch loss, while improving the IP3 to +3dBm. The associated noise figure is 11dB.

Mixer

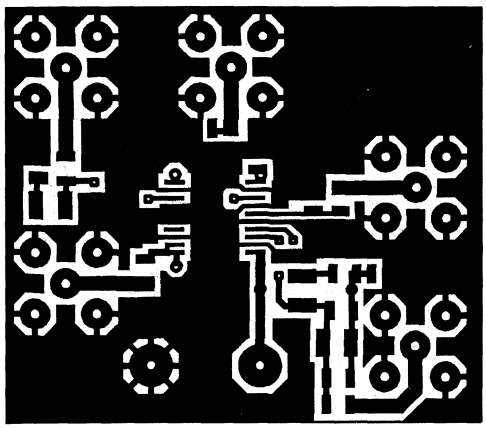
Input Match: The mixer is configured for maximum gain and best noise figure. The user needs to supply L/C elements to achieve this performance.

Power Gain: The gain can be increased by approximately 1.5dB by placing R2 across C7, instead of C5.

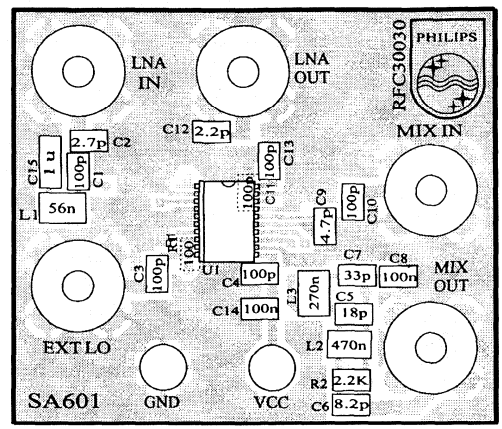
Power Down: The mixer can be disabled by connecting Pin 7 to ground. When the mixer is disabled, 3mA is saved.

Power Combining: The mixer output circuit features passive power combining (patent pending) to optimize conversion gain and noise figure performance without using extra DC current or degrading the IP3. For IF frequencies significantly different than 83MHz, the component values must be altered accordingly.

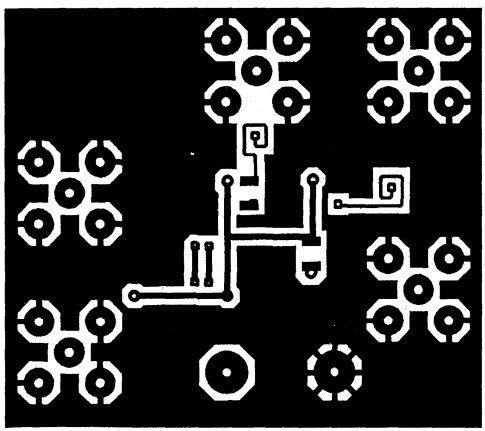
Filter Interface: For system integration where a high impedance filter of 1kΩ is to be cascaded at the mixer IF output, capacitors C5 and C6 need to be changed to 27pF and 1000pF, respectively.



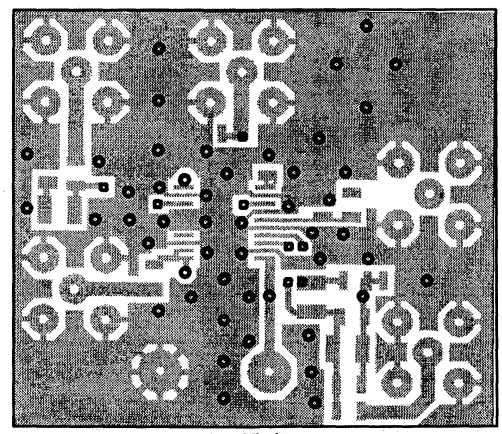
Top View



Silk Screen



Bottom View

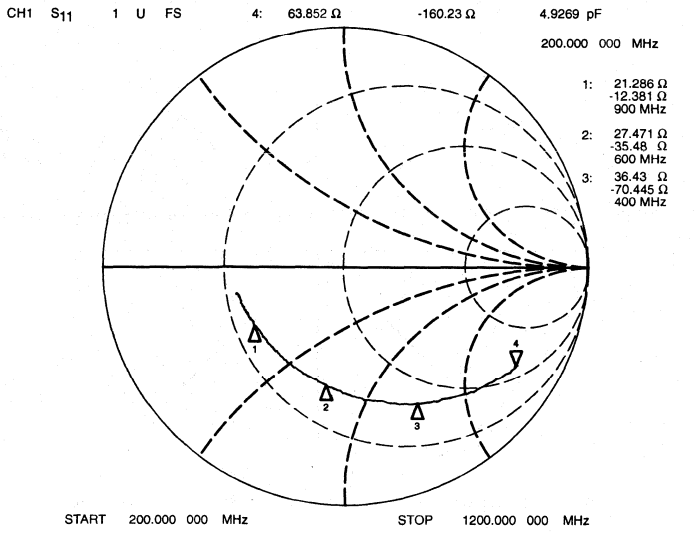


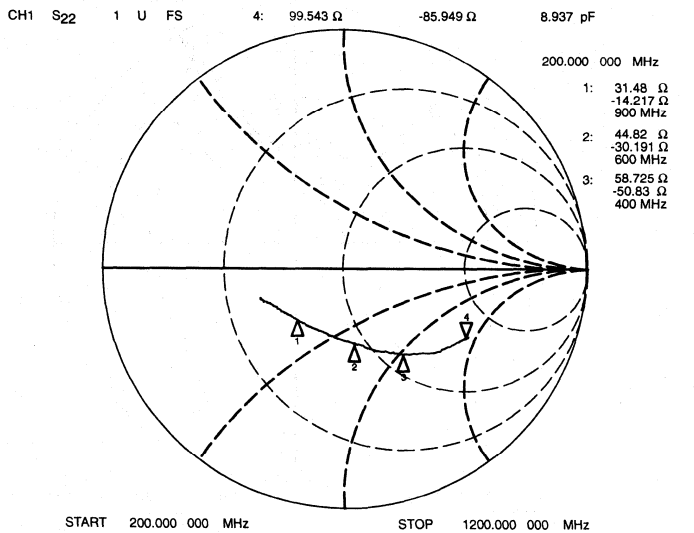
Via Layer

SR00061

Figure 4. SA601 Demoboard Layout (Not Actual Size)

TYPICAL PERFORMANCE CHARACTERISTICS

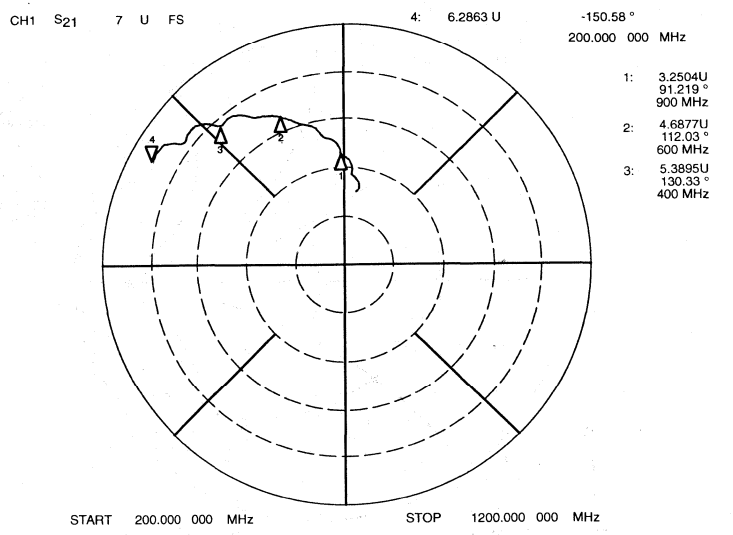


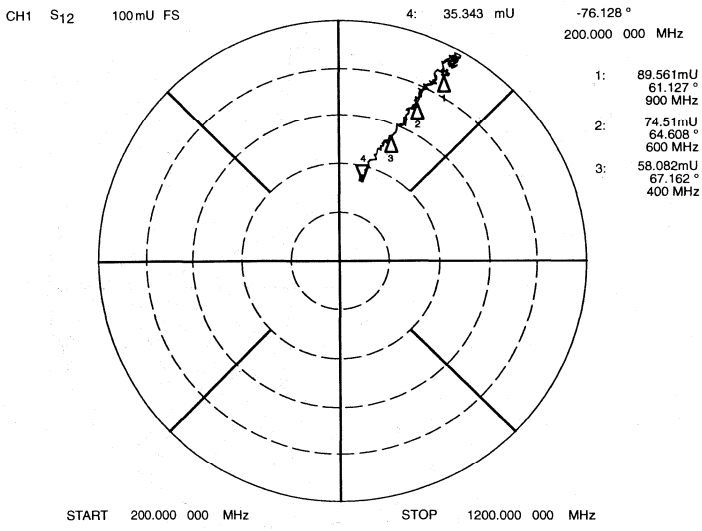


SR00062

Figure 5. LNA Input and Output Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)





SR00063

Figure 6. LNA Transmission and Isolation Characteristics (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

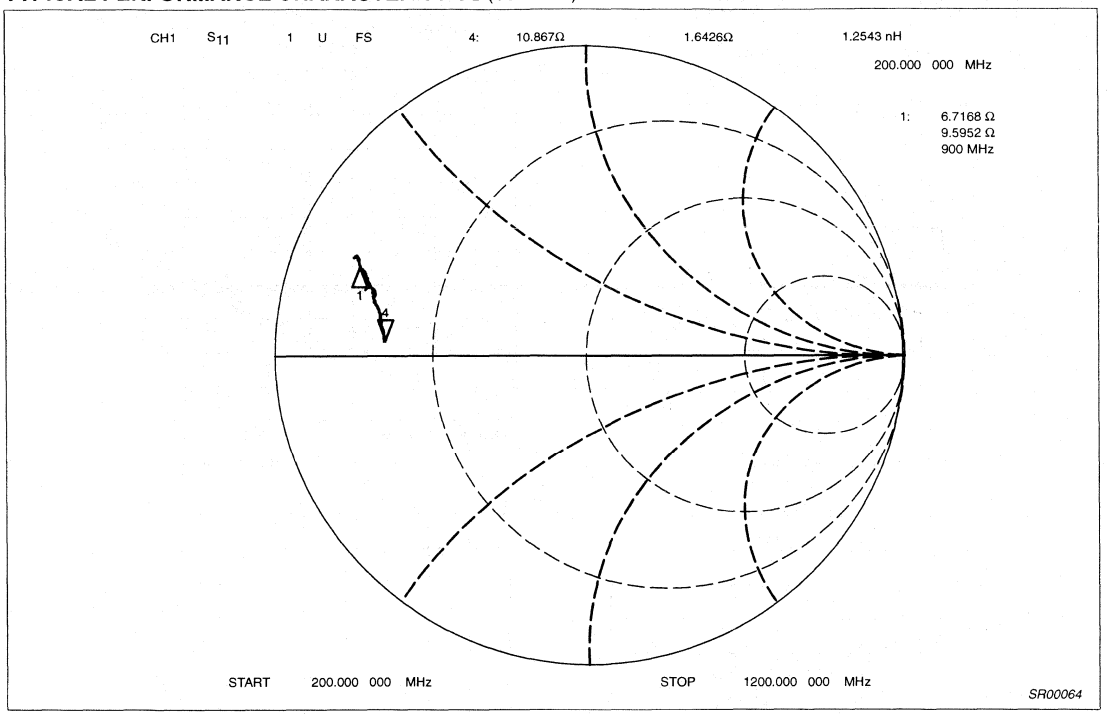


Figure 7. Mixer RF Input Match (at Device Pin)

Table 2. Typical LNA and Mixer S-Parameters

	LNA				Mixer
f	**S_{11}**	**S_{22}**	**S_{21}**	**S_{12}**	**S_{11}**
200MHz	63.852Ω – j 160.23Ω	99.543Ω – j 85.949Ω	6.2863U ∠ 150.58°	35.343mU ∠ 76.128°	10.867Ω + j 1.6426Ω
300MHz	44.879Ω – j 101.69Ω	73.387Ω – j 67.707Ω	5.8096U ∠ 140.47°	47.946mU ∠ 71.169°	10.4Ω + j 3.4609Ω
400MHz	36.43Ω – j 70.445Ω	58.725Ω – j 50.83Ω	5.3895U ∠ 130.33°	58.082mU ∠ 67.162°	10.067Ω + j 4.897Ω
500MHz	30.395Ω – j 48.393Ω	49.928Ω – j 38.813Ω	5.0428U ∠ 120.5°	66.44mU ∠ 66.388°	9.394Ω + j 6.0142Ω
600MHz	27.471Ω – j 35.48Ω	44.82Ω – j 30.191Ω	4.6877U ∠ 112.03°	74.51mU ∠ 64.608°	8.8945Ω + j 7.2227Ω
700MHz	24.428Ω – j 25Ω	39.268Ω – j 24.502Ω	4.2409U ∠ 104.44°	82.235mU ∠ 65.002°	8.1353Ω + j 8.1597Ω
800MHz	22.434Ω – j 17.255Ω	34.664Ω – j 18.59Ω	3.7491U ∠ 97.765°	86.582mU ∠ 62.743°	7.976Ω + j 9.1958Ω
900MHz	21.286Ω – j 12.381Ω	31.48Ω – j 14.217Ω	3.2504U ∠ 91.219°	89.561mU ∠ 61.127°	6.7168Ω + j 9.5952Ω
1000MHz	20.261Ω – j 8.7109Ω	27.887Ω – j 10.77Ω	2.8785U ∠ 84.957°	95.135mU ∠ 60.539°	6.2393Ω + j 10.271Ω
1100MHz	19.718Ω – j 6.252Ω	25.741Ω – j 8.2607Ω	2.5752U ∠ 82.893°	97.348mU ∠ 62.202°	6.0791Ω + j 10.571Ω
1200MHz	19.101Ω – j 4.9316Ω	23.584Ω – j 6.2715Ω	2.1386U ∠ 80.257°	96.558mU ∠ 61.563°	5.8185Ω + j 10.288Ω

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

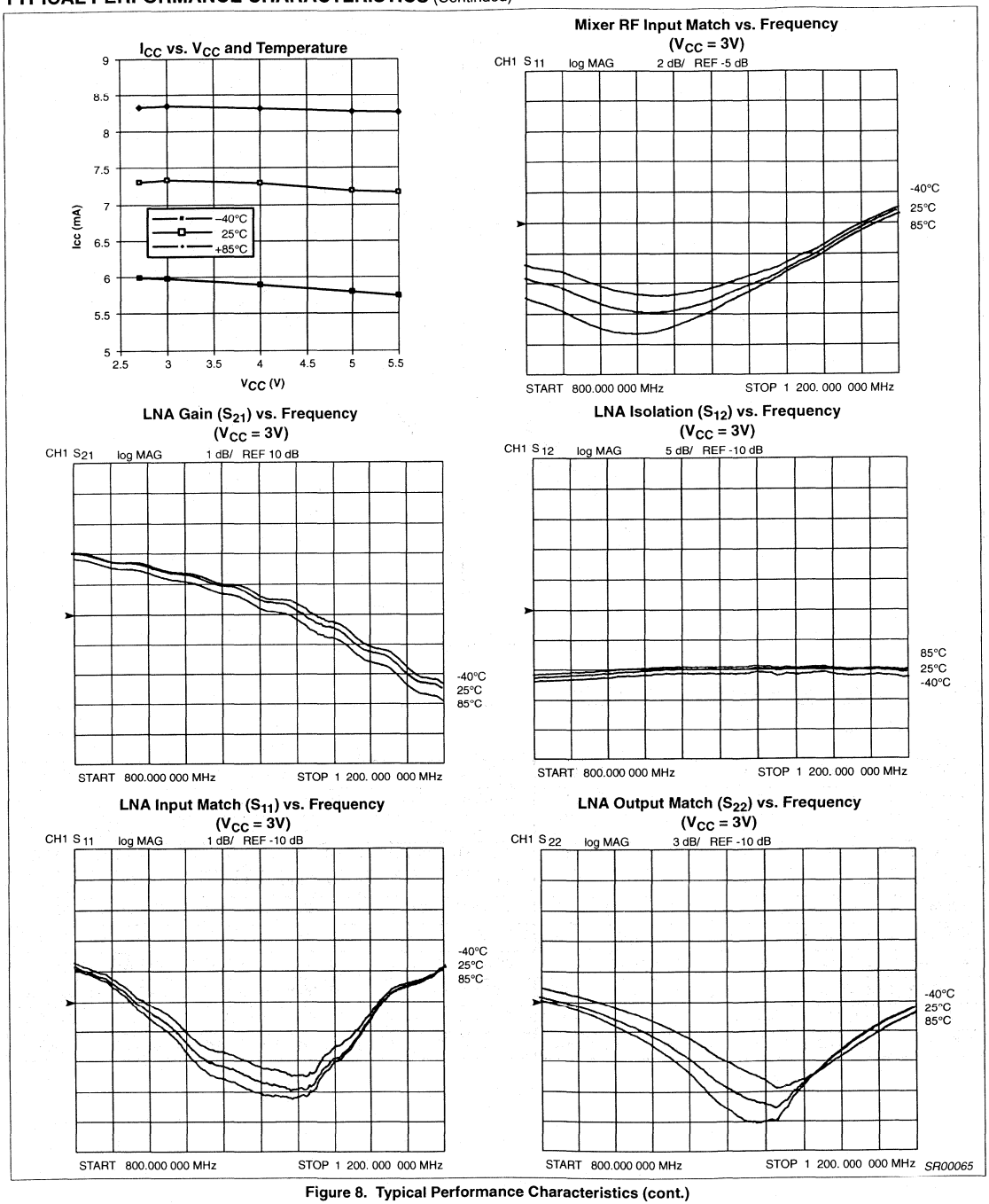


Figure 8. Typical Performance Characteristics (cont.)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

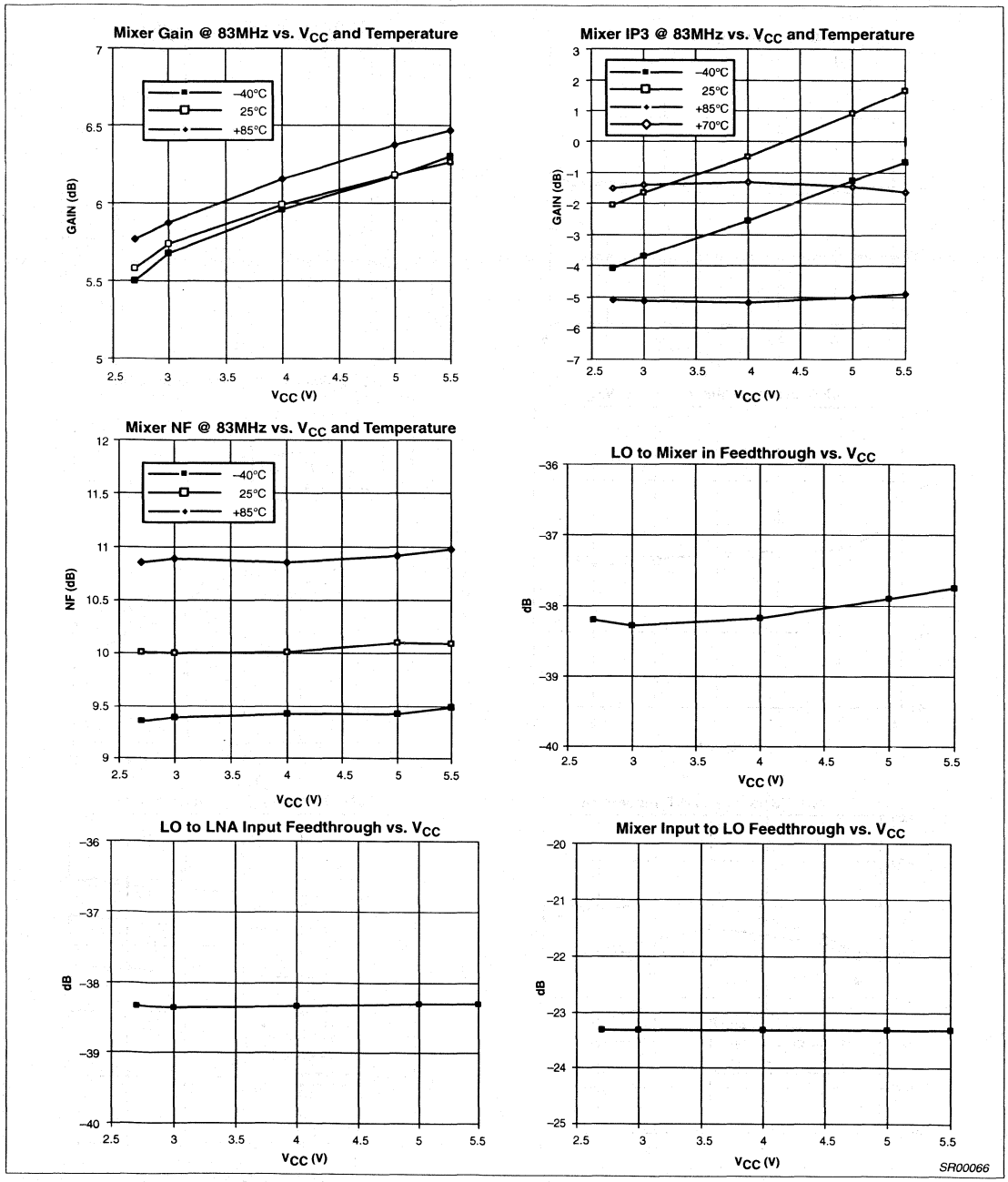


Figure 9. Typical Performance Characteristics (cont.)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

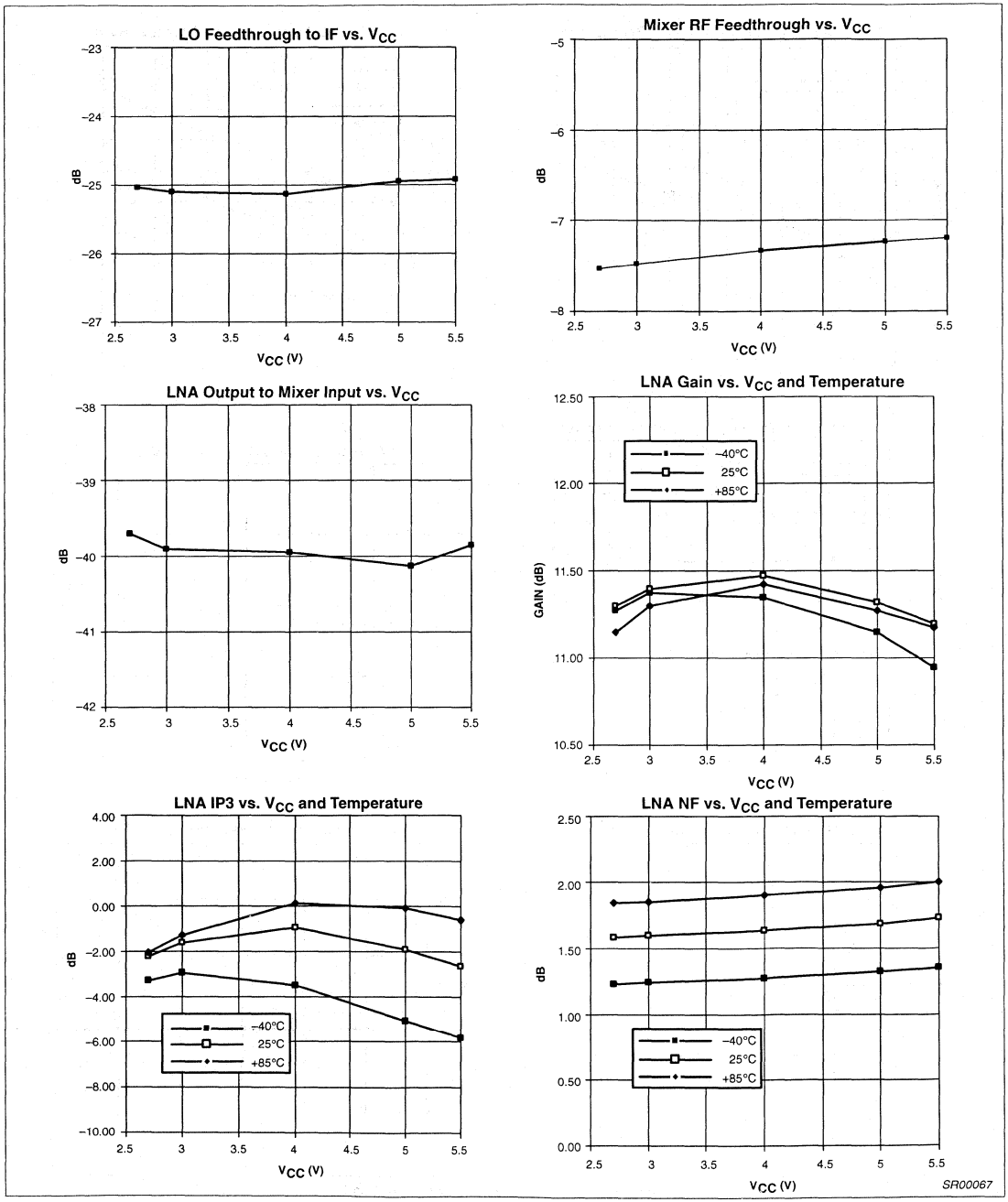


Figure 10. Typical Performance Characteristics (cont.)

1GHz low voltage LNA and mixer SA611

DESCRIPTION

The SA611 is a combined low-noise amplifier, and mixer designed for high-performance low-power communication systems from 800-1000MHz. The low-noise preamplifier has a 1.7dB noise figure at 881MHz with 15dB gain and an IP3 intercept of -7dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has a 12dB noise figure and IP3 of +7.0dBm at the input at 881MHz. The nominal current drawn from a single 3V supply is 8.3mA. Additionally, the entire circuit can be powered down to further reduce the supply current to less than 20µA.

FEATURES

- Low current consumption
- Outstanding gain and noise figure
- Excellent gain stability versus temperature and supply voltage
- LNA and mixer power down capability

PIN CONFIGURATION

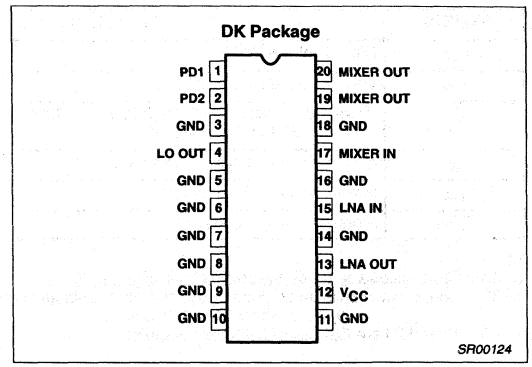


Figure 1. Pin Configuration

APPLICATIONS

- 900MHz cellular and cordless front-end
- Spread spectrum receivers
- RF data links
- UHF frequency conversion
- Portable radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount, SSOP)	-40 to +85°C	SA611DK	SOT266-1

BLOCK DIAGRAM

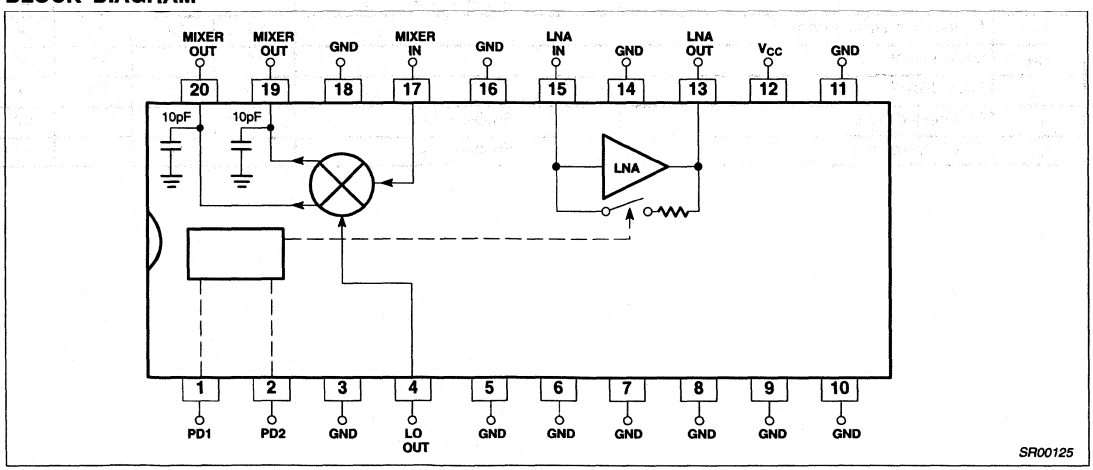


Figure 2. SA611 Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[NO TAG]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)NO TAG 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,
   θ_{JA}: 20-Pin SSOP = 110°C/W
3. Pins 19 and 20 are ESD sensitive (mixer outputs).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current	Full power-on		8.3		mA
		LNA powered-down		5.2		mA
		Full power-down		20		µA
V_T	PD logic threshold voltage		1.2	1.6	1.8	V
V_{IH}	Logic 1 level		2.0		V_{CC}	V
V_{IL}	Logic 0 level		–0.3		0.8	V
I_{IL}	PD1 input current	Enable = 0.4V		10		µA
I_{IH}	PD2 input current	Enable = 2.4V		10		µA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V, T_A = 25°C; RF_{IN} = 881MHz, f_{VCO} = 964MHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			–3σ	TYP	+3σ	
Low Noise Amplifier						
f_{RF}	RF input frequency range		800		1000	MHz
S_{21}	Amplifier gain			15		dB
S_{21}	Amplifier gain in power-down mode			-28		dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled			0.006		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.0GHz		±0.013		dB/MHz
S_{12}	Amplifier reverse isolation	@ 881 MHz		-28		dB
S_{11}	Amplifier input match	With ext. impedance matching		-10		dB
S_{22}	Amplifier output match			-10		dB
P_{-1dB}	Amplifier input 1dB gain compression			-20		dBm
IP3	Amplifier input third order intercept			-7		dBm
NF	Amplifier noise figure			1.7		dB
t_{ON}	Amplifier turn-on time (Enable Lo → Hi)			120		µs
t_{OFF}	Amplifier turn-off time (Enable Hi → Lo)			0.3		µs
Mixer						
PG_C	Mixer power conversion gain: $R_P = R_L$ = 1.2kΩ,	f_{RF} = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz		8.7		dB
S_{11M}	Mixer input match	Ext. impedance matching req.		-10		dB
NF_M	Mixer SSB noise figure			12		dB
P_{-1dB}	Mixer input 1dB gain compression			-14.5		dBm
$IP3_M$	Mixer input third order intercept			7.0		dBm
IP_{2INT}	Mixer input second order intercept			15		dBm
P_{RFM-IF}	Mixer RF feedthrough	RF_{IN} = -28dBm		-45		dBm
P_{LO-IF}	LO feedthrough to IF	LO = -0dBm		-23		dBm
P_{LO-RFM}	LO to mixer input feedthrough			-36		dBm
P_{LO-RF}	LO to LNA input feedthrough			-38		dBm
Overall System						
G_{SYS}	System gain	LNA + Mixer	23.0	23.7	24.4	dB

Table 3. Power ON/OFF Control Logic

PD1	PD2	
0	0	Full chip power-down
0	1 or open	Mixer on, LNA power-down
1 or open	0	Standby (bias on)
1 or open	1 or open	Full chip power-on (default)

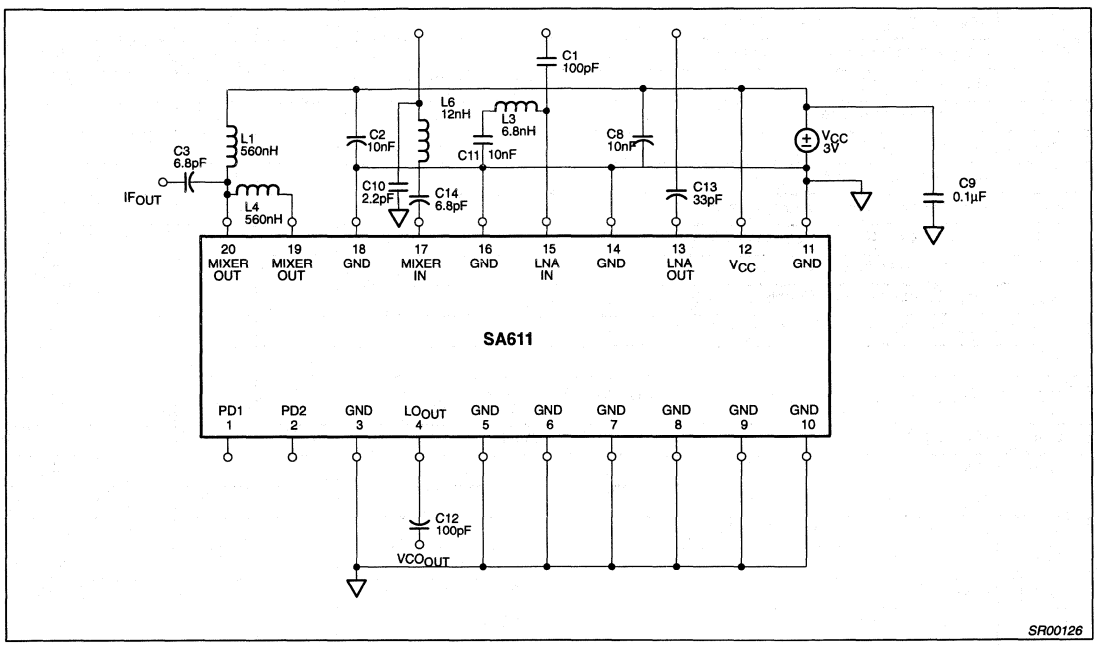


Figure 3. SA611 Applications Circuit

PERFORMANCE CHARACTERISTICS

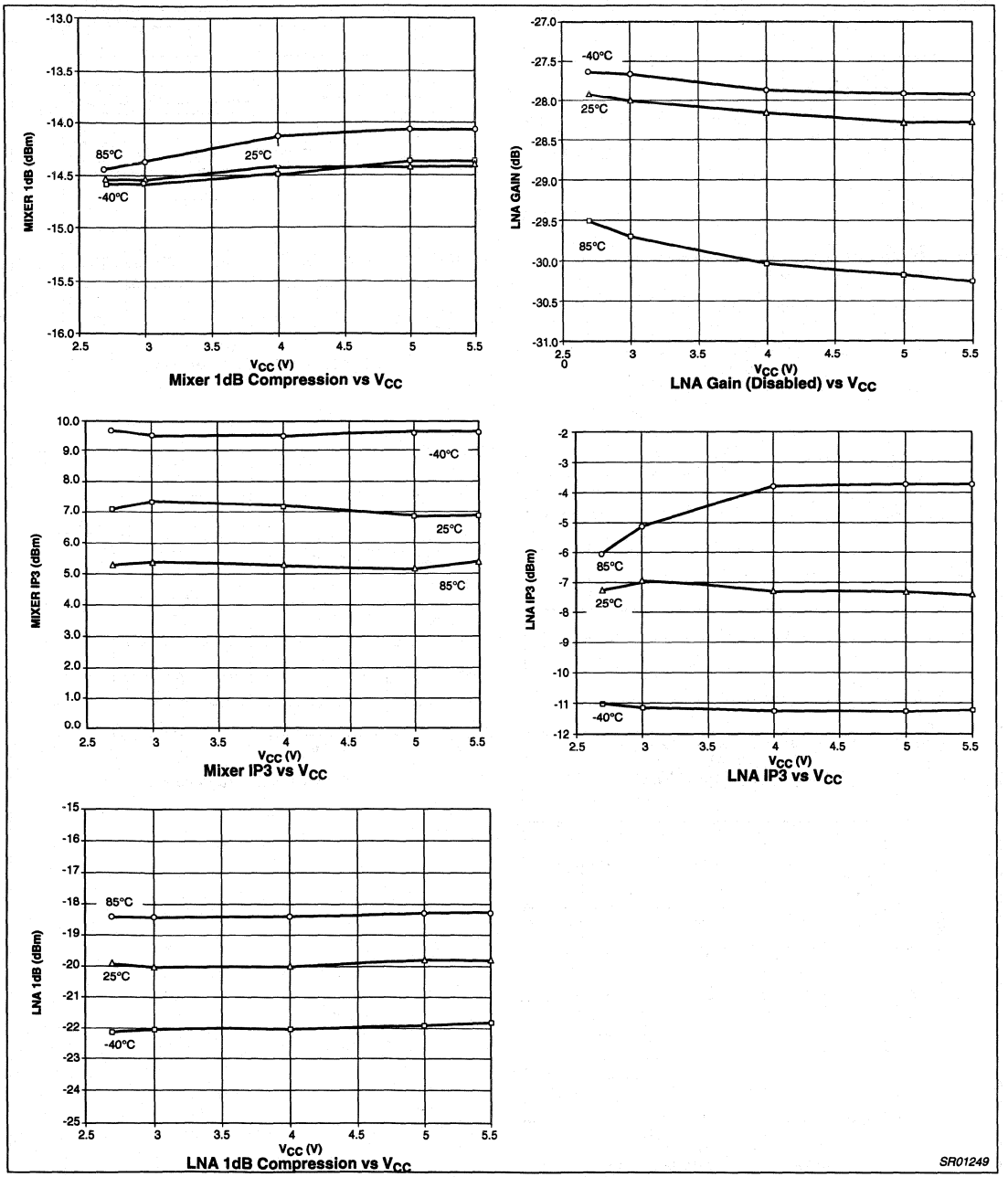
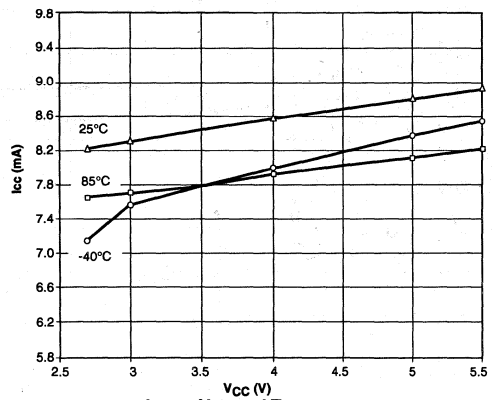
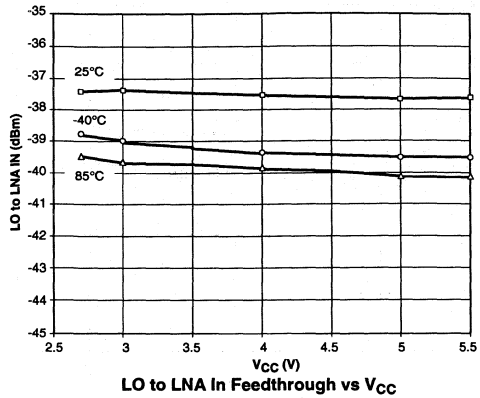


Figure 4.

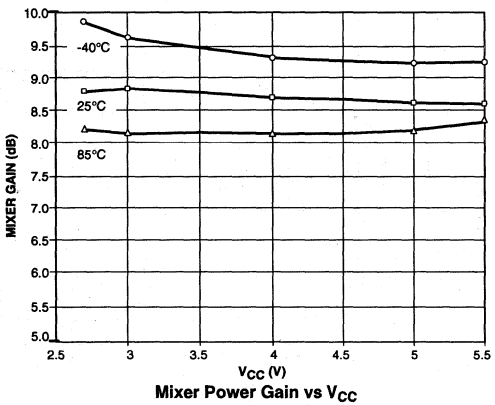
PERFORMANCE CHARACTERISTICS



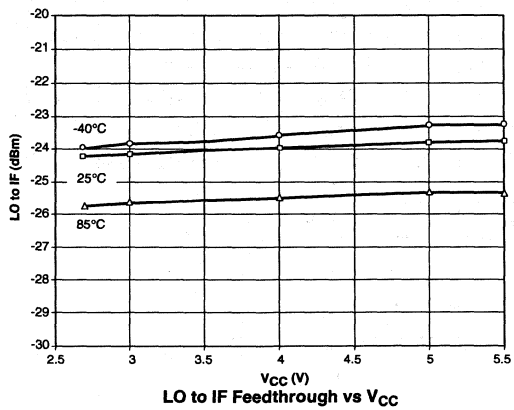
I_{CC} vs V_{CC} and Temperature



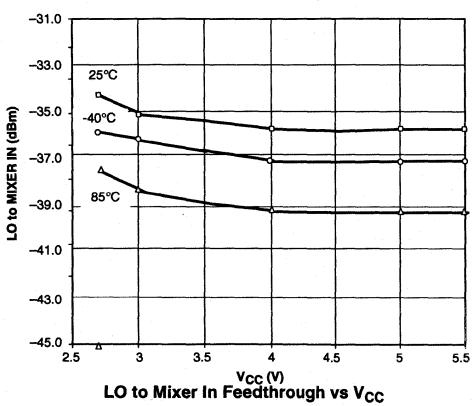
LO to LNA In Feedthrough vs V_{CC}



Mixer Power Gain vs V_{CC}



LO to IF Feedthrough vs V_{CC}



LO to Mixer In Feedthrough vs V_{CC}

SR01250

Figure 5.

PERFORMANCE CHARACTERISTICS

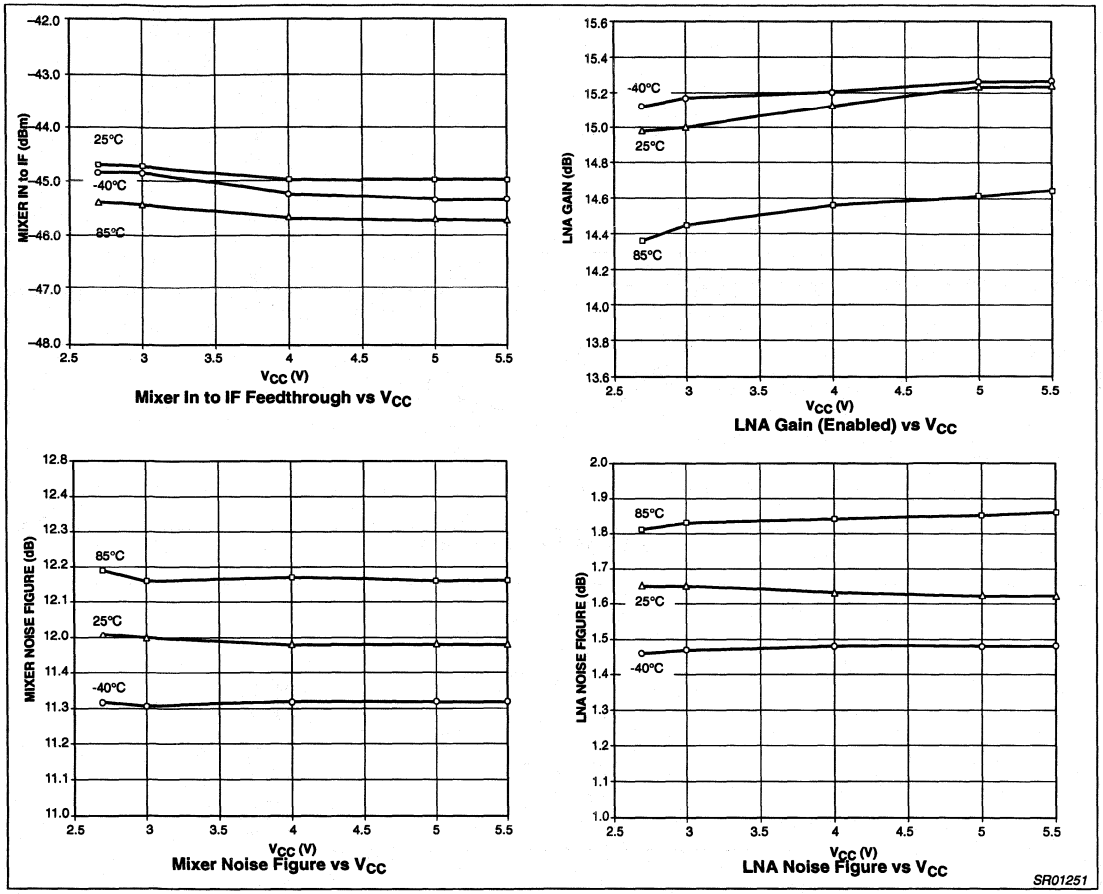


Figure 6.

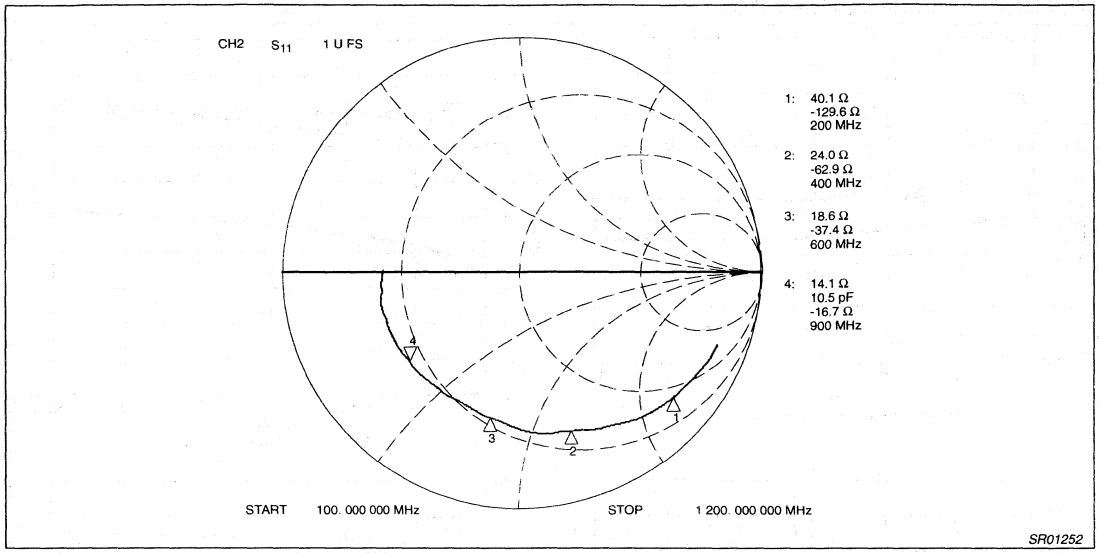


Figure 7. Typical S_{11} of LNA at 3V

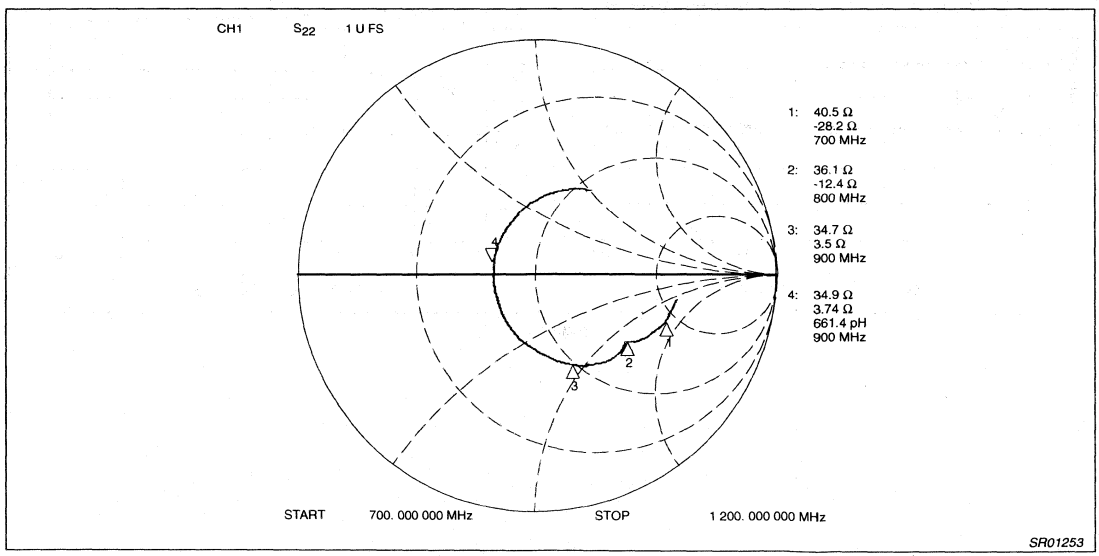


Figure 8. Typical S_{22} of LNA at 3V

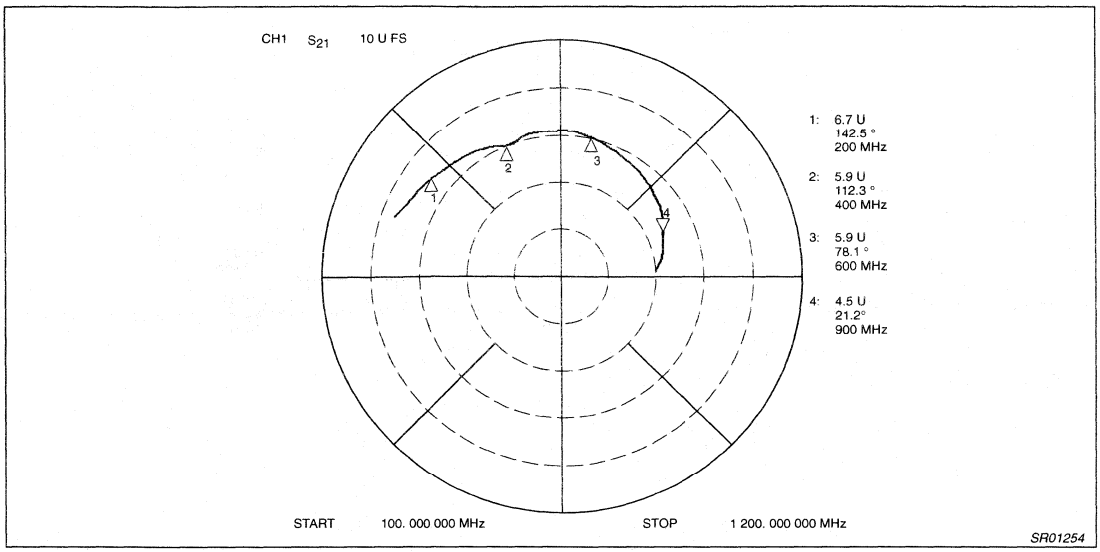


Figure 9. Typical S_{21} of LNA at 3V

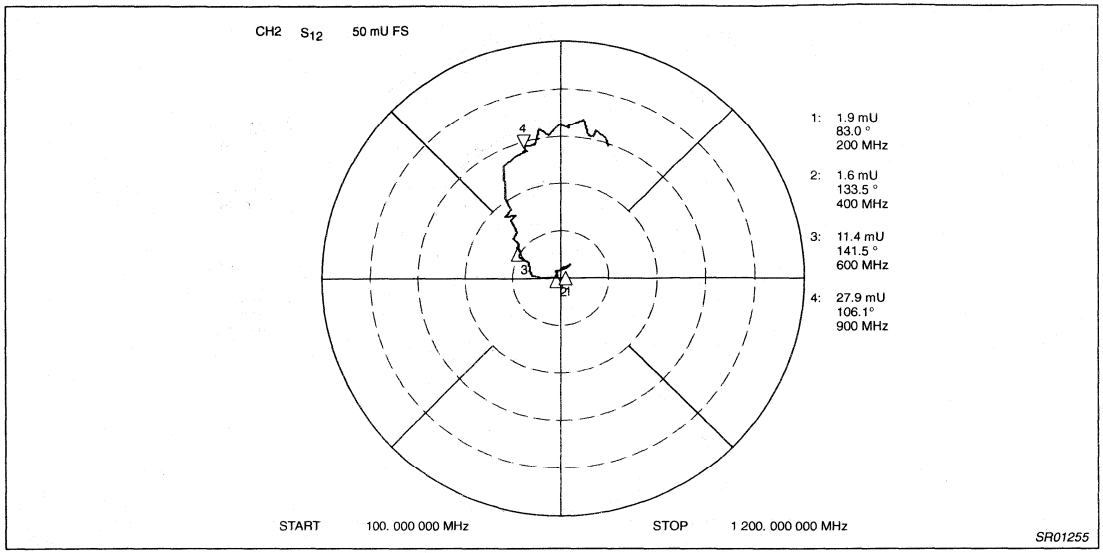


Figure 10. Typical S_{12} of LNA at 3V

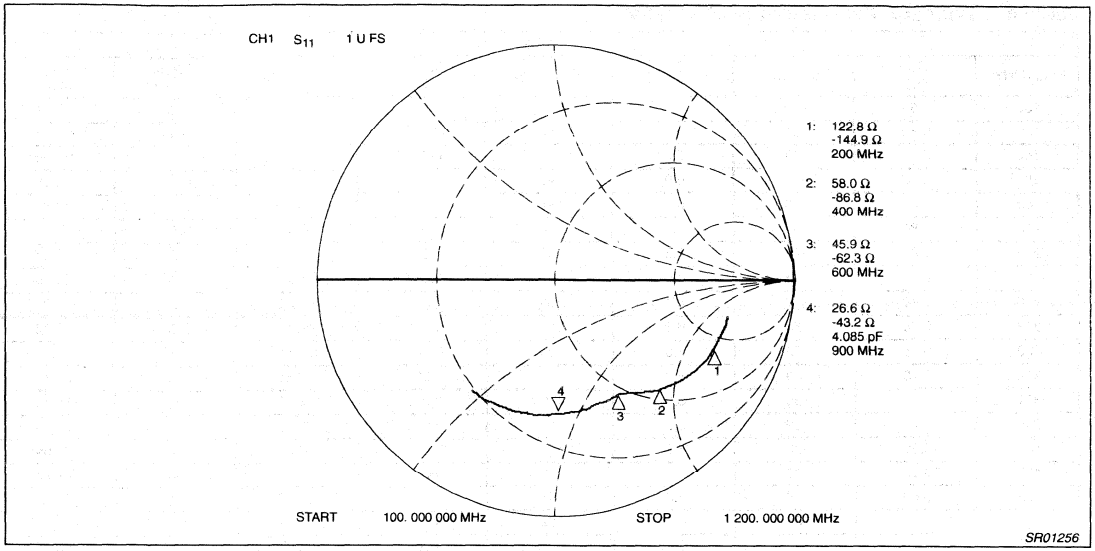


Figure 11. Typical S_{11} of Mixer at 3V

Table 4. Typical S-Parameters of LNA at 3V

LNA								
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)	$\|S_{21}\|$ (U)	$<S_{21}$ (deg)	$\|S_{12}\|$ (U)	$<S_{12}$ (deg)	$\|S_{22}\|$ (U)	$<S_{22}$ (deg)
100	0.86	-20	7.4	160	0.001	91.91	0.59	-9.62
122	0.86	-24	7.1	156	0.001	62	0.58	-11.71
144	0.85	-28	7.0	151	0.001	105.42	0.58	-13.86
166	0.83	-32	6.9	148	0.000	91.65	0.57	-15.89
188	0.82	-36	6.8	144	0.002	100.23	0.57	-17.80
210	0.81	-41	6.7	140	0.002	73.57	0.56	-20.05
232	0.80	-45	6.6	136	0.002	99.70	0.55	-22.37
254	0.79	-48	6.5	133	0.001	84.00	0.54	-24.60
276	0.78	-52	6.4	130	0.001	103.18	0.53	-26.89
298	0.76	-56	6.3	126	0.002	94.33	0.52	-28.72
320	0.75	-59	6.3	123	0.002	66.98	0.51	-30.98
342	0.73	-63	6.2	119	0.002	108.53	0.50	-32.79
364	0.71	-66	6.1	116	0.002	118.13	0.48	-34.68
386	0.70	-69	6.0	113	0.001	103.4	0.47	-36.06
408	0.69	-72	5.9	111	0.001	175.94	0.46	-36.64
430	0.68	-76	5.9	109	0.004	174.1	0.45	-37.21
452	0.69	-78	6.0	106	0.006	162.02	0.46	-38.41
474	0.68	-82	6.1	102	0.007	160.07	0.47	-41.54
496	0.67	-85	6.1	97	0.008	153.6	0.47	-45.75
518	0.66	-89	6.1	93	0.010	146.17	0.46	-50.35
540	0.65	-92	6.1	89	0.009	142.13	0.45	-54.73
562	0.63	-96	6.1	85	0.010	138.49	0.43	-59.16
584	0.62	-99	6.0	81	0.011	146.17	0.42	-63.93
606	0.62	-102	5.9	77	0.011	140.55	0.40	-68.56
628	0.61	-104	5.8	72	0.013	137.2	0.38	-73.48
650	0.61	-107	5.7	69	0.013	130.62	0.36	-78.19
672	0.60	-109	5.7	65	0.016	129.77	0.34	-83.75
694	0.60	-112	5.6	61	0.016	131.94	0.31	-89.81
716	0.59	-115	5.5	57	0.017	128.67	0.29	-96.92
738	0.59	-118	5.5	53	0.019	127.53	0.27	-104.48
760	0.59	-121	5.3	48	0.021	123.42	0.24	-112.81
782	0.59	-124	5.3	44	0.021	122.31	0.22	-122.41
804	0.59	-126	5.1	40	0.022	119.52	0.21	-132.81
826	0.59	-129	5.0	36	0.024	118.29	0.19	-145.39
848	0.59	-132	4.9	31	0.026	115.98	0.18	-159.13
870	0.59	-135	4.8	26	0.027	111.9	0.17	-175.11
892	0.59	-138	4.6	22	0.028	108.11	0.18	169.02
914	0.59	-142	4.5	18	0.028	105.92	0.19	154.96
936	0.59	-144	4.3	14	0.028	106.13	0.20	141.94
958	0.59	-148	4.2	9	0.030	99.79	0.22	130.27
980	0.59	-151	4.0	4	0.031	99.30	0.24	119.5
1002	0.59	-153	3.8	0	0.031	94.81	0.26	110.61
1024	0.59	-157	3.6	-2	0.032	90.91	0.28	102.16
1046	0.59	-160	3.5	-6	0.032	85.65	0.30	94.98
1068	0.59	-164	3.3	-10	0.033	86.10	0.33	88.45
1090	0.59	-167	3.2	-14	0.033	80.59	0.35	82.47
1112	0.59	-170	3.0	-18	0.031	79.18	0.36	77.17
1134	0.58	-172	2.8	-22	0.030	46.32	0.38	71.98
1156	0.58	-175	2.7	-25	0.031	78.57	0.39	67.45
1178	0.57	-178	2.5	-28	0.031	73.66	0.41	62.73
1200	0.57	178	2.4	-31	0.029	71.78	0.42	58.87

Table 5. Typical S-Parameters of Mixer at 3V

Mixer		
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)
100	0.73	-11
122	0.73	-147
144	0.72	-16
166	0.72	-19
188	0.72	-21
210	0.71	-24
232	0.70	-27
254	0.70	-29
276	0.69	-32
298	0.68	-34
320	0.67	-37
342	0.66	-39
364	0.64	-42
386	0.63	—44
408	0.62	-46
430	0.61	-48
452	0.59	-50
474	0.58	-52
496	0.57	-53
518	0.56	-54
540	0.55	-56
562	0.55	-57
584	0.54	-59
606	0.54	-61
628	0.54	-62
650	0.54	-64

Mixer		
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)
672	0.54	-65
694	0.54	-67
716	0.54	-69
738	0.54	-71
760	0.54	-73
782	0.55	-76
804	0.55	-78
826	0.55	-80
848	0.55	-82
870	0.55	-85
892	0.56	-87
914	0.55	-90
936	0.56	-93
958	0.56	-96
980	0.56	-98
1002	0.56	-101
1024	0.57	-104
1046	0.57	-106
1068	0.57	-110
1090	0.57	-112
1112	0.57	-115
1134	0.57	-118
1156	0.57	-121
1178	0.57	-124
1200	0.57	-127

Low voltage front-end circuits: SA601, SA620 AN1777

Author: M. B. Judson

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I. INTRODUCTION

The objectives of this application note are to highlight key features and distinguish key differences between the SA601 and SA620. The power, gain, noise figure, and third-order intercept point of the LNA and mixer will be characterized. A resonant circuit implementing a high loaded-Q μ-strip inductor and an extensive discussion of open-collector mixer outputs and how to match them will also be presented.

The SA601 and SA620 are products designed for high performance low power RF communication applications from 800 to 1200MHz. These chips offer the system designer an alternative to discrete front-end designs which characteristically introduce a great deal of end-product variation, require external biasing components, and require a substantial amount of LO drive. The SA601 and SA620 contain a low noise amplifier and mixer, offering an increase in manufacturability and a minimum of external biasing components due to integration. The LO drive requirements for active mixers are less stringent than passive mixers, thus minimizing LO isolation problems associated with high LO drive-levels. These chips also contain power down circuitry for turning off all or portions of the chip while not in use. This minimizes the average power consumed by the front-end circuitry. The SA620 features an internal VCO that eliminates additional cost and space needed for an external VCO. The SA601 and SA620 fit within a 20-pin surface mount plastic shrink small outline package (SSOP), thus saving a considerable amount of space.

II. KEY ATTRIBUTES OF THE SA601 AND SA620

The primary differences between the SA601 and SA620 are the LNA power down capability, the implementation of the mixer output circuitry, and the incorporation of an integrated VCO.

Table 1 below summarizes the attributes of both parts.

Table 1. Showing SA601 and SA602 Attributes

Product	Diff. Mixer Output	LNA Thru Mode	Mixer Power Down	Int. VCO and VCO Pwr Down
SA601	Yes	No	Yes	No
SA620	No	Yes	Yes	Yes

III. POWER CONSUMPTION

As mentioned above, the average power consumed by the front-end circuitry can be decreased by selectively turning off circuitry that is not in use. The supply current at a given voltage will decrease more than 3mA for each LNA, mixer, or VCO disabled. When the LNA is disabled on the SA620 it is replaced by a 9dB attenuator. This is useful for extending the dynamic range of the receiver when an overload condition exists. Tables 2 and 3 below contain averaged data taken on the SA601 and SA620 while in an application board environment.

Table 2. Showing SA601 Supply Current

V_{CC}	I_{CC} (mA)	I_{CC} (mA) Mixer Disabled
3.0	8.4	4.9
4.0	8.4	4.7
5.0	8.3	4.5

Table 3. Showing SA620 Supply Current

V_{CC}	I_{CC} (mA)	I_{CC} (mA) LNA Disabled	I_{CC} (mA) Mixer Disabled	I_{CC} (mA) VCO Disabled	I_{CC} (mA) Chip Fully Powered Down
3.0	11.4	8.0	8.1	8.2	1.4
4.0	11.6	8.5	8.0	8.2	1.6
5.0	11.7	8.9	8.0	8.2	1.7

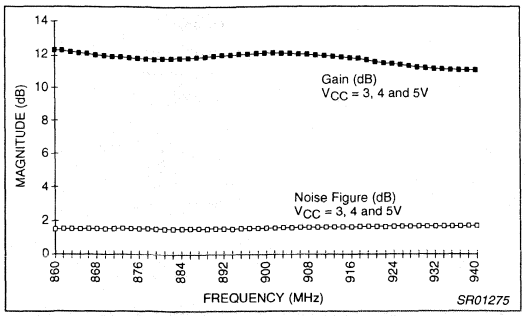


Figure 1. Noise Figure and Gain vs Frequency SA601 LNA

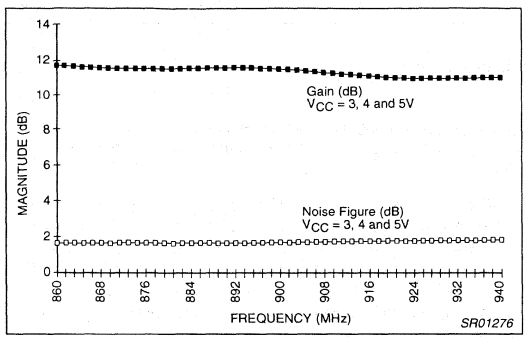


Figure 2. Noise Figure and Gain vs Frequency SA620 LNA

IV. LOW NOISE AMPLIFIERS

The performance of the SA601 and SA620 low noise amplifiers are virtually identical. You can expect an average gain of approximately 11.5 ±1.5dB and a noise figure of approximately 1.6 ±0.3dB. The LNA input and output networks are matched for optimum return loss, gain and best noise figure over the 869 - 894MHz band. They also perform well when utilized in the 902 - 928MHz band without any additional modification to the LNA matching networks. Figures 1 and 2 show gain and noise figure of a typical SA601 and SA620 LNA in the application board environment. Both the gain and the noise figure remain almost constant as V_{CC} is adjusted to 3, 4 and 5V. Therefore, only one curve is shown for clarity.

V. SA620 MIXER

The SA620 mixer is intended for operation with the integrated VCO and employs a single open-collector output structure. The open-collector output structure allows the designer to easily match any high impedance load for maximum power transfer with a minimum of external components. This eliminates the need for elaborate matching networks. The external mixer output circuitry also incorporates a network which distributes the power from the mixer output to two unequal loads. This enables the mixer output to be matched to a high impedance load such as a SAW bandpass filter (typically 1kΩ) while simultaneously providing a 50Ω test point that can be used for production diagnostics. The mixer output circuitry generates the majority of questions for those utilizing this part in their current applications, so some basic concepts regarding open-collector outputs are presented below, as well as a discussion of the network used to provide the 50Ω diagnostic point.

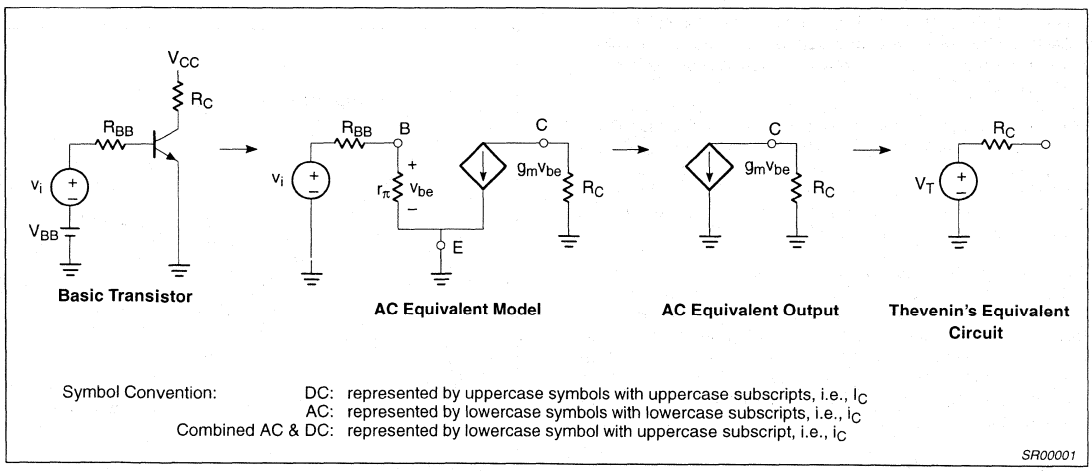


Figure 3. R_C as Source Resistor

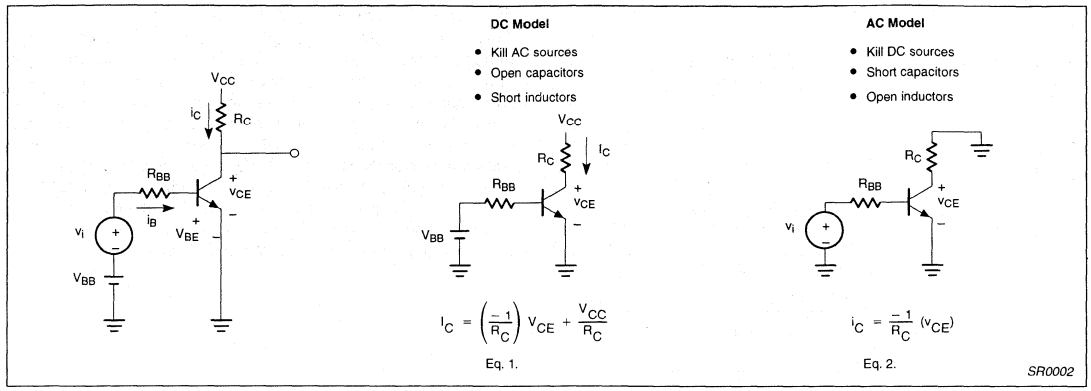


Figure 4. Basic Transistor Analysis

Open-Collector Output Basics [1, 2, 3, 6]

Why R_C Acts Like A Source Resistor

An open-collector output allows a designer the flexibility to choose the value of the R_C resistor. Choosing this resistor value not only sets the DC bias point of the device but also defines the source impedance value. Figure 3 shows the AC model of the transistor. Converting the output structure by applying a Norton and Thevenin transformation, one can conclude that R_C becomes the source resistance. Thus, by choosing R_C to be equal to the load, maximum power transfer will then occur.

Figure 4 shows an active transistor with a collector and base resistor. From basic transistor theory Equation 1 is generated and has the same form as the general equation for a straight line

$$y = mx + b$$

The slope of the DC load line is generated by the value of the collector resistor (m = -1/Rc) and is shown in Figure 5. For a given small signal base current, the collector current is shown by the dotted curve.

The intersection of the dotted curve and the DC load line is called the Quiescent point (Q-point) or DC bias determinant. The location of the Q-point is important because it determines where the transistor is operated; in the cutoff, active, or saturation regions. In most cases, the Q-point should be in the active region because this is where the transistor acts like an amplifier.

Figure 6 shows the ac collector-emitter voltage (V_{CE}) output swing with respect to an AC collector current (i_c). Collector current is determined by the AC voltage presented to the input transistor's base (v_i) because it effects the base current (i_b) which then effects i_c. This is how the v_i is amplified and seen at the output. Recall that this is with no external load (R_{LOAD}) present at the collector. Since no load is present, the AC load line has an identical slope as the DC load line as seen in equation 1 and 2 (m = -1/Rc).

Open-Collector With R_{LOAD}

A filter with some known input impedance is a typical load for the output of the transistor. For simplicity, we will assume a resistive load (R_{LOAD}) and neglect any reactance. Since a resistive load is used (see Figure 7), the AC output swing is measured at V_{OUT} or V_{CE}.

A DC blocking capacitor is used between the R_{LOAD} and the V_{CE} output to assure that the Q-point is not influenced by R_{LOAD}. It is also necessary to avoid passing DC to the load in applications where the load is a SAW filter. However, R_{LOAD} will affect the AC load line which is seen in Equation 4 in Figure 7. Notice that the V_{CE} voltage swing is reduced and thus, the V_{OUT} signal is reduced (see Figure 8).

Since the value of R_C and R_{LOAD} affects the AC load line slope, the value chosen is important. The higher the impedance of R_{LOAD} and Rc, the greater the AC output swing will be at the output, which means more conversion gain in a mixer. This is due to the slope getting flatter, thus allowing for more output swing.

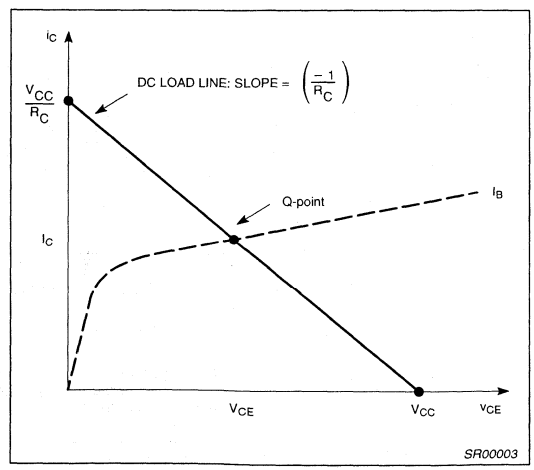


Figure 5. Load Line and Q-Point Graph

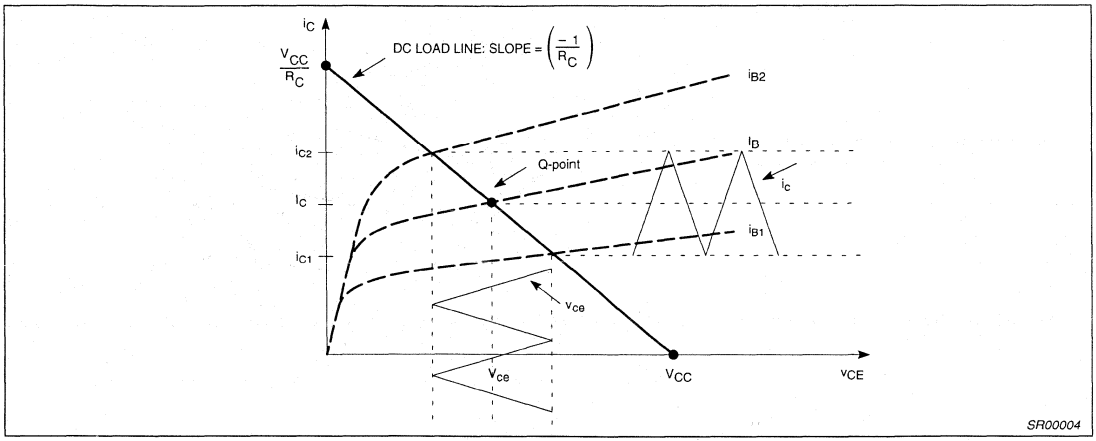


Figure 6. Graphical Analysis for the Circuitry in Figure 4

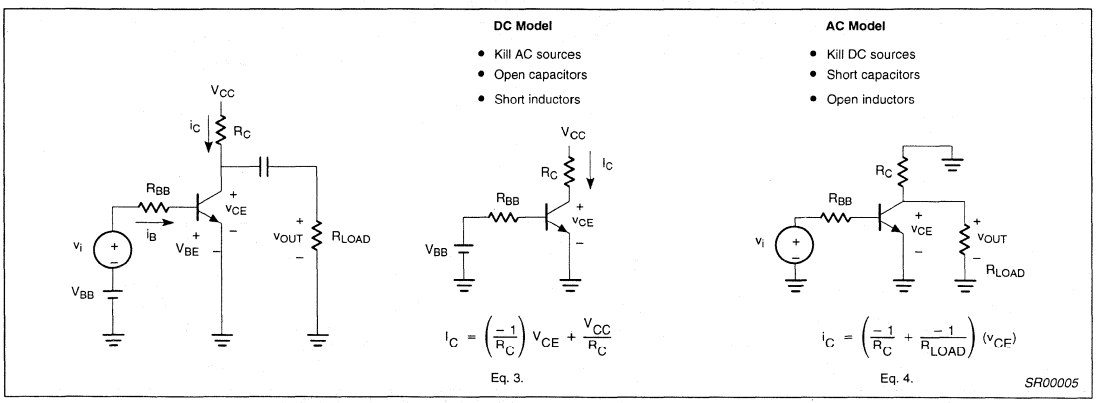


Figure 7. Basic Transistor Analysis with R_{LOAD}

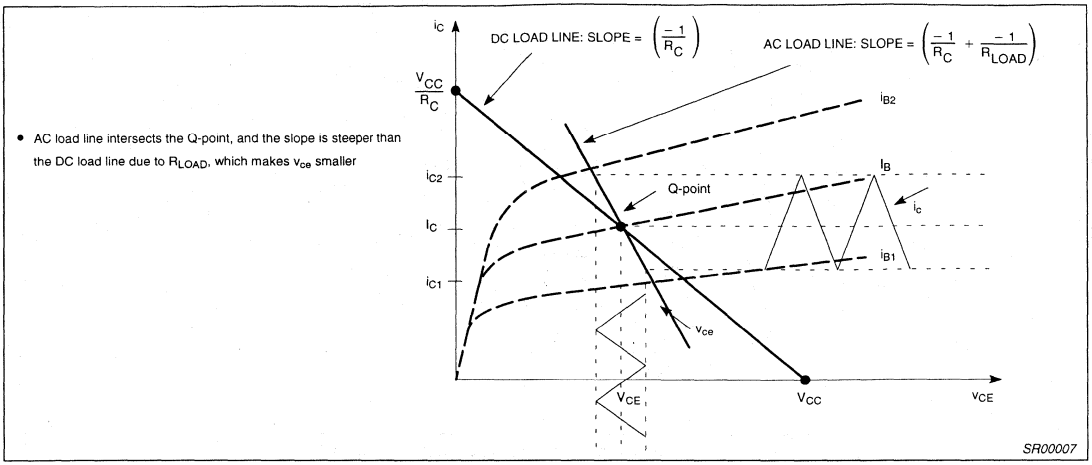


Figure 8. Graphical Analysis for the Circuitry in Figure 7

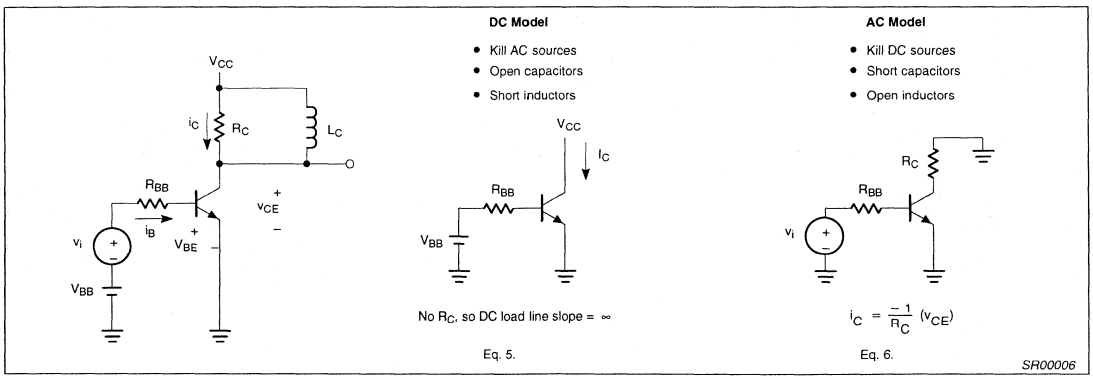


Figure 9. Basic Transistor Analysis with Inductor Added to Collector

Open-Collector With Inductor (L_C)

Adding an inductor in parallel with R_C can increase the AC output signal V_{CE}. Figure 9 shows the DC and AC analysis of this circuit configuration. In Equation 5, there is no R_C influence because the inductor acts like a short in the DC condition. This means the slope of the DC load line is infinite and causes the Q-point to be centered around V_{CC}, thus moving it to the right of the curve. The AC load line slope is set only by R_C because no load is present. Notice that it has the same AC load line slope as the first condition in Figure 4, Equation 2.

Referring to Figure 10, one might notice that the base current (AC and DC) curves spread open as V_{CE} increases. This is caused by a non-infinite early voltage (see Figure 11), which causes the collector current to be dependent on V_{CE}. Taking advantage of this non-ideal condition, the peak-to-peak AC output swing V_{CE}, can thereby be increased by moving the DC Q-point to the right due to the wider spreading between the curves corresponding to different base currents. Figure 12 combines Figures 6 and 10 to show the different AC output signals with different Q-points.

Looking at the AC output level, one might ask how the V_{CE} peak voltage can exceed the supply voltage V_{CC}. Recall that the inductor is an energy storing device (v=Ldi/dt). Therefore, total instantaneous voltage is V_{CC} plus the voltage contribution of the inductor.

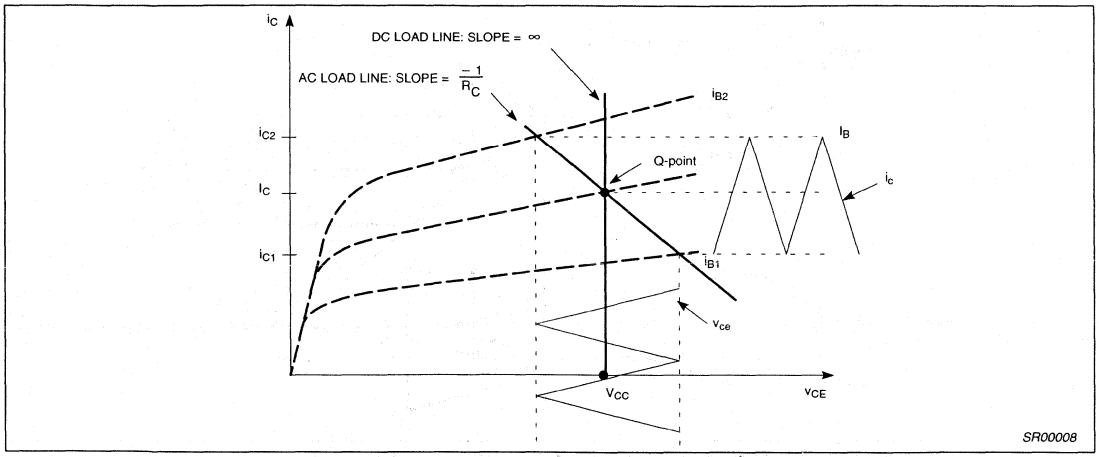


Figure 10. Graphical Analysis for the Circuitry in Figure 9

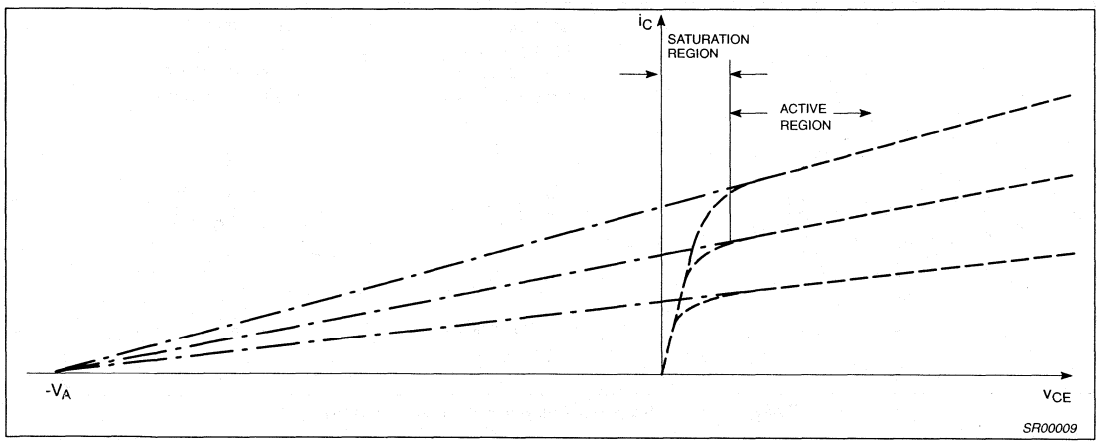


Figure 11. Graphical Representation of Early Voltage Effect

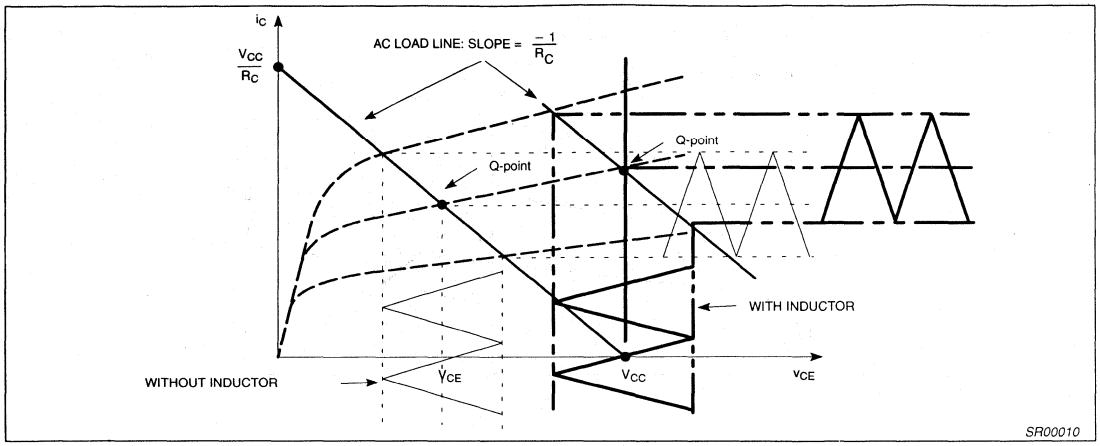


Figure 12. Comparison of Open-Collector Circuit With Inductor vs Without Inductor

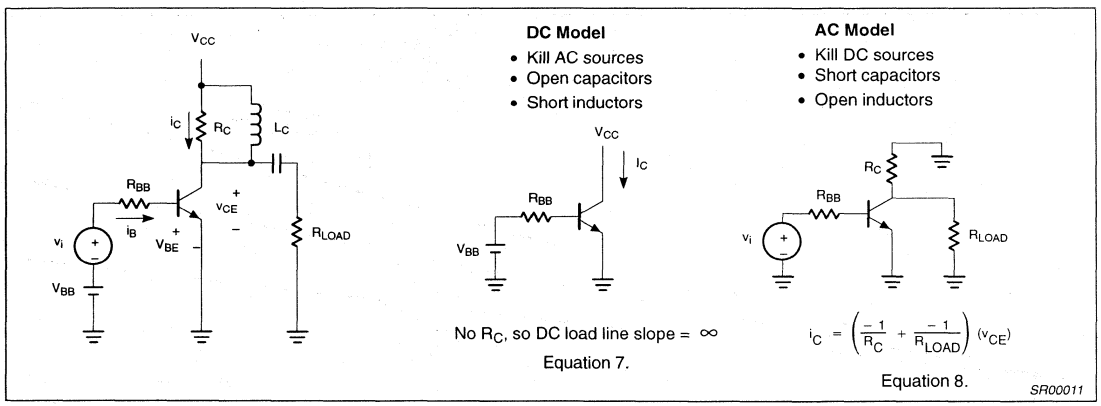


Figure 13. Basic Transistor Analysis with Inductor and R_{LOAD}

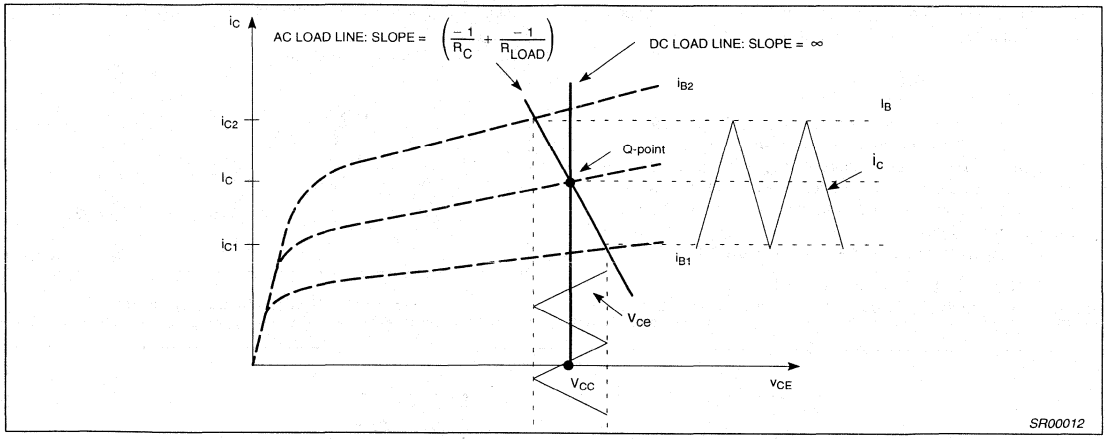


Figure 14. Graphical Analysis for the Circuitry in Figure 13

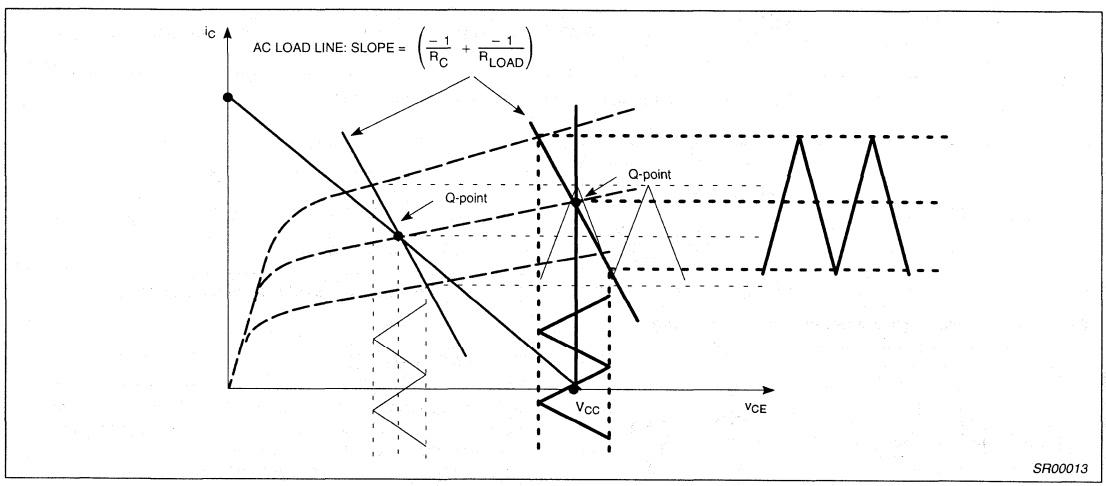


Figure 15. Comparison of Open-Collector R_{LOAD} Circuit With Inductor vs Without Inductor

Open-Collector With Inductor (L_C) and R_{LOAD}

Figure 13 shows the DC and AC analysis with the inductor and load resistor. Again, from the DC analysis, the inductor causes R_C to be non-existent so the DC load line is vertical. In the AC analysis, the AC load line slope is influenced by both R_C and R_{LOAD} resistors (see Equation 8). The AC load line slope is the same as the example of the open-collector without the inductor. Figure 14 shows the response for the open-collector with L_C and R_{LOAD}. Figure 15 combines Figures 8 and 14 showing the increase in AC output swing.

In conclusion, for the load line, R_C plays a role in setting up the bias determined Q-point as well as the AC source impedance. However, when an inductor is placed in parallel with R_C, a different Q-point is set and the AC source impedance is altered. Moving the Q-point takes advantage of the transistor's non-ideal i_c dependence on V_{CE} to get more signal output without having to change the base current. Since R_C is in parallel with R_{LOAD} in the AC condition, it influences the AC load line slope.

VI. FLEXIBLE MATCHING CIRCUIT [6]

A useful variation of the open collector matching concepts previously outlined provides the capability of delivering equal power to two unequal resistive loads. This allows the power delivered to the load to be measured indirectly at another test point in the circuit where the impedance can be arbitrarily defined. If this impedance is defined to be 50Ω, a spectrum analyzer can be easily placed directly into the circuit. This is an excellent troubleshooting technique and a valuable option to have available in high production environments.

Figure 16 shows the schematic for this flexible matching circuit. In this circuit, C_B functions only as a DC blocking capacitor and presents a negligible impedance at the frequency of interest. Recall from the previous open collector matching dicussions that, when R_C

is placed in parallel with an inductor, it has no effect on the Q-point, but does influence the slope of the AC load line as

$$\text{Slope} = \frac{-1}{R_C} + \frac{-1}{R_{LOAD}}.$$

The capacitor C_S functions not only as a DC blocking capacitor, but is also chosen such that the impedance presented by the combination of L, R_C and C_S is equal to R_{LOAD} for optimum power transfer. The analysis is done in the following manner. First, note that inductor L is connected to V_{CC} which is an effective AC ground. So, L can be redrawn to ground. Next, R_C and C_S are converted to their parallel equivalent values as shown in Figure 17.

The resulting parallel LCR circuit is shown in Figure 18. At resonance, the parallel L, C_P combination will be an effective open circuit leaving only R_P. R_P is then simply chosen to be equal to R_{LOAD}.

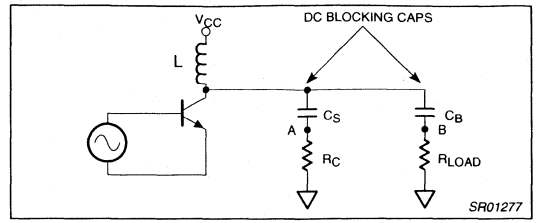


Figure 16. Flexible Matching Circuit

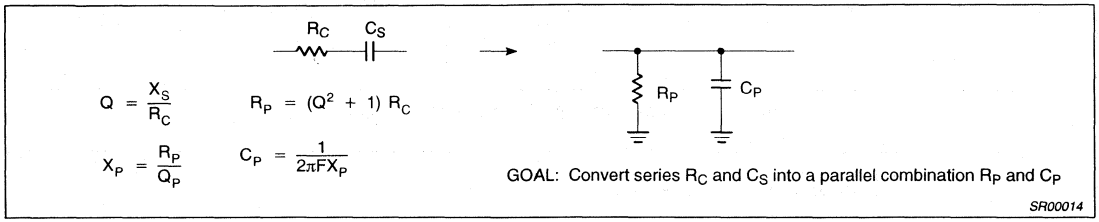


Figure 17. Converting from Series to Parallel Configuration

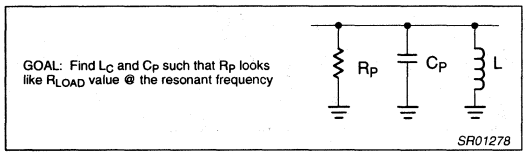


Figure 18. Converting from Series to Parallel Configuration

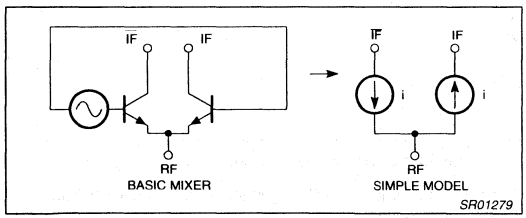


Figure 19. Circuit Model of Differential Open-Collector Output

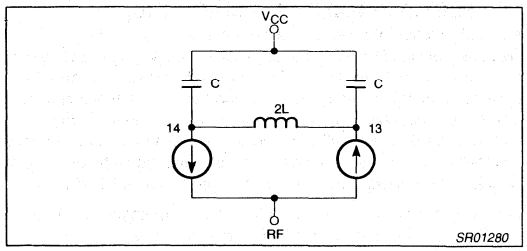


Figure 20. External current-combiner Circuit

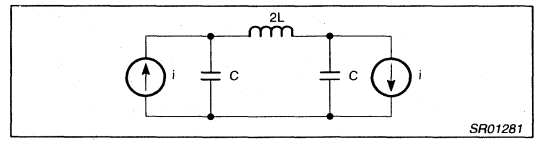


Figure 21. Ideal AC Equivalent Circuit

VII. SA601 MIXER [6]

The SA601 mixer is intended for operation with an external VCO and employs a differential output structure. The current wireless markets demand front-end solutions with low power, and high gain. The differential output offers higher gain than the conventional single-ended open-collector output without an increase in supply current. An equivalent model can be seen in Figure 19. A characteristic of the differential output is that the two output currents are 180° out of phase. This is why the mixer output is labeled IF and $\overline{IF}$.

The current-combiner circuit shown in Figure 20 consists of two capacitors and one inductor. The purpose of the current-combiner is to combine the currents such that they are in phase with one another. By aligning the currents in phase with one another, the output will have a larger AC output swing due to the increased signal current.

Figure 21 shows the ideal AC equivalent model. In the ideal case, it is assumed that all component Q's are high enough to be neglected and the output impedances of the current sources are also high enough to be neglected. By source transformation, the parallel capacitor and current source can be converted to a voltage source and a source capacitor. The inductor, 2L, can be split into two inductors where L becomes the new value (See Step 2 in Figure 22). Since two inductors of equal value in series will be twice that

value, we can split the one inductor into two series inductors each equal to L.

The series capacitor and inductor (L) at resonance will act like a short circuit. Therefore, for this analysis we can redraw the circuit, as seen in Figure 22, step 3.

In Step 4, the voltage source and series inductor (L) is converted back into a current source and parallel inductor. Source transformation, in this simple form, the values of L and C do not change. It is the value of the current and voltage source that changes.

Using Ohm's Law, i=v/z and v = i(1/jωc), while Z =jωL, the imaginary j causes the current to be negative at the resonant frequency specified in Equation 9 of Figure 22. Therefore, by switching the current's direction, the negative sign disappears and the current source is aligned in the same direction as the other one.

VIII. MATCHING THE OPEN-COLLECTOR DIFFERENTIAL OUTPUT

Figure 23 shows the current-combiner and the open-collector matching circuit. The collector current is increased and passes through the load resistor which allows for more AC output swing.

Since the SA601 has differential open-collector outputs, it is possible to implement both a current-combiner and a flexible matching circuit (see Figure 24).

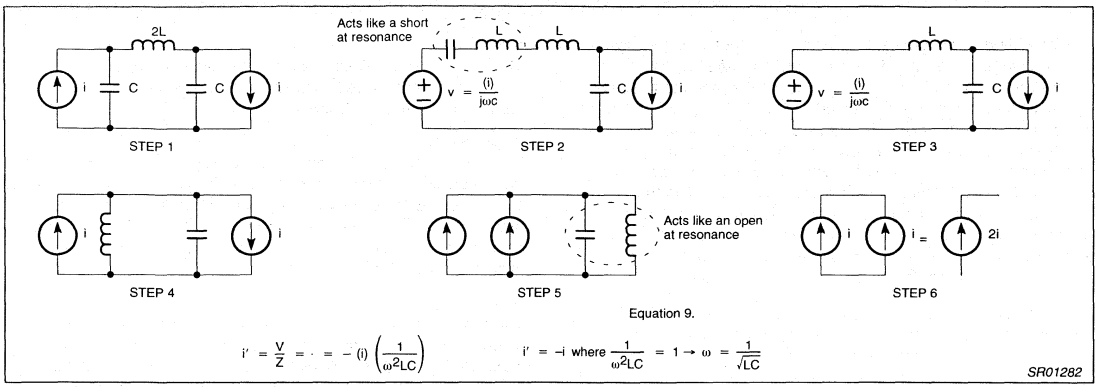


Figure 22. Equivalent Circuit Transformations at Resonance

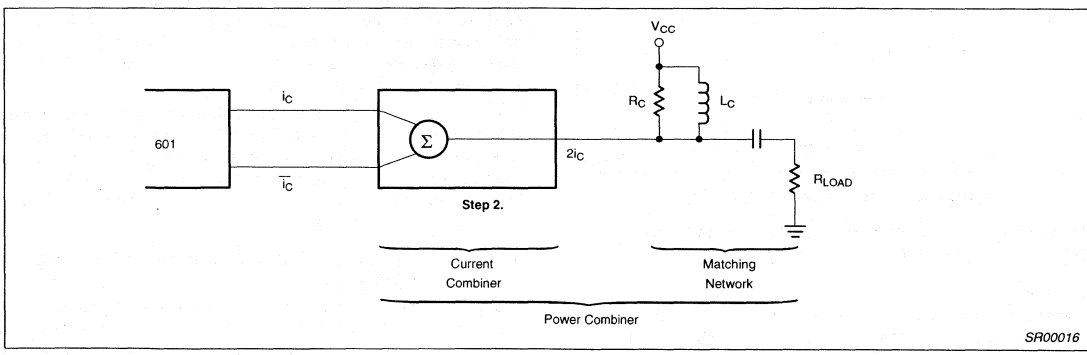


Figure 23. Power Combiner

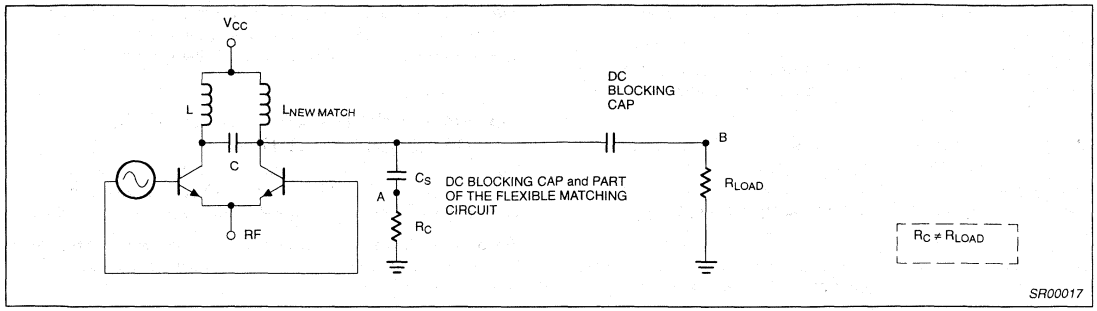


Figure 24. current-combiner with Flexible Matching Circuit

Understanding and implementing the mixer output match is most likely the biggest challenge for those using the SA601. As in most cases, there are many solutions to obtaining the required match for a given circuit. The method selected for the following examples was chosen in order to simply demonstrate some key principles involved in obtaining both high impedance and 50Ω matching while also maintaining some continuity to the previous discussions pertaining to the ideal current-combiner circuit. Each component in the current-combiner/matching circuit will be identified as well as the role each plays in obtaining the required matched condition. In addition, a general procedure for acquiring a good matching circuit along with Smith chart documentation will be provided.

The schematic of the mixer output circuitry utilized on the SA601 demo-board is reproduced here in Figure 25 for convenience.

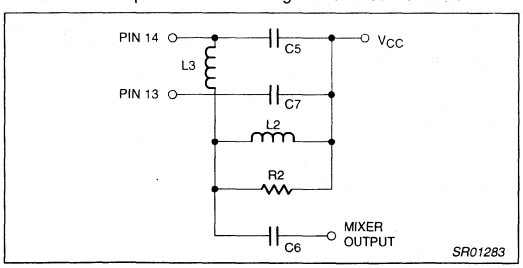


Figure 25. External Mixer Output Circuit

The following is a descriptive summary of the components comprising the external mixer output circuitry.

Inductor L_2
In order to minimize the deviation from the ideal current-combiner circuit, this inductor is chosen to be as large as possible. The inductor will then function only as a choke at the IF frequency and, therefore, should not interact with the current-combiner circuit or effect the matching conditions. This inductor is also necessary to provide the needed DC path from V_{CC} to Pins 13 and 14. In all the examples to follow, a 6.8µH inductor was used for L_2.

Capacitors C_5 and C_7
Also, in order to adhere to the analysis set forth in the ideal current-combiner discussions, these capacitors will be set equal to each other in the examples to follow. The main function of these capacitors is to define the resonant frequency of the current-combiner. They also play a secondary role in defining the output impedance.

Inductor L_3
This inductor also defines the resonant frequency of the current-combiner as well as the output impedance of the current-combiner at resonance.

Capacitor C_6
This capacitor is used to determine the output impedance for 50Ω matches only. For high impedance matches greater than or equal to 1kΩ this capacitor is not very effective. Thus, in this case it is usually replaced with a large capacitance value, adding almost no contribution to the match. A 1000pF is used in the high impedance examples that follow.

Resistor R_2
This resistor is used to simplify the high impedance matching process. In a 50Ω match, the series impedance presented by capacitor C_6 greatly simplifies the process of moving to the 50Ω point on the Smith chart. At high impedance, C_6 is no longer effective and it is often extremely difficult to obtain the proper match by varying just the components associated with the current-combiner circuit. A simple solution to this problem is to obtain the proper resonance condition at a higher impedance than the targeted impedance and then reduce it by placing a resistor of the correct value in parallel with it.

The best way to configure the mixer output circuitry for optimum gain is to optimize the return loss (S_{11}) for this port at the required IF. This, by itself, does not guarantee that optimum gain will occur at this frequency due to the phase relationships of the signals inside the current-combiner, but it is usually very close. The best tool available for this is a network analyzer.

Method of Achieving High Impedance Matching with a Network Analyzer

The network analyzer lends itself very nicely to obtaining 50Ω matches. However, for high impedance matches the Smith chart data will be far to the right of the chart and will be inaccurate, hard to read, and hard to interpret. If the network analyzer were normalized to the impedance value to which you want to match, the data would be in the center of the Smith chart and easy to interpret.

One method of doing this is to disconnect the 'A' port from an HP network analyzer and attach a high impedance probe to this port. Next take an SMA connector (or whatever connector type your analyzer uses) and solder two resistors each equal to the target impedance in the following manner: Solder one end of one of the resistors to the center lead of the connector and leave the other end open. This resistor will define the normalization on the network analyzer during calibration. Next, solder one end of the other resistor to the ground of the connector and leave the other end

open. This resistor will function as a dummy load during calibration. Connect this SMA connector to port '1' on the network analyzer. You are now ready to calibrate. Prior to initiating the open portion of the one-port calibration procedure, contact the open end of the resistor soldered to the center lead of the connector with the high impedance probe (see Figure 26). After this has been completed, contact ground on the connector with the high impedance probe prior to initiating the short portion of the one-port calibration procedure (see Figure 26). Then connect the two open ends of the resistors with solder. Prior to initiating the load portion of the one-port calibration procedure, contact the connection between the resistors with the high impedance probe (see Figure 27). The network analyzer should now be normalized to your target impedance. Thus, the optimum match will once again be in the center of the chart. When making connection to a circuit it is necessary to include a resistor of the same value used during the calibration between the center lead of the connector and its connection to the circuit. Impedance measurements are taken by contacting the high impedance probe at the end of this resistor nearest the circuit (see Figure 28).

Another tip concerning the calibration of the network analyzer should be mentioned. It is often useful to be able to look at a Smith chart over more than one frequency range. A wide frequency range is useful initially when your results are far off the target. Then the narrower range is useful for fine tuning your results. So, it is recommended that you calibrate in both frequency ranges and save the settings in the internal registers of the network analyzer if possible.

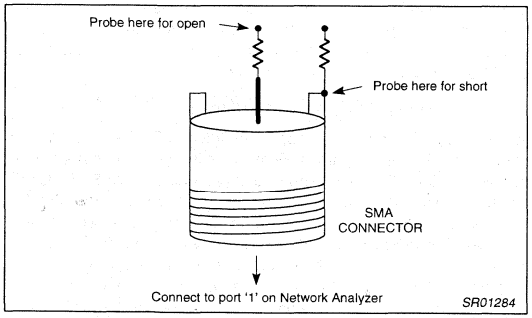


Figure 26. Open- and Short-circuit Calibration Locations

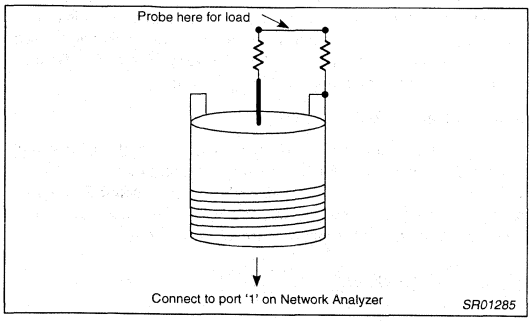


Figure 27. Load Impedance Calibration Location

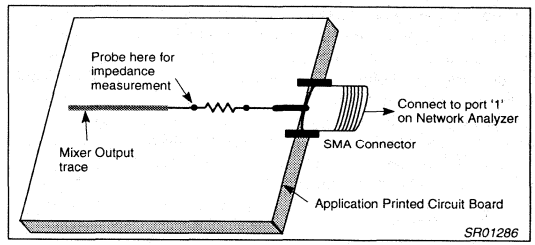


Figure 28. PCB Impedance Measurement Configuration

Non-Ideal Current-Combiner Ckt Considerations

Before we go through some actual impedance matching examples, some key differences between the ideal current-combiner circuit presented earlier and a non-ideal circuit which takes into account the finite Q of inductor L_3 as well as the output impedances of the current sources should be discussed. Through a series of Thevenin/Norton conversions and Series/Parallel equivalent impedance conversions similar to the analysis of the ideal circuit, the mixer output circuit can be modeled by the circuit shown in Figure 29.

The two main things to note in this circuit are the presence of the shunt resistors, R_O and R_Q, and that the current-combiner circuit looks like a simple parallel LRC circuit to capacitor C_6.

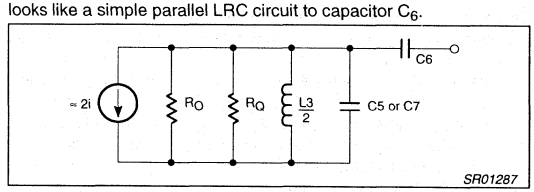


Figure 29. Non-ideal Mixer Output Equivalent Circuit

The significance of the resistors is their role in determining the output impedance of the overall circuit. R_Q is smaller in value than R_O which is the relatively high impedance of the open-collector outputs. Thus, because they are in parallel, R_Q defines the output impedance of the current-combiner circuit at resonance. The value of R_Q is a function of frequency, the component Q of inductor L_3, and the inductance value of inductor L_3. We do not have direct control over component Q or frequency, so the value of R_Q is adjusted by simply changing the value of inductor L_3. A more detailed explanation of this will be shown in the examples to follow.

It is not intuitively obvious why the matching portion of the mixer output circuitry used to obtain the 50Ω matches is composed of a single series capacitance. Many customers using the SA601 have asked why this works because it does not seem to adhere to basic two element matching concepts. To answer this, let's first take a quick look at the general parallel LC circuit shown in Figure 30. This circuit will resonate according to the simple resonance calculation

$$\omega = \frac{1}{\sqrt{LC}}$$

If the capacitor of this circuit is cut in half and the inductor is equivalently represented by two parallel inductors, the circuit in Figure 31 results. At the original resonant frequency $\omega = \frac{1}{\sqrt{LC}}$, the capacitor and one of the inductors will resonate $\omega = [(0.5C)\ (2L)]^{-\frac{1}{2}} = (LC)^{-\frac{1}{2}}$. What is left over is a shunt inductance of 2L presented to the output. Thus, the general

principle is that by decreasing the capacitance of a parallel LC circuit, you will present a shunt inductance to the output of that circuit at the same frequency. This concept when applied to the circuit in Figure 29 offers an explanation of where the missing shunt inductance element is coming from. If capacitors C_5 and C_7 are decreased, this will present a shunt inductance to capacitor C_6. Thus, two element matching concepts would still apply to this circuit. How much inductance is referred to C_6, and what value of C_6 it takes to obtain the matching conditions, is difficult to predict. So, we will rely on the network analyzer to point us in the right direction.

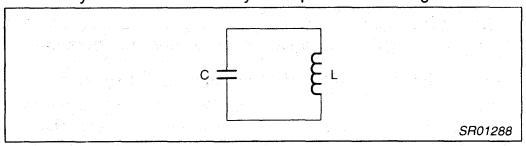


Figure 30. Parallel L_C Network

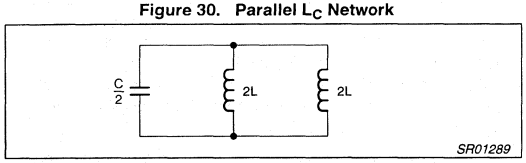


Figure 31. Parallel L_C Network with Decreased Capacitance

One of the most frustrating parts of matching on the network analyzer is it often does not give you very much information until you are at least "in the ball park" of the component values required. The first example will purposely begin with component values to create this condition to give an idea of what might initially be encountered. Additionally, Table 4 at the end of this section contains values for the components required to obtain optimum gain from the mixer at IF frequencies of 45, 83 and 110MHz at both a high impedance of 1kΩ and a low impedance of 50Ω. Using this table you should be able to obtain a good guess for the initial values for your particular application.

IX. MATCHING EXAMPLES

A procedure for acquiring a good high impedance matching circuit for providing optimum gain from the mixer output can be summarized as follows:

1. Normalize the network analyzer to the impedance of interest.
2. Set inductor L_2 to be a large inductance value.
3. Choose "ball park" values for the initial component values based on the simple resonance calculation and /or the tabulated data provided in Table 4.
4. Adjust $C_{5,7}$ to obtain the required match.
5. If the output impedance at resonance is above its target and resonance occurs at the targeted IF, the required match can be obtained with the appropriate value for R_2.
6. If the resonant frequency is above the target IF and the output impedance at resonance is below its target, change inductor L_3 to a higher value and return to step 4.
7. If the resonant frequency is below the target IF and the output impedance at resonance is above its target, change inductor L_3 to a lower value and return to step 4.
8. Design a matching circuit to bring the impedance back down to 50Ω.
9. Make final fine tuning adjustments to $C_{5,7}$ based on the frequency response as observed on a spectrum analyzer.

A procedure for acquiring a good 50Ω impedance matching circuit for providing optimum gain from the mixer output can be summarized as follows:

1. Set inductor L_2 to be a large inductance value.
2. Choose "ball park" values for the initial component values based on the simple resonance calculation and/or the tabulated data provided.
3. If the output impedance at resonance is greater than its target, increase capacitor C_6 until the curve on the Smith chart passes through the center of the chart.
4. If the output impedance at resonance is less than its target, decrease capacitor C_6 until the curve on the Smith chart passes through the center of the chart.
5. If the resonant frequency is greater than the target IF, increase the values of C_5 and C_6 until resonance occurs at the target IF.
6. If the resonant frequency is less than the target IF, decrease the values of C_5 and C_6 until resonance occurs at the target IF.
7. Make final fine tuning adjustments to $C_{5,7}$ based on the frequency response as observed on a spectrum analyzer.

83MHz, 1 kΩ Match

The objective of the first matching circuit we will look at is intended to provide a 1kΩ match at 83MHz. It has inductance values L_2 = 6.8μH and L_3 = 270nH. (These will be the values for these inductors in all the examples unless stated otherwise.) This match is a high impedance 1kΩ match so capacitance C_6 was set to 1000 pF. The simple resonant calculation

$$\omega = [(0.5CL)]^{-\frac{1}{2}} = [(0.5)\ (270nH)\ (C)]^{-\frac{1}{2}} = 2\pi\ (83MHz)$$

suggests that $C_{5,7}$ should be approximately 27pF. The actual value needed to optimize the gain is always less than the value predicted by this equation. Figure 32 shows what an unfavorable Smith Chart might look like when you go in the wrong direction. In this example $C_{5,7}$ was set to 33pF. The chart shows resonance does not occur anywhere between 75 and 95MHz. If you were to continue this curve, it would eventually hit the real axis at a much lower frequency. According to the simple resonance calculation this suggests that our capacitance value is too large. As $C_{5,7}$ is decreased, the plot on the Smith chart starts to resemble a constant admittance circle. Figure 33 shows that a $C_{5,7}$ value of 23pF yields a more favorable curve where resonance occurs at 83MHz as desired. The only problem is the impedance at resonance is not 1kΩ as desired. The Smith chart in Figure 33 has been normalized to 1kΩ. The real part coordinate of 61.984Ω. shown on the Smith chart must be converted in the following manner:

Z_O = (61.984/50) (1kΩ) = 1.24kΩ.

We could at this point choose another value for inductor L_3 and then again find the right value for $C_{5,7}$ to acquire resonance. However, we will take this opportunity to demonstrate how resistor R_2 might be used. The needed shunt resistance R_2 can be calculated from the simple formula for combining parallel resistances.

$$R_2 = \frac{(Z_O)\ (Z_{TARGET})}{(Z_O - Z_{TARGET})} = \frac{(1.24)\ (1)}{(1.24 - 1)} = 5.17k\Omega$$

Figures 34 and 35 show the resulting output match when a 5kΩ resistor is used for R_2.

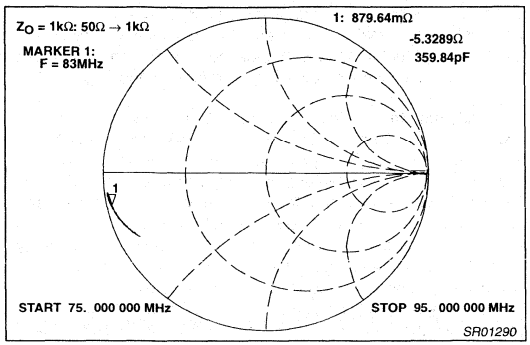


Figure 32. Smith Chart S_{11}: Showing Poor Initial Conditions

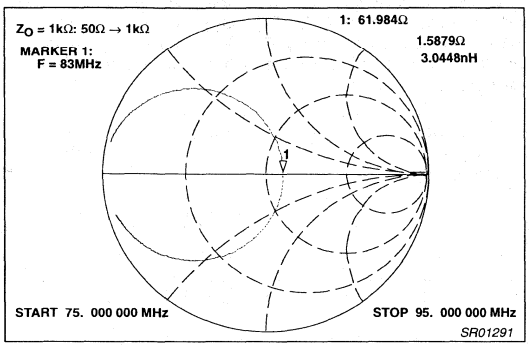


Figure 33. Smith Chart S_{11}: Showing Targeted Resonant Frequency, But Output Impedance Is Too High

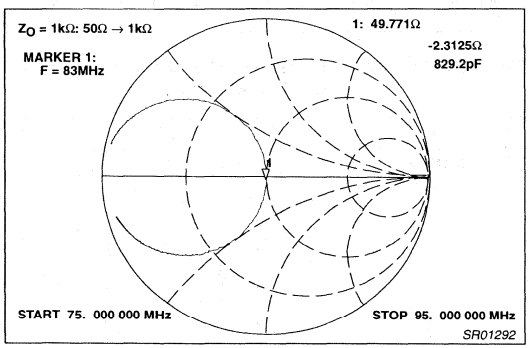


Figure 34. Smith Chart S_{11}: Showing Targeted Resonant Frequency And Output Impedance

In order to verify the high impedance match in the absence of a system in which to test it, a wideband matching circuit was designed to convert the high impedance 1kΩ match back down to 50Ω where it can then be terminated into a standard 50Ω test equipment port. Figures 36, 37 and 38 show the design of such a circuit. A detailed discussion of the design of this type of circuit can be found in [1]. Figure 39 shows the frequency response of the mixer output as the LO was varied to change the IF output. The envelope of this response has been added for clarity. The RF input signal to the mixer was -30dBm. So, the plot shows a very favorable gain of approximately 10.6dB at 81.75MHz. At 83MHz, which is the intended IF, the gain is only about 1dB lower.

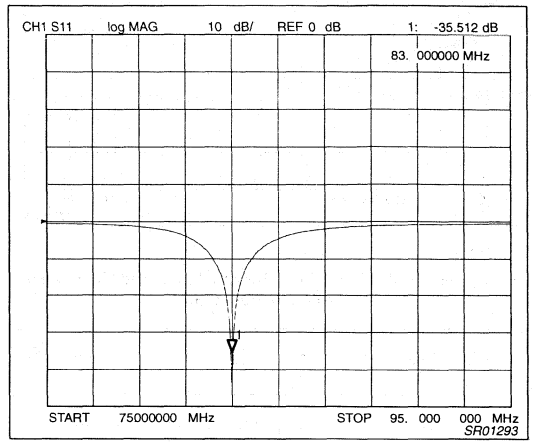


Figure 35. S_{11} Reflection at Mixer Output

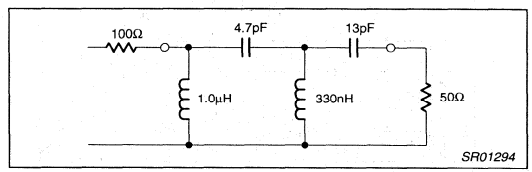


Figure 36. Wideband 1kΩ to 50Ω Matching Network

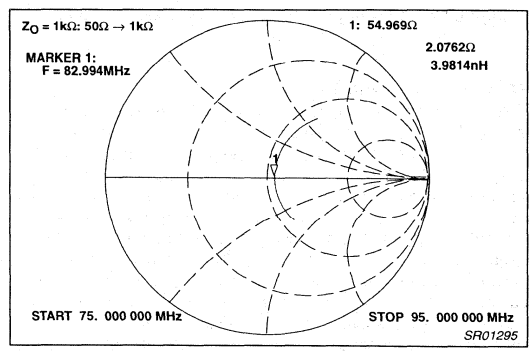


Figure 37. Smith Chart S_{11}: Showing Wideband Matching of Circuit in Figure 36

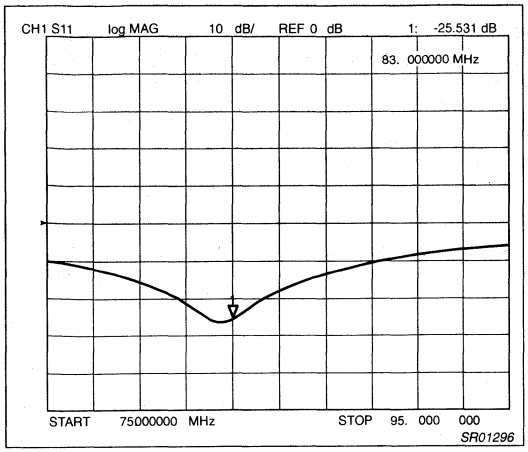


Figure 38. Smith Chart S_{11}: Showing Wideband Matching of Circuit in Figure 36

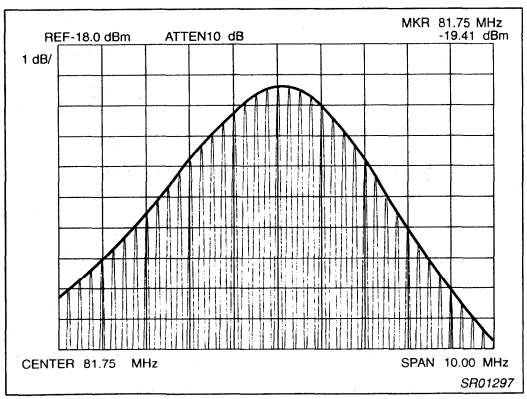


Figure 39. Showing the Frequency Response of the Mixer Output

45MHz, 1 kΩ Match

The next example is designed to show how to determine when inductor L3 is too low or too high to enable you to acquire the proper matching conditions. The objective is to provide a 1kΩ match at the much lower IF of 45MHz. Before we can determine if we have the wrong inductance value for L_3, we must first understand what effect adjusting C_5 and C_7 has on the circuit. The simple resonance calculation suggests that a decrease in $C_{5,7}$ should increase the frequency at which resonance occurs. This also causes a change in the output impedance at resonance. When $C_{5,7}$ is decreased the output impedance at the new higher resonant frequency will also be higher. As $C_{5,7}$ is adjusted the resonant frequency and the output impedance at resonance will change in the same direction. In other words, both will increase as $C_{5,7}$ is decreased or both will decrease as $C_{5,7}$ is increased. This means that if a condition exists where the resonant frequency is greater than the target IF and the impedance at resonance is below its target, the inductance value used for inductor L_3 is too small. Conversely, if the resonant frequency is less than the target IF and the impedance at resonance is greater than its target, the inductance value used for L_3 is too large.

To demonstrate these concepts, inductor L_3 was chosen to be larger than usual (L_3 = 750nH) and $C_{5,7}$ was also chosen to be much larger than usual ($C_{5,7}$ = 82pF). Capacitor C_6 was again set to 1000pF making it negligible during high impedance matching. Again, it should be noted that the following Smith charts have been normalized to 1kΩ. Figure 40 shows that the component values listed above yield a 1kΩ output impedance at a resonant frequency of just 28MHz instead of the 45MHz target IF. In an effort to increase the resonant frequency $C_{5,7}$ was decreased to 33pF. Figure 41 shows that the resonant frequency is close but below the target IF and the impedance is well above 1kΩ. According to the discussions above, this suggests that inductor L3 is too large. Figure 42 shows the results when inductor L3 is decreased to 620nH. This chart shows that both the resonant frequency and the impedance at resonance are greater than their targeted values. This indicates that there is still a chance that the match can be made with some further adjustment of $C_{5,7}$. $C_{5,7}$ was increased to 39pF to lower the resonant frequency. Figure 43 shows that when this was done the condition that suggests that inductor L_3 is too large still exists.

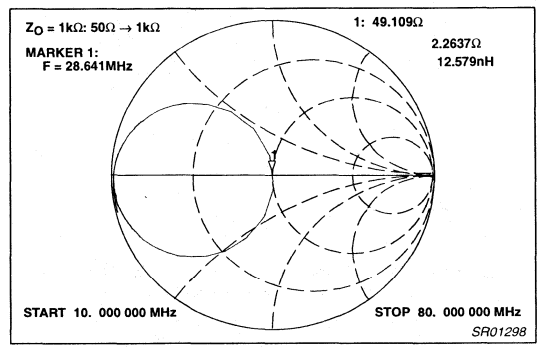


Figure 40. Smith Chart S_{11}: Showing Resonant Frequency Well Below 45MHz Target

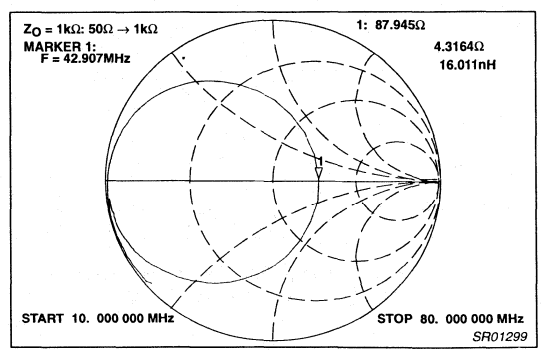


Figure 41. Smith Chart S_{11}: Showing Output Impedance Well Above the 1kΩ Target

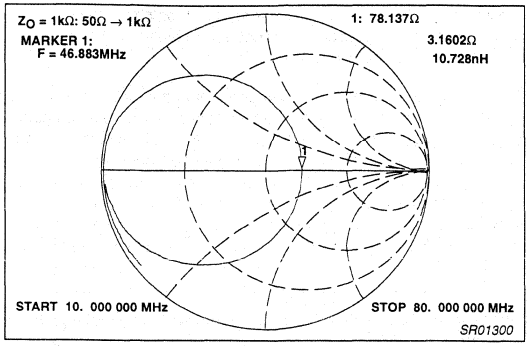


Figure 42. Smith Chart S_{11} , L_3 = 620nH: Showing the Resonant Frequency and the Output Impedance are Both Above the 45MHz, 1kΩ Target Values

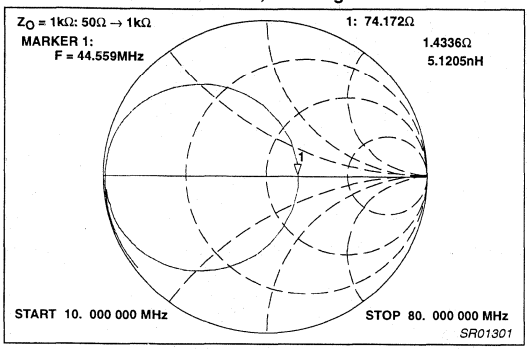


Figure 43. Smith Chart S_{11} , L_3 = 620nH: Showing the Resonant Frequency Below 45MHz Target and Output Impedance Above 1kΩ Target Values

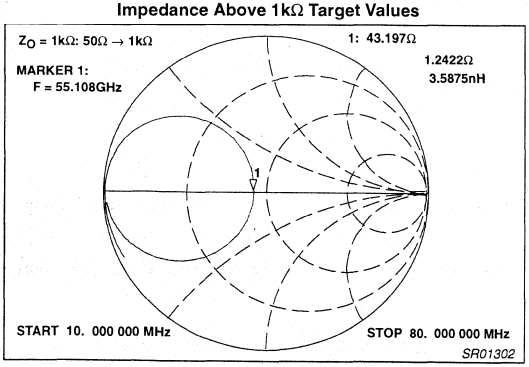


Figure 44. Smith Chart S_{11} , L_3 = 270nH: Showing the Resonant Frequency Above 45MHz Target and the Output Impedance Less than 1kΩ Target Values

Next, in order to demonstrate the other condition, inductance L_3 was changed to 270nH and $C_{5,7}$ was changed to 56pF. Figure 44 shows that the resonant frequency is greater than the target IF and the output impedance at resonance is less than 1kΩ. According to the discussions above, this is the condition which suggests that inductance L_3 is too small. So, inductance L_3 was then increased to 390nH. Figure 45 shows that the 390nH inductance yields a resonant frequency and an output impedance at resonance that are both slightly above their targets. At this point you are close enough to use another wideband matching circuit for dropping the 1kΩ impedance to 50Ω allowing you to check the frequency response directly. It was determined that changing $C_{5,7}$ from 56pF to 62pF yielded optimum gain at exactly the target IF. Figure 46 shows this gain to be approximately 10dB.

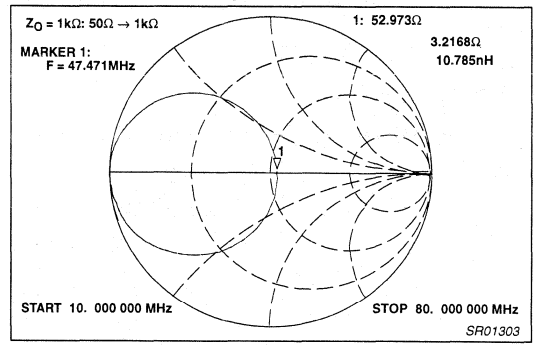


Figure 45. Smith Chart S_{11} , L_3 = 390nH

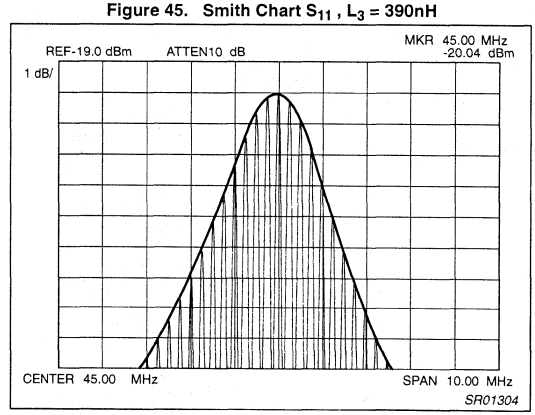


Figure 46. Frequency Response of the Mixer Output

110.592MHz, 50Ω Match

The next example will demonstrate how to obtain a 50Ω match. There are a couple of things to note concerning matching at a higher IF. The first is to expect an increase in the general sensitivity of the matching conditions with relatively small component variations. Secondly, the difference in frequency between the point of optimum gain and the point where the return loss (S_{11}) is minimized greatly increases when matching at a higher IF. To demonstrate these things the objective of the following example will be to provide a 50Ω match at 110.592MHz, which is a relatively high 1st IF.

The initial component values for this matching circuit (see Figure 25 are 6.8uH and 270nH for inductances L_2 and L_3, respectively. Capacitors C_5, C_6 and C_7 were all set to 10pF. It should be noted that C_6 is no longer set at 1000pF and plays a major role in determining the required match at 50Ω as we will see. Figure 47 shows the results of the initial component values. The Smith chart indicates that the resonance frequency is much too low and the impedance at resonance is too high. In our previous high

impedance matching discussions this meant that the inductor L_3 was too Large. In 50Ω matching this is no longer the case. Due to the lower impedance matching condition, the output impedance at resonance can now be significantly altered by varying the series capacitance element C_6. As mentioned previously, the matching circuit is much more sensitive to component variations at a higher IF. Figure 48 shows a small change in $C_{5,7}$ from 10pF to 4.7pF caused the resonant frequency to shift from well above the target IF to well below the target IF with very little change in the output impedance at resonance.

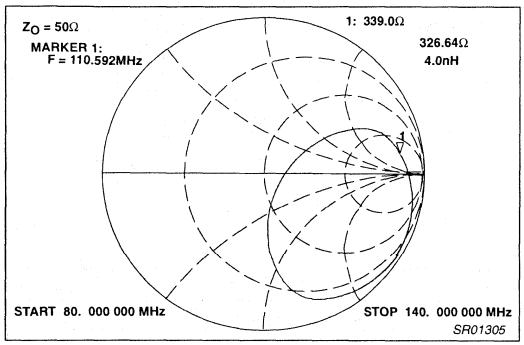


Figure 47. Smith Chart S_{11}: Showing Initial Component Results

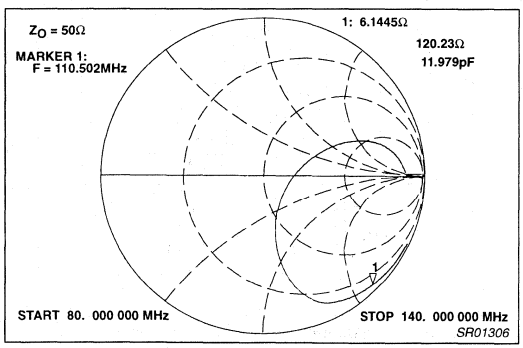


Figure 48. Smith Chart S_{11}: Showing Sensitivity to Small Changes in $C_{5,7}$

These observations suggest a general method of attack for obtaining the output impedance at 50Ω. When the series capacitance element C_6 is increased/decreased it will cause the somewhat circular curve on the Smith chart to increase/decrease in diameter. An effective method for obtaining the required match would be to adjust C_6 such that this curve passes through the center of the Smith chart and then make the necessary adjustments to $C_{5,7}$ to set the resonant frequency at the target IF. Looking at Figure 48 again, we see that the output impedance at resonance is too high. We should be able to decrease this by increasing the series capacitance element C6. In addition, from Figures 47 and 48 we know that the correct value for $C_{5,7}$ to obtain resonance at 110.592MHz is between 4.7pF and 10pF. So, we will increase C_6 to 12pF and set $C_{5,7}$ to 6pF and see what happens. Figure 49 shows the output impedance at resonance is very close to the target but the resonant frequency is still a bit too high. Figures 50 and 51 show that by adding 1pF to $C_{5,7}$ the required match is obtained. An additional matching network is not needed to evaluate the circuit because we are already at 50Ω.

In previous discussions, it was mentioned that the frequency at which the return loss is obtained does not guarantee optimum gain at this same frequency due to the phase relationships of the signals within the current-combiner circuitry. Figure 52 shows that approximately 12dB of gain is obtained but at a frequency of 115MHz, which is approximately 5MHz away from the targeted IF. To correct this we simply adjusted $C_{5,7}$ to 8.5pF to obtain a similar condition 5MHz lower than the previous result as shown in Figures 53, 54 and 55.

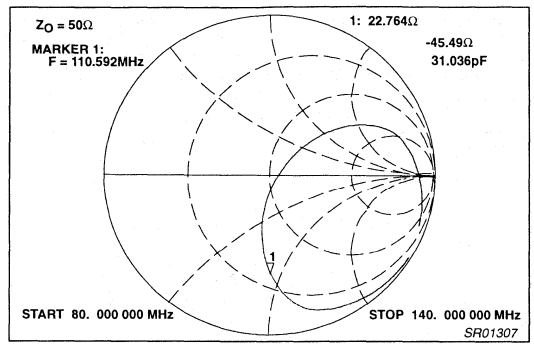


Figure 49. Smith Chart S_{11}: Showing Results of Adjustment to Capacitor $C_{5,6,7}$

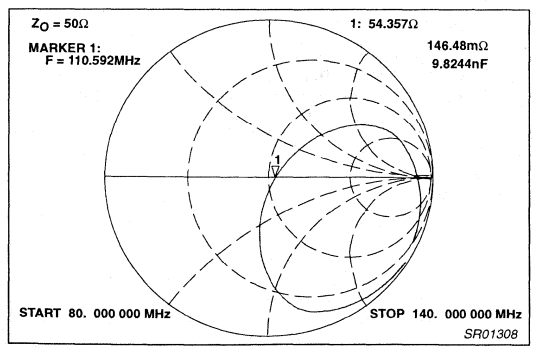


Figure 50. Smith Chart S_{11}: Showing Final 110.592MHz, 50Ω Results

Table 4. Mixer Output Component Values

	50Ω Match			1kΩ Match		
	MHz			MHz		
	45	83	110	45	83	110
L_1	6.8μH			6.8μH		
L_3	270nH			390nH	270nH	
$C_{3,7}$	80pF	18pF	8.5pF	62pF	22pF	10pF
C_6	22pF	15pF	12pF	1000pF		
R_2	— — — — —			—	5k	—

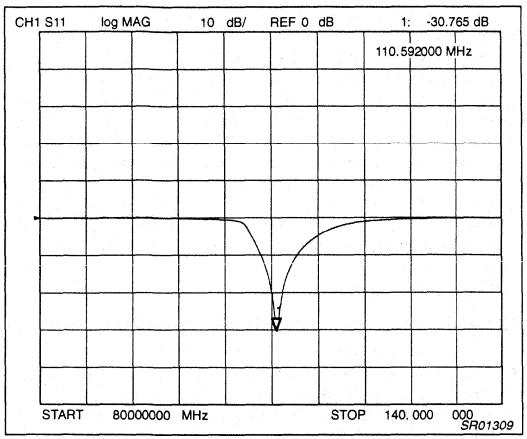


Figure 51. Final 110.592MHz, 50Ω Results

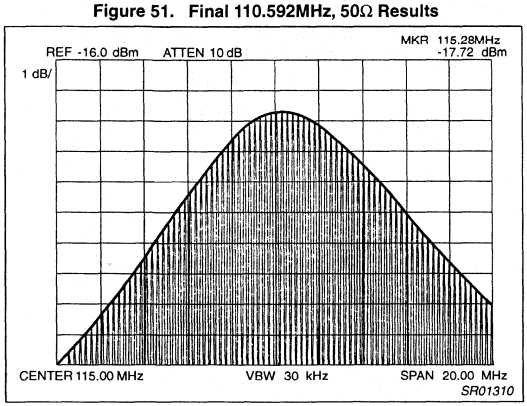


Figure 52. Mixer Output Freq. Resp. Peak is 5MHz Too High

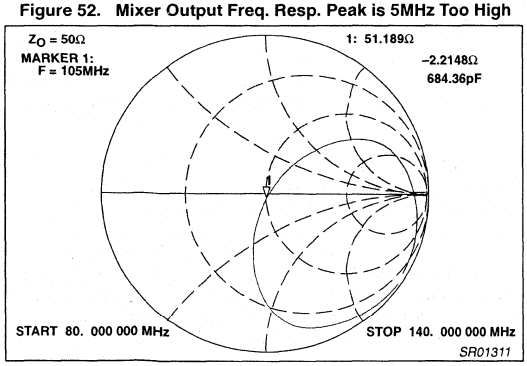


Figure 53. Smith Chart S_{11}: Showing Match With $C_{5,7}$ = 8.5pF

SA601 $IP3_{IN}$ Considerations

It should be noted that it is often necessary to give up some mixer gain of the device in order to obtain acceptable IP3in performance. The previous examples and procedures demonstrated how to optimize the gain. To meet the IP3in specifications of your particular application, it may be necessary to make some changes. The demoboard schematic for the SA601 in Figure 67 shows these changes. One difference between the previous discussions and this schematic is that C_5 and C_7 are not of equal value. It has been found that loading the differential output in an asymmetrical fashion by making C_5 less than C_7 is beneficial to $IP3_{IN}$ performance. So, your frequency adjustments would then be made by keeping C_7 constant and varying C_5. Also, inductor L_2 can no longer be chosen arbitrarily large. It must be chosen such that a high impedance parallel resonance condition occurs with C_7 at the frequency of interest. Resistance R_2 can then be used to obtain the required high impedance match. C_6 is used to acquire the 50Ω match exactly as before. The IP3in and gain performance for this configuration at 83MHz is shown in Figures 56 and 57. Notice the gain is approximately 8dB which is approximately 2dB less than that obtained in the previous examples. This was the trade-off for obtaining the better $IP3_{IN}$ performance (see Figure 57).

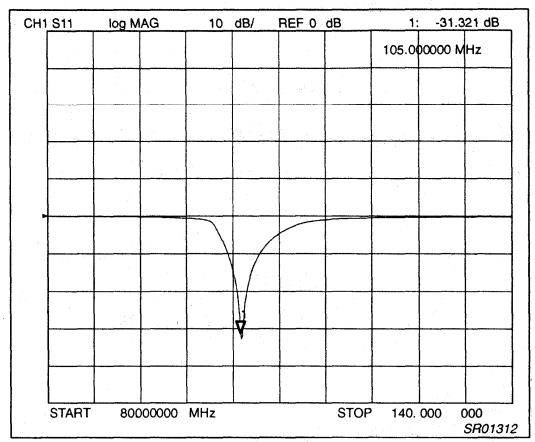


Figure 54. Mixer Output Set 5MHz Below Target to Get Final Result at 110.592MHz

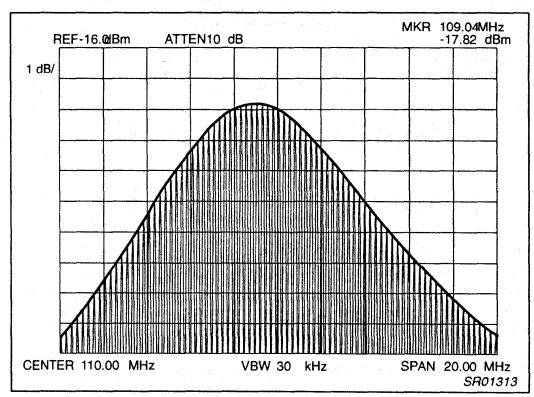


Figure 55. Mixer Output Set 5MHz Frequency Response Peak Very Near 110.592MHz Target

Summary of Mixer Open-Collector Output Concepts

The open-collector of a transistor offers a designer using the SA601 and SA620 the flexibility to provide impedance matching with minimal external components. Additionally, when an inductor is strategically located in the circuit, more AC output swing will occur due to the Early-Voltage effect of the device without adding any additional current.

When using the SA601 differential open-collector output, a designer can use the current-combiner circuit to combine the currents such that additional output signal swing is achieved. This preserves the RF signal and thus eliminates the need for interstage amplifiers. The current-combiner differential mixer output is not available on the SA620.

A flexible matching circuit can be used to deliver an equal amount of power to unequal resistive loads. The flexible matching circuit is ideal for trouble-shooting.

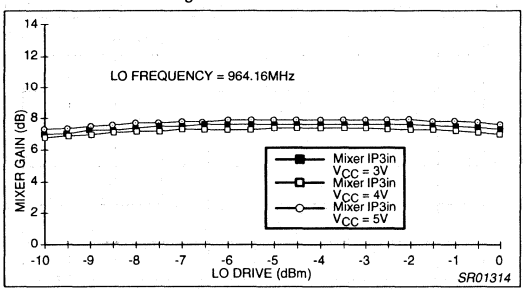


Figure 56. Mixer Gain vs LO Drive SA601

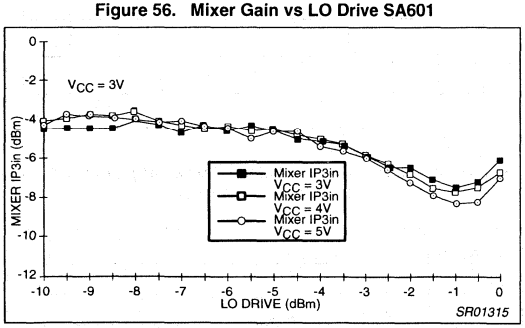


Figure 57. Mixer $IP3_{IN}$ vs LO Drive SA601

X. SA601 MIXER CHARACTERIZATION

Figure 56 shows a mixer gain vs. LO drive curve for a SA601 utilizing the current-combiner circuit in an application board environment. It shows that over an LO drive-level range of -10dBm to 0dBm the mixer gain deviates from an average value of 7.5dB by less than 0.5dB. It also shows that the gain will change by less than 0.5dB when V_{CC} is varied from 3V to 5V.

The noise figure of the SA601 generally increases with decreasing LO drive. Over the LO drive-level range of -10dBm to 0dBm the noise figure varied from approximately -12dB to approximately -8dB, respectively. The noise figure at - 5dBm LO drive is approximately 10dB.

Figure 57 shows the mixer's 60kHz $IP3_{IN}$ vs. LO drive curve for the SA601 in an application board environment. It should be noted that the $IP3_{IN}$ was measured with a -35dBm RF input at 881MHz and an offset of just 60kHz. 881MHz is the center of the 869 to 894 IS-54 Rx band, -35dBm was selected to ensure P_{IN} vs P_{OUT} linearity, and 60kHz was chosen as a suitable representation of current application alternate-channel constraints. The figure shows $IP3_{IN}$ to be constant at approximately -4.3dB over an LO drive-level range from -10dBm to approximately -5dBm. For LO drive-levels greater than -5dBm, $IP3_{IN}$ will decrease by approximately 1dB for every 1dB increase in LO drive. It is for this reason, that even though the mixer noise figure continues to decrease with larger LO drives, *the LO drive-level which optimizes gain, noise figure and $IP3_{IN}$ for current IS-54 applications is approximately -5dBm.*

SA601 System 12dB SINAD Performance

Figure 59 shows the 12dB SINAD vs RF input frequency of a receiver system composed of the SA601 utilizing the differential mixer output and the SA606 low-voltage FM-IF as shown in Figure 58. Data was taken over an input frequency range covering the 869 - 894MHz IS-54/AMPS Rx band as well as the 902 - 928 ISM band. *The 12dB SINAD performance in both bands was approximately -121 to -122dBm without a duplexer.* The system 12dB SINAD with a duplexer present will typically increase by approximately 3dB.

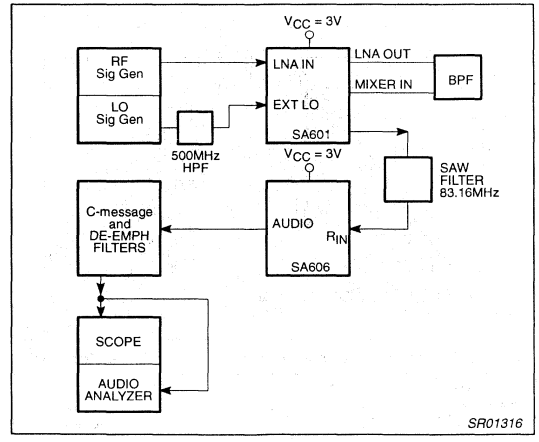


Figure 58. SA601 12dB SINAD System Test Configuration

XI. SA620 VCO

The SA620 features a low-power integrated VCO for providing an LO to the mixer. Thus, the additional cost and space associated with the use of an external VCO are eliminated. In the Philips SA620 application board environment shown in Figure 71, the VCO can be operated from 900MHz to approximately 1200MHz with the frequency range (using a 5V control voltage) increasing from 20MHz to 70MHz, respectively. Figure 60 shows the LO frequency vs. control voltage for two LO ranges centered at 960 and 995 MHz.

Figure 61 shows the VCO output power for the same LO ranges shown in Figure 60. The average VCO output power is approximately -20dBm and varies less than 0.5dB over the 5V control voltage range.

Figure 62 shows the VCO phase noise at a 60kHz offset for the same LO ranges shown in Figures 60 and 61. *The average phase noise (60kHz offset) is approximately -103dBc/Hz on*

non-silver-plated application boards and varies approximately 1dB across the 5V control voltage range. Phase noise performance may be improved another 1 – 2 dBc/Hz in with silver plating (see discussion below). It should be noted that a significant degradation of the phase noise performance was observed in the application board environment when the VCO was operated at frequencies above 1100MHz.

XII. μ-STRIP INDUCTOR OSCILLATOR RESONANT CIRCUIT [4, 5, 8]

The SA620 application board utilizes a high Q, μ-strip inductor in its oscillator resonant circuit to improve phase noise performance. Information concerning phase noise, μ-strips, and their implementation on the SA620 applications board is presented below

General Theoretical Background

Phase noise $S_\theta(fm)$ is a performance parameter of an oscillator circuit's spectral purity describing the energy it produces at frequencies fm on either side of the wanted carrier frequency f_c. To express how this works, an oscillator can be modeled as a feedback loop employing a phase modulator and noise-free amplifier to show how the resonator effects the phase characteristics of the resulting output. (A complete analysis of this model can be found in [4].)

In Figure 63, the phase spectral-density noise factor $S_{\theta IN}$ models internal phase noise produced by the oscillator's active components (e.g. BJT, FET etc.). Essentially, this factor is filtered by an external resonator that accepts energy from the noiseless amplifier which has sufficient gain G_O to sustain closed loop oscillations. Active circuitry with low internal phase noise will produce cleaner outputs for a given degree of filtering. Similarly, increasing the filtering will produce a cleaner output for a given internal spectral phase noise. Note that because of the feedback arrangement, the output spectral phase noise can never be less than that produced internally. These relations are summarized in the following equations, assuming the external resonator to be a simple parallel resonant LC tank circuit.

$$S\theta_{OUT}(fm) = |H(j\theta)|^2 \, S\theta_{IN}(fm) \qquad (10)$$

$$S\theta_{OUT}(fm) = \left[1 + \left(\frac{f_o}{2Q_L\, fm}\right)^2\right] S\theta_{IN}(fm) \; ; (fm) > 0 \qquad (11)$$

In practice, a spectrum analyzer is commonly used to obtain an indirect measure of phase noise by measuring power vs. frequency, or the power spectrum on some specified bandwidth at various carrier offset frequencies m and then normalizing each reading to the equivalent power in a bandwidth of 1Hz. This technique of measuring SSB phase noise L(m) usually takes the peak carrier power as the 0dB reference. Thus, Equation 11 can be expressed as

$$L_{OUT}(fm) = \frac{1}{2}\left[1 + \left(\frac{f_o}{2Q_L\, fm}\right)^2\right] S\theta_{IN}(fm) \; ; (fm) > 0 \qquad (12)$$

SSB Phase Noise

and

$$L(fm) \equiv \frac{\text{noise power (in 1 Hz) with instrument corrections at } fm \text{ offset from the carrier } f_c}{\text{carrier power}} = \frac{N}{C} \qquad (13)$$

Equation 12 shows two possible ways to decrease an oscillators output phase noise $L_{OUT}(fm)$. Basically, we can decrease $S_{\theta IN}(fm)$ or increase the loaded-Q, Q_L of the tank circuit. In the case of the SA620, only the latter is feasibly controllable since $S_{\theta IN}(fm)$ is a property of the internal circuitry and, as already noted, places a lower attainable bound on $L_{OUT}(fm)$ as $Q_L \Rightarrow \infty$.

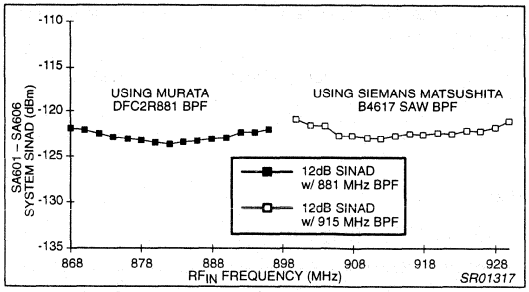


Figure 59. SA601 - SA606 System 12dB SINAD vs RF_{IN} Frequency

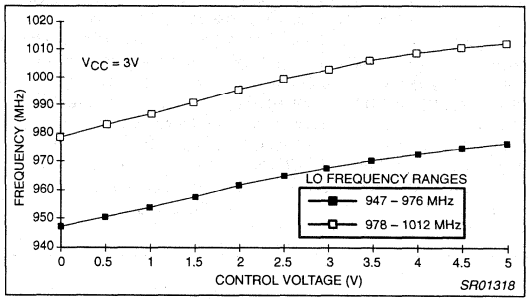


Figure 60. LO Frequency vs Control Voltage SA620 VCO

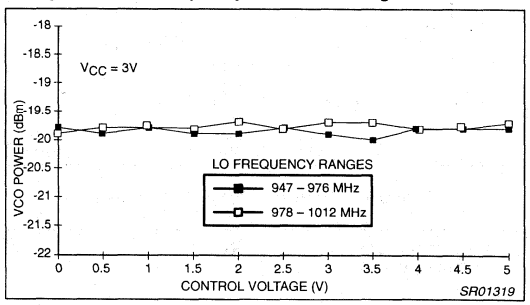


Figure 61. VCO Power vs Control Voltage SA620 VCO

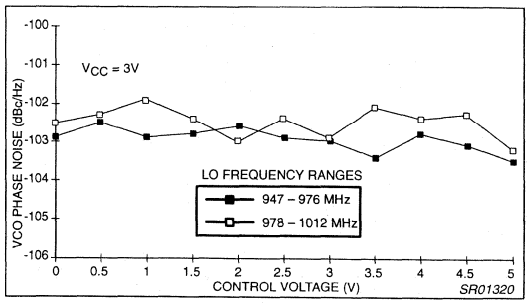


Figure 62. VCO Phase Noise vs Control Voltage SA620 VCO

Increasing Loaded-Q

Figure 64 shows the oscillator section of the SA620 with a conventional 2nd order parallel tuned tank circuit configured as the external resonator.

From the basic equations for parallel resonance, the resonator's loaded-Q is given by

$$Q_L = R_P \left[\frac{C_T}{L_T}\right]^{(1/2)} \quad (14)$$

where

$$R_P = R_T \,||\, R_C = \left[\left(\frac{1}{R_T}\right) + \left(\frac{1}{R_C}\right)\right]^{-1} \quad (15)$$

represents the net shunt tank resistance appearing across the network at resonance. R_T represents losses in the inductance L_T and capacitance C_T (almost always dominated by inductor losses), and R_C is the active circuits load impedance at resonance. Improving the quality (i.e., their Q) of the tank components, L_T and C_T will increase R_T, but since R_C is low in the case of the SA620, the resulting increase in R_P is relatively small. We can increase R_P by decoupling Z_C from the tank circuit (note that R_C is the real part of Z_C at resonance). Decoupling this impedance by using either tapped-L or tapped-C tank configurations is possible. Inspection of the circuit shows that DC biasing is necessary for Pins 9 and 10 (osc1 and osc2, respectively), so a tapped-C approach would require shunt-feeding these pins to V_{CC}. Thus, the most practical way is to employ a tapped-L network.

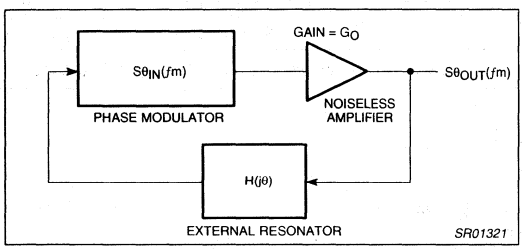


Figure 63. Oscillator Phase Noise Model

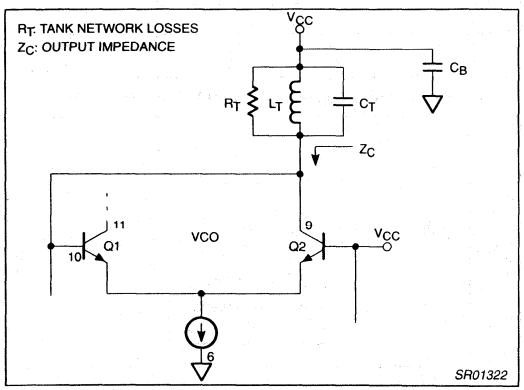


Figure 64. SA620 With External Resonator

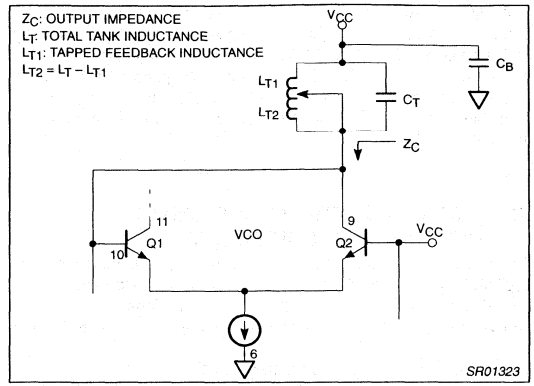


Figure 65. SA620 With Tapped-L Resonator

Figure 65 shows the basic tapped-L circuit. The effective multiplied shunt impedance at resonance across C_T is given by

$$\hat{R}_P = R_P \left[\left(\frac{L_{T2}}{L_{T1}}\right) + 1\right]^{1/2} \quad (16)$$

with a corresponding increase in loaded Q

$$\hat{Q}_L = Q_L \left[\left(\frac{L_{T2}}{L_{T1}}\right) + 1\right]^{1/2} \quad (17)$$

Feedback is caused by an RF voltage appearing across L_T, coupled through bypass capacitor C_B and its ground return to the cold end of the current source at Pin 6. The significance of this path increases with frequency. At 900MHz it becomes very critical to obtaining stable oscillations and must be kept as short as possible. Attention to layout detail cannot be overlooked here!

High-Q Short μ-Strip Inductor

Realizing a stable tapped-L network using lumped surface-mount inductors is impractical due to their low unloaded-Q and finite physical size. Another approach utilizes a high-Q short microstrip inductor. The conventional approach to microstrip resonators treats them as a length of transmission line terminated with a short which reflects back an inductive impedance which simulates a lumped inductor. The approach presented here deviates from this technique by specifically exploiting the very high unloaded-Q attainable with short microstrip inductors where we design for a large C/L ratio by making the microstrip a specific but short length. Resonance is achieved by replacing the short with whatever capacitance is needed for proper resonance. One equation for the inductance of a strip of metal having length l (mil) and width w (mil) is

$$L = [5.08E-3]\,\ell\,[\ln(\ell/w) + 1.193 + 0.224(w/\ell)] \quad [nH/mil] \quad [4] \quad (18)$$

This technique results in a much shorter strip of metal for a given inductance. One intriguing property of microstrip inductors is that they are capable of very high unloaded-Q's. An equation describing the quality factor for a "wide" microstrip line is

$$Q_C = 0.63h\,[\sigma f_{GHz}]^{1/2} \quad [5] \quad (19)$$

where h is the dielectric thickness in centimeters, σ is the conductivity in [S/m] and f is frequency in GHz. This equation predicts an unloaded-Q exceeding 700 when silver-coated copper is used. Also, wide microstrip lines are defined as those whose strip width w to height h ratio is approximately or greater than 1, i.e. w/h > 1. The parallel capacitor formed by the metal strip over the

ground plane should also be included and may be calculated by the classic formula and included in the total needed to resonate with the inductance result found from equation (18). This "strip" capacitance is given by

$$C_S = K\varepsilon_o\varepsilon_r\ [wl/h]\ [Farad] \quad (20)$$

where ε_O= 8.86E-12 [F/cm] is the permitivity of free space, r is the relative dielectric constant of the substrate. A "fringe factor" K is included to account for necessary fringing (est 2% to 15%). These equations are meant to provide insight into circuit behavior and should, therefore, be applied cautiously to specific applications.

UHF VCO Using the SA620 at 900MHz

The basic electrical circuit involving the SA620 is shown in Figure 66. Feedback occurs when sufficient RF voltage develops across the tap inductances L_{T1} and L_{T2} (due to tap-1 and tap-2 respectively); note that inductance is reckoned from the cold end of the tank at node A. Taps 1 and 2 should be as close as possible to Pins 10 and 9, respectively. Also, nodes A (cold end of tank) and B (Pin 6) must be as physically close together and exhibit as low an impedance as possible to discourage parasitic oscillations. This "inner-loop" composed of L_{T2}, inductance of taps 1 and 2 connecting to Pins 10 and 9, and stray low Q inductance between nodes A and B create a parasitic loop that will favor oscillations that no longer depend on the full tapped-L tank circuit. This low-Q loop will exhibit very poor phase noise and typically oscillate well above 1200MHz; it has been observed as high as 1600MHz.

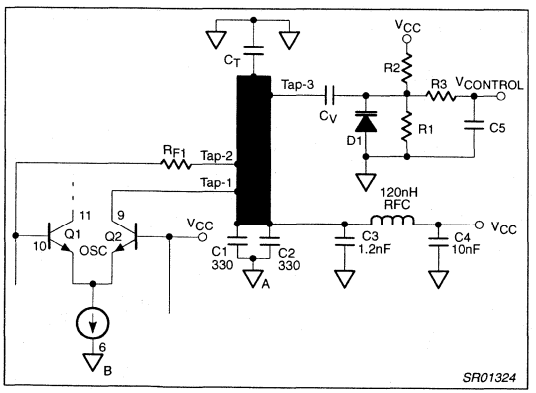


Figure 66. SA620 with Tapped-L μ-Strip Resonator

Another factor also affects this unwanted parasitic oscillation. As the loaded-Q of the tapped tank circuit decreases, the circuit becomes conditionally stable and will eventually favor the parasitic loop exclusively. This occurs because tapped-L loaded-Q affects the magnitude of the RF voltage appearing across the entire microstrip tank. Thus, feedback at taps 1 and 2 is reduced as the Q decreases. This increases the likelihood of the inner-loop parasitic controlling the oscillator, since its feedback voltage is largely independent of the μ-strip tank Q.

Equation 19 shows that microstrip inductors are capable of very high unloaded-Q's. This depends on a number of physical factors: frequency, dielectric thickness and its quality, and the skin depth conductance of the metal strip itself. For example, at 900MHz, when coated with silver, unloaded-Q is somewhere about 750; when coated with lead (or sloppy soldering!) it drops to less than 230. If the unloaded-Q is too low, the loaded-Q also drops and the circuit becomes conditionally stable, and now will either oscillate at the higher parasitic inner-loop or the wanted tapped-L lower complete tank circuit frequency. Components should be connected by narrow traces closely connected to component pads to avoid soldering on the microstrip layer.

The addition of R_{F1} introduces necessary losses to control the inner-loop parasitic oscillation. Its size should be made as small as possible consistent with stability, startup and good phase noise performance. Since it also decreases feedback, LO injection falls off as it increases. Typically, experimental values from 4Ω to 30Ω have proved sufficient. Stability as a function of V_{CC} is a good way to assess conditional stability. Provided the microstrip tank has a high loaded-Q, stability should be independent of V_{CC} down to less than 2.5V, or so. When loaded-Q decreases, so as to favor the inner-loop parasitic, conditional stability will occur. This can readily be observed by increasing V_{CC} beginning at about 1.0V and noting whether the VCO jumps back and forth unpredictably. Mixer and LO port loading also affect this condition and should be considered.

Dimensions for the microstrip resonator are based on several criteria. The strip must be "wide": its width to height must be on the order of 1 or greater. Minimum strip length seems to be about 200 mils for a 62 mil thick board. L/C ratios somewhere about 500 have yielded quite good results. Note that we usually specify the "L/C" ratio because it is always greater than 1, even though in a parallel resonant circuit it appears in the Q equation as C/L. Thus, decreasing the "L/C ratio" by making the microstrip shorter helps the loaded inductor Q, and the circuit loaded-Q_L, increase (see Equation 14). However, the effect of the lower Q of C_T, even when using a "hi-Q" SM type, decreased the expected larger increase in the net loaded circuit Q. Thus, the expected increase in Q_L may not be fully realizable. Assuming a 62 mil thick board with FR5 dielectric, a strip 50 by 300 mils gave very good experimental results where C_T was about 4.3pF with oscillations occurring from about 950 to 1000MHz for various test boards. A shorter inductor designed to increase the C/L ratio requiring 7.5pF experimentally resulted in only about 1–2dB improvement at 950MHz.

Tap-1 may be anywhere between the cold end of the tank (where C_1 and C_2 are located) and tap-2. Tap-2 yields good results at about 1/3 the strip length. Making it too close to the cold end in an effort to increase Q_L will result in loss of control over the inner-loop parasitic. To keep Q_L as large as possible, C_T should be a Hi-Q SM type. Differences greater than 5dB in SSB phase noise have been observed between a generic NPO SM and Hi-Q NPO SM capacitor.

Tap-3 can be at the end of the microstrip where C_T is connected. However, the varactor inevitably will cause a decrease in overall loaded-Q, typically by as much as 5dB. Moving it back some distance from the high end of the tank will decrease this effect and yield better results. A good starting point is about 1/4 back or 3/4 of the length from the cold end. C_1 and C_2 are paralleled lower value capacitors to yield a better low-impedance ground return to Pin 6 (node B) since relatively large RF currents flow through them. Note that as Q_L increases the peak circulating RF current will also increase, as will the RF voltage at the high end of the microstrip. At 900MHz good results have been obtained when both are about 330pF. RFC was chosen to be approximately series-resonant around 900MHz and constitutes the series feed path for DC biasing. It may be possible to neglect this component entirely, provided the PCB connection to the cold end of the tank is very close to RF ground. Finally, note that shielding of the entire microstrip may be necessary to meet part 15 emission limitations (where applicable).

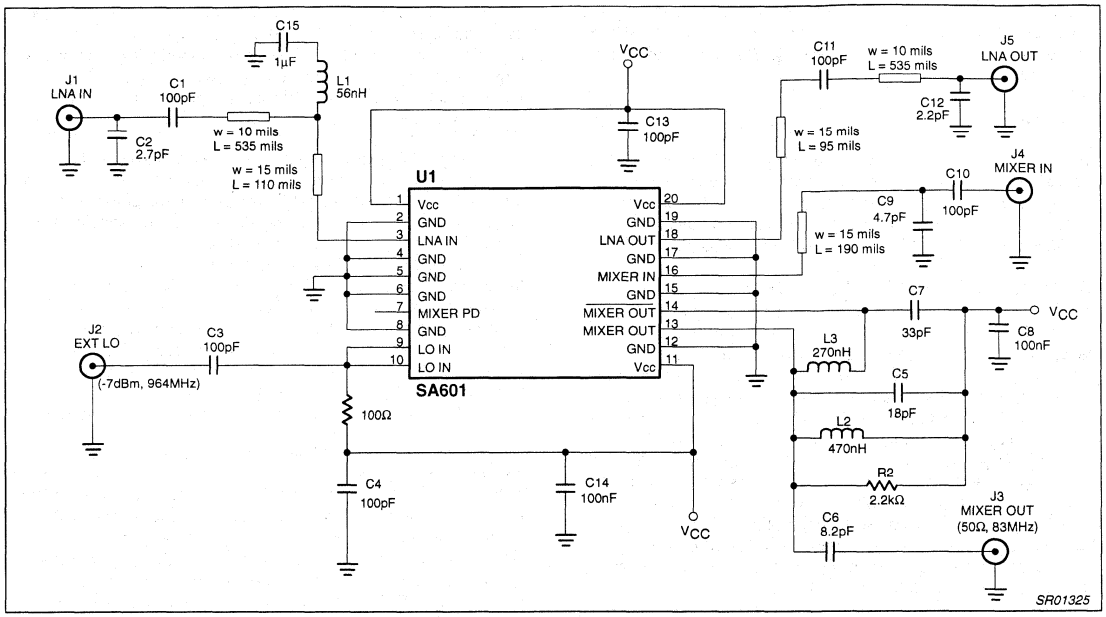
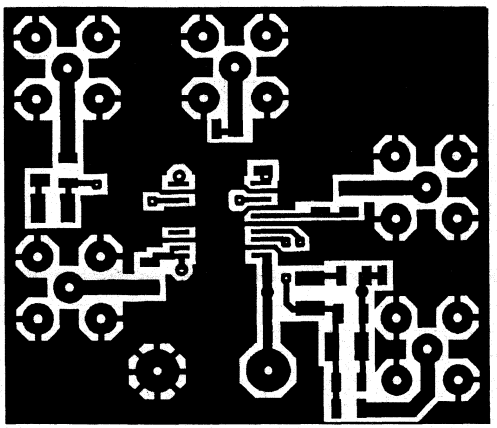
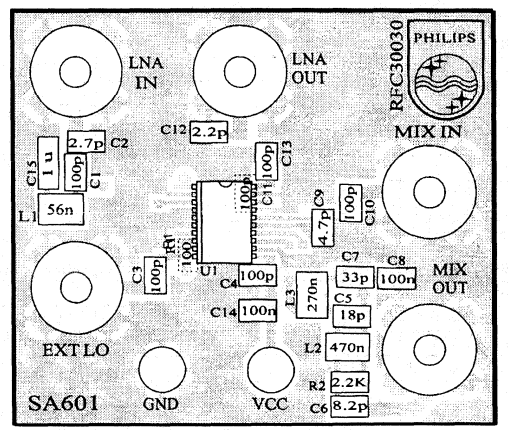


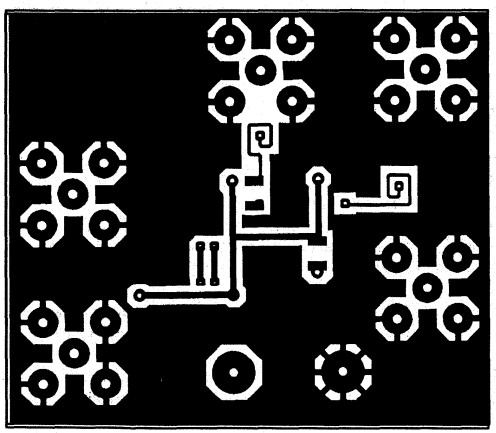
Figure 67. SA601 Application Board Schematic



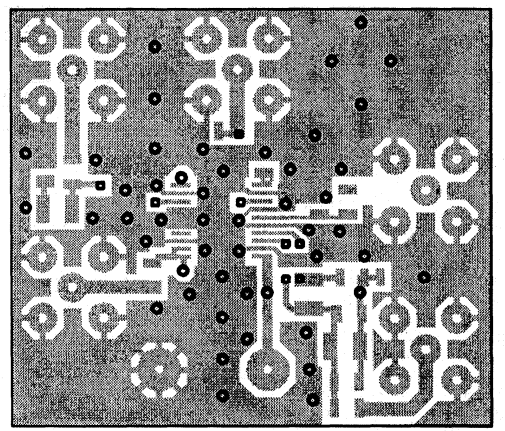
Top View



Silk Screen



Bottom View



Via Layer

SR01326

Figure 68. SA601 Demoboard Layout (Not Actual Size)

Table 5. Customer Application Component List for SA601

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	2.2pF	50V	C12	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG229C9BB0
1	2.7pF	50V	C2	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG279C9BB0
1	4.7pF	50V	C9	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG479C9BB0
1	8.2pF	50V	C6	Cer Cap 0805 NPO ± 0.5pF	Garrett	Philips	0805CG829C9BB0
1	18pF	50V	C5	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG180J9BB0
1	33pF	50V	C7	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG330J9BB0
6	100pF	50V	C1, C3, C4, C10, C11, C13	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG101J9BB0
2	0.1µF	50V	C8, C14	Cer Cap 0805 Z5U ± 20%	Garrett	Philips	0805E104M9BB0
1	1µF	25V	C15	Cer Cap 1206 Y5V ± 20%	Garrett	Rohm	MCH312F105ZP
Surface Mount Resistors							
1	100Ω	50V	R1	Chip Res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR10JW101
1	2.2kΩ	50V	R2	Chip Res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR10JW222
Surface Mount Inductors							
1	56nH		L1	1008 size chip inductor ± 10%	Coilcraft	Coilcraft	1008HS-560XKBB
1	270nH		L3	1008 size chip inductor ± 10%	Coilcraft	Coilcraft	1008HS-271XKBB
1	470nH		L2	1008 size chip inductor ± 10%	Coilcraft	Coilcraft	1008HS-471XKBB
Surface Mount Integrated Circuit							
1		3V	U1	RF low noise amplifier / mixer	Philips	Philips	SA601DK
Miscellaneous							
5				SMA gold connector	Newark	EF–Johnson	142-0701-801
2				Terminal	Newark	Cambion	160-1558-02-01
1				Printed Circuit Board	Excel	Philips	SA601 - RFC30030
29 Total Parts							

XIII. APPLICATION BOARDS

SA601 Applications Board

Figure 67 shows the schematic of the current application board for the SA601.

The functional description of each pin and its associated external circuitry is summarized below.

Pins 1, 11 and 20 are all V_{CC} supply pins. Capacitor C_{13} is for decoupling purposes.

Pins 2, 4, 5, 6, 8, 12, 15, 17 and 19 are all ground connections and should be tied to a common ground plane and as close to the chip as possible.

Pin 3 is the LNA mixer input pin. The LNA input has an associated network for the purpose of optimizing the return loss while minimizing the degradation of the noise figure. This network is composed of Capacitor C_2, L_1 and the 535 mil spiral inductor. Capacitor C_1 is a DC blocking cap.

Capacitor C_{15} and inductor L_1 also provide the LNA with voltage compensation.

Pin 7 is the mixer power-down pin. It will disable the mixer if set low. The application board simply leaves this pin open.

Pin 9 and Pin 10 are both connected to the local oscillator input. It is important to have good return loss at this pin to allow small LO drive-levels to be used. Capacitors C_4 and C_{14} are decoupling caps. C_3 is a DC blocking cap.

Pin 13 and Pin 14 are the differential mixer outputs. Inductor L_3 and capacitors C_5 and C_7 comprise the differential-to-single-ended translation circuit which combines the output currents and forces them to be in phase with each other. This circuit is extensively described in the previous discussions. R_2 sets the output impedance of the mixer output and L_2 is the DC bypass inductor which increases the gain of the open-collector output. Capacitor C_6, in conjunction with L_2, is used to match the mixer output port to 50Ω.

Pin 16 is the mixer input pin. Capacitor C_9 is used to optimize return loss and noise figure. Capacitor C_{10} is a DC blocking cap.

Pin 18 is the LNA output pin. Capacitor C_{12} in conjunction with the 535 mil spiral inductor comprise a network for optimizing return loss and obtaining best noise figure. C_{11} is a DC blocking cap.

SA601 Application Board Modification For Increasing Mixer Gain

The SA601 application board can be modified by disconnecting the 2.2kΩ resistor R2 in Figure 67 and reconnecting it in parallel with C7. Figure 69 shows a comparison of the mixer gain with and without this modification. This modification yields a 2dB improvement in mixer conversion gain for LO drive-levels from -10dBm to 0dBm. Figure 70 shows a comparison of the mixer $IP3_{IN}$ with and without this modification over the same LO drive-level range as in Figure 69. This data shows that the $IP3_{IN}$ performance of the mixer is not degraded for LO drive-levels less than or equal to -5dBm. Some degradation does occur for LO drive-levels above -5dBm. Laboratory comparison data of noise figure performance also showed that over the LO drive-level range of -10dBm to 0dBm the modification of R_2 yielded a decrease in noise figure of approximately 0.3dB. The R_2 modification does draw about 0.3mA more supply current, however.

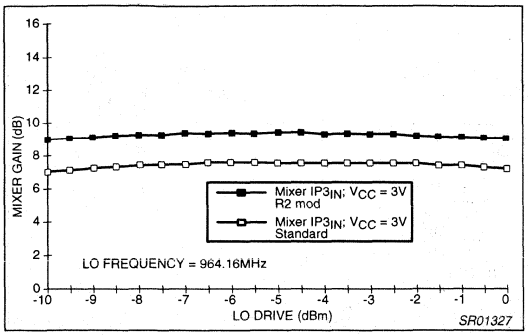


Figure 69. SA601 Mixer Gain vs LO Drive Standard/R2 Modification Comparison

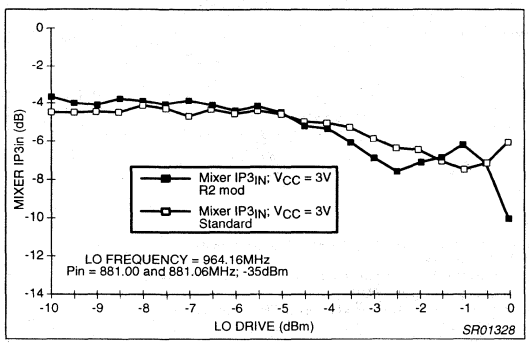


Figure 70. SA601 Mixer $IP3_{IN}$ vs LO Drive Standard/R2 Modification Comparison

SA620 Applications Board [7]

Figure 71 shows the schematic of the current application board for the SA620. The functional description of each pin and it's associated circuitry is summarized below.

Pin 1 is the LNA enable pin. This pin is used for selecting the gain in the LNA path.

The logic levels for the SA620 LNA enable are specified as:

Logic "1" level (LNA on):	+2.0V to V_{CC}
Logic "0" level (LNA off):	-0.3 to +0.8V

Referring to the application board schematic, resistor R_8 and capacitor C_{25} are used to improve LNA enable switching time. If fast switching is not a requirement, or if the LNA does not need to be disabled, these two components can be eliminated.

Pins 2, 4, 5 and 19 are ground connections. These pins provide the RF ground path for the LNA and should be tied to a common ground plane as close to the IC, and each other, as possible.

Pin 3 is the LNA input. The LNA input exhibits a return loss of 7dB at 900MHz. However, the designer can implement an external matching circuit to further improve the match. For this reason, S_{11} plots of the LNA input impedance measured right at Pin 3 are provided in the SA620 data sheet.

Referring again to the application board schematic, the 260 mil long transmission line, inductors L_1, the 4.7nH spiral inductor, and capacitor C_2 are the matching elements. Capacitor C_1 is a DC blocking capacitor. Conjugately matching the LNA input for optimum gain performance will degrade the noise figure slightly. Typically, 1.6dB noise figure can be achieved when the return loss is improved to 10dB.

Pin 6 and Pin 12 are the oscillator ground connections. These pins provide the RF ground path for the oscillator section of the SA620 and should be tied to a common ground plane as close to the IC, and each other, as possible.

Pin 7 and Pin 8 are the mixer and oscillator power down pins, respectively. These pins can be used to individually power down the mixer and the oscillator sections of the SA620.

The DC levels at Pins 7 and 8 are approximately 2.3V and 1.5V, respectively, and these levels must be established by the IC and not the power down circuitry. Placing a Schottky diode (V_f = 0.3V) between each power down pin and the LNA ENABLE pin will allow the designer to power-down the IC via a single control voltage, the LNA enable, while allowing the voltages at Pins 7 and 8 to float at the IC levels when in the power-up mode.

Pin 9 and Pin 10 drive the base of one and the collector of another of the broadband VCO differential pair input stage transistors as shown in Figure 64. Components C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}, L_2, R_1, R_2, R_3, R_4, D_1 and the 300 mil μ-strip comprise the resonant tank circuit described in detail above and shown in Figure 66.

Pin 11 is the open-collector VCO output and is provided to couple out VCO energy for frequency synthesis for example. Resistor R_5 is chosen to be small so as not to excessively load down the VCO. Hence, only about -20dBm of VCO fundamental output power will be measured at the VCO $_{OUT}$ connector on the application board. Note that the second harmonic power level will actually be slightly higher than that of the fundamental. This is not a problem because this isn't the same signal that is driving the mixer, and the mixer develops its own second harmonic as a result of the mixing process anyway. The 4.7nH spiral inductor and capacitor C_{12} on the application board are the 50Ω matching elements. Capacitor C_{13} is a decoupling capacitor.

Pin 13 is the open-collector mixer output. Referring to the application board schematic, R_6 establishes the output impedance to be 1kΩ. Inductor L_3 and capacitors C_{15} and C_{16} are 50Ω matching elements.

Pin 14 is the mixer bypass pin. This is not a signal output. It is provided for designers to optimize the IP3 performance of the mixer circuit. If you look closely at the application board schematic, you will notice that the two circuit elements at Pin 14, the 2.5 - 6.0pF capacitor and the 4.7nH spiral inductor, are very small impedances at the 83MHz IF frequency. The intent is to reflect RF leakage energy back into Pin 14 to achieve phase cancellation of this energy inside the IC, thus reducing the level of third-order intermodulation products. While looking at the third-order intermodulation products on a spectrum analyzer, the designer can tune with C_{17} to minimize the level of these products at the IF output. To obtain the best $IP3_{IN}$ performance over the entire frequency range of the VCO the following procedure is recommended:

1. Set the VCO control voltage to its mid-range value of 2.5V.
2. Adjust capacitor C_9 to obtain the desired mid-range frequency,
3. Tune C_{17} for best $IP3_{IN}$.

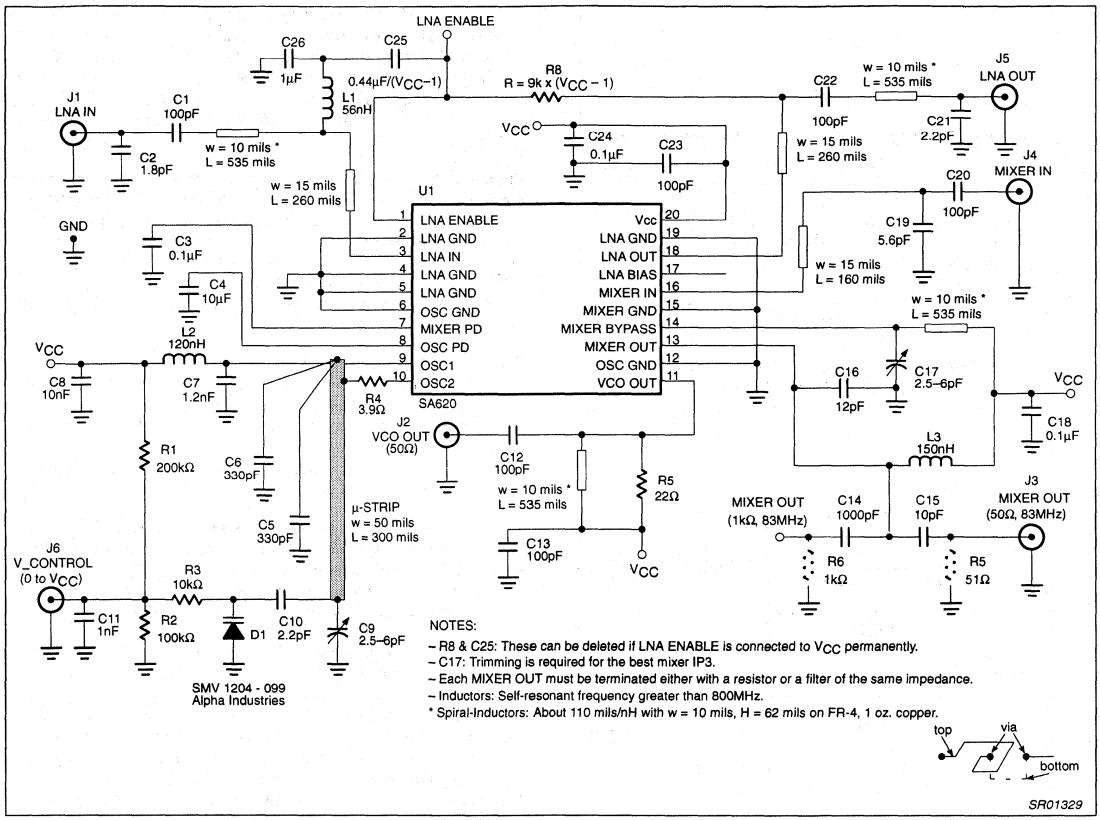


Figure 71. SA620 Application Board

Pin 15 is the mixer ground connection. This pin provides the RF ground path for the mixer section of the SA620 and should be tied to a common ground plane as close to the IC as possible.

Pin 16 is the mixer input pin. The mixer input is not matched to 50Ω, therefore, external matching elements are required to achieve optimum performance. The 160 mil long transmission line and capacitor C_{19} are the matching elements on the application board. C_{20} is a DC blocking capacitor. If no matching elements are used, the IP3 performance is typically maximized at +3dBm at the expense of gain, which will be reduced by 3dB.

Pin 17 is the LNA bias pin. This is a DC check pin for use during the manufacture of the SA620 only. Customers should float this pin in their designs.

Pin 18 is the LNA output pin. The LNA output has an intrinsic return loss of approximately 9dB at 900MHz. However, to achieve optimum performance from the SA620, the designer can implement an external matching circuit to further improve the match. For this reason, S_{22} plots of the LNA output impedance measured right at Pin 18 are provided in the SA620 data sheet. Referring again to the application board schematic, the 260 mil long transmission line, the 4.7nH spiral inductor, and capacitor C_{21} are the matching elements. Capacitor C_{22} is a DC blocking capacitor.

Pin 20 is the DC power input to the SA620 where capacitors C_{23} and C_{24} are strictly for decoupling purposes.

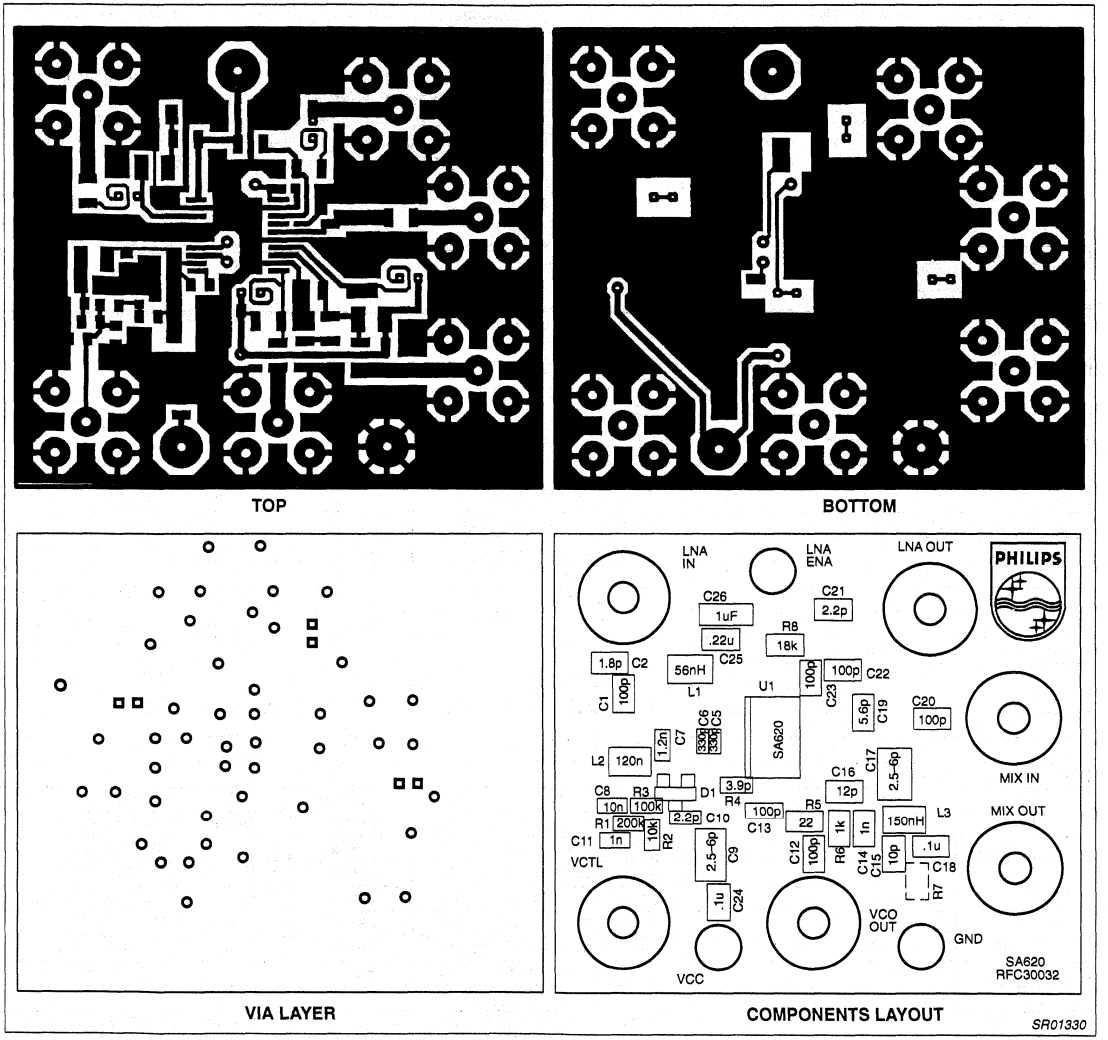


Figure 72. SA620 Demoboard Layout (Not Actual Size)

XIV. TEST AND MEASUREMENT TIPS

Noise Figure and Gain

The LNA of both the SA601 and SA620 can be tested identically. The gain and noise figure can be measured on a noise figure meter such as the HP8970. The correct measurement mode on this particular piece of equipment is obtained by selecting special function 1.0. It is important to do all noise figure measurements within a screen room to ensure the receiver of the noise figure meter is not picking up any stray signals. The LNA gain can also be measured on a spectrum analyzer. For accurate measurements, be sure to properly compensate for losses in the cables and connectors used. Also, make sure that the input power used is well below the 1dB compression point for the device. P_{IN} = -25dBm is a good value.

The SA601 and SA620 mixers require more precaution while testing. The correct measurement mode for mixer noise figure and gain measurements is obtained on the HP8970 by selecting special function 1.4. It should be stated again that all noise figure measurements should be done within a screen room. The noise source used in conjunction with the noise figure meter is generally a wideband noise source. So, for a given LO frequency there are two regions of the wideband noise power spectrum which will mix to the specified IF frequency. Thus, an image-reject bandpass filter should be placed between the noise source and the mixer input. In this way

the unwanted input noise power will be rejected yielding proper single sideband noise figure measurements. The loss through this image-reject filter should also be accounted for. Losses prior to the mixer input can be compensated for on the HP8970 by selecting special function 34.2. The noise figure of the mixers is highly dependent on the strength and quality of the LO signal. The LO signal should be passed through a high-pass filter. A 500MHz HPF is typically used. The noise figure is dependent on the LO drive-level. Generally, the noise figure will decrease as the LO drive-level is increased. The noise figure has also been observed to show some dependence on the range setting of the signal generator. The high-frequency components present at the IF output of the mixer should also be filtered out prior to entering the input port of the noise figure meter. This is typically done with a 300MHz low-pass filter. If the conversion gain of the mixer is to be measured directly on a spectrum analyzer, be sure that the input power is well below the 1dB compression point. Again, -25dBm is a good value.

Table 6. Customer Application Component List for SA620

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	2.2pF	50V	C10	Cer Cap 0603 NPO ± .25pF	Garrett	Rohm	MCH185A2R2CK
2	330pF	50V	C5, C6	Cer Cap 0603 NPO ± 5%	Garrett	Rohm	MCH185A331JK
1	1000pF	50V	C11	Cer Cap 0603 X7R ± 10%	Garrett	Rohm	MCH185C102KK
1	1200pF	50V	C7	Cer Cap 0603 X7R ± 10%	Garrett	Rohm	MCH185C122KK
1	0.01µF	25V	C8	Cer Cap 0603 X7R ± 10%	Garrett	Rohm	MCH185C103KK
1	1.8pF	50V	C2	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG189C9BB0
1	2.2pF	50V	C21	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG229C9BB0
1	5.6pF	50V	C19	Cer Cap 0805 NPO ± 0.5pF	Garrett	Philips	0805CG569C9BB0
1	10pF	50V	C15	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG100J9BB0
1	12pF	50V	C16	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG120J9BB0
6	100pF	50V	C1, C12, C13, C20, C22, C23	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG101J9BB0
1	1000pF	50V	C14	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG102J9BB0
3	0.1µF	50V	C3, C18, C24	Cer Cap 0805 Z5U ± 20%	Garrett	Philips	0805E104M9BB0
1	0.22µF	50V	C25	Cer Cap 0805 Y5V ± 20%	Garrett	Rohm	MCH212F224ZK
1	10µF	10V	C4	Tant Chip Cap B 3528 ± 10%	Garrett	Philips	49MC106C010KOAS
1	1µF		C26	Cer Cap 1206 Y5V ± 20%	Garrett	Rohm	MCH312F105ZP
Surface Mount Variable Capacitors							
2	2–6pF		C9, C17	Trimmer capacitor	Murata	Murata	TZV02Z060A110
Surface Mount Resistors							
1	3.9Ω		R4	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW3.9
1	10kΩ		R3	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW103
1	100kΩ		R2	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW104
1	200kΩ		R1	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW204
1	22Ω		R5	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW220
1	51Ω		R7	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW510
1	1kΩ		R6	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW102
1	18kΩ		R8	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW183
Surface Mount Inductors							
1	56nH		L1	Chip inductor 1008CS ± 10%	Coilcraft	Coilcraft	1008CS-560XKBB
1	120nH		L2	Chip inductor 1008CS ± 10%	Coilcraft	Coilcraft	1008CS-121XKBB
1	150nH		L3	Chip inductor 1008CS ± 10%	Coilcraft	Coilcraft	1008CS-151XKBB
Surface Mount Integrated Circuit							
1		3V	U1	Low voltage LNA & Mixer	Philips	Philips	SA620DK
Miscellaneous							
1			D1	Varactor	Wireless Components	Alpha Industries	SMV 1204-099
6				SMA gold connector	Newark	EF-Johnson	142-0701-801
3				Terminal	Newark	Cambion	160-1558-02-01
1				Printed Circuit Board	Excel	Philips	SA620 - RFC30032
49 Total Parts							

1dB Compression Point

This is determined by taking P_{OUT} vs. P_{IN} data at very low input power where the relationship between these quantities is linear. An input power range between -35dBm and -30dBm is sufficient for both the LNA and mixer. The input power is then increased to the

point where the difference between an extrapolation of the low input vs output power line and the output power is 1dB. The input power at which this occurs is the 1dB compression point. A shorter and more practical method of obtaining this parameter is to adjust the input power at a low level such that the output power is some integer number. Then increase the input power in 1dB increments. The output should also increase in 1dB increments. When the output power becomes exactly 1dB less than the expected value, the input power at which this occurs is the 1dB compression point.

Input Third-Order Intercept Point

$IP3_{IN}$ is typically measured on a spectrum analyzer by combining two input signals of equal power that are detuned by approximately 60kHz. This is then connected to the input of the device. Be sure to measure the output power of the two peaks after the power combiner because the two ports of the power combiner rarely attenuate equally. $IP3_{IN}$ is read off the spectrum analyzer by measuring the difference between the two carrier peaks and the intermodulation peaks, then adding half this difference to the input power.

It is extremely important to take this data at very low input power because this calculation assumes linearity. Input power of -35dBm is sufficient.

Phase Noise

The most economical way to measure phase noise is using the spectrum analyzer. As previously stated, this is done very simply by measuring the difference between the carrier frequency peak power and the power at some specified offset from the carrier. Unfortunately, the spectrum analyzer does not have the capability of measuring this with a 1Hz resolution bandwidth. Thus, a calculation must be made as follows:

$$\text{Phase Noise (dBc/Hz)} = -(|\Delta| + 10\log(\text{RBW}))$$

where Δ is the difference between the peak power at the carrier frequency and the power at the specified offset frequency, and RBW is the resolution bandwidth of the spectrum analyzer while taking the measurement.

XV. COMMON QUESTIONS AND ANSWERS

Q. I'm not getting the Mixer Noise Figure that is stated in the databook. What could be wrong?
A. There are quite a few things that can affect your noise figure. The most important thing to do initially is to check your measurement setup by following the suggestions in the test and measurement section of this application note. Aside from that, maintaining a good match at the LO input is very important and using the same LO drive-level specified in the databook is also necessary.

Q. Does the SA620 VCO meet AMPS stringent phase noise requirements?
A. The SA620 VCO phase noise is typically about -102dBc/Hz @ 60kHz. This does not meet AMPS specifications of -110dBc/Hz @ 60kHz.

Q. Can the SA620 be used with an external VCO to get better phase noise performance?
A. Although possible, this is not recommended due to the higher output power of the external VCO causing LO leakage problems at the mixer output.

Q. Why was the current-combiner implemented with a C - L - C arrangement instead of its dual circuit approach?
A. The C - L - C arrangement has the advantage of being low-pass in nature. Thus, it supplies additional rejection of the higher frequency RF_{IN} and LO signals at the mixer output.

Q. Why am I not getting the $IP3_{IN}$ values that are stated in the databook?
A. In addition to checking your test setup, you might want to check what the offset is between your two RF input signals. Some of the databook values are taken with an offset of 1MHz. Chances are that your offset is much smaller. For instance, AMPS alternate channel spec is only 60kHz. $IP3_{IN}$ will decrease when this offset is decreased.

Q. What are the necessary components needed to ensure unconditional stability of the LNAs.
A. Capacitor C_{15} and inductor L_1 on the SA601 schematic of Figure 67 are the necessary components needed to ensure stability. Without these components, the amplifier will generate spurs approximately 1.5MHz off the carrier at V_{CC} = 3V. The similar components on the SA620 schematic in Figure 71 are capacitor C_{26} and inductor L_1.

XVI. REFERENCES

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Evaluation of the SA601/SA606 demoboard AN1000

Author: Randall Yogi

INTRODUCTION

Philips Semiconductors is dedicated to playing a major role in the wireless communication market. Key to this goal is Philips' commitment for design assistance at all levels. This is the purpose of the SA601/SA606 combo-board. The SA601 is a combined RF amplifier and mixer designed for high-performance low-power communication systems from 800-1200MHz. The SA606 is a low-voltage high performance monolithic FM IF system that, when combined with the SA601, results in a high performance double down-conversion FM receiver. To better support this type of application, Philips has combined the SA601 and SA606 ICs onto a single board which highlights how well the SA601 and the SA606 work together. This application note explains how to overcome many of the technical problems that might arise, and shows how to achieve the best possible performance from the SA601 and SA606. Test results are also included.

This application note is divided into four main sections:

I. Overview of the SA601/SA606 combination board
II. Layout
  A. Schematic, Components Specifics and Parts List
  B. Impedance Matching
III. Performance
  A. Test Setup and Procedures
  B. Test Data and Results
IV. Conclusion
  A. Q/A section

I. OVERVIEW

Both the SA601 and the SA606 are designed for portable, low voltage, low power communication applications. For a better understanding of what is involved in combining these boards, or for more information regarding the individual boards, please review application notes AN1777 (for the SA601) and AN1993-AN1996 (for the Second-IF ICs) which can be found in the Philips RF/Wireless Communications Data Handbook, IC17.

The SA601/SA606 demoboard is designed to meet AMPS specifications. Section 2 of the EIA Interim Standard, "Recommended Minimum Standard for 800MHz Cellular Subscriber Units" (EIA/IS-19-B), was consulted as a guide. Specific sections used were:

2.3.1 RF Sensitivity
2.3.2 Adjacent and Alternate Channel Desensitization
2.3.3 Intermodulation Spurious-Response Interference
2.3.4 Protection Against Spurious Response

Measured results demonstrate that the SA601/SA606 demoboard successfully meets and surpasses the specifications listed above.

Although the SA601/SA606 demoboard is designed to meet AMPS cellular specifications, it can be modified for other analog cellular specifications such as TACS, ETACS, and NAMPS. The demoboard could also be configured for ISM band (902MHz – 928MHz) applications.

II. LAYOUT

The layout of any high frequency board is critical and always challenging. As stated previously, understanding each board separately is the key to combining them. Before a single-board layout was attempted, the SA601 and the SA606 individual demoboards were cascaded together, along with an RF SAW filter and a 1st IF SAW filter. The performance with this configuration was satisfactory, thus permitting the next step of combining everything on one board (Figure 2). As with the original SA601 and SA606 individual demoboards, the majority of the components are on one side of the board.

The SA601/SA606 demoboard layout can be configured to provide two different types of matching to the IF SAW filter (Figure 1). It can be configured as a 50 Ω impedance match, or a high impedance match to the 83.161MHz SAW filter. The 50 Ω impedance matching network allows a designer to evaluate or troubleshoot each individual block. For example, a designer can find conversion gain measurements of the SA601 or measure SINAD for only the SA606 block.

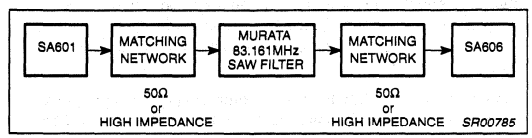

Figure 1. Block Diagram: Matching 1st IF SAW Filter

The 50 Ω impedance match can also be used as a reference for the high impedance match. Because 50 Ω impedance matching requires more components, a high impedance match is preferred. Matching for high impedance can be difficult, but since each block is optimized through a 50 Ω impedance match, the designer has a target/reference. For example, if 12dB SINAD = -120dBm for a 50 Ω impedance matched system, ideally a high impedance match should yield the same results, if not better.

The majority of the single-board layout was adapted from the individual application demoboards, except for the two SAW filters (the image rejection filter centered at 881MHz and the 83.161MHz SAW filter). The layout for the two filters required additional design work. The 881MHz image-rejection SAW filter was placed between the LNA-Out and the Mixer-In of the SA601. Placement of the 881MHz image reject SAW filter, whether it was on the top or bottom of the board, did not have a dramatic impact on performance. This was because isolation between the LNA-Out and the Mixer-In trace had already been considered in the SA601 demoboard. However, because of its high Q, narrowband, and high impedance, the 83.161MHz SAW filter was much more difficult to position. Its placement was critical in passing AMPS specification 2.3.4 Protection Against Spurious-Response Interference. The specification was met with margin to spare by moving the Mixer-Out (Pins 13 and 14) of the SA601 as far away as possible from RF-In (Pin 1) of the SA606.

Schematic, Components Specifics, and Parts List

The schematic shown in Figure 3 is for both 50 Ω impedance matching and high impedance matching to the 83.161MHz SAW filter. The schematic shows the configuration for 50 Ω impedance matching. By making the modifications listed in the box on the bottom right of the schematic (Figure 3), the board can be configured for a high impedance match.

Table 1 lists the basic function of each external component for the schematic shown in Figure 3. This may help answer any questions that arise about the specifics of the board.

Evaluation of the SA601/SA606 demoboard AN1000

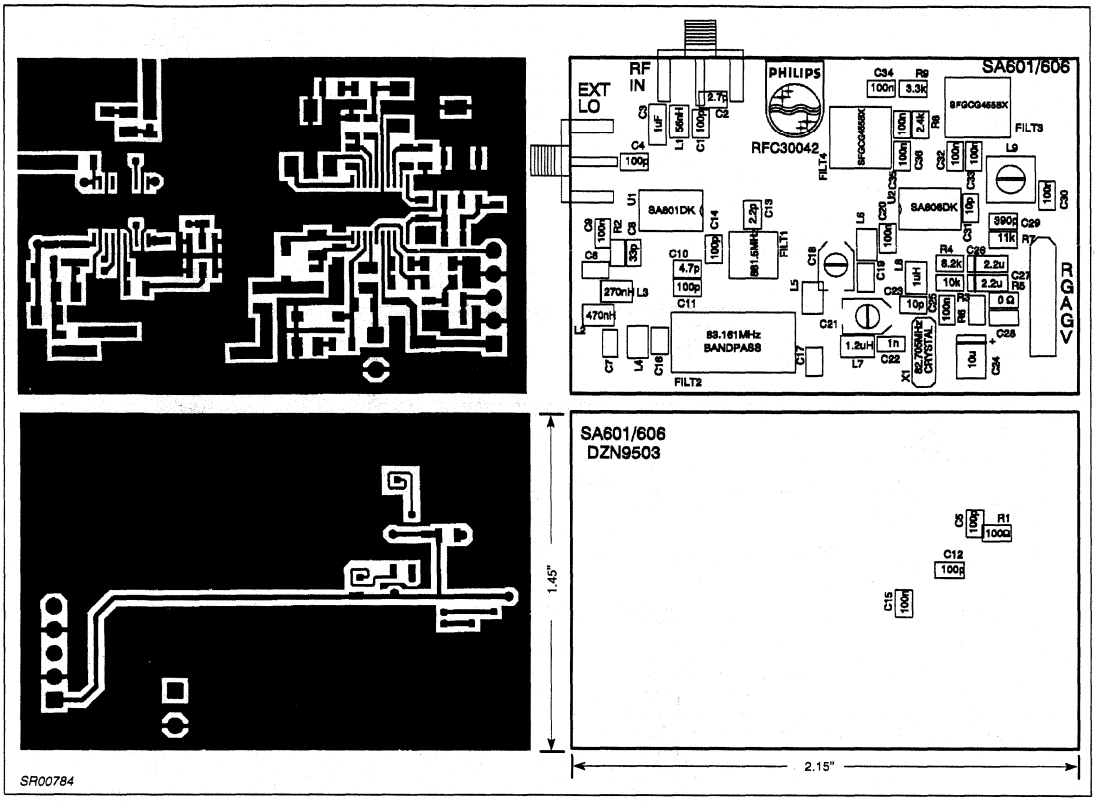

Figure 2. Layout of the SA601/SA606 Demoboard (Not Actual Size)

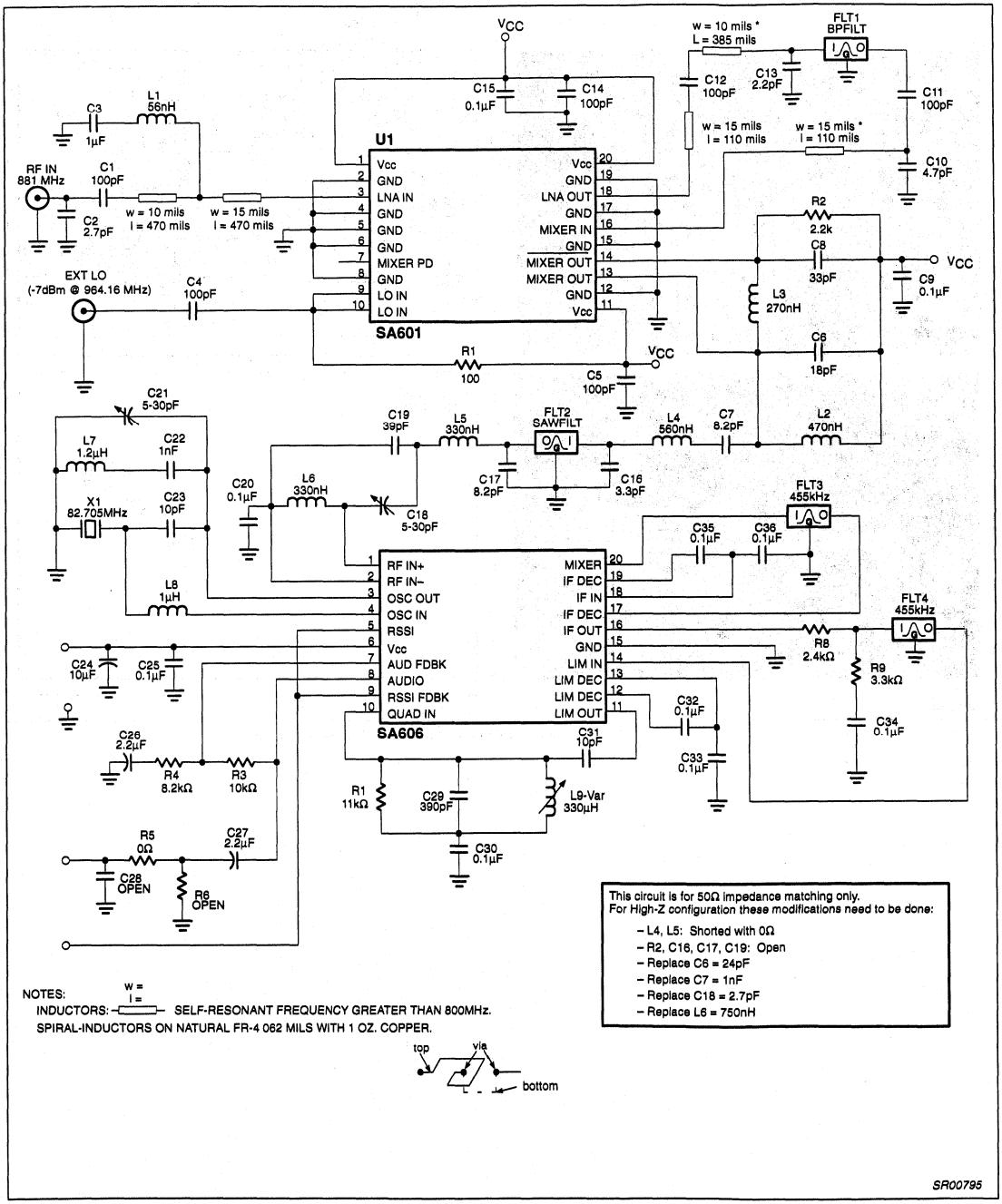

Figure 3. Schematic of the SA601/SA606 Demoboard

Table 1. Components List: Description of Functionality

Part #	Description
C1	LNA Mixer input DC blocking cap
C2	Part of the matching network that optimizes the return loss while minimizing the degradation of the noise figure
C3	Voltage compensation cap for the LNA
C4	LO DC blocking cap
C5, C9, C14, C15, C24, C25	Supply bypassing
C6, C8, L3	Part of the differential to single-ended translation circuit of the mixer out
C7, L2	Part of the matching network of the mixer output
C10, C13	Part of the matching network that optimizes the return loss while minimizing the degradation of the noise figure
C11	Mixer Input DC blocking cap
C12	LNA Output DC blocking cap
C16, C17, L4, L5	Part of the matching network of the 83.161MHz SAW filter
C18, C19, L6	Part of the tapped-C network that matches the RF input of the SA606
C20	AC grounds Pin 2, the RF input of the SA606
C21, C22, C23, L7, L8	Colpitts oscillator network
C26, C34	AC de-coupling cap
C27	DC blocking cap
C28, R5, R6	Part of the filter network that filters 3kHz-15kHz on the SA7025 (Low-voltage 1GHz fractional-N synthesizer). This network is only used on the 7025 IC production tester.
C29, L9	Quad tank component that resonates at 455kHz
C30	AC grounds the quad tank
C31	Provides the 90° phase shift to the phase detector
C32, C33	IF limiter decoupling cap
C35, C36	IF amp decoupling cap
R1	DC pull-up resistor that provides isolation (reduces IF to LO and RF to LO leakage)
R2	Sets output impedance of the Mixer Output
R3	Part of the Audio op-amp that sets a gain of 2dB thus stabilizing distortion
R4	Part of the Audio op-amp that sets a gain of 2dB thus stabilizing distortion
R7	Lowers the Q of the quad tank and thus lowers the S-Curve slope
R8, R9	Part of a network to control linearity of the RSSI
L1	Voltage compensation to LNA
FILT1	Murata SAFC881.5MA70N-TC 881.5MHz bandpass SAW filter: This is a 869MHz to 894MHz bandpass filter. It is used to reject the image frequency (LO + 83.16MHz in our case) and to attenuate the transmit signal (RF-45MHz) leaking through the duplexer so that the SA601 mixer doesn't reach its 1dB compression point from a strong signal leaking through. Some electrical characteristics from Murata are provided (Table 2).
FILT2	Murata SAFC83.161MA51X-TC 83.161MHz SAW filter: 1st-IF filter for attenuating adjacent and alternate channel spurs. The filter plays a larger role in achieving the high performance of the receiver in areas such as dynamic range, spurious performance, and data communication accuracy. The 83.16MHz SAW filter provides a 30kHz bandpass characteristic utilizing electrodes deposited on a piezoelectric substrate. These electrodes form an inter-digitated pattern on the substrate and serve as transducers to launch an acoustic wave. When an RF voltage is applied to one set of transducers, an electric field is generated and causes the acoustic waves to propagate along the surface to an opposite transducer where an output voltage is produced. (See Reference 8, Alan Victor). The Electrical Characteristics for the Murata SAW filter are shown in Table 3.
FILT3, 4	Murata SFGCG455BX-TC 455kHz bandpass filter (30kHz bandwidth).
X1	An 82.705MHz crystal from either HY-Q or Reeves Hoffman is a 3rd overtone crystal used to generate the LO for the SA606

Table 2. Electrical Characteristics of the Murata SAFC881.5MA70N-TC

Tested at 20 ±2°C. Standard condition: Temp = 20 ±2°C. Humidity = 65 ±5%; Applicable condition: Temp = 5 ~ 35°C. Humidity = 45 ~ 85%.

	Item	Requirements	Typical at 20°C (Reference Value in Standard Condition)
6 – 1	Nominal Center Frequency (f_O)	881.5 MHz	–
6 – 2	Insertion Loss I) within 869 ~ 894 MHz (Pass Bandwidth) II) within DC ~ 780 MHz III) within 824 ~ 849 MHz (Duplex Freq. Range) IV) within 970 ~ 2000 MHz	 4.5 dB max. 40 dB max. 20 dB min. 35 dB min.	 3.5 dB 48 dB 30 dB 40 dB
6 – 3	Ripple Deviation (within 869 to 894 MHz)	2.0 dB max.	1.0 dB
6 – 4	V.S.W.R. (within 869 to 894 MHz)	2.5:1 max.	1.7:1
6 – 5	Input / Output Impedance (nominal)	50Ω // 0pF	–

Table 3. Electrical Characteristics of the Murata SAFC83.161MA51X-TC

	Item	Requirements
1.1	Nominal Center Frequency (f_O)	83.161 MHz
1.2	3 dB Bandwidth (from 83.161 MHz)	±15 kHz min.
1.3	Stop Band Attenuation (from Peak Level) 1.3.1 f_O – 1000 kHz to f_O – 930 kHz 1.3.2 f_O – 930 kHz to f_O – 890 kHz 1.3.3 f_O – 890 kHz to f_O – 700 kHz 1.3.4 f_O – 700 kHz to f_O – 400 kHz 1.3.5 f_O – 400 kHz to f_O – 120 kHz 1.3.6 f_O – 120 kHz to f_O – 60 kHz 1.3.7 f_O + 60 kHz to f_O + 120 kHz 1.3.8 f_O + 120 kHz to f_O + 150 kHz 1.3.9 f_O + 150 kHz to f_O + 400 kHz 1.3.10 f_O + 400 kHz to f_O + 1000 kHz	 40 dB min. 70 dB min. 40 dB min. 30 dB min. 40 dB min. 20 dB min. 20 dB min. 40 dB min. 30 dB min. 40 dB min.
1.4	Insertion Loss (at minimum loss point)	5.0 dB max.
1.5	Ripple (within f_O = 15 kHz)	1.5 dB max.
1.6	Group Delay Deviation (within f_O ± 11 kHz)	10 µs max.
1.7	Intermodulation Input Signal : f_O + 60 kHz, f_O + 120 kHz Input Level : –20 dBm	–90 dBm max.

A complete SA601/SA606 demoboard parts list is provided in Table 14 at the end of this document. The parts list includes vendor names and part numbers as a convenience to designers.

Impedance Matching

Matching of the 83.16MHz SAW filter is an involved task. This is because the HP8753C Network Analyzer can only be calibrated for 50 Ω impedance and the 83.16MHz SAW filter has a specified impedance of 850 // -2pF. Refer to Philips application note AN1777 for an explanation of how to setup the calibration for high-impedance. Although calibration at higher impedance is not as accurate as at 50Ω impedance, the results were close enough to get a good impedance match.

Improved impedance matching yields better sensitivity performance because matching of the 83.161MHz SAW filter suppresses unwanted group delay distortion. The response of the 83.161MHz SAW filter is shown in Figure 4. When the filter response is flat, the SAW filter is matched; when it is not, group delay distortion, represented by the hump, is apparent (Figure 4).

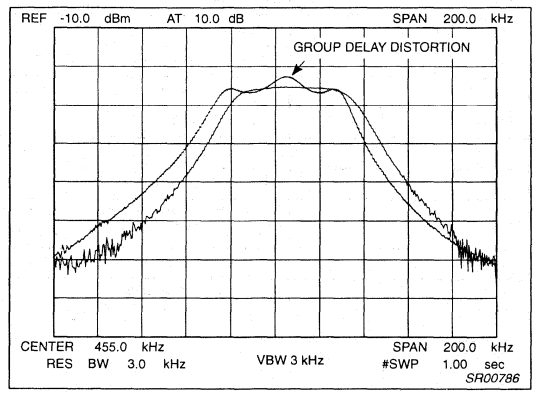

Figure 4. Group Delay Distortion

The steps to match the 83.161MHz SAW filter to a high impedance are as follows:

1. Separate the board into three sections by making two cuts in the trace. Cut 1 is between the Mixer out of the SA601 and the input of the SAW filter. Cut 2 is between the SAW filter output and the RF input of the SA606. (see Figure 5)

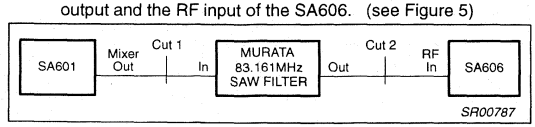

Figure 5. Three Sections of Demoboard

2. Start with SAW filter input of Figure 6 and terminate that side with an 850 Ω resistor.

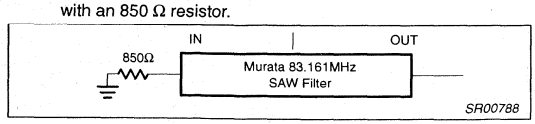

Figure 6. Termination of SAW Filter

3. Measure the impedance of the output of the SAW filter by placing an SMA connector on the trace and marking the corresponding impedance on the Smith Chart.

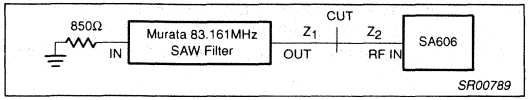

Figure 7. Termination Matching of SAW Filter

4. After identifying the impedance of the SAW filter output indicated by Z_1 in Figure 7, the RF input impedance, Z_2, must be adjusted to provide a conjugate match to Z_1. Z_2 is found on the Smith Chart by reflecting Z_1 about the purely resistive axis represented by the horizontal line running through the center of the Smith Chart.

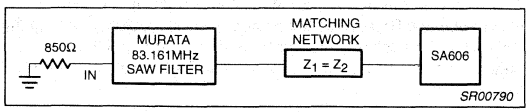

Figure 8. Impedance Matching from SAW Filter to SA606

5. After a conjugate match between Z_1 and Z_2 has been achieved, connect the output of the SAW filter to the matching network. (Figure 8)

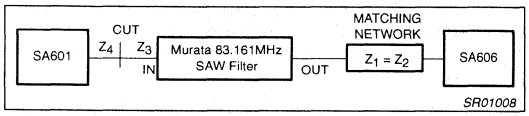

Figure 9. Impedance Matching from SA601 to SAW Filter

6. Remove the 850Ω resistor and measure the impedance at the SAW filter input, Z_3.

7. Obtain a conjugate match to Z_3 at the SA601 mixer output, Z_4, and then connect together (Figure 9).

To double check the matching, remove the 2nd-IF filter from the mixer-out of the SA606 and check the frequency response for any group delay distortion. Figure 4 shows a matched SAW-filter response (flat curve) and a poorly matched response that has group delay distortion.

To make a quick visual check of the frequency response of the board up to the SA606 Mixer output, use the FM modulation of the HP signal generator and spectrum analyzer, as follows:

1. Leave the frequencies (LO and RF) at their respective values. (example: RF = 881MHz and LO = 964.16MHz)
2. Set the FM deviation to 200kHz and the FM modulation to 200Hz on the RF's signal generator.
3. Remove the 2nd-IF filter connected to Pin 20 of the SA606.
4. Set the Spectrum Analyzer sweep time to 1 second, set the center frequency to the 2nd IF frequency (455kHz), and probe Pin 20 with a FET probe. The results should look like the flat response in Figure 4.

III. PERFORMANCE EVALUATION

Procedures

The AMPS specification was used as a guide to test the SA601/SA606 demo board. Sections 2.3.1 through 2.3.4 of the IS-19-B EIA Interim Standard were the procedures used for testing the SA601/SA606 demoboard. These tests were crucial in determining performance of the demoboard.

Figure 10 shows the block diagram of the test setup following the procedures outlined in the AMPS specification.

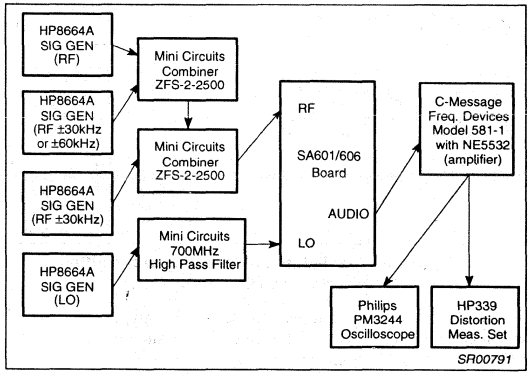

Figure 10. Test Setup for Measuring RF Sensitivity, Adjacent and Alternate Channel Rejection and Spurious Rejection

Transmitter desensitization occurs when the transmit signal from the handset is degrading the performance of the receiver.

To measure transmitter (Tx) desensitization, do the following:

1. Configure the test equipment as shown in Figure 11.
2. Set the Tx signal 45MHz below the RF signal.
3. Measure the Tx power at the Ant of the duplexer on the HP8920A Radio Test Set.
4. Measure 12dB SINAD on the HP8920A Radio Test Set when the Tx signal is on and again when it is off.
5. If there is degradation in sensitivity when the Tx signal is on, the difference of the 12dB SINAD readings is the Tx desensitization.

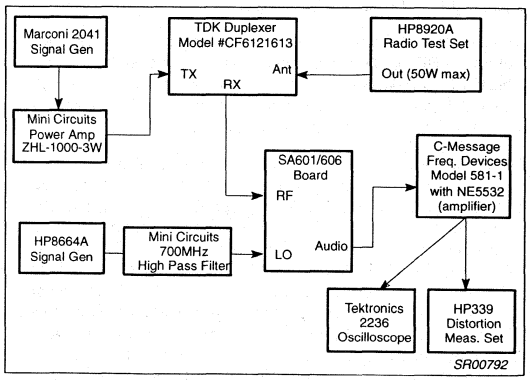

Figure 11. Test Setup for Measuring Transmitter Desensitization

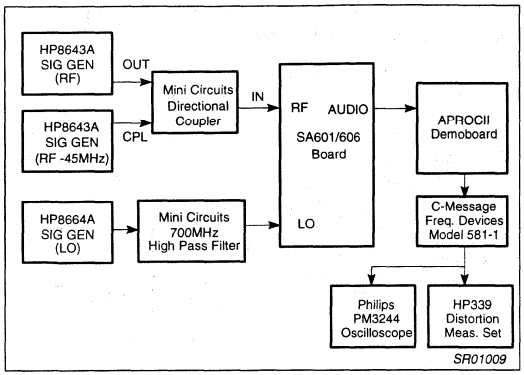

Figure 12. Test Setup for Measuring Transmitter Desensitization Without Duplexer

Because customers' preferences for duplexers vary, Tx desensitization was done another way to evaluate the performance of the SA601/SA606 demoboard.

1. The setup can be configured as shown in Figure 12. Set RF = 869MHz, LO = 957.16MHz and Tx = 824MHz.
2. Set the transmit power to -10dBm because we are assuming that the Tx leakage through the Rx port is that much.
3. Record 12dB SINAD.
4. Reduce the transmit power by 1dB and repeat Step 3.
5. Repeat Step 4 until Tx power reaches -30dBm.
6. Repeat all steps for RF, LO Tx frequencies at mid band (RF = 881MHz, LO = 964.16MHz, Tx = 836MHz) and high band (RF = 894MHz, LO = 977.16MHz, Tx = 849MHz)

Data and Results

Adjacent Channel, Alternate Channel and Intermodulation Spurious Response

The data provided in Tables 4 to 6 shows the sensitivity, adjacent channel, alternate channel, and intermodulation spurious response of the demoboard. The data was taken at V_{CC} = 3V, 4V, and 5V, as well as at three different frequencies.

The data taken was recorded without a duplexer. Adding a duplexer before the RF input will cause sensitivity to decrease by about 3 dB. This board is well within the specified parameters for adjacent channel, alternate channel and intermodulation spurious response rejection in accordance with AMPS specifications.

Protection Against Spurious Response Interference

The next set of data shown is also part of the AMPS specification 2.3.4 Protection Against Spurious Response Interference (Tables 7 to 9). The frequencies tested were the image frequencies that could cause degradation in performance. When using a TDK duplexer (TDK BandPass Filter Model CF6121613), the image frequencies are attenuated, so the image spurs (1047.32MHz) will not degrade the performance of the demoboard. The 2nd IF image frequency is the only frequency that caused problems. This frequency is above the RF by exactly twice the 2nd IF (2 × 455kHz = 910kHz). The problem occurs because, when RF + 910kHz mixes with the 1st LO (964.16MHz), the frequency produced is (RF + 910kHz –1st LO = 82.25MHz). This is equal to the 2nd IF image frequency. When the 2nd IF image frequency is mixed with the crystal oscillator, the frequency produced is the 2nd-IF frequency. The SA606 will demodulate this unwanted frequency, as well as the desired signal.

Example:

RF = 881MHz
LO = 964.16MHz
2nd LO = 82.705MHz
881MHz + 910kHz = 881.91MHz
881.910MHz mixes with the LO (964.16MHz) = 82.25MHz
82.25MHz mixes with the 2nd LO (82.705MHz) = 455kHz

To resolve this problem, the 83.161MHz SAW filter must be isolated. The unwanted frequency was leaking around the SAW filter and into the RF input of the SA606. So the distance between the SA601 mixer out to the RF input of the SA606 was increased by rotating the SAW filter. This solved the problem and the board met the protection against spurious response specification with at least 14dB to spare.

Transmitter desensitization

Another issue was to evaluate how the SA601/SA606 performs with the transmit section of a radio on (transmitter desensitization). Transmitter desensitization will degrade the sensitivity of the receiver if the strong Tx signal is allowed to pass through and cause the SA601 to reach its 1dB compression point in the LNA and the Mixer. Tables 10 to 12 show the results of three test boards for transmitter desensitization as the transmit power is increased from 100mW to 1W.

Using a TDK duplexer (TDK BandPass Filter Model CF6121613), the board performed well. At most, the board degraded by 2dB from the transmitter desensitization.

Since most customers will not want to use the TDK duplexer, Tx desensitization was done another way, as explained in the procedures. Table 13 show the results. The results show that with a duplexer that has Tx leakage of -14dBm or less through the Rx port, the SA601/SA606 will meet the sensitivity requirement according to IS-19-B (-116dBm for 12 dB SINAD), assuming the duplexer has 3dB of loss.

RSSI, AM Rejection, THD, Noise, Audio Output Level

The next set of data shows RSSI performance at 3V, 4V, and 5V (Figure 13) and AM rejection, THD, Noise, and Audio output level (Figure 14).

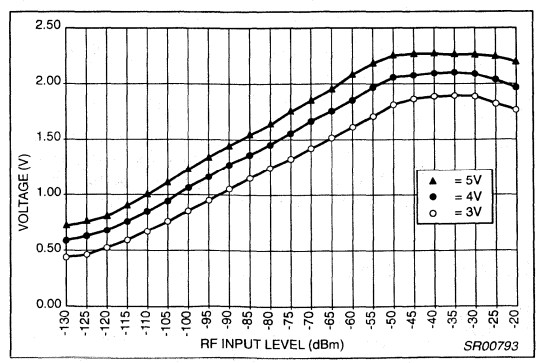

Figure 13. RSSI (Average of Three Boards)

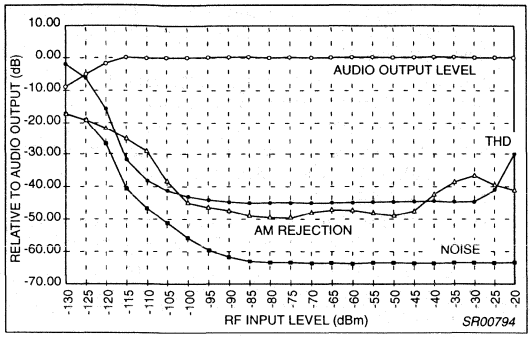

Figure 14. Receiver Performance (Average of Three Boards)

IV. CONCLUSION

The SA601/SA606 application demoboard demonstrates how well the two chips perform together. Meeting the stated AMPS cellular specifications is a good test of a receiver's performance. Not all receivers can meet these stringent requirements. The SA601/SA606 demoboard not only meets, but exceeds, the criteria of sensitivity with 12dB SINAD of about -122dBm, which is 3dB better than AMPS specification, assuming 3dB loss from the duplexer. Adjacent channel exceeds the requirement by 33dB, Alternate channel exceeds the requirement by 7.5dB, Intermodulation Spurious Response exceeds the requirement by 4.5dB, and Protection Against Spurious Response Interference exceeds the requirement by 11dB.

Many key factors such as board layout and impedance matching help the performance exceed the receiver specifications for AMPS. Many issues looked at in this application note will help answer customers' questions as Philips customers design greater and better things.

Questions and Answers

Q. What is the difference between the 50 Ω demoboard and the high-impedance demoboard?

A. Visually, the 50 Ω boards have more components near the 83.161MHz SAW filter. The 50 Ω boards have two 5-30pF trim capacitors. The high-impedance board out performs the 50 Ω board by 1dB on sensitivity. Keep in mind that the 50 Ω board allows troubleshooting of each block.

Q. What do I do if I don't achieve the sensitivity as the data shows?

A. Here is a check list you can follow:

1. Check the solder connections.
2. Make sure the LO drive level is -5dBm to -7dBm to the SA601 mixer.
3. Check for the 700MHz high pass filter (see Figure 10).
4. Check the C-Message filter. (An active C-Message filter with 10dB of gain was used for sensitivity tests.)
5. Probe for signals from the SA601 inputs down to the SA606 limiter-out. Check to see if there are significant losses. The probe points are:
   a. RF input of the SA601
   b. LO input of the SA601
   c. LNA-out of the SA601
   d. Before the 881MHz SAW filter
   e. After the 881MHz SAW filter
   f. Mixer-in of the SA601
   g. Mixer-out of the SA601
   h. Before the 83.161MHz SAW filter
   i. After the 83.161MHz SAW filter
   j. RF input of the SA606
   k. The 82.705MHz crystal
   l. Mixer-out of the SA606
   m. IF-in of the SA606
   n. IF-out of the SA606
   o. Limiter-in of the SA606
   p. Limiter-out of the SA606

Q. What is the difference between the 1008HS and the 1008CS inductors from Coilcraft?

A. There is no difference in performance between the two types of inductors. The only external difference is the packaging.

Q. What should I do if I don't meet the specification for Protection Against Spurious-Response?

A. Make sure that all the grounds of the 83.161MHz SAW filter are connected, especially the grounds closest to the input and output. Shield each section which will isolate each block and improve performance.

Q. Why do you use an IF of 83.16MHz instead of 45MHz?

A. 83.16MHz is used as the IF because, at 45MHz, serious problems may result because of the existence of spurious performance degradation and potential interference due to the half-IF mixer spurious content. The half-IF (RF + 22.5MHz) is only a problem with IF frequencies which are less than twice the receiver bandwidth. An AMPS receiver with 45MHz 1st IF can have a half-IF problem, while at 83.16MHz it will not because the half-IF, at 45MHz for example, will be 891.50MHz (869MHz + 22.5MHz). Since 891.5MHz falls in the pass band, this signal will desensitize the receiver. Also, at 83.16MHz, the image frequency is further away than 45MHz. (See Reference 8)

Q. Will phase noise of the signal generator cause performance degradation when testing Tx desensitization?

A. Yes it will because, when doing the Tx desensitization test without a duplexer, sensitivity dramatically improved as levels on the signal generator were decremented. Also, when cascading two duplexers together, the noise was attenuated and sensitivity improved.

In most handsets, a bandpass filter (center frequency at 836MHz) is placed before the power amplifier; therefore, the out-of-band noise is attenuated before being amplified. This attenuation will lower the phase noise and allow less Tx desensitization.

Q. What spurs will effect the sensitivity of the receiver? How can these spurs be rejected?

A. Consult table below for unwanted spurs:

Spurs	EQ.[1]	Range (MHz)	Rejected by...
1st Image	RF+2(IF1)	1035.32–1060.32	Duplexer
2nd Image	RF+2(IF2)	869.91–894.91	83.16MHz SAW
Half IF	RF+.5(IF1)	910.58–935.58	Duplexer
Tx Intermod[2]	Tx–45MHz	779–804	Duplexer
Tx Isolation[2]	Tx + IF1	907.16–932.16	Duplexer

NOTES:
1. IF1 = 83.16MHz; IF2 = 455kHz
2. Not measured

V. REFERENCES

1. "AN1777: Low Voltage Front-End Circuits", RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
2. "AN1993: High sensitivity application of low-power RF/IF Integrated circuits", RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
3. "AN1994: Reviewing key areas when designing with the NE605", RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
4. "AN1995: Evaluating the NE605 SO and SSOP demoboard, RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
5. "AN1996: Demodulation at 10.7MHz IF with NE/SA605/625", RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
6. "Low-voltage LNA and mixer - 1GHz", (SA601 data sheet), RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
7. "Low-voltage high performance mixer FM IF system", (SA606 data sheet), RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
8. Victor, Alan, "Saw Filters Aid Communications System Performance", Microwaves and RF, Aug. 1991, pg. 104-111.
9. "Recommended Minimum Standards for 800-MHz Cellular Subscriber Units", EIA/IS-19-B. Electronic Industries Association, 1988.

Table 4. RF Sensitivity, Adjacent and Alternate Channel Rejection, and Intermodulation Spurious Response Rejection at V_{CC} = 3V

All data taken without a duplexer.

Frequency	12 dB SINAD	Adjacent Channel Above (+30kHz)	Adjacent Channel Below (-30kHz)	Alternate Channel Above (+60kHz)	Alternate Channel Below (-60kHz)	Intermodulation Spurious Response (+60 & +120 kHz)	Intermodulation Spurious Response (-60 & -120 kHz)
High Impedance Board #1: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	55 dB	53 dB	86 dB	88 dB	71.5 dB	70.5 dB
RF = 869MHz; LO = 952.161MHz	-122 dBm	49 dB	50 dB	88 dB	87 dB	70.5 dB	70.5 dB
RF = 894MHz; LO = 977.161MHz	-122 dBm	51 dB	54 dB	88 dB	87 dB	71.5 dB	70 dB
High Impedance Board #2: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122.5 dBm	51.5 dB	52.5 dB	71.5 dB	77.5 dB	71 dB	71 dB
RF = 869MHz; LO = 952.161MHz	-123 dBm	52 dB	51 dB	72 dB	82 dB	70.5 dB	70.5 dB
RF = 894MHz; LO = 977.161MHz	-122.5 dBm	51.5 dB	50.5 dB	72.5 dB	77.5 dB	69.5 dB	69.5 dB
High Impedance Board #3: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	49 dB	54 dB	91 dB	87 dB	73 dB	71 dB
RF = 869MHz; LO = 952.161MHz	-123 dBm	50 dB	56 dB	93 dB	88 dB	73 dB	71 dB
RF = 894MHz; LO = 977.161MHz	-122 dBm	50 dB	55 dB	92 dB	89 dB	72 dB	71 dB

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better
2.3.2 Adjacent and Alternate Channel Desensitization: 16dBm min for adjacent channel; 60dB min for alternate channel.
2.3.3 Intermodulation Spurious Response Interference: 65dB min.

Table 5. RF Sensitivity, Adjacent and Alternate Channel Rejection, and Intermodulation Spurious Response Rejection at V_{CC} = 4V

All data taken without a duplexer.

Frequency	12 dB SINAD	Adjacent Channel Above (+30kHz)	Adjacent Channel Below (-30kHz)	Alternate Channel Above (+60kHz)	Alternate Channel Below (-60kHz)	Intermodulation Spurious Response (+60 & +120 kHz)	Intermodulation Spurious Response (-60 & -120 kHz)
High Impedance Board #1: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	51 dB	52 dB	88 dB	86 dB	71.5 dB	69.5 dB
RF = 869MHz; LO = 952.161MHz	-122 dBm	50 dB	51 dB	88 dB	87 dB	72.5 dB	69.5 dB
RF = 894MHz; LO = 977.161MHz	-122 dBm	51 dB	51 dB	87 dB	87 dB	72 dB	70 dB
High Impedance Board #2: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122.5 dBm	51.5 dB	51.5 dB	70.5 dB	67.5 dB	70.5 dB	69.5 dB
RF = 869MHz; LO = 952.161MHz	-122.5 dBm	52.5 dB	50.5 dB	71.5 dB	80.5 dB	69 dB	69 dB
RF = 894MHz; LO = 977.161MHz	-122 dBm	52 dB	51 dB	72 dB	76 dB	70 dB	76 dB
High Impedance Board #3: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	50 dB	55 dB	91 dB	87 dB	73 dB	71 dB
RF = 869MHz; LO = 952.161MHz	-123 dBm	50 dB	54 dB	93 dB	88 dB	73 dB	70 dB
RF = 894MHz; LO = 977.161MHz	-123 dBm	50 dB	53 dB	91 dB	87 dB	72 dB	70 dB

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better
2.3.2 Adjacent and Alternate Channel Desensitization: 16dBm min for adjacent channel; 60dB min for alternate channel.
2.3.3 Intermodulation Spurious Response Interference: 65dB min.

Table 6. RF Sensitivity, Adjacent and Alternate Channel Rejection, and Intermodulation Spurious Response Rejection at V_{CC} = 5V.

All data taken without a duplexer.

Frequency	12 dB SINAD	Adjacent Channel Above (+30kHz)	Adjacent Channel Below (-30kHz)	Alternate Channel Above (+60kHz)	Alternate Channel Below (-60kHz)	Intermodulation Spurious Response (+60 & +120 kHz)	Intermodulation Spurious Response (-60 & -120 kHz)
High Impedance Board #1: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	50 dB	52 dB	86 dB	85 dB	71.5 dB	69.5 dB
RF = 869MHz; LO = 952.161MHz	-122 dBm	49 dB	52 dB	87 dB	86 dB	71.5 dB	69 dB
RF = 894MHz; LO = 977.161MHz	-122 dBm	52 dB	51 dB	86 dB	86 dB	72 dB	70 dB
High Impedance Board #2: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	52 dB	50 dB	70 dB	76 dB	70.5 dB	69.5 dB
RF = 869MHz; LO = 952.161MHz	-122.5 dBm	52.5 dB	49.5 dB	70.5 dB	78.5 dB	69 dB	69 dB
RF = 894MHz; LO = 977.161MHz	-121.5 dBm	52.5 dB	50.5 dB	71.5 dB	75.5 dB	70 dB	68 dB
High Impedance Board #3: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-121.5 dBm	49.5 dB	53.5 dB	90.5 dB	86.5 dB	73 dB	70 dB
RF = 869MHz; LO = 952.161MHz	-122.5 dBm	52.5 dB	49.5 dB	87.5 dB	91.5 dB	73 dB	70 dB
RF = 894MHz; LO = 977.161MHz	-121 dBm	50 dB	53 dB	91 dB	87 dB	72 dB	70 dB

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better
2.3.2 Adjacent and Alternate Channel Desensitization: 16dBm min for adjacent channel; 60dB min for alternate channel.
2.3.3 Intermodulation Spurious Response Interference: 65dB min.

Table 7. Protection Against Spurious Response Interference V_{CC} = 3V

All test measured with TDK duplexer (Model CF6121613D)

Frequency	Interfering Frequency (MHz)	Board #1	Board #2	Board #3
RF = 881MHz; LO = 964.161MHz		**-121 dBm for 12 dB SINAD**	**-121 dBm for 12 dB SINAD**	**-121 dBm for 12 dB SINAD**
	881.91	82.5 dB	76.5 dB	78.5 dB
	922.58	108.5 dB	108.5 dB	108.5 dB
	1005.74	108.5 dB	108.5 dB	108.5 dB
	1047.32	99.5 dB	97.5 dB	92.5 dB
RF = 869MHz; LO = 952.161MHz		**-119.5 dBm for 12 dB SINAD**	**-121 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**
	869.91	81 dB	73.5 dB	75.5 dB
	910.58	108 dB	108.5 dB	107.5 dB
	993.74	108 dB	108.5 dB	107.5 dB
	1035.32	98 dB	95.5 dB	88.5 dB
RF = 894MHz; LO = 977.161MHz		**-119 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**	**-119.5 dBm for 12 dB SINAD**
	894.91	79.5 dB	82.5 dB	79 dB
	935.58	108.5 dB	110.5 dB	108 dB
	1018.74	108.5 dB	110.5 dB	108 dB
	1060.32	99.5 dB	100.5 dB	96 dB

Requirements per IS-19-B:

2.3.4 Protection Against Spurious Response Interference: 60dB min.

Table 8. Protection Against Spurious Response Interference V_{CC} = 4V

All test measured with TDK duplexer (Model CF6121613D)

Frequency	Interfering Frequency (MHz)	Board #1	Board #2	Board #3
RF = 881MHz; LO = 964.161MHz		**-121 dBm for 12 dB SINAD**	**-121 dBm for 12 dB SINAD**	**-121.5 dBm for 12 dB SINAD**
	881.91	84.5 dB	74.5 dB	79 dB
	922.58	108.5 dB	108.5 dB	109 dB
	1005.74	108.5 dB	108.5 dB	109 dB
	1047.32	101.5 dB	98.5 dB	93 dB
RF = 869MHz; LO = 952.161MHz		**-120 dBm for 12 dB SINAD**	**-120.5 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**
	869.91	80.5 dB	71 dB	73.5 dB
	910.58	107.5 dB	108 dB	107.5 dB
	993.74	107.5 dB	108 dB	107.5 dB
	1035.32	95.5 dB	93 dB	88.5 dB
RF = 894MHz; LO = 977.161MHz		**-119.5 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**
	894.91	80 dB	78.5 dB	81.5 dB
	935.58	108 dB	108.5 dB	107.5 dB
	1018.74	108 dB	108.5 dB	107.5 dB
	1060.32	100 dB	99.5 dB	95.5 dB

Requirements per IS-19-B:

2.3.4 Protection Against Spurious Response Interference: 60dB min.

Table 9. Protection Against Spurious Response Interference V_{CC} = 5V

All test measured with TDK duplexer (Model CF6121613D)

Frequency	Interfering Frequency (MHz)	Board #1	Board #2	Board #3
RF = 881MHz; LO = 964.161MHz		**-121 dBm for 12 dB SINAD**	**-121 dBm for 12 dB SINAD**	**-121.5 dBm for 12 dB SINAD**
	881.91	84.5 dB	74 dB	77.5 dB
	922.58	108.5 dB	109 dB	108.5 dB
	1005.74	108.5 dB	109 dB	108.5 dB
	1047.32	108.5 dB	97 dB	104.5 dB
RF = 869MHz; LO = 952.161MHz		**-120 dBm for 12 dB SINAD**	**-120.5 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**
	869.91	79.5 dB	71 dB	71 dB
	910.58	107.5 dB	108 dB	108 dB
	993.74	107.5 dB	108 dB	108 dB
	1035.32	101.5 dB	94 dB	93 dB
RF = 894MHz; LO = 977.161MHz		**-119.5 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**
	894.91	80.5 dB	77 dB	81.5 dB
	935.58	107.5 dB	108 dB	111.5 dB
	1018.74	107.5 dB	108 dB	111.5 dB
	1060.32	106.5 dB	100 dB	106.5 dB

Requirements per IS-19-B:

2.3.4 Protection Against Spurious Response Interference: 60dB min.

Table 10. Transmit desensitization – Board #1

Frequency	Transmit Power (mW)	12 dB SINAD without Tx (dBm)	12 dB SINAD with Tx (dBm)	Tx desensitization (dB)
RF = 881MHz; LO = 964.161MHz, Tx = 836MHz				
	100	-120	-119.5	0.5
	200	-120	-119.5	0.5
	300	-120	-119	1
	400	-120	-119	1
	500	-120	-119	1
	600	-120	-119	1
	700	-120	-119	1
	800	-120	-118	2
	900	-120	-118	2
	1000	-120	-118	2
RF = 869MHz; LO = 952.161MHz, Tx = 824MHz				
	100	-119.5	-119.5	0
	200	-119.5	-119.5	0
	300	-119.5	-119.5	0
	400	-119.5	-119.5	0
	500	-119.5	-119.5	0
	600	-119.5	-119.5	0
	700	-119.5	-119.5	0
	800	-119.5	-119.5	0
	900	-119.5	-119.5	0
	1000	-119.5	-119.5	0
RF = 894MHz; LO = 977.161MHz, Tx = 849MHz				
	100	-119	-119	0
	200	-119	-119	0
	300	-119	-119	0
	400	-119	-119	0
	500	-119	-119	0
	600	-119	-119	0
	700	-119	-119	0
	800	-119	-119	0
	900	-119	-119	0
	1000	-119	-119	0

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better

Table 11. Transmit desensitization – Board #2

Frequency	Transmit Power (mW)	12 dB SINAD without Tx (dBm)	12 dB SINAD with Tx (dBm)	Tx desensitization (dB)
RF = 881MHz; LO = 964.161MHz, Tx = 836MHz				
	100	-120	-119.5	0.5
	200	-120	-119.5	0.5
	300	-120	-119	1
	400	-120	-119	1
	500	-120	-119	1
	600	-120	-119	1
	700	-120	-119	1
	800	-120	-118	2
	900	-120	-118	2
	1000	-120	-118	2
RF = 869MHz; LO = 952.161MHz, Tx = 824MHz				
	100	-119.5	-119.5	0
	200	-119.5	-119.5	0
	300	-119.5	-119.5	0
	400	-119.5	-119.5	0
	500	-119.5	-119.5	0
	600	-119.5	-119.5	0
	700	-119.5	-119.5	0
	800	-119.5	-119.5	0
	900	-119.5	-119.5	0
	1000	-119.5	-119.5	0
RF = 894MHz; LO = 977.161MHz, Tx = 849MHz				
	100	-119.5	-119.5	0
	200	-119.5	-119.5	0
	300	-119.5	-119.5	0
	400	-119.5	-119.5	0
	500	-119.5	-119.5	0
	600	-119.5	-119	0.5
	700	-119.5	-119	0.5
	800	-119.5	-119	0.5
	900	-119.5	-119	0.5
	1000	-119.5	-119	0.5

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better

Table 12. Transmit desensitization – Board #3

Frequency	Transmit Power (mW)	12 dB SINAD without Tx (dBm)	12 dB SINAD with Tx (dBm)	Tx desensitization (dB)
RF = 881MHz; LO = 964.161MHz, Tx = 836MHz				
	100	-119.8	-119.3	0.5
	200	-119.8	-119.3	0.5
	300	-119.8	-118.8	1
	400	-119.8	-118.8	1
	500	-119.8	-118.8	1
	600	-119.8	-118.8	1
	700	-119.8	-118.8	1
	800	-119.8	-117.8	2
	900	-119.8	-117.8	2
	1000	-119.8	-117.8	2
RF = 869MHz; LO = 952.161MHz, Tx = 824MHz				
	100	-119	-117	0
	200	-119	-117	0
	300	-119	-117	0
	400	-119	-117	0
	500	-119	-117	0
	600	-119	-117	0
	700	-119	-117	0
	800	-119	-117	0
	900	-119	-117	0
	1000	-119	-117	0
RF = 894MHz; LO = 977.161MHz, Tx = 849MHz				
	100	-119	-119	0
	200	-119	-119	0
	300	-119	-119	0
	400	-119	-119	0
	500	-119	-119	0
	600	-119	-118.5	0.5
	700	-119	-118.5	0.5
	800	-119	-118.5	0.5
	900	-119	-118.5	0.5
	1000	-119	-118.5	0.5

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better

Table 13. Transmit desensitization Without Duplexer

Tx Level (dBm)	Board #1			Board #2			Board #3		
	12dB SINAD (dBm)			12dB SINAD (dBm)			12dB SINAD (dBm)		
	824MHz	836MHz	849MHz	824MHz	836MHz	849MHz	824MHz	836MHz	849MHz
-10	-118.5	-117.5	-117	-119	-118.5	-117.5	-119	-118.5	-117.5
-11	-118.5	-118	-117	-119	-118.5	-117.5	-119	-118.5	-117.5
-12	-118.5	-118	-117	-119.5	-118.5	-118	-119.5	-119	-117.5
-13	-119	-118.5	-117.5	-119.5	-119	-118	-119.5	-119	-118
-14	-120	-119.5	-119	-120.5	-120	-119.5	-121	-120.5	-119
-15	-120	-120	-119	-121	-120.5	-119.5	-121	-120.5	-119.5
-16	-120.5	-120	-119.5	-121	-120.5	-120	-121	-121	-120
-17	-120.5	-120	-119.5	-121	-121	-120.5	-121	-121	-120
-18	-120.5	-120.5	-120	-121	-121	-120.5	-121.5	-121	-120.5
-19	-121	-121	-120.5	-122	-121.5	-121.5	-122	-122	-121
-20	-121.5	-121	-121	-122	-122	-121.5	-122	-122	-121.5
-21	-121.5	-121	-121	-122	-122	-121.5	-122.5	-122	-121.5
-22	-121.5	-121.5	-121	-122	-122	-122	-122.5	-122.5	-121.5
-23	-121.5	-121.5	-121.5	-122.5	-122	-122	-122.5	-122.5	-121.5
-24	-122	-122	-121.5	-122.5	-122.5	-122	-122.5	-122.5	-121.5
-25	-122	-122	-121.5	-122.5	-122.5	-122.5	-123	-123	-121.5
-26	-122	-122	-121.5	-122.5	-122.5	-122.5	-123	-123	-122
-27	-122	-122	-122	-123	-122.5	-122.5	-123	-123	-122
-28	-122	-122	-122	-123	-122.5	-122.5	-123	-123	-122
-29	-122.5	-122	-122	-123	-123	-122.5	-123	-123	-122.5
-30	-122.5	-122	-122	-123	-123	-122.5	-123	-123	-122.5
OFF	-122.5	-122	-122	-123	-123	-122.5	-123	-123	-122.5

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better

Table 14. Customer Application Component List for SA601/SA606

Qty.	Part Value	Part Reference	Part Description	Vendor	Mfg	Part Number
****** Surface Mount Capacitors ******						
1	2.2pF	C13	NPO Ceramic 0805 ±.25pF	Garrett	Philips	0805CG229C9BB0
1	2.7pF	C2	NPO Ceramic 0805 ±.25pF	Garrett	Philips	0805CG279C9BB0
1	2.7pF	C18 for Hi Z board	NPO Ceramic 1206 ±.25pF	Garrett	Rohm	1206MCH315A2R7CK
1	3.3pF	C16	NPO Ceramic 0805 ±.25pF	Garrett	Philips	0805CG339C9BB0
1	4.7pF	C10	NPO Ceramic 0805 ±.25pF	Garrett	Philips	0805CG479C9BB0
2	8.2pF	C7, C17	NPO Ceramic 0805 ±5pF	Garrett	Philips	0805CG829C9BB0
2	10pF	C23, C31	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG100J9BB0
1	18pF	C6	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG180J9BB0
1	24pF	C6 for Hi Z board	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG240J9BB0
1	33pF	C8	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG330J9BB0
1	39pF	C19	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG390J9BB0
6	100pF	C1, C4, C5, C11, C12, C14	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG101J9BB0
1	390pF	C29	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG391J9BB0
2	1nF	C22, (C7 for Hi Z board)	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG102J9BB0
10	100nF	C9, C15, C20, C25, C30, C32, C33, C34, C35, C36	Z5U Ceramic 0805 ±20%	Garrett	Philips	08052E104M9BB0
1	1µF	C3	Tant Chip Cap ±10%	Garrett	Philips	49MC105A016KOAS
2	2.2µF	C26, C27	Tant Chip Cap ±10%	Garrett	Philips	49MC225A010KOAS
1	10µF	C24	Tant Chip Cap ±10%	Garrett	KOA Speer	TMC-M1AB106KLRH
2	5-30pF	C18, C21	SMT Trimmer Cap	Jaco	Kyocera	CTZ3S-30C-B
****** Resistors ******						
1	0Ω	R5	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F000
1	100Ω	R1	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F101
1	2.2kΩ	R2	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F222
1	2.4kΩ	R8	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F242
1	3.3kΩ	R9	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F332
1	8.2kΩ	R4	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F822
1	10kΩ	R3	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F103
1	11kΩ	R7	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F113
****** Inductors ******						
1	56nH	L1	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-560 ±10%
1	270nH	L3	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-271 ±10%
2	330nH	L5, L6	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-331 ±10%
1	470nH	L2	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-471 ±10%
1	560nH	L4	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-561 ±10%
1	750nH	L6 Hi Z board	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-751 ±10%
1	1.2µH	L7	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-122 ±10%
1	330µH	L9	Variable SMT Inductor	Digikey	Toko	TKS2272CT-ND ±3%
1	1µH	L8	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-102 ±10%
****** Filters ******						
1	881.5MHz	FILT1	881.5MHz SAW Bandpass	Murata	Murata	SAFC881.5MA70N-TC
1	83.161MHz	FILT2	83.161MHz SAW Bandpass	Murata	Murata	SAFC83.161MA51X-TC
2	455kHz	FILT3, FILT4	455kHz FM IF Filter	Murata	Murata	SFGCG455BX-TC
****** IC ******						
1	SA601	U1	Low Voltage LNA & Mixer	Philips	Philips	SA601DK
1	SA606	U2	Low Voltage FM IF System	Philips	Philips	SA606DK
****** Miscellaneous ******						
1	82.705MHz	X1	82.705MHz crystal	Hy-Q International or Reeves–Hoffman 82.705MHz		
2			SMA Gold Connector	Digikey J502-ND		EF Johnson 142-0701-801
1			5 Pins Gold Test point	Digikey		3M929647-01-36-ND
1			Printed circuit board	RF# 30042		Excel 601/606 #30042

433MHz front-end with the SA601 or SA620 AN95021

Author: Rob Bouwer

ABSTRACT

Although designed for 1GHz, the SA601 and SA620 can also be used in the 433MHz ISM band. The SA601 performs amplification of the antenna signal and down conversion to a first IF. The SA620 has the same functionality, but also has a VCO on-chip. This VCO drives the mixer, so no external LO signal is required.

Applying the SA601 or SA620 means that a receiver with high sensitivity and wide dynamic range can be built without a lot of external components. The design will be easier compared with discrete Front Ends.

Combined with an IF system like the SA676, a high performance dual conversion receiver can be built. This receiver can operate from 2.7 to 5.5V allowing the use of a 3-cell battery. IF frequencies can be chosen according to one's needs with a maximum first IF of 100MHz and a maximum second IF frequency of 2MHz.

This application note explains how to use the SA601 or SA620 at 433MHz. The performance at 433MHz is discussed. The application circuit diagrams that are used to obtain the measurement results are shown.

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1. INTRODUCTION

The SA601 and SA620 address high performance applications at 1GHz like cellular and cordless phones. The SA601 comprises a Low Noise Amplifier (LNA) and a Mixer. The SA620 comprises, besides an LNA and Mixer, a VCO (Voltage Controlled Oscillator). Although intended for 1GHz, it is possible to apply these Front-Ends at lower frequencies.

This paper describes the performance of these devices at 433MHz. This band is being used for remote control systems, car alarms, telemetry, wireless audio links, etc.

By using the SA601 or SA620 followed by, for example an SA676 FM IF, a low voltage, high performance receiver for FM, AM, FSK, ASK demodulation can be built. The Front-Ends require only a few passive components for decoupling and signal handling. No extra circuitry is required for compensation for temperature and power supply variations. This will ease your 433MHz receiver design without trading off performance, and give you fast time to market.

2. SA601

The SA601 comprises a 1.2GHz LNA and Mixer. The block diagram is shown in Figure 1. In a receiver it performs the amplification of the antenna signal and the down conversion to the first IF frequency. This signal can then be handled by an IF system like the SA676 which takes care of AM and FM demodulation.

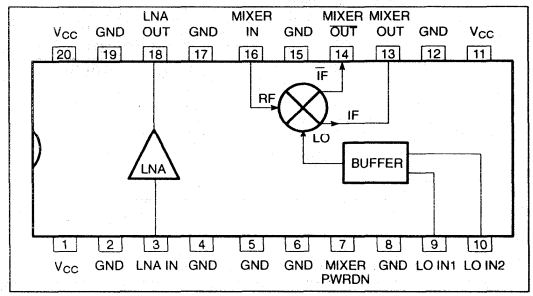


Figure 1. SA601 Block Diagram

Using the SA601 at 433MHz will show the following differences compared to the performance at 900MHz:

- The LNA will show a higher gain while having the same Noise Figure (NF)
- Because of this higher gain, the Intercept point (IP3) becomes less

The higher gain increases the sensitivity of the receiver. It also offers the possibility to allow some mismatch at the LNA input and hence, some gain loss. This means that a 50Ω source can be connected directly to the LNA input without matching. In case you do want to calculate the matching circuits for the LNA and mixer input, Table 1 shows the S-parameters of the LNA and mixer input at 433MHz.

The IP3 performance of the SA601 at 433MHz is worse than at 1GHz. However, it is still more than sufficient for applications in the 433MHz band.

Table 1. SA601 and SA620 S-parameters

	LNA				Mixer
	S_{11}	S_{22}	S_{21}	S_{12}	S_{11}
	R + j X	R + j X			R + j X
433MHz	34.0Ω - 62.8Ω	55.1Ω - 47.4Ω	5.4U ∠ 128°	62mU ∠ 68°	9.9Ω + 5.4Ω

2.1 Application circuit

The application circuit diagram is shown in Figure 2.

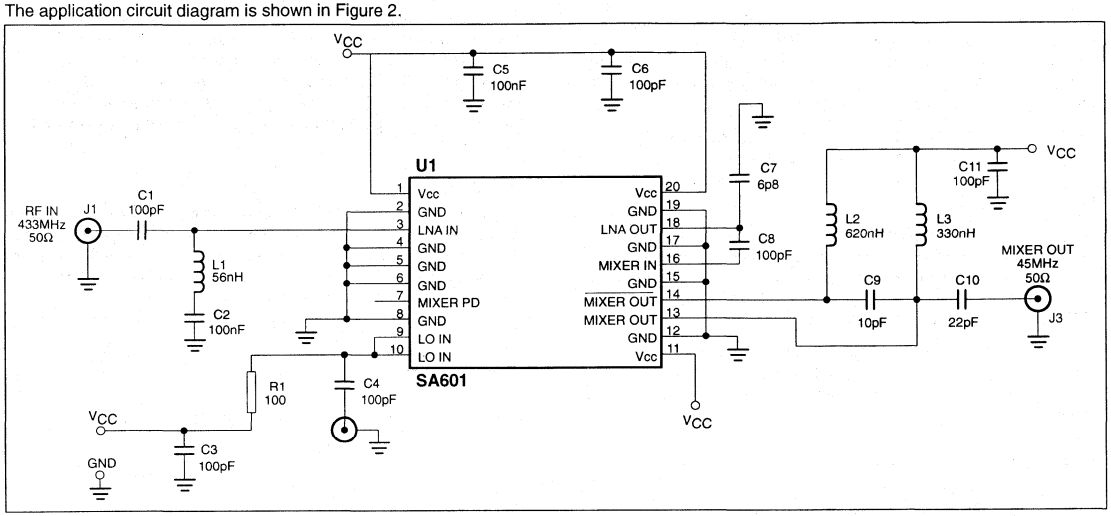


Figure 2. Application Circuit Diagram

Table 2. SA601 Application Components

C1	DC blocking	C9	Mixer output current combiner
C2	Time constant for LNA compensation loop	C10	Mixer output match to 50Ω load
C3	V_{CC} decoupling	C11	V_{CC} decoupling
C4	DC blocking	R1	LO input match
C5	Vcc decoupling	L1	AC blocking
C6	Vcc decoupling	L2	Mixer output current combiner
C7	LNA to Mixer input match	L3	Mixer output current combiner
C8	DC blocking		

Table 2 shows that most of the external components are for blocking DC at the in- and outputs and decoupling of the power supply. In your actual receiver the DC-blocking capacitors for RF IN, LO IN and MIXER OUT can be removed if there is no DC path present.

Capacitor C2 determines the bandwidth of the compensation loop of the LNA. The LNA is stabilized for temperature and power supply variations. To achieve a compensation loop which controls the LNA gain, the bandwidth of this control loop must be low compared to the actual input frequency. Otherwise the compensation loop and, thus, the LNA gain would be affected by the RF input signal.

To isolate C2 from the LNA input for 433MHz signals an inductor L1 is included. This forms a short for the compensation loop frequencies and an open for the 433MHz frequencies.

If there is already a DC path at the LNA input (J1) to ground, then L1 and C2 can be omitted. In that case C1 must be increased to 100nF. C1 has two functions then: block DC from the LNA input, and determine the bandwidth of the compensation loop.

The LNA output is matched to the Mixer input with a 6.8pF capacitor (C7) to ground and a series inductor of 9nH. This inductor is realized by the traces between LNA out and Mixer and the inductance of C8.

The SA601 mixer has differential outputs. This means that a direct interface with a symmetrical filter or symmetrical gain stage is possible. However, most filters are asymmetrical, therefore, a transformation from differential to single-ended is required. With a current combiner circuit[1], the differential output currents are shifted such that they are in phase. These currents are then combined to create a single-ended output. L2, L3 and C9 form this current combiner circuit.

The inductor can be calculated as follows:

- Choose a value for C9: 10pF
- F is 45MHz
- Calculate L for appropriate current combining

$$F = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot 2 \cdot C}}$$

$$L = \frac{1}{(2 \cdot \pi \cdot F)^2 \cdot 2 \cdot C} = \frac{1}{(2 \cdot \pi \cdot 45MHz) \cdot 2 \cdot 10pF}$$

$$L = 625nH$$

1. A current combiner circuit for better mixer conversion gain, Sheng Lee, Alvin K. Wong, Michael G. Wong, Philips Semiconductors

Figure 3 shows the implementation of the calculated component values.

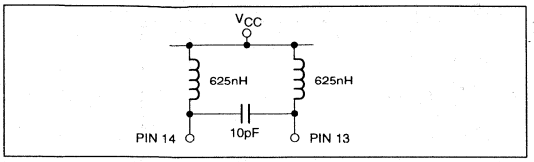


Figure 3. Current Combiner Circuit

After designing the current combiner circuit, the next step is to match the mixer output to the impedance of the load. In the application circuit the load is assumed to be 50 Ω. This is done to make evaluation more simple since most RF measurement equipment have 50 Ω inputs.

In addition to the impedance of the load (50 Ω), it is also important to know what the optimum load impedance is for the mixer output. For the SA601 mixer output this is 600 Ω. To create a matching from 600 to 50 Ω the circuit from Figure 4 is applied.

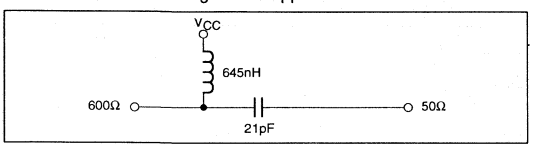


Figure 4. Mixer Output Match to 50Ω Load

The circuits from Figures 3 and 4 can be merged into one circuit as is shown in Figure 5. The values between brackets are the actual component values applied in the application circuit diagram.

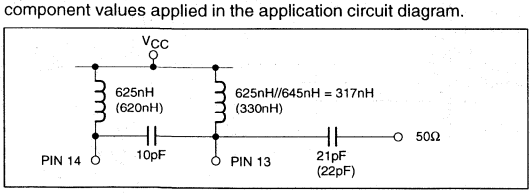


Figure 5. Mixer Output Circuitry With Current Combiner and 50Ω Matching

2.2 Measurement Results

For the measurements a power supply of 3V is applied. The RF frequency is 433MHz and the LO frequency is 478MHz with a level of -7dBm.

The current consumption of this application is 7.8mA.

2.2.1 Conversion gain, Noise Figure and IP3

In Table 3 the performance of the LNA and mixer is shown together with the overall performance.

Table 3. LNA, Mixer Measurement Results

	LNA	Mixer	LNA & Mixer	Units
Gain	15.4	9.2	24.7	dB
Noise Figure	1.5	12	2.5	dB
IIP3	-14.3	+1.7	-18.1	dBm

The results show that this Front-End offers 25dB of power gain with a noise figure contribution of only 2.5dB at 433MHz.

2.2.2 Isolation

Another important parameter for a Front-End receiver is the isolation between the Local Oscillator and the Antenna (LNA input). For 433MHz applications the requirement[2] is that spurious signals generated by the receiver have a maximum level of -57dBm for frequencies below 1GHz. The LO level measured at the LNA input is -53dBm. This means only 4dB extra suppression is required to meet the requirements. Because the Local Oscillator is offset 45MHz of the RF frequency, a simple bandpass filter, or the selectivity of the antenna, is already sufficient.

3. SA620

The SA620 comprises a 1.2GHz LNA, Mixer and VCO. The block diagram is shown in Figure 6. In a receiver the SA620 performs the amplification of the antenna signal and the down conversion to the first IF frequency. The VCO can be part of a phase-lock-loop or set to a fixed frequency by using a resonator. The output signal of the mixer can be handled by an IF system like the SA676 which takes care of AM and FM demodulation.

The S-parameters of the LNA and mixer input are the same as for the SA601. These parameters are shown in Table 1.

The LNA performance of the SA620 is the same as for the SA601. The mixer performance, however, is different. This is due to the output structure of the mixer. Figure 6 shows that there is one mixer output. Remember the SA601 has 2 mixer outputs which were combined using the current combiner circuit. Therefore, the mixer conversion gain is higher for the SA601 mixer. Furthermore, the SA620 incorporates a buffered VCO output (Pin 11) which can be used to drive the input of a frequency synthesizer.

3.1 Application circuit

Figure 7 shows the application circuit for a 433MHz receiver with a 478MHz VCO design.

2. ETSI I-ETS 300 220 Annex A.1.3.

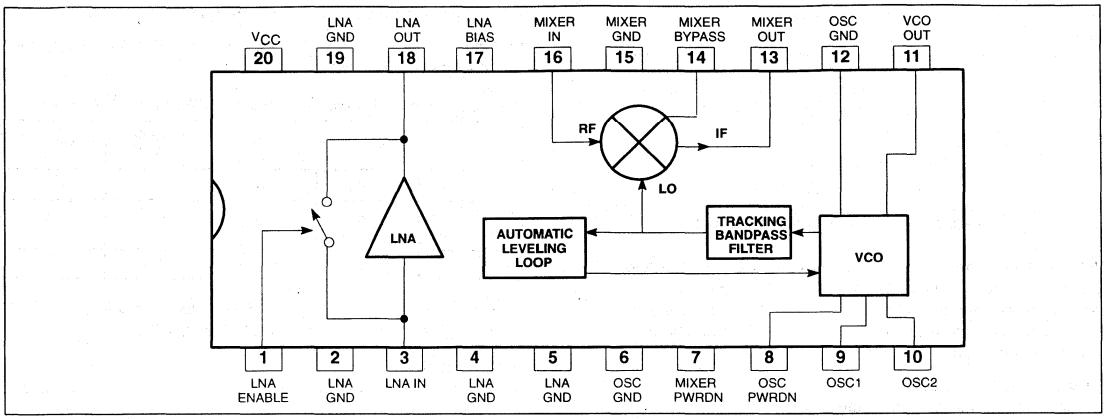


Figure 6. SA620 Block Diagram

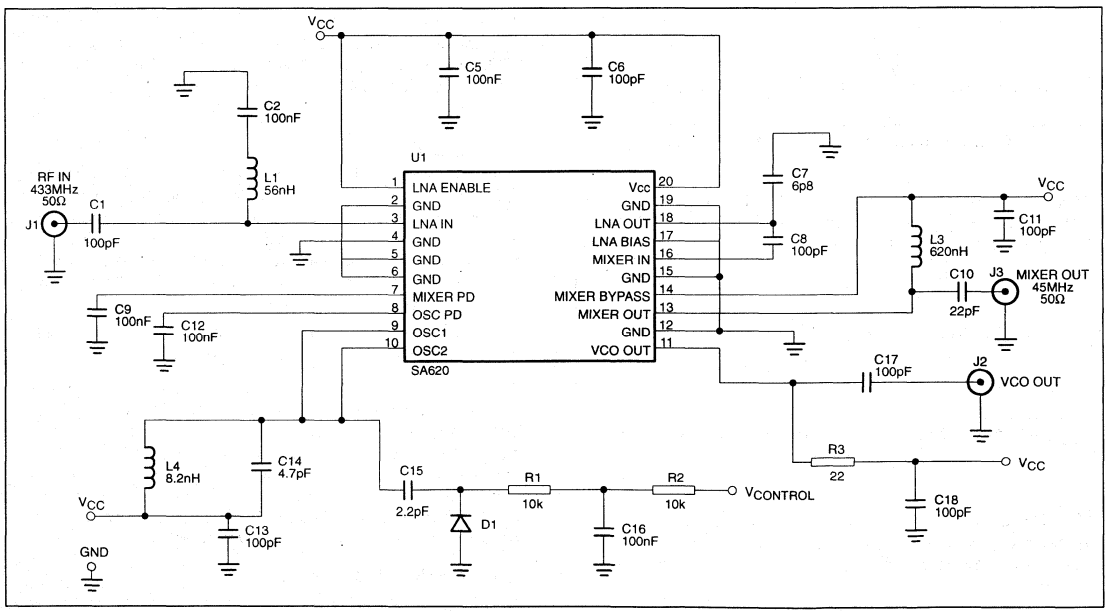


Figure 7. Application Circuit Diagram

Table 4 shows that most of the external components are for blocking DC at the in- and outputs and decoupling of the power supply. In your actual receiver the DC-blocking capacitors for RF IN, LO IN and MIXER OUT can be removed if there is no DC path present.

As with the SA601 capacitor, C2 determines the bandwidth of the compensation loop of the LNA. The LNA is stabilized for temperature and power supply variations. To achieve that a compensation loop controls the LNA gain. The bandwidth of this control loop must be low compared to the actual input frequency. Otherwise the compensation loop and, thus, the LNA gain, would be affected by the RF input signal. To isolate C2 from the LNA input for 433MHz signals, an inductor L1 is included. This forms a short for the compensation loop frequencies and an open for the 433MHz frequencies.

Table 4. SA620 Application Components

C1	DC blocking
C2	Timeconstant for LNA compensation loop
C5	V_{CC} decoupling
C6	V_{CC} decoupling
C7	LNA to Mixer input match
C8	DC blocking
C9	Mixer Bias decoupling
C10	Mixer output match to 50 Ω load
C11	V_{CC} decoupling
C12	VCO Bias decoupling
C13	V_{CC} decoupling
C14	Tuning capacitor
C15	Limits tuning range of VCO
C16	Filters noise at $V_{control\ line}$
C17	DC blocking
C18	V_{CC} decoupling
L1	AC blocking
L3	Mixer output match to 50 Ω load
L4	Tuning inductor
R1	Prevents loading of Tank circuit by the $V_{control\ line}$
R2	Filters noise at $V_{control\ line}$
D1	Varactor SMV 1204-099 Alpha Industries

If there is already a DC path at the LNA input (J1) to ground, then L1 and C2 can be omitted. In that case, C1 must be increased to 100nF. C1 has two functions then: block DC from the LNA input, and determine the bandwidth of the compensation loop.

The LNA output is matched to the Mixer input with a 6.8pF capacitor (C7) to ground and a series inductor of 9nH. This inductor can be realized by the traces between LNA Out and Mixer In and the parasitic inductance of C8.

The mixer output is matched to 50 Ω at 45MHz with L3 and C10.

The VCO output, Pin 11, delivers -20dBm into a 50 Ω load. The output level is set with R3. A lower output level can be achieved by reducing the value of this resistor. A higher value for R3 is not recommended because this will affect the VCO performance.

The components that determine the actual frequency of the VCO are L4, C14, C15 and D1 according to:

$$F = \frac{1}{2 \cdot \pi \cdot \sqrt{L4 \cdot \left(C14 + \left(\frac{C15 \cdot CD1}{C15 + CD1}\right)\right)}}$$

Figure 8.

The formula shows that the influence of the varactor D1 on the VCO frequency depends on the value of C15. That means that, if the tuning range of the VCO is too wide, it can be scaled back by reducing the value of C15.

The SA620 VCO can easily oscillate from 300 to 1.2GHz, so it is important to have only one resonance circuit at Pins 9 and 10. Also, parasitic resonances must be prevented, which can be accomplished by putting the components close to Pins 9 and 10, and by decoupling the power supply close to L4 and C14.

3.2 Measurement Results

For the measurements a power supply of 3V is applied. The RF frequency is 433MHz and the VCO frequency is tuned to 478MHz.

The current consumption of this application is 11.3mA.

3.2.1 Conversion gain, Noise Figure and IP3

In Table 5 the performance of the LNA and mixer is shown together with the overall performance.

Table 5. Measurement Results

	LNA	Mixer	LNA & Mixer	Units
Gain	15.5	4.5	19.5	dB
Noise Figure	1.5	8.5	2.6	dB
IIP3	-14.2	0.0	-18.5	dBm

The results show that this Front-End offers 19.5dB of power gain with a noise figure contribution of 2.6dB at 433MHz.

3.2.2 Isolation

The isolation between the LO signal and antenna input is -59dBm. The requirement[3] for 433MHz ISM band is -57dBm at the antenna input for signals outside the 433MHz band and below 1GHz. This means that, without any selectivity at the antenna input, this requirement is already met. In practice there will be selectivity from the antenna filter or the antenna itself, meaning the LO signal is further suppressed.

4. CONCLUSION

The advantages of using the SA601 or SA620 as a 433MHz Front End are:

- Ease of design
- Good performance
- Minimum amount of external components
- Power supply operation from 2.7 to 5.5V

When there is an external Local Oscillator available, the SA601 is the best choice because it has higher overall gain than the SA620. This is because the SA601 mixer has a differential mixer output. The SA620 has the benefit of having a VCO on-chip. With this VCO the LO frequency is generated, so no extra VCO module is required.

Both the SA601 and SA620 come in an SSOP20 and are in full volume production.

3. ETSI I-ETS 300 220 Annex A.1.3.

Double-balanced mixer and oscillator NE/SA602A

DESCRIPTION

The NE/SA602A is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602A make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external LO. For higher frequencies the LO input may be externally driven. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the NE/SA602A a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

FEATURES

- Low current consumption: 2.4mA typical
- Excellent noise figure: <4.7dB typical at 45MHz
- High operating frequency
- Excellent gain, intercept and sensitivity
- Low external parts count; suitable for crystal/ceramic filters
- SA602A meets cellular radio specifications

PIN CONFIGURATION

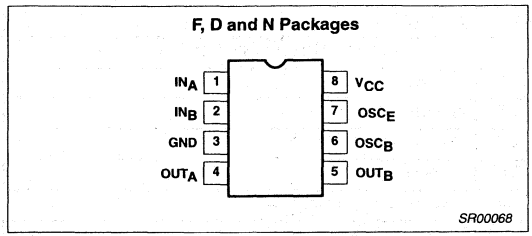


Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio mixer/oscillator
- Portable radio
- VHF transceivers
- RF data links
- HF/VHF frequency conversion
- Instrumentation frequency conversion
- Broadband LANs

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Plastic (DIP)	0 to +70°C	NE602AN	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to +70°C	NE602AD	SOT96-1
8-Pin Ceramic Dual In-Line Package (Cerdip)	0 to +70°C	NE602AFE	0580A
8-Pin Plastic Dual In-Line Plastic (DIP)	-40 to +85°C	SA602AN	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA602AD	SOT96-1
8-Pin Ceramic Dual In-Line Package (Cerdip)	-40 to +85°C	SA602AFE	0580A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE602A	0 to +70	°C
	SA602A	-40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	N package	75	°C/W

BLOCK DIAGRAM

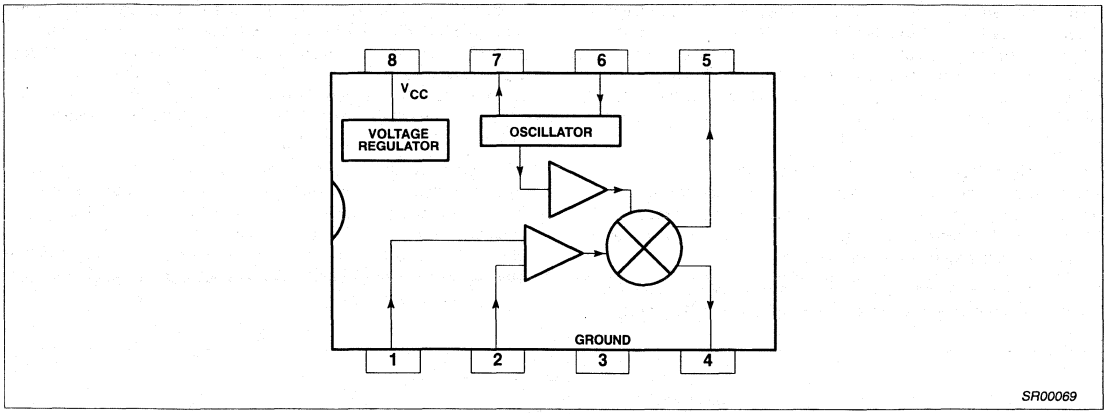


Figure 2. Block Diagram

AC/DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA602A			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figure at 45MHz			5.0	5.5	dB
	Third-order intercept point	RF_{IN} = -45dBm: f_1 = 45.0MHz, f_2 = 45.06MHz		-13	-15	dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The NE/SA602A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA602A is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio second IF and demodulator, the SA602A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -13dBm (that is approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues are not critical, the input to the NE602A should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE/SA602A is designed to be flexible. The input, RF mixer output and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k ll 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 5 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 6 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required LO is beyond oscillation limits, or the system calls for an external LO, the external signal can be injected at Pin 6 through a DC blocking capacitor. External LO should be at least $200mV_{P-P}$.

Figure 7 shows several proven oscillator circuits. Figure 7a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 8 shows a Colpitts varactor tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. A 22kΩ resistor will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

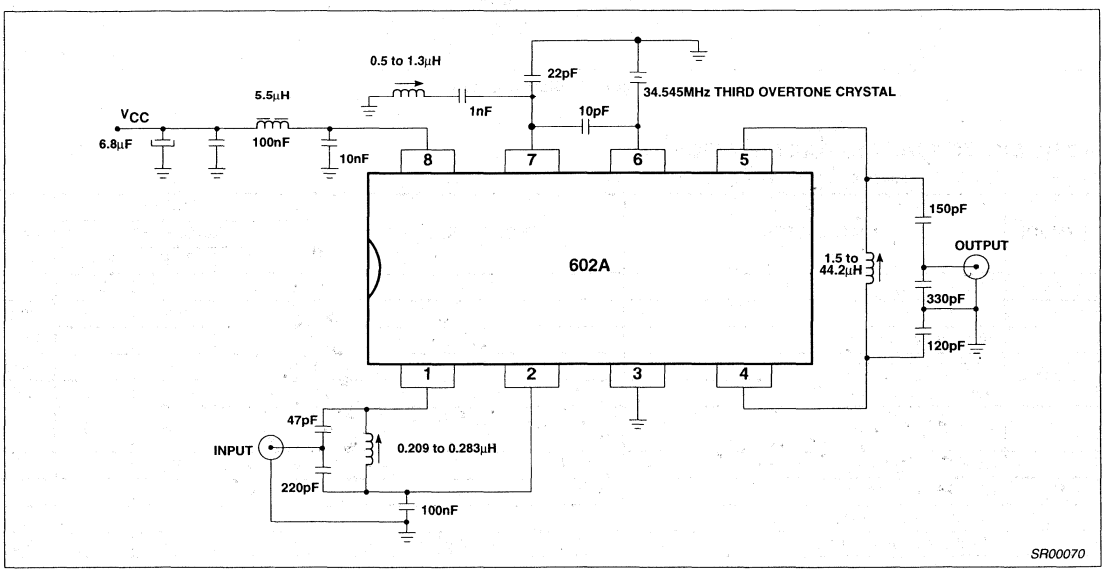


Figure 3. Test Configuration

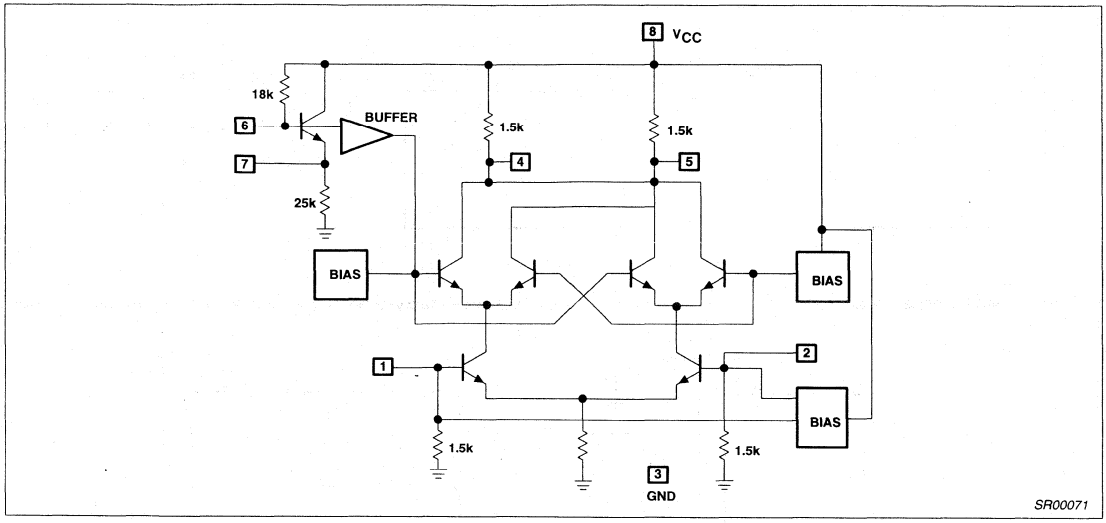
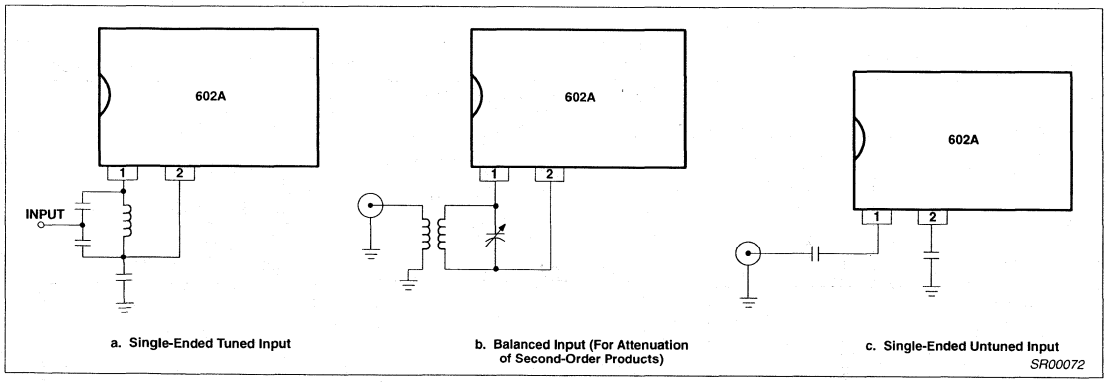


Figure 4. Equivalent Circuit



a. Single-Ended Tuned Input

b. Balanced Input (For Attenuation of Second-Order Products)

c. Single-Ended Untuned Input

Figure 5. Input Configuration

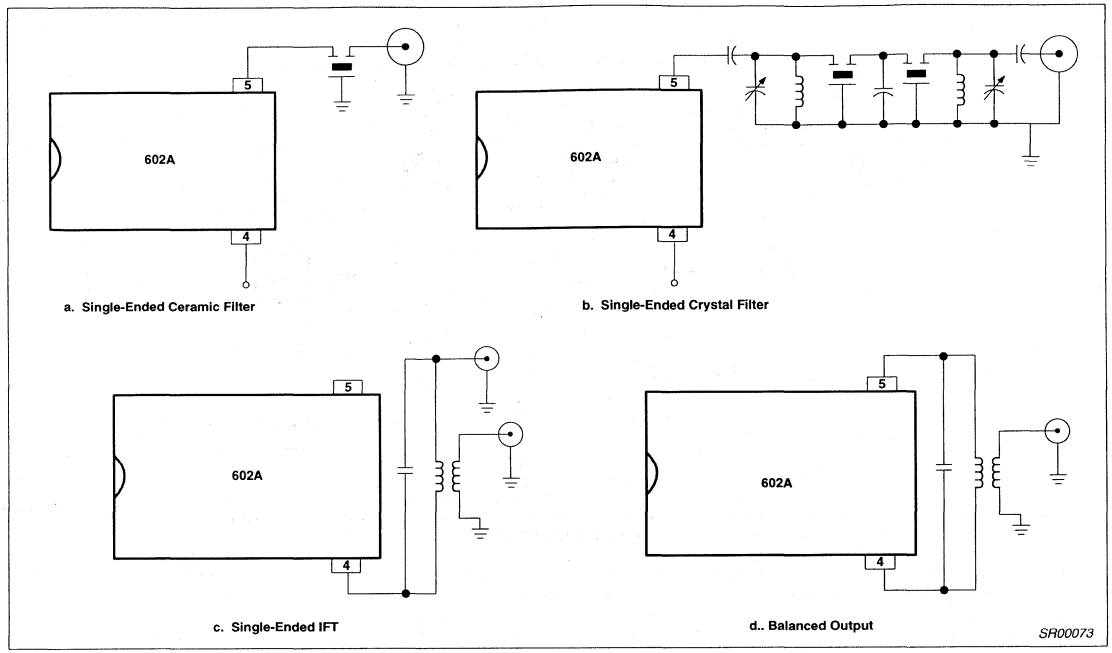


Figure 6. Output Configuration

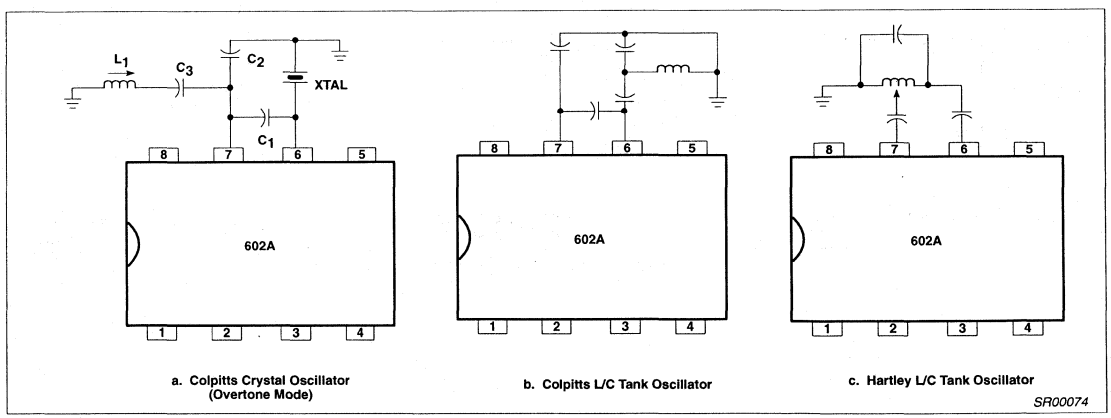


Figure 7. Oscillator Circuits

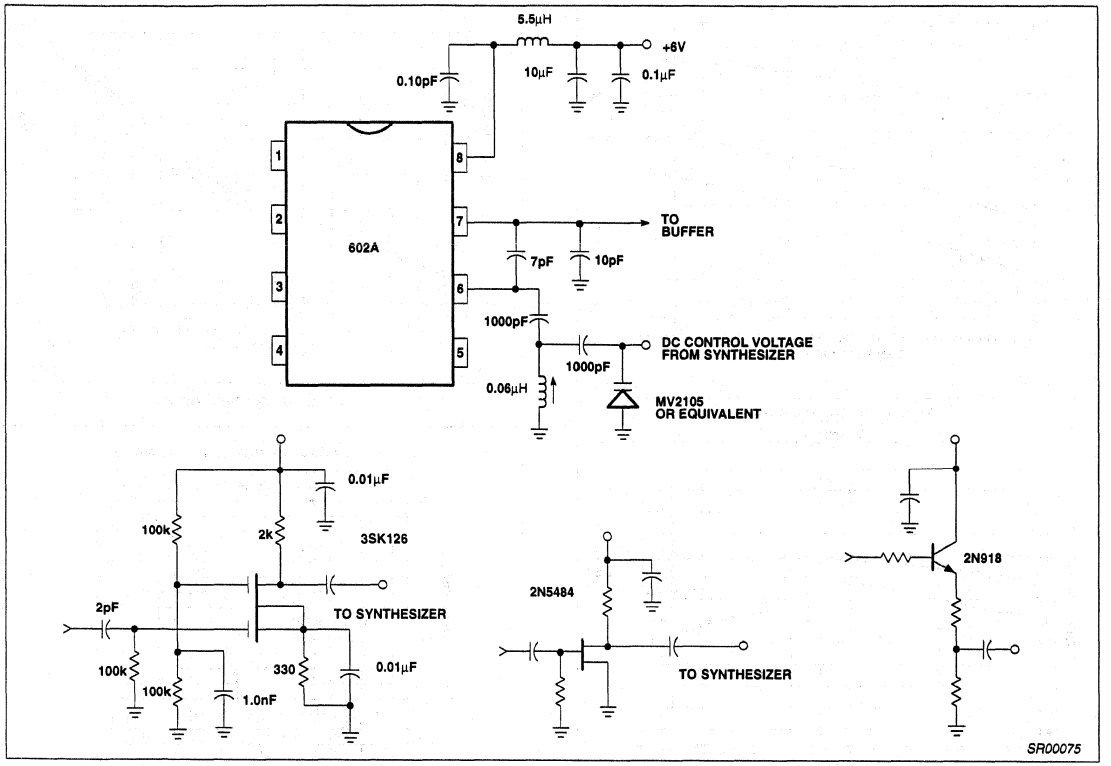


Figure 8. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

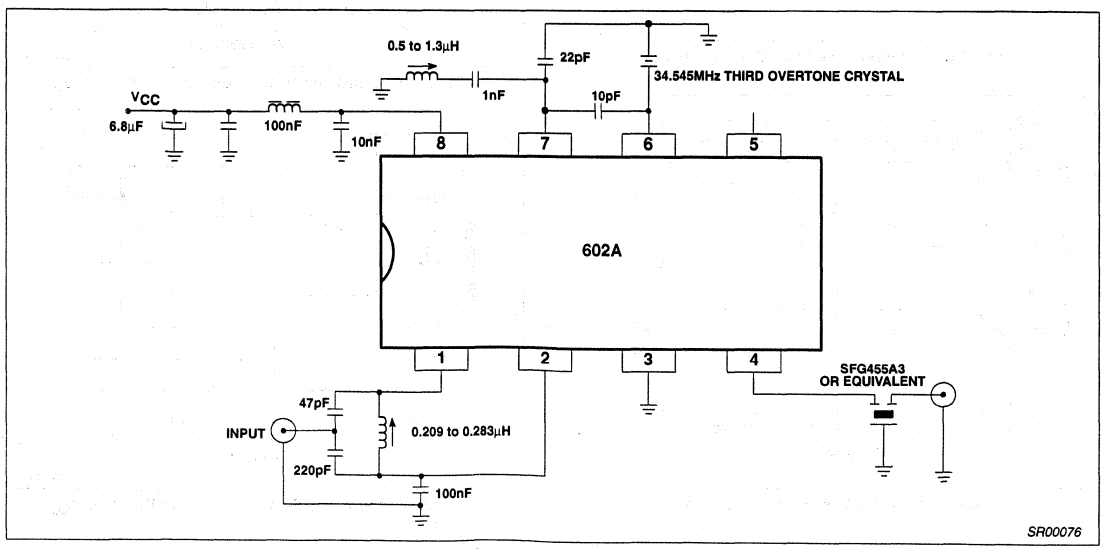


Figure 9. Typical Application for Cellular Radio

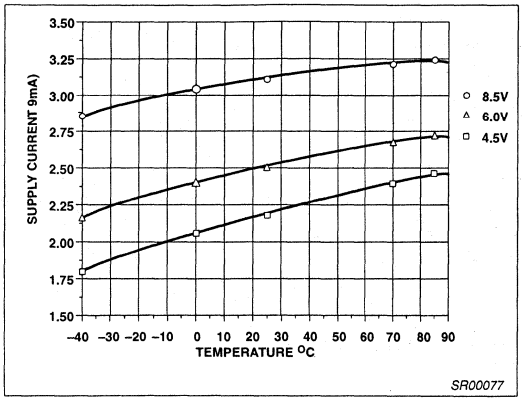


Figure 10. I_{CC} vs Supply Voltage

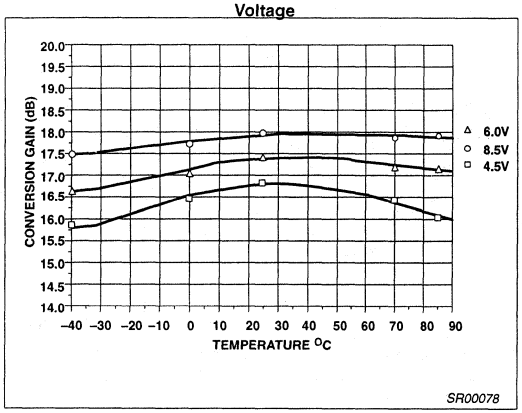


Figure 11. Conversion Gain vs Supply Voltage

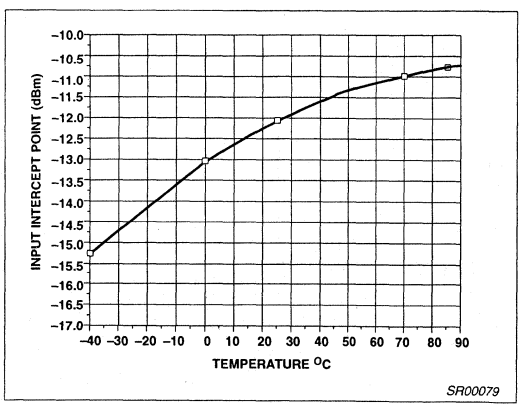


Figure 12. Third-Order Intercept Point

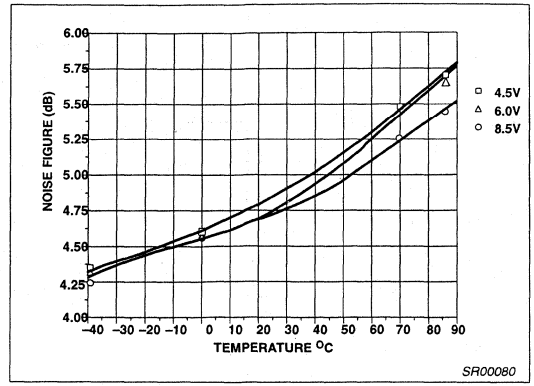


Figure 13. Noise Figure

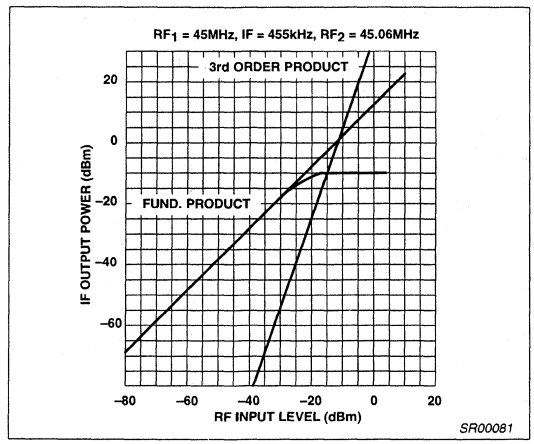


Figure 14. Third-Order Intercept and Compression

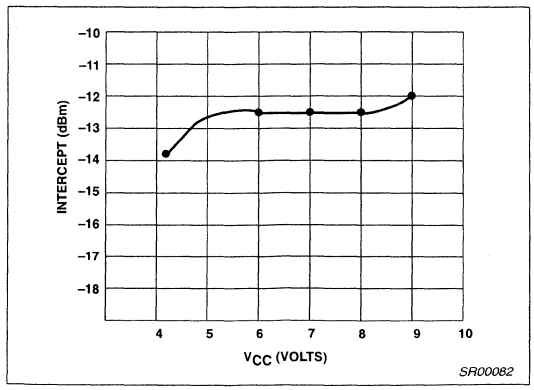


Figure 15. Input Third-Order Intermod Point vs V_{CC}

Double-balanced mixer and oscillator NE/SA612A

DESCRIPTION

The NE/SA612A is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 45MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 45MHz is typically below 6dB and makes the device well suited for high performance cordless phone/cellular radio. The low power consumption makes the NE/SA612A excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE/SA612A is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

FEATURES

- Low current consumption
- Low cost
- Operation to 500MHz
- Low radiated energy
- Low external parts count; suitable for crystal/ceramic filter
- Excellent sensitivity, gain, and noise figure

PIN CONFIGURATION

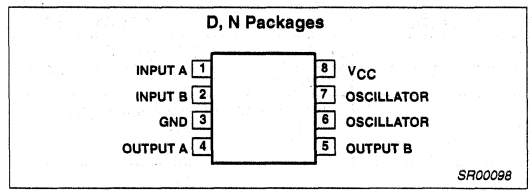


Figure 1. Pin Configuration

APPLICATIONS

- Cordless telephone
- Portable radio
- VHF transceivers
- RF data links
- Sonabuoys
- Communications receivers
- Broadband LANs
- HF and VHF frequency conversion
- Cellular radio mixer/oscillator

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Plastic (DIP)	0 to +70°C	NE612AN	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-Mount)	0 to +70°C	NE612AD	SOT96-1
8-Pin Plastic Dual In-Line Plastic (DIP)	-40 to +85°C	SA612AN	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-Mount)	-40 to +85°C	SA612AD	SOT96-1

BLOCK DIAGRAM

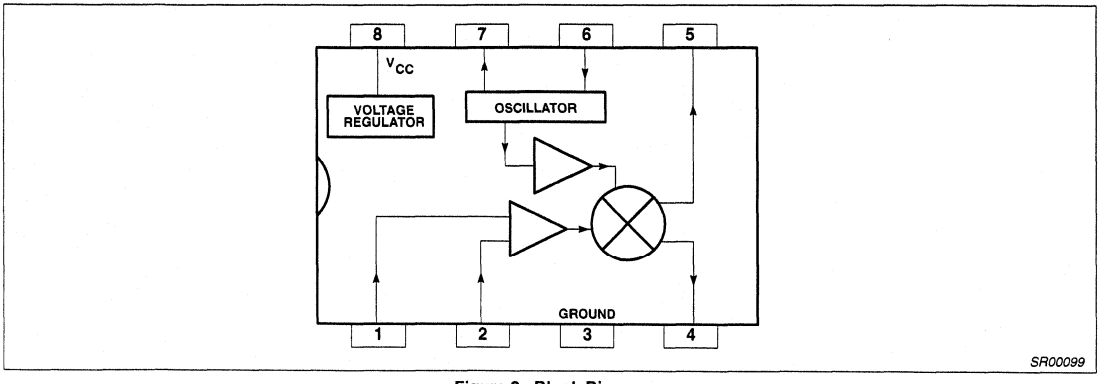


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Operating ambient temperature range NE SA	 0 to +70 -40 to +85	°C

AC/DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC} = 6V, Figure 3

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	3.0	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0		dB
	Third-order intercept point at 45MHz	RF_{IN}=-45dBm		-13		dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The NE/SA612A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA612A is designed for optimum low power performance. When used with the NE614A as a 45MHz cordless phone/cellular radio 2nd IF and demodulator, the NE/SA612A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE/SA612A should be appropriately scaled.

TEST CONFIGURATION

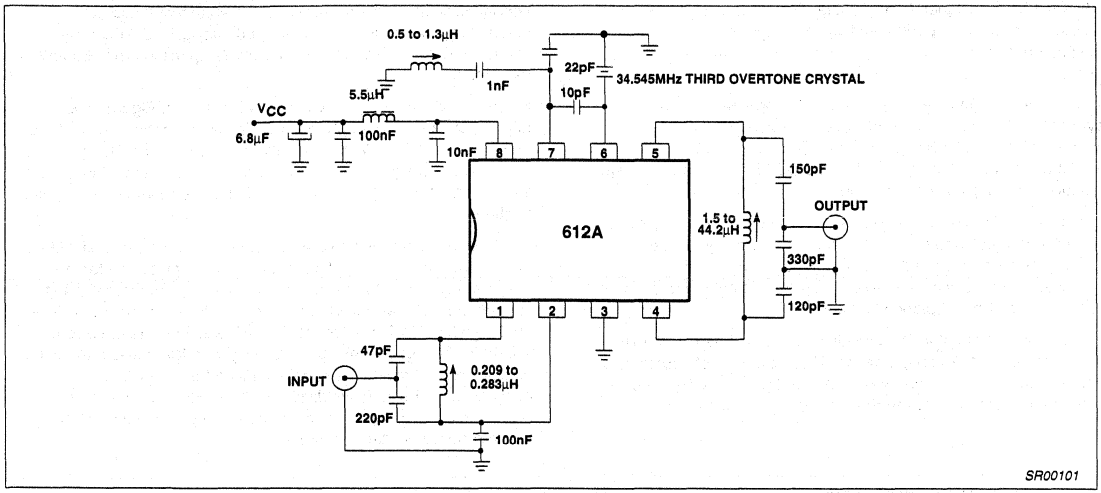


Figure 3. Test Configuration

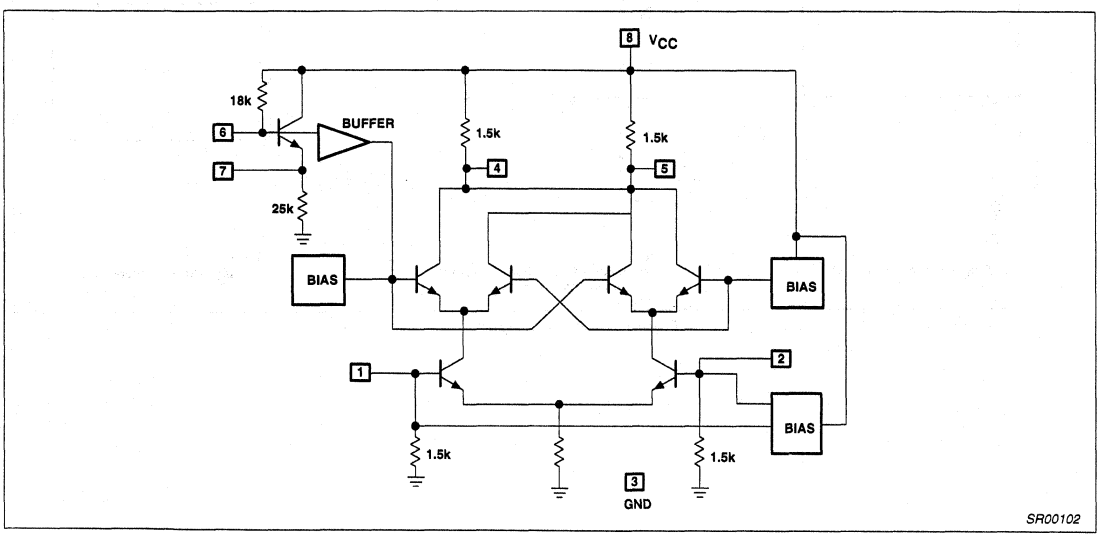


Figure 4. Equivalent Circuit

Besides excellent low power performance well into VHF, the NE/SA612A is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k ll 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 5 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 6 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be $200mV_{P-P}$ minimum to $300mV_{P-P}$ maximum.

Figure 7 shows several proven oscillator circuits. Figure 7a is appropriate for cordless phones/cellular radio. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 8 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

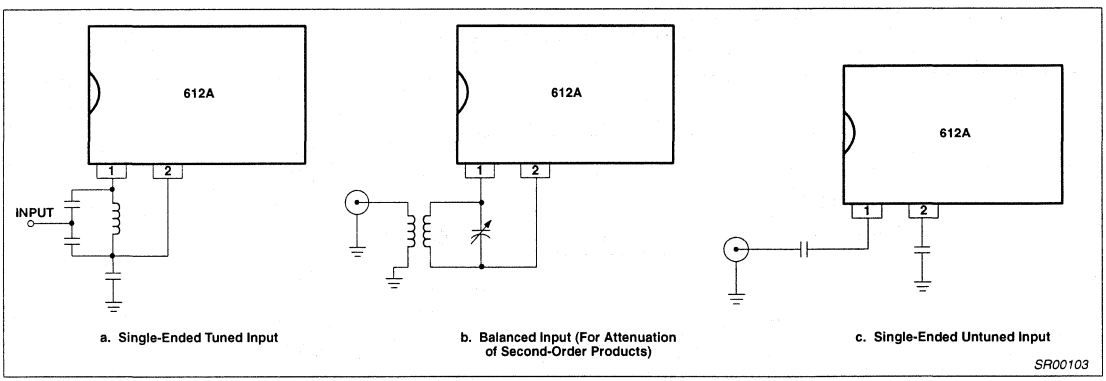


Figure 5. Input Configuration

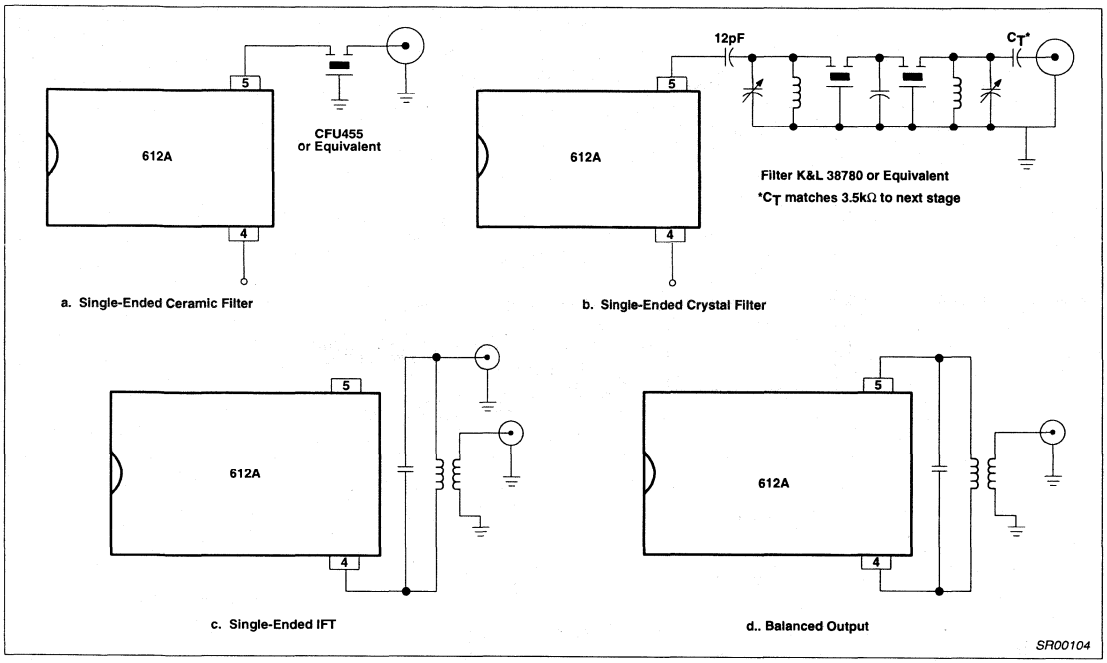


Figure 6. Output Configuration

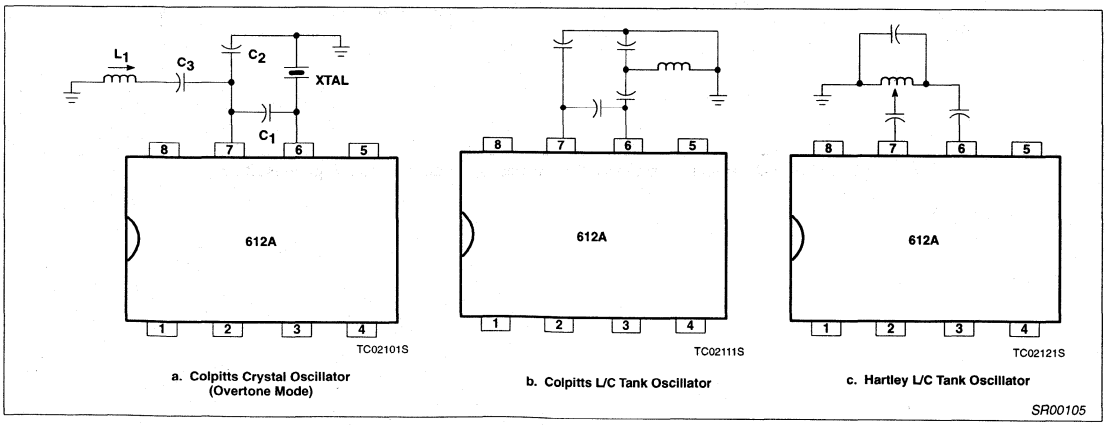


Figure 7. Oscillator Circuits

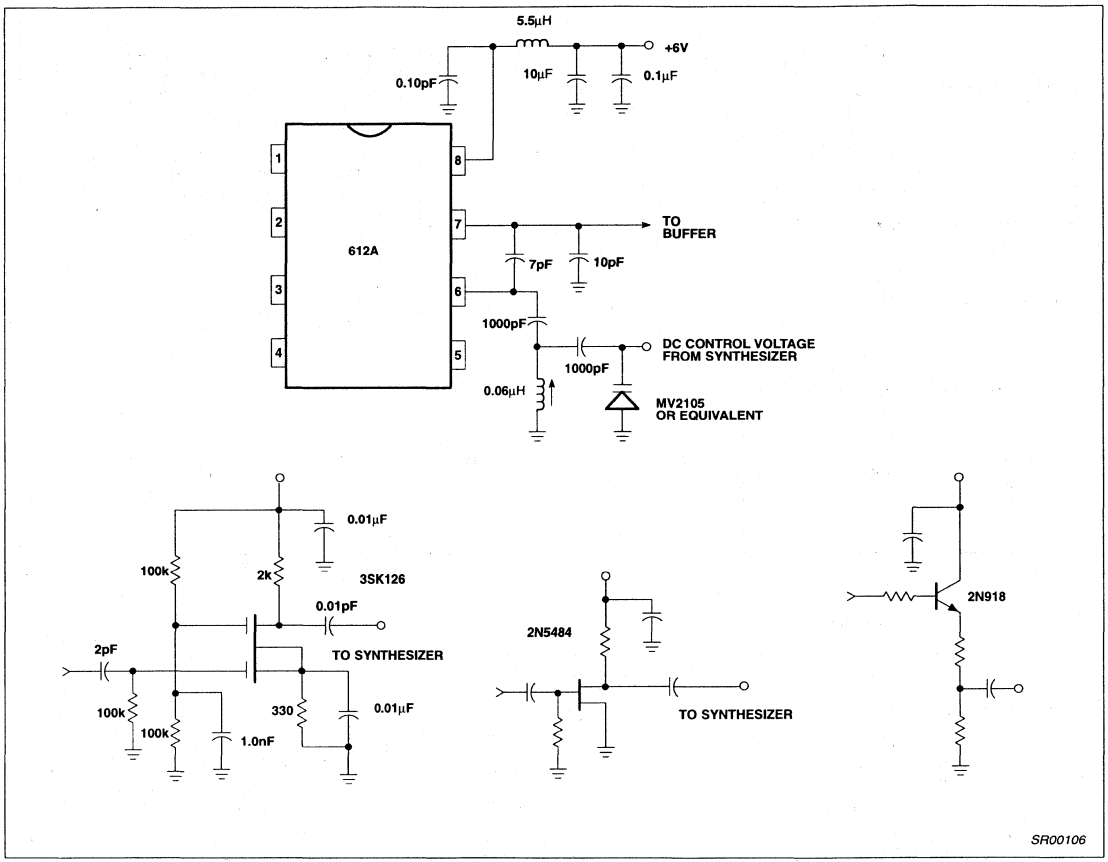


Figure 8. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

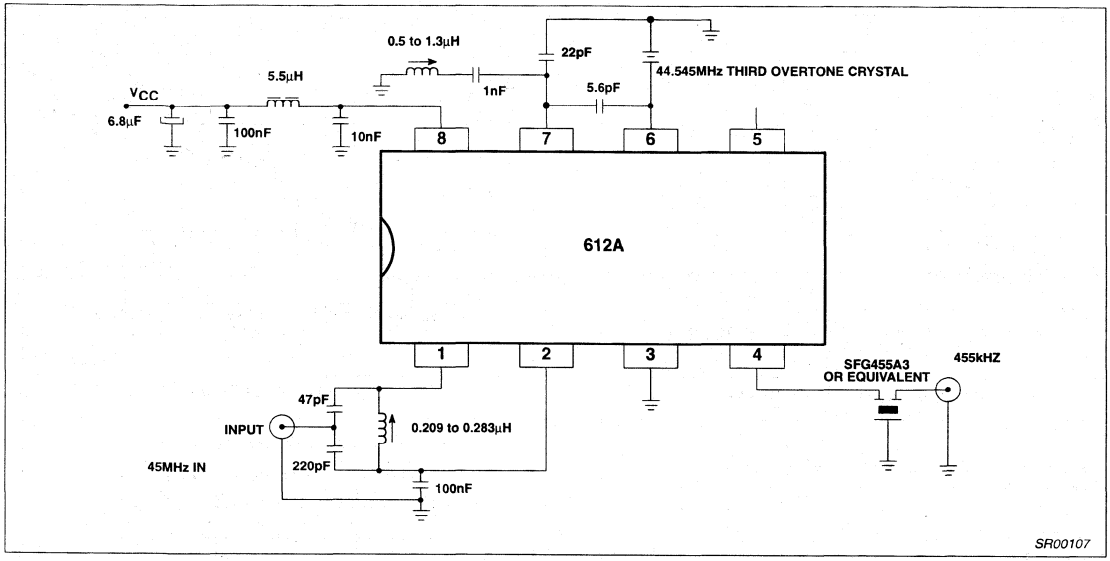


Figure 9. Typical Application for Cordless/Cellular Radio

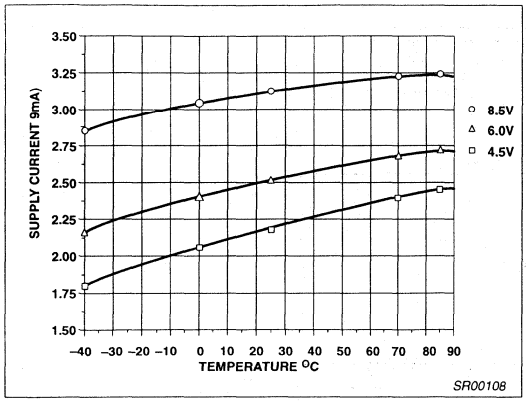


Figure 10. I_{CC} vs Supply Voltage

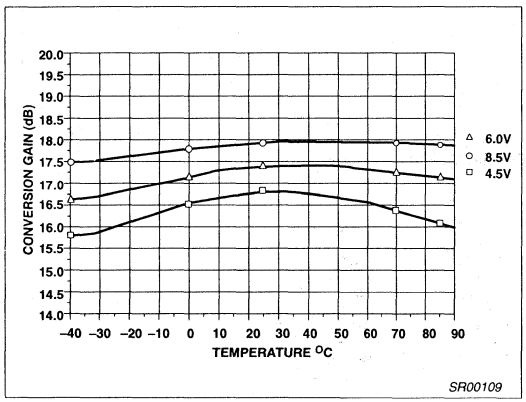


Figure 11. Conversion Gain vs Supply Voltage

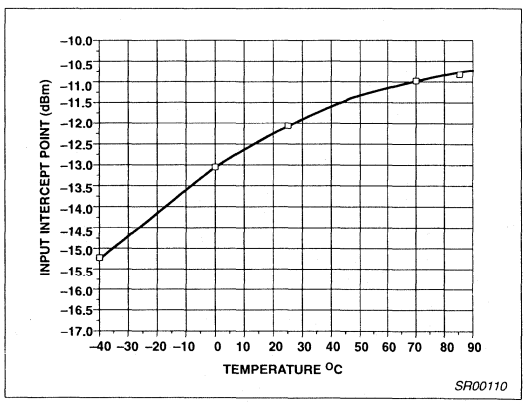


Figure 12. Third-Order Intercept Point

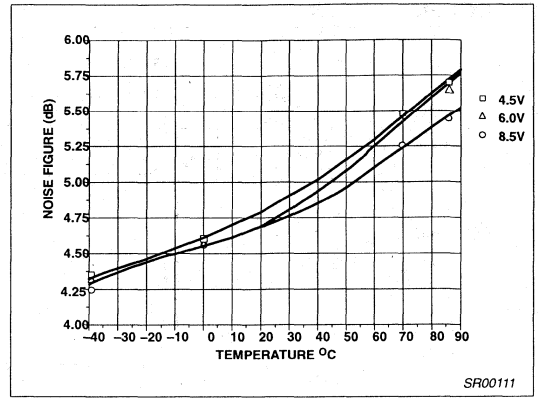


Figure 13. Noise Figure

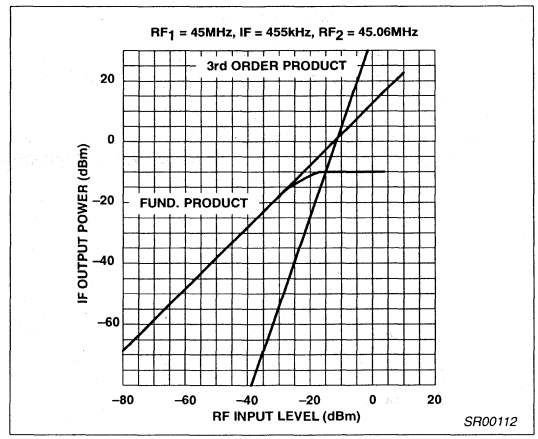


Figure 14. Third-Order Intercept and Compression

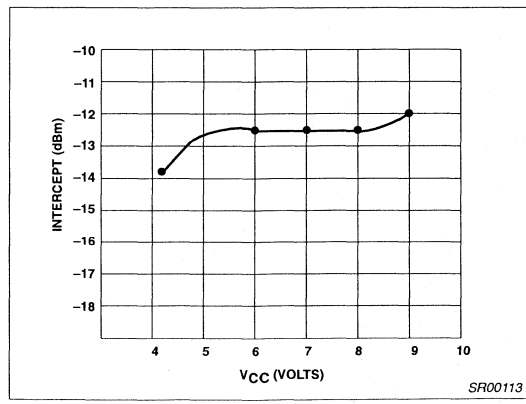


Figure 15. Input Third-Order Intermod Point vs V_{CC}

New low-power single sideband circuits AN1981

Author: Robert J. Zavrell Jr.

INTRODUCTION

Several new integrated circuits now permit RF designers to resurrect old techniques of single-sideband generation and detection. The high cost of multi-pole crystal filters limits the use of the SSB mode to the most demanding applications, yet the advantages of SSB over full-carrier AM and FM are well documented (Ref 1 &2). The use of multi-pole filters can now be circumvented by reviving some older techniques without sacrificing performance. This has been made possible by the availability of some new RF and digital integrated circuits.

DESCRIPTION

Figure 1 shows the frequency spectrum of a 10MHz full-carrier double-sideband AM signal using a 1kHz modulating tone. This well-known type of signal is used by standard AM broadcast radio stations. Full-carrier AM's advantage is that envelope detection can be used in the receiver. Envelope detection is a simple and economical technique because it simplifies receiver circuitry. Figure 2 shows the time domain "envelope" of the same AM signal.

The 1kHz tone example of Figures 1 and 2 serves as a simple illustration of an AM signal. Typically, the sidebands contain complex waveforms for voice or data communications. In the full-carrier double sideband mode (AM), all the modulation information is contained in both sidebands, while the carrier "rides along" without contributing to the transfer of intelligence. Only one sideband without the carrier is needed to effectively transmit the modulation information. This mode is called "single-sideband suppressed carrier". Because of its reduced bandwidth, it has the advantages of improved spectrum utilization, better signal-to-noise ratios at low signal levels, and improved transmitter efficiency when compared with either FM or full-carrier AM. A finite frequency allocation using SSB can support three times the number of channels when compared with comparable FM or AM full-carrier systems.

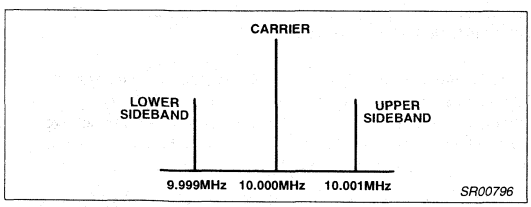


Figure 1. Frequency Domain Display of a 10MHz Carrier AM Modulated by a 1kHz Tone (Spectrum Analyzer Display)

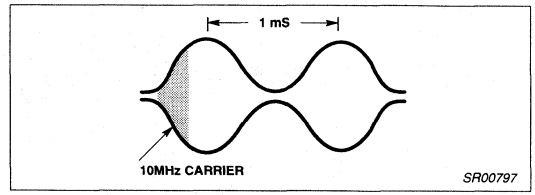


Figure 2. Time Domain Display of the Same Signal Shown in Figure 1. (Oscilloscope Display)

There are three basic methods of single-sideband generation. All three use a balanced modulator to produce a double-sideband suppressed carrier signal. The undesired sideband is then removed by phase and amplitude nulling (the phasing method), high Q multi-pole filters (the filter method), or a "third" method which is a derivation of the phasing technique called here the "Weaver" method for the apparent inventor. The reciprocal of the generator functions is employed to produce sideband detectors. Generators start with audio and produce the SSB signal; detectors receive the SSB signal and reproduce the audio. Since the sideband signal is typically produced at radio frequencies, it can be amplified and applied to an antenna or used as a subcarrier.

Reproduction of the audio signal in a full-carrier AM receiver is simplified because the carrier is present. The signal envelope, which contains the carrier and the sidebands, is applied to a non-linear device (typically a diode). The effect of envelope detection is to multiply the sideband signal by the carrier; this results in the recovery of the audio waveform. The mathematical basis for this process can be understood by studying trigonometric identities.

Since the carrier is not present in the received SSB signal, the receiver must provide it for proper audio detection. This signal from the local oscillator (LO) is applied to a mixer (multiplier) together with the SSB signal and detection occurs. This technique is called product detection and is necessary in all SSB methods. A major problem in SSB receivers is the ability to maintain accurate LO frequencies to prevent spectral shifting of the audio signal. Errors in this frequency will result in a "Donald Duck" sound which can render the signal unintelligible for large frequency errors.

Theory of Single-Sideband Detection

Figures 3 through 8 illustrate the three methods of SSB generation and detection. Since they are reciprocal operations, the circuitry for generation and detection is similar with all three methods. Duplication of critical circuitry is easy to accomplish in transceiver applications by using appropriate switching circuits.

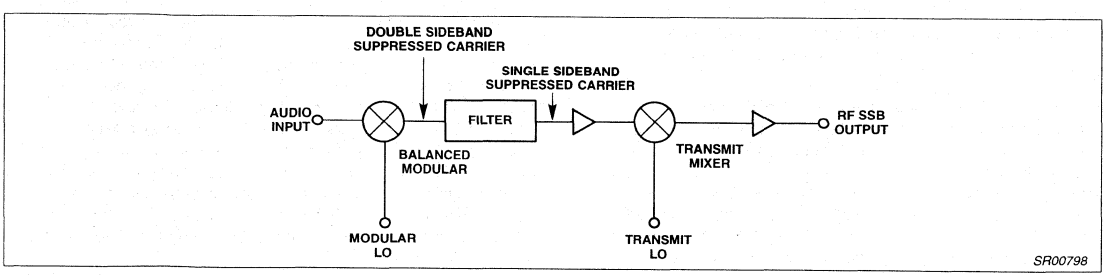


Figure 3. Filter Method SSB Generator

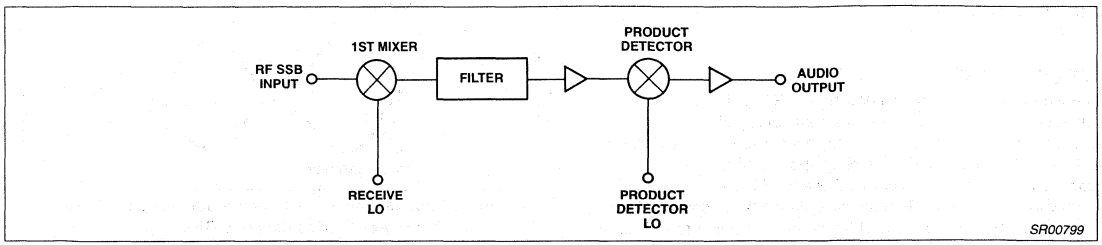


Figure 4. Filter Method SSB Detector

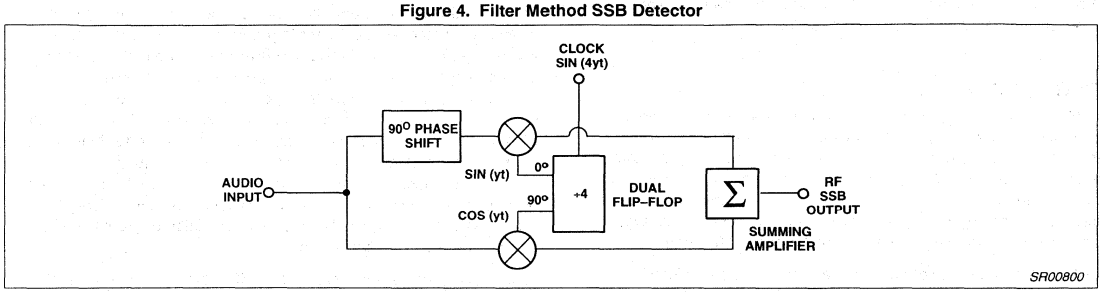


Figure 5. Phasing Method Generator

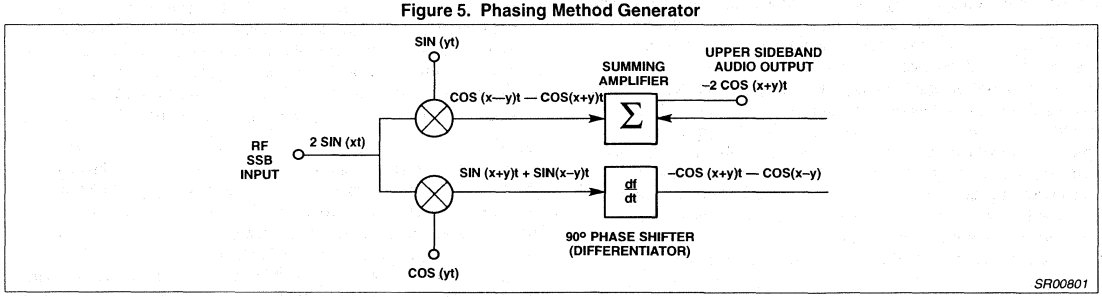


Figure 6. Phasing Method Detector with Simplified Mathematical Model

Figures 3 and 4 show the generation and detection techniques employed in the filter method. In the generator a double sideband signal is produced while the carrier is eliminated with the balanced modulator. Then the undesired sideband is removed with a high Q crystal bandpass filter. A transmit mixer is usually employed to convert the SSB signal to the desired output frequency. The detection scheme is the reciprocal. A receive mixer is used to convert the selected input frequency to the IF frequency, where the filter removes the undesired SSB response. Then the signal is demodulated in the product detector. A major drawback to the filter method is the fact that the filter is fixed-tuned to one frequency. This necessitates the receive and transmit mixers for multi-frequency operation.

Figures 5 and 6 show block diagrams of a generator and demodulator which use the phase method. Figure 6 also includes a mathematical model. The input signal (Cos(Xt)) is fed in-phase to two RF mixers where "X" is the frequency of the input signal. The other inputs to the mixers are fed from a local oscillator (LO) in quadrature (Cos(Yt) and Sin(Yt)), where "Y" is the frequency of the LO signal. By differentiating the output of one of the mixers and then summing with the other, a single sideband response is obtained. Switching the mixer output that is differentiated will change the selected sideband, upper (USB) or lower (LSB). In most cases the mixer outputs will be the audio passband (300 to 3000Hz). Differentiating the passband involves a 90 degree phase shift over more than three octaves. This is the most difficult aspect of using the phasing method for voice band SSB.

For voice systems, difficulty of maintaining accurate broadband phase shift is eliminated by the technique used in Figures 7 and 8. The "Weaver" method is similar to the phasing method because both require two quadrature steps in the signal chain. The difference between the two methods is that the Weaver method uses a low frequency (1.8kHz) subcarrier in quadrature rather than the broad-band 90 degree audio phase shift. The desired sideband is thus "folded over" the 1.8kHz subcarrier and its energy appears between 0 and 1.5kHz. The undesired sideband appears 600Hz farther away between 2.1 and 4.8kHz. Consequently, sideband rejection is determined by a low-pass filter rather than by phase and amplitude balance. A very steep low-pass response in the Weaver method is easier to achieve than the very accurate phase and amplitude balance needed in the phasing method. Therefore, better sideband rejection is possible with the Weaver method than with the phasing method.

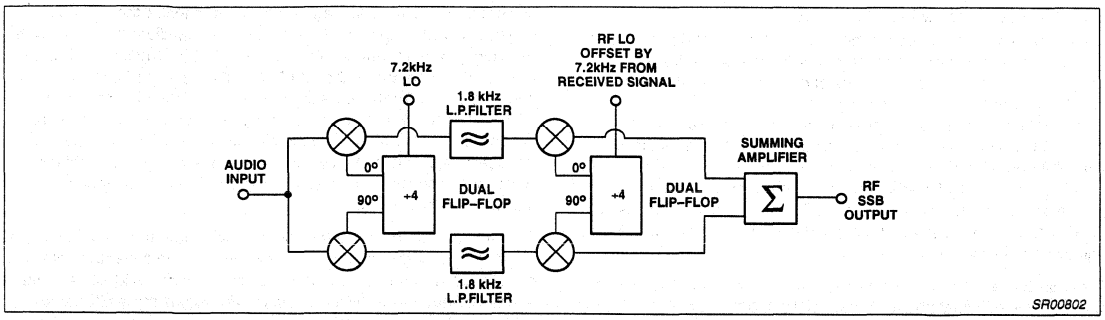


Figure 7. Weaver Method Generator

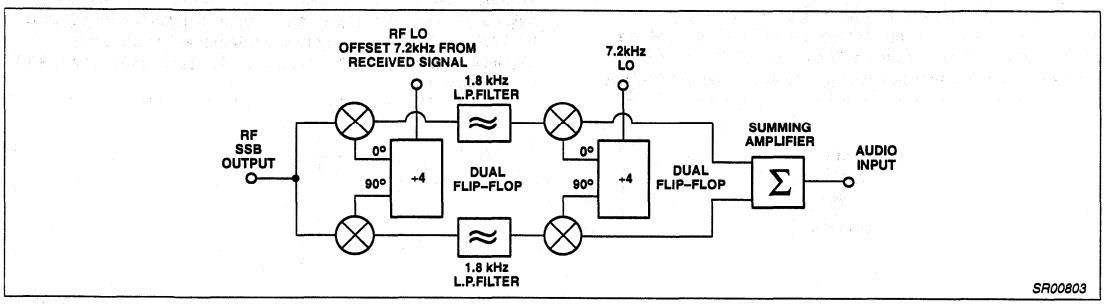


Figure 8. Weaver Method Detector

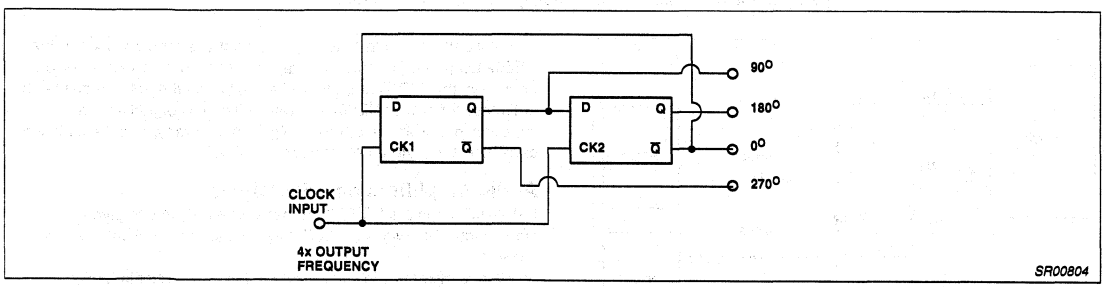


Figure 9. Dual Flip-Flop Quadrature Synthesis

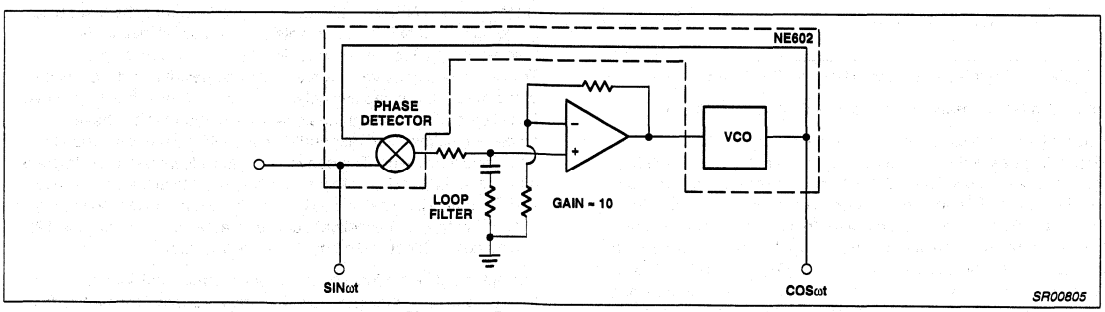


Figure 10. PLL Quadrature Synthesis

Quadrature Dual Mixer Circuits

One of the two critical stages in the phasing method and both critical stages in the Weaver method require quadrature dual mixer circuits. Figures 9 and 10 show two methods of obtaining quadrature LO signals for dual mixer applications. Other methods exist for producing quadrature LO signals, particularly use of passive LC circuits. LC circuits will not maintain a quadrature phase relationship when the operating frequency is changed. The two illustrated circuits are inherently broad-banded; therefore, they are far more flexible and do not require adjustment. These circuits are very useful for SSB circuits, but also can be applied to FSK, PSK, and QPSK digital communications systems.

The NE602 is a low power, sensitive, active, double-balanced mixer which shows excellent phase characteristics up to 200MHz. This makes it an ideal candidate for this and many other applications.

The circuit in Figure 9 uses a divide-by-four dual flip-flop that generates all four quadratures. Most of the popular dual flip-flops can be used in different situations. The HEF4013 CMOS device uses very little power and can maintain excellent phase integrity at clock rates up to several megahertz. Consequently, the HEF4013 can be used with the ubiquitous 455kHz intermediate frequency with excellent power economy. For higher clock rates (up to 120MHz for up to 30MHz operation), the fast TTL 74F74 is a good choice. It has been tested to 30MHz operating frequencies with good results (>30 dB SSB rejection). At lower frequencies (5MHz) sideband rejection increases to nearly 40dB with the circuits shown. The ultimate low frequency rejection is mainly a function of the audio phase shifter. Better performance is possible by employing higher tolerance resistors and capacitors.

The circuit in Figure 10 shows another technique for producing a broadband quadrature phase shift for the LO. The advantage of this circuit over the flip-flops is that the clock frequency is identical to the operating frequency; however, phase accuracy is more difficult to achieve. A PLL will maintain a quadrature phase relationship when the loop is closed and the VCO voltage is zero. The DC amplifier will help the accuracy of the quadrature condition by presenting gain to the VCO control circuit. The other problem that can arise is that PLL circuits tend to be noisy. Sideband noise is troublesome in both SSB and FM systems,

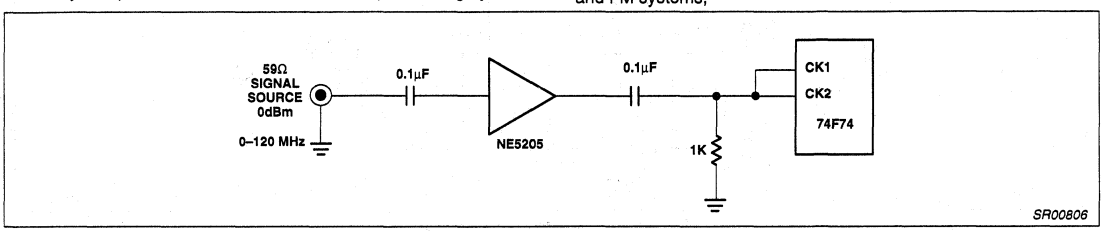


Figure 11. FAST TTL Driver from Analog Signal Source Using NE5205

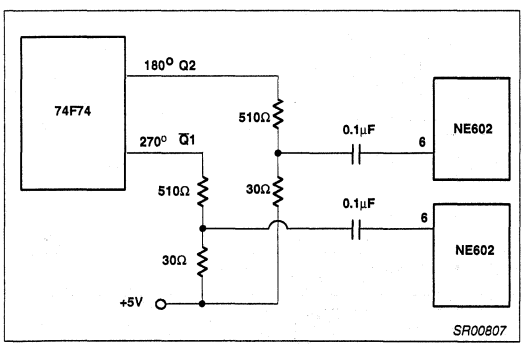


Figure 12. Interface Circuitry Between 74F74 and the NE602s

but SSB is less sensitive to phase noise problems in the LO.

Figure 11 shows a circuit that is effective for driving the 74F74, or other TTL gates, with a signal generator or analog LO. The NE5205 provides about 20dB gain with 50Ω input and output impedances from DC to 450MHz. Minimum external components are required. The 1kΩ resistor is about optimum for "pulling" the input voltage down near the logic threshold. A 50Ω output level of 0dBm can be used to drive the NE5205 and 74F74 to 100MHz. Two NE5205s can be cascaded for even more sensitivity while maintaining extremely wide bandwidth. An advantage of using digital sources for the LO is that low-frequency power supply ripple will not cause hum in the receiver front end. This is a common problem in direct conversion designs.

Figure 12 shows the interface circuitry between the 74F74 and the NE602 LO ports. The total resistance reflects conservative current drain from the 74F74 outputs, while the tap on the voltage divider is optimized for proper NE602 operation. The low signal source impedance further helps maintain phase accuracy, and the isolation capacitor is miniature ceramic for DC isolation.

Audio Amplifiers and Switching

Using active mixers (NE602) in these types of circuits gives conversion gain, typically 18dB. More traditional applications use passive
diode ring mixers which yield conversion loss, typically 7dB. Consequently, the detected audio level will be about 25dB higher when using the NE602. This fact can greatly reduce the first audio stage noise and gain requirements and virtually eliminate the "microphonic" effect common to direct conversion receivers. Traditional direct conversion receivers use passive audio LC filters at the mixer output and low noise, discrete JFETs or bipolars in the first stages. The very high audio sensitivity required by these amplifiers makes them respond to mechanical vibration – thus the "microphonics" result. The conversion gain allows use of a simple op amp stage (Figure 13) set up as an integrator to eliminate ultra-sonic and RF instability. The NE5534 is well known for its low noise, high dynamic range, and excellent audio characteristics (Reference 12) and makes an ideal audio amp for the 602 detector.

The sideband select function is easily accomplished with an HEF4053 CMOS analog switch. This triple double-pole switch drives the phase network discussed in the next section and also chooses one of two amplitude balance potentiometers, one for each sideband. Figure 14 illustrates this circuit. A buffer op amp is used

with the two sideband select sections to reduce THD, maintain amplitude integrity, and not change the filter network input resistance values. The gain distribution within both legs of the receiver was found to be very consistent (within 1dB), thus the amplitude balance pots may be eliminated in less demanding applications. The NE602s have excellent gain as well as phase integrity.

Audio Phase Shift Circuits

The two critical stages for the phasing method are a dual quadrature mixer and a broadband audio phase shifter (differentiator). There are several broadband, phase shift techniques available. Figure 15 shows an analog all-pass differential phase shift circuit. When the inputs are shorted and driven with a microphone circuit, the outputs will be 90 degrees out-of-phase over the 300 to 3000Hz band. This "splitting" and phase shift is necessary for the phasing generator. For phasing demodulation the two audio detectors are fed to the two inputs. The outputs are then summed to affect the sideband rejection and audio output.

Standard 1% values are shown for the resistors and capacitors, although better gain tolerances can be obtained with 0.1% laser-trimmed integrated resistors. Polystyrene capacitors are preferred for better value tolerance and audio performance. Two quad op amps fit nicely into this application. One op amp serves as a switch buffer and the other three form a phasing section. The NE5514 quad op amps perform well for this application. Careful attention to active filter configurations can yield highly linear and very high dynamic range circuits. Yet these characteristics are much easier to achieve at audio than the common IF RF frequencies. This fact, coupled with the lack of IF tuned circuits, shielding, and higher power requirements make audio IF systems attractive indeed.

Figure 16 shows a "tapped" analog delay circuit which uses weighted values of resistors to affect the phase shift. Excellent phase and amplitude balance are possible with this technique, but the price for components is high. It should be stressed that the audio phase shift accuracy and amplitude balance are the limiting factors for SSB rejection when using the phase method; thus the higher cost may be justified in some applications.

Audio Processing

The summing amplifier is a conventional, inverting op amp circuit. It may be useful to configure a low-pass filter around this amplifier, and thus help the sharp audio filters which follow. Audio filters are necessary to shape the desired bandpass. Steep slope audio bandpass filters can be built from switched capacitor filters or from active filters

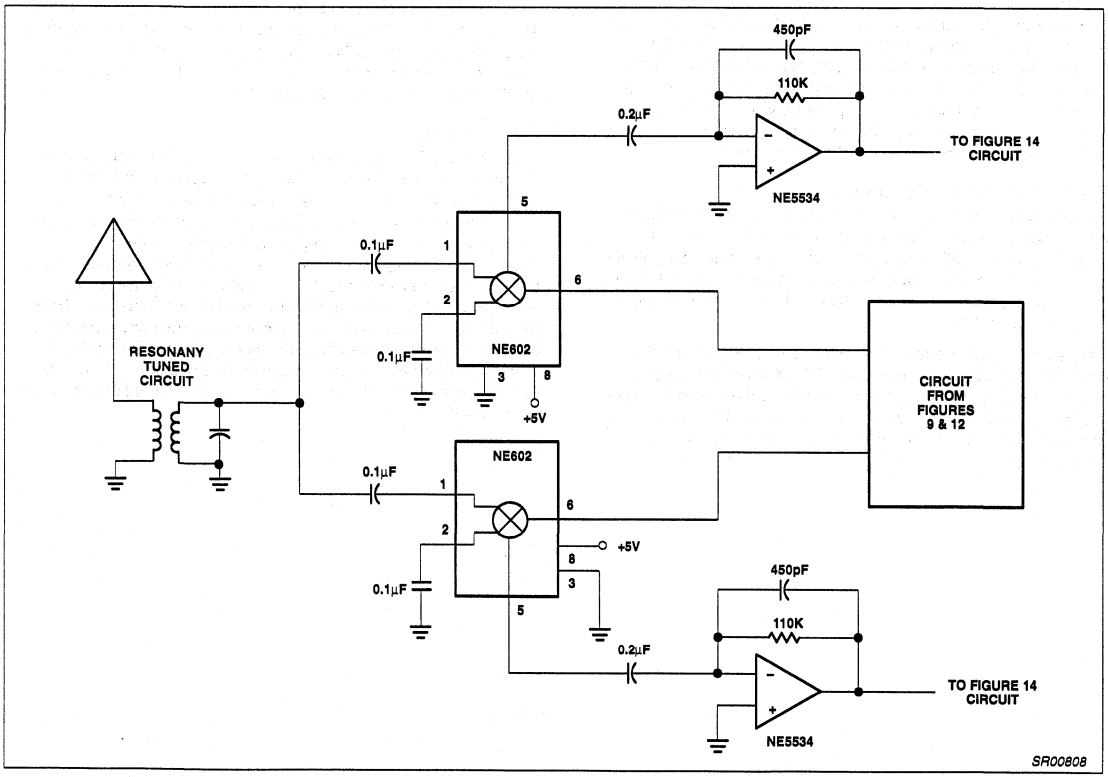


Figure 13. Phasing Method Detector for Direct Conversion Receiver

requiring more op amps. Switched capacitor filters have the disadvantage of requiring a clock frequency in the RF range. Harmonics can cause interference problems if careful design techniques are not used. Also, better dynamic range is obtained with

active filter techniques using "real" resistors although much work is being done with SCF's and performance is improving.

Direct conversion receivers rely heavily on audio filters for selectivity. Active analog or switched capacitor filters can produce the high Q and dynamic ranges necessary. Signal strength or "S-meters" can be constructed from the NE602's companion part, the NE604. The "RSSI" or "received signal strength indicator" function on the 604 provides a logarithmic response over a 90dB dynamic range and is easy to use at audio frequencies. Finally, the AGC (automatic gain control) function can also be performed in the audio section. Attack and delay times can be independently set with excellent distortion specifications with the NE572 compandor IC. The audio-derived AGC eliminates the need for gain controlling and RF stage, but relies on an excellent receiver front-end dynamic range. In ACSSB (Amplitude Compandored Single-Side Band) systems transmitter compression and receiver expansion are defined by individual system specifications.

Phasing-Filter Technique

High quality SSB radio specifications call for greater than 70dB sideband rejection. Using the circuits described in this paper for the phasing method, rejection levels of 35dB are obtainable with good reliability. Coupled with an inexpensive two-pole crystal or ceramic filter, the 70dB requirement is obtained. Also, the filtering ahead of the NE602 greatly improves the intermodulation performance of the receiver. Figure 17 shows a complete SSB receiver using the Phasing-Filter technique. The sensitivity of the NE602 allows low gain stages and low power consumption for the RF amplifier and first mixer. A new generation of low power CMOS frequency synthesizers is now available from several manufacturers including the TDD1742 and dual chip HEF4750/51 solutions.

Direct Conversion Receiver

The antenna can be connected directly to the input of the NE602 (via a bandpass filter) to form a direct conversion SSB receiver using the phasing method. 35dB sideband rejection is adequate for many applications, particularly where low power and portable battery operation are required. Figure 13 shows a typical circuit for direct conversion applications.

There are many other applications which can make use of SSB technology. Cordless telephones use FM almost exclusively. Eavesdropping could be greatly reduced for systems which employ SSB rather than FM. Furthermore, the better signal-to-noise ratio will extend the range, and battery life will be extended because no carrier is needed.

SSB is also used for subcarriers on microwave links and coaxial lines. Telephone communications networks that use SSB are called FDM or Frequency Domain Multiplex systems. The low power and high sensitivity of the NE602 can offer FDM designers new techniques for system configuration.

Weaver Method Receiver Techniques

The same quadrature dual mixer can be used for the first stage in both the phasing and Weaver method receiver. The subcarrier stage in the Weaver method receiver can use CMOS analog switches (HEF4066) for great power economy. Figure 18 shows a circuit for the subcarrier stage. A 1.8kHz subcarrier requires a 7.2kHz clock frequency. If switched capacitor filters are used for the low-pass and audio filters, a single clock generator can be used for all circuits with appropriate dividers. Furthermore, if the receiver is used as an IF circuit, the fixed LO signal could also be derived from the same clock. This has the added advantage that harmonics from the various circuits will not interfere with the received signal.

Results

The circuit shown in Figures 13, 14, and 15 has a 10dB S/N sensitivity of 0.5μV with a dynamic range of about 80dB. Single-tone audio harmonic distortion is below 0.05% with two-tone intermodulation products below 55dB at RF input levels only 5dB below the 1dB compression point. The sideband rejection is about 38dB at a 9MHz operating frequency. The good audio specifications are a side benefit to direct conversion receivers. When used with inexpensive ceramic or crystal filters, this circuit can provide these specifications with >70dB sideband rejection.

Conclusions

Single sideband offers many advantages over FM and full-carrier double-sideband modulation. These advantages include: more efficient spectrum use, better signal-to-noise ratios at low signal levels, and better transmitter efficiency. Many of the disadvantages can now be overcome by using old techniques and new state-of-the-art integrated circuits. Effective and inexpensive circuits can use direct conversion techniques with good results. 35dB sideband rejection with less than 1μV sensitivity is obtained with the NE602 circuits. 70dB sideband rejection and superior sensitivity are obtained by using phasing-filter techniques. Either the phasing or Weaver methods can be used in either the direct conversion or IF section applications. The filter and phase-filter methods can be used in only the IF application.

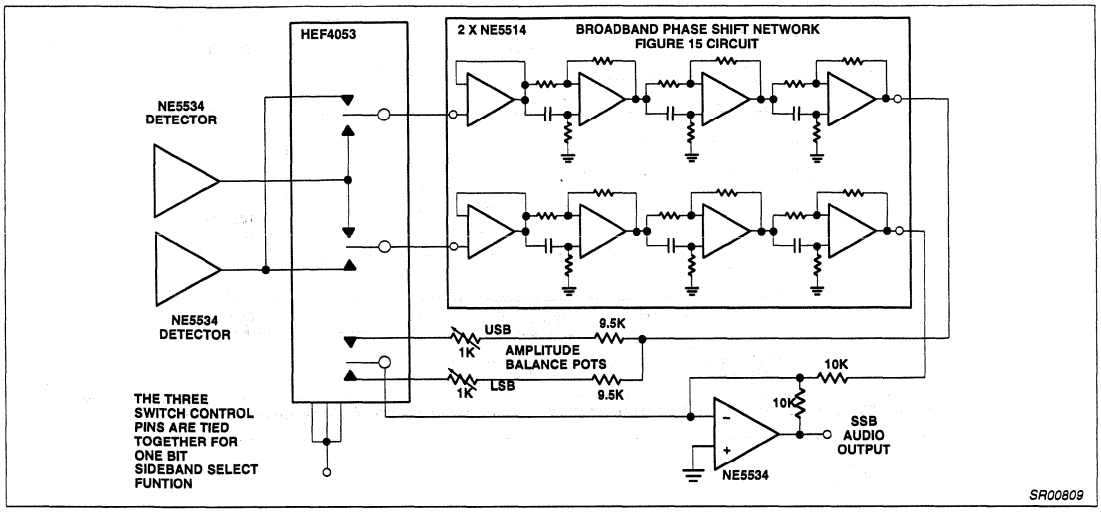


Figure 14. Sideband Select Switching Function

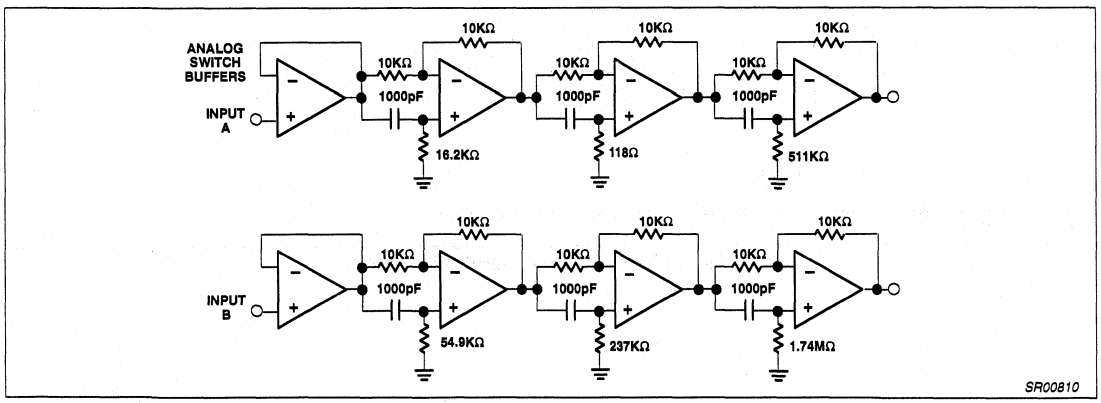


Figure 15.

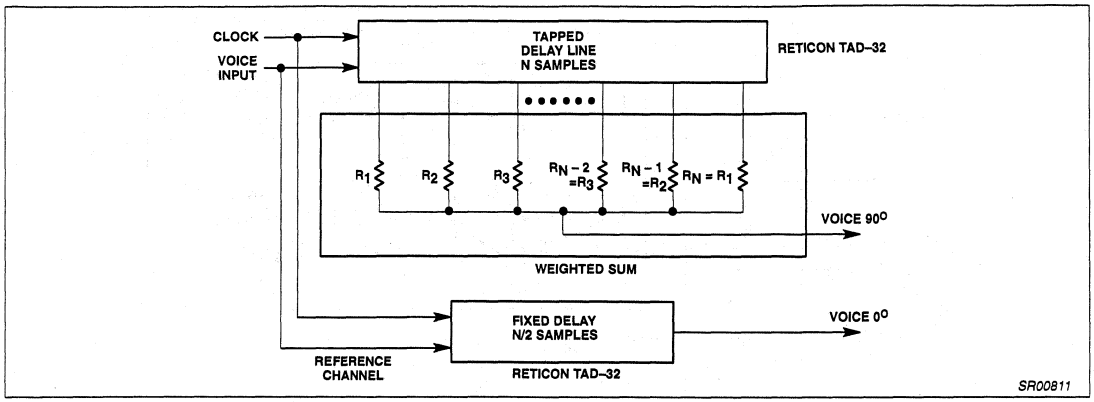


Figure 16. Broadband 90° Audio Phase Shift Technique Using Tapped Delay Line (Reference 4)

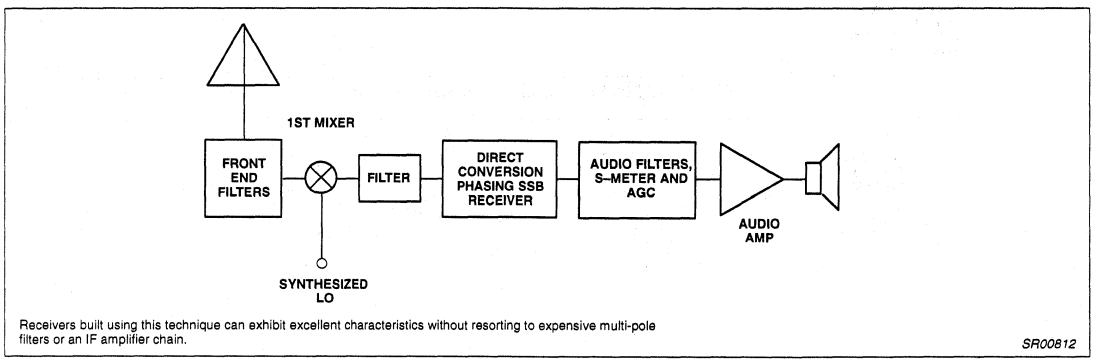


Figure 17. Complete Phasing-Filter Receiver

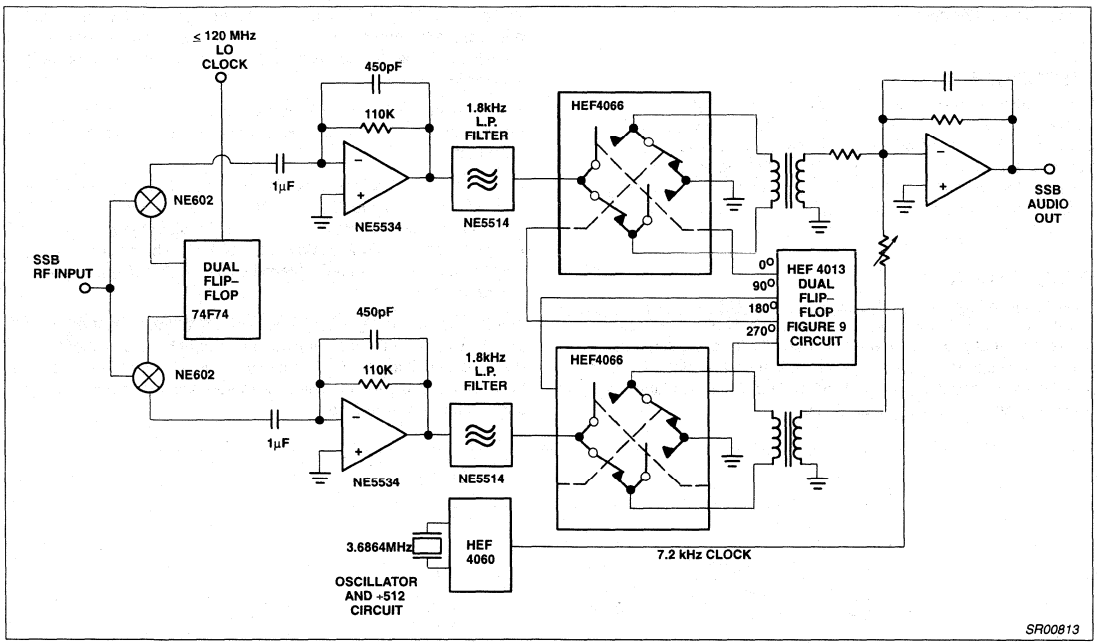


Figure 18. Weaver Method Receiver Concept Example for ≤ 30MHz Operation

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Applying the oscillator of the NE602 in low-power mixer applications

AN1982

Author: Donald Anderson

INTRODUCTION

For the designer of low power RF systems, the Philips Semiconductors NE602 mixer/oscillator provides mixer operation beyond 500MHz, a versatile oscillator capable of operation to 200MHz, and conversion gain, with only 2.5mA total current consumption. With a proper understanding of the oscillator design considerations, the NE602 can be put to work quickly in many applications.

DESCRIPTION

Figure 1 shows the equivalent circuit of the device. The chip is actually three subsystems: A Gilbert cell mixer (which provides differential input gain), a buffered emitter follower oscillator, and RF current and voltage regulation. Complete integration of the DC bias permits simple and compact application. The simplicity of the oscillator permits many configurations.

While the oscillator is simple, oscillator design isn't. This article will not address the rigors of oscillator design, but some practical guidelines will permit the designer to accomplish good performance with minimum difficulty.

Either crystal or LC tank circuitry can be employed effectively. Figure 2 shows the four most commonly used configurations in their most basic form.

In each case the Q of the tank will affect the upper frequency limits of oscillation: the higher the Q the higher the frequency. The NE602 is fabricated with a 6GHz process, but the emitter resistor from Pin 7 to ground is nominally 20k. With 0.25mA typical bias current, 200MHz oscillation can be achieved with high Q and appropriate feedback.

The feedback, of course, depends on the Q of the tank. It is generally accepted that a minimum amount of feedback should be used, so even if the choice is entirely empirical, a good trade-off between starting characteristics, distortion, and frequency stability can be quickly determined.

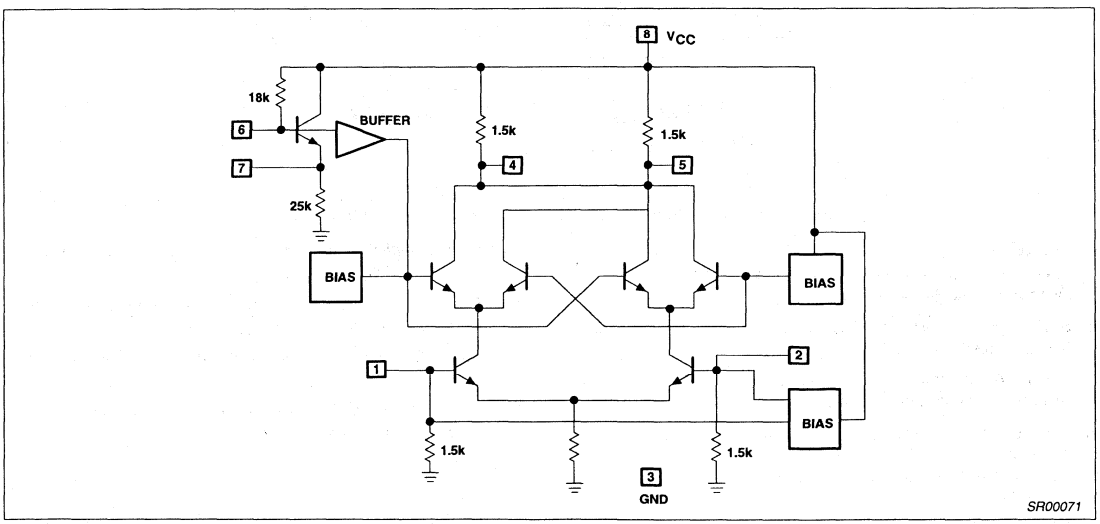

Figure 1. Equivalent Circuit

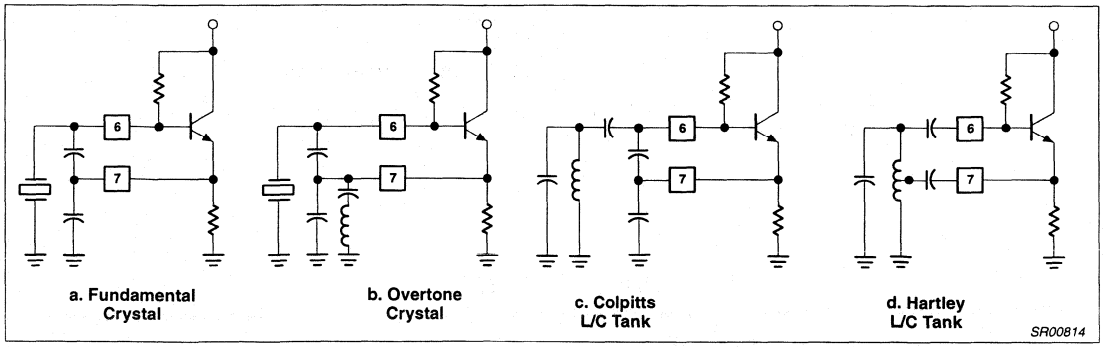

Figure 2.

Crystal Circuit Considerations

Crystal oscillators are relatively easy to implement since crystals exhibit higher Q's than LC tanks. Figure 3 shows a complete implementation of the SA602 (extended temperature version) for cellular radio with a 45MHz first IF and 455kHz second IF.

The crystal is a third overtone parallel mode with 5pF of shunt capacitance and a trap to suppress the fundamental.

LC Tank Circuits

LC tanks present a little greater challenge for the designer. If the Q is too low, the oscillator won't start. A trick which will help if all else fails is to shunt Pin 7 to ground with a 22k resistor. In actual applications this has been effective to 200MHz with high Q ceramic capacitors and a tank inductor of 0.08mH and a Q of 90. Smaller resistor value will upset DC bias because of inadequate base bias at the input of the oscillator. An external bias resistor could be added from VCC to Pin 6, but this will introduce power supply noise to the frequency spectrum.

The Hartley configuration (Figure 2D) offers simplicity. With a variable capacitor tuning the tank, the Hartley will tune a very large range since all of the capacitance is variable. Please note that the inductor must be coupled to Pin 7 with a low impedance capacitor. The Colpitts oscillator will exhibit a smaller tuning range since the fixed feedback capacitors limit variable capacitance range; however, the Colpitts has good frequency stability with proper components.

Synthesized Frequency Control

The NE602 can be very effective with a synthesizer if proper precautions are taken to minimize loading of the tank and the introduction of digital switching transients into the spectrum. Figure 4 shows a circuit suitable for aircraft navigation frequencies (108–118MHz) with 10.7MHz IF.

The dual gate MOSFET provides a high degree of isolation from prescaler switching spikes. As shown in Figure 4, the total current consumption of the NE602 and 3SK126 is typically 3mA. The MOSFET input is from the emitter of the oscillator transistor to avoid loading the tank. The Gate 1 capacitance of the MOSFET in series with the 2pF coupling capacitor adds slightly to the feedback capacitance ratio. Use of the 22k resistor at Pin 7 helps assure oscillation without upsetting DC bias.

For applications where optimum buffering of the tank, or minimum current are not mandatory, or where circuit complexity must be minimized, the buffers shown in Figure 5 can be considered.

The effectiveness of the MRF931 (or other VHF bipolar transistors) will depend on frequency and required input level to the prescaler. A bipolar transistor will generally provide the least isolation. At low frequencies the transistor can be used as an emitter follower, but by VHF the base emitter junction will start to become a bidirectional capacitor and the buffer is lost.

The 2N5484 has an IDSS of 5mA max. and the 2SK126 has IDSS of 6mA max. making them suitable for low parts count, modest current buffers. The isolation is good.

Injected LO

If the application calls for a separate local oscillator, it is acceptable to capacitively-couple 200 to 300mV at Pin 6.

Summary

The NE602 can be an effective low power mixer at frequencies to 500MHz with oscillator operation to 200MHz. All DC bias is provided internal to the device so very compact designs are possible. The internal bias sets the oscillator DC current at a relatively low level so the designer must choose frequency selective components which will not load the transistor. If the guidelines mentioned are followed, excellent results will be achieved.

Applying the oscillator of the NE602 in low-power mixer applications

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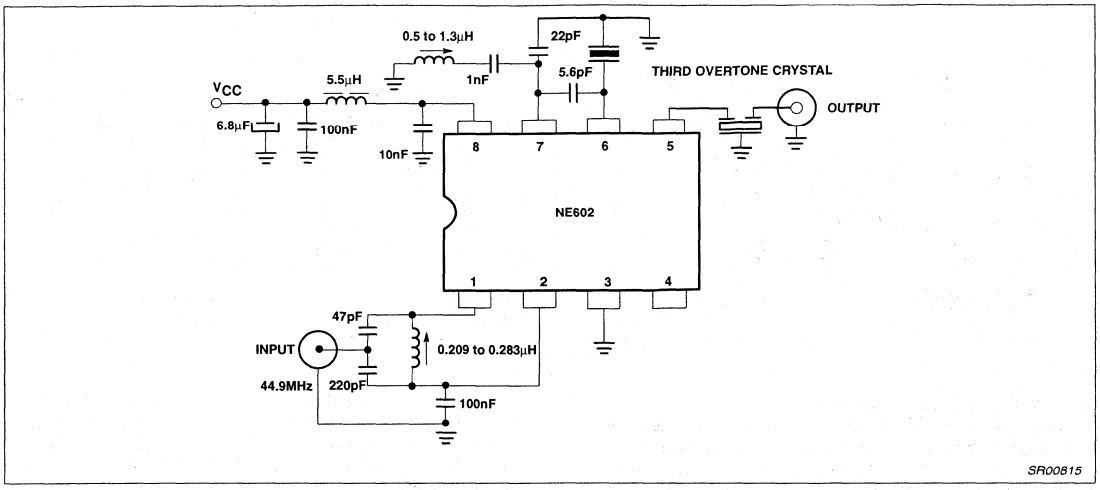

Figure 3. Cellular Radio Application

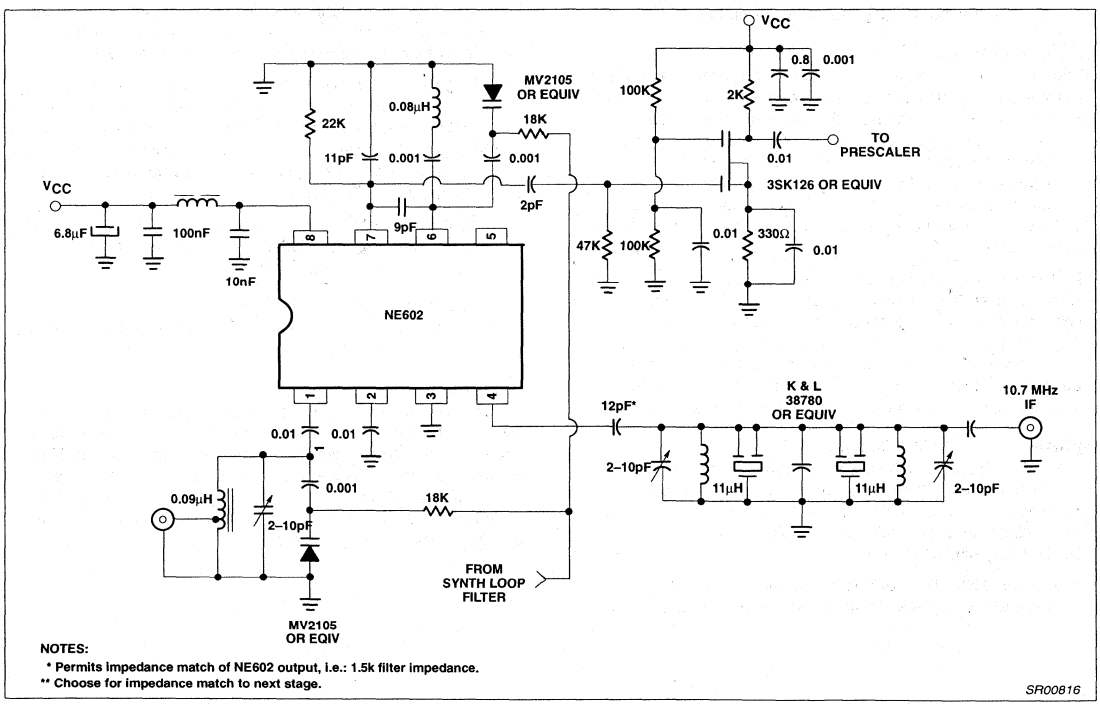

Figure 4.

Applying the oscillator of the NE602 in low-power mixer applications

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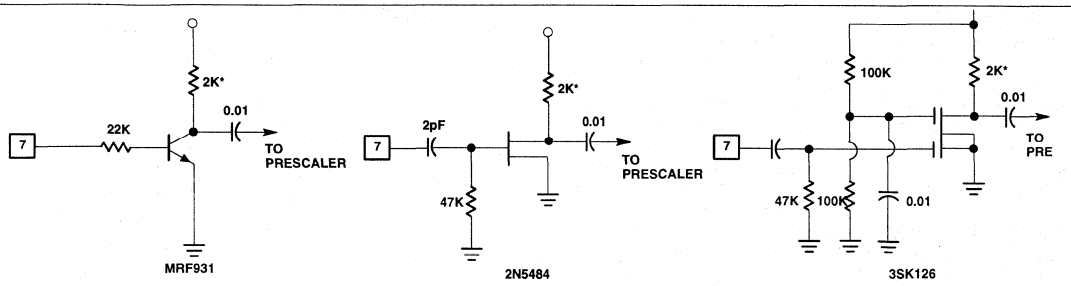


NOTES:
* 2k or as necessary for current limits or prescaler impedance match.

SR00817

Figure 5.

1GHz low voltage LNA, mixer and VCO — SA620

DESCRIPTION

The SA620 is a combined RF amplifier, VCO with tracking bandpass filter and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 1.6dB noise figure at 900MHz with 11.5dB gain and an IP3 intercept of -3dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has an 9dB noise figure and IP3 of –6dBm at the input at 900MHz. An external LO can be used in place of the internal VCO for improved mixer input IP3 and a 3mA reduction in current. The chip incorporates a through-mode option so the RF amplifier can be disabled and replaced by an attenuator (S_{21} = –7.5dB). This is useful for improving the overall dynamic range of the receiver when in an overload situation. The nominal current drawn from a single 3V supply is 10.4mA and 7.2mA in the thru-mode. Additionally, the VCO and Mixer can be powered down to further reduce the supply current to 1.2mA.

FEATURES

- Low current consumption: 10.4mA nominal, 7.2mA with thru-mode activated
- Outstanding noise figure: 1.6dB for the amplifier and 9dB for the mixer at 900MHz
- Excellent gain stability versus temperature and supply voltage
- Switchable overload capability
- Independent LNA, mixer and VCO power down capability
- Internal VCO automatic leveling loop
- Monotonic VCO frequency vs control voltage

PIN CONFIGURATION

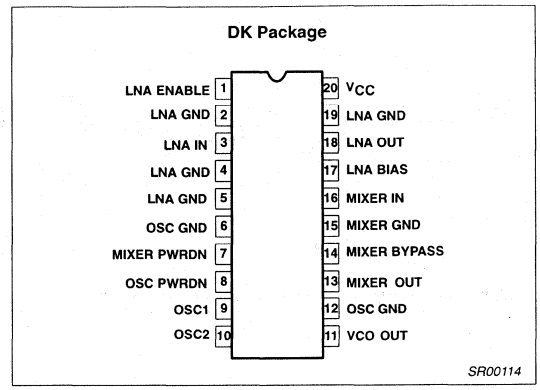


Figure 1. Pin Configuration

APPLICATIONS

- 900MHz cellular front-end
- 900MHz cordless front-end
- Spread spectrum receivers
- RF data links
- UHF frequency conversion
- Portable radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount, SSOP)	-40 to +85°C	SA620DK	SOT266-1

BLOCK DIAGRAM

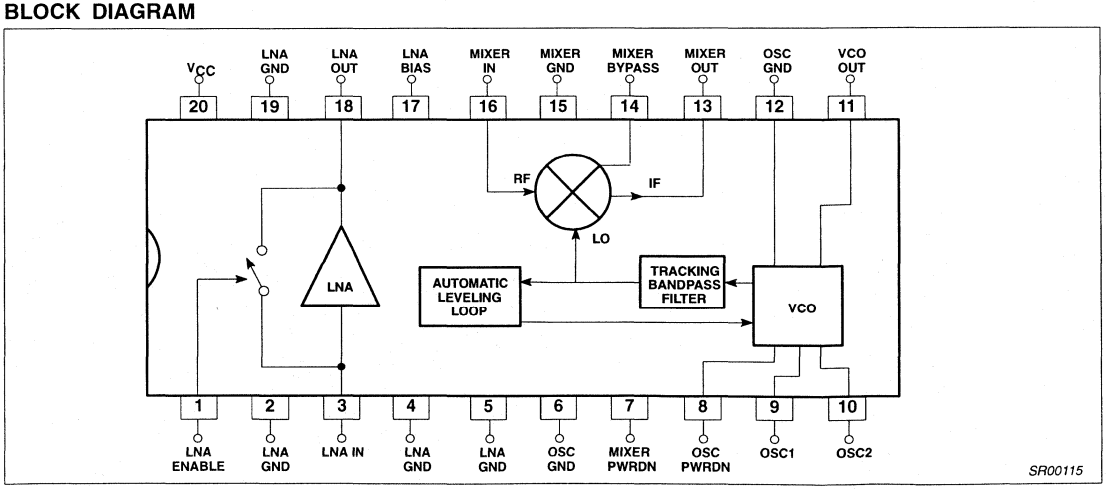


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,
   θ_{JA}: 20-Pin SSOP = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current	LNA enable input high		10.4		mA
		LNA enable input low		7.2		mA
		VCO power-down input low		7.4		mA
		Mixer power-down input low		7.4		mA
		Full chip power-down		1.2		mA
V_T	Enable logic threshold voltage[NO TAG]		1.2	1.5	1.8	V
V_{IH}	Logic 1 level	RF amp on	2.0		V_{CC}	V
V_{IL}	Logic 0 level	RF amp off	–0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	µA
V_{LNA-IN}	LNA input bias voltage	Enable = 2.4V		0.78		V
$V_{LNA-OUT}$	LNA output bias voltage	Enable = 2.4V		2.1		V
V_B	LNA bias voltage	Enable = 2.4V		2.1		V
V_{MX-IN}	Mixer RF input bias voltage			0.94		V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the SA620 LNA.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; Enable = +3V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			-3σ	TYP	+3σ	
S_{21}	Amplifier gain	900MHz	10	11.5	13	dB
S_{21}	Amplifier gain in through mode	Enable = 0.4V, 900MHz	-9	-7.5	-6	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity in pwr-dwn mode	900MHz		-0.014		dB/°C
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled	900MHz		0.003		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz		0.01		dB/MHz
S_{12}	Amplifier reverse isolation	900MHz		-20		dB
S_{11}	Amplifier input match[1]	900MHz		-10		dB
S_{22}	Amplifier output match[1]	900MHz		-12		dB
P_{-1dB}	Amplifier input 1dB gain compression	900MHz		-16		dBm
IP3	Amplifier input third order intercept	900MHz	-4.5	-3	-1.5	dBm
NF	Amplifier noise figure	900MHz	1.3	1.6	1.9	dB
t_{ON}	Amplifier turn-on time (Enable Lo → Hi)	See Figure 3		50		µs
t_{OFF}	Amplifier turn-off time (Enable Hi → Lo)	See Figure 3		5		µs
VG_C	Mixer voltage conversion gain: $R_P = R_L$ = 1kΩ,	f_S = 0.9GHz, f_{LO} = 0.8GHz, f_{IF} = 100MHz	14.5	16	17.5	dB
PG_C	Mixer power conversion gain: $R_P = R_L$ = 1kΩ,	f_S = 0.9GHz, f_{LO} = 0.8GHz, f_{IF} = 100MHz	1.5	3	4.5	dB
S_{11M}	Mixer input match[1]	900MHz		-10		dB
NF_M	Mixer SSB noise figure	900MHz	7.5	9	10.5	dB
P_{-1dB}	Mixer input 1dB gain compression	900MHz		-13		dBm
$IP3_M$	Mixer input third order intercept	f_2–f_1 = 1MHz, 900MHz	-7.5	-6	-4.5	dBm
IP_{2INT}	Mixer input second order intercept	900MHz		12		dBm
P_{RFM-IF}	Mixer RF feedthrough	900MHz		-20		dB
P_{LO-IF}	LO feedthrough to IF	900MHz		-25		dBm
P_{LO-RFM}	LO to mixer input feedthrough	900MHz		-30		dBm
P_{LO-RF}	LO to LNA input feedthrough	900MHz		-45		dBm
P_{VCO}	VCO buffer out	900MHz		-16		dBm
	VCO frequency range		300 (min)		1200 (max)	MHz
	VCO phase noise	Offset = 60kHz		-105		dBc/Hz

NOTE:
1. Simple L/C elements are needed to achieve specified return loss.

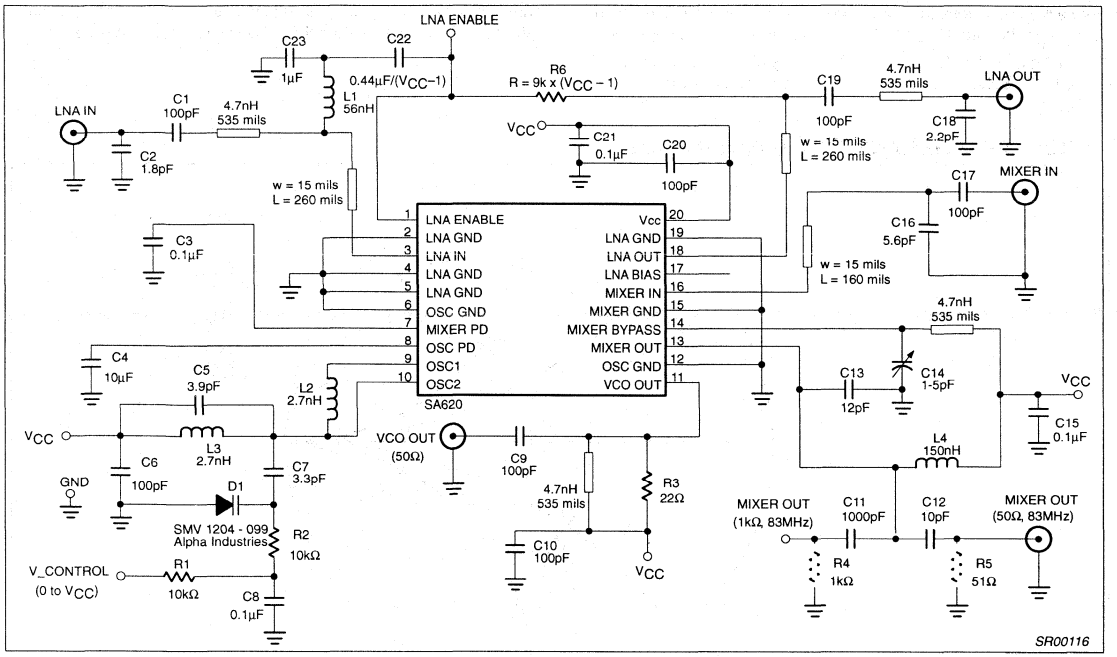


Figure 3. A Complete LNA, Mixer and VCO

CIRCUIT TECHNOLOGY

LNA

Impedance Match: Intrinsic return loss at the input and output ports is 7dB and 9dB, respectively. With no external matching, the associated LNA gain is ≈10dB and the noise figure is ≈1.4dB. However, the return loss can be improved at 900MHz using suggested L/C elements (Figure NO TAG) as the LNA is unconditionally stable.

Noise Match: The LNA achieves 1.6dB noise figure at 900MHz when S_{11} = -10dB. Further improvements in S_{11} will slightly increase the NF and S_{21}.

Thru-Mode: A series switch can be activated to feed RF signals from LNA input to output with an attenuator (S_{21} = −7.5dB). As a result, the power handling is greatly improved and current consumption is decreased by 3.2mA as well. However, if this mode is not required, C23 and R6 can be deleted.

Temperature Compensation: The LNA has a built-in temperature compensation scheme to reduce the gain drift to 0.003dB/°C from −40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 3V to 5V.

Mixer

Input Match: The mixer is configured for maximum gain and best noise figure. The user needs to supply L/C elements to achieve this performance.

Mixer Bypass: To optimize the IP3 of the mixer input, one must adjust the value of C14 for the given board layout. The value typically lies between 1 and 5pF. Once a value if selected, a fixed capacitor can be used. Further improvements in mixer IP3 can be achieved by inserting a resistive loss at the mixer input, at the expense of system gain and noise figure.

Tracking Bandpass Filter: At the LO input port of the mixer there is a second-order bandpass filter (approx. 50MHz bandwidth) which will track the VCO center frequency. The result is the elimination of low frequency noise injected into the mixer LO port without the need for an external LO filter.

Power Down: The mixer can be disabled by connecting Pin 7 to ground. If a Schottky diode is connected between Pin 1 (cathode) and Pin 7 (anode), the LNA disable signal will control both LNA and mixer simultaneously When the mixer is disabled, 3mA is saved.
Test Port: Resistor R5 can be substituted with an external test port of 50Ω input impedance. Since R5 and MIXER OUT have the same output power, the result is a direct power gain measurement.

VCO

Automatic Leveling Loop: An on-chip detector and loop amplifier will adjust VCO bias current to regulate the VCO amplitude regardless of the Q-factor (>10) of the resonator and varactor diode. However, the real current reduction will not occur until the VCO frequency falls below 500MHz. For a typical resonator the steady-state current is 3mA at 800MHz.

Buffered VCO Output: The VCO OUT (Pin 11) signal can drive an external prescaler directly (see also the Philips SA7025 low voltage, fractional-N synthesizer). The extracted signal levels need to be limited to −16dBm or less to maintain mixer IIP3.

Phase Noise: If close-in phase noise is not critical, or if an external synthesizer is used, C4 (Pin 8) can be decreased to a lower value.

Power-Down: The VCO can be disabled by connecting Pin 8 to ground. If a Schottky diode is connected between Pin 1 (cathode) and Pin 8 (anode), the LNA disable signal will control both LNA and VCO simultaneously. When the VCO is disabled, 3mA is saved.

TYPICAL PERFORMANCE CHARACTERISTICS

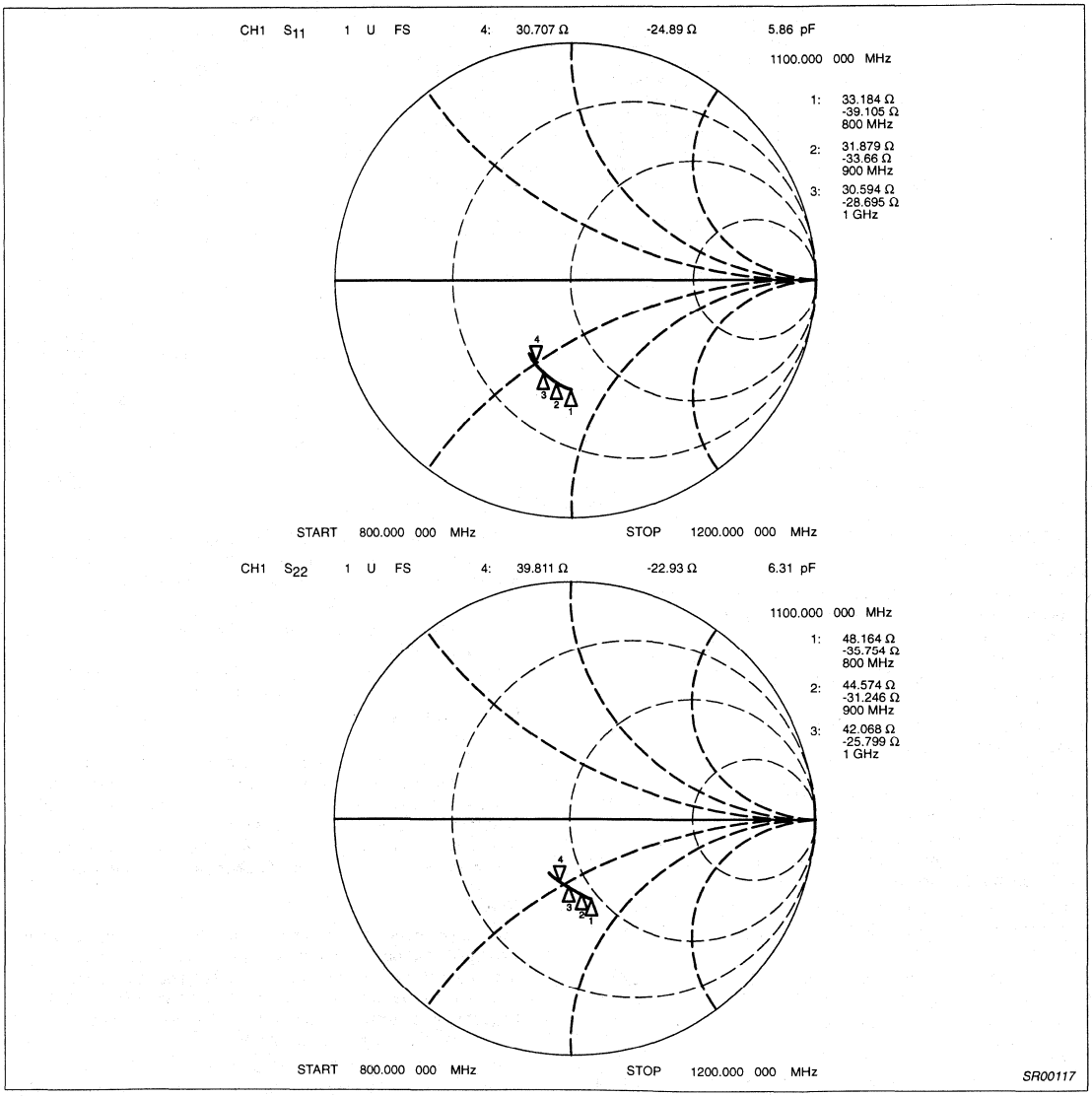
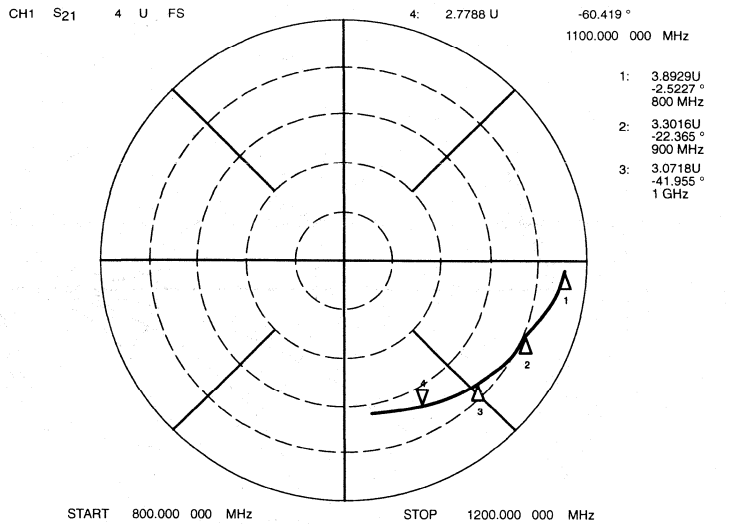


Figure 4. LNA Input and Output Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



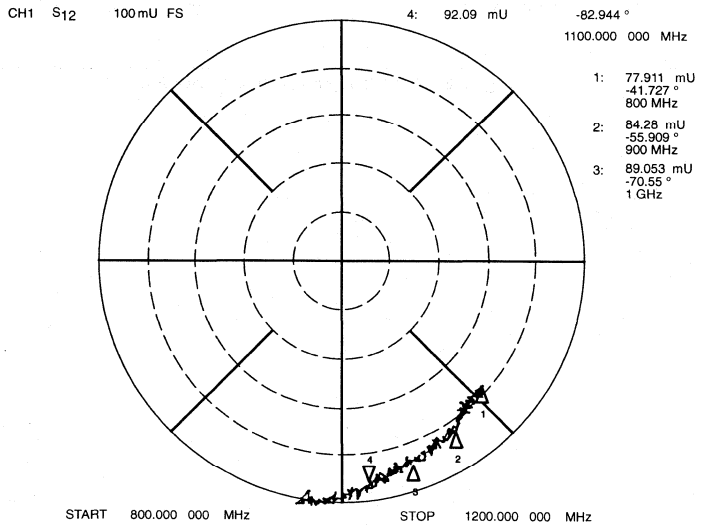


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Figure 5. LNA Transmission and Isolation Characteristics (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

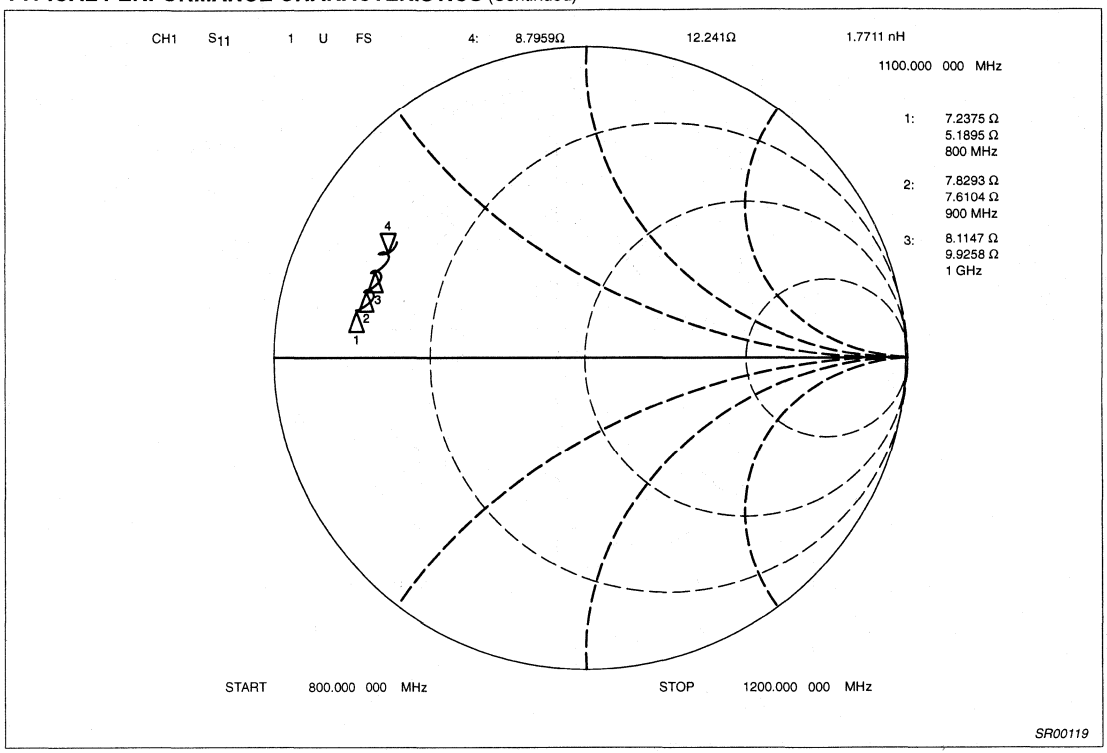


Figure 6. Mixer RF Input Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

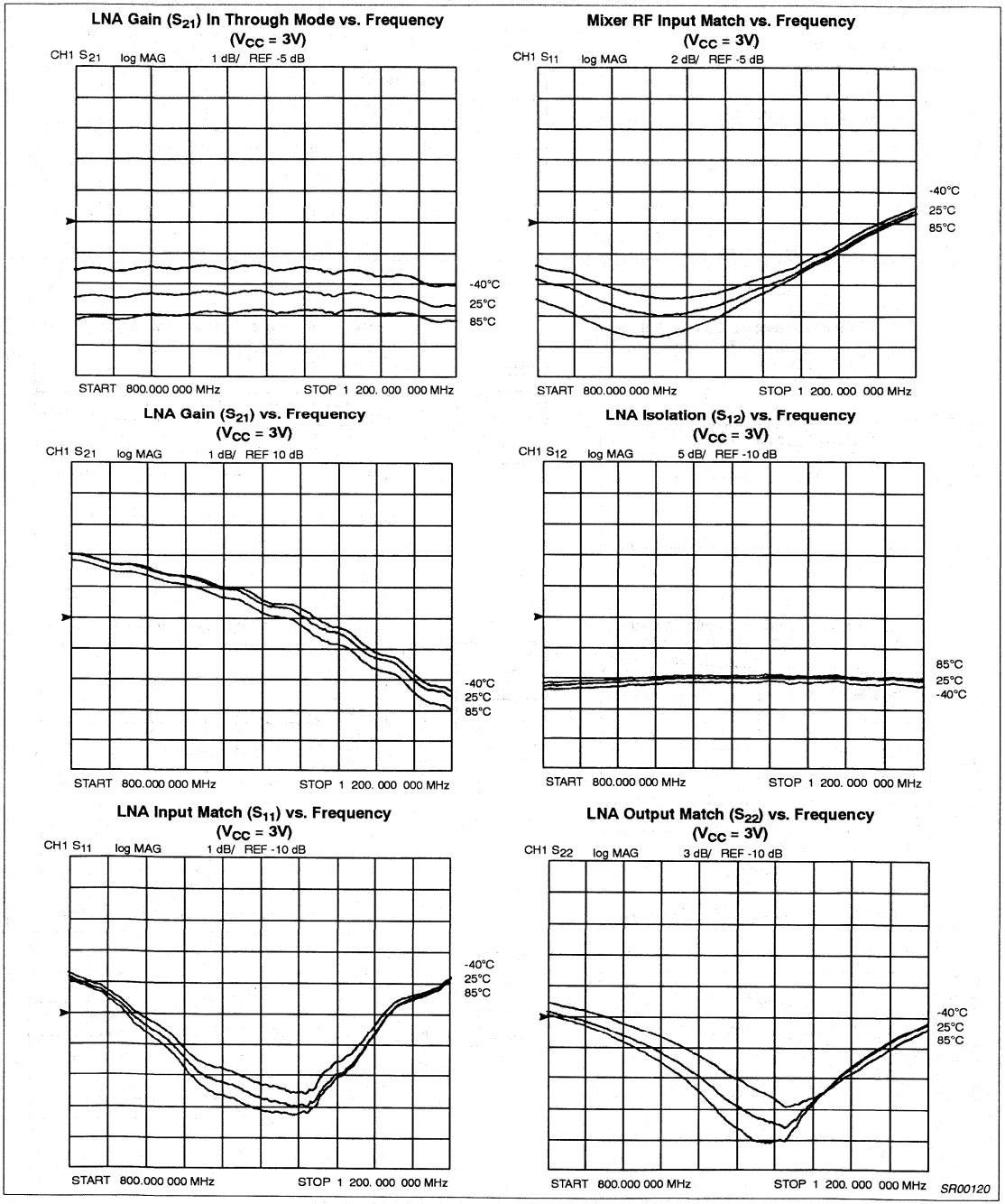


Figure 7. Typical Performance Characteristics (cont.)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

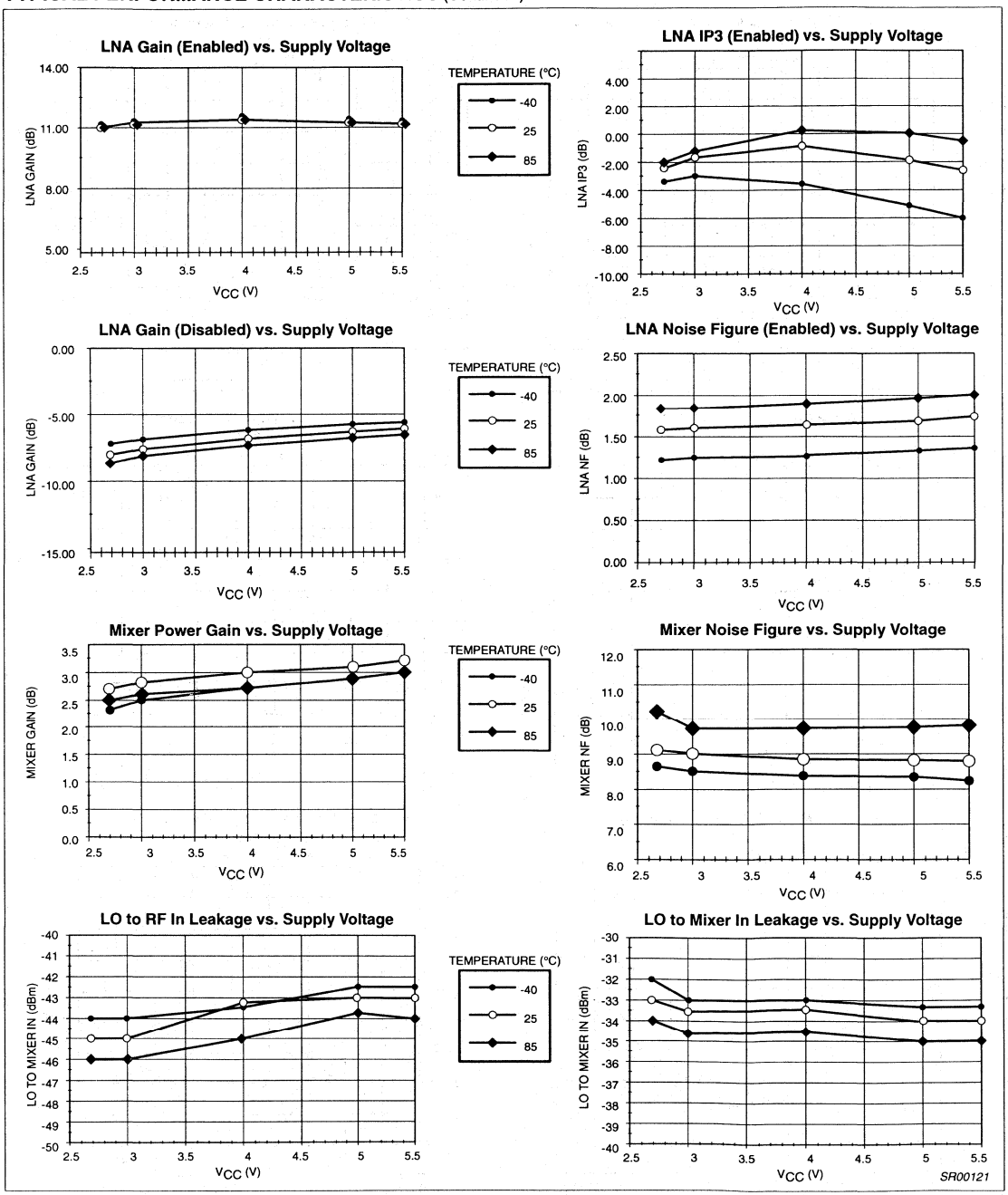


Figure 8. Typical Performance Characteristics (cont.)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

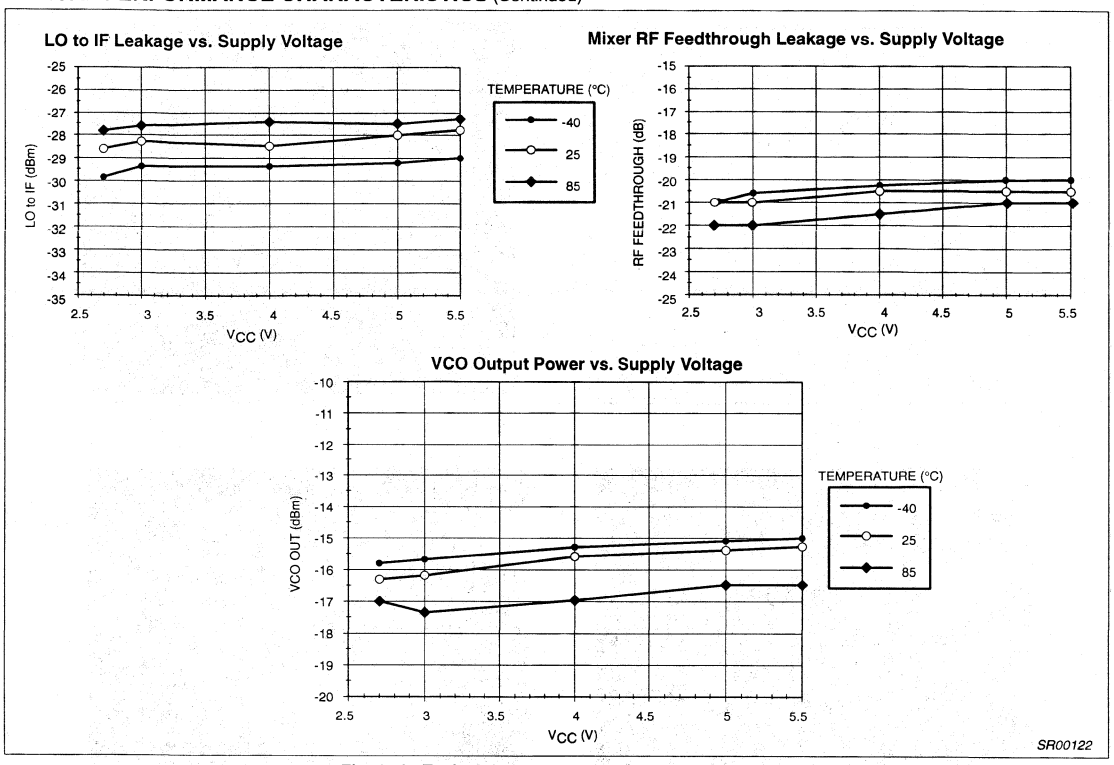
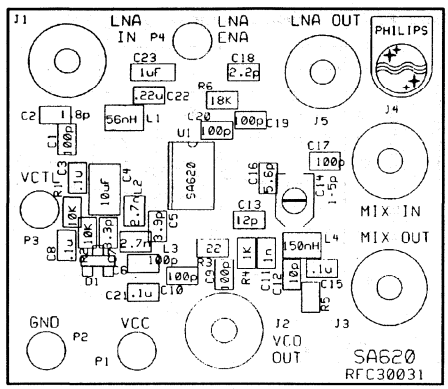
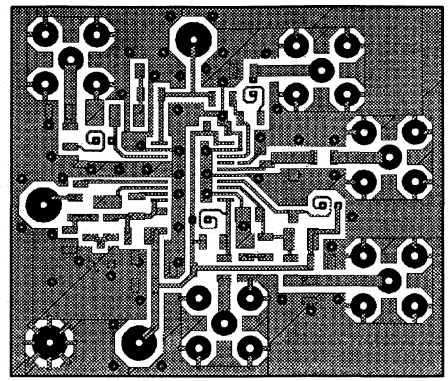
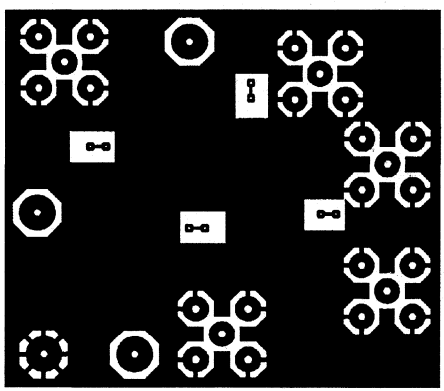


Figure 9. Typical Performance Characteristics (cont.)







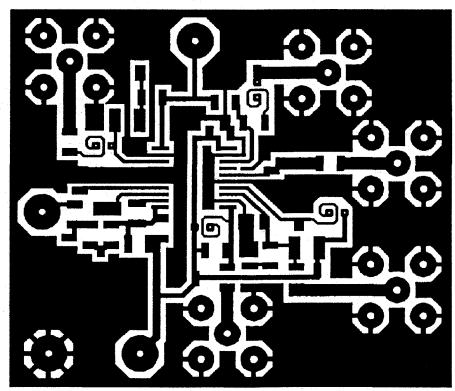


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Figure 10. Board Layout (NOT ACTUAL SIZE)

1GHz low voltage LNA, mixer and VCO SA621

DESCRIPTION

The SA621 is a combined low-noise amplifier, mixer and VCO designed for high-performance low-power communication systems from 800-1000MHz. The low-noise preamplifier has a 1.7dB noise figure at 881MHz with 15dB gain and an IP3 intercept of -7dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has a 12dB noise figure and IP3 of +4.5dBm at the input at 881MHz. The integrated VCO circuit with external resonator produces a high quality LO signal that drives the mixer and is buffered to an external PLL synthesizer IC. The nominal current drawn from a single 3V supply is 13.3mA. Additionally, the entire circuit can be powered down to further reduce the supply current to less than 20µA.

FEATURES

- Low current consumption
- Outstanding gain and noise figure
- Excellent gain stability versus temperature and supply voltage
- LNA, mixer and VCO power down capability
- Monotonic VCO frequency vs control voltage

PIN CONFIGURATION

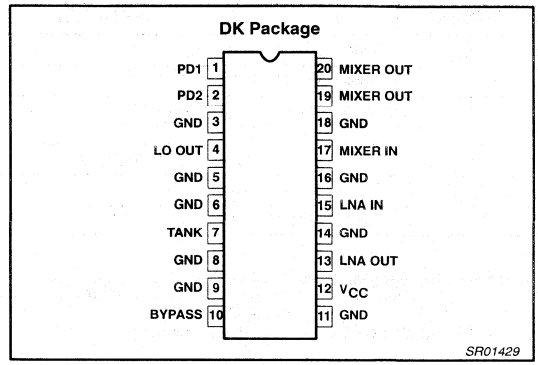


Figure 1. Pin Configuration

APPLICATIONS

- 900MHz cellular and cordless front-end
- Spread spectrum receivers
- RF data links
- UHF frequency conversion
- Portable radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount, SSOP)	-40 to +85°C	SA621DK	SOT266-1

BLOCK DIAGRAM

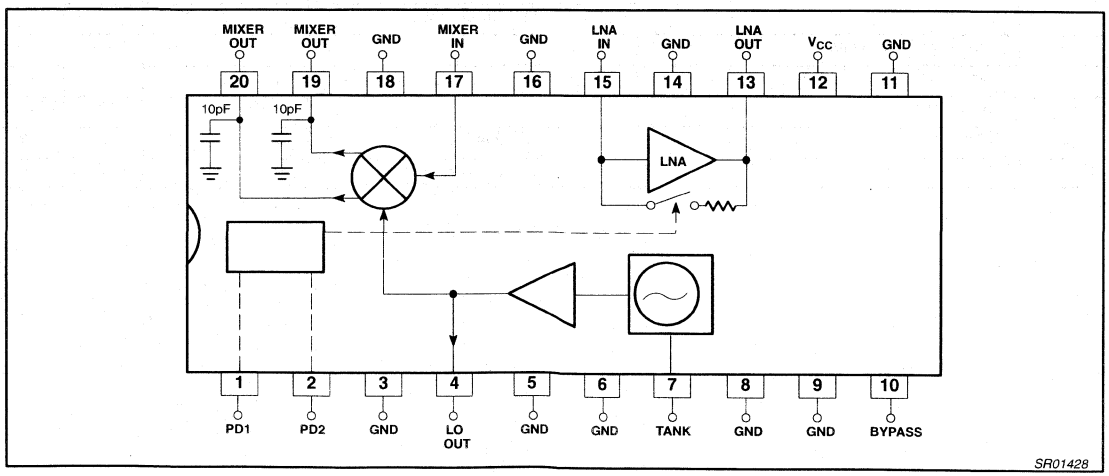


Figure 2. SA621 Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)2 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,
   θ_{JA}: 20-Pin SSOP = 110°C/W
3. Pins 19 and 20 are ESD sensitive (mixer outputs).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current	Full power-on		13.3		mA
		LNA powered-down		10		mA
		Standby (VCO + bias)		5.7		mA
		Full power-down		20		µA
V_T	PD logic threshold voltage		1.2	1.6	1.8	V
V_{IH}	Logic 1 level		2.0		V_{CC}	V
V_{IL}	Logic 0 level		–0.3		0.8	V
I_{IL}	PD1 input current	Enable = 0.4V		10		µA
I_{IH}	PD2 input current	Enable = 2.4V		10		µA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V, T_A = 25°C; RF_{IN} = 881MHz, f_{VCO} = 964MHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			–3σ	TYP	+3σ	
Low Noise Amplifier						
f_{RF}	RF input frequency range		800		1000	MHz
S_{21}	Amplifier gain			15		dB
S_{21}	Amplifier gain in power-down mode			-28		dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled			0.006		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.0GHz		±0.013		dB/MHz
S_{12}	Amplifier reverse isolation	@ 881 MHz		-28		dB
S_{11}	Amplifier input match	With ext. impedance matching		-10		dB
S_{22}	Amplifier output match			-10		dB
P_{-1dB}	Amplifier input 1dB gain compression			-20		dBm
IP3	Amplifier input third order intercept			-7		dBm
NF	Amplifier noise figure			1.7		dB
t_{ON}	Amplifier turn-on time (Enable Lo → Hi)			120		µs
t_{OFF}	Amplifier turn-off time (Enable Hi → Lo)			0.3		µs
Mixer						
PG_C	Mixer power conversion gain: $R_P = R_L$ = 1.2kΩ,	f_{RF} = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz		8.7		dB
S_{11M}	Mixer input match	Ext. impedance matching req.		-10		dB
NF_M	Mixer SSB noise figure			12		dB
P_{-1dB}	Mixer input 1dB gain compression			-10		dBm
$IP3_M$	Mixer input third order intercept			4.5		dBm
IP_{2INT}	Mixer input second order intercept			15		dBm
P_{RFM-IF}	Mixer RF feedthrough	RF_{IN} = -25dBm		-41		dBm
P_{LO-IF}	LO feedthrough to IF	LO = -10dBm		-23		dBm
P_{LO-RFM}	LO to mixer input feedthrough			-52		dBm
P_{LO-RF}	LO to LNA input feedthrough			-38		dBm
Voltage Controlled Oscillator (VCO)[1]						
f_{VCO}	VCO frequency range		883		1083	MHz
P_{VCO}	VCO power out	See Figure 3	-10	-8		dBm
	VCO phase noise[2]	Offset = 30kHz		-109		dBc/Hz
		Offset = 60kHz		-115		
	Harmonic content			-22		dBc
	Residual modulation				45	dB
	Pulling figure	VSWR=2:1, all phases		±500		kHz
	Pushing figure			±100		kHz/V
Overall System						
G_{SYS}	System gain	LNA + Mixer	23.0	23.7	24.4	dB

NOTES:
1. VCO performance dependent on external components.
2. Based on copper-plated 2mm ceramic resonator (1/4 wave), f = 1025MHz, and can be improved by silver-plated or larger resonators.

Table 6. Power ON/OFF Control Logic

PD1	PD2	
0	0	Full chip power-down
0	1 or open	VCO on, Mixer on, LNA power-down
1 or open	0	VCO on, LNA and Mixer power-down
1 or open	1 or open	Full chip power-on (default)

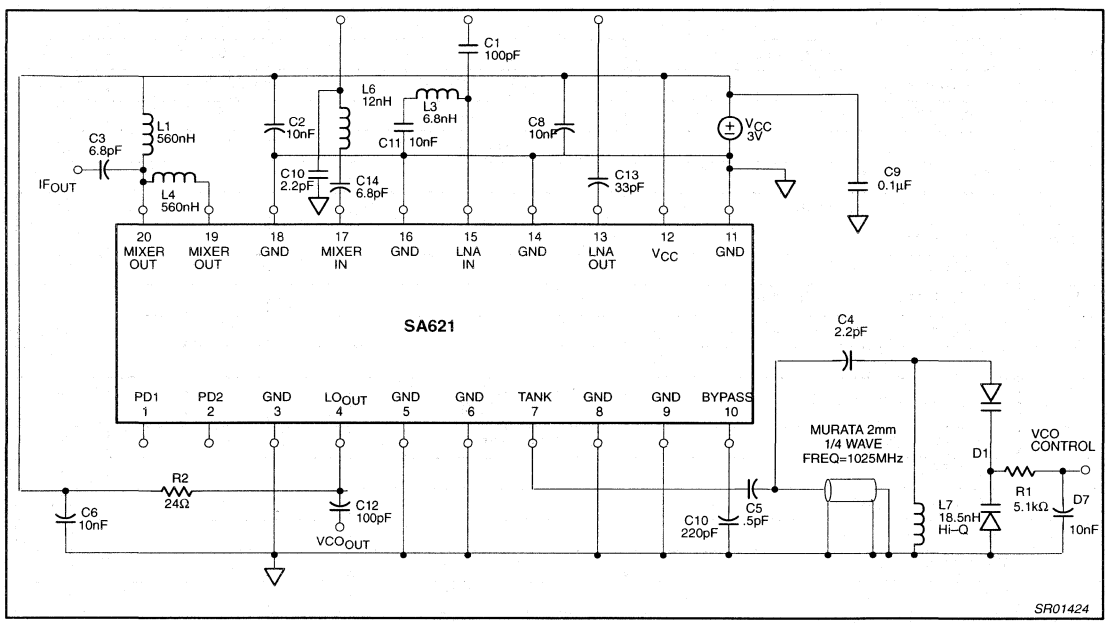


Figure 3. SA621 Applications Circuit

PERFORMANCE CHARACTERISTICS

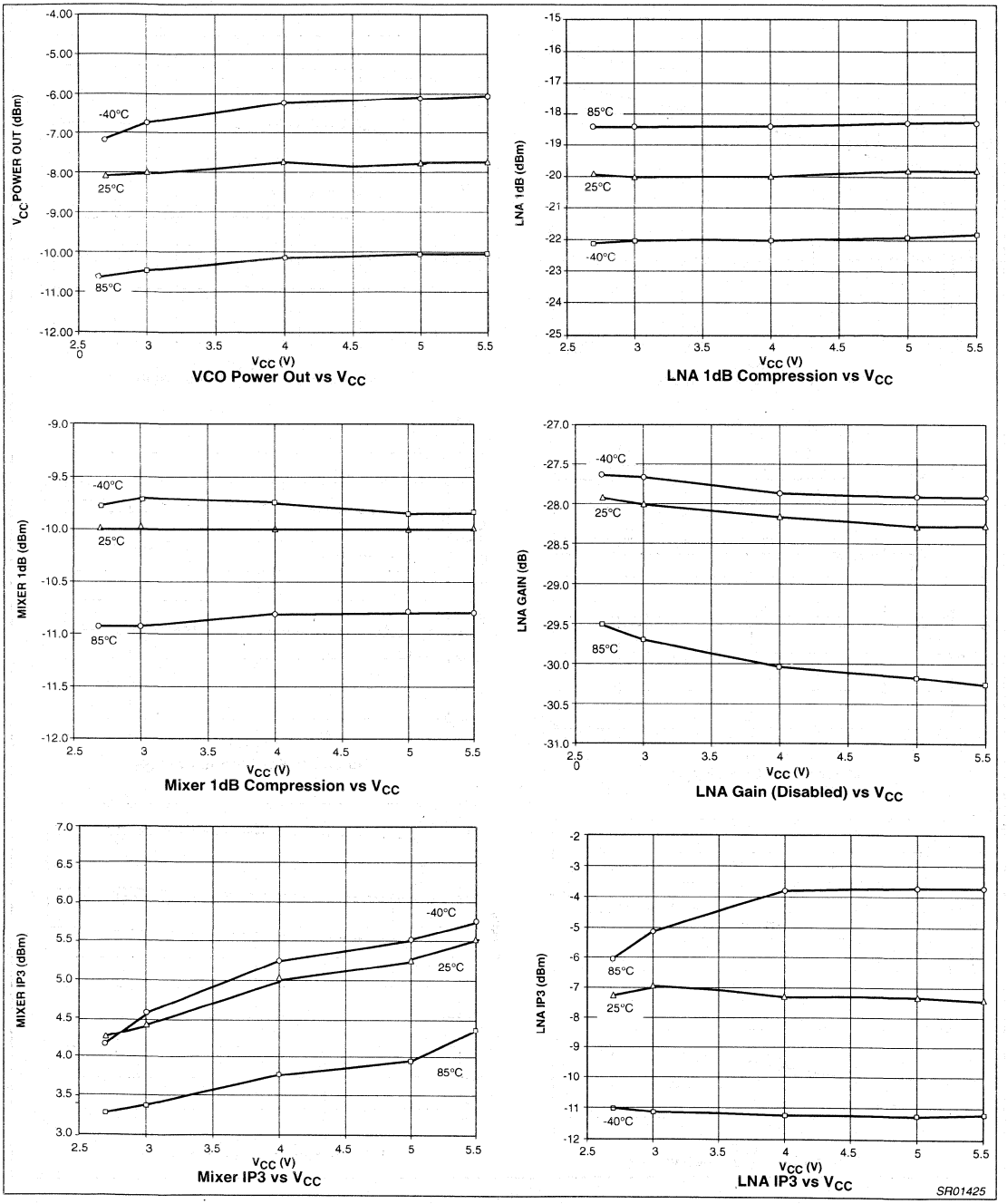
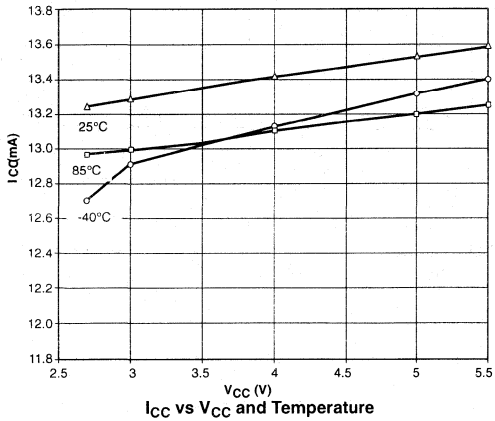
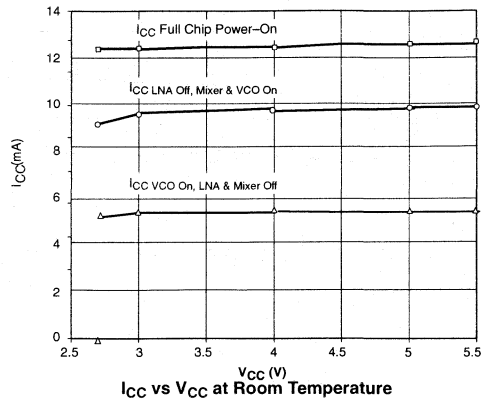


Figure 4.

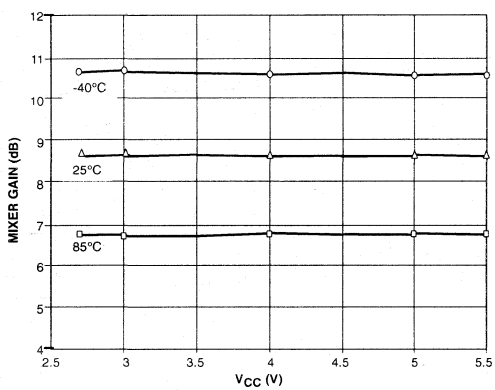
PERFORMANCE CHARACTERISTICS



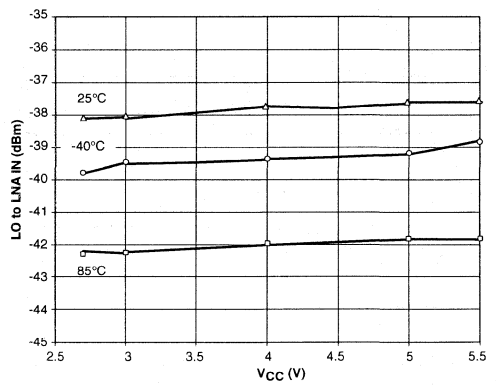
I_{CC} vs V_{CC} and Temperature



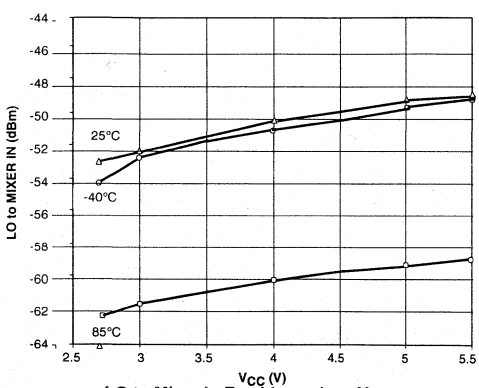
I_{CC} vs V_{CC} at Room Temperature



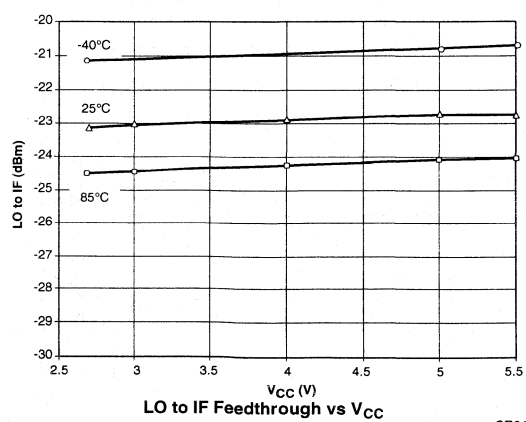
Mixer Power Gain vs V_{CC}



LO to LNA In Feedthrough vs V_{CC}



LO to Mixer In Feedthrough vs V_{CC}



LO to IF Feedthrough vs V_{CC}

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Figure 5.

PERFORMANCE CHARACTERISTICS

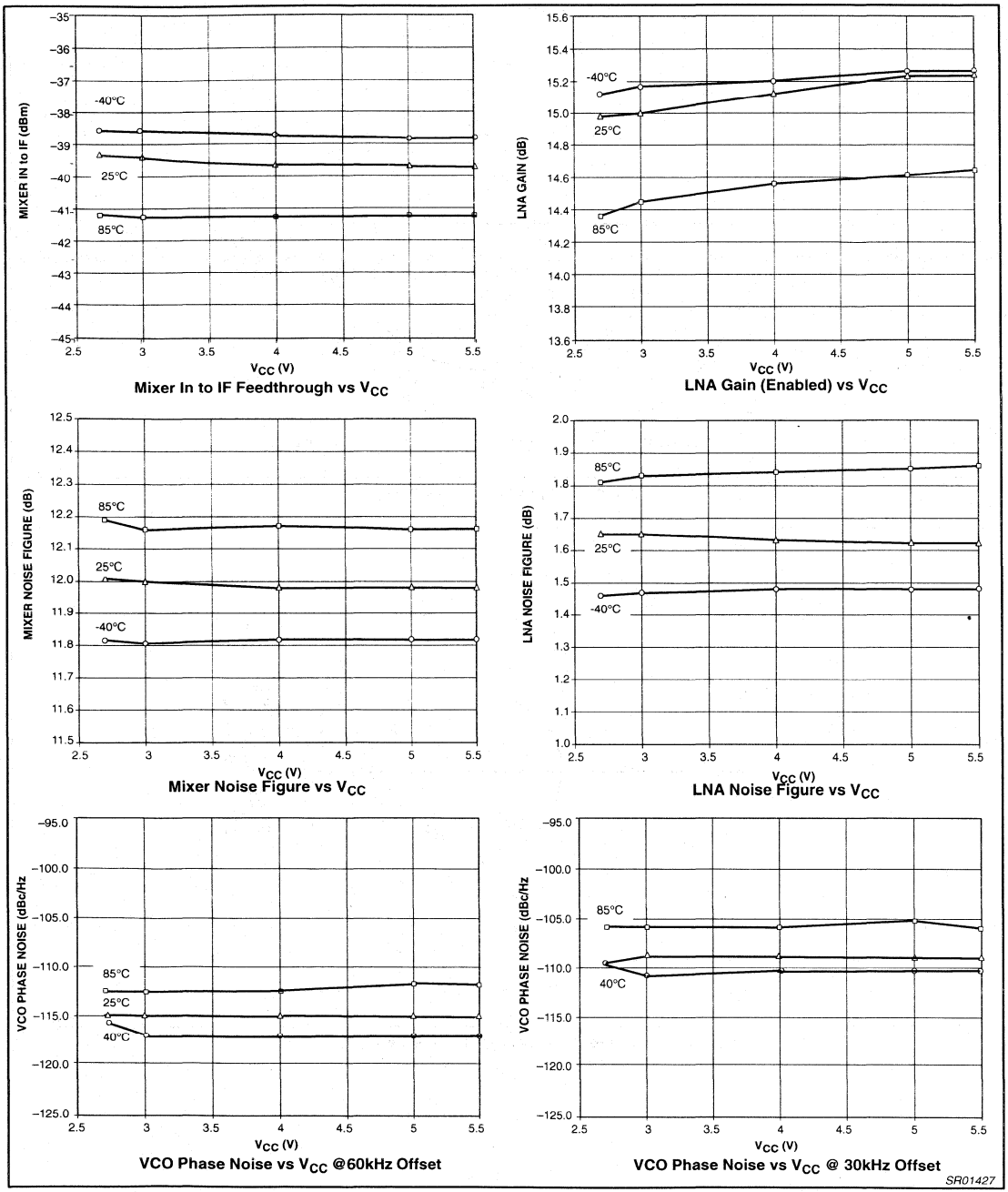


Figure 6.

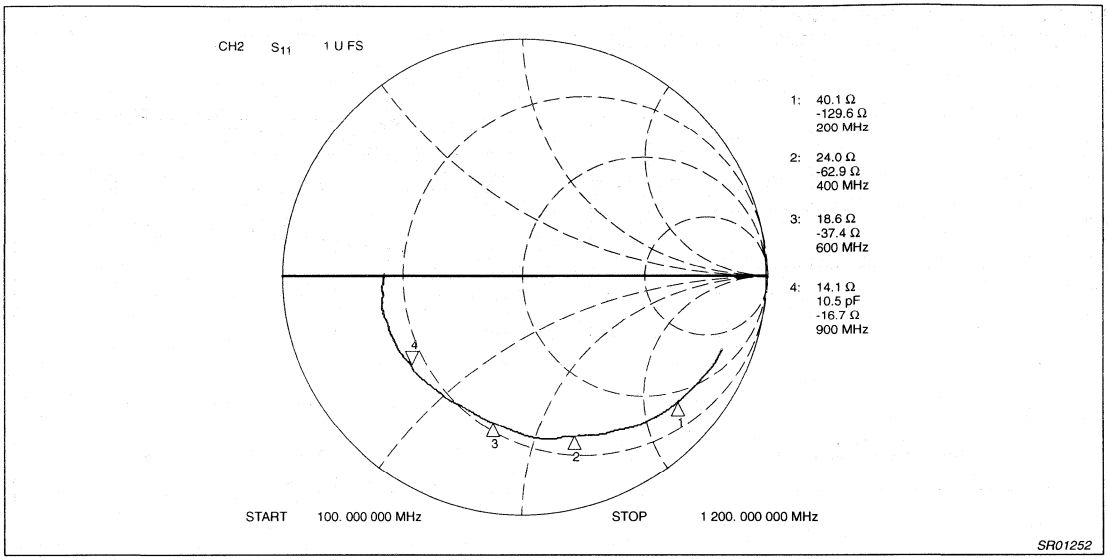


Figure 7. Typical S_{11} of LNA at 3V

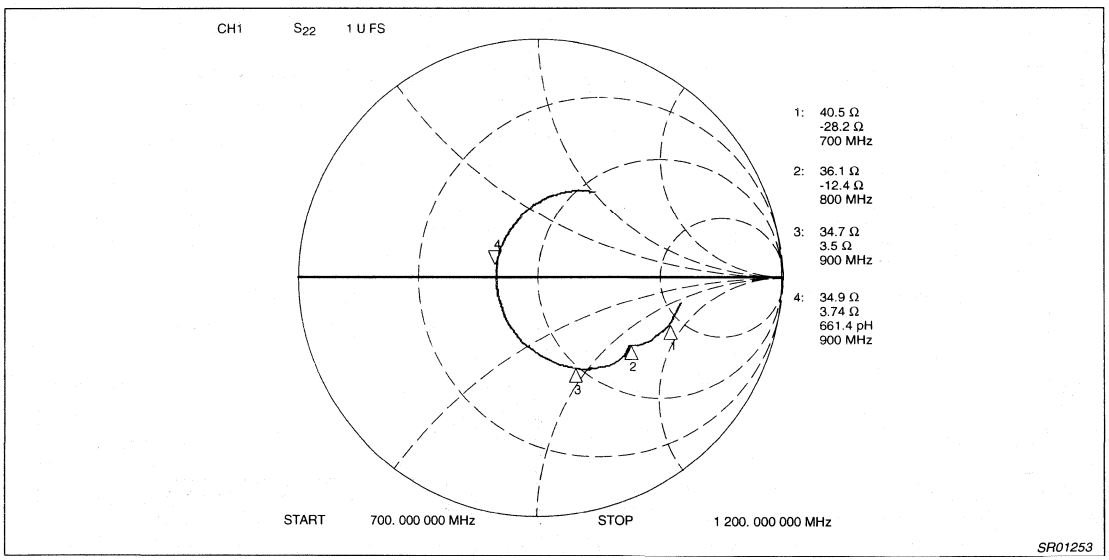


Figure 8. Typical S_{22} of LNA at 3V

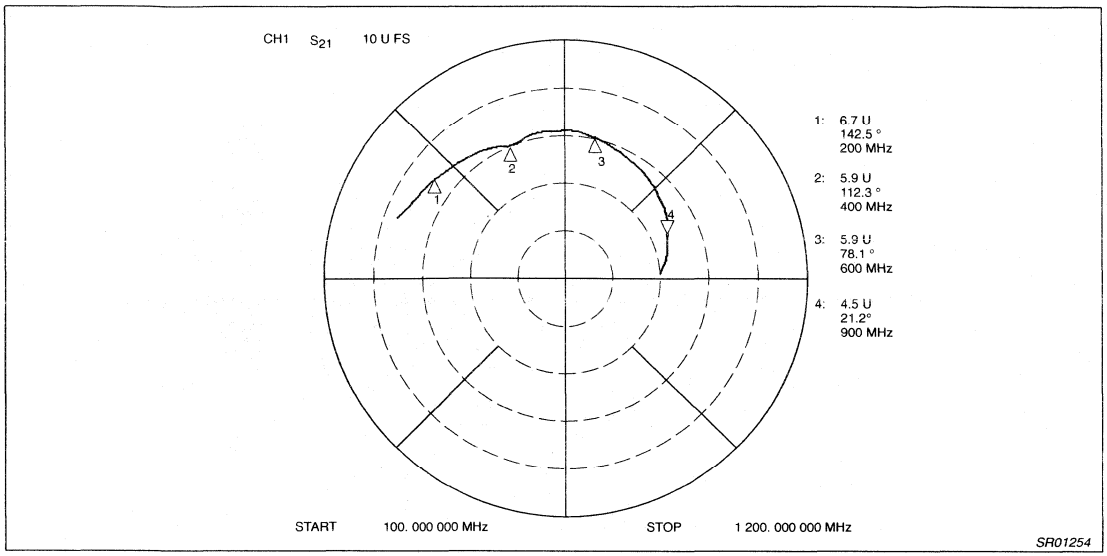


Figure 9. Typical S_{21} of LNA at 3V

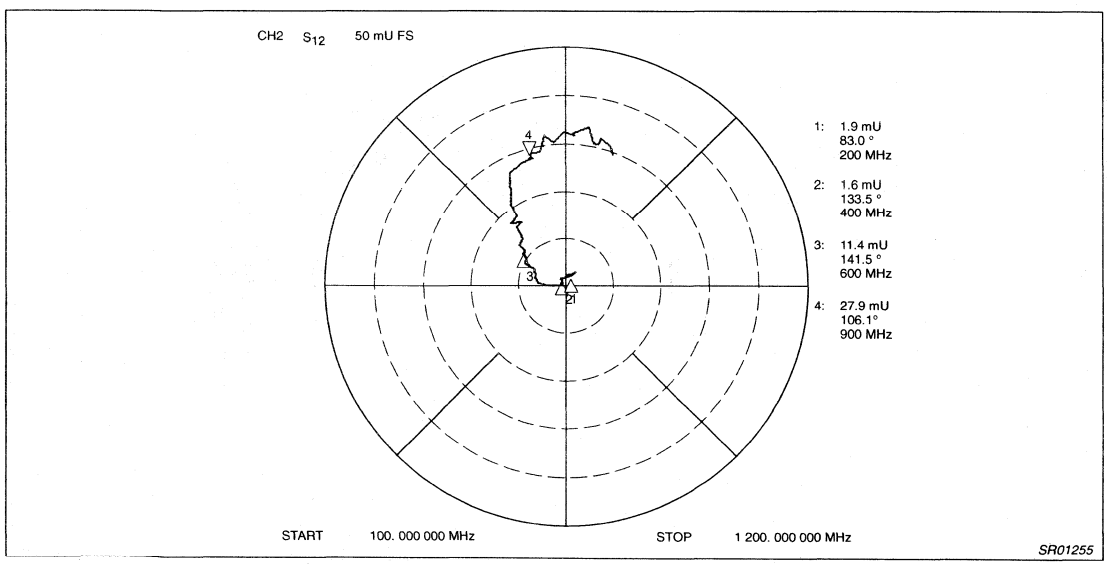


Figure 10. Typical S_{12} of LNA at 3V

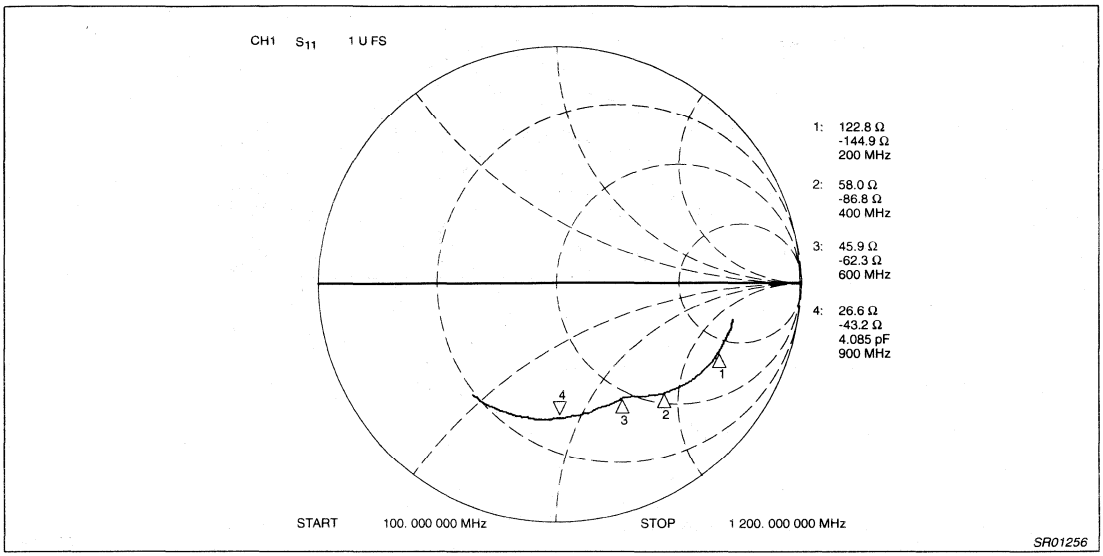


Figure 11. Typical S_{11} of Mixer at 3V

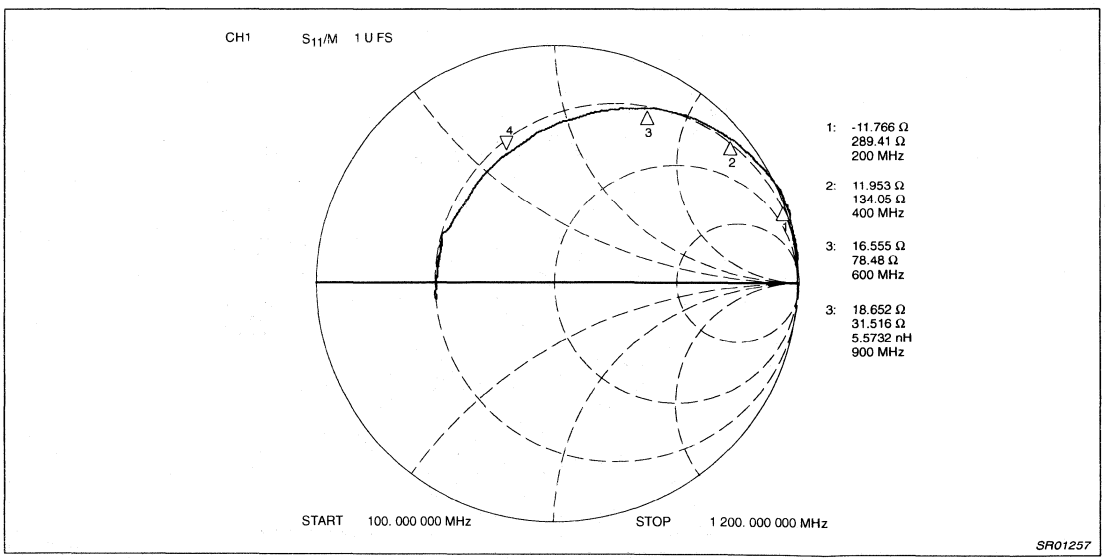


Figure 12. Typical $1/S_{11}$ of VCO (Pin 7)at 3V

Table 7. Typical S-Parameters of LNA at 3V

LNA								
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)	$\|S_{21}\|$ (U)	$<S_{21}$ (deg)	$\|S_{12}\|$ (U)	$<S_{12}$ (deg)	$\|S_{22}\|$ (U)	$<S_{22}$ (deg)
100	0.86	-20	7.4	160	0.001	92	0.59	-10
122	0.86	-24	7.1	156	0.001	62	0.58	-12
144	0.85	-28	7.0	151	0.001	105	0.58	-14
166	0.83	-32	6.9	148	0.000	92	0.57	-16
188	0.82	-36	6.8	144	0.002	100	0.57	-18
210	0.81	-41	6.7	140	0.002	74	0.56	-20
232	0.80	-45	6.6	136	0.002	100	0.55	-22
254	0.79	-48	6.5	133	0.001	84	0.54	-25
276	0.78	-52	6.4	130	0.001	103	0.53	-27
298	0.76	-56	6.3	126	0.002	94	0.52	-29
320	0.75	-59	6.3	123	0.002	67	0.51	-31
342	0.73	-63	6.2	119	0.002	108	0.50	-33
364	0.71	-66	6.1	116	0.002	118	0.48	-35
386	0.70	-69	6.0	113	0.001	103	0.47	-36
408	0.69	-72	5.9	111	0.001	176	0.46	-37
430	0.68	-76	5.9	109	0.004	174	0.45	-37
452	0.69	-78	6.0	106	0.006	162	0.46	-38
474	0.68	-82	6.1	102	0.007	160	0.47	-42
496	0.67	-85	6.1	97	0.008	153	0.47	-46
518	0.66	-89	6.1	93	0.010	146	0.46	-50
540	0.65	-92	6.1	89	0.009	142	0.45	-55
562	0.63	-96	6.1	85	0.010	138	0.43	-59
584	0.62	-99	6.0	81	0.011	146	0.42	-64
606	0.62	-102	5.9	77	0.011	141	0.40	-69
628	0.61	-104	5.8	72	0.013	137	0.38	-73
650	0.61	-107	5.7	69	0.013	131	0.36	-78
672	0.60	-109	5.7	65	0.016	130	0.34	-84
694	0.60	-112	5.6	61	0.016	132	0.31	-90
716	0.59	-115	5.5	57	0.017	129	0.29	-97
738	0.59	-118	5.5	53	0.019	128	0.27	-104
760	0.59	-121	5.3	48	0.021	123	0.24	-113
782	0.59	-124	5.3	44	0.021	122	0.22	-122
804	0.59	-126	5.1	40	0.022	120	0.21	-133
826	0.59	-129	5.0	36	0.024	118	0.19	-145
848	0.59	-132	4.9	31	0.026	116	0.18	-159
870	0.59	-135	4.8	26	0.027	112	0.17	-175
892	0.59	-138	4.6	22	0.028	108	0.18	169
914	0.59	-142	4.5	18	0.028	106	0.19	155
936	0.59	-144	4.3	14	0.028	106	0.20	142
958	0.59	-148	4.2	9	0.030	100	0.22	130
980	0.59	-151	4.0	4	0.031	99	0.24	120
1002	0.59	-153	3.8	0	0.031	95	0.26	111
1024	0.59	-157	3.6	-2	0.032	91	0.28	102
1046	0.59	-160	3.5	-6	0.032	86	0.30	95
1068	0.59	-164	3.3	-10	0.033	86	0.33	88
1090	0.59	-167	3.2	-14	0.033	81	0.35	82
1112	0.59	-170	3.0	-18	0.031	79	0.36	77
1134	0.58	-172	2.8	-22	0.030	46	0.38	72
1156	0.58	-175	2.7	-25	0.031	79	0.39	67
1178	0.57	-178	2.5	-28	0.031	74	0.41	63
1200	0.57	178	2.4	-31	0.029	72	0.42	59

Table 8. Typical S-Parameters of Mixer at 3V

Mixer		
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)
100	0.73	-11
122	0.73	-147
144	0.72	-16
166	0.72	-19
188	0.72	-21
210	0.71	-24
232	0.70	-27
254	0.70	-29
276	0.69	-32
298	0.68	-34
320	0.67	-37
342	0.66	-39
364	0.64	-42
386	0.63	—44
408	0.62	-46
430	0.61	-48
452	0.59	-50
474	0.58	-52
496	0.57	-53
518	0.56	-54
540	0.55	-56
562	0.55	-57
584	0.54	-59
606	0.54	-61
628	0.54	-62
650	0.54	-64

Mixer		
Freq (MHz)	$\|S_{11}\|$ (U)	$<S_{11}$ (deg)
672	0.54	-65
694	0.54	-67
716	0.54	-69
738	0.54	-71
760	0.54	-73
782	0.55	-76
804	0.55	-78
826	0.55	-80
848	0.55	-82
870	0.55	-85
892	0.56	-87
914	0.55	-90
936	0.56	-93
958	0.56	-96
980	0.56	-98
1002	0.56	-101
1024	0.57	-104
1046	0.57	-106
1068	0.57	-110
1090	0.57	-112
1112	0.57	-115
1134	0.57	-118
1156	0.57	-121
1178	0.57	-124
1200	0.57	-127

Low voltage GSM front-end transceiver SA1620

DESCRIPTION

The SA1620 is a combined receive (Rx) and transmit (Tx) front-end for GSM cellular telephones. The receive path contains two low noise amplifiers (LNA1 and LNA2) with four switchable attenuation steps. A Gilbert Cell mixer in the receive path down-converts the RF signal to a first IF of 70 to 500 MHz. A second Gilbert Cell in the transmit path transposes a GMSK or phase modulated IF to RF by image reject mixing and has a fixed IF of 400 MHz. A buffered LO signal is fed to Rx and Tx mixers. Rx or Tx path or the entire circuit may be powered-down.

FEATURES

- Excellent noise figure: <2dB for the LNAs at 950MHz
- LNAs matched to 50Ω with external matching components
- LNAs with gain control, 59dB dynamic range in four discrete steps
- LNA gain stability ±0.5dB within -40 to 85°C
- Feedthrough attenuation LNA1 to Rx mixer ≥ 35dB
- Tx power adjustable from -3 to +12dBm by external resistor
- Direct supply: 2.7V to 5.5V
- Battery supply voltage V_{BATT} = 3.3V to 7.5V or direct supply
- Two DC regulators programmable for 3.0V, 3.4V, 3.7V or 5.1V
- Low current consumption: 28mA for Rx or 59mA for Tx
- Fully compatible with SA1638 GSM IF Digital I/Q circuit

APPLICATIONS

- 900MHz front end for GSM hand-held units
- Portable radio, TDMA systems

PIN CONFIGURATION

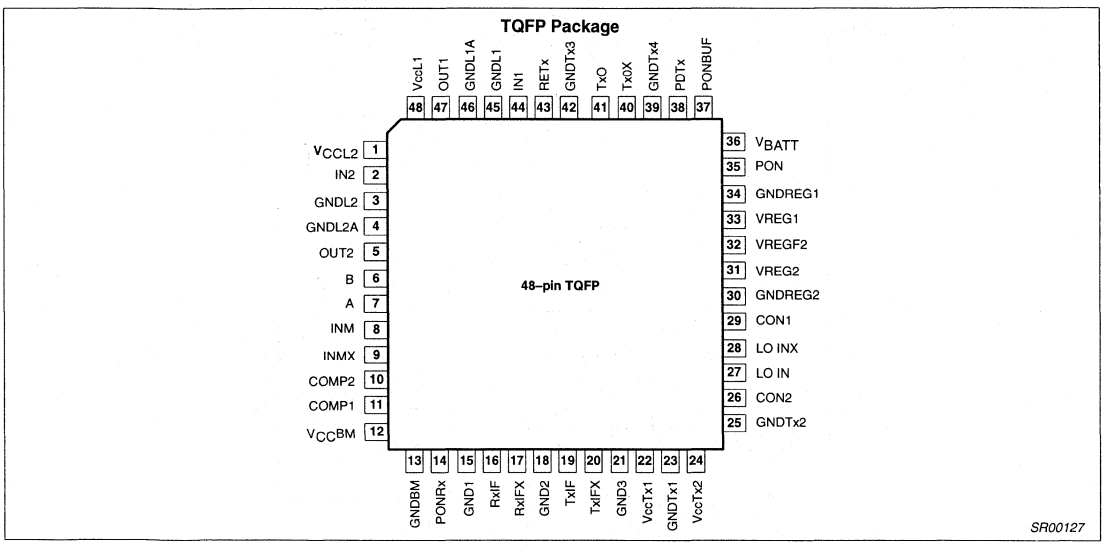


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (TQFP)	-40 to +85°C	SA1620BE	SOT313-2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	2.7 to 5.5	V
V_{BATT}	Battery voltage	3.3 to 7.5	V
T_A	Operating ambient temperature range	-40 to +85	°C

BLOCK DIAGRAM

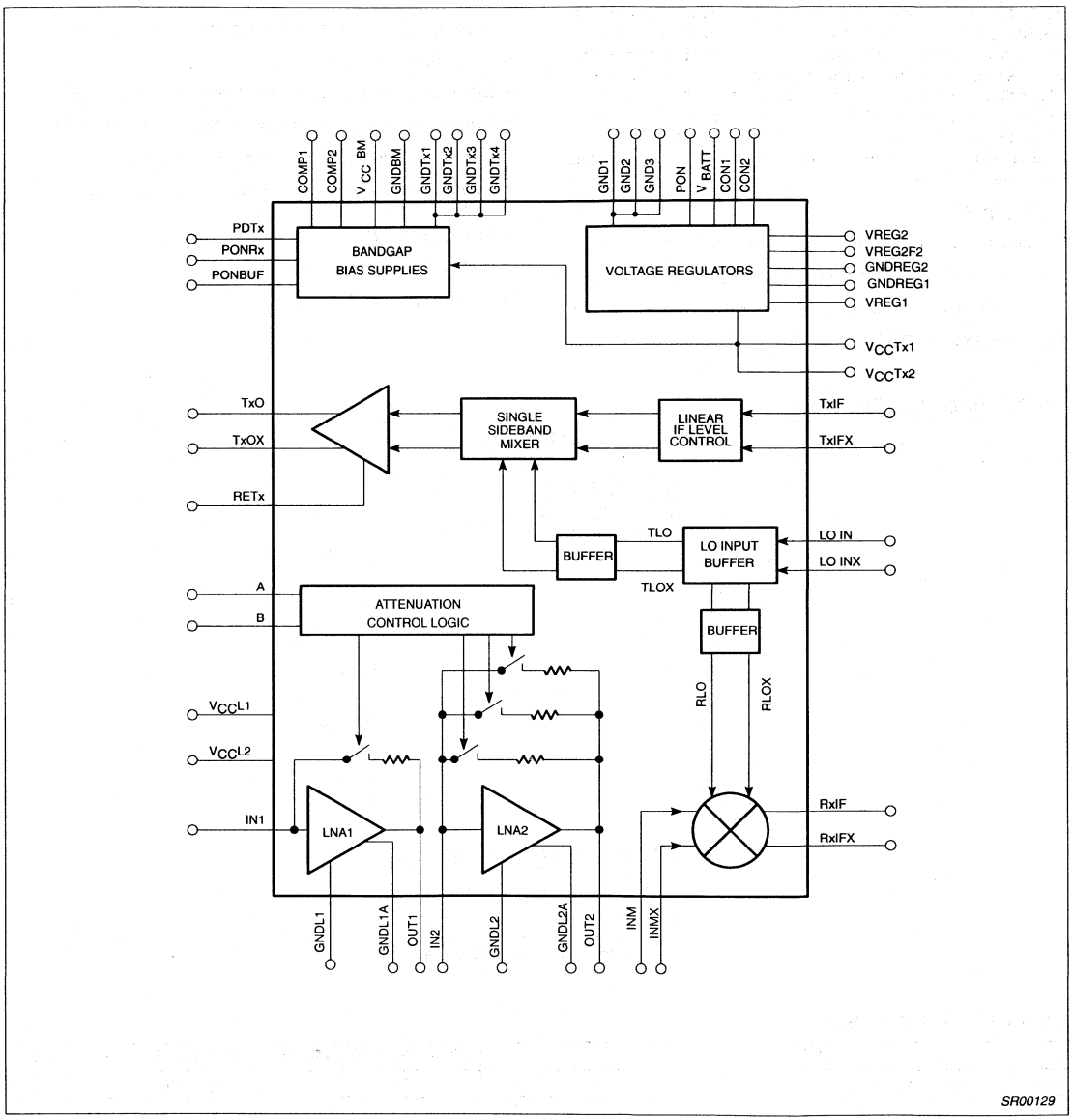


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
DC Regulators		
15	GND1	Ground of regulator supply
18	GND2	Ground of regulator supply
21	GND3	Ground of regulator supply
26	CON2	Control 2, voltage select for regulator 1 and 2
29	CON1	Control 1, voltage select for regulator 1 and 2
30	GNDREG2	Ground of regulator 2
31	VREG2	Output of regulator 2
32	VREG2F2	Feedback of regulator 2
33	VREG1	Output of regulator 1
34	GNDREG1	Ground of regulator 1
35	PON	Power-on input of regulators
36	V_{BATT}	Input of regulator 1 and 2
Rx Path		
1	$V_{CC}L2$	Positive supply for LNA2
2	IN2	Input LNA2
3	GNDL2	Ground L2 for LNA2
4	GNDL2A	Ground L2A for LNA2
5	OUT2	Output LNA2
6	B	Attenuation select B for LNA1 and LNA2
7	A	Attenuation select A for LNA1 and LNA2
8	INM	RF input for Rx mixer, open emitter
9	INMX	Inverse RF input for Rx mixer, open emitter
10	COMP2	Capacitor for bias stabilization
11	COMP1	Capacitor for bias stabilization
12	$V_{CC}BM$	V_{CC} for Rx Bias and Rx mixer
13	GNDBM	Ground for Rx Bias and Rx mixer
14	PONRx	Power on input for Rx bias supply
16	RxIF	IF output, open collector
17	RxIFX	Inverse IF output, open collector
44	IN1	Input to LNA1
45	GNDL1	Ground L1 for LNA1
46	GNDL1A	Ground L1A for LNA1
47	OUT1	Output LNA1
48	$V_{CC}L1$	Positive supply for LNA1
Tx Path		
19	TxIF	IF input for Tx
20	TxIFX	Inverse IF input for Tx
22	$V_{CC}Tx1$	Positive supply for Tx input
23	GNDTx1	Ground for Tx input
24	$V_{CC}Tx2$	Positive supply for LO and Tx input
25	GNDTx2	Ground for LO and Tx input
38	PDTx	Power down Tx input
39	GNDTx4	Ground for Tx output
40	TxOX	Inverse Tx output, open collector
41	TxO	Tx output, open collector
42	GNDTx3	Ground 1 for Tx output side
43	RETx	Reference resistor for Tx output current
Elements for Tx and Rx Path		
27	LO IN	Input for Local Oscillator signal
28	LO INX	Inverse input for LO or AC ground
37	PONBUF	Power on first stage LO input buffer and bias

NOTES:
1. Device is ESD sensitive. There are no ESD protection diodes at Pins 16, 17, 40 and 41. Thus, open-collector outputs may have increased DC voltage or higher AC peak voltage.
2. Pins 15, 18 and 21 are connected to each other and to a separate ground in REG1 and REG2.
3. Pins 23, 25, 42 and 39 are connected to each other and to the Tx path, LO buffer and associated bias supplies.
4. Pins 22 and 24 are connected to each other providing a sense input. They are also connected to the Tx path, LO buffer and associated bias supplies.
5. Pins 30 and 34 are not internally connected. They must be connected to external grounds.
6. Pins 48, 1, and 12 are not internally connected and have no ESD protection diodes between them. Power may be saved by connecting $V_{CC}L1$ and IN1 or $V_{CC}L2$ and IN2 to ground if LNA1 or LNA2 is not needed.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{BATT}	Battery voltage	-0.3 to +8.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CCXX}+0.3)	V
ΔV	V_{CC}Tx1,2 pins to V_{CC}BM	-0.3 to +1	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	800	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C
V_{TXO}, V_{TXOX}	Positive RF peak voltage at Tx outputs	6	V
V_{RXIF}, V_{RXIFX}	Positive IF peak voltage at Rx mixer outputs	6	V

NOTES:
1. Maximum junction temperature is determined by the power dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}. 48-pin TQFP: θ_{JA} = 67°C/W.

DC REGULATORS

Two low drop regulators (REG1 and REG2) are included on the chip and may be used to deliver the supply voltage of the main circuitry (e.g., 3V) out of the battery (at V_{BATT} = 3.3 to 7.5V) as shown in Figure 4 and in Table 1.

REG1 is intended to supply, at least, the internal functions of the SA1620. Both regulators may also be used for external circuitry. For this application, different voltages may be programmed as shown in Table 1.

The transmitter supply pins (V_{CC}Tx1,2) also operate as a sensor connection in the feedback loop of REG1 and must be externally connected to pin VREG1. For REG2, the sensor pin VREGF2 must be connected to VREG2.

All ground pins are internally bonded to the header except for pins GNDL1, GNDREG1 and GNDREG2.

When both regulators are not used, connect pins V_{BATT}, PON, CON1, CON2, VREG1, VREG2 and VREG2F2 to ground.

Table 1. DC Reg Output Voltage Control Pins

CON1	CON2	VREG1	VREG2	UNITS
L	L	3 ±5%	3 ±5%	V
L	H	3.4 ±5%	3.4 ±5%	V
H	L	3.7 ±5%	3.7 ±5%	V
H	H	5.1 ±5%	5.1 ±10%	V

NOTES:
1. Logic levels at CON1 and CON2:
   H – Open circuit. Pin must not be connected externally.
   Logic high level supplied on chip.
   L – Connected to ground.
2. Currents at CON1 and CON2:
   H – 0µA
   L (PON = H) – 50µA
   L (PON = L) – <1µA

Table 2. DC Regulators

SYMBOL	PARAMETER		RATING	UNITS
V_{BATT}	Common positive input voltage at both regulators		3.3 to 7.5	V
VREG1, VREG2	Output voltages of regulators 1 and 2		See Table 1	V
I_{INT1}	Internal current of REG1 in power-on mode		$4 + I_{VREG1}/10$	mA
I_{INT2}	Internal current of REG2 in power-on mode		$2.5 + I_{VREG2}/10$	mA
I_{INT01}, I_{INT02}	Internal current in power-down mode		<15	µA
$I_{VREG1MAX}$[5]	Max output current at VREG1		100	mA
$I_{VREG2MAX}$[5]	Max output current at VREG2		30	mA
C13[4]	Capacitor at pin VREG1		0.1 to 1000	µF
C14[4]	Capacitor at pin VREG2		0.1 to 500	µF
BW[6]	V_{BATT} = 3.3V, I_{REG1} = 0.1mA		0.03	kHz
	V_{BATT} = 3.3V, I_{REG1} = 100mA		60	
	V_{BATT} = 7.5V, I_{REG1} = 100mA		80	
F_{REG}[7]	f	≤100kHz	≤–61	dB
		10MHz	≤–32	
		100MHz	≤–37	
		400MHz	≤–48	

NOTES:
1. Power-on pin of Regulator 1 and 2: PON
2. Input currents at PON: <1µA. There are no pull-up or pull-down resistors.
3. Feedthrough attenuation from the logic input PON to the outputs VREG1 and VREG2: ≥40dB.
4. Recommended load capacitors: In every case C529 = C530 = 1µF to ground with series resistance ≤0.1Ω. Additional capacitor optional ≤1000µF with series resistance ≤5Ω.
5. At $T_j \geq 150°C$ a thermal switch reduces the output current.
6. Typical open loop bandwidths of regulator 1 at V_{REG1} = 3V and C529 = 1µF.
7. Feedthrough attenuation (at the indicated frequency f) from the input V_{BATT} to the outputs V_{REG1} and V_{REG2} at V_{BATT} = 3.3V, (CON1=CON2=L): F_{REG} (f) = V_{REG} (f) / V_{BATT} (f).

DC ELECTRICAL CHARACTERISTICS

V_{CCxxx} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Transmitter						
I_{VCC}	Total supply current	Transmit mode R_{546} = 240Ω		59		mA
R1	External resistor[1]			240		Ω
V_{R1}	Internal supply at pin RETx	V_{CC}Tx1,2 = 2.7V		0.43		V
		V_{CC}Tx1,2 = 5.5V		0.45		
I_{R1}	Current at pin RETx	R546 = 240Ω, V_{CC}Tx1,2 = 2.7V		1.7		mA
		R546 = 240Ω, V_{CC}Tx1,2 = 5.5V		1.8		
Low noise amplifiers						
I_{VCC}L1	Current at pin V_{CC}L1	G1hi mode	2.5	3.5		mA
I_{VCC}L2	Current at pin V_{CC}L2	G2hi mode	2.5	3.5		mA
Receiver						
I_{VCC}	Total supply current	Receive mode R_{546} = 240Ω		28		mA
Regulators						
Vreg1	Voltage @ 100mA load	Con1 Con2				
		L L	2.85	3.0	3.15	V
		L H	3.23	3.4	3.57	V
		H L	3.515	3.7	3.885	V
		H H	4.61	5.1	5.61	V
Vreg2	Voltage @ 30mA load	Con1 Con2				
		L L	2.85	3.0	3.15	V
		L H	3.23	3.4	3.57	V
		H L	3.515	3.7	3.885	V
		H H	4.61	5.1	5.61	V
Logic levels[2]						
V_{IH}	Logic 1 level	P_{ON}BUF, PDTx, P_{ON}Rx, A, B	2.0		V_{CCBM}[3]	V
V_{IH}	Logic 1 level	P_{ON}	2.0		V_{BAT}	V
V_{IL}	Logic 0 level		0		0.8	V
I_I	Input logic current				1	µA
C_{Ia}	Input logic capacitance			1.7		pF

NOTES:

1. The output current I_{TXO} + I_{TXOX} is adjustable by the external resistor R546. I_{TXO} + I_{TXOX} = 10 * I_{R546}, I_{R546} = V_{R1}/R546,
2. Thresholds are independent of supply voltages. Thus the SA1620 is compatible with SA1638 and with the power down inputs of usual external voltage regulators.
3. P_{ON} logic 1 max is V_{BAT}.

AC ELECTRICAL CHARACTERISTICS

V_{CCXX} = +3V, T_A = 25°C; RF = 940MHZ; IF=400MHz, f_{LO}=RF + IF; LO = -15dBm; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[1]					UNITS
			MIN[1]	-3σ	TYP	3σ	MAX[1]	
Low Noise Amplifier LNA1[2]								
S_{21}	Gain	G1hi mode		9.4	10	10.6		dB
		G1hi mode, RF = 1800MHz			-2.5			
		G1lo mode		-13	-12	-11		
	IP3	G1lo mode			28			
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	G1hi mode			0.003			dB/°C
		G1lo mode			0.0140			
$\Delta S_{21}/\Delta V_{CCL1}$	Gain/voltage sensitivity				0.1			dB/V
$\Delta S_{21}/\Delta f$	Gain frequency variation				0.01			dB/MHz
S_{12}	Reverse isolation	G1hi mode			-19			dB
S_{11}	Input match[3]	50Ω			-11			dB
S_{22}	Output match[3]	50Ω			-14			dB
P_{-1dB}	Input 1dB gain compression	G1hi mode		-15.5	-14	-12.5		dBm
IIP3	Input third order intercept			-5.5	-4	-2.5		dBm
IIP3/Δt	Input third order intercept				.011			dB/°C
NF	Noise figure				1.9			dB
t_{ON}	Turn-on time				7			µs
t_{OFF}	Turn-off time				0.5			µs
Low Noise Amplifier LNA2[2]								
S_{21}	Gain	G2hi mode		9	10	11		dB
		G2hi mode, RF = 1800MHz			-1.5			dB
		G2lo1 mode		-8.5	-7.5	-6.5		dB
		G2lo2 mode		-22.5	-21.5	-20.5		
		G2lo3 mode		-30	-28.5	-27		
	IP3	G2lo1 mode			18			
		G2lo2 mode			20			
		G2lo3 mode			25			
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	G2hi mode			0.003			dB/°C
		G2lo1,2,3 modes			0.014			
$\Delta S_{21}/\Delta V_{CCL2}$	Gain/voltage sensitivity				0.1			dB/V
$\Delta S_{21}/\Delta f$	Gain frequency variation				0.01			dB/MHz
S_{12}	Reverse isolation	G2hi mode			-24			dB
S_{11}	Input match[3]	50Ω			-13			dB
S_{22}	Output match[3]	50Ω			-15			dB
P_{-1dB}	Input 1dB gain compression	G2hi mode		-18	-16	-14		dBm
IIP3	Input third order intercept			-8	-6	-4		dBm
IIP3/Δt	Input third order intercept				.019			dB/°C
NF	Noise figure				2			dB
t_{ON}	Turn-on time				7			µs
t_{OFF}	Turn-off time				0.5			µs

AC ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[1]					UNITS
			MIN[1]	-3σ	TYP	3σ	MAX[1]	
Rx Mixer								
PG_C	Power conversion gain[5]			7.5	+8.5	9.5		dB
		RF = 1800MHz			-4			
$PG_C/\Delta T$	Gain temperature sensitivity							dB/°C
$PG_C/\Delta f$	Gain frequency variation							dB/MHz
S_{11}	Mixer input match at ports INM and INMX[4]				-13			dB
NF_M	SSB combined noise figure				10			dB
P_{-1dB}	Input 1dB compression				-7.3			dBm
IIP3	Input third order intercept			0	2	4		dBm
IIP3/Δt	Input third order intercept				.005			dB/°C
IIP2	Input second order intercept				19			dBm
G_{RFM-IF}	RF feedthrough	400MHz			-26			dB
$G_{LOfloor}$	LO floor feedthrough	400MHz			-30			dB
G_{LO-IF}	LO feedthrough to IF	1.3GHz			-16			dB
G_{LO-RFM}	LO to mixer input feedthrough	1.3GHz			-50			dBm
G_{LO-RF1}	LO to RF LNA1 input feedthrough	1.3GHz			-65			dBm
G_{LNA1-2}	LNA1 output to LNA2 input feedthrough	400MHz 1290-1760MHz			-41 -26			dB
G_{LNA2-M}	LNA2 output to mixer input feedthrough	1290-1760MHz			-23			dB
G_{LNA1-M}	LNA1 output to mixer input feedthrough	400MHz 1290-1760MHz			-50 -35			dB
Receiver[6]								
	Conversion gain	A,B Logic Level		–30		30		
		H,H	23.5	26.5	28.5	30.5	33.5	
		H,L	6	9	11	13	16	
		L,H	-8	-5	-3	-1	+2	
		L,L	-41	-36	-32	+28	-23	
	Input IP3 @ RFin=–40dBm	H,H		-20	-18	-16		
LO input								
Z_{IN}	Input impedance (each single-ended input)	1.3GHz			35-j97			Ω
P_{IN}	Input power				-15			dBm
A_{SAT}	Transistor saturation limit, max input amplitude				500			mV
Tx IF input								
$\|Z_{IN}\|$	Input impedance	400MHz			2			kΩ
P_{IN}	Input power				-20			dBm
Tx RF output								
P_{OUT}	R546 = 240Ω, V_{CC}Tx1,2 = 2.7V		5	7.5	8.5	9.5		dBm
	R546 = 240Ω, V_{CC}Tx1,2 = 5.5V			8.2	9.2	10.2		dBm

NOTES:

1. Due to our automatic test equipment accuracy and repeatability test limits may not reflect the ultimate device performance. Standard deviations are calculated from characterization data.
2. If the LNA1 is not needed, connect pin V_{CC}L1 and IN1 to GND. If the LNA2 is not needed, connect pin V_{CC}L2 and IN2 to GND.
3. Simple L/C elements are needed to achieve specified return loss.
4. The mixer RF inputs (emitters of a Gilbert Cell) may be driven by a symmetrical matching network.
5. Input symmetry suppression is such that the product 6*RF–4*LO is to be suppressed by at least 66dB relative to the wanted IF output when the input to the mixer is at –32dBm.
6. 0 db insertion less between LNA1 out to LNA2 in and LNA2out to mixer in.

Table 3. Power-Down and Tx/Rx Control Logic

No.	PONBUF	PDTX	PONRX	MODE	RESULT
1	H	H	L	Standby	LO buffer active, Tx and Rx path inactive
2	H	L	L	Transmit	LO buffer active, Tx path active, Rx path inactive (LNAs + mixer)
3	H	H	H	Receive	Tx path inactive, LO buffer and Rx path active (LNAs + mixer)
4	H	L	H	Calibrate	Tx path and Rx LNAs inactive, LO buffer and Rx mixer active
5	L	x	x	Power-Down	Tx- and Rx-path, LO buffers and Bias inactive

NOTES:
1. Logic levels of PONBUF, PDTx and PONRx: TTL, see DC Electrical Characteristics.
2. Logic levels / polarities are compatible with Philips Semiconductors Power Amp Controller PCA5075 and synthesizers UMA1019 or SA8025.
3. First stage of LO buffer and parts of bias supply are powered on by PONBUF.
4. Tx- or Rx-paths may be activated for special timeslots. Lines 1 and 4 show options to support DC offset calibrations at baseband mixers, following in the receiver chain (SA1638).

Table 4. Gain Control Logic for LNA1 and LNA2

INPUT		ATTENUATION STEP	GAIN		POWER CONSUMPTION	
a	b		LNA1	LNA2	LNA1	LNA2
H	H	0	G1hi	G2hi	on	on
H	L	1	G1hi	G2lo1	on	off
L	H	2	G1hi	G2lo2	on	off
L	L	3	G1lo	G2lo3	off	off

NOTES:
1. Logic levels of a and b: TTL
2. For values of G1hi and G1lo, G2hi, G2lo1, G2lo2 and G2lo3 see LNA1 and LNA2 AC Electrical Characteristics.

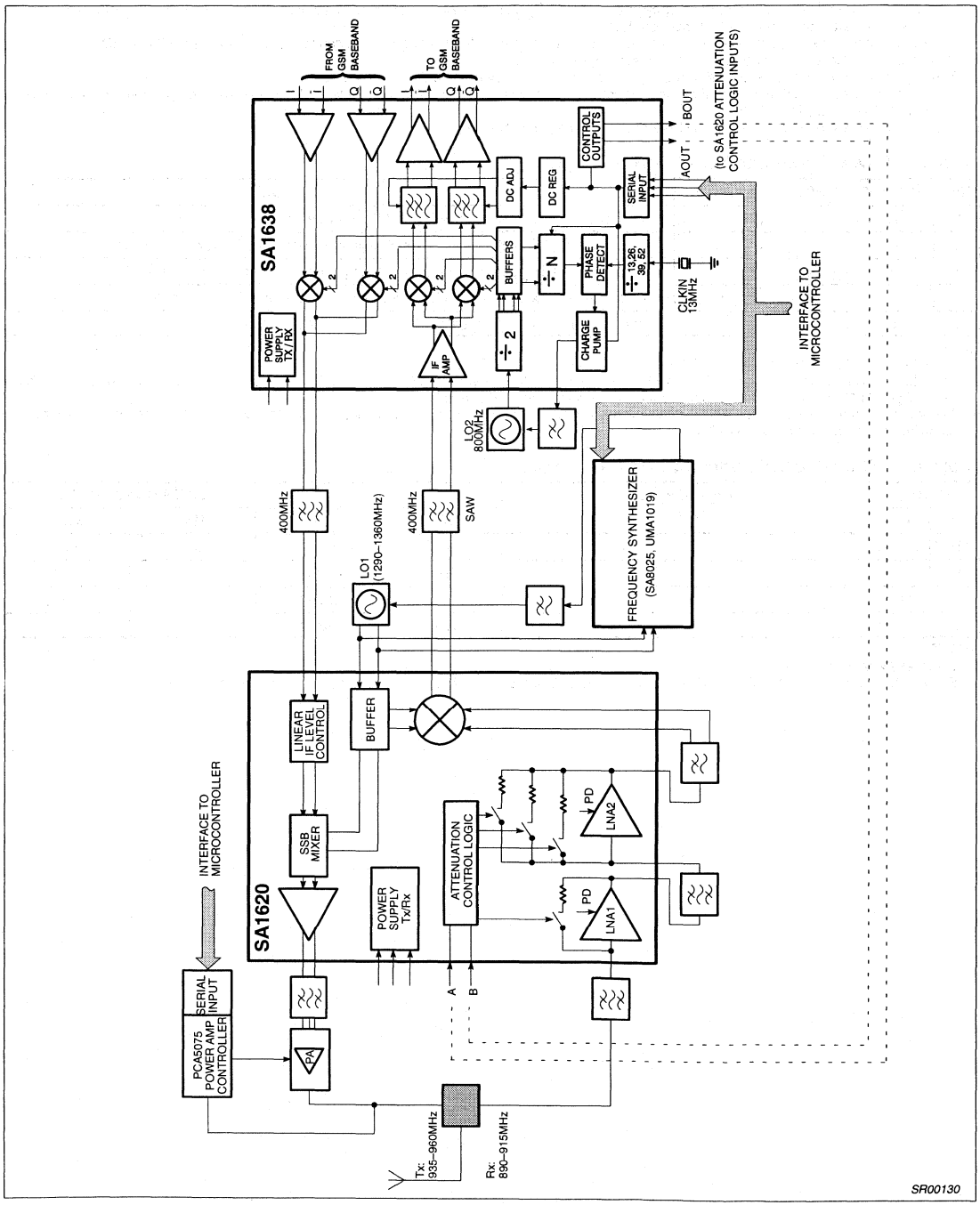

FROM GSM BASEBAND
TO GSM BASEBAND
SA1638
POWER SUPPLY TX/RX
IF AMP
÷ 2
BUFFERS
÷ N
PHASE DETECT
÷ 13,26, 39, 52
CHARGE PUMP
DC ADJ
DC REG
CONTROL OUTPUTS
SERIAL INPUT
AOUT
BOUT
(to SA1620 ATTENUATION CONTROL LOGIC INPUTS)
CLKIN 13MHz
INTERFACE TO MICROCONTROLLER
LO2 800MHz
400MHz
SAW
400MHz
LO1 (1290–1360MHz)
FREQUENCY SYNTHESIZER (SA8025, UMA1019)
SA1620
LINEAR IF LEVEL CONTROL
BUFFER
SSB MIXER
POWER SUPPLY Tx/Rx
ATTENUATION CONTROL LOGIC
PD
LNA2
PD
LNA1
A
B
INTERFACE TO MICROCONTROLLER
SERIAL INPUT
PCA5075 POWER AMP CONTROLLER
PA
Tx: 935–960MHz
Rx: 890–915MHz
SR00130

Figure 3.

Overview of Dual GSM/PCN Architecture

The SA1620 RF front-end and SA1638 IF transceivers form a dual conversion architecture which uses a common IF and standard I/Q baseband interface for both transmit and receive paths. This approach avoids the screening difficulties of direct modulation in the transmit direction and the mass production and practical performance issues related to direct conversion in the receive direction. The time division multiplex nature of the GSM system permits integration of the transmit and receive functions together on the one RF and one IF chips. This simplifies the distribution of local oscillator signals, maximizes circuitry commonality, and reduces power consumption.

The SA1620 and SA1638 allow considerable flexibility to optimize the transceiver design for particular price/size/performance requirements, through choice of appropriate RF and IF filters. The receive IF may be chosen freely in the range 70–500MHz, while the transmit IF is fixed to 400 MHz. The comparison frequency of the SA1638 PLL is high in order to provide fast switching time.

With suitable choice of the IF, an identical SA1638 IF receiver design can be used for both 900MHz GSM and 1800MHz PCN (DCS1800) equipment.

General Benefits/Advantages

- 2.7V operation. Compatible with 3V digital technology and portable applications. (Higher voltage operation also possible, if desired.)
- Excellent dynamic range. The availability of two LNAs allows flexibility in receiver dynamic design for portable and mobile GSM spec. applications with appropriate filters. If for a particular application a GaAs or discrete front-end is desired, one of the LNAs can be left unpowered. The placing of the AGC gains switches at the front means that for most of the time some attenuation will be inserted, further increasing typical dynamic performance beyond that specified by GSM.
- High power transmit output driver, delivering +8.5dBm output. This is sufficient to drive a filter and power amplifier input, without a driver amplifier. To avoid unnecessary current consumption the output power can be reduced, if not required, by appropriate choice of an external resistor.
- DC offsets generated in the receive channel are independent of the AGC setting, and correctable by software to prevent erosion of signal handling dynamic range by DC offsets. Independence of DC from AGC setting is achieved by putting the gain switches in the RF front-end.
- Minimal high-quality filter requirements. As a result of the integration in the SA1638 of high quality channel selectivity filters, only sufficient filtering is needed in the receive path to provide blocking protection for the second mixers. This reduces receiver cost and size.
- Operation at a high IF allows RF image reject filters to be relaxed. For example, at a 400MHz IF, the natural gain roll-off in the LNAs and mixer suppresses the image signal in the 1800MHz band by typically 28dB below the desired 900MHz band signal.

Receive Path

Multiple LNAs allow the flexibility to exploit the best choice of currently available filters (on performance, size, or cost grounds).

This approach is preferable to a single high-gain stage as the stray cross-coupling effects between pins remain manageable. In a single stage amplifier this would limit the amount of rejection of out-of-band signals that could be achieved, and would also limit the amount of AGC attenuation that could be practically implemented.

The LNAs are powered up only when PONBUF, PDTx and PONRx are high, to allow a high degree of battery economy. If greater sensitivity is required for an application, an external preamplifier circuit can be used instead of LNA1, and LNA1 left unconnected.

A special mode is provided with just the IF output related circuitry active in order to allow calibration of the DC offset at the SA1638 baseband receive outputs. This offset contains a contribution due to coupling effects between the second local oscillator and the IF circuitry, and therefore the receiver is set up in the receive state (but with incoming signals excluded) to allow accurate offset calibration.

Gain Control

Gain control is implemented in the SA1620 RF front-end. This avoids the disruption of the DC offset at the baseband IQ outputs that is typically caused by changes in the AGC. The SA1620 and SA1638 are designed so that the GSM dynamic range requirements can be met with the AGC remaining on the maximum gain setting.

These gain steps scale the dynamic range of the received signal (e.g., 90dB for GSM) into the dynamic range of the baseband processing device.

The absolute gain tolerances may be measured together with the attenuation tolerances of external filters during production of the receiver equipment. After software calibration switching from one dynamic range to another will cause only minor errors.

Tx Path

TXIF and TXIFX are differential IF inputs for phase modulated signals (e.g., GMSK). There is an IF level control loop which provides a constant amplitude to an image reject up mixer. Thus, this mixer operates linearly in the IF path, independent of IF level tolerances.

The single sideband up mixer is sufficient in quadrature to achieve the typical performance indicated in Table 6 over an IF range of 250 to 500MHz. The mixer is operating in switching mode by well matched 0° and 90° LO signals, optimized for 1.1 to 1.5GHz.

The Tx output stage operates in switching mode. Thus, parasitic AM at the IF is not transferred. The outputs TXO and TXOX may be used symmetrically or single-ended. Some spurious emissions will be very low when a symmetrical output signal is used.

$$P_{OUT} = R_e \left[6.25V \cdot (Z_{Pin\,40} + Z_{Pin\,41}) \cdot (I_{R546})^2\right]$$

according to Figure 4 and $I_{R546} = \frac{V_{R546}}{R_{546}}$ according to DC Electrical Characteristics. P_{OUT} is adjustable with R546 and is accurate to within ±1dB over the full voltage range 2.7 to 5.5V, and ±0.5dB from a given supply voltage. The absolute limit of the negative peak voltage swing at pins TxO and TxOX is $V_{SAT} = V_{CC}Tx1,2 - 1V$. The absolute limit of the positive peak voltage is +6V.

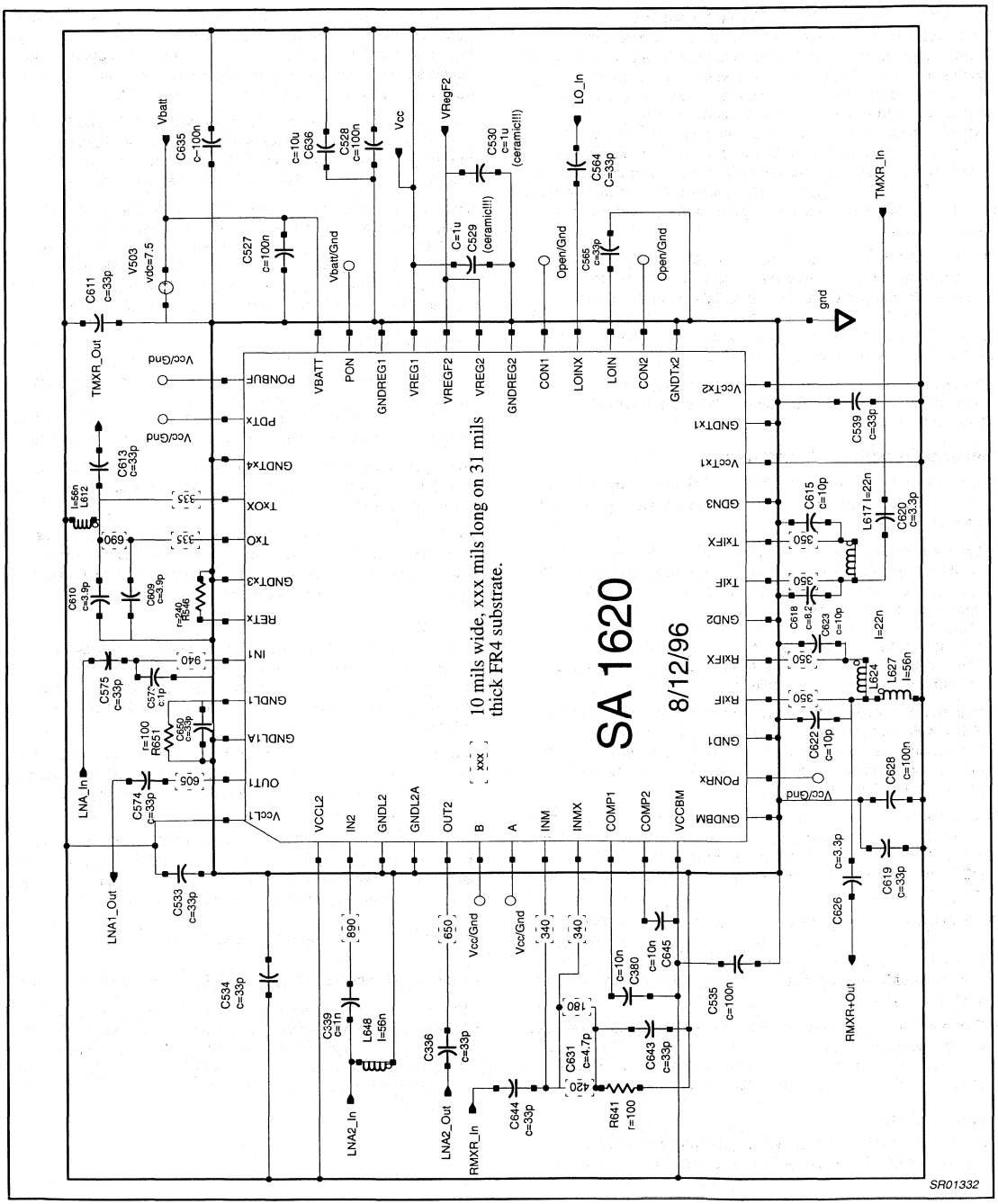


Figure 4. Application Circuit

APPLICATION CIRCUIT

LNA

Impedance Match: Intrinsic return losses at the input and output ports are 7dB and 11dB, respectively. However, since long and narrow traces are always needed to fan out the pins, the user can adjust the traces' dimensions so that only one shunt capacitor at the input is required to achieve excellent impedance match for both ports. If the user wants to skip the input matching network for simplicity, then roughly 0.7dB gain would be lost, although it benefits the system IP3.

Noise Match: The LNA1 and LNA2 can achieve 1.9dB and 2.0dB noise figure, respectively, when S11 = –11dB. Further improvement in S_{11} will slightly decrease NF and increase S_{21}.

Gain Control: The LNA1 can be switched to the attenuation mode, while LNA2 has three attenuation modes to choose from. When gain and loss modes from two LNAs are combined, there will be a total dynamic range of 59dB in the RF block; 3.0V operation is preferred to achieve better IP3 for both LNA1 and LNA2.

Temperature Compensation: Both LNAs have a built–in temperature compensation scheme to reduce the gain drift rate to 0.003dB/°C from –40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 2.7V to 5.5V.

Mixer

Mixer Input Match: The mixer is configured for best gain, noise figure and spurious response. The user must supply an external, patented resonant balun to provide the differential drive as well as the impedance match (embedded in). Because the mixer consists of two single–balance mixers, whose inputs are connected in parallel instead of in series, the differential and common–mode impedances are equal.

Output Match: The mixer output circuit also features an external, patented resonant balun to optimize the conversion gain and noise figure. The principal IF operating frequency is 400 MHz.

LO Drive: The internal buffer only requires –15dBm from an external source. Furthermore, the transmitter incorporates an integrated SSB upconverter that consists of narrowband phase shifters at 1300MHz (LO side) and 400MHz (IF side), so the LO frequency is recommended to be the receiver band plus 400MHz. Additionally, the LO leakage at the input of LNA1 is extremely low, which can greatly alleviate the LO re–radiation problem.

Outband Blocking: For optimum performance, passive R/C network is added at each input of the mixer. The resistors degenerate the noise conversion gain, while the capacitors preserve the gain and noise figure at RF frequencies.

Noise Figure and IP3: The resonant balun is superior to the conventional balun in terms of insertion loss, size and cost. As a result, the user can expect excellent SSB noise figure and gain which is 10dB and 8.5dB, respectively, at 400MHz IF. And the associated input IP3 is 2dBm typically. In the meantime, due to the internal LO buffer, the noise figure and IP3 are not sensitive to the LO levels. As discussed in the LNA Impedance Match session, a better system IP3 can be achieved (if necessary) through LNAs' gain reduction.

Transmitter

The resonant balun is applied again to maximize the gain and output power, for a given bias current. Typical output power is 8.5dBm when the input level exceeds –25dBm.

LO Input

The LO input is used in Tx- and in Rx-mode.

Only one synthesizer PLL is necessary to supply the LO input with different frequencies in Tx and Rx timeslots.

The LO input buffer should only be set in power-down mode together with the PLL. As further buffering is included on chip there will be no influence on the PLL in active mode when the SA1620 Rx- or Tx-path is power On or Off. Current consumption can thus be saved by powering on the Rx- and Tx-circuitry just before it is required, without disruption of the LO circuitry. LO input pins LO IN and LO INX may be used single-ended or symmetrically.

Table 5. GSM/DSC1800 Frequency Specification

(GSM 05.05, Version 4.2.0, April 1992) Mobile Stations Frequency Bands

	GSM	EGSM	DCS1800	Unit
Tx	890 to 915	880.2 to 915	1710 to 1785	MHz
Rx	935 to 960	925.2 to 960	1805 to 1880	MHz

Table 6. Measured Tx Output Frequency and Tx Mixer Products

IF=400MHz, symmetrical load at pins TxO, TxOX.

No.	SPECTRAL LINE f=n*IF+m*LO MHz					RELATIVE POWER OF SPECTRAL LINE			REMARKS
	LO = 1280MHz	LO = 1300MHz	LO = 1315MHz	Order					
				n	m	min dBc	typ dBc	max dBc	
1	80	100	115	–3	1		–70		
2	160	200	230	–6	2		–76		
3	320	300	285	4	–1		–60		
4	400	400	400	1	0		–46		IF
5	480	500	515	–2	1		–31		
6	560	600	630	–5	2		–62		
7	720	700	685	5	–1		–56		
8	800	800	800	2	0		–37		2)
9	880	900	915	–1	1		0		1)
10	960	1000	1030	–4	2		–46		3)
11	1020	1100	1185	6	–1		–63		
12	1200	1200	1200	3	0		–60		
13	1280	1300	1315	0	1		–32		LO
14	1360	1400	1430	–3	2		–46		
15	1440	1500	1545	–6	3		–64		
16	1600	1600	1600	4	0		–75		
17	1680	1700	1715	1	1		–50		4) 5)
18	1760	1800	1830	–2	2		–34		3)
19	1840	1900	1945	–5	3		–68		3)
20	2000	2000	2000	5	0		–77		
21	2080	2100	2115	2	1		–74		
22	2160	2200	2230	–1	2		–67		
23	2240	2300	2345	–4	3		–59		
24	2400	2400	2400	6	0		–75		
25	2480	2500	2515	3	1		–76		
26	2560	2600	2630	0	2		–70		2LO

NOTE:
1. Desired Tx output frequency LO–IF corresponding to EGSM Tx band in Table 5.
2. (LO+IF)–(LO–IF) = 2 * IF
3. See Rx bands in Table 5
4. LO+IF = mixer image frequency
5. See Tx bands in Table 5

Table 7. Measured Tx Output Noise Floor

Frequency MHz		dBc/Hz			REMARKS
		MIN	TYP	MAX	
< 860			–135		
860 to 880			–134		
880.2 to 890			–133		EGSM TX extension
890 to 915			–133		GSM TX
915 to 925			–133		
925.2 to 935			–134		EGSM RX extension
935 to 960			–135		GSM RX
960 to 1000			–135		
1000 to 1710			–135		
1710 to 1785			–146		DCS1800 TX
1785 to 1805			–145		
1805 to 1880			–144		DCS1800 RX
1880 to 12750			–147		
>12750			tbd		
Adjacent Channel			–130		

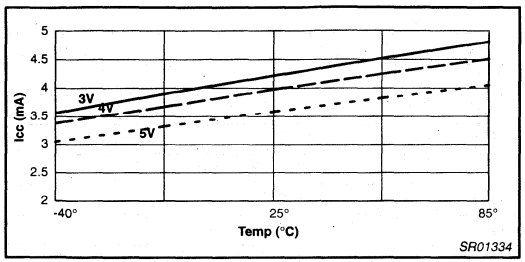


Figure 5. LNA1_ICC vs. Temp

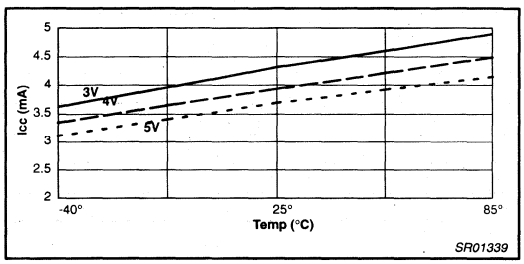


Figure 6. LNA_2 ICC vs. Temp

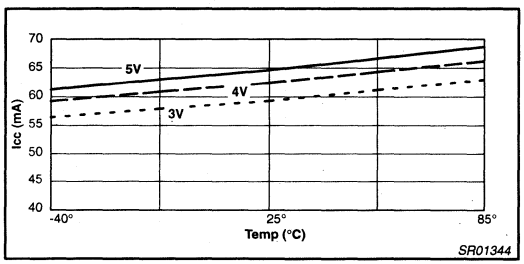


Figure 7. Transmit_ICC vs. Temp

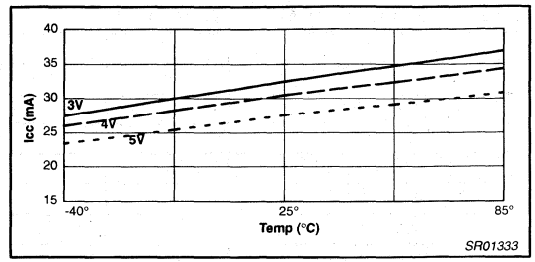


Figure 8. Receive ICC vs. Temp

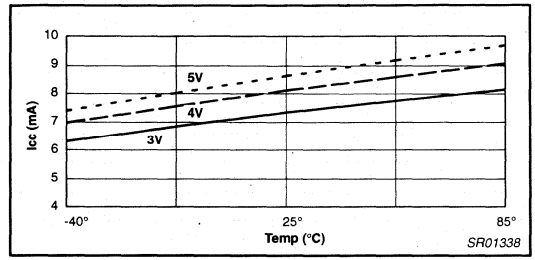


Figure 9. Standby_ICC vs. Temp

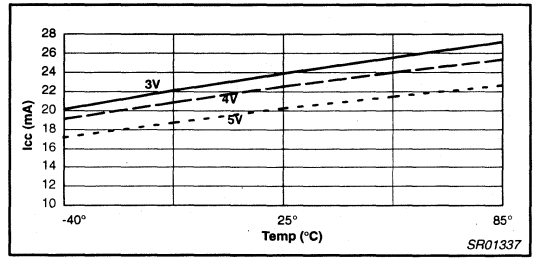


Figure 10. Calibrate_ICC vs. Temp

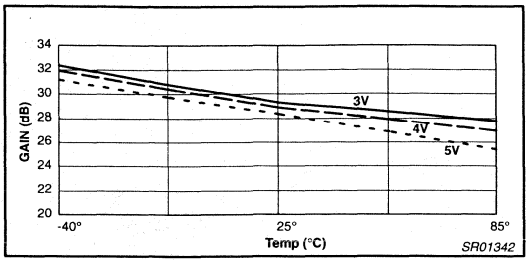


Figure 11. Receive_Gain Mode1 vs. Temp

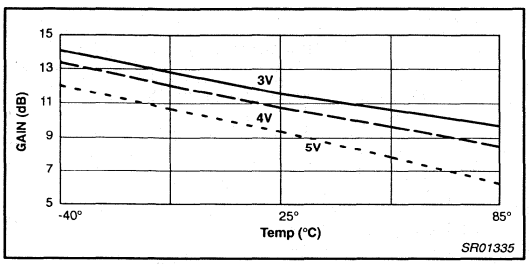


Figure 12. Receive_Gain_Mode2 vs. Temp

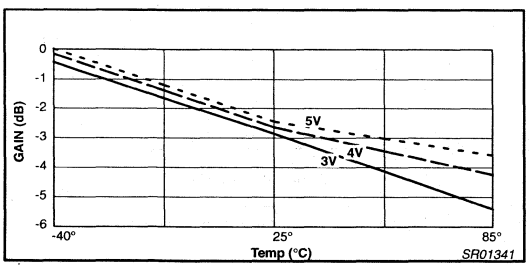


Figure 13. Receive_Gain_Mode3 vs. Temp

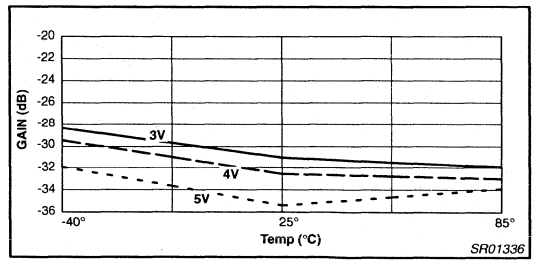


Figure 14. Receive_Gain_Mode4 vs. Temp

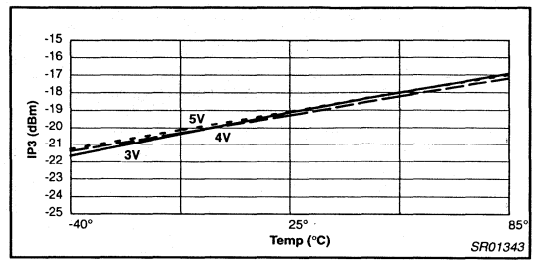


Figure 15. Receive IIP3 vs. Temp

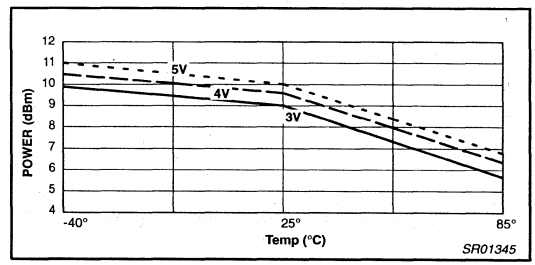


Figure 16. Transmit_Power_20 vs. Temp

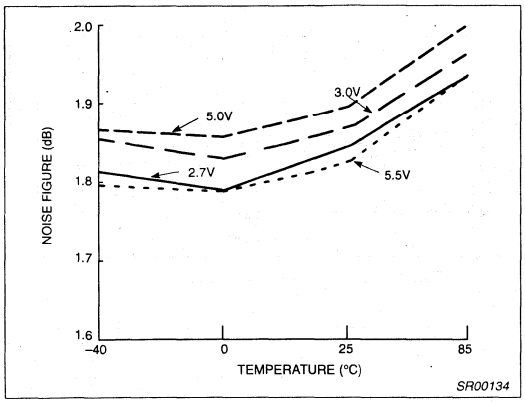


Figure 17. Receive LNA1 Noise Figure

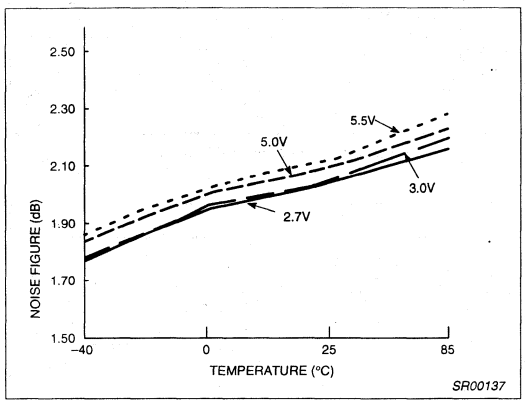


Figure 18. Receive LNA2 Noise Figure

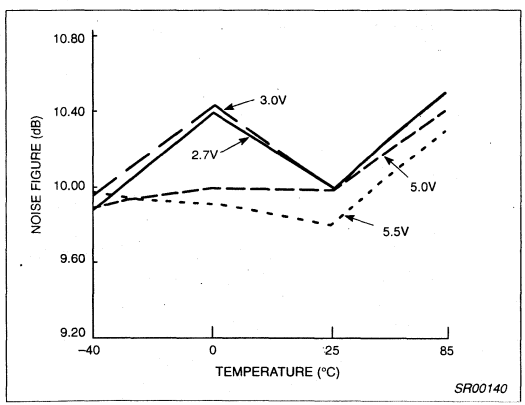


Figure 19. Receive Mixer Noise Figure

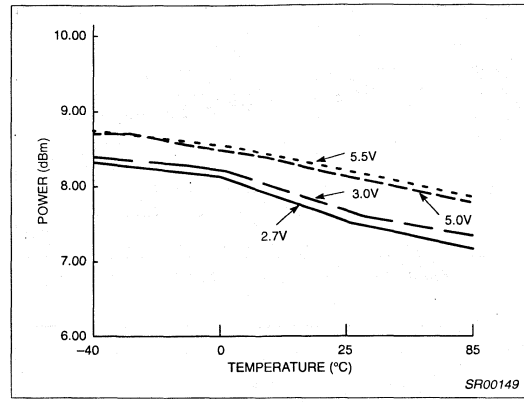


Figure 20. Transmit Power @ -25dBm

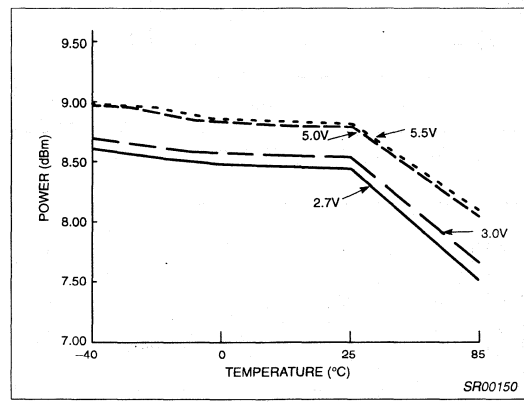


Figure 21. Transmit Power @ -15dBm

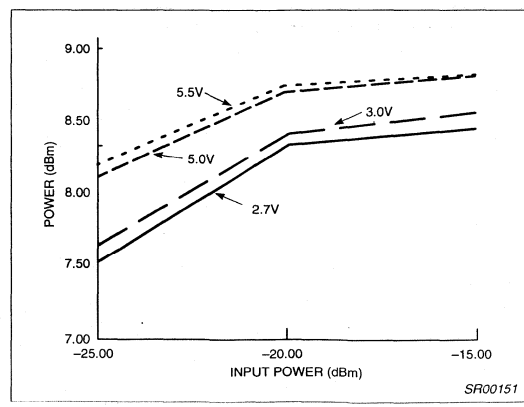


Figure 22. Transmit Power @ 25°C

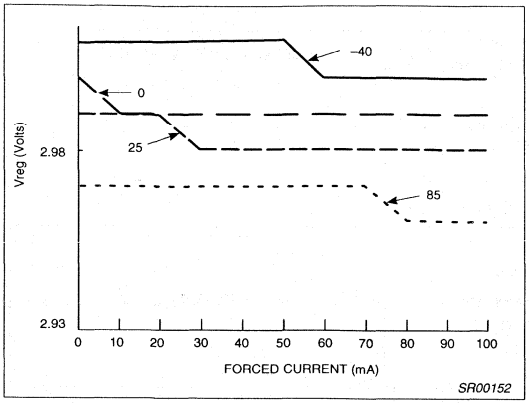


Figure 23. Regulator 1 Load Regulation (V_{BAT} = 3.5V)

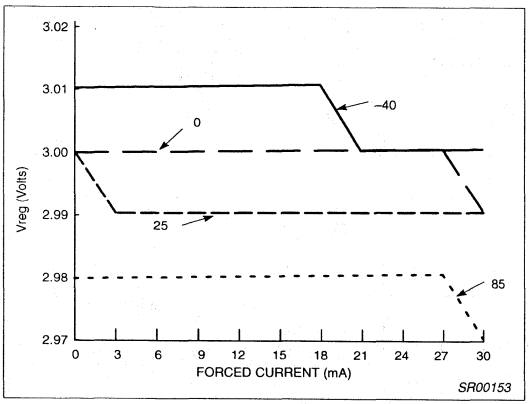


Figure 24. Regulator 2 Load Regulation (V_{BAT} = 3.5V)

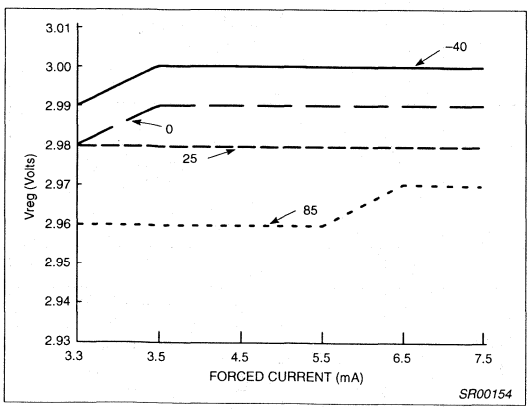


Figure 25. Regulator 1 Line Regulation @ 100mA Load

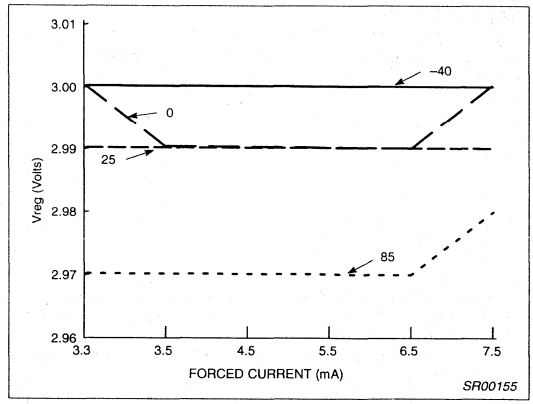


Figure 26. Regulator 2 Line Regulation @ 30mA Load

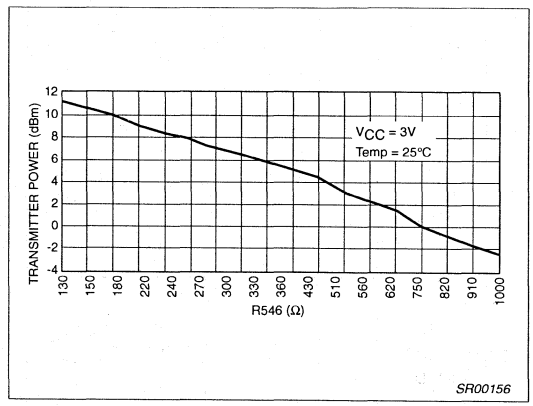


Figure 27. Transmit Output Power vs R(546) @ V_{CC} = 3V

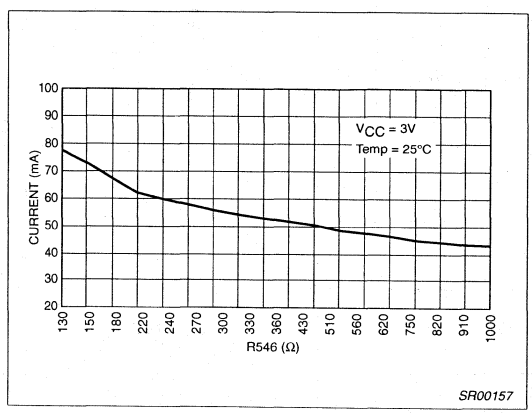
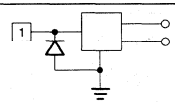
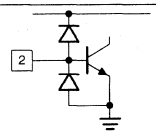
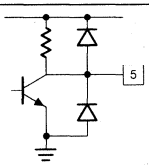
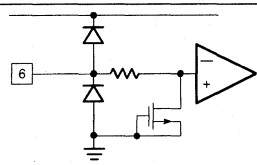
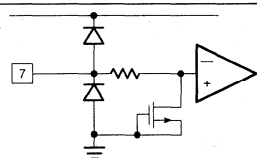
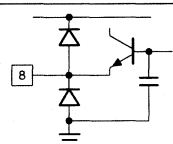
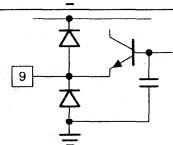
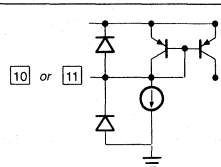


Figure 28. Transmit Mode Current vs R(546) @ V_{CC} = 3V

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	V_{CC}	3.0	
2	IN2	0.8	
3	GNDL2	0.0	
4	GNDL2a	0.0	
5	OUT2	2.2	
6	B CMOS INPUT		
7	A CMOS INPUT		
8	INM	0.4	
9	INMX	0.4	
10	COMP2	2.2	
11	COMP1	2.2	

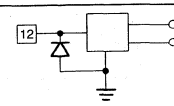
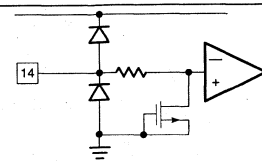
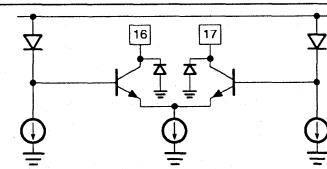
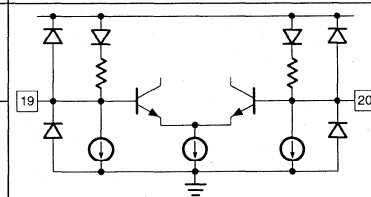
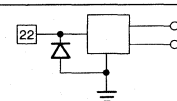
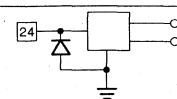
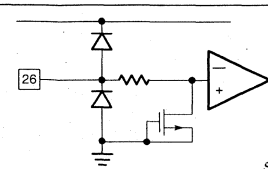
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
12	$V_{CC}BM$	3.0	
13	GND	0.0	
14	POnRx CMOS INPUT		
15	GND	0.0	
16	Rxif	3.0	
17	RxifX	3.0	
18	GND	0.0	
19	Txif	2.2	
20	TxifX	2.2	
21	GND	0.0	
22	$V_{CC}Tx$	3.0	
23	GND	0.0	
24	$V_{CC}Tx$	3.0	
25	GND	0.0	
26	CON2 CMOS INPUT		

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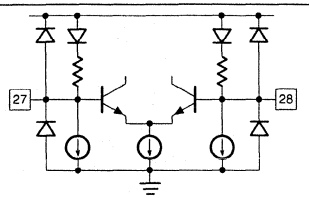
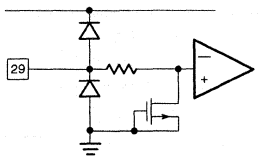
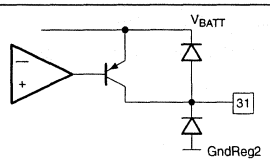
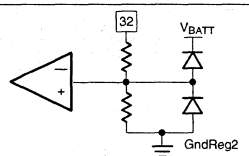
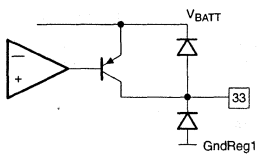
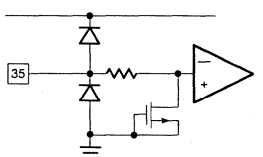
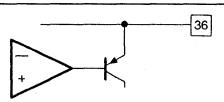
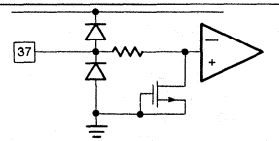
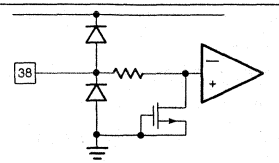
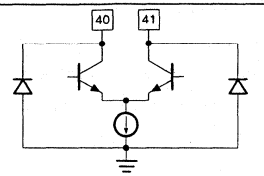
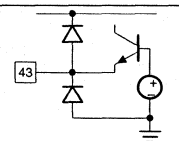
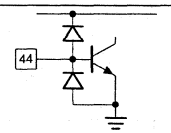
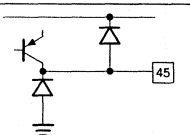
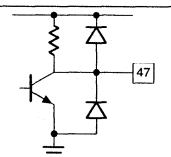
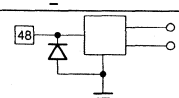
Figure 29. Pin Functions

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
27	LOin	2.2	
28	LOinX	2.2	
29	CON1 CMOS INPUT		
30	GndReg1	0.0	
31	VReg2	3.0	
32	VRegF2	3.0	
33	VReg1	3.0	
34	GndReg1	0.0	
35	POn CMOS INPUT		
36	V_{BATT}	3.0	

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
37	POnBuf CMOS INPUT		
38	PDTx CMOS INPUT		
39	GndTx	0.0	
40	TxOx	3.0	
41	TxO	3.0	
42	GndTx	0.0	
43	RETx	0.4	
44	IN1	0.8	
45	GndL1	0.0	
46	GndTx	0.0	
47	OUT1	2.2	
48	$V_{CC}L1$	3.0	

SR00163

Figure 30. Pin Functions

2.45GHz low voltage RF transceiver | SA2420

DESCRIPTION

The SA2420 transceiver is a combined low-noise amplifier, receive mixer, transmit mixer and LO buffer IC designed for high-performance low-power communication systems for 2.4-2.5GHz. The LNA has a 2.5dB noise figure at 2.4GHz with 14dB gain and an IP3 intercept of -6dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over the -40 to +85°C temperature range. The wide-dynamic-range receive mixer has a 11dB noise figure and an input IP3 of -1dBm at 2.4GHz. The nominal current drawn from a single 3V supply is 34mA in transmit mode and 21mA in receive mode.

FEATURES

- Low current consumption: 34mA nominal transmit mode and 21mA nominal receive mode
- Fabricated on a high volume, rugged BiCMOS technology
- High system power gain: 22dB (LNA + Mixer) at 2.45GHz
- TSSOP24 package
- Excellent gain stability versus temperature and supply voltage
- -10dBm LO can be used to drive the mixer
- Operates with either full or half frequency LO
- Wide IF range: 50–500MHz
- ESD protected

PIN CONFIGURATION

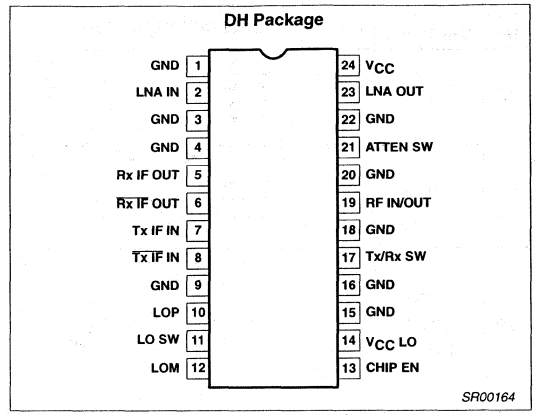


Figure 1. Pin Configuration

APPLICATIONS

- 2.45GHz WLAN front-end (802.11, ISM)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Thin Shrink Small Outline Package (Surface-mount, TSSOP)	-40 to +85°C	SA2420DH	SOT355-1

BLOCK DIAGRAM

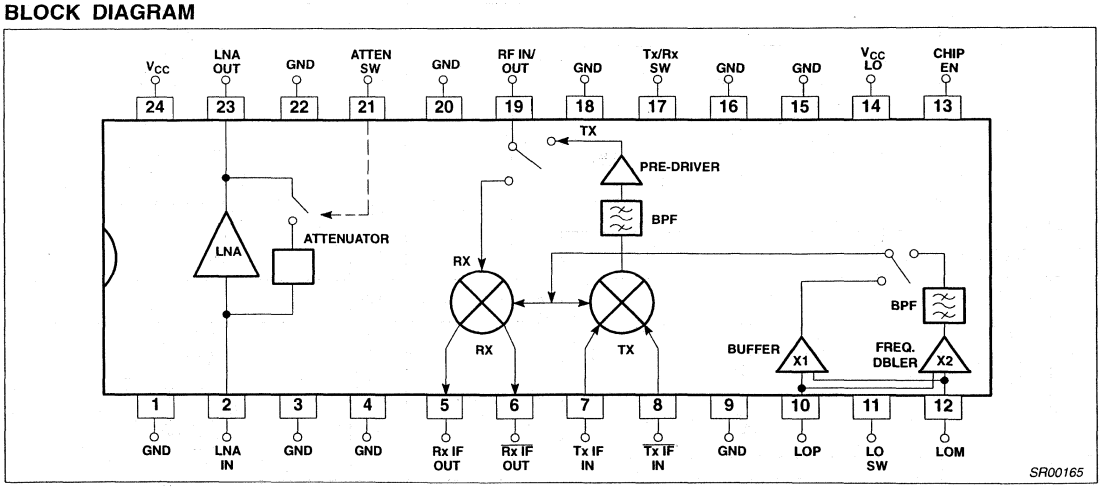


Figure 2. SA2420 Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 24-Pin Plastic TSSOP	555	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power (RF/IF/LO pins)	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage the product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,
   θ_{JA}: 24-Pin TSSOP = 117°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-3σ	TYP	+3σ	MAX	
I_{CCTX}	Supply current, Transmit	LO mode = Hi	25		34		42	mA
I_{CCRX}	Supply current, Receive	LO mode = Hi	15		21		26	mA
$I_{CC\ OFF}$	Power down mode (Tx/Rx SW = Low)	LO mode = Hi, LNA gain = Hi			0		10	µA
$V_{LNA\text{-}IN}$	LNA input voltage	Receive mode			0.855			V
$I_{LNA\text{-}OUT}$	LNA output bias current	Receive mode			4.0			mA
$V_{LO\ 2.1}$	LO buffer DC input voltage	LO mode = Hi			2.1			V
$V_{LO\ 1.05}$	LO buffer DC input voltage	LO mode = Low			2.1			V
$V_{TX\ IF}$	Tx Mixer input voltage	Transmit mode			1.7			V
$V_{TX\ IFB}$	Tx Mixer input voltage	Transmit mode			1.7			V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; LO_{IN} = -10dBm @ 2.1GHz; f_{RF} = 2.45GHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-3σ	TYP	+3σ	MAX	
Low Noise Amplifier (In = Pin 2; Out = 23)								
S_{21}	Amplifier gain	LNA gain = Hi			14.0			dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	LNA gain = Hi			-0.002			dB/°C
$\Delta S_{21}/\Delta V_{CC}$	Gain V_{CC} drift	LNA gain = Hi			0.3			dB/V
S_{12}	Amplifier reverse isolation	LNA gain = Hi			-22			dB
S_{11}	Amplifier input match[1]	LNA gain = Hi			-10			dB
S_{22}	Amplifier output match[1]	LNA gain = Hi			-10			dB
ISO	Isolation: LO_1 to LNA_{IN}	LO mode = Hi, LNA gain = Hi			-45			dB
P_{-1dB}	Amplifier input 1dB gain compression	LNA gain = Hi			-17			dBm
IP3	Amplifier input third order intercept	$f_1 - f_2$ = 1MHz, LNA gain = Hi			-6			dBm
NF	Amplifier noise figure (50Ω)	LNA gain = Hi			2.5			dB
LNA High Overload Mode								
S_{21}	Amplifier gain	LNA gain = Low			-8			dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	LNA gain = Low			-0.01			dB/°C
$\Delta S_{21}/\Delta V_{CC}$	Gain V_{CC} drift	LNA gain = Low			0.3			dB/V
S_{12}	Amplifier reverse isolation	LNA gain = Low			-16			dB
S_{11}	Amplifier input match[1]	LNA gain = Low			-8			dB
S_{22}	Amplifier output match[1]	LNA gain = Low			-8			dB
ISO	Isolation: LO_1 to LNA_{IN}	LO mode = Hi, LNA gain = Low			-45			dB
P_{-1dB}	Amplifier input 1dB gain compression	LNA gain = Low			5			dBm
IP3	Amplifier input third order intercept	$f_1 - f_2$ = 1MHz, LNA gain = Low			13			dBm
NF	Amplifier noise figure (50Ω)	LNA gain = Low			17			dB
Rx Mixer (RF = Pin 19, IF = Pins 5 and 6, LO = Pin 10 or 12, P_{LO} = -10dBm)								
PG_C	Power conversion gain into 50Ω : external matching to balun	f_S = 2.45GHz, f_{LO} = 2.1GHz, f_{IF} = 350MHz			8			dB
$\Delta G_C/\Delta T$	Gain temperature drift				-0.016			dB/°C
$\Delta G_C/\Delta V_{CC}$	Gain V_{CC} drift				0.34			dB/V
S_{11-RF}	Input match at RF (2.45GHz)[1]				-15			dB
NF_M	SSB noise figure (2.45GHz) (50Ω)				11			dB
P_{-1dB}	Mixer input 1dB gain compression				-10			dBm
IP3	Input third order intercept	$f_1 - f_2$ = 1MHz			+1			dBm
IP_{2INT}	Mixer input second order intercept				TBD			dBm
f_{RF}	RF frequency range		2.2		2.45		2.7	GHz
f_{IF}	IF frequency range		50		350		500	MHz

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-3σ	TYP	+3σ	MAX	
Rx Mixer Spurious Components (P_{IN} = P_{-1dB})								
P_{RF-IF}	RF feedthrough to IF	C_L = 2pF per side			-35			dBc
P_{LO-IF}	LO feedthrough to IF	C_L = 2pF per side			-35			dBc
Tx Mixer (RF = Pin 19, IF = Pins 7 and 8, LO = Pin 10 or 12, P_{LO} = -10dBm)								
PG_C	Power conversion gain: R_L = 50Ω R_S = 50Ω	f_S = 2.45GHz, f_{LO} = 2.1GHz, f_{IF} = 350MHz			18			dB
$\Delta G_C/\Delta T$	Gain temperature drift				-0.007			dB/°C
$\Delta G_C/\Delta V_{CC}$	Gain voltage drift				0.4			dB/V
S_{11-RF}	Output match at RF (2.45GHz)[1]				-10			dB
NF_M	SSB noise figure (2.45GHz) (50Ω)				12			dB
P_{-1dB}	Output 1dB gain compression				+3			dBm
IP3	Output third order intercept	$f_1 - f_2$ = 1MHz			+10			dBm
IP_{2INT}	Output second order intercept				TBD			dBm
f_{RF}	RF frequency range		2.2		2.45		2.7	GHz
f_{IF}	IF frequency range		50		350		500	MHz
Tx Mixer Spurious Components (P_{OUT} = P_{-1dB})								
P_{IF-RF}	IF feedthrough to RF				-29			dBc
P_{LO-RF}	LO feedthrough to RF				-22			dBc
P_{2LO-RF}	2*LO feedthrough to RF				-25			dBc
$P_{IMAGE-RF}$	Image feedthrough to RF				-4			dBc
LO Buffer: Full and Half Frequency inputs								
P_{LO}	LO drive level		-10		-7		5	dBm
S_{11-LO1}	Mixer input match (LO = 2.1GHz)	LO mode = Hi			-11			dB
S_{11-LO2}	Mixer input match (LO = 1.05GHz)	LO mode = Low			-11			dB
f_{LO2G}	LO2G frequency range	LO mode = Hi	1.9		2.1		2.3	GHz
f_{LO1G}	LO1G frequency range	LO mode = Low	0.85		1.05		1.25	GHz
Switching[2]								
t_{Rx-Tx}	Receive-to-transmit switching time				1			µs
t_{Tx-Rx}	Transmit-to-Receive switching time				1			µs
$t_{POWER\ UP}$	Chip enable time				1			µs
$t_{PWR\ DWN}$	Chip disable time				1			µs

NOTES:
1. With simple external matching
2. With 50pF coupling capacitors on all RF and IF ports

Table 8. Truth Table

Chip-En	TxRx-SW	LNA-SW	LO-SW	Mode	LNA Gain	LO Freq. (Typ)
0	X	X	X	Sleep	N/S	N/S
1	0	1	1	Receive	+14dB	2.1GHz
1	0	0	1	Receive	-8dB	2.1GHz
1	0	1	0	Receive	+14dB	1.05GHz
1	0	0	0	Receive	-8dB	1.05GHz
1	1	X	1	Transmit	N/S	2.1GHz
1	1	X	0	Transmit	N/S	1.05GHz

FUNCTIONAL DESCRIPTION

The SA2420 is a 2.45GHz transceiver front-end available in the TSSOP-24 package. This integrated circuit (IC) consists of a low noise amplifier (LNA) and up- and down-converters. The injection of the local oscillator (LO) signal has two options: 1) direct injection of the LO signal at approximately 2GHz, or 2) injection of an LO signal at approximately 1GHz through an on-chip doubler. The SA2420 functions with a supply voltage range of 3 – 5 V (nominally). There is an enable/disable switch available to power up/down the entire chip in 1µs, typically. This transceiver has several unique features.

The LNA has two operating modes: 1) high gain mode with a gain = +14dB; and 2) low gain mode with a gain <-10dB. The switch for this option is internal and is controlled externally by high and low logic to the pin. When the LNA is switched into the attenuation mode, active matching circuitry (on-chip) is switched in (reducing the number of off-chip components required). The input and output are internally matched to 50Ω. To reduce power consumption when the chip is transmitting, the LNA is automatically switched into a "sleep" mode (internally) without the use of external circuitry.

The up and down frequency converters are single-ended at the RF port of the mixers. The up and down converters share the same (RF) pin and use an internal switch for transmitting (up-converting) or receiving (down-converting) modes. The switch is controlled externally by high and low logic states. The RF port is matched to 50Ω and has an input IP3 of +1dBm (mixer only). The down-convert mixer is buffered and has open collectors at the pins to allow for matching to common SAW filters. The up-convert mixer has differential inputs (IF port) and single-ended output (RF port), with an input pin to output pin gain of 18dB. The output of the up-converter is designed for a power level = +3dBm (P_{-1dB}). The mixers are fed by the two LO options.

The available LO options are: direct injection (2.1GHz at the pin) or through an on-chip doubler. The doubler has a simple LC bandpass filter (internal) at its output which passes the second harmonic to the mixers. Through an internal switch (controlled externally), either LO can be used depending on the designer's application. If an application requires the use of a 1.05GHz VCO, then the doubler option would be used to double the frequency (2 × 1.05GHz = 2.1GHz) before being injected into the mixers. For a 2.1GHz VCO, the direct option would be used. With this option, the signal passes through an on-chip buffer and is then injected into the mixers.

Image reject 1 800 MHz transceiver for DECT applications

UAA2067G

FEATURES

- Receiver with:
  - low noise amplifier
  - dual quadrature mixers for image rejection (lower sideband)
  - I and Q combining networks at a fixed IF
- Both high-frequency and low-frequency VCOs including buffers with good isolation for low pulling
- Transmitter with:
  - dual quadrature mixers for image rejection (lower sideband)
  - amplitude ramping circuit
  - amplifier with high output power.

APPLICATIONS

- 1800 MHz transceiver for DECT hand-portable equipment
- TDMA systems.

GENERAL DESCRIPTION

The UAA2067G is a low-power transceiver intended for use in portable and base station transceivers complying with the DECT system. The IC performs in accordance with specifications in the −30 to +85°C temperature range.

The UAA2067G contains a front-end receiver for the 1800 to 1900 MHz frequency range, a high-frequency VCO for the 1650 to 1850 MHz range, a low-frequency VCO for the 100 to 140 MHz frequency range and a transmitter with a high-output power amplifier driver stage for the 1800 to 1900 MHz frequency range. Designed in an advanced BiCMOS process, it combines high performance with low-power consumption and a high degree of integration, thus reducing external component costs and total radio size.

Its first advantage is to provide typically 34 dB of image rejection in the receiver path. Thus, the image filter between the LNA and the mixer is redundant and consequently can be removed. The receive section consists of a low-noise amplifier that drives a quadrature mixer pair. Image rejection is achieved by this RF mixer pair and the two phase shifters in the I and Q channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

Signals presented at the RF input at LO − IF frequency are rejected through this signal processing while signals at LO + IF frequency can form the IF signal.

Its second advantage is to provide a good buffered high-frequency VCO signal to the RX and TX mixers and to the synthesizer-prescaler. Switching the receive or transmit section **on** gives a very small change in VCO frequency.

Its third advantage is to provide a good buffered low-frequency VCO signal to the TX mixers, to the synthesizer-prescaler and the second down conversion mixer in a double conversion receiver. Switching the transmit section **on** gives a very small change in VCO frequency.

The frequency of each VCO is determined by a resonator network that is external to the IC. Each VCO has a regulated power supply voltage that has been designed specifically for minimizing a change in frequency due to changes in the power supply voltage, which may be caused for instance by switching **on** the power amplifier.

Its fourth advantage is to provide typically 33 dBc of image rejection in the single-sideband up-conversion mixer. Thus the image filter between the power amplifier and the antenna is redundant and may consequently be removed. Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two phase shifters in the low-frequency VCO signal that shifts the phase to 0° and 90°. The output signals of the mixers are summed to form the single-upper-sideband output signal.

The output stage is a high-level output buffer with an output power of approximately 4 dBm. The output level is sufficient to drive a three-stage bipolar preamplifier for DECT.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2067G	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1

QUICK REFERENCE DATA

For conditions see Chapters "DC characteristics" and "AC characteristics".

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.0	3.6	5.5	V
$I_{CC(RX)}$	receive supply current	–	24	–	mA
$I_{CC(TX)}$	transmit supply current	–	42	–	mA
$I_{CC(RFLO)}$	RF oscillator supply current	–	15	–	mA
$I_{CC(IFLO)}$	IF oscillator supply current	–	7	–	mA
NF_{RX}	receive noise figure	–	–	7.0	dB
G_{CP}	conversion power gain	–	30	–	dB
IR_{RX}	receive image frequency rejection	–	34	–	dB
f_{RFLO}	RFLO frequency range	1.65	–	1.85	GHz
f_{IFLO}	IFLO frequency range	100	–	140	MHz
P_{out}	output transmit power	–	4	–	dBm
IR_{TX}	transmit image frequency rejection	–	33	–	dBc
T_{amb}	operating ambient temperature	–30	+25	+85	°C

BLOCK DIAGRAM

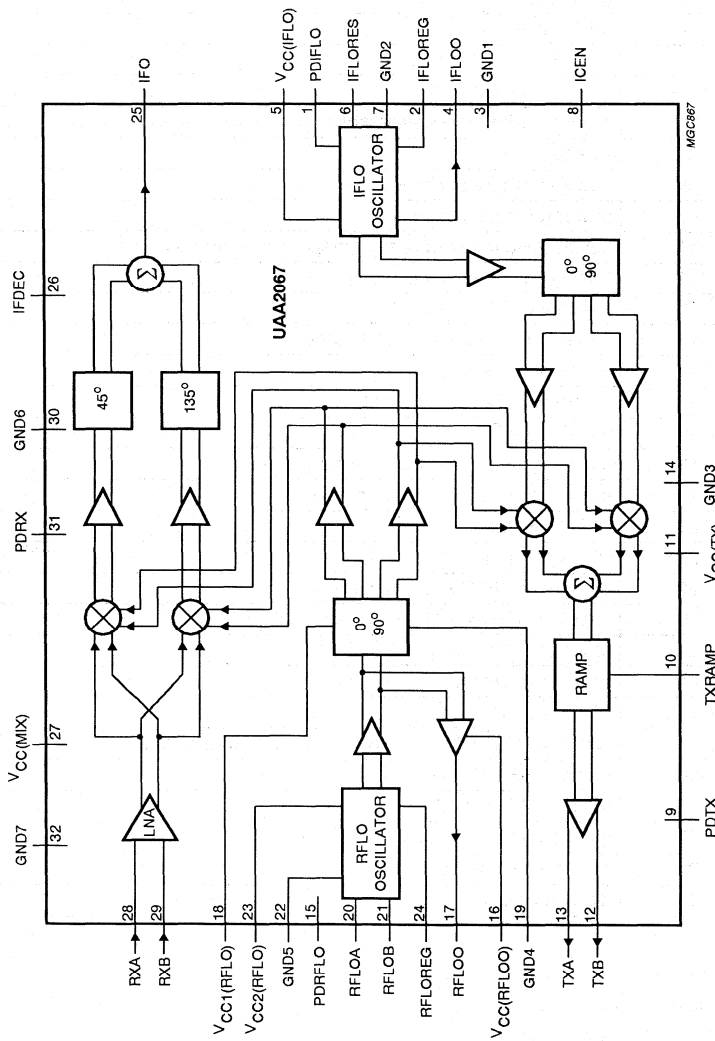


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
PDIFLO	1	power-down for IFLO
IFLOREG	2	regulator decoupling for IFLO
GND1	3	ground for IFLO; note 1
IFLOO	4	IFLO output
$V_{CC(IFLO)}$	5	supply voltage for IFLO
IFLORES	6	IFLO resonator
GND2	7	ground for IFLO resonator; note 1
ICEN	8	IC enable
PDTX	9	power-down for transmitter
TXRAMP	10	power ramping transmitter
$V_{CC(TX)}$	11	supply voltage for transmitter output stage; note 2
TXB	12	transmitter RF output B
TXA	13	transmitter RF output A
GND3	14	ground for transmitter output stage
PDRFLO	15	power-down for RFLO
$V_{CC(RFLOO)}$	16	supply voltage for RFLO output
RFLOO	17	RFLO output
$V_{CC1(RFLO)}$	18	supply voltage for RFLO oscillator; note 3
GND4	19	ground for RFLO oscillator; note 4
RFLOA	20	RFLO resonator
RFLOB	21	RFLO resonator
GND5	22	ground for RFLO oscillator; note 4
$V_{CC2(RFLO)}$	23	supply voltage for RFLO oscillator; note 3
RFLOREG	24	regulator decoupling for RFLO
IFO	25	receiver IF output
IFDEC	26	IF decoupling
$V_{CC(MIX)}$	27	supply voltage for receive and transmit mixers; note 2
RXA	28	receiver RF input A
RXB	29	receiver RF input B
GND6	30	ground for receive and transmit mixers
PDRX	31	power-down for receiver
GND7	32	die-pad ground

Notes

1. Pins 3 and 7 are internally short-circuited.
2. Pins 11 and 27 should be at the same DC voltage.
3. Pins 18 and 23 are internally short-circuited.
4. Pins 19 and 22 are internally short-circuited.

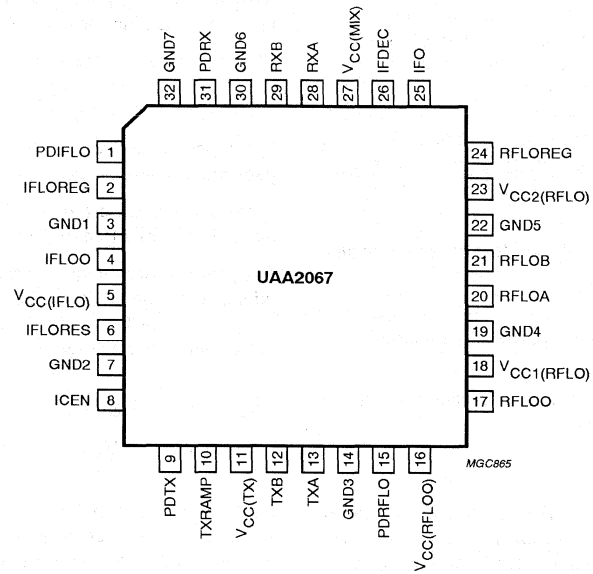


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a balanced low-noise amplifier followed by two high dynamic range mixers. The local oscillator signals, shifted in phase to 0 and 90° mix the amplified RF signal to the I and Q channels.These two channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection. Signals at the RF input at RFLO – IF frequencies are rejected through the signal processing while signals at the RFLO + IF frequencies form the IF signals.

An image rejection of typically 34 dB is obtained for an IF between 100 and 120 MHz.

Balanced signals are used for minimizing crosstalk due to package parasitics. The IF output is single-ended. The typical load is 50 Ω.

Fast switching, **on**/**off** of the receive section is controlled by the hardware input PDRX.

RFLO section

The high-frequency oscillator (RFLO oscillator) supplies the local oscillator signal for the down-conversion (receive) and up-conversion (transmit) mixers. This VCO uses an on-chip regulator for a power-supply voltage-independent output frequency. The buffered VCO signal is fed into a phase shifter and an off-chip prescaler-synthesizer. The output signal of the phase-shifter is used for driving the RX and TX mixers. Due to the good isolation in the buffer stages, a very small change in VCO frequency is obtained when switching the RX and TX mixers **on**.

Fast switching, **on**/**off** of the oscillator section is controlled by the hardware input PDRFLO.

IFLO section

The low-frequency oscillator (IFLO oscillator) internally supplies the local oscillator signal to the single-sideband transmit mixer. The buffered VCO signal is fed into a phase shifter. The output signal of the phase-shifter is used for driving the TX mixers.

Due to the good isolation in the buffer stages, a very small change in VCO frequency is obtained when switching the TX mixer **on**.

Fast switching **on**/**off** of the oscillator section is controlled by the hardware input PDIFLO input.

Transmit section

The circuit contains two balanced mixers, each of which is driven by the RFLO and IFLO signals. The output signal of the two mixers is summed and buffered to obtain the single upper-sideband signal at frequency RFLO + IFLO.

With the use of an off-chip time constant, the ramping circuit defines the power ramp-up and ramp-down of the pre-amplifier output signal.

Balanced signals are used for minimizing crosstalk due to package parasitics.

Fast switching, **on**/**off**, of the transmit section is controlled by the hardware input PDTX.

The power supply voltage of the transmit mixers, the adding circuit and ramping circuit is taken from the $V_{CC(MIX)}$ and GND6 for maximum isolation from the preamplifier output stage.

OPERATING MODES

To use the IC, **all** V_{CC} pins must be connected to the supply voltage.

For transceiving a DECT signal, the RFLO and IFLO sections should be powered-on. After a stable frequency has been reached (mainly determined by the synthesizer design), the receiver or transmitter can be powered-on.

GMSK data modulation can be supplied in two different ways: the data is directly modulated on IFLO or RFLO.

The ramping of the power level can be set with a time constant that is external to the IC.

Table 1 gives the definition of the polarity of the switching signals on the receive, the RFLO, the IFLO and the transmit sections.

Table 1 Switching signals on the receiver

SIGNAL	SECTION	LEVEL	on/off
PDRX	receive section powered-on	LOW	on[1]
	receive section powered-off	HIGH	off
PDRFLO	RFLO section powered-on	LOW	on[1]
	RFLO section powered-off	HIGH	off
PDIFLO	IFLO section powered-on	LOW	on[1]
	IFLO section powered-off	HIGH	off
PDTX	transmit section powered-on	LOW	on[1]
	transmit section powered-off	HIGH	off
ICEN	all sections disabled	LOW	off
	all sections enabled	HIGH	on

Note

1. Active when ICEN is enabled.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–	6	V
ΔGND	difference in ground supply voltage applied between all grounds	note 1	–	+ 0.3	V
$P_{I(max)}$	maximum power input		–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature		–	+150	°C
$P_{dis(max)}$	maximum power dissipation in stagnant air at 25°C		–	500	mW
T_{stg}	storage temperature		–65	+150	°C

Note

1. Pins short-circuited internally must be short-circuited externally.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	90	K/W

HANDLING

Every pin withstands the ESD test in accordance with *"MIL-STD-883C class 2 (method 3015.5)"*.

DC CHARACTERISTICS

V_{CC} = 3.6 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: $V_{CC(MIX)}$, $V_{CC(TX)}$, $V_{CC(IFLO)}$, $V_{CC1(RFLO)}$, $V_{CC2(RFLO)}$ and $V_{CC(RFLOO)}$						
V_{CC}	supply voltage	over full temperature range	3.0	3.6	5.5	V
$I_{CC(RX)}$	supply current	receive section **on**; DC tested	18	24	30	mA
$I_{CC(RFLO)}$	supply current RFLO	RFLO section **on**; DC tested	11	15	20	mA
$I_{CC(IFLO)}$	supply current IFLO	IFLO section **on**; DC tested	5	7	9	mA
$I_{CC(TX)}$	supply current	transmit section **on**; DC tested	34	42	54	mA
$I_{CC(PD)}$	supply current	power-down mode; DC tested	–	2	50	µA
Pins: PDRX, PDTX, PDRFLO, PDIFLO and ICEN						
V_{IH}	HIGH level input voltage		2.1	–	V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} − 0.4 V	−1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	−1	–	+1	µA
Pins: RXA, RXB, IFO and IFDEC						
$V_{RXA,B}$	DC input voltage level	receive section **on**	2.1	2.4	2.7	V
V_{IFO}	DC output voltage level	receive section **on**	0.9	1.1	1.3	V
V_{IFDEC}	DC level	receive section **on**	2.45	2.65	2.85	V
Pins: RFLOA, RFLOB, RFLOREG and RFLOO						
$I_{RFLOA,B}$	DC current	RFLO section **on**	1	2	3	mA
$V_{RFLOREG}$	DC level	RFLO section **on**	2.45	2.65	2.85	V
V_{RFLOO}	DC output voltage level	RFLO section **on**	2.8	3.1	3.4	V
Pins: IFLORES, IFLOREG and IFLOO						
$V_{IFLORES}$	DC level	IFLO section **on**	1.85	2.1	2.3	V
$V_{IFLOREG}$	DC level	IFLO section **on**	2.35	2.55	2.8	V
V_{IFLOO}	DC output voltage level	IFLO section **on**	2.2	2.45	2.7	V
Pins: TXA, TXB and TXRAMP						
$I_{TXA,B}$	DC output current	transmit section **on**	2	10	18	mA
I_{TXRAMP}	DC input current	V_{TXRAMP} = 3 V; transmit section **on**	–	–	200	µA

AC CHARACTERISTICS

V_{CC} = 3.0 to 5.5 V; T_{amb} = −30 to +85°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive mode (receive and RFLO sections powered-on)						
f_{RFI}	RF input frequency		1800	–	1900	MHz
R_{iRF}	RF input resistance (real part of the parallel input impedance)	balanced; at 1890 MHz	–	190	–	Ω
C_{iRF}	RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1890 MHz	–	0.8	–	pF
$PRFLO_{RX}$	RFLO level at input to RX balun	note 1	–	−70	−40	dBm
$DES3_{RX}$	RF interference for 3 dB desensitization	interference frequency offset 6 MHz; note 1	–	−35	–	dBm
G_{CP}	conversion power gain	RF input to IF output (typical load)				
		over full temperature range	24	30	36	dB
		T_{amb} = 25 °C	27	30	33	dB
$CP1_{RX}$	1 dB input compression point	referenced to RF input; note 1	−36	−33	–	dBm
$P_{o(RX)}$	IF power for $CP1_{RX} < P_{in} < +8$ dBm	referenced to IF power at $CP1_{RX}$; note 1	−6	–	+6	dB
t_{rec}	recovery time for P_{in} = +12 dBm	note 1	–	2	30	μs
$IP2\text{-}2_{RX}$	mixer 2-2 spurious intercept point	referenced to the RF input; note 1	−6	+2	–	dBm
$IP3_{RX}$	3rd order intercept point	referenced to the RF input; note 1	−30	−25	–	dBm
NF_{RX}	overall noise figure	RF input to IF output; note 1	–	5.8	7	dB
f_{IF}	IF frequency range		100	110	120	MHz
$Z_{L(IF)}$	typical application IF output load impedance	f_{IF} = 110 MHz	–	50	–	Ω
IR_{RX}	image frequency rejection	over full temperature range	20	34	–	dB
		T_{amb} = 25 °C	23	34	–	dB
PSRR	power supply rejection ratio	note 1; typical load; at 110 MHz	35	–	–	dB

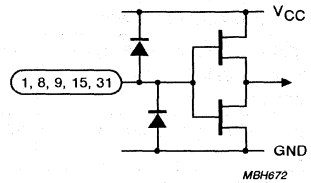
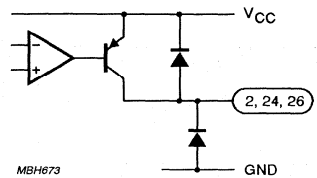
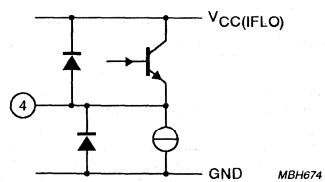
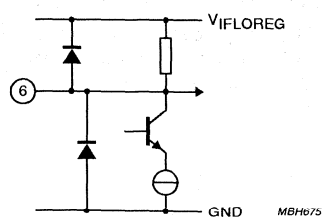
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF local oscillator (RFLO section powered-on)						
$f_{RFLO(min)}$	minimum oscillator frequency range		1650	–	1850	MHz
$R_{i(RFLO)}$	oscillator input resistance (real part of the parallel input impedance)	balanced; at 1.77 GHz	–	–250	–	Ω
$C_{i(RFLO)}$	oscillator input capacitance (imaginary part of the parallel input impedance)	balanced; at 1.77 GHz	–	2.7	–	pF
$V_{o(RFLO)}$	local oscillator output level at pin 17; RMS value	note 2; typical load resistance	50	75	–	mV
$Z_{o(RFLO)}$	local oscillator output impedance at pin 17	at 1.77 GHz	–	30 – 60j	–	Ω
$R_{L(RFLO)}$	typical load resistance		–	300	–	Ω
$HAR_{(RFLO)}$	harmonic levels at RFLO output (pin 17)	note 1	–	–	–20	dBc
IF local oscillator (IFLO section powered-on)						
$f_{IFLO(min)}$	minimum oscillator frequency range		100	120	140	MHz
$R_{i(IFLO)}$	oscillator input resistance (real part of the parallel input impedance)		–	–480	–	Ω
$C_{i(IFLO)}$	oscillator input capacitance (imaginary part of the parallel input impedance)		–	2.1	–	pF
$V_{o(IFLO)}$	IF local oscillator output level at pin 4; RMS value		100	160	–	mV
$Z_{o(IFLO)}$	local oscillator output impedance (real part)		–	–	100	Ω
$R_{L(IFLO)}$	typical load resistance		–	5	–	kΩ
$C_{L(IFLO)}$	typical load capacitance		–	7	–	pF
$HAR_{(IFLO)}$	harmonic levels at IFLO output	note 1	–	–	–15	dBc

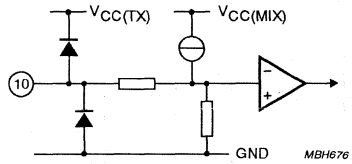
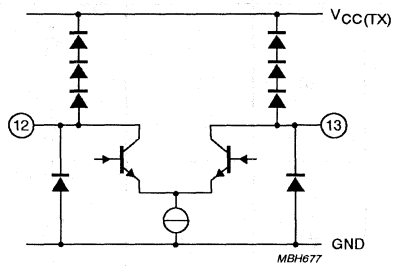
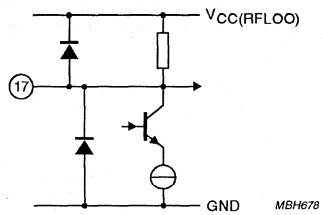
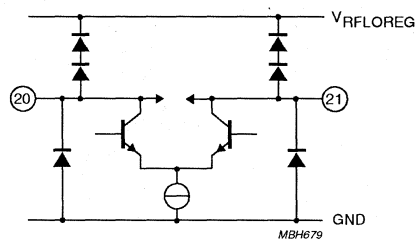
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit mode (transmit, RFLO and IFLO sections powered-on)						
f_{TX}	RF output frequency		1800	–	1900	MHz
$R_{o(TX)}$	RF output resistance (real part of the parallel output impedance)	balanced; note 1	–	110	–	Ω
$C_{o(TX)}$	RF output capacitance (imaginary part of the parallel output impedance)	balanced; note 1	–	0.6	–	pF
$FTRFLO_{TX}$	RFLO feedthrough at the TX output	referenced to the desired frequency; T_{amb} = 25 °C; note 1	–	–25	–23	dBc
Pout	output transmit power	V_{TXRAMP} = 0 V; note 1				
		over full temperature range	–2	4	8	dBm
		T_{amb} = 25 °C	1	4	7	dBm
IR_{TX}	image frequency rejection	referenced to the desired frequency; note 1				
		over full temperature range	20	33	–	dBc
		T_{amb} = 25 °C	23	33	–	dBc
$Z_{inTXRAMP}$	input impedance at pin TXRAMP		10	–	–	kΩ
$C_{inTXRAMP}$	input capacitance at pin TXRAMP		–	–	10	pF
$V_{TXRAMP(max)}$	ramp voltage for $P_{out} = P_{max}$		–	0		V
$V_{TXRAMP(min)}$	ramp voltage for $P_{out} = P_{max} - 30$ dB		–	3.0	–	V
CNR_{TX}	carrier-to-noise ratio at TX output	T_{amb} = 25 °C; notes 1 and 3	+130	+133	–	dBc/Hz
Timing						
t_{up}	start-up/power-down time of each block	over full temperature range	–	5	10	µs
C_i	input capacitance of logic inputs	over full temperature range	–	–	5	pF

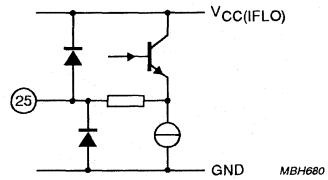
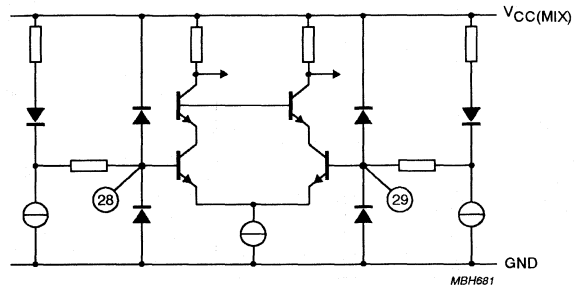
Notes

1. Measured and guaranteed only on the Philips demonstration board, including PCB and balun.
2. The imaginary part of the load impedance has been tuned out. A power match is assumed.
3. A simplified DECT type approval measurement is used; the spectrum analyser has the following settings: RBW = 100 kHz, VBW = 100 Hz, use delta marker and add 50 dB (correction for RBW = 100 kHz), f_{RFLO} = 1.77 GHz and f_{IFLO} = 120 MHz, Δf = 4.686 MHz.

INTERNAL PIN CONFIGURATION

SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
PDIFLO	1	–	
ICEN	8	–	
PDTX	9	–	
PDRFLO	15	–	
PDRX	31	–	
IFLOREG	2	2.55	
RFLOREG	24	2.65	
IFDEC	26	2.65	
GND	3, 7, 14, 19, 22, 30, 32	0	
IFLOO	4	2.45	
V_{CC}	5, 11, 16, 18, 23, 27	3.6	
IFLORES	6	2.1	

SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
TXRAMP	10	–	
TXB	12	V_{CC}	
TXA	13	V_{CC}	
RFLOO	17	3.1	
RFLOA	20	2.0	
RFLOB	21	2.0	

SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
IFO	25	1.1	
RXA	28	2.4	
RXB	29	2.4	

APPLICATION INFORMATION

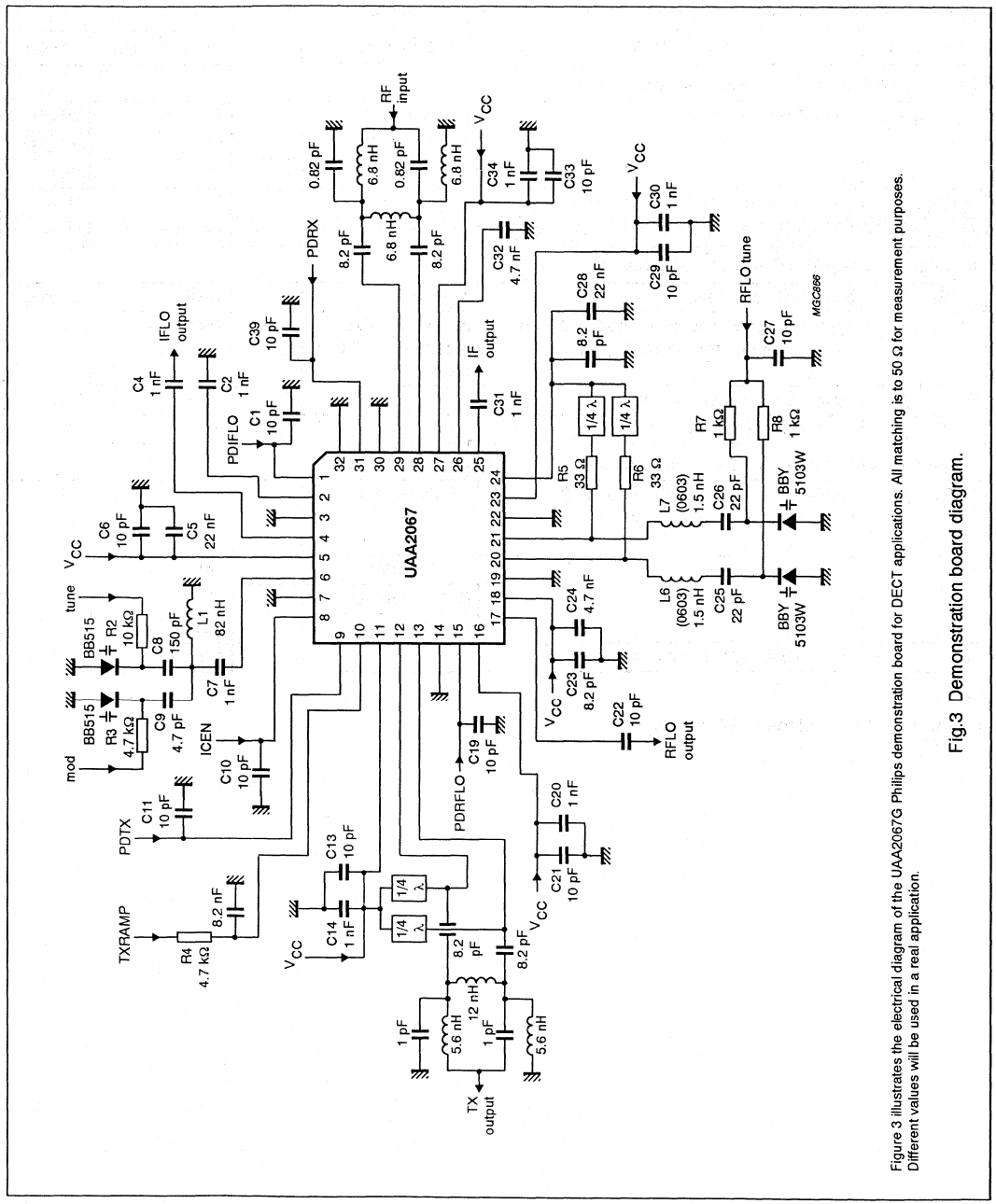


Fig.3 Demonstration board diagram.

Figure 3 illustrates the electrical diagram of the UAA2067G Philips demonstration board for DECT applications. All matching is to 50 Ω for measurement purposes. Different values will be used in a real application.

Application-indicative values

Measured on the Philips demonstration board, including PCB and balun at T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF local oscillator (RFLO section powered-on)						
CNR_{RFLO}	carrier-to-noise ratio	Δf = 864 kHz	–	117	–	dBc/Hz
		Δf = 2500 kHz	–	128	–	dBc/Hz
		Δf = 4686 kHz	–	134	–	dBc/Hz
$PULL_{RFLO}$	pulling due to enabling RX or TX	V_{TXRAMP} = 3 V	–	5	–	kHz
$SHIFT_{RFLO}$	frequency shift due to 200 mV V_{CC} change		–	5	–	kHz
IF local oscillator (IFLO section powered-on)						
CNR_{IFLO}	carrier-to-noise ratio	Δf = 4686 kHz	–	140	–	dBc/Hz
$SPUR_{IFLO}$	spurious signal modulation due to 0.5 mV (RMS value) on the power supply	Δf = 4686 kHz; measured at TX output	–	−60	–	dBc
$PULL_{IFLO}$	pulling due to enabling TX		–	1	–	kHz
$SHIFT_{IFLO}$	frequency shift due to 200 mV V_{CC} change		–	2.5	–	kHz
Transmit mode (transmit, RFLO and IFLO sections powered-on)						
$PSRR_{TX}$	spurious signal modulation due to 0.5 mV (RMS value) on $V_{CC(MIX)}$, $V_{CC(TX)}$ and $V_{CC(RFLO)}$ only	Δf = 4686 kHz; note 1	–	−74	–	dBc
$SPUR_{TX}$	spurious signals	RFLO − 3IFLO	–	−40	–	dBc
		RFLO + 2IFLO	–	−35	–	dBc
		RFLO + 5IFLO	–	−51	–	dBc
N_{TX}	white noise level at the output		–	135	–	dBc/Hz

Note

1. Including PSRR of the RFLO circuitry.

Image rejecting front-end for GSM applications UAA2072M

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for up to 60 dB on-chip image rejection
- Programmable IF I/Q combiner
- On-chip programmable quadrature network
- Very fast 3-wire control bus
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2072M contains both a receiver front-end and a high frequency transmit mixer intended to be used in the GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2072M is its ability to provide at least 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne or supradyne reception. The precision needed for this signal processing is achieved by compensating for process spreads and trimming for the choosen IF frequency and the LO band centre frequency via a 3-wire serial bus interface.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The overall phase rotation is programmable for maximum image rejection at a given IF. The IF output drivers have differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced, and 200 Ω is used as standard RF impedance.

A 3-pin unidirectional serial interface is used to program the circuits, using 16-bit words. This data bus allows compensation of process spreads, and is used to adjust for maximum image rejection performance at a given IF. It also offers a selection to reject the upper or lower image frequency and control over the different power-down modes. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	4.5	4.8	5.3	V
I_{CCRX}	receive supply current	26	31.5	38	mA
I_{CCTX}	transmit supply current	10	12	14	mA
I_{CCPD}	supply current in power-down	–	–	50	μA
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2072M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

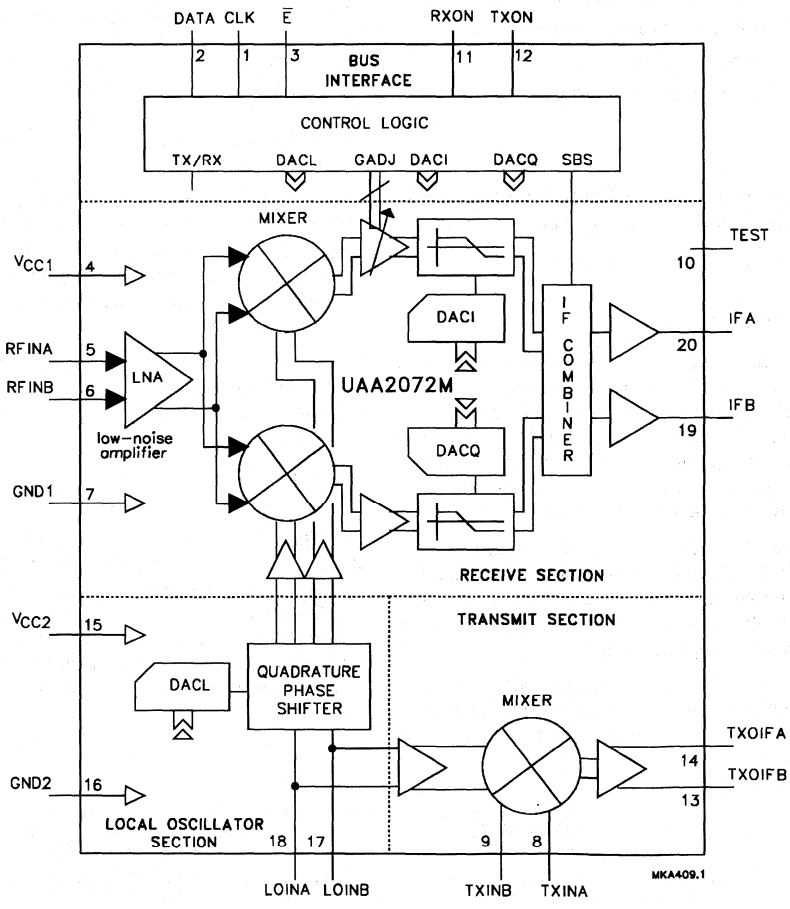


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	serial bus clock
DATA	2	serial bus data
$\overline{E}$	3	serial bus enable (active LOW)
V_{CC1}	4	supply voltage for LNA, IF parts and TX mixer
RFINA	5	RF balance input A
RFINB	6	RF balance input B
GND1	7	ground for synthesizer buffer and logic
TXINA	8	transmit mixer input A (balanced)
TXINB	9	transmit mixer input B (balanced)
TEST	10	reserved for test purposes, should be connected to ground
RXON	11	hardware power-on for receive parts
TXON	12	hardware power-on for transmit mixer
TXOIFB	13	transmit mixer IF output B (balanced)
TXOIFA	14	transmit mixer IF output A (balanced)
V_{CC2}	15	supply voltage for local oscillator parts
GND2	16	ground for LO parts
LOINB	17	LO input B (balanced)
LOINA	18	LO input A (balanced)
IFB	19	IF output (balanced)
IFA	20	IF output (balanced)

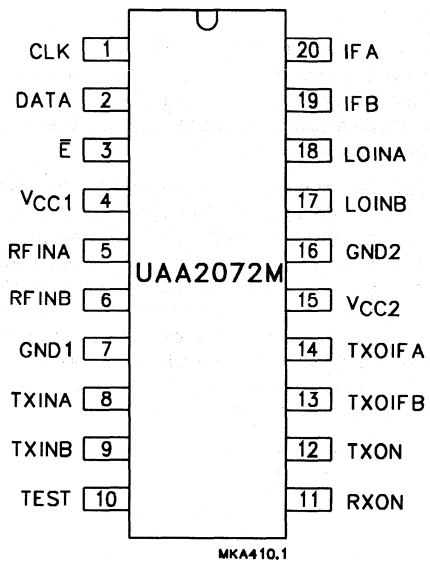


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

The serial bus interface is used for tuning to maximum image rejection at a given IF. The contents of registers ip5 to ip0 and qp5 to qp0 (named IF phase adjustment words) are digital-to-analog converted in the DACI and DACQ blocks. The obtained internal voltages control the phase shift in I and Q; thus allowing them to be trimmed precisely to 45° and 135° at any given IF between 30 and 90 MHz. The gain in the I channel is slightly adjustable using the four bits ga3 to ga0 to allow compensation of small gain mismatches between I and Q.

One bit (sbs) allows selection between infradyne or supradyne reception.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 200 Ω, choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; i.e. a 1 kΩ resistor load at each IF output, plus a 2 kΩ resistor to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

In the event of only one output being used, a 1 kΩ resistive load in parallel with a tuning inductor to V_{CC}, provides a matched 1 kΩ output to the external IF filter.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON or via the bus interface by changing the srx-bit in the internal register.

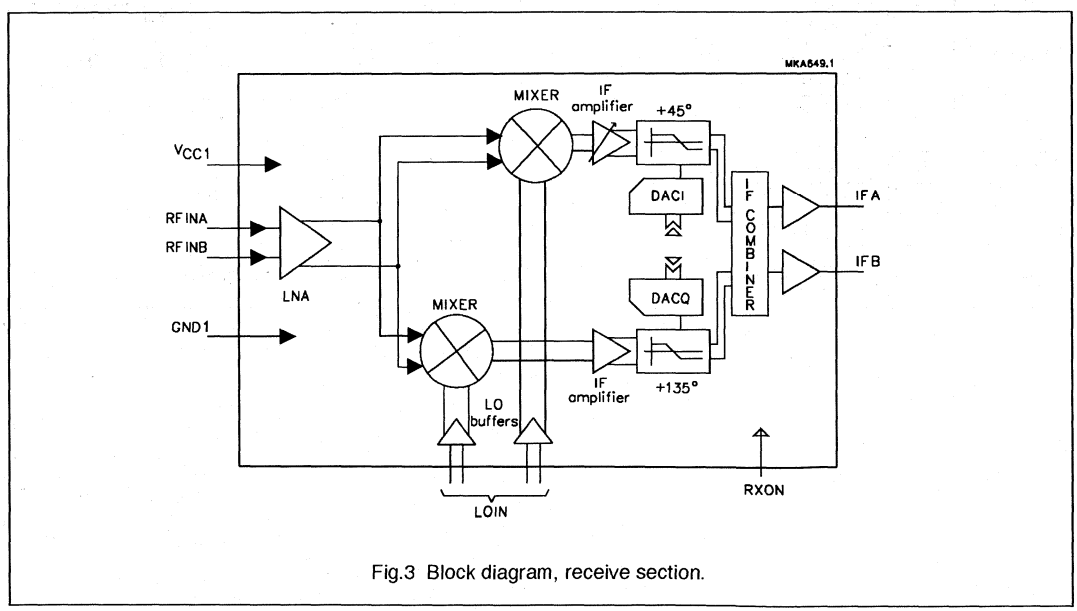


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by programming via the serial bus. The word 'lo5 to lo0' named LO Quad Centre Frequency Adjustment word is converted to an analog voltage in a digital-to-analog converter (DACL, see Fig.6). This voltage trims the all-pass network to the selected LO frequency range. To obtain the 30 dB specified image rejection the precision required on this trimming remains low.

The LO input impedance is 100 Ω differential. Switching from RX to TX or power-down mode has little influence on the LO input impedance.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 kΩ load. The IF outputs are low impedance (common collector type).

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON or via the serial bus interface by changing the stx-bit in the internal register.

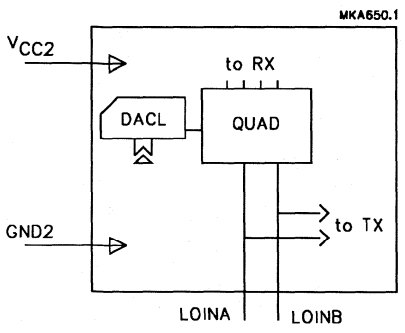


Fig.4 Block diagram, LO section.

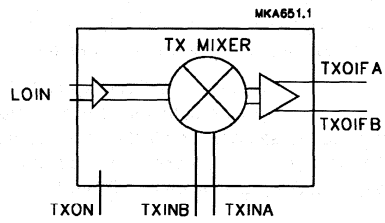


Fig.5 Block diagram, transmit mixer.

Serial bus interface

The 3-wire serial bus interface allows control over the selective power-up of the transmit, receive and LO buffer circuits, the tuning of the LO quadrature and IF quadrature circuits and the selection of sideband rejection. The interface consists of a 16-bit programming register, three working latches and three DACs which provide the tuning voltages for the image rejection of the receive quadrature circuits.

BUS FORMAT

A 3-wire unidirectional bus is used to program the circuit, the 3 wires being: DATA, CLOCK (CLK) AND ENABLE ($\overline{E}$). The timing diagram is illustrated in Fig.6. The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their corresponding data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed working latch when $\overline{E}$ returns HIGH.
Only the last 16 bits clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. If $\overline{E}$ returns HIGH while CLK is still LOW, the extra clock edge produced will cause data shift. The bus interface will not output any address recognition.

Data is entered with the most significant bit first. The leading 12 bits make up the data field, while the trailing 4 bits comprise the address. The first bit entered is p1, the last bit p16. The bits in the programming registers and addresses are arranged as shown in Table 1.

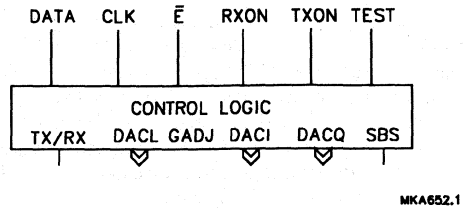


Fig.6 Block diagram, serial bus interface.

Table 1 Register bit allocation

REGISTER BIT ALLOCATION															
FIRST															**LAST**
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16
DATA FIELD												ADDRESS			
dt11	dt10	dt9	dt8	dt7	dt6	dt5	dt4	dt3	dt2	dt1	dt0	ad3	ad2	ad1	ad0
This register is reserved for test purposes and should not be programmed												0	0	0	0
X	X	X	X	sbs	X	X	X	X	hpn	srx	stx	0	0	0	1
ga3	ga2	ga1	ga0	X	X	lo5	lo4	lo3	lo2	lo1	lo0	0	0	1	0
ip5	ip4	ip3	ip2	ip1	ip0	qp5	qp4	qp3	qp2	qp1	qp0	0	0	1	1

Table 2 Bit allocation description

BIT	REMARKS	LOGIC		PRESET
stx	software transmit power-on	1 = power-up	0 = power-down	0
srx	software receive power-on	1 = power-up	0 = power-down	0
hpn	hardware priority not (selects if power status of blocks is controlled via hardware or software)	1 = soft priority	0 = hard priority	0
sbs	sideband select	1 = upper sideband selected	0 = lower sideband selected	0
ga3 to ga0	IF I channel gain adjustment			0111
lo5 to lo0	LO quadrature centre frequency adjustment			011111
ip5 to ip0	IF I channel phase adjustment			011111
qp5 to qp0	IF Q channel phase adjustment			011111
X	not used			

Table 3 details the different power-up modes of the circuit. Attention should be paid to the hpn-bit. This bit enables the RXON and TXON pins to take any logic position when software programming for power-up is used.

Table 3 Control of power status (note 1)

REGISTER BIT STATUS			EXTERNAL PIN LEVEL		CIRCUITS POWER STATUS	
hpn	**stx**	**srx**	**TXON**	**RXON**	**TRANSMIT**	**RECEIVE**
0	X	X	LOW	LOW	off	off
0	X	X	LOW	HIGH	off	on
0	X	X	HIGH	LOW	on	off
0	X	X	HIGH	HIGH	on (2)	on(2)
1	0	0	x	x	off	off
1	0	1	x	x	off	on
1	1	0	x	x	on	off
1	1	1	x	x	on(2)	on(2)

Notes

1. X = don't care; x = HIGH or LOW logic voltage level applied at designated pin.
2. Circuit is operative in this mode but specification is NOT guaranteed.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	v
ΔGND	difference in ground supply voltage applied between GND1 and GND2	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 4.8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CC1}, V_{CC2}, LOINA and LOINB						
V_{CC}	supply voltage	over full temperature range	4.5	4.8	5.3	V
I_{CCRX}	supply current	receive mode active; DC tested	26	31.5	38	mA
I_{CCTX}	supply current	transmit mode active; DC tested	10	12	14	mA
I_{CCPD}	supply current in power-down mode	DC tested	–	–	50	μA
Pins: CLK, DATA, $\overline{E}$, RXON, TXON and TEST						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} − 0.4 V	−1	–	+1	μA
I_{IL}	LOW level static input current	pin at 0.4 V	−1	–	+1	μA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	1.7	2.1	2.4	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	2.0	2.5	3.5	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	1.8	2.2	2.5	V
Pins: TXOIFA and TXOIFB						
V_O	DC output voltage level	transmit section enabled	2.5	2.9	3.4	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4.8 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RFI}	RF input impedance	balanced	–	200	–	Ω
f_{RFI}	RF input frequency		925	–	960	MHz
RL_{RF}	return loss on matched RF input impedance	note 1	15	20	–	dB
G_{CP}	conversion power gain	RF impedance to 1 IF output matched to 500 Ω	20	23	26	dB
		RF impedance to differential IF outputs matched to 1 kΩ differential	23	26	29	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.1	0.5	dB
ΔG/T	gain variation with temperature	note 2	−20	−15	−10	mdB/K
$CP1_{RX}$	1 dB input compression point	note 1	−26	−24.5	–	dBm
$IP2_{RX}$	2nd order intercept point referenced to the RF input	single-ended output; note 2	+15	+22	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF input differential	differential output; note 2	–	+32	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	−18	−15	–	dBm
F_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	4	5	dB
$Z_{L(IF)}$	typical application IF output load impedance	unbalanced	–	500	–	Ω
$C_{L(IF)}$	IF output load capacitance	unbalanced	–	–	2	pF
f_{IF}	IF frequency range	RF < LO	30	71	90	MHz
		RF > LO	30	45	50	MHz
f_{IR}	image frequency rejection	note 4	30	–	–	dB
f_{IRp}	image rejection at preset	superheterodyne; f_{IF} = 71 MHz; note 1	30	35	–	dB
Local oscillator section (receive section enabled)						
f_{LO}	LO input frequency		875	–	1050	MHz
Z_{LO}	LO input impedance	balanced	–	100	–	Ω
RL_{LO}	return loss on matched input (including standby mode)	note 2	10	15	–	dB
$P_{i(LO)}$	LO input power level		−7	−4	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section enabled)						
Z_O	TX IF output impedance		–	–	200	Ω
Z_L	TX IF load impedance		–	1000	–	Ω
C_L	maximum TX IF load capacitance		–	–	2	pF
$Z_{i(RF)}$	TX RF input impedance	balanced	–	200	–	Ω
f_{TXmix}	TX mixer input frequency		880	–	915	MHz
RL_{TX}	return loss on matched TX input	note 2	15	20	–	dB
G_{CP}	conversion power gain	from 200 Ω to 1 kΩ output	8	10	12	dB
$f_{o(TX)}$	TX mixer output frequency		40	–	200	MHz
$CP1_{TX}$	1 dB input compression point		–20	–15	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+20	–	dBm
$IP3_{TX}$	3rd order intercept point		–10	–7	–	dBm
F_{TX}	noise figure	double sideband; note 2	–	–	12	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	μs

Notes

1. Measured and guaranteed only on UAA2072M demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2072M demonstration board.
3. This value includes printed-circuit board and balun losses.
4. This value might be dependent upon control values sent by a microcontroller via the serial bus. This performance is maintained over the RF band for a fixed phase rotation control word.

TIMING CHARACTERISTICS

Typical values measured at V_{CC} = 4.8 V; T_{amb} = 25 °C; maximum value conditions under maximum clock speed; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial bus interface					
f_{clk}	clock frequency	–	–	13	MHz
Serial programming clock (pin CLK)					
t_r	rise time	–	10	40	ns
t_f	fall time	–	10	40	ns
T_{cy}	clock period	75	–	–	ns
Enable programming (pin $\overline{E}$)					
t_{START}	delay to rising edge of clock	30	–	–	ns
t_{END}	delay from last edge of clock	10	–	–	ns
t_W	minimum inactive pulse width	75	–	–	ns
t_{NEW}	delay from $\overline{E}$ inactive to new data	150	–	–	ns
Register serial input data (pin DATA)					
t_{su}	input data to CLK set-up time	20	–	–	ns
t_h	input data to CLK hold time	20	–	–	ns

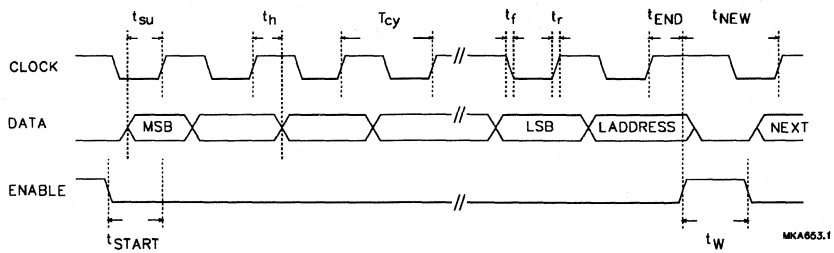


Fig.7 Serial bus timing diagram.

APPLICATION INFORMATION

Figure 8 illustrates the electrical diagram of the UAA2072M Philips demonstration board. All matching is to 50 Ω for measurement purposes. Different values will be used in a real application.

Component manufacturers

All surface mounted resistors and capacitors are manufactured by Philips Components. The small value capacitors are multi-layer ceramic with NPO dielectric.

The inductors are manufactured by Coilcraft UK.

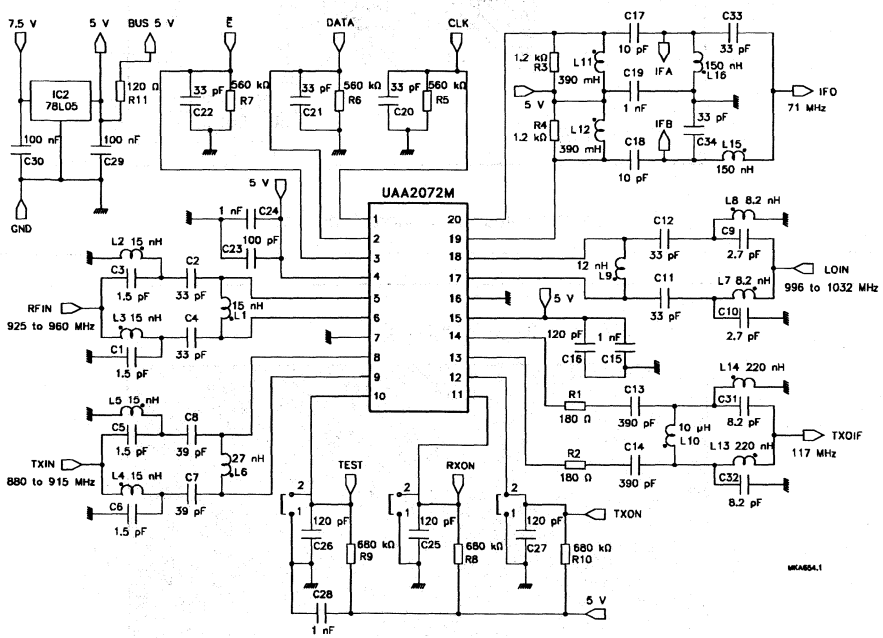


Fig.8 Application diagram.

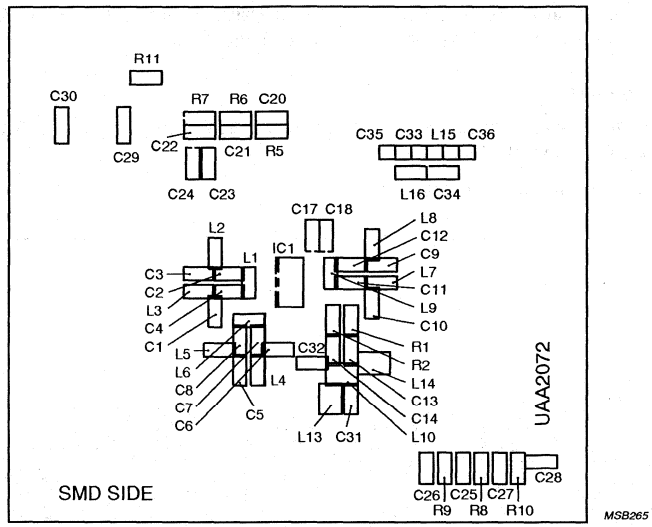


Fig.9 Printed-circuit board, SMD side.

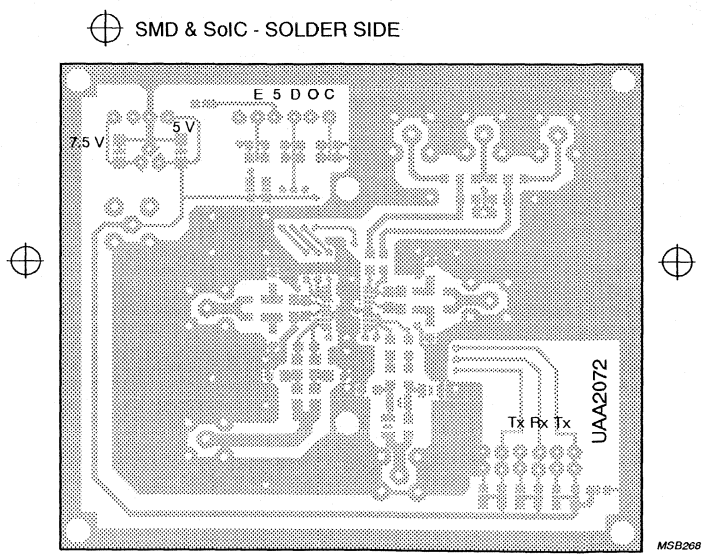


Fig.10 Printed-circuit board, SMD solder side.

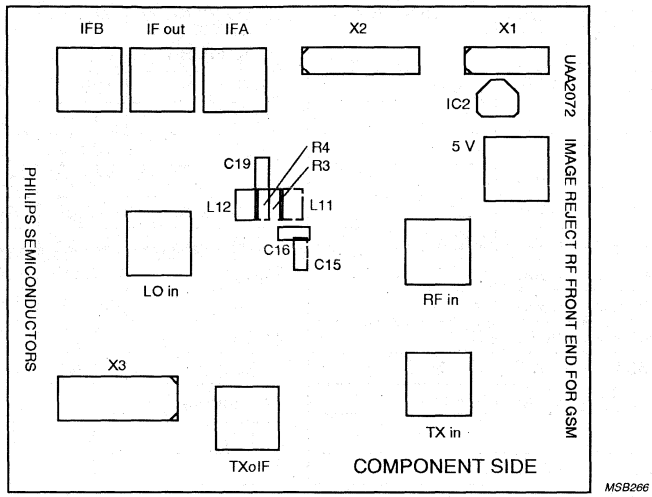


Fig.11 Printed-circuit board, component side for image reject RF front-end for GSM.

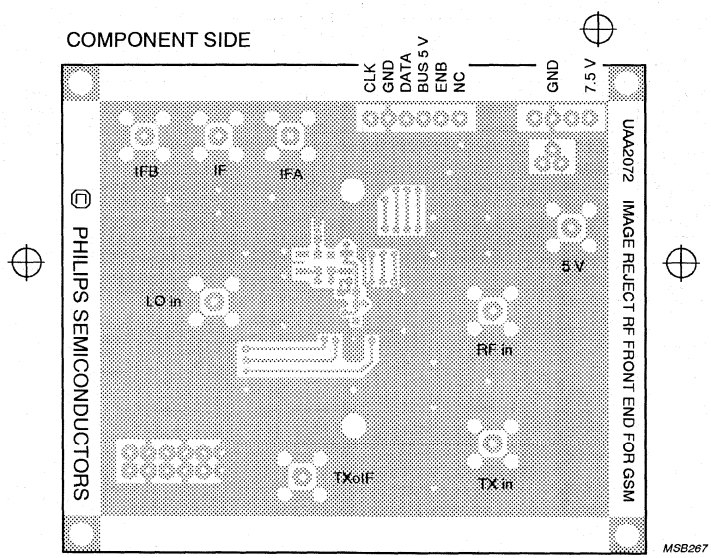


Fig.12 Printed-circuit board, component solder side for image reject RF front-end for GSM.

DEMONSTRATION BOARD - PARTS LIST

COMPONENT	VALUE	SIZE	LOCATION
Resistors			
R1	180 Ω	0805	TXOIF
R2	180 Ω	0805	TXOIF
R3	1.2 kΩ	0805	IF
R4	1.2 kΩ	0805	IF
R5	560 kΩ	0805	CLK
R6	560 kΩ	0805	DATA
R7	560 kΩ	0805	$\overline{E}$
R8	680 kΩ	0805	RXON
R9	680 kΩ	0805	TEST
R10	680 kΩ	0805	TXON
R11	120 Ω	0805	5 V BUS
Capacitors			
C1	1.5 pF	0805	RFIN
C2	33 pF	0805	RFIN
C3	1.5 pF	0805	RFIN
C4	33 pF	0805	RFIN
C5	1.5 pF	0805	TXIN
C6	1.5 pF	0805	TXIN
C7	39 pF	0805	TXIN
C8	39 pF	0805	TXIN
C9	2.7 pF	0805	LOIN
C10	2.7 pF	0805	LOIN
C11	33 pF	0805	LOIN
C12	33 pF	0805	LOIN
C13	390 pF	0805	TXOIF
C14	390 pF	0805	TXOIF
C15	1 nF	0805	V_{CC2}
C16	120 pF	0805	V_{CC2}
C17	10 pF	0805	IFO
C18	10 pF	0805	IFO
C19	1 nF	0805	IF / 5 V
C20	33 pF	0805	CLK
C21	33 pF	0805	DATA
C22	33 pF	0805	$\overline{E}$
C23	100 pF	0805	V_{CC1}
C24	1 nF	0805	V_{CC1}
C25	120 pF	0805	RXON
C26	120 pF	0805	TEST

COMPONENT	VALUE	SIZE	LOCATION
Capacitors			
C27	120 pF	0805	TXON
C28	1 nF	0805	5 V
C29	100 nF	1206	5 V regulator
C30	100 nF	1206	5 V regulator
C31	8.2 pF	0805	TXOIF
C32	8.2 pF	0805	TXOIF
C33	33 pF	0805	IFO
C34	33 pF	0805	IFO
C35	link	0805	IF/NOT USED
C36	link	0805	IF/NOT USED
Inductors			
L1	15 nH	0805	RFIN
L2	15 nH	0805	RFIN
L3	15 nH	0805	RFIN
L4	15 nH	0805	TXIN
L5	15 nH	0805	TXIN
L6	27 nH	0805	TXIN
L7	8.2 nH	0805	LOIN
L8	8.2 nH	0805	LOIN
L9	12 nH	0805	LOIN
L10	10 μH	1008	TXOIF/OPTIONAL
L11	390 nH	1008	IFO
L12	390 nH	1008	IFO
L13	220 nH	1008	TXOIF
L14	220 nH	1008	TXOIF
L15	150 nH	0805	IFO
L16	150 nH	0805	IFO

Other components

COMPONENT	DESCRIPTIONS
IC1	UAA2072M
IC2	5 V regulator; type 78L05
SMA/RIM	sockets for RF and IF inputs/outputs
SMB	5 V socket (optional, in place of IC2)
X1, X2 and X3	various 2.54 mm (0.1 inch) connectors

Image rejecting front-end for GSM applications UAA2073M

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for at least 30 dB on-chip image rejection
- IF I/Q combination network for 50 to 90 MHz
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2073M contains both a receiver front-end and a high frequency transmit mixer intended for GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2073M is its ability to provide over 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne or supradyne reception. Image rejection is at an optimum when the IF is 71 MHz and local oscillator is above the wanted signal.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection.The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The all-pass filters outputs are buffered before been fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced to reduce EMC issues.

Fast power-up switching is possible. A synthon mode enables LO buffers independent of the other circuits. When SYNTHON pin is high, all internal buffers on the LO path of the circuit are turned on, thus minimizing LO pulling when remainder of receive chain is powered-up.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	3.75	5.3	V
I_{CCRX}	receive supply current	22	26	32	mA
I_{CCTX}	transmit supply current	9	12	15	mA
NF	noise figure on demonstration board (including matching and PCB losses)	–	3.35	4.3	dB
G_P	conversion power gain	20	23	26	dB
IR	image frequency rejection	30	-	-	dB
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2073M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

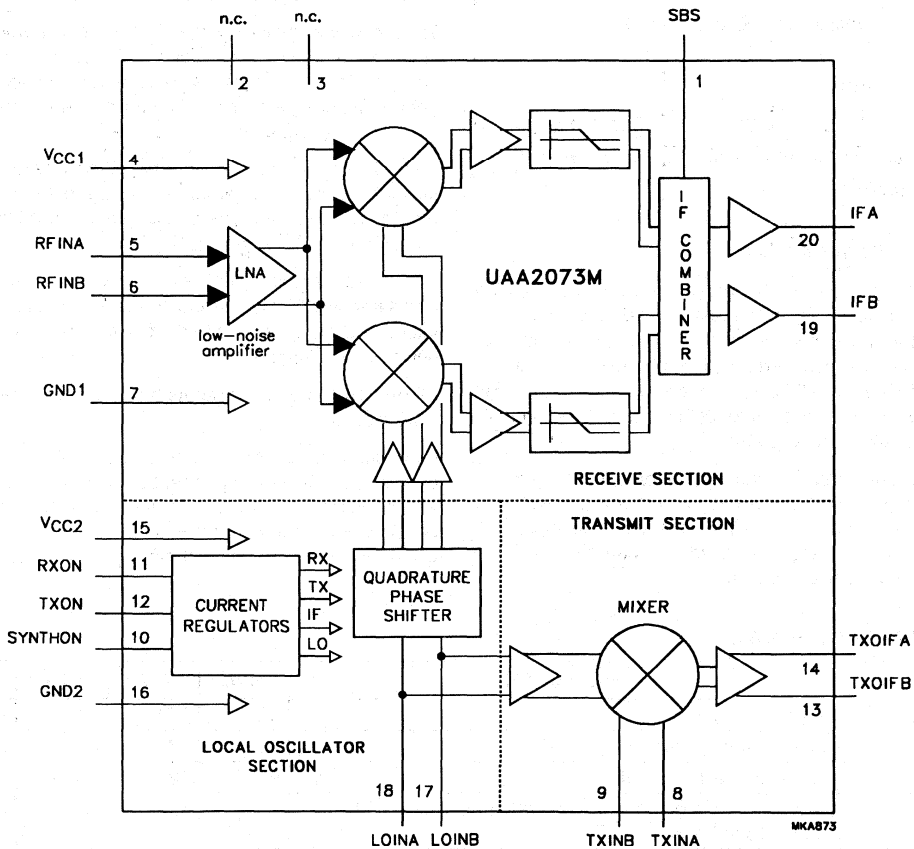


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SBS	1	sideband selection (LOW = LO > RF)
n.c.	2	not connected
n.c.	3	not connected
V_{CC1}	4	supply voltage for LNA, IF parts and TX mixer
RFINA	5	RF balance input A
RFINB	6	RF balance input B
GND1	7	ground 1 for receiver and transmitter mixer
TXINA	8	transmit mixer input A (balanced)
TXINB	9	transmit mixer input B (balanced)
SYNTHON	10	hardware power-on of internal LO buffer
RXON	11	hardware power-on for receive parts
TXON	12	hardware power-on for transmit mixer
TXOIFB	13	transmit mixer IF output B (balanced)
TXOIFA	14	transmit mixer IF output A (balanced)
V_{CC2}	15	supply voltage for LO parts
GND2	16	ground 2 for LO parts
LOINB	17	LO input B (balanced)
LOINA	18	LO input A (balanced)
IFB	19	IF output (balanced)
IFA	20	IF output (balanced)

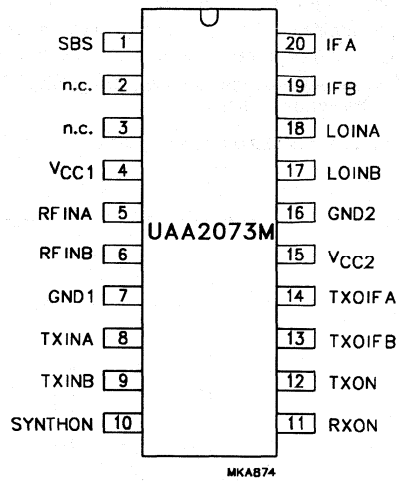


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type. The whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin (SBS) allows selection between infradyne or supradyne reception.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 150 Ω, choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type, tuned for 71.3 MHz. Typical application will load the output with a differential 500 Ω load; i.e. a 500 Ω resistor load at each IF output, plus a 1 kΩ resistor to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

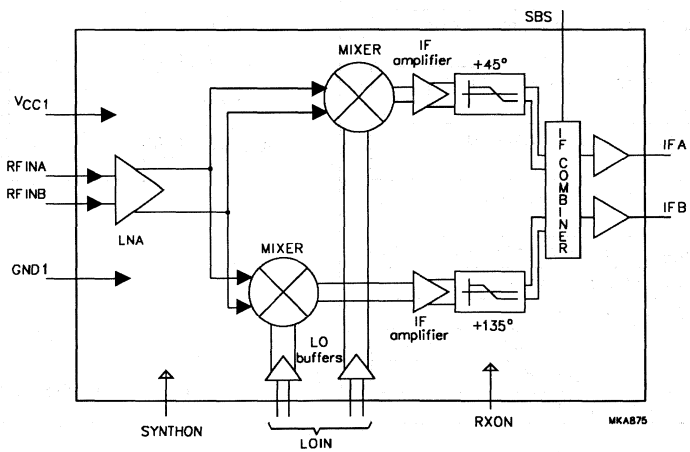


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The LO input impedance is 50 Ω differential.

A synthon mode is used to power-up the buffering on the LO inputs, minimizing the pulling effect on the external VCO when entering transmit or receive modes.

This mode is active when the SYNTHON input is high. Table 1 shows status of circuit in accordance with TXON, RXON and SYNTHON inputs.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 kΩ load. The IF outputs are low impedance (emitter followers).

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON.

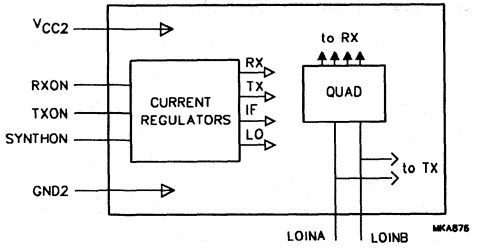


Fig.4 Block diagram, LO section.

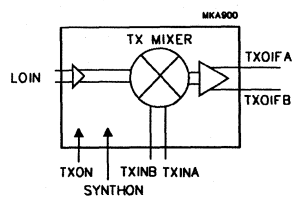


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SYNTHON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	receive section on
HIGH	LOW	LOW	transmit section on
LOW	LOW	HIGH	synthon on mode, transmit and receive LO buffers enabled
LOW	HIGH	HIGH	receive section on and synthon mode active
HIGH	LOW	HIGH	transmit section on and synthon mode active
HIGH	HIGH	LOW	receive and transmit sections on; specification not guaranteed
HIGH	HIGH	HIGH	receive and transmit sections on; specification not guaranteed

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between GND1 and GND2	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	−65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CC1}, V_{CC2}, LOINA and LOINB						
V_{CC}	supply voltage	over full temperature range	3.6	3.75	5.3	V
I_{CCRX}	supply current	receive mode active; DC tested	21	26	32	mA
I_{CCTX}	supply current	transmit mode active; DC tested	9.3	12	14.7	mA
I_{CCSX}	supply current	synthon mode only	4.4	5.6	6.6	mA
I_{CCSRX}	supply current	receive and synthon mode active	22	28	34	mA
I_{CCSTX}	supply current	transmit and synthon mode active	12.5	15.0	19.5	mA
I_{CCPD}	supply current in power-down mode	DC tested	–	0.01	50	μA
Pins: SYNTHON, RXON, TXON and SBS						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} − 0.4 V	−1	–	+1	μA
I_{IL}	LOW level static input current	pin at 0.4 V	−1	–	+1	μA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	2.0	2.2	2.4	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	2.4	3.0	3.6	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	2.1	2.4	2.6	V
Pins: TXOIFA and TXOIFB						
V_O	DC output voltage level	transmit section enabled	1.8	1.9	2.1	V
Pins: LOINA and LOINB						
V_I	DC input voltage level	receive section enabled	2.3	2.5	2.8	V
		transmit section enabled	2.3	2.5	2.8	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RF}	RF input impedance	balanced	–	150	–	Ω
f_{RF}	RF input frequency		925	–	960	MHz
RL_{RF}	return loss on matched RF input	note 1	15	20	–	dB
G_{CP}	conversion power gain	differential RF input to differential IF output matched to 1 kΩ differential	20	23	26	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.2	0.5	dB
$\Delta G/T$	gain variation with temperature	note 2	−20	−15	−10	mdB/K
DES_1	1 dB desensitization input power		–	−30	–	dBm
$CP1_{RX}$	1 dB input compression point	note 1	−24.5	−23.0	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF input differential	differential output; note 2	+30	+40	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	−18	−15	–	dBm
NF_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	3.25	4.30	dB
$Z_{L(IF)}$	typical application IF output load impedance	balanced	–	1	–	kΩ
$C_{L(IF)}$	IF output load capacitance	unbalanced	–	–	2	pF
f_{IF}	IF frequency range	RF < LO	50	71	100	MHz
		RF > LO	50	71	100	MHz
IR	image frequency rejection		30	37	–	dB
Local oscillator section (transmit and receive section enabled, SYNTHON = 1)						
f_{LO}	LO input frequency		850	–	1100	MHz
Z_{LO}	LO input impedance	balanced	–	50	–	Ω
ΔZ_{LO}	impedance change when switching from synthon mode to transmit or receive	mUnits measured on Smith chart	–	20	–	
RL_{LO}	return loss on matched input (including standby mode)	note 2	10	15	–	dB
$P_{i(LO)}$	LO input power level		−7	−4	0	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section enabled)						
Z_O	TX IF output impedance		–	–	200	Ω
Z_L	TX IF load impedance		–	1	–	kΩ
C_L	maximum TX IF load capacitance		–	–	2	pF
$Z_{i(RF)}$	TX RF input impedance	balanced	–	200	–	Ω
f_{TXmix}	TX mixer input frequency		890	–	915	MHz
RL_{TX}	return loss on matched TX input	note 2	15	20	–	dB
G_{CP}	conversion power gain	from 200 Ω to 1 kΩ output	5	7.4	10	dB
$f_{o(TX)}$	TX mixer output frequency		40	–	200	MHz
$CP1_{TX}$	1 dB input compression point		−22	−17.5	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+20	–	dBm
$IP3_{TX}$	3rd order intercept point		−12	−9	–	dBm
NF_{TX}	noise figure	double sideband; note 2	–	9.8	12	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{start}	start-up time of each block		1	5	20	μs

Notes

1. Measured and guaranteed only on UAA2073M demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2073M demonstration board.
3. This value includes printed-circuit board and balun losses on Philips UAA2073M demonstration board over full temperature range.

APPLICATION INFORMATION

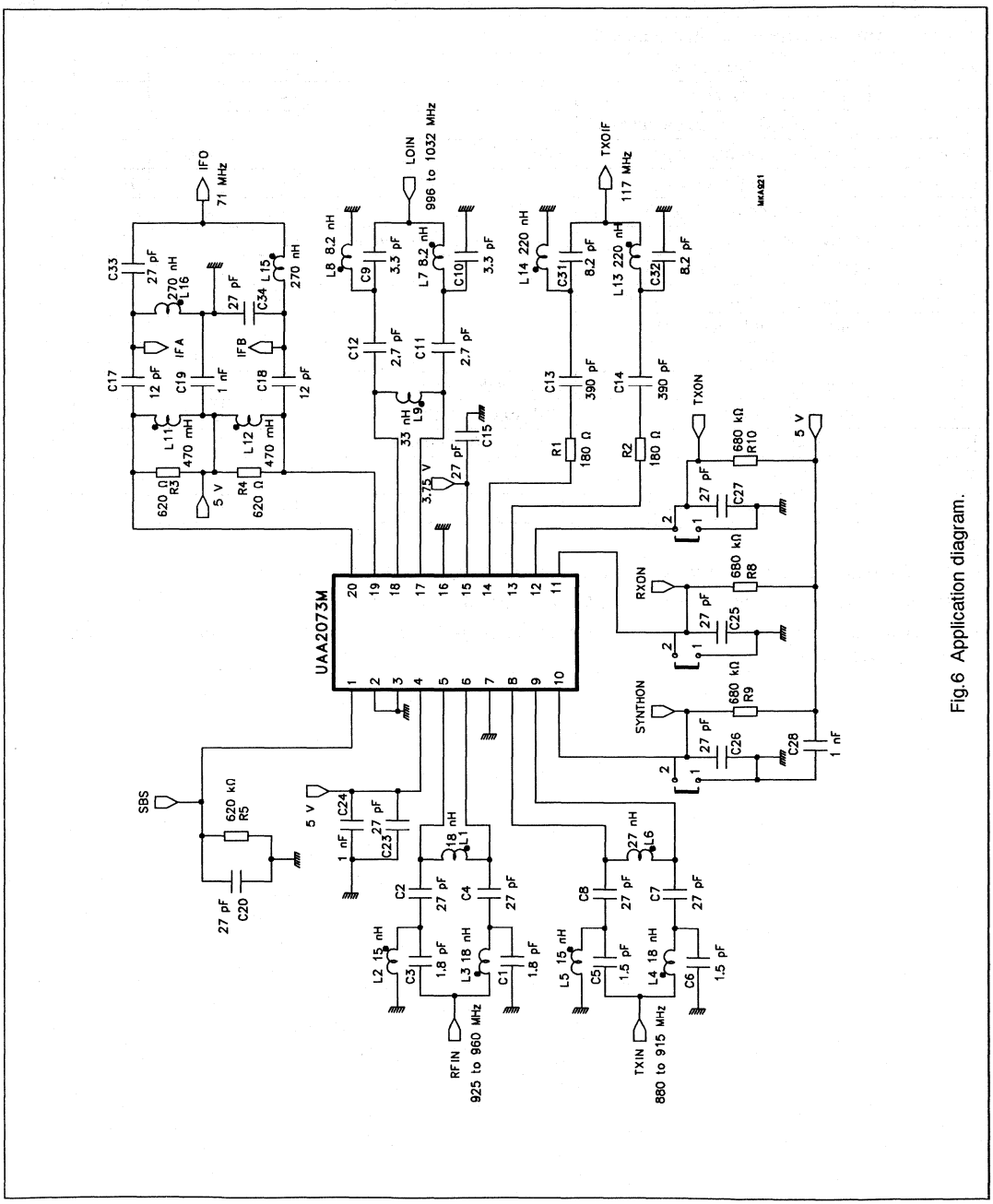


Fig.6 Application diagram.

Table 2 UAA2073M demonstration board parts list

PART	VALUE	SIZE	LOCATION
Resistors			
R1	180 Ω	0805	TXOIF
R2	180 Ω	0805	TXOIF
R3	620 Ω	0805	IF
R4	620 Ω	0805	IF
R5	620 Ω	0805	SBS
R8	680 kΩ	0805	RXON
R9	680 kΩ	0805	SYNTHON
R10	680 kΩ	0805	TXON
Capacitors			
C1	1.8 pF	0805	RFIN
C2	27 pF	0805	RFIN
C3	1.8 pF	0805	RFIN
C4	27 pF	0805	RFIN
C5	1.5 pF	0805	TXIN
C6	1.5 pF	0805	TXIN
C7	27 pF	0805	TXIN
C8	27 pF	0805	TXIN
C9	3.3 pF	0805	LOIN
C10	3.3 pF	0805	LOIN
C11	27 pF	0805	LOIN
C12	27 pF	0805	LOIN
C13	390 pF	0805	TXOIF
C14	390 pF	0805	TXOIF
C15	27 pF	0805	V_{CCLO}
C16	120 pF	0805	V_{CCLO}
C17	12 pF	0805	IF
C18	12 pF	0805	IF
C19	1 nF	0805	IF/V_{CC}
C20	27 pF	0805	SBS
C23	27 pF	0805	V_{CCLNA}
C24	1 nF	0805	V_{CCLNA}
C25	27 pF	0805	RXON
C26	27 pF	0805	SYNTHON
C27	27 pF	0805	TXON
C28	1 nF	0805	V_{CC}
C29	100 nF	1206	V_{CCREG}
C30	100 nF	1206	V_{CCREG}
C31	8.2 pF	0805	TXOIF
C32	8.2 pF	0805	TXOIF
C33	27 pF	0805	IF
C34	27 pF	0805	IF
C35	link	0805	IF/not used
C36	link	0805	IF/not used
Inductors			
L1	18 nH	0805	RFIN
L2	15 nH	0805	RFIN
L3	15 nH	0805	RFIN
L4	15 nH	0805	TXIN
L5	15 nH	0805	TXIN
L6	27 nH	0805	TXIN
L7	8.2 nH	0805	LOIN
L8	8.2 nH	0805	LOIN
L9	33 nH	0805	LOIN/ optional
L10	–	1008	TXOIF/ not required
L11	470 nH	1008	IF
L12	470 nH	1008	IF
L13	220 nH	1008	TXOIF
L14	220 nH	1008	TXOIF
L15	270 nH	0805	IF
L16	270 nH	0805	IF

Other components

COMPONENT	DESCRIPTIONS
IC1	UAA2073M
SMA/RIM	sockets for RF and IF inputs/outputs
SMB	V_{CC} socket (optional in place of IC2)
025 connect	various 2.54 mm (0.1 inch) connectors

Component manufacturers

All surface mounted resistors and capacitors are from Philips Components. The small value capacitors are multilayer ceramic with NPO dielectric. The inductors are from Coilcraft UK.

Image rejecting front-end for GSM applications

UAA2073AM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for at least 30 dB on-chip image rejection
- IF I/Q combination network for 175 MHz
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast **on/off** power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2073AM contains both a receiver front-end and a high frequency transmit mixer intended for GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2073AM is its ability to provide over 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

This means that signals presented at the RF input at LO – IF frequency are rejected through this signal processing while signals at LO + IF frequency can form the IF signal.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection.The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced to reduce EMC issues.

Fast power-up switching is possible. A synthesizer-on (SX) mode enables LO buffers independent of the other circuits. When SXON pin is HIGH, all internal buffers on the LO path of the circuit are turned **on**, thus minimizing LO pulling when remainder of receive chain is powered-up.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2073AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

QUICK REFERENCE DATA

Note 1.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	3.75	5.3	V
$I_{CC(RX)}$	receive supply current	21	26	32	mA
$I_{CC(TX)}$	transmit supply current	9	12	15	mA
NF_{RX}	noise figure on demonstration board (including matching and PCB losses)	–	3.6	4.7	dB
G_{CPRX}	conversion power gain	19	22	25	dB
IR	image frequency rejection	30	45	–	dB
T_{amb}	operating ambient temperature	–30	+25	+75	°C

Note

1. For conditions see Chapters "DC characteristics" and "AC characteristics".

BLOCK DIAGRAM

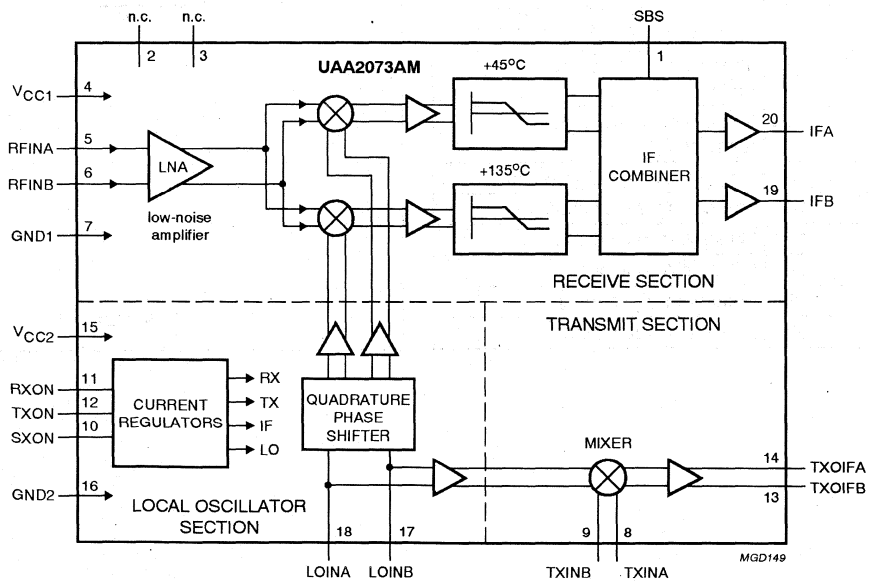


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SBS	1	sideband selection (should be grounded for $f_{LO} < f_{RF}$)
n.c.	2	not connected
n.c.	3	not connected
V_{CC1}	4	supply voltage for receive and transmit sections
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
GND1	7	ground 1 for receive and transmit sections
TXINA	8	transmit mixer input A (balanced)
TXINB	9	transmit mixer input B (balanced)
SXON	10	hardware power-on of LO section (including buffers to RX and TX)
RXON	11	hardware power-on for receive section and LO buffers to RX
TXON	12	hardware power-on for transmit section and LO buffers to TX
TXOIFB	13	transmit mixer IF output B (balanced)
TXOIFA	14	transmit mixer IF output A (balanced)
V_{CC2}	15	supply voltage for LO section
GND2	16	ground 2 for LO section
LOINB	17	LO input B (balanced)
LOINA	18	LO input A (balanced)
IFB	19	IF output B (balanced)
IFA	20	IF output A (balanced)

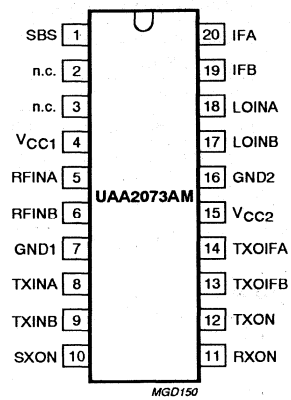


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type. The whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin SBS allows sideband selection:

- $f_{LO} > f_{RF}$ (SBS = 1)
- $f_{LO} < f_{RF}$ (SBS = 0).

Where f_{RF} is the frequency of the wanted signal.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF differential input impedance is 150 Ω (parallel real part), choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type, tuned for 175 MHz. Typical application will load the output with a 680 Ω resistor load at each IF output, plus a 1 kΩ load consisting in the input impedance of the IF filter or in the input impedance of the matching network for the IF filter. The power gain refers to the available power on this 1 kΩ load. The path to V_{CC} for the DC current should be achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, **on/off**, of the receive section is controlled by the hardware input RXON.

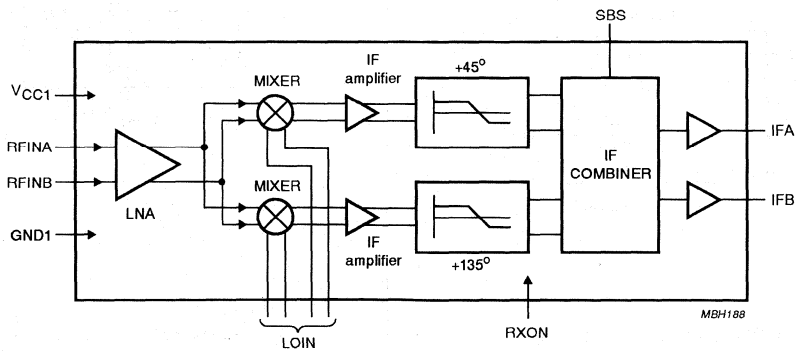


Fig.3 Block diagram, receive section.

Local oscillator section

The Local Oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The LO differential input impedance is 50 Ω (parallel real part).

A synthesizer-on (SX) mode is used to power-up the buffering on the LO inputs, minimizing the pulling effect on the external VCO when entering transmit or receive modes.

This mode is active when the SXON input is HIGH. Table 1 shows status of circuit in accordance with TXON, RXON and SXON inputs.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 kΩ load. The IF outputs are low impedance (emitter followers).

Fast switching, **on/off**, of the transmit section is controlled by the hardware input TXON.

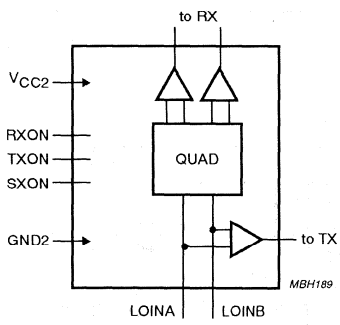


Fig.4 Block diagram, LO section.

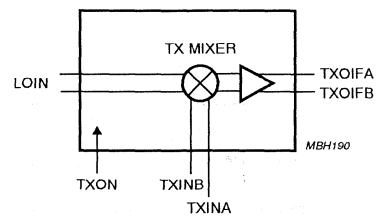


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	**RXON**	**SXON**	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	RX mode: receive section and LO buffers to RX **on**
HIGH	LOW	LOW	TX mode: transmit section and LO buffers to TX **on**
LOW	LOW	HIGH	SX mode: complete LO section **on**
LOW	HIGH	HIGH	SRX mode: receive section **on** and SX mode active
HIGH	LOW	HIGH	STX mode: transmit section **on** and SX mode active
HIGH	HIGH	LOW	receive and transmit sections **on**; specification not guaranteed
HIGH	HIGH	HIGH	receive and transmit sections **on**; specification not guaranteed

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between GND1 and GND2	–	0.6	V
$P_{i(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in stagnant air	–	250	mW
T_{stg}	IC storage temperature	–65	+150	°C

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

DC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CC1} and V_{CC2}						
V_{CC}	supply voltage	over full temperature range	3.6	3.75	5.3	V
$I_{CC(RX)}$	supply current in RX mode		21	26	32	mA
$I_{CC(TX)}$	supply current in TX mode		9	12	15	mA
$I_{CC(SX)}$	supply current in SX mode		4.5	5.8	7.0	mA
$I_{CC(SRX)}$	supply current in SRX mode		23	28	34	mA
$I_{CC(STX)}$	supply current in STX mode		12.5	15.0	19.5	mA
$I_{CC(PD)}$	supply current in power-down mode		–	0.01	50	μA
Pins: SXON, RXON, TXON and SBS						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	μA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	μA
Pins: RFINA and RFINB						
$V_{I(RFIN)}$	DC input voltage level	receive section **on**	2.0	2.2	2.4	V
Pins: IFA and IFB						
$I_{O(IF)}$	DC output current	receive section **on**	2.3	3.0	3.8	mA
Pins: TXINA and TXINB						
$V_{I(TXIN)}$	DC input voltage level	transmit section **on**	2.1	2.4	2.6	V
Pins: TXOIFA and TXOIFB						
$V_{O(TXOIF)}$	DC output voltage level	transmit section **on**	1.8	1.9	2.1	V
Pins: LOINA and LOINB						
$V_{I(LOIN)}$	DC input voltage level	receive section **on**	2.3	2.5	2.8	V
		transmit section **on**	2.3	2.5	2.8	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = −30 to +75 °C; unless otherwise specified.

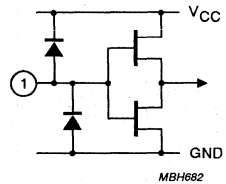
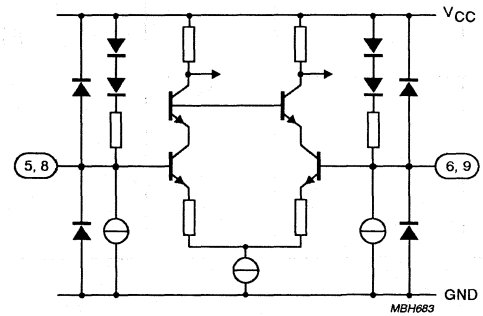
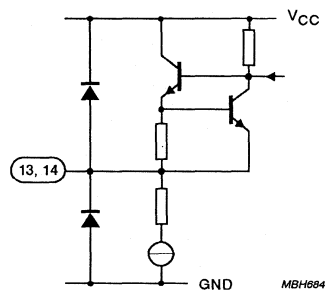
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section on)						
R_{iRX}	RF input resistance (real part of the parallel input impedance)	balanced; at 942.5 MHz	–	150	–	Ω
C_{iRX}	RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 942.5 MHz	–	1	–	pF
f_{iRX}	RF input frequency		925	–	960	MHz
RL_{iRX}	return loss on matched RF input	note 1	15	20	–	dB
G_{CPRX}	conversion power gain	differential RF input to differential IF output matched to 1 kΩ differential	19	22	25	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.2	0.5	dB
ΔG/T	gain variation with temperature	note 2	−20	−15	−10	mdB/K
DES1	1 dB desensitization input power	interferer frequency offset 3 MHz	–	−30	–	dBm
$CP1_{RX}$	1 dB input compression point	note 1	−25	−23.0	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	−21.5	−15	–	dBm
NF_{RX}	overall noise figure	RF input to differential IF output; note 3				
		T_{amb} = +25°C	–	3.6	4.0	dB
		over full temperature range	–	–	4.7	dB
R_{LRX}	typical application IF output load impedance	balanced	–	1000	–	Ω
C_{LRX}	IF output load capacitance	unbalanced	–	–	2	pF
f_{oRX}	IF frequency range		–	175	–	MHz
IR	image frequency rejection	$f_{LO} < f_{RF}$	30	45	–	dB

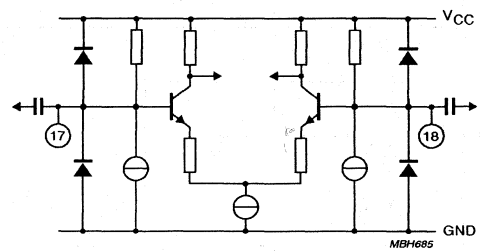
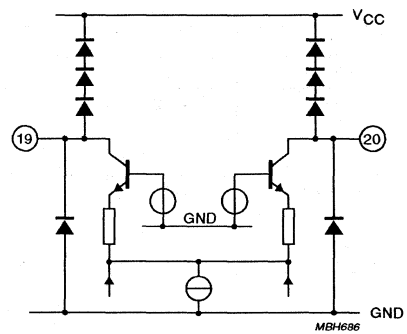
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Local oscillator section (RXON or TXON or SXON = 1)						
f_{iLO}	LO input frequency		750	–	785	MHz
R_{iLO}	LO input resistance (real part of the parallel input impedance)	balanced; at 767.5 MHz	–	80	–	Ω
C_{iLO}	LO input capacitance (imaginary part of the parallel input impedance)	balanced; at 767.5 MHz	–	2	–	pF
RL_{iLO}	return loss on matched input (including power-down mode)	note 2	10	15	–	dB
ΔRL_{iLO}	return loss variation between SX, SRX and STX modes	linear S_{11} variation; note 1	–	20	–	mU
P_{iLO}	LO input power level		−7	−4	0	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 2	40	–	–	dB
Transmit section (transmit section on)						
Z_{oTX}	TX IF output impedance		–	–	200	Ω
Z_{LTX}	TX IF load impedance		–	1	–	kΩ
C_{LTX}	TX IF load capacitance		–	–	2	pF
R_{iTX}	TX RF input resistance (real part of the parallel input impedance)	balanced; at 897.5 MHz	–	200	–	Ω
C_{iTX}	TX RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 897.5 MHz	–	1	–	pF
f_{iTX}	TX input frequency		880	–	915	MHz
RL_{iTX}	return loss on matched TX input	note 1	15	20	–	dB
G_{CPTX}	conversion power gain	from 200 Ω to 1 kΩ output; note 2	5	7.4	10	dB
f_{oTX}	TX output frequency		40	–	200	MHz
$CP1_{TX}$	1 dB input compression point	note 1	−22	−17.5	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+20	–	dBm
$IP3_{TX}$	3rd order intercept point		−12	−9	–	dBm
NF_{TX}	noise figure	double sideband; notes 2 and 3	–	9.8	12	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{start}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on Philips UAA2073AM demonstration board at T_{amb} = 25 °C.
2. Measured and guaranteed only on Philips UAA2073AM demonstration board.
3. This value includes printed-circuit board and balun losses on Philips UAA2073AM demonstration board over full

INTERNAL PIN CONFIGURATION

PIN	SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
1	SBS		
10	SXON		
11	RXON		
12	TXON		
4	V_{CC1}	+3.75	
15	V_{CC2}	+3.75	
7	GND1	0	
16	GND2	0	
5	RFINA	+2.2	
6	RFINB	+2.2	
8	TXINA	+2.4	
9	TXINB	+2.4	
13	TXOIFB	+1.9	
14	TXOIFA	+1.9	

PIN	SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
17	LOINB	+2.5	
18	LOINA	+2.5	
19	IFB	+3.0	
20	IFA	+3.0	

APPLICATION INFORMATION

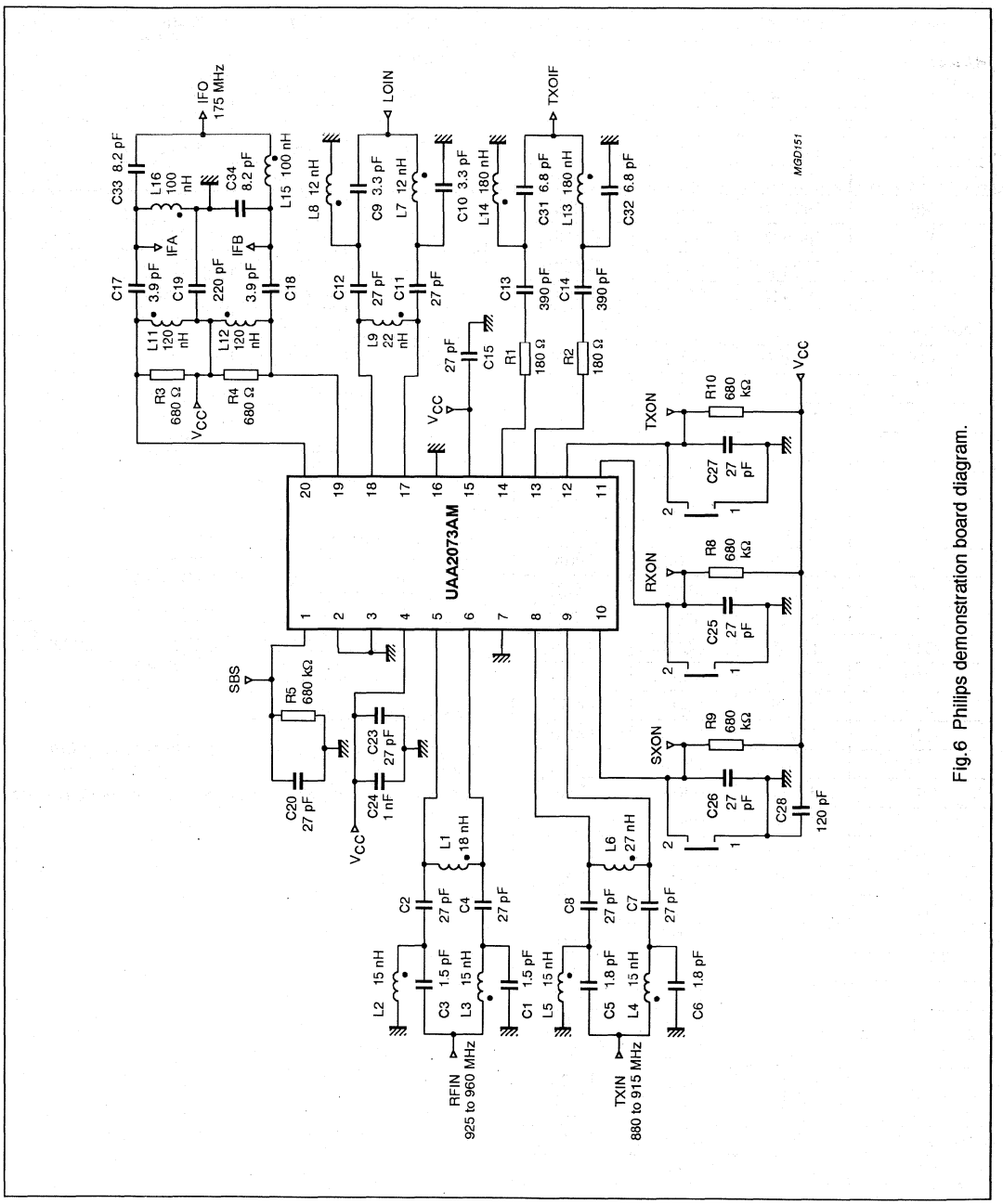


Fig.6 Philips demonstration board diagram.

Table 2 UAA2073AM demonstration board parts list

PART	VALUE	SIZE	LOCATION
Resistors			
R1	180 Ω	0805	TXOIF
R2	180 Ω	0805	TXOIF
R3	680 Ω	0805	IFO
R4	680 Ω	0805	IFO
R5	680 kΩ	0805	SBS
R8	680 kΩ	0805	RXON
R9	680 kΩ	0805	SXON
R10	680 kΩ	0805	TXON
Capacitors			
C1	1.5 pF	0805	RFIN
C2	27 pF	0805	RFIN
C3	1.5 pF	0805	RFIN
C4	27 pF	0805	RFIN
C5	1.8 pF	0805	TXIN
C6	1.8 pF	0805	TXIN
C7	27 pF	0805	TXIN
C8	27 pF	0805	TXIN
C9	3.3 pF	0805	LOIN
C10	3.3 pF	0805	LOIN
C11	27 pF	0805	LOIN
C12	27 pF	0805	LOIN
C13	390 pF	0805	TXOIF
C14	390 pF	0805	TXOIF
C15	27 pF	0805	V_{CCLO}
C17	3.9 pF	0805	IFO
C18	3.9 pF	0805	IFO
C19	220 pF	0805	IF/V_{CC}
C20	27 pF	0805	SBS
C23	27 pF	0805	V_{CCLNA}
C24	1 nF	0805	V_{CCLNA}
C25	27 pF	0805	RXON
C26	27 pF	0805	SXON
C27	27 pF	0805	TXON
C28	120 pF	0805	V_{CC}
C31	6.8 pF	0805	TXOIF
C32	6.8 pF	0805	TXOIF
C33	8.2 pF	0805	IFO
C34	8.2 pF	0805	IFO

PART	VALUE	SIZE	LOCATION
Inductors			
L1	18 nH	0805	RFIN
L2	15 nH	0805	RFIN
L3	15 nH	0805	RFIN
L4	15 nH	0805	TXIN
L5	15 nH	0805	TXIN
L6	27 nH	0805	TXIN
L7	12 nH	0805	LOIN
L8	12 nH	0805	LOIN
L9	22 nH	0805	LOIN
L11	120 nH	1008	IFO
L12	120 nH	1008	IFO
L13	180 nH	0805	TXOIF
L14	180 nH	0805	TXOIF
L15	100 nH	1008	IFO
L16	100 nH	1008	IFO

Other components

COMPONENT	DESCRIPTIONS
IC1	UAA2073AM
SMA/RIM	sockets for RF and IF inputs/outputs
SMB	V_{CC} socket

Component manufacturers

All surface mounted resistors and capacitors are from Philips Components. The small value capacitors are multilayer ceramic with NPO dielectric. The inductors are from Coilcraft UK.

Image rejecting front ends

AN96106

Muriel Gombaud

Abstract

The UAA2072M, UAA2073M, UAA2073AM, UAA2077AM, UAA2077BM and UAA2077CM are low power integrated front–ends with on–chip image rejection. This further integration level permits to reduce significantly radio designs cost and time.

This report contains background information related to image rejection, a detailed description of the ICs, a worked–out application example and measurement results.

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Summary

This report is intended to provide application support for designing image rejecting front–ends with the UAA2072M, UAA2073M, UAA2073AM, UAA2077AM, UAA2077BM and UAA2077CM integrated circuits from Philips Semiconductors.The first of the line, the UAA2072M, has been developed for GSM applications. The UAA2073M and UAA2073AM are derivatives from the UAA2072M and hence closely related. The UAA2077AM, UAA2077BM and UAA2077CM are based on the same structure but are intended for use in 2GHz applications. They permit low power applications and eliminate the need for an external bulky ceramic filter required for image rejection.They contain a receiver front–end and a high frequency transmit mixer (not on the UAA2077AM).

Chapter 1 covers complete theoretical background of image rejection. Chapters 2 and 3 contain a general and functional description of these ICs. Chapter 4 gives useful equations, which have been utilized for impedance matching. A worked–out application example, based on the UAA2077BM is given in Chapter 5. The related schematics, layout and assembly drawings can be found in Chapter 7. Matching results, image rejection, IP3 and all relevant RF characteristics of the circuits are included in Chapter 6, to aid in proper circuit design.

Since it was not possible to give, for each topic, the features of the all 6 ICs, it was decided to take into account only one circuit at a time as an example.

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1. BASIC THEORY OF IMAGE REJECTION

In a conventional heterodyne receiver, the incoming signal is amplified with a single stage of tuned RF amplifier and mixed with an adjustable local oscillator (LO) to produce a signal at a fixed intermediate frequency (IF). A selective RF filter is then needed to attenuate all frequencies outside the band of interest.

Let's consider the case of the following reception : the LO frequency is lower than the RF wanted frequency.

A simple application for the 935 to 960 MHz GSM band is shown below. Assuming that the IF frequency is chosen equal to 70 MHz, this leads to the values of 865 to 890 MHz for the LO frequency. The image frequency band, placed at 140 MHz away from the desired band is at 795 to 820 MHz. The signal at LO–IF frequency, presented at the RF input has to be rejected while the signal at LO+IF must go through the reception chain. On the same way, the lower side band can be also rejected.

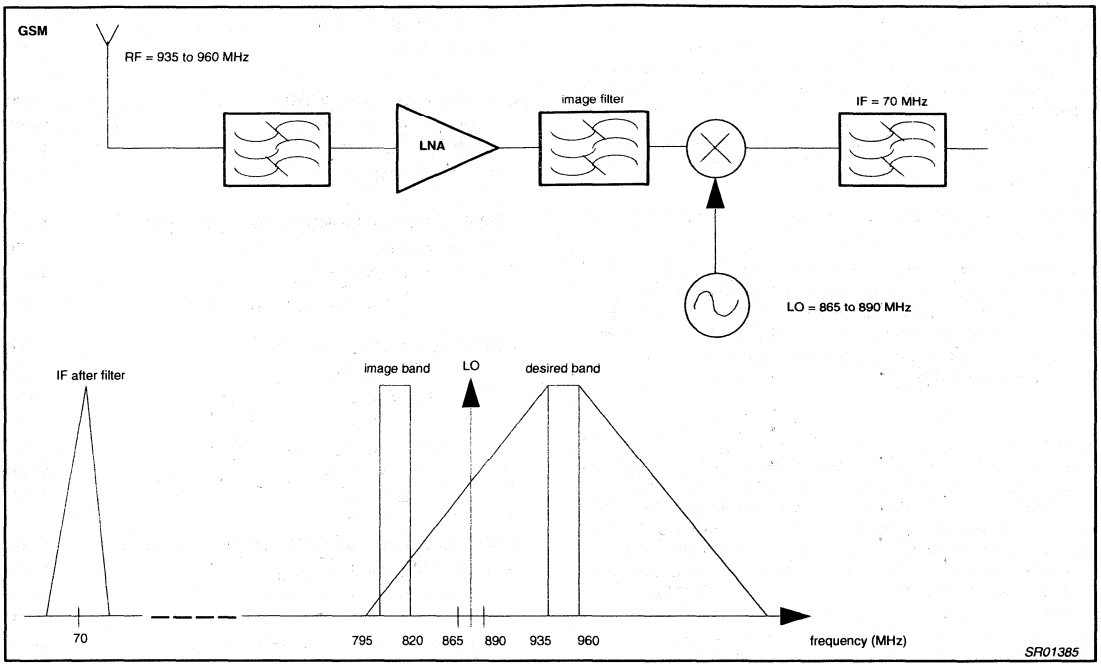


Figure 1. Heterodyne radio receiver and frequency plan

Another way to suppress response at the image frequency is to use an image reject mixer. The basic principle is to use phase cancellation instead of frequency selective attenuation. The basic circuit consists of a pair of mixers, driven from a quadrature LO source, a 905 phase shifter and a power combiner, as shown below :

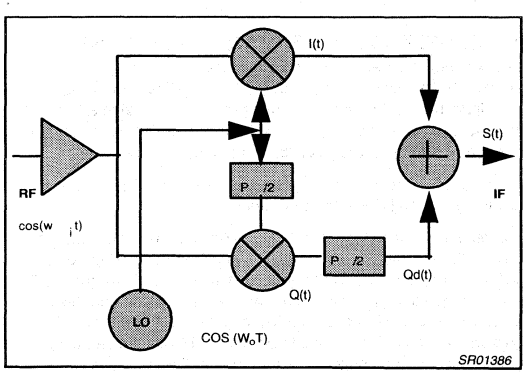


Figure 2. Image reject mixers

To understand how the process of image rejection with this circuit is done, let's follow the mathematics equations behind that :

The signal **I(t)**, corresponding to the in–phase mixer product is equal to :
$I(t) = \cos(\omega_i t)*\cos(\omega_o t) = 1/2\ (\cos(\omega_i - \omega_o)t + \text{sum frequency}) = 1/2 \cos(\omega_d t)$
with $\omega_d = \omega_i - \omega_o > 0$, considering the case of the RF wanted signal above the LO signal.

The signal **Q(t)**, related to the quadrature mixer product is :
$Q(t) = \cos(\omega_i t)*\cos(\omega_o t - 90°) = 1/2 \cos(\omega_d t + 90°) = -1/2 \sin(\omega_d t)$

The quadrature shifter, introduced in one path, produces a signal **Qd(t)** such as :
$Q_d(t) = -1/2 \sin(\omega_d t - 90°) = 1/2 \cos(\omega_d t)$

The signal **S(t)** , after summing the in–phase and quadrature signals is :
$S(t) = Q_d(t) + I(t) = \cos \omega_d t$, provided that ω_i is the RF frequency and $\omega_d = \omega_i - \omega_o > 0$
Now, assume that $\omega_d = \omega_i - \omega_o < 0$ ω_i is the image frequency
$I(t) = 1/2 \cos(-\omega_d t) = 1/2 \cos(\omega_d t)$
$Q(t) = 1/2 \cos(-\omega_d t + 90°) = 1/2 \sin(\omega_d t)$
$Qd(t) = 1/2 \sin(\omega_d t - 90°) = -1/2 \cos(\omega_d t)$
Sum I(t) and $Q_d(t)$: $S(t) = 1/2 \cos(\omega_d t) - 1/2 \cos(\omega_d t) = 0$

2. INTRODUCTION TO THE IMAGE REJECTING FRONT ENDS

This chapter provides an overview of this IC family and follows with detailed description, specific to each circuit.

Image rejecting front ends AN96106

The UAA2072M was the first IC in the image rejection family. To satisfy the need of the emerging digital mobile communications equipment, a family of image rejecting front–end IC's based around the UAA2072M has been developed : the UAA2073M and UAA2073AM dedicated for GSM and the UAA2077AM, UAA2077BM and UAA2077CM dedicated for 2 GHz applications. A simplified block–diagram, representing the main common functionalities of these circuits is shown in Fig. 3. The IC is divided into three main blocks : the receive, transmit and local oscillator sections. The transmit block is not integrated in the UAA2077AM.

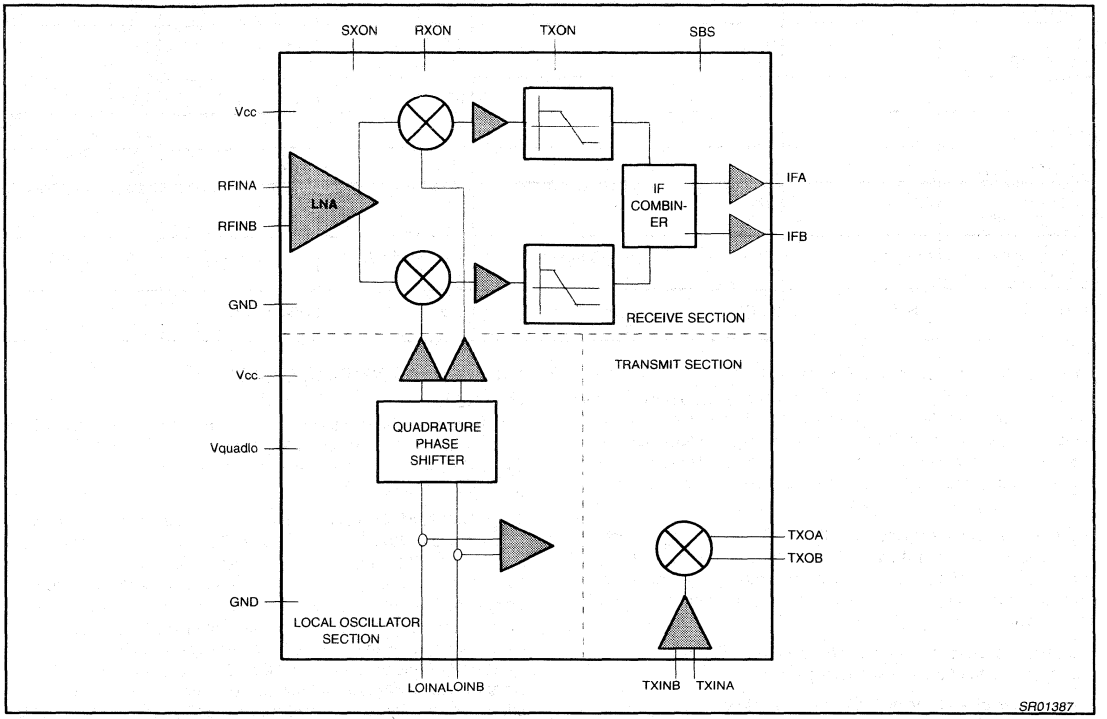


Figure 3. Block–diagram

The circuits present the following common features :

2.1 Common Features

- low–noise, wide dynamic range amplifier
- double balanced image reject mixing
- integrated Rx and Tx blocks
- IF I/Q combiner
- on–chip quadrature network
- low–power consumption
- very low–noise figure
- small package SSOP20
- ***very small application (no image filter)***

All relevant parameters are summed up in the following table :

Table 1. Quick reference data

	UAA2072M	UAA2073M	UAA2073AM	UAA2077AM	UAA2077BM	UAA2077CM
V_{CC} (V)	4.5 to 5.3	3.6 to 5.5	3.6 to 5.3	3.15 to 5.3	3.6 to 5.3	3.6 to 5.3
I_{CRX}(MA)	31.5	26	26	27	27	36
RX Noise Figure (dB)	4	3.25	3.6	4.3	4.3	4.0
Gain (dB)	26	23	22	20	20	23
IP3 (dBm)	–15	–15	–15	–17	–17	–17
CP1 (dBm)	–24.5	–23	–23	–232	–23	–24
Image Rejection (dB)	35	37	45	32	32	38
IF frequency (MHz)	program	71 (nominal)	A75 (nominal)	110 (nominal)	188 (nominal)	188 (nominal)
Application	GSM	GSM	GSM	DECT	DCS1800	DCS1800/ PCS1800

Table 1 Quick reference data

All these circuits comprise an LNA and an image reject mixer. In the previous equipment designs generation, this RF part was composed of discrete LNA, mixer and image filter. This higher integration level reduces variation of RF performance in production. Therefore, high frequency radio manufacturability is eased so that reliability and reproducibility are thus improved.

The image reject mixer gives typically over 30 dB of image rejection (see Table 1). This means little RF input filtering is necessary, enabling the use of only one low–cost RF input filter. Moreover, the removal of the bulky expensive ceramic image filter enables smaller phone designs.

The performance is such that all critical RF parameters are stable over the entire temperature and voltage ranges.

Particularities of each circuit are described below.

2.2 the UAA2072M

Its supply voltage ranges from 4.5 to 5.3 V ; it is intended to be used in the GSM cellular telephones. To adjust for maximum image rejection performance at a given IF, a control logic programmable via the 3–wire serial bus interface is provided. This permits indeed compensation for process spreads and trimming for the chosen IF frequency and the LO band center frequency. The power–up of the transmit, receive and LO buffers as well as the selection of sideband rejection are also programmable by the 3–wire serial bus.

2.3 the UAA2073M and UAA2073AM

The UAA2073M is the second generation front–end for 900 MHz applications. It offers better performance than the UAA2072M.

The supply voltage range is lower, from 3.6 to 5.3 V with a typical 3.75 V supply. The power consumption has been improved to 26 mA typically in receive mode. The whole control block for tuning image rejection has been suppressed. The image rejection is optimum when the IF frequency is equal to 71 MHz.

The UAA2073AM is a derivative of the UAA2073M, with an IF frequency equal to 175 MHz. The image frequency rejection has been improved to 45 dB but at the expense of a reduced range of possible IF frequencies.

2.4 the UAA2077AM, UAA2077BM and UAA2077CM

In order to meet the rapidly increasing demand for mobile radio 1800 MHz equipment, the UAA2077AM, the UAA2077BM and UAA2077CM have been developed and have become the new generation of image rejection ICs.

The UAA2077AM is intended for use in the digital cordless system DECT, the UAA2077BM and UAA2077CM in the digital cellular systems DCS1800 and PCS1900. One particularity of the UAA2077AM is that it doesn't include a transmit block. One the other hand, the voltage supply can be reduced up to 3.15 V for temperature from 0 to 70 °C. This offers the possibility to connect directly the chip to an unregulated 3–cell battery supply. The UAA2077BM has been designed for DCS1800 applications. The UAA2077CM, a derivative of that IC, was designed initially to address the stringent requirements of PCS1900 applications, but is also suitable for DCS1800 applications.

3. FUNCTIONAL DESCRIPTION

3.1 Power–down modes

The UAA2072M is the only one of this ICs' family to feature software power–down modes. For the five other circuits, several power–down modes are exclusively controlled by hardware input pins. Let's take the example of the UAA2073M. According to the block–diagram, 3 different functional areas are defined:

- the receive section
- the transmit section
- the local–oscillator section

For minimizing the pulling effect on the external VCO when entering in the receive or transmit modes, a special mode of operation has been created : the synthesizer–ON (synthon) mode . This mode is used to power–up the buffering on the LO inputs. The whole local oscillator section is thus turned **on**; this includes the quadrature phase shifter and buffers.

When the transmit mode is active, the down conversion mixer and the low–noise amplifier, including in the transmit section are turned **on**. The LO buffer (from the LO section) is also needed to drive the transmit IF down conversion mixer and has to be powered–on.

For the receive mode, the whole receive section is turned **on**, just as the quadrature phase shifter and the LO buffer on the path.

For example, a typical cellular transceiver would first assert SXON, to power–up LO buffers and allow VCO to stabilize, followed some time later by RXON being asserted just before the wanted signal arrives. At the end of the receive burst, RXON only is de–activated to power–down the receiver. The circuit is left in SX mode, as following slots will be used for example for transmitting. The circuit will enter TX mode when TXON is asserted. When the complete transceiver re–enters IDLE mode (no active call), the IC is returned to power down mode by de–activating SXON, RXON and TXON.

The different modes of operation are then defined as follows:

- the RX mode : the receive section and LO buffers to RX are **on**
- the TX mode : the transmit section and LO buffers to TX are **on**
- the Synthon mode : the complete LO section is **on**
- the SRX mode : the receive section is **on** and the Synthon mode active
- the STX mode : the transmit section is **on** and the Synthon mode active

The control of these different power status is done by hardware, with the pins TXON, RXON and SYNTHON.

Different logical combinations allow a selection of all the modes defined above (see Table 2).

Table 2. Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SYNTHON	
LOW	LOW	LOW	power–down mode
LOW	HIGH	LOW	RX mode
HIGH	LOW	HIGH	TX mdoe
LOW	LOW	HIGH	Synthon mode
LOW	HIGH	HIGH	SRX mode
HIGH	LOW	HIGH	STX mode
HIGH	HIGH	LOW	receive and transmit sections on; specification not guaranteed
HIGH	HIGH	HIGH	receive and transmit sections on; specification not guaranteed

Figure 4 Shows These Modes of Operation.

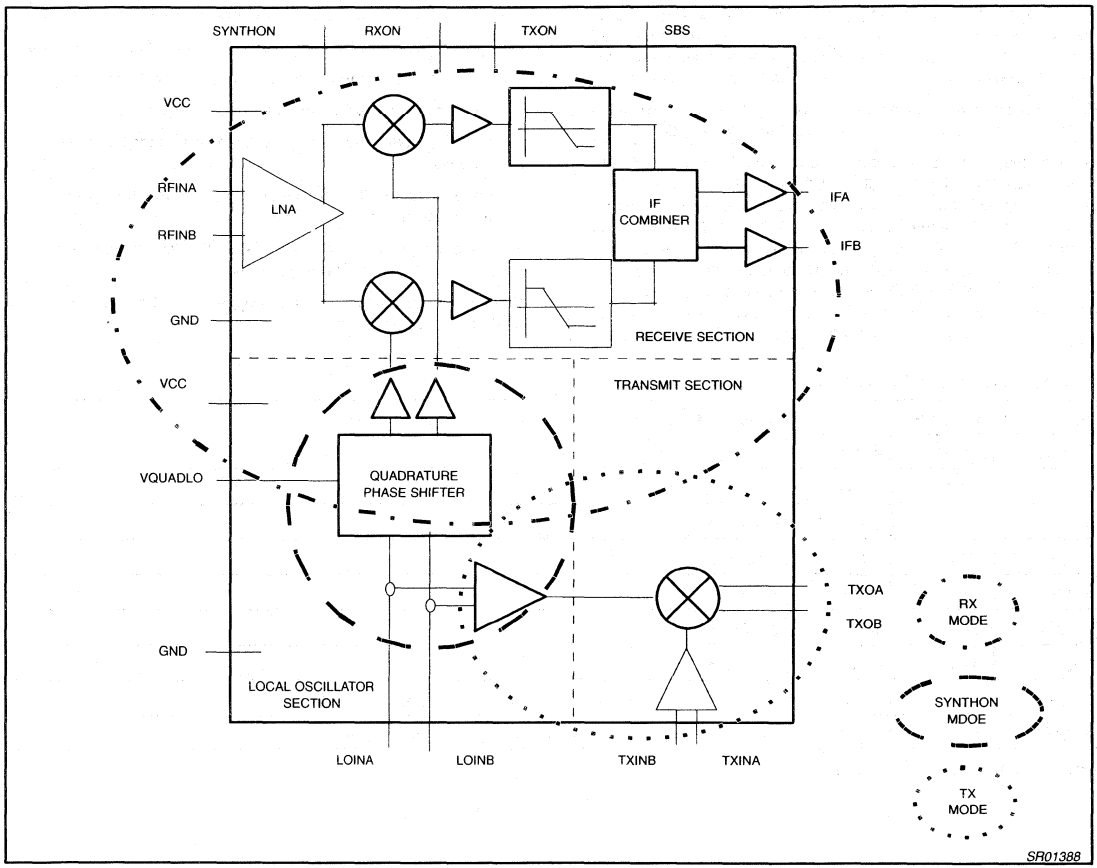


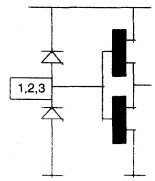
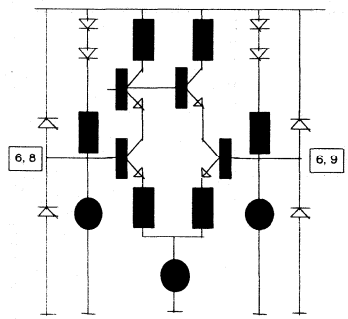
Figure 4. Power–down modes

Power–down modes for the UAA2077AM/BM/CM operate in the same way. The SYNTHON pin is named in that case the SXON pin and refers to the SX mode (instead of Synthon).

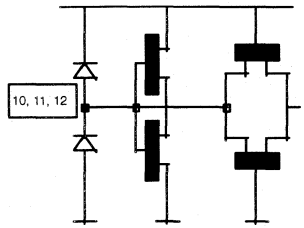
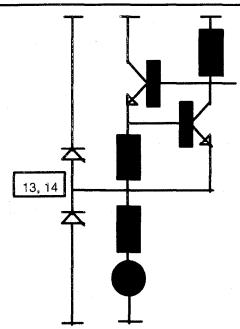
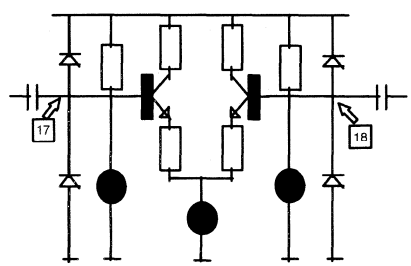
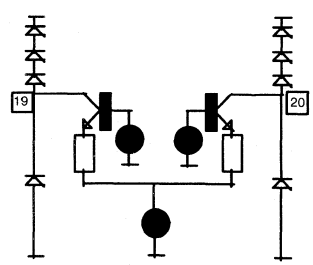
3.2 Pin Function Diagram

The following table shows the equivalent circuit per pin for the UAA2072M. An analogy can be made for the pins functions diagrams of the UAA2073M/AM and UAA2077AM/BM/CM.

- the equivalent circuits related to the LO, RF, TX inputs and IF outputs are common for all ICs.
- the TX output on the UAA2077BM/CM is identical to the IF output on the UAA2072M.
- the TX output of the UAA2073M/AM is identical to the TX output of the UAA2072M.
- the TXON, RXON and SXON pin diagrams on UAA2073M/AM and UAA2077AM/BM/CM are similar to the CLK, DATA and $\overline{E}$ ones on the UAA2072M.

PIN N		DCV	EQUIVALENT CIRCUIT
1	CLK		
2	DATA		
3	$\overline{E}$		
5	RFNA	+2.1	
6	RFNB	+2.1	
8	TXINA	+2.2	
9	TXNB	+2.2	

SR01389

PIN N	PIN MNEMONIC	DCV	EQUIVALENT CIRCUIT
10	TEST		
11	RXON		
12	TXON		
13	TXOIFB	+2.8	
14	TXOIFA	+2.9	
17	LOINB	+4.8	
18	LOINA	+4.8	
19	IFB	+2.5	
20	IFA	+2.5	

3.3 Phase shifter

The principle of phase shifting, implemented in the image rejecting front–ends is based on all–pass filters.

The basic cell is then as follows :

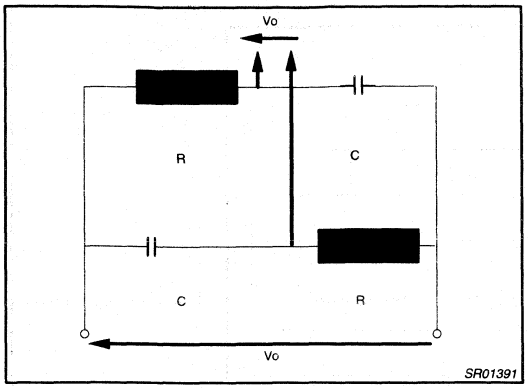


Figure 5. All–Pass Filter

From the equations associated with the circuit, it can be easily deduced that :

$$|Vo| = |Vi|$$

$Df = -2\arctan(RCw)$

For the LO quadrature phase shifter, two cells of such type are used, one set to 45 ° and the other to 135 ° and work in their linearity zone. Graphs of simulated LO phase shift are given so that exact quadrature phase can be obtained for a given LO frequency (see Fig. 6 and Fig. 7).

The design procedure for phase–shifting on the I and Q channels is similar.

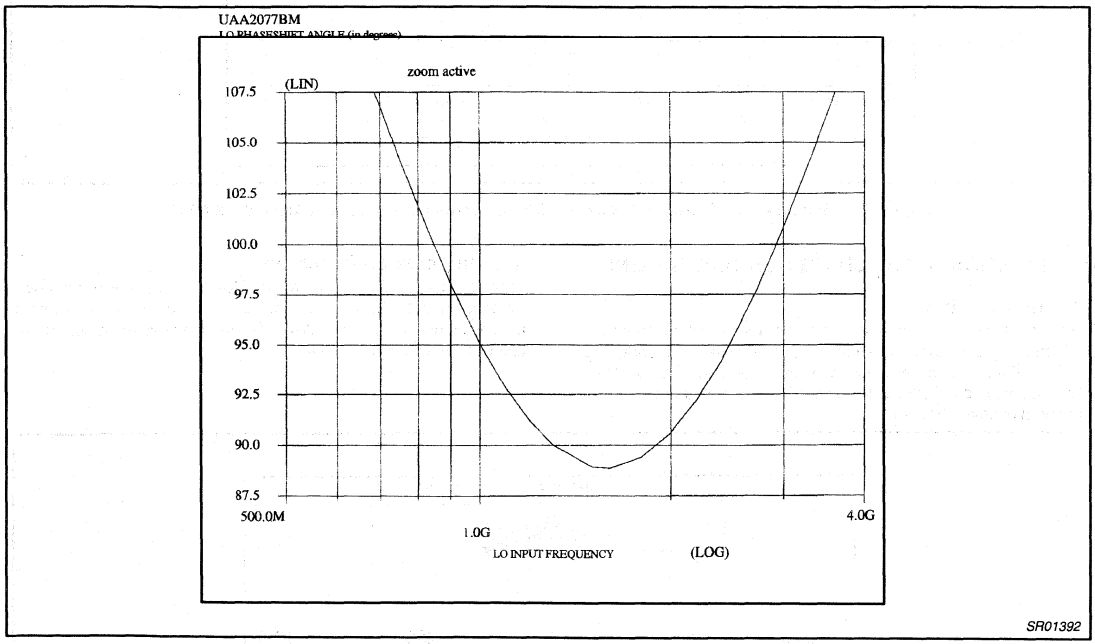


Figure 6. Simulated LO Phase Shift Versus LO Input Frequency

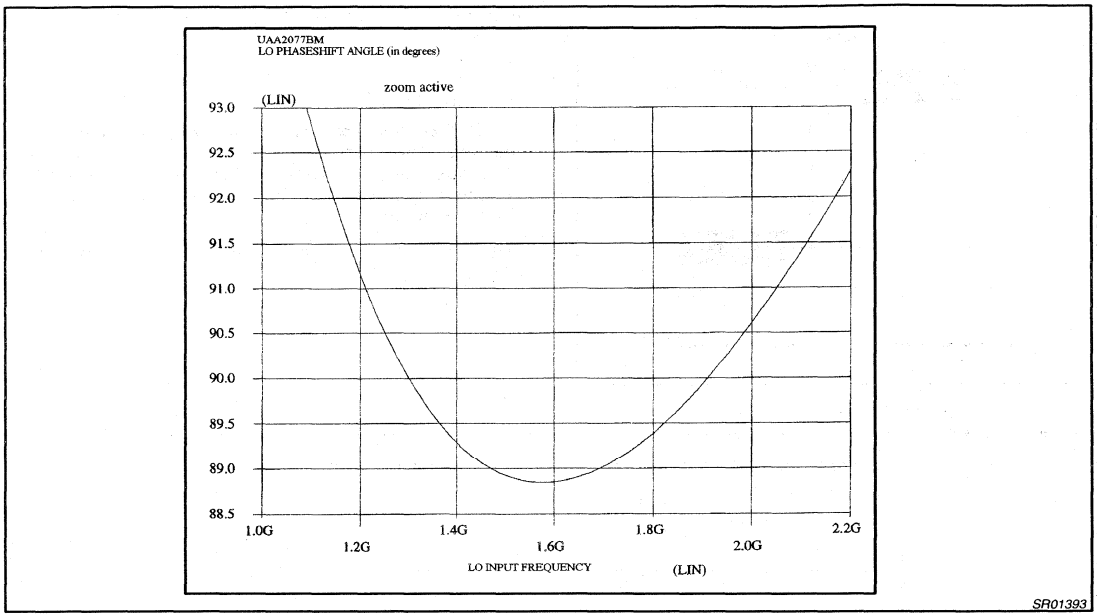


Figure 7. Simulated LO Phase Shift Versus LO Input Frequency (Magnified Around 1.6 GHz)

4. IMPEDANCE MATCHING CONSIDERATIONS

4.1 Introduction

Transfer of power between a source and its load must be done with a minimum of loss, particulary if the originated signal is already very low. Therefore, special care must be taken for impedance matching when designing a RF circuit. The aim is indeed to enable a maximum of power transfer.

4.2 Impedance Matching

Let's assume first that the source and load impedances are purely resistive equal to RS and RL. A matching can be easily done with a L–network design, shown below . It is the simplest and most widely used circuit as a matching circuit :

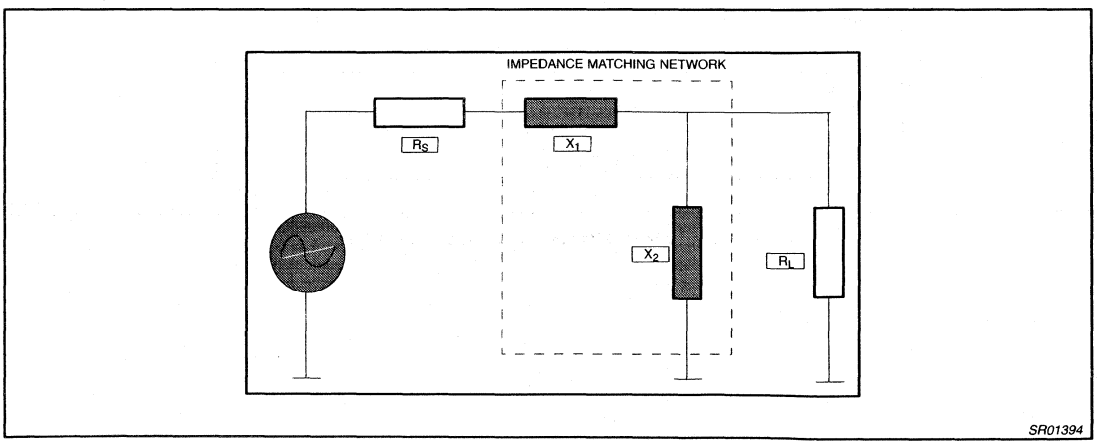


Figure 8. L–network Circuit

RS : source resistance

RL : load resistance

X1 : series reactance

X2 : parallel reactance

Let's now introduce the equations, which can be used to design this network.

Dealing with the quality factor Q, the following equations provide a simple and quick solution.

Determine the Q factors from

$$Q1 = Q2 = \sqrt{\frac{RL}{RS} \pm 1}$$

Determine X1 and X2 from

Q1 = X1 / RS Q2 = RL / X2

Since there are 2 possible arrangements of the L and C components, X1 and X2 can be either capacitive or inductive reactance; it depends on the configuration required, low–pass or high–pass.

In most cases, the impedance is rarely purely resistive. Source and load impedances are almost always complex, i.e. they contain both resistive and reactive components. Therefore, it is also necessary to handle these stray reactances.

Two basic approaches can be used : the stray reactances present in the source and load can be absorbed in the matching network when the stray element values are smaller than the calculated element values. If not, they can be resonated with an equal and opposite reactance. This is the basic of any matching design, to make the source drive its complex conjugate as a load impedance The reactive parts thus cancel each other and leave only RS and RL . If RS and RL are equal, maximum power transfer is achieved.

4.3 Balun Design

A balun is a device for matching an unbalanced line (e.g. a coax) to a balanced load (e.g. an antenna).

The standard configuration of all baluns utilized in our application is depicted in Fig. 9.

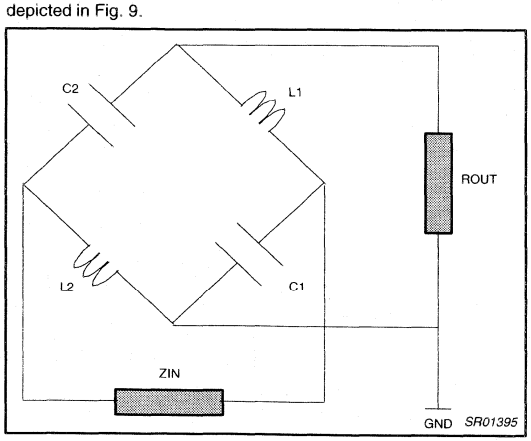


Figure 9. Balun Circuit

Since Rout represents the output impedance of the generator, it is always resistive (e.g. 50 Ω). Zin represents the differential input impedance of the circuit. In order to simplify the balun design, let's assume that Zin is also resistive, equal to Rin.

Therefore, L1 = L2

C1 = C2

The mathematics associated with the circuit give the following results; the balun parameters, depending on the input / output resistances and frequency are :

$$L = \frac{\sqrt{Rin * Rout}}{\omega} \quad \text{and} \quad C = \frac{1}{\omega * \sqrt{Rin * Rout}}$$

To get more information on printed balun design, please refer to the "OM5045 Dect radio design" application note (see references).

5. TYPICAL APPLICATION CIRCUITS

5.1 Worked Examples

In this chapter, a design example, based around the UAA2077BM for DCS1800 applications is given. The circuit is typically connected as shown in Fig. 26. All values related to input / output impedances are mentioned in the product datasheet (dated from 9 Jan 96). The input impedance parameters are always specified in parallel configuration.

Multilayer ceramic capacitors with NPO dielectric have been used for general coupling/decoupling aspects :

– a value of 8.2 pF for decoupling 2 GHz frequencies (C1, C3, C17, C18, C19, C29 for AC–coupling; C6 to C9, C27, C30 for supply voltage decoupling).

– a value of 100 pF for decoupling 100–200 MHz frequencies (C11, C23 for AC–coupling; C5, C31 for supply voltage decoupling)

This choice results in a compromise between a high capacitive value needed for decoupling and the effect of parasitic inductance (self resonance frequency) appearing when dealing with high frequencies.

5.1.1 RF input

Rp, the real part of the parallel impedance is equal to 60 Ω

Cp, the imaginary part of the parallel impedance is equal to 1 pF

fi , the RF input frequency is equal to 1850 MHz

The balun component values are then calculated at 1850 MHz with Rin = 60 Ω and Rout = 50 Ω

L = 4.7 nH On the demo board, L6 = L1 = 5.6 nH

C = 1.6 pF On the demo board, C2 = C14 = 1.2 pF

The difference found between calculated and real values are due to PCB parasitic effects. An optimization has also been done in order to get a noise figure as small as possible.

Now, let's resonate Cp with an equal and opposite reactance at 1850 MHz :

LCpω2 = 1 hence L = 7.4 nH On the demoboard, L15= 6.8 nH.

5.1.2 TX Input

Rp, the real part of the parallel impedance is equal to 65 Ω

Cp, the imaginary part of the parallel impedance is equal to 1 pF

fi , the RF input frequency is equal to 1750 MHz

This yields to the following values :

L = 5.2 nH L7 = L8 = 4.7 nH

C = 1.6 pF C15 = C16 = 1.8 pF

5.1.3 IF Output

According to the pin function diagram, the IF output is of the open–collector type. It can also be deduced that the voltage output can not be greater than Vcc+3Vbe.

It is decided to proceed in 2 stages :

– a first matching from 1.2 kΩ to 50 Ω in single–ended mode that means on each IF output

– a second matching using a balun in order to provide from both IF ouputs, IFA and IFB (100 Ω differential) one terminal single ended output IFO at 50 Ω.

Matching

The need for a DC path between VCC and the output pin dictates the need for an inductor in the shunt leg of the matching network.

ZLRX, the typical application IF output load impedance is equal to 1kΩ in balanced configuration. CIF, the typical internal capacitance, measured on the demo board is equal to 4 pF.

The application is then for 1 kΩ load in differential mode i.e. 1 kΩ on each single–ended IF output.

For our application, CL is equal to 4 pF

RL is chosen equal to 1.2 kΩ

RS = 50 Ω

fIF = 188 MHz

Following the basic design procedure from paragraph 4.2 yields :

$$Q_1 = Q_2 = \sqrt{\frac{1200}{50} \pm 1} = 4.8$$

$X_1 = Q_1 * R_S = 50 * 4.8 = 240$

$X_2 = R_L / Q2 = 1200 / 4.8 = 250$

$X_1 = 1 / C\omega \Rightarrow C = 1 / X1\ \omega = 1 / (240 * 2\pi * 188.106) = 3.5$ pF

On the schematic, C22 = C24 = 3.9 pF

$X_2 = L\omega \Rightarrow L = X_2 / \omega = 250 / (2\pi * 188.106) = 212$ nH

The matching for the reactive part of the load, CL = 4 pF, leads to the following value for L' :

$L'C\omega 2 = 1 \Rightarrow L' = 1 / (4.10^{-12} * (2\pi * 188.10^6)2) = 1.79.10^{-7}$

The resultant inductance is :

$L // L' = 97 * 10^{-9} = 97$ nH

On the schematic, L11 = L12 = 100 nH

Balun

Rin = 100 Ω

Rout = 50 Ω

$L = \sqrt{100 * 50} / (2\pi * 188 * 10^6) = 59.8$ nF L13 = L14 = 56 nH

$C = 1 / (\sqrt{100 * 50} * 2\pi * 188.10^6) = 11.9$ pF C25 = C26 = 12 pF

6. MEASUREMENTS and RESULTS

6.1 Matching results

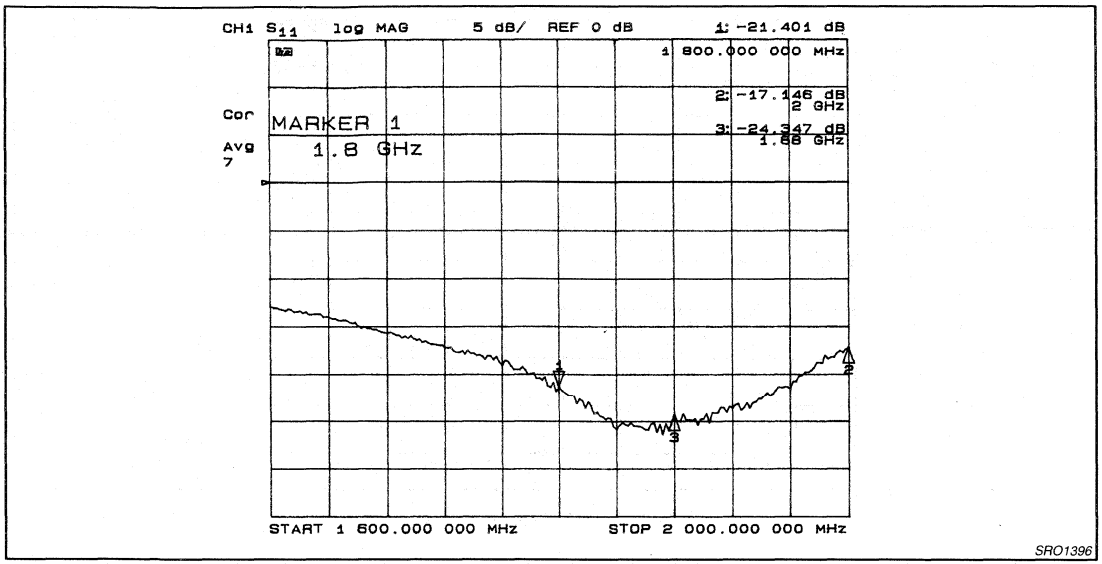


Figure 10. Matching at RF Input

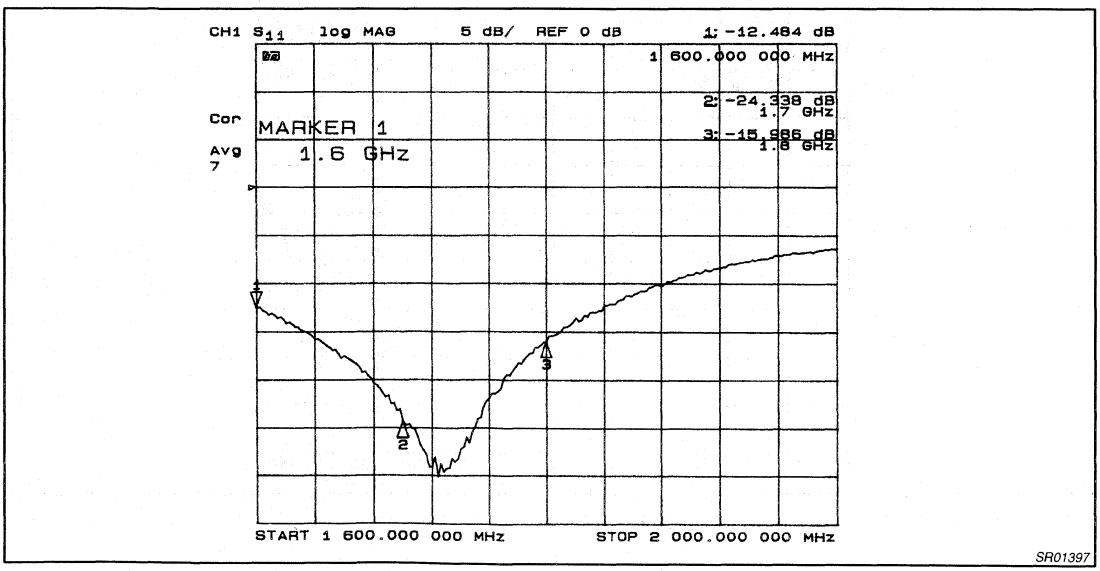


Figure 11. Matching at TX Input

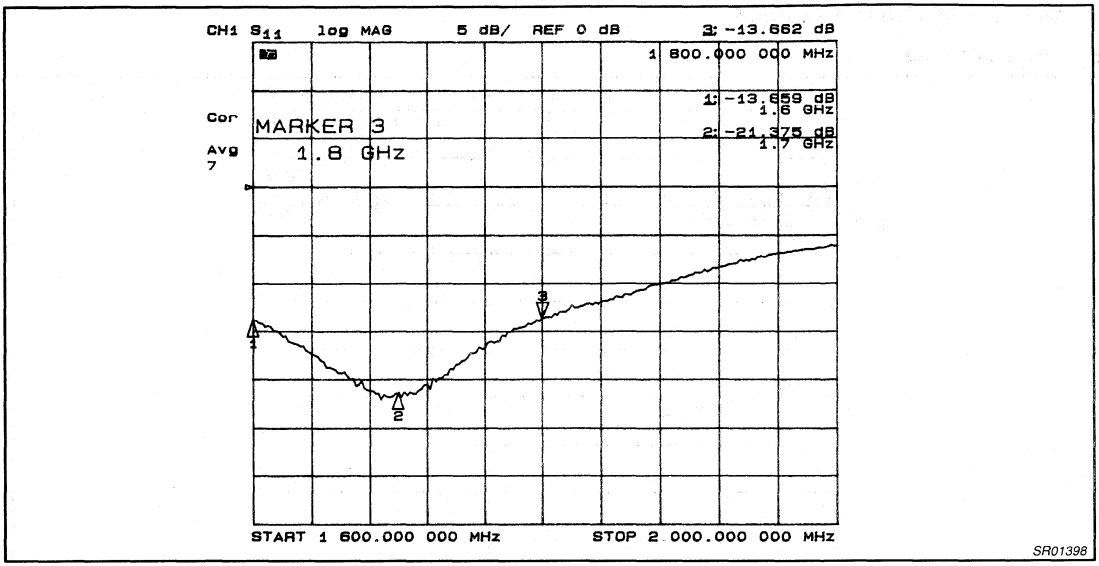


Figure 12. Matching at LO input

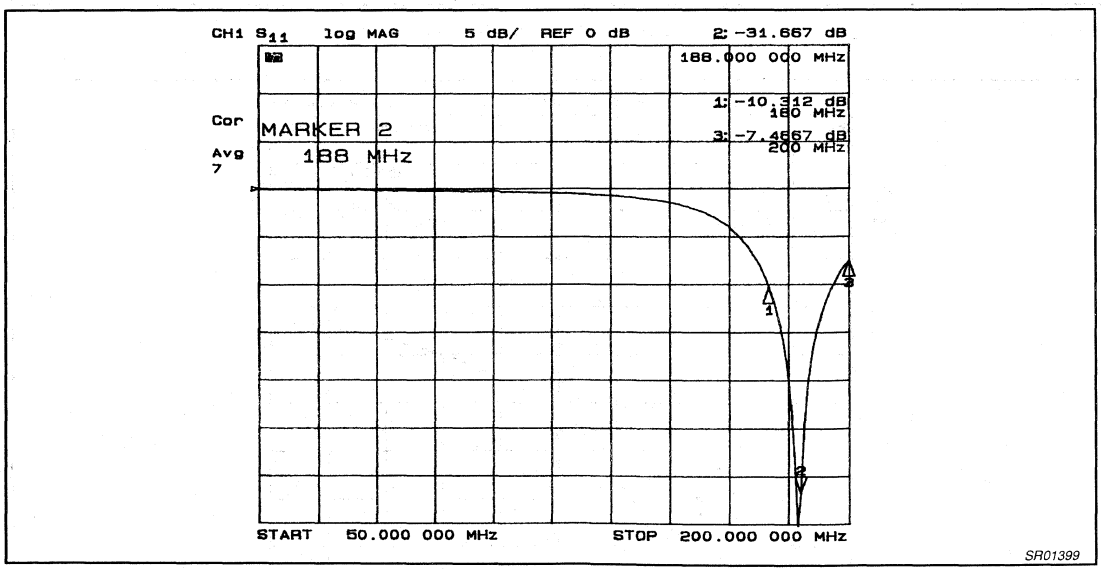


Figure 13. Matching at IF output

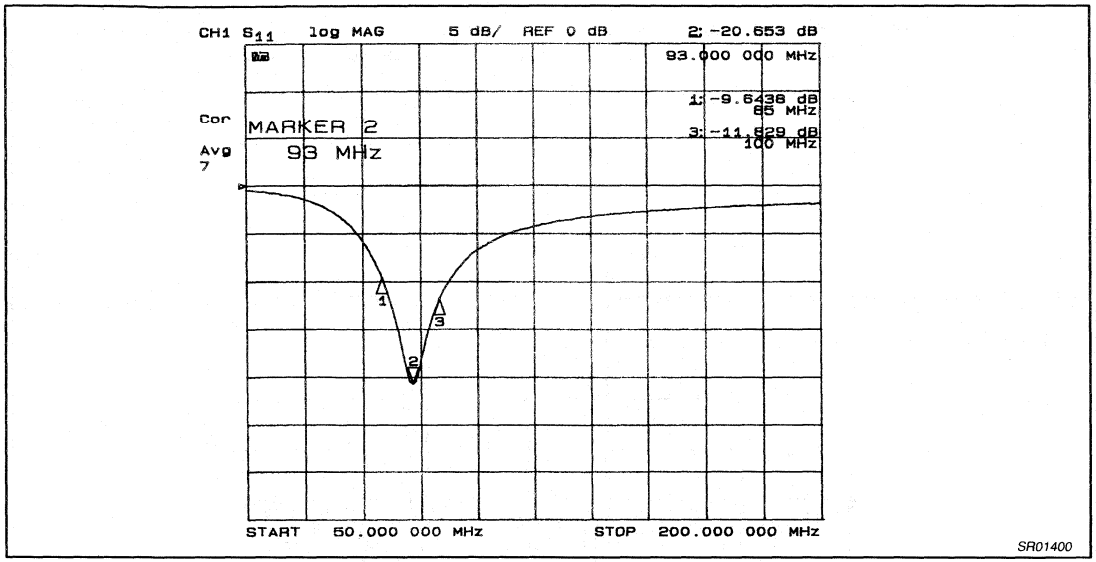


Figure 14. Matching at TX Output

6.2 Linearity / spurious response

In Fig. 15 is depicted the setup used for measuring the spurious response . Two separate measurements have been done :

– the RF frequency sweeps from RF – 4IF to RF + IF with a variable step of IF/(3*4*5) in order to reach the 2nd, 3rd, 4th and 5th harmonics.

– the RF frequency sweeps from IF to 22 IF with a fixed step equal to IF/5

In both cases, the LO frequency is fixed and the network analyzer always looks at a fixed IF frequency.

The results are shown on Fig. 16 and Fig. 17.

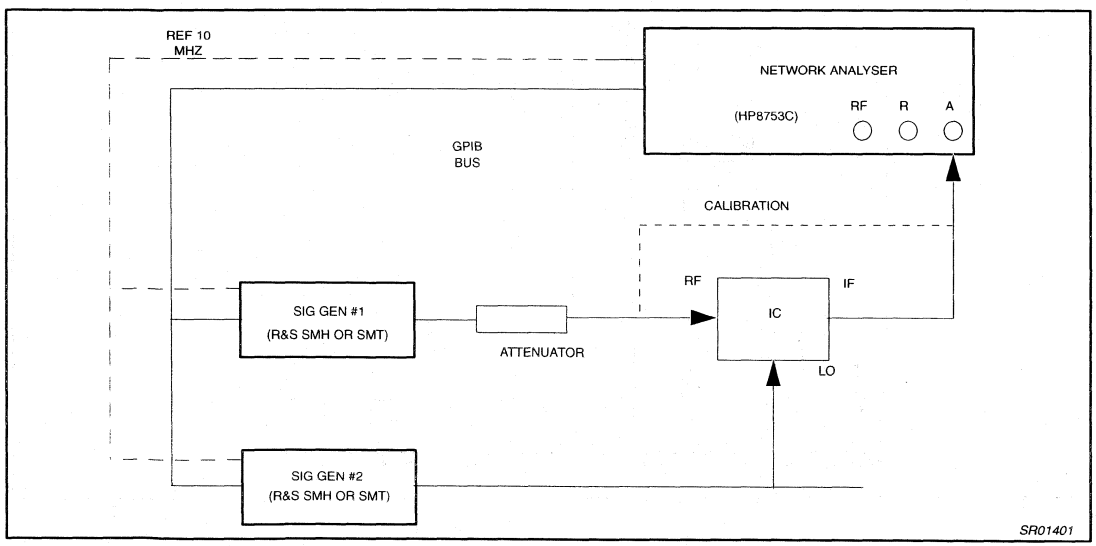


Figure 15. Spurious Response Measurement Setup

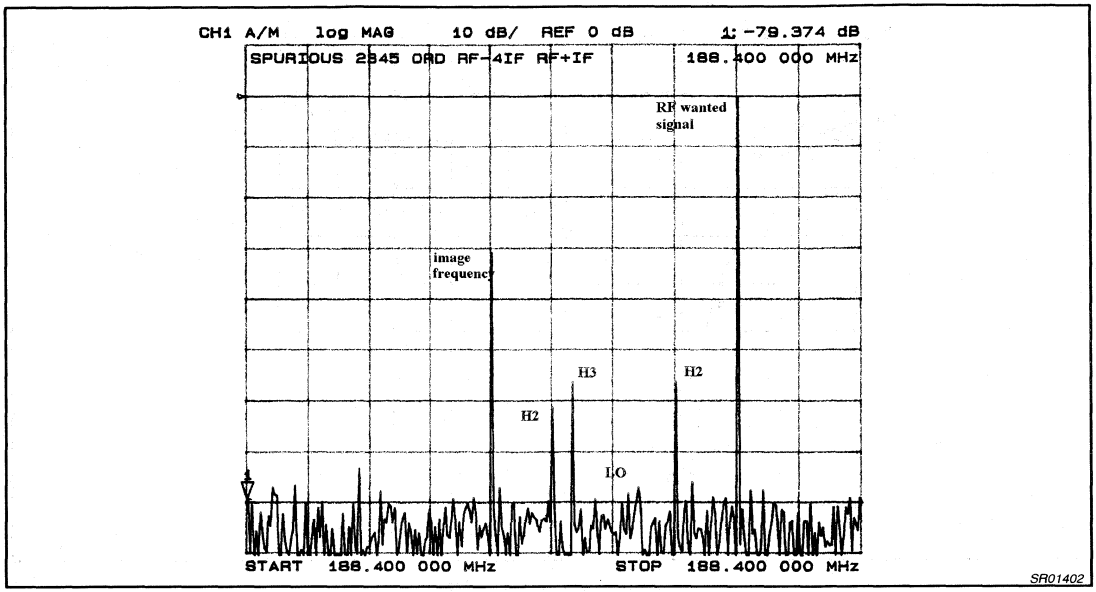


Figure 16. UAA2077BM Spurious Response

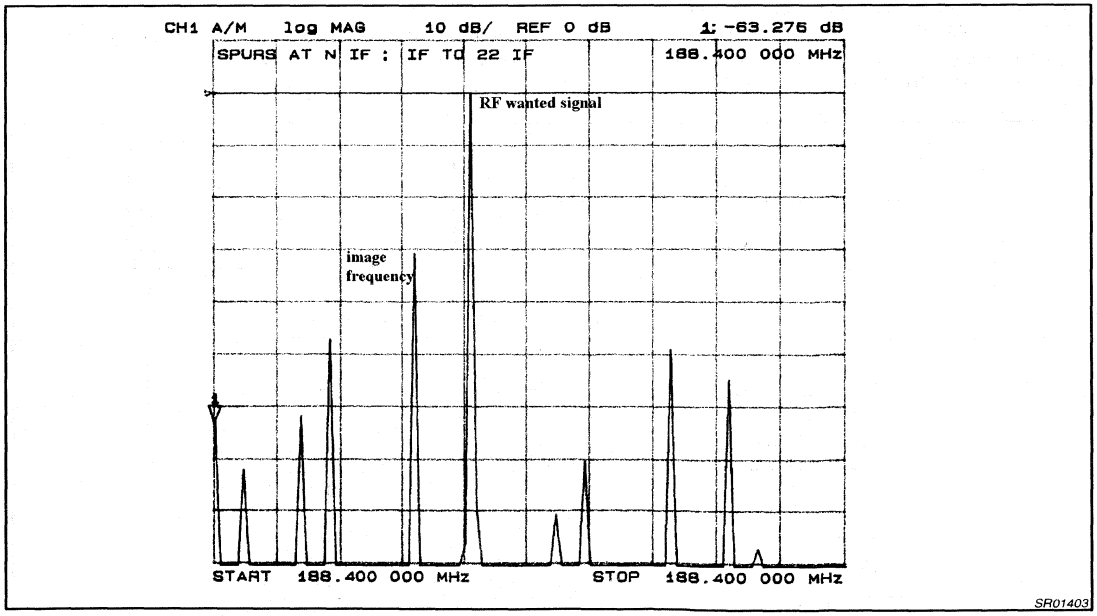


Figure 17. UAA2077BM Spurious Response

6.3 Image rejection

Image rejection measurements have been proceeded in varying 2 different parameters :

– the image rejection is given versus the IF frequency with a fixed LO . The RF signal is swept. The appropriate set–up is depicted on Fig. 18. Results are shown on Fig. 19 and 20.

– the image rejection is given versus the RF frequency with a fixed IF. Both RF and LO input signals are swept. The set–up, in that case, is identical to the one used for spurious response measurement (see Fig. 15). The results are shown on Fig. 21.

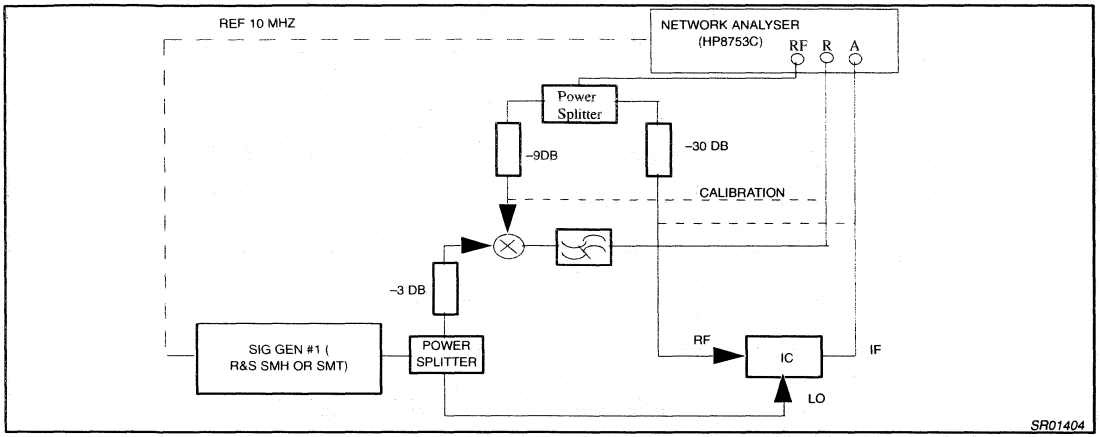


Figure 18. Image Rejection Measurement Setup With a Fixed LO Frequency

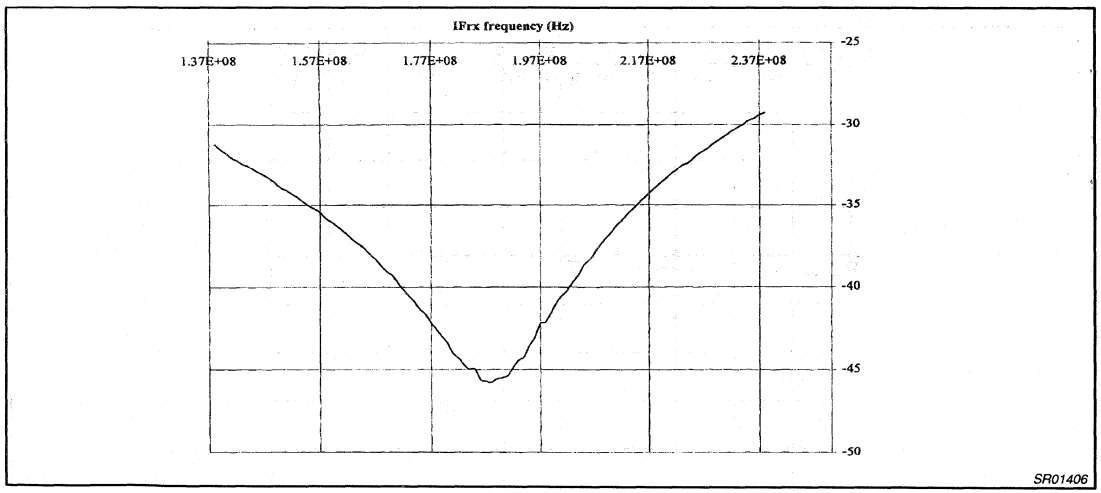


Figure 19. UAA2077CM Image Rejection Persus IF Frequency for fRF Wanted > fLO

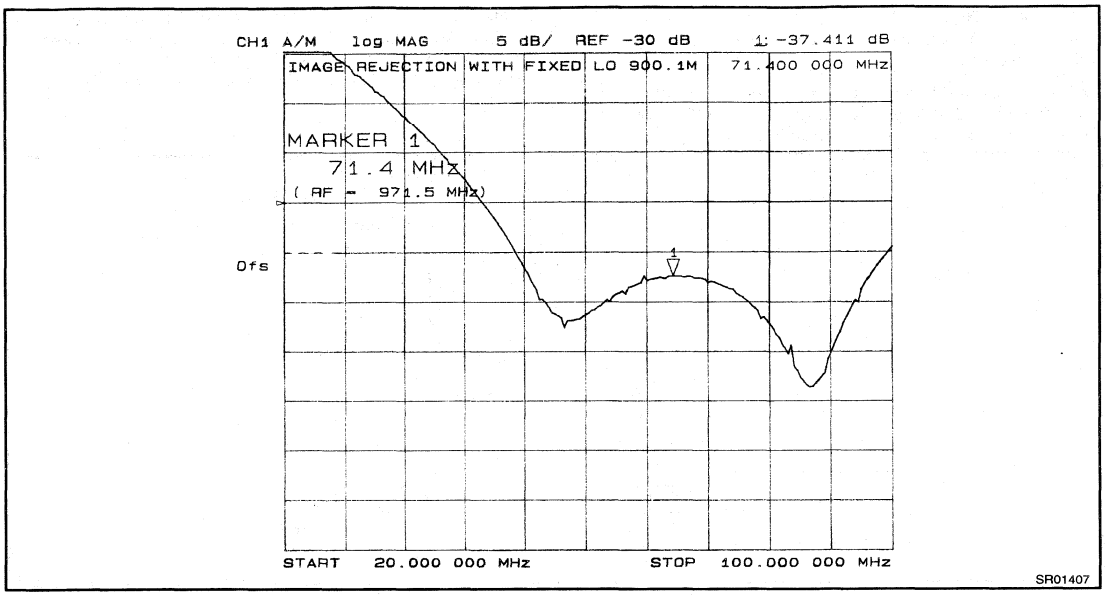


Figure 20. UAA2073M Image Rejection Versus IF Frequency

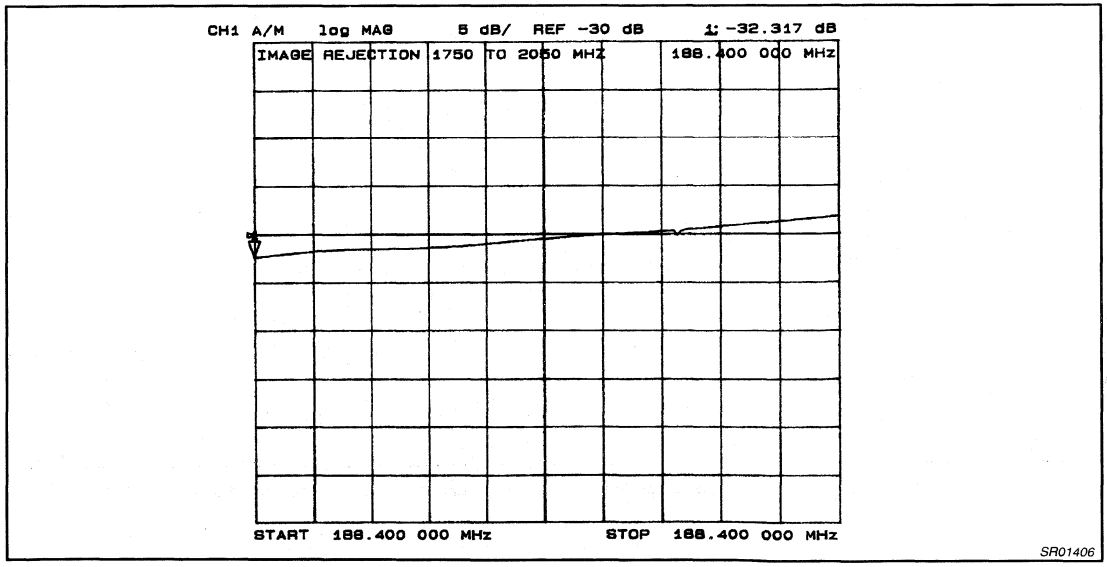


Figure 21. UAA2077BM Image Rejection Versus LO Frequency

6.4 Gain, Compression Point and IP3

The gain presented on Fig. 23 has been measured for a fixed IF frequency with a RF swept from 1.75 to 2.05 GHz. The set–up utilized in that case is the same as the one shown on Fig. 15.

The 1 dB compression point has been measured following the test set–up depicted on Fig. 20.

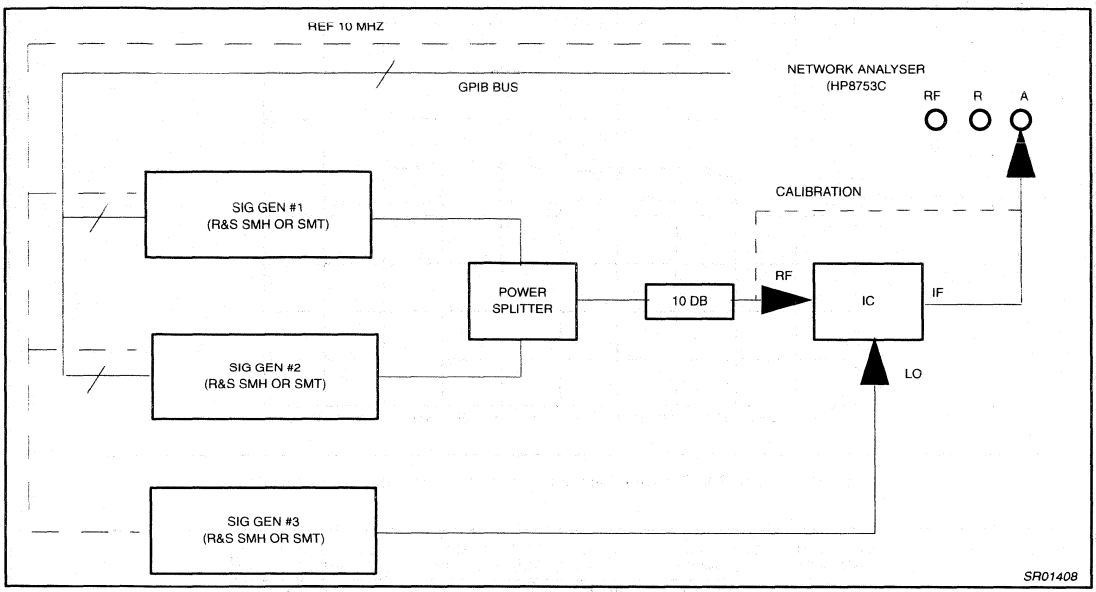


Figure 22. Third Order Intercept Point Set–Up

The set–up shown on the following figure enables a measurement of the 3rd order intercept point parameter.

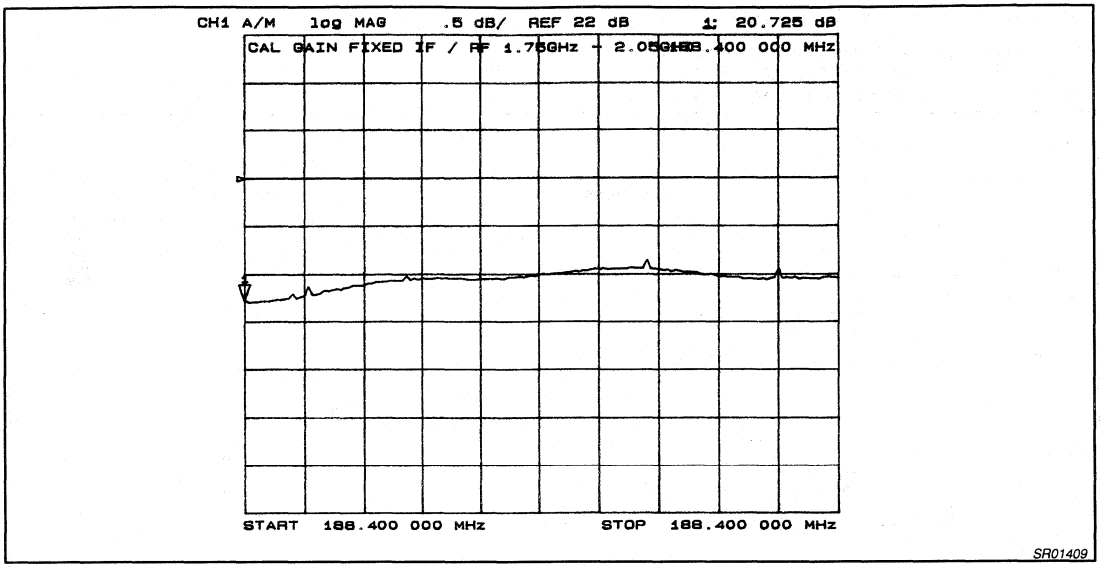


Figure 23. UAA2077BM Gain Versus Input Frequency (From 1.75 to 2.05 GHz)

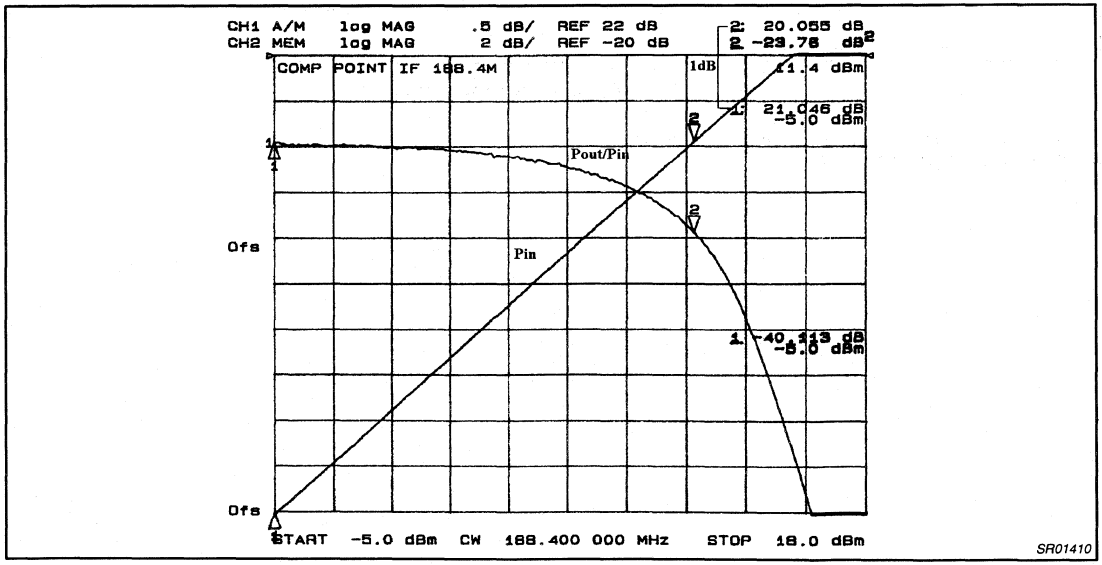


Figure 24. UAA2077BM 1 dB Compression Point

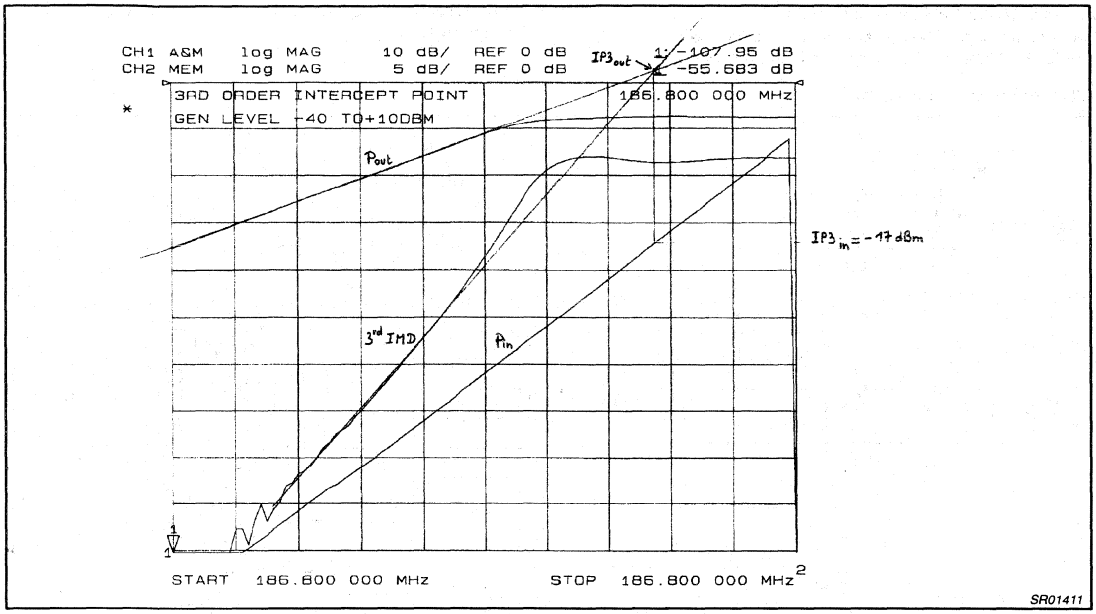


Figure 25. UAA2077BM 3rd order Intercept Point

7. DEMONSTRATION BOARD

Two different kinds of board have been designed, one related to the UAA2073XM ICs, the other one to the UAA2077XM ICs.The UAA2077BM and the UAA2073M have been taken as an example for both families.

7.1 Schematic Drawings

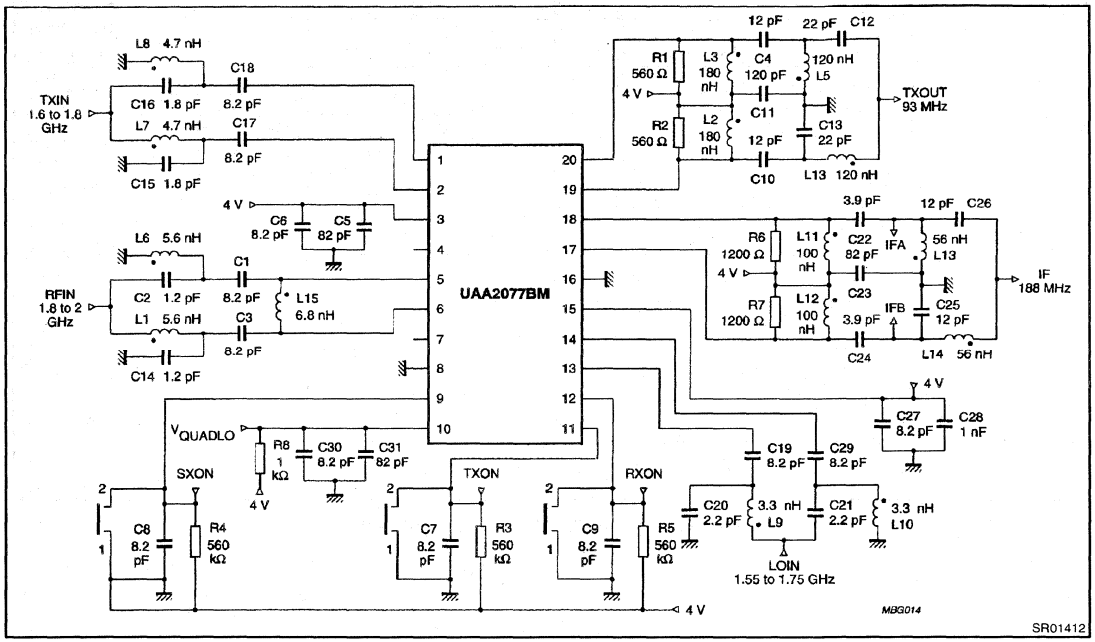


Figure 26. UAA2077BM Application Diagram

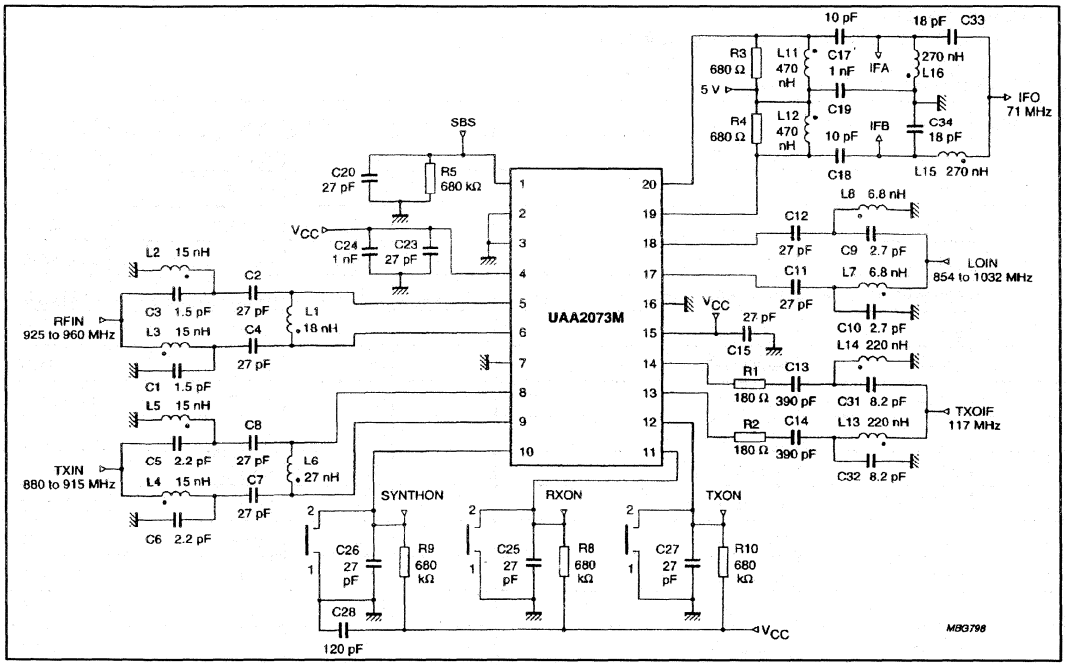


Figure 27. UAA2073M Application Diagram

7.2 Component lists

Component values for the UAA2077BM demoboard are indicated below.

Table 3 Demo Board Component List

Reference	Value	Type / Size		Reference	Value	Type / Size
L1	5.6 nH	0603 SMD		C13	22 pF	0805 SMD
L2	180 nH	0805 SMD		C14	1.2 pF	0603 SMD
L3	180 nH	0805 SMD		C15	1.8 pF	0603 SMD
L4	120 nH	0805 SMD		C16	1.8 pF	0603 SMD
L5	120 nH	0805 SMD		C17	8.2 pF	0603 SMD
L6	5.6 nH	0603 SMD		C18	8.2 pF	0603 SMD
L7	4.7 nH	0603 SMD		C19	8.2 pF	0603 SMD
L8	4.7 nH	0603 SMD		C20	2.2 pF	0603 SMD
L9	3.3 nH	0603 SMD		C21	2.2 pF	0603 SMD
L10	3.3 nH	0603 SMD		C22	3.9 pF	0805 SMD
L11	100 nH	0805 SMD		C23	82 pF	0805 SMD
L12	100 nH	0805 SMD		C24	3.9 pF	0805 SMD
L13	56 nH	0805 SMD		C25	12 pF	0805 SMD
L14	56 nH	0805 SMD		C26	12 pF	0805 SMD
L15	6.8 nH	0603 SMD		C27	8.2 pF	0805 SMD
C1	8.2 pF	0603 SMD		C28	1 nF	1206 SMD
C2	1.2 pF	0603 SMD		C29	8.2 pF	0603 SMD
C3	8.2 pF	0603 SMD		C30	8.2 pF	0805 SMD
C4	12 pF	0805 SMD		C31	82 pF	0805 SMD
C5	82 pF	0805 SMD		R1	560 Ω	0805 SMD
C6	8.2 pF	0805 SMD		R2	560 Ω	0805 SMD
C7	8.2 pF	0805 SMD		R3	560 k Ω	0805 SMD
C8	8.2 pF	0805 SMD		R4	560 k Ω	0805 SMD
C9	8.2 pF	0805 SMD		R5	560 k Ω	0805 SMD
C10	12 pF	0805 SMD		R6	1.2 k Ω	0805 SMD
C11	120 pF	0805 SMD		R7	1.2 k Ω	0805 SMD
C12	22 pF	0805 SMD		R8	1 k Ω	0805 SMD

Component values for the UAA2073M demoboard are indicated below.

Table 4 Demo Board Component List

Reference	Value	Type / Size		Reference	Value	Type / Size
R1	180 Ω	0805 SMD		C20	27 pF	0805 SMD
R2	180 Ω	0805 SMD		C23	27 pF	0805 SMD
R3	680 Ω	0805 SMD		C24	1 nF	0805 SMD
R4	680 Ω	0805 SMD		C25	27 pF	0805 SMD
R5	680 kΩ	0805 SMD		C26	27 pF	0805 SMD
R8	680 kΩ	0805 SMD		C27	27 pF	0805 SMD
R9	680 kΩ	0805 SMD		C28	120 pF	0805 SMD
R10	680 kΩ	0805 SMD		C31	8.2 pF	0805 SMD
C1	1.5 pF	0805 SMD		C32	8.2 pF	0805 SMD
C2	27 pF	0805 SMD		C33	18 pF	0805 SMD
C3	1.5 pF	0805 SMD		C34	18 pF	0805 SMD
C4	27 pF	0805 SMD		L1	18 nH	0805 SMD
C5	2.2 pF	0805 SMD		L2	15 nH	0805 SMD
C6	2.2 pF	0805 SMD		L3	15 nH	0805 SMD
C7	27 pF	0805 SMD		L4	15 nH	0805 SMD
C8	27 pF	0805 SMD		L5	15 nH	0805 SMD
C9	2.7 pF	0805 SMD		L6	27 nH	0805 SMD
C10	2.7 pF	0805 SMD		L7	6.8 nH	0805 SMD
C11	27 pF	0805 SMD		L8	6.8 nH	0805 SMD
C12	27 pF	0805 SMD		L11	470 nH	1008 SMD
C13	390 pF	0805 SMD		L12	470 nH	1008 SMD
C14	390 pF	0805 SMD		L13	220 nH	0805 SMD
C15	27 pF	0805 SMD		L14	220 nH	0805 SMD
C17	10 pF	0805 SMD		L15	270 nH	1008 SMD
C18	10 pF	0805 SMD		L16	270 nH	1008 SMD
C19	1 nF	0805 SMD				

7.3 Layout and Assembly Drawings

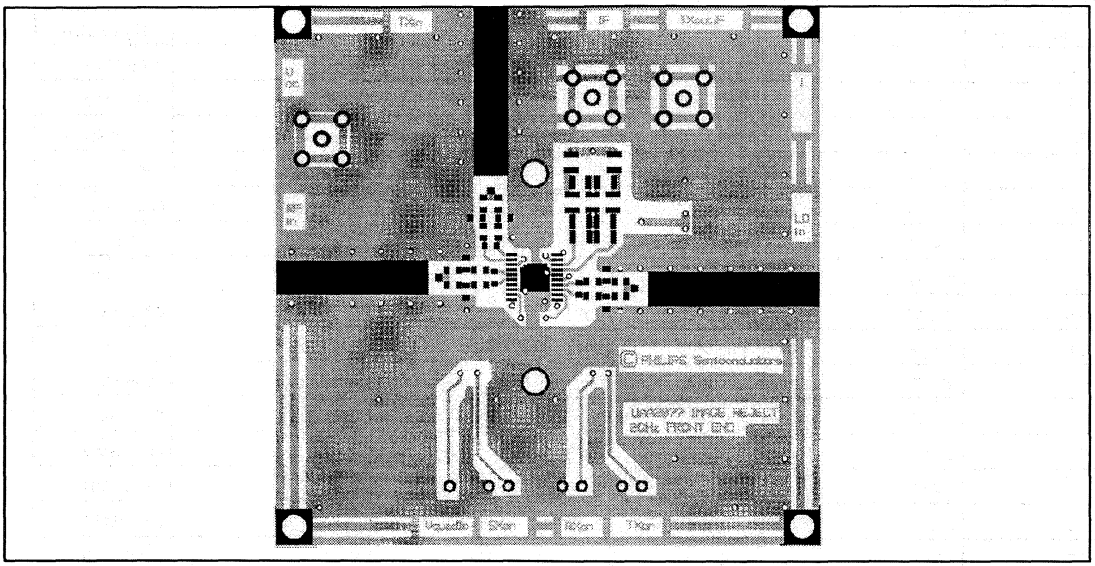


Figure 28. UAA2077XM Demo Board – Layer 1

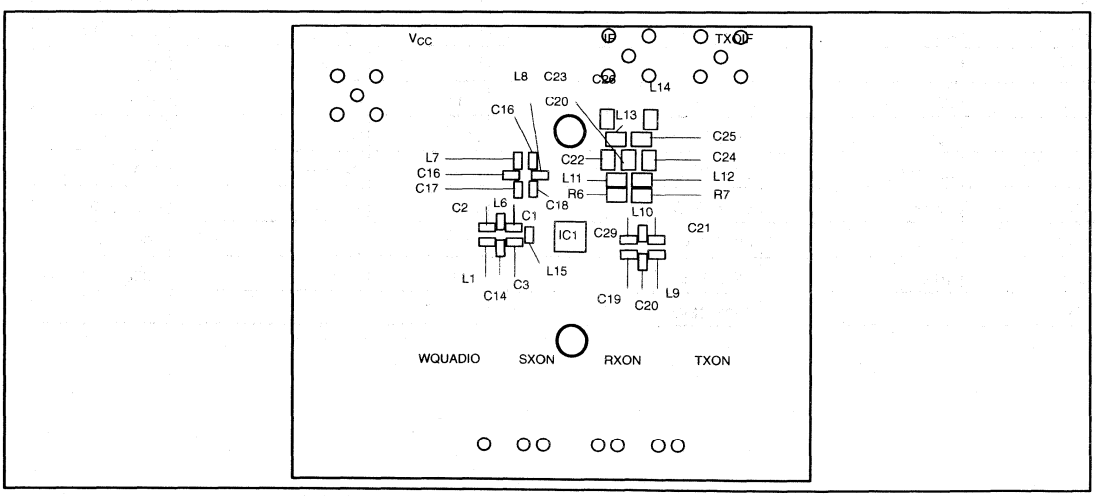


Figure 29. UAA2077XM Demo board – Layer 1 Assembly

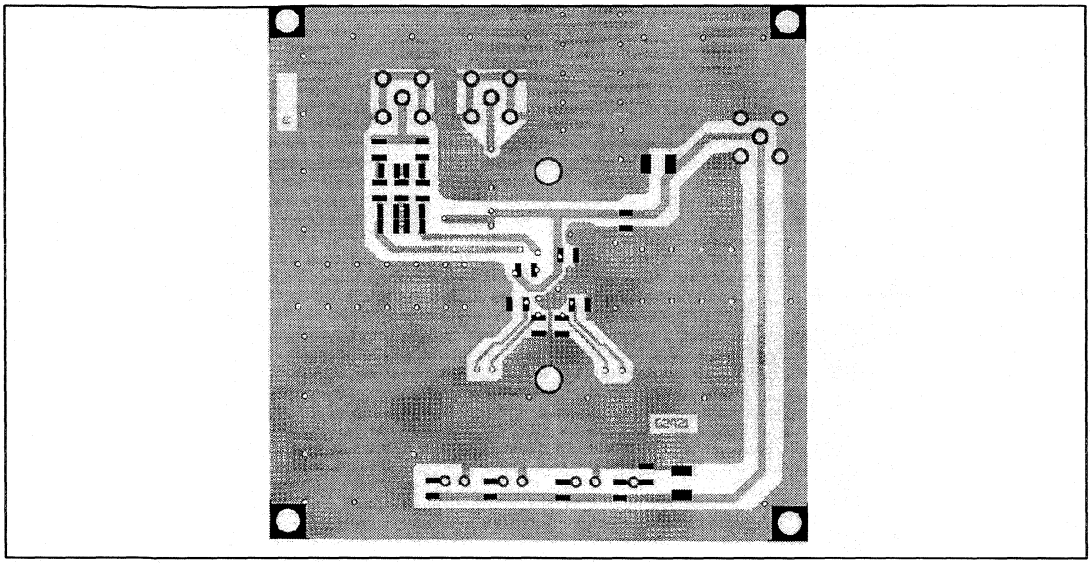


Figure 30. UAA2077XM Demo Board – Layer 2 Layout

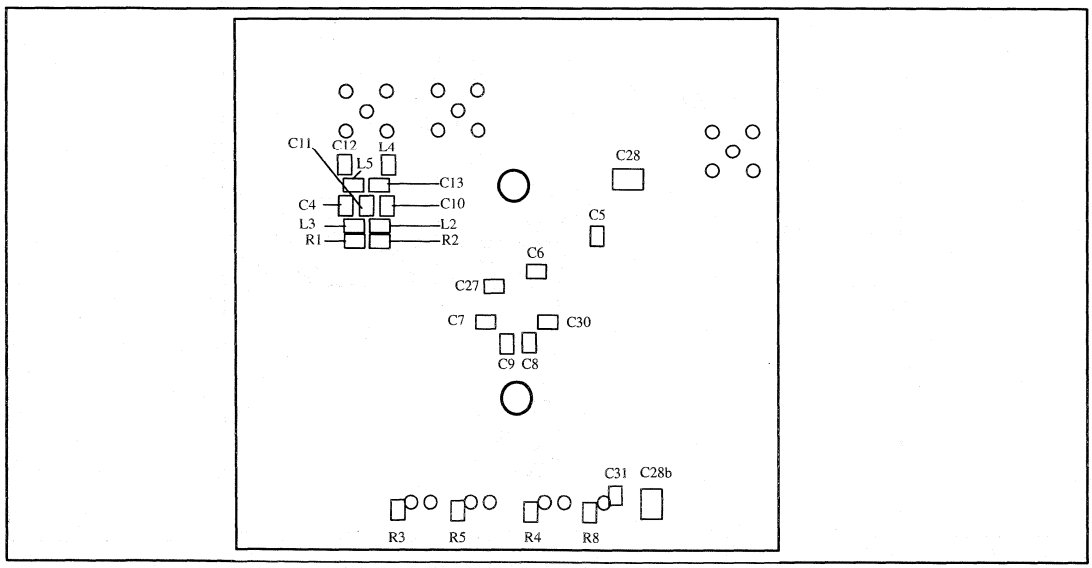


Figure 31. UAA2077XM Demo Board – Layer 2 Assembly

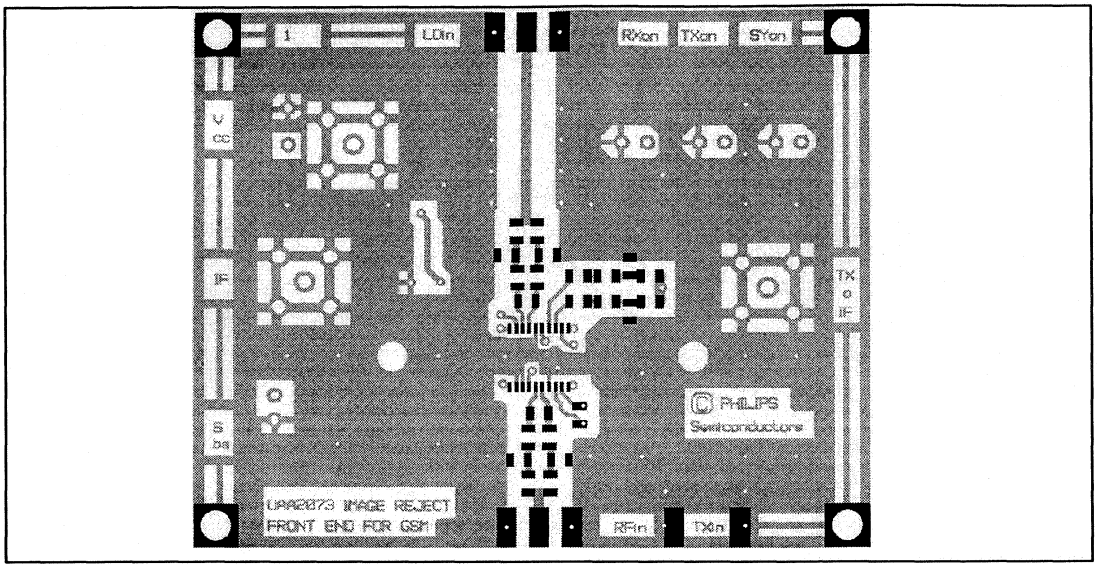


Figure 32. UAA2073XM Demo Board – Layer 1 Layout

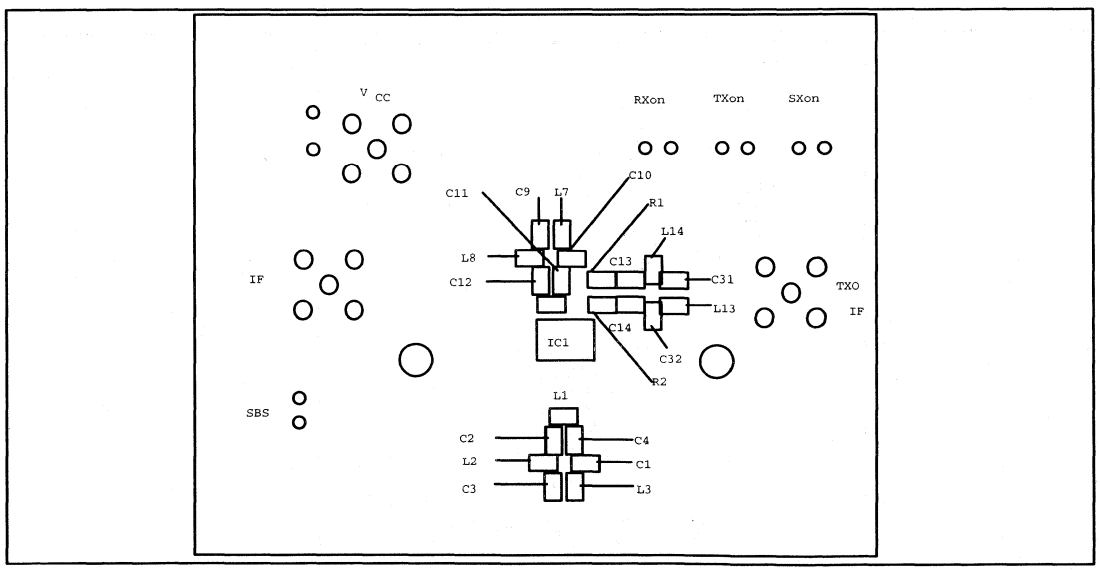


Figure 33. UAA2073XM Demo board – Layer 1 Assembly

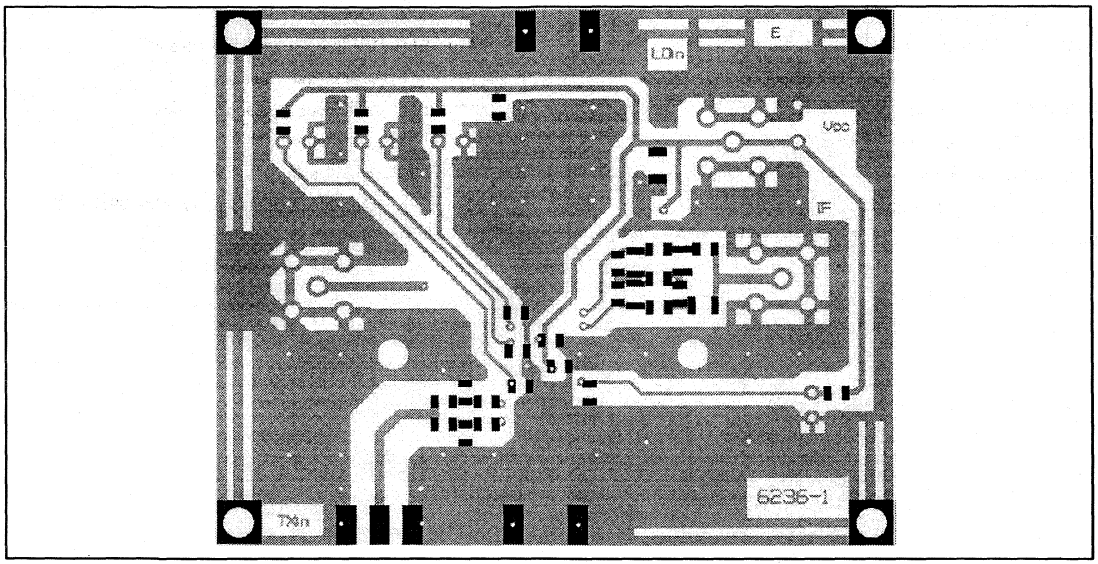


Figure 34. UAA2073XM Demo Board – Layer 2 Layout

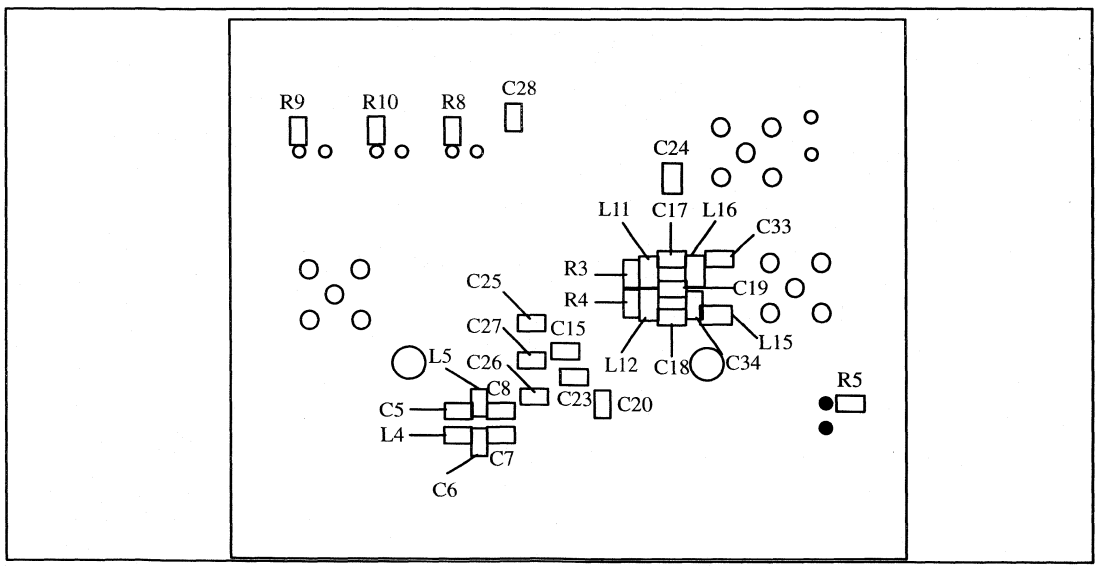


Figure 35. UAA2073XM Demo Board – Layer 2 Assembly

8. REFERENCES

[1] UAA2072M Image rejecting front–end for GSM applications
Datasheet – November 94

[2] UAA2073M Image rejecting front–end for GSM applications
Datasheet – 07 December 95

[3] UAA2073AM Image rejecting front–end for GSM applications
Datasheet

[4] UAA2077AM Image rejecting front–end for DECT applications
Datasheet –04 July 96

[5] UAA2077BM 2 GHz Image rejecting front–end
Datasheet – 09 January 96

[6] UAA2077CM 2 GHz Image rejecting front–end
Datasheet

[7] OM5045 DECT Radio Design
Application note (report n°AN95096) – 31 October 1995

Image rejecting front-end for DECT applications UAA2077AM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 30 dB on-chip image rejection
- IF I/Q combiner at 110 MHz
- On-chip quadrature network
- RX fast on/off power-down mode
- Shrink small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 1800 MHz front-end for DECT hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2077AM contains a high frequency low noise receiver front-end intended to be used in DECT mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077AM is its ability to provide over 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne (LO < RF) or supradyne (LO > RF) reception.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers.The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers. All RF and IF inputs or outputs are balanced.

Two pins RXON and SXON are used to control the different power-down modes. A special mode of operation called synthesizer-ON mode, controlled by pin SXON can be used to minimize the LO pulling when the receiver is turned on. When SXON is HIGH, all internal buffers on the LO path are turned on. Pin SBS allows a selection of whether to reject the upper or lower image frequency. When SBS is HIGH, supradyne reception is activated. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	T_{amb} = 0 to 70 °C	3.15	4.0	5.3	V
			3.6	4.0	5.3	V
I_{CCRX}	receive supply current		22	27	33	mA
I_{CCPD}	supply current in power-down		–	–	50	µA
T_{amb}	operating ambient temperature		–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2077AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

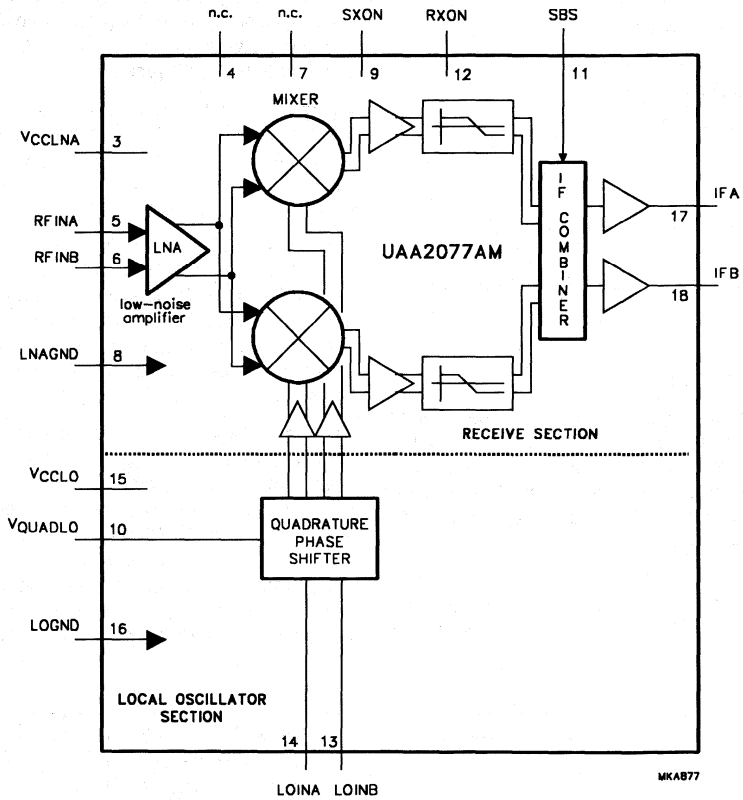


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
V_{CCLNA}	3	supply voltage for LNA and IF parts
n.c.	4	not connected
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
n.c.	7	not connected
LNAGND	8	ground for LNA and IF parts
SXON	9	synthesizer-ON mode enable
V_{QUADLO}	10	input voltage for LO quadrature trimming
SBS	11	sideband selection input
RXON	12	receive mode enable
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
n.c.	19	not connected
n.c.	20	not connected

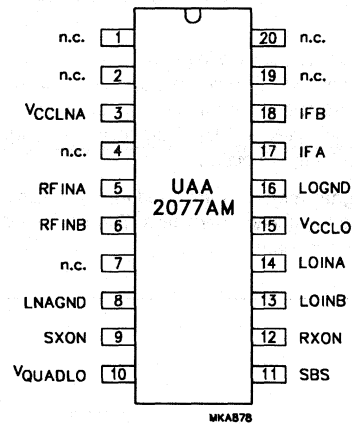


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 35 Ω (real part).

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; i.e. a 1 kΩ resistor load at each IF output, plus a 2 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, on/off, of the receive section is controlled by the hardware input RXON.

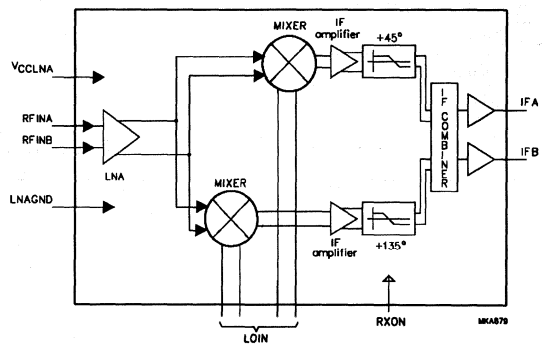


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by the voltage on pin V_{QUADLO}. This voltage trims the all-pass network to the selected LO frequency range. This should be achieved by connecting a resistor between V_{QUADLO} and V_{CC}. Optimization of image rejection can be obtained by trimming at this point.

The LO differential input impedance is 35 Ω (real part). A synthesizer-ON mode is used to power-up the LO input buffers, thus minimizing the pulling effect on the external VCO when entering receive mode. This mode is active when SXON = 1.

There are no internal biassing components attached to the pins LOINA and LOINB. These pins are connected by capacitors to the internal phase shifting network.

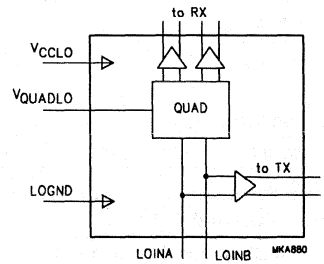


Fig.4 Block diagram, LO section.

Table 1 Control of power status

EXTERNAL PIN LEVEL		CIRCUIT MODE OF OPERATION
RXON	SXON	
LOW	LOW	power-down mode
HIGH	X	receive mode
LOW	HIGH	synthesizer-ON mode (only LO buffers enabled)

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{I(max)}$	maximum power input	–	20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
P_{max}	maximum power dissipation	–	250	mW
T_{stg}	storage temperature	−65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C Class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CCLNA} and V_{CCLO}						
V_{CC}	supply voltage	over full temperature range	3.6	4.0	5.3	V
		T_{amb} between 0 and 70 °C	3.15	4.0	5.3	V
I_{CCRX}	receive supply current	receive mode active; DC tested	22	27	33	mA
I_{CCPD}	supply current in power-down	DC tested	–	–	50	μA
I_{CCSX}	supply current	synthesizer-ON mode only	3	5	7	mA
Pins: RXON, SXON and SBS						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		0.7V_{CC}	–	V_{CC}	V
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} − 0.4 V	−1	–	+1	μA
I_{IL}	LOW level static input current	pin at 0.4 V	−1	–	+1	μA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	–	2.0	–	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	–	2.5	–	mA

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RF}	RF input impedance (real part)	balanced; at 1890 MHz	–	35	–	Ω
f_{RF}	RF input frequency		1880	–	1900	MHz
RL_{RF}	return loss on matched RF input	balanced; note 1	11	15	–	dB
G_{CP}	conversion power gain	differential RF inputs to differential IF outputs loaded to 1 kΩ differential	17	20	23	dB
G_{ripple}	gain ripple as a function of RF frequency	note 2	–	0.1	–	dB
ΔG/T	gain variation with temperature	note 2	−15	−10	−5	mdB/K
$CP1_{RX}$	1 dB compression point	differential RF inputs to differential IF outputs; note 1	−26	−23	–	dBm

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DES3	3 dB desensitization point	interference frequency offset 3 MHz; differential RF inputs to differential IF outputs; note 1	–	–30	–	dBm
		interference frequency offset 20 MHz; differential RF inputs to differential IF outputs; note 1	–	–27	–	dBm
$IP2D_{RX}$	2nd order intercept point	differential RF inputs to differential IF outputs; note 2	15	22	–	dBm
$IP3_{RX}$	3rd order intercept point	differential RF inputs to differential IF outputs; note 2	–23	–17	–	dBm
NF_{RX}	overall noise figure	differential RF inputs to differential IF outputs; notes 2 and 3	–	4.3	5.0	dB
$Z_{L(IF)}$	typical application IF output load impedance	balanced	–	1	–	kΩ
RL_{IF}	return loss on matched IF output	balanced; note 1	11	15	–	dB
f_{IF}	IF frequency range	RF < LO	–	110	–	MHz
IR	rejection of image frequency	V_{QUADLO} tuned	30	–	–	dB
		infradyne; f_{IF} = 110 MHz; note 4	–	tbf	–	dB
Local oscillator section (receive section enabled)						
f_{LO}	LO input frequency		1770	–	2010	MHz
Z_{LO}	LO input impedance (real part)	balanced	–	35	–	Ω
RL_{LO}	return loss on matched LO input (including standby mode)	note 1	9	12	–	dB
ΔRL_{LO}	return loss variation ratio between SXON and RXON modes	linear S_{11} variation	tbf	tbf	tbf	–
$P_{I(LO)}$	LO input power level		–6	–3	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 2	40	–	–	dB
R_{tune}	image rejection tuning resistor	connected between V_{QUADLO} and V_{CC}	0	1	–	kΩ
Timing						
t_{start}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2077AM demonstration board at T_{amb} = 25 °C.
2. Measured and guaranteed only on UAA2077AM demonstration board.
3. This value includes printed-circuit board and balun losses.
4. V_{QUADLO} open-circuit.

APPLICATION INFORMATION

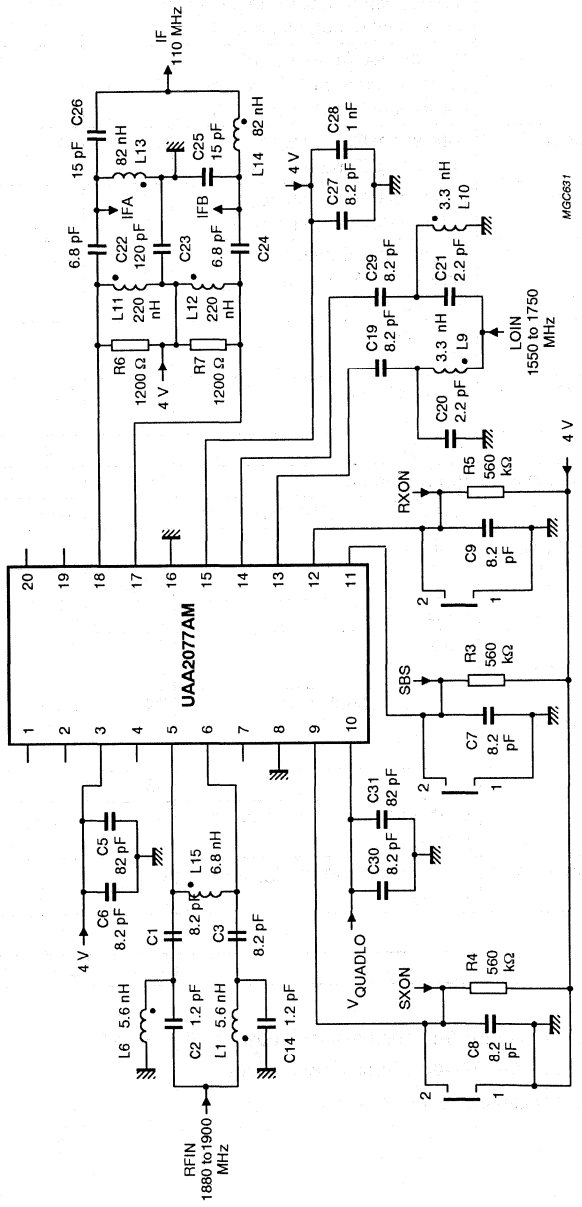


Figure 5 illustrates the electrical diagram of the UAA2077AM Philips demonstration board for DECT applications. All matching is to 50 Ω for measurement purposes. Different values will be used in a real application.

Fig.5 Application diagram.

2GHz image rejecting front-end UAA2077BM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 25 dB on-chip image rejection
- IF I/Q combiner at 188 MHz
- On-chip quadrature network
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 1800 MHz front-end for DCS1800 hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers e.g. PCS, RF-LANS.

GENERAL DESCRIPTION

UAA2077BM contains both a receiver front-end and a high frequency transmit mixer intended to be used in mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077BM is its ability to provide over 25 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne (LO < RF) or supradyne (LO > RF) reception.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers.The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a low-noise amplifier, and a down-conversion mixer. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced.

Pins RXON, TXON and SXON allow a selection of whether to reject the upper or lower image frequency and control of the different power-down modes. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	4.0	5.3	V
I_{CCRX}	receive supply current	22	27	33	mA
I_{CCTX}	transmit supply current	11	14	17	mA
I_{CCPD}	supply current in power-down	–	–	50	μA
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2077BM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

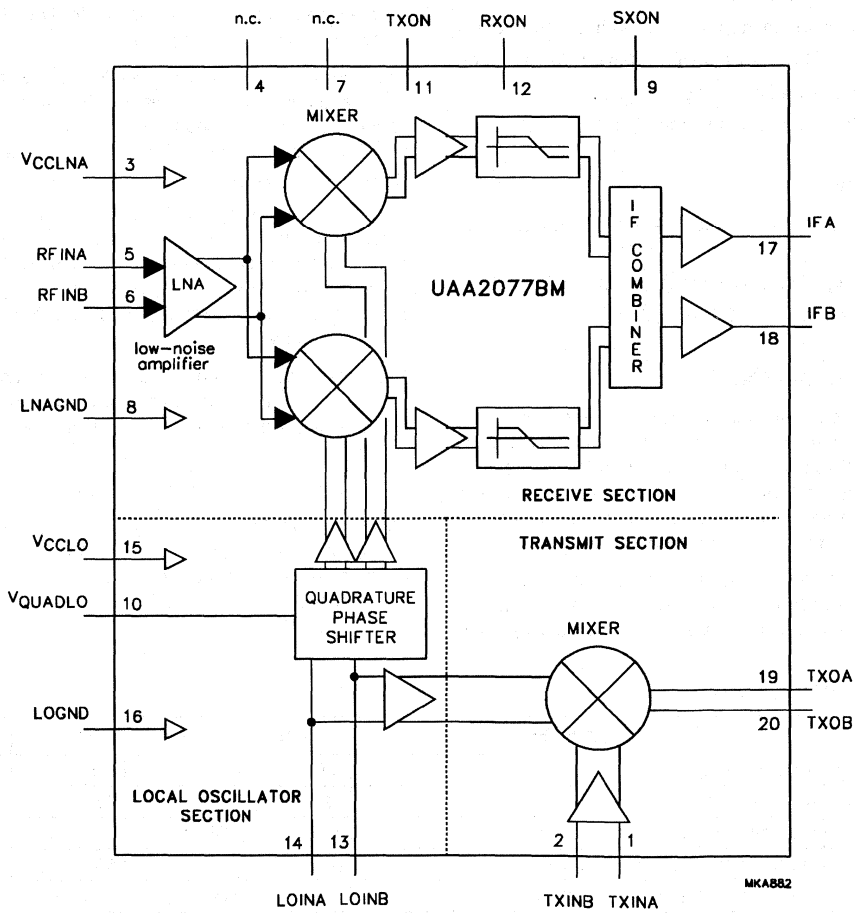


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXINA	1	transmit mixer input A (balanced)
TXINB	2	transmit mixer input B (balanced)
V_{CCLNA}	3	supply voltage for LNA, IF parts and TX mixer
n.c.	4	not connected
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
n.c.	7	not connected
LNAGND	8	ground for LNA and IF parts
SXON	9	synthesizer-ON mode enable
V_{QUADLO}	10	input voltage for LO quadrature trimming
TXON	11	transmit mode enable
RXON	12	receive mode enable
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
TXOA	19	transmit mixer IF output A (balanced)
TXOB	20	transmit mixer IF output B (balanced)

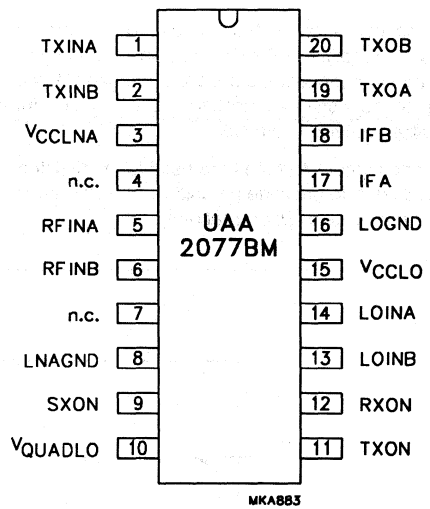


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF differential input impedance is 35 Ω (real part).

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; i.e. a 1 kΩ resistor load at each IF output, plus a 2 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

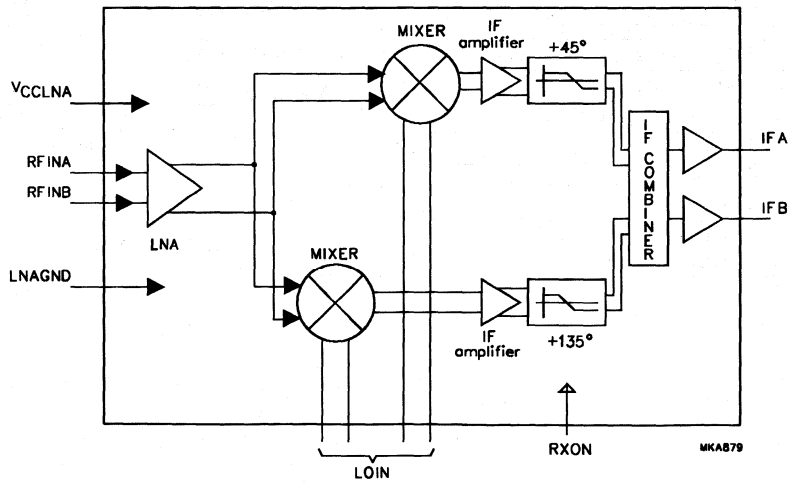


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by the voltage on pin V_{QUADLO}. This should be done by connecting a resistor between V_{QUADLO} and V_{CC}. Over 25 dB of image rejection can be obtained by an optimum resistor value.

The LO differential input impedance is 35 Ω (real part). A synthesizer-ON mode is used to power-up all LO input buffers, thus minimizing the pulling effect on the external VCO when entering receive or transmit mode. This mode is active when SXON = 1.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF which is down-converted to a modulated transmit IF frequency, phase locked with the baseband modulation.

The transmit mixer provides a differential input at 40 Ω and a differential HIGH impedance output. The IF outputs are HIGH impedance (open-collector type); i.e. a 500 Ω resistor load at each IF output, plus a 1 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The mixer can also be used for frequency up-conversion.

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON.

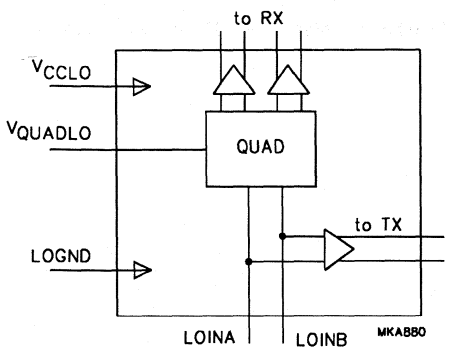


Fig.4 Block diagram, LO section.

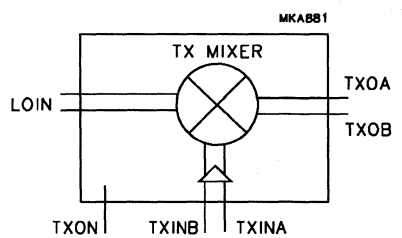


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SXON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	receive section on, infradyne reception
HIGH	LOW	LOW	transmit section on
LOW	LOW	HIGH	synthesizer-ON mode (only LO buffers enabled)
LOW	HIGH	HIGH	receive section on and synthesizer-ON mode active, infradyne reception
HIGH	LOW	HIGH	transmit section on and synthesizer-ON mode active
HIGH	HIGH	LOW	receive section on, supradyne reception
HIGH	HIGH	HIGH	receive section on and synthesizer-ON mode active, supradyne reception

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	−65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands 1500 V ESD Human Model and 200 V Machine Model; refer to MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 4 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CCLNA}, V_{CCLO}						
V_{CC}	supply voltage	over full temperature range	3.6	4.0	5.3	V
$I_{CC(RX)}$	supply current	receive mode active; DC tested	22	27	33	mA
$I_{CC(TX)}$	supply current	transmit mode active; DC tested	11	14	17	mA
$I_{CC(PD)}$	supply current in power-down mode	DC tested	–	–	50	µA
$I_{CC(SX)}$	supply current	synthesizer-ON mode only	6	7.5	9	mA
$I_{CC(SRX)}$	supply current	receive and synthesizer-ON mode active	–	29	–	mA
$I_{CC(STX)}$	supply current	transmit and synthesizer-ON mode active	–	18	–	mA
Pins: RXON, TXON and SXON						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
I_{IH}	HIGH level static input current	pins at V_{CC} − 0.4 V	−1	–	+1	µA
I_{IL}	LOW level static input current	pins at 0.4 V	−1	–	+1	µA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	–	2.0	–	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	–	2.5	–	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	–	2.0	–	V
Pins: TXOA and TXOB						
I_O	DC output current	transmit section enabled	–	0.9	–	mA
Pins: LOINA and LOINB						
V_{LOIN}	DC input voltage level	RXON, TXON or SXON HIGH	–	3.3	–	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RFI}	RF input impedance (real part)	balanced; at 1850 MHz	–	35	–	Ω
f_{RFI}	RF input frequency		1800	–	2000	MHz
RL_{RF}	return loss on matched RF input	balanced; note 1	11	15	–	dB
G_{CP}	conversion power gain	differential RF inputs to differential IF outputs loaded to 1 kΩ differential	17	20	23	dB
G_{rip}	gain ripple as a function of RF frequency	between 1805 and 1880 MHz; note 2	–	0.1	–	dB
ΔG/T	gain variation with temperature	note 2	−15	−10	−5	mdB/K
$CP1_{RX}$	1 dB compression point	differential RF inputs to differential IF outputs; note 1	−26	−23	–	dBm
DES3	3 dB desensitisation point	interferer frequency offset: 3 MHz; differential RF inputs to differential IF outputs; note 1	–	−30	–	dBm
		interferer frequency offset: 20 MHz; differential RF inputs to differential IF outputs; note 1	–	−27	–	dBm
$IP2D_{RX}$	2nd order intercept point	differential RF inputs to differential IF outputs; note 2	+15	+22	–	dBm
$IP3_{RX}$	3rd order intercept point	differential RF inputs to differential IF outputs; note 2	−23	−17	–	dBm
NF_{RX}	overall noise figure	differential RF inputs to differential IF outputs; notes 2 and 3	–	4.3	5.0	dB
$Z_{L(IF)}$	typical application IF output load impedance	balanced	–	1	–	kΩ
RL_{IF}	return loss on matched IF input	balanced; note 1	11	15	–	dB
f_{IF}	IF frequency range		170	188	210	MHz
IR	rejection of image frequency	V_{QUADLO} tuned	20	–	–	dB
		infradyne; f_{IF} = 188 MHz; note 4	25	32	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Local oscillator section (receive section enabled)						
f_{LO}	LO input frequency		1600	–	2200	MHz
Z_{LO}	LO input impedance (real part)	balanced	–	35	–	Ω
RL_{LO}	return loss on matched input (including standby mode)	note 1	9	12	–	dB
ΔRL_{LO}	return loss variation between SX, SRX and STX modes	linear S_{11} variation; note 1	–		–	mU
$P_{i(LO)}$	LO input power level		–6	–3	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB
R_{tune}	image rejection tuning resistor	connected between V_{QUADLO} and V_{CC}	0	1000	–	Ω
Transmit section (transmit section enabled)						
Z_L	TX IF typical load impedance		–	500	–	Ω
RL_{TXIF}	return loss on matched transmitter IF input		11	15	–	dB
$Z_{i(RF)}$	TX RF input impedance (real part)	balanced; at 1750 MHz	–	40	–	Ω
f_{TXmix}	TX mixer input frequency		1600	–	2000	MHz
RL_{TX}	return loss on matched TX input	note 1	10	15	–	dB
G_{CP}	conversion power gain	differential transmitter inputs to differential transmitter IF outputs loaded with 500 Ω differential	6	9	12	dB
$f_{o(TX)}$	TX mixer output frequency		50	–	400	MHz
$CP1_{TX}$	1 dB input compression point		–25	–22	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+22	–	dBm
$IP3_{TX}$	3rd order intercept point		–19	–16	–	dBm
NF_{TX}	noise figure	double sideband; notes 2 and 3	–	6	9	dB
I_{TX}	isolation	LOIN to TXIN; note 1	40	–	–	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 1	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2077BM demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2077BM demonstration board.
3. This value includes printed-circuit board and balun losses.
4. Measured and guaranteed only on UAA2077BM demonstration board at T_{amb} = +25 °C, with a 1 kΩ resistor between V_{QUADLO} and V_{CC}.

APPLICATION INFORMATION

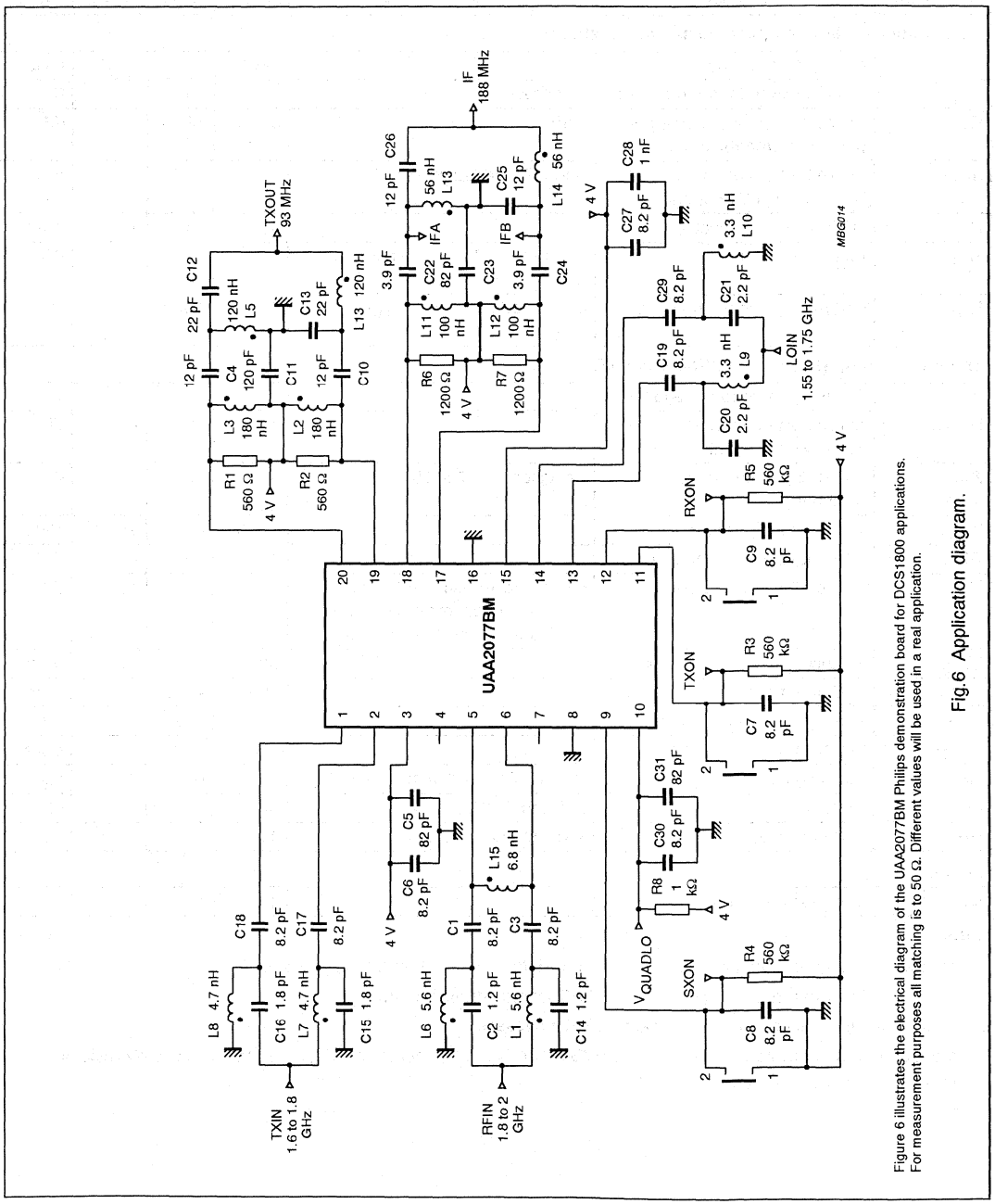


Fig.6 Application diagram.

Figure 6 illustrates the electrical diagram of the UAA2077BM Philips demonstration board for DCS1800 applications. For measurement purposes all matching is to 50 Ω. Different values will be used in a real application.

2 GHz image rejecting front-end UAA2077CM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 30 dB on-chip image rejection
- IF I/Q combiner at 188 MHz
- On-chip quadrature network
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- High frequency front-end for DCS1800/PCS1900 hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers e.g. RF-LANS.

GENERAL DESCRIPTION

UAA2077CM contains both a receiver front-end and a high frequency transmit mixer intended to be used in mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077CM is its ability to provide over 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

Signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a low-noise amplifier, and a down-conversion mixer. In the transmit mode, an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced.

Pins RXON, TXON and SXON allow to control the different power-down modes. A synthesizer-on (SX) mode enables LO buffers independent of the other circuits. When pin SXON is HIGH, all internal buffers on the LO path of the circuit are turned on, thus minimizing LO pulling when remainder of the receive or transmit chain is powered up. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	3.75	5.3	V
$I_{CC(RX)}$	receive supply current	27.5	36	44.5	mA
$I_{CC(TX)}$	transmit supply current	11	14	17.5	mA
$I_{CC(PD)}$	supply current in power-down	–	–	50	μA
T_{amb}	operating ambient temperature	–30	+25	+75	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2077CM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

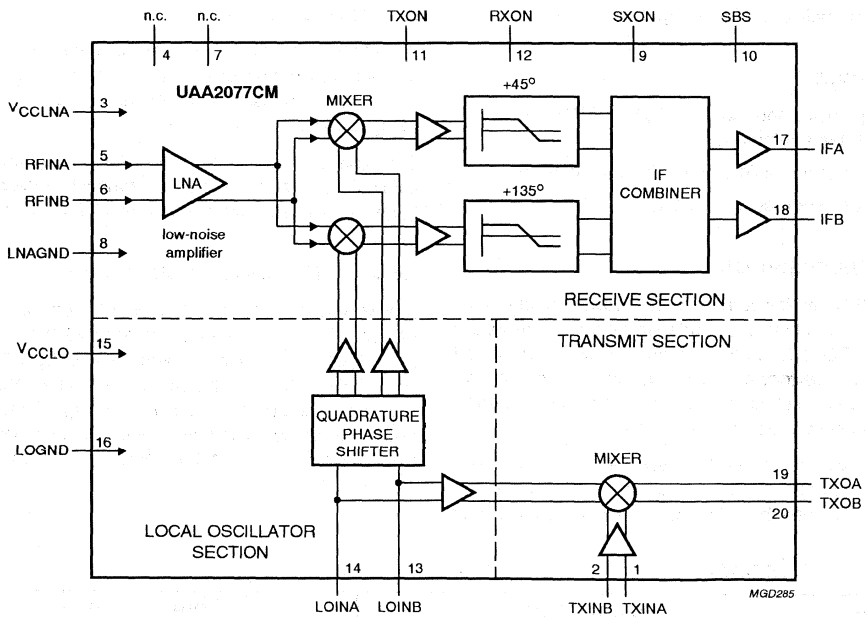


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXINA	1	transmit mixer input A (balanced)
TXINB	2	transmit mixer input B (balanced)
V_{CCLNA}	3	supply voltage for LNA, IF parts and TX mixer
n.c.	4	not connected
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
n.c.	7	not connected
LNAGND	8	ground for LNA, IF parts and TX mixer
SXON	9	SX mode enable (see Table 1)
SBS	10	sideband selection (should be grounded for $f_{LO} < f_{RF}$)
TXON	11	TX mode enable (see Table 1)
RXON	12	RX mode enable (see Table 1)
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
TXOA	19	transmit mixer IF output A (balanced)
TXOB	20	transmit mixer IF output B (balanced)

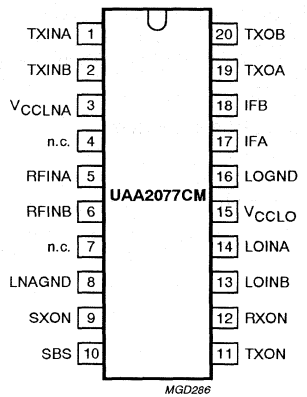


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin SBS allows sideband selection:

- $f_{LO} > f_{RF}$ (SBS = 1)
- $f_{LO} < f_{RF}$ (SBS = 0).

Where f_{RF} is the frequency of the wanted signal.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics.

The IF output is differential and of the open-collector type. Typical application will load the output with a 680 Ω resistor load at each IF output, plus a differential 1 kΩ load made of the input impedance of the IF filter or the input impedance of the matching network for the IF filter. The power gain refers to the available power on this 1 kΩ load. The path to V_{CC} for the DC current should be achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

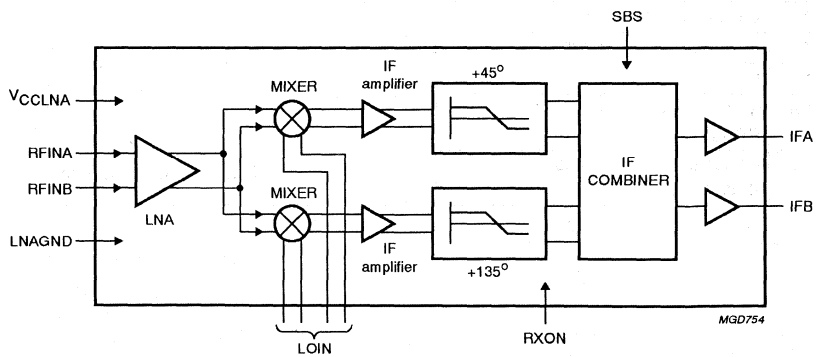


Fig.3 Block diagram, receive section.

Local oscillator section

The Local Oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

A synthesizer-ON mode (SX mode) is used to power-up all LO input buffers, thus minimizing the pulling effect on the external VCO when entering receive or transmit mode. This mode is active when SXON = 1.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF which is down-converted to a modulated transmit IF frequency, phase locked with the baseband modulation.

The IF outputs are HIGH impedance (open-collector type). Typical application will load the output with a 560 Ω resistor load, connected to V_{CC} for DC path, at each TX output, plus a differential 1 kΩ made of the input impedance of the matching network for the following TX part. The mixer can also be used for frequency up-conversion.

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON.

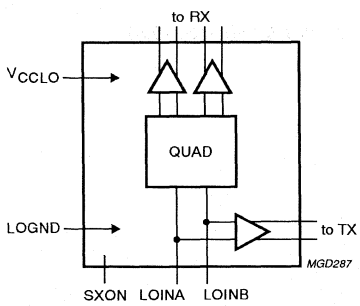


Fig.4 Block diagram, LO section.

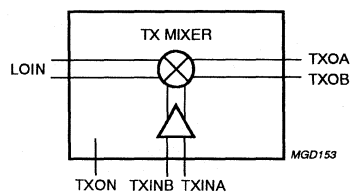


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SXON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	RX mode: receive section and LO buffers to RX on
HIGH	LOW	LOW	TX mode: transmit section and LO buffers to TX on
LOW	LOW	HIGH	SX mode: complete LO section on
LOW	HIGH	HIGH	SRX mode: receive section on and SX mode active
HIGH	LOW	HIGH	STX mode: transmit section on and SX mode active
HIGH	HIGH	X	receive section and transmit section on; specification not guaranteed

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{i(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	−65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

All pins withstand 1500 V ESD test in accordance with *"MIL-STD-883C class 1 (method 3015.5)"*.

DC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CCLNA} and V_{CCLO}						
V_{CC}	supply voltage	over full temperature range	3.6	3.75	5.3	V
$I_{CC(RX)}$	supply current in RX mode		27.5	36	44.5	mA
$I_{CC(TX)}$	supply current in TX mode		11	14	17.5	mA
$I_{CC(PD)}$	supply current in power-down mode		–	–	50	μA
$I_{CC(SX)}$	supply current in SX mode		7	9	11	mA
$I_{CC(SRX)}$	supply current in SRX mode		29.5	38.5	47.5	mA
$I_{CC(STX)}$	supply current in STX mode		15	19.5	24	mA
Pins: RXON, TXON, SXON and SBS						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
I_{IH}	HIGH level static input current	pins at V_{CC} − 0.4 V	−1	–	+1	μA
I_{IL}	LOW level static input current	pins at 0.4 V	−1	–	+1	μA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive section on	1.8	2.0	2.2	V
Pins: IFA and IFB						
I_O	DC output current	receive section on	2.3	3.0	3.8	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section on	1.9	2.15	2.4	V
Pins: TXOA and TXOB						
I_O	DC output current	transmit section on	0.8	1.0	1.2	mA
Pins: LOINA and LOINB						
V_{LOIN}	DC input voltage level	RXON, TXON or SXON HIGH	2.6	2.9	3.2	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = −30 to +75 °C; f_{oRX} = 188 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
R_{iRX}	RF input resistance (real part of the parallel input impedance)	balanced; at 1960 MHz	–	60	–	Ω
C_{iRX}	RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1960 MHz	–	0.8	–	pF
f_{iRX}	RF input frequency		1805	–	1990	MHz
RL_{iRX}	return loss on matched RF input	balanced; note 1	15	20	–	dB
G_{CPRX}	conversion power gain	differential RF inputs to differential IF outputs loaded to 1 kΩ differential	20	23	26	dB
G_{rip}	gain ripple as a function of RF frequency	within 100 MHz bandwidth; note 2	–	0.2	0.5	dB
ΔG/T	gain variation with temperature	note 2	−20	−15	−10	mdB/K
$CP1_{RX}$	1 dB compression point	differential RF inputs to differential IF outputs; note 1	−25	−24	–	dB
DES	desensitisation	interferer frequency offset: 3 MHz; P_{in} = −26 dBm; interferer frequency offset: 20 MHz, P_{in} = −23 dBm differential RF inputs to differential IF outputs; note 1	–	–	5	dB
$IP2D_{RX}$	Half IF spurious rejection ($f_{RF} = f_{LO} + 0.5*f_{IF}$)	differential RF inputs to differential IF outputs; note 2	tbf	–	–	dBm
$IP3_{RX}$	3rd order intercept point	differential RF inputs to differential IF outputs; note 2	−21.5	−17	–	dBm
NF_{RX}	overall noise figure	differential RF inputs to differential IF outputs				
		T_{amb} = 25 °C; DCS frequency range; note 3	–	3.8	–	dB
		T_{amb} = 25 °C; PCS frequency range; notes 2 and 3	–	4.0	4.4	dB
		T_{amb} = −30 to +65 °C; PCS frequency range; notes 2 and 3	–	–	5.0	dB
Z_{LRX}	typical application IF output load impedance	balanced	–	1000	–	Ω
RL_{oRX}	return loss on matched IF output	balanced; note 1	15	20	–	dB
f_{oRX}	IF frequency range		–	188	–	MHz
IR	rejection of image frequency	$f_{RF} > f_{LO}$; f_{RF} is the frequency of the wanted signal	30	38	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Local oscillator section (receive section enabled)						
f_{iLO}	LO input frequency		1617	–	1802	MHz
R_{iLO}	LO input resistance (real part of the parallel input impedance)	balanced; at 1770 MHz	–	90	–	Ω
C_{iLO}	LO input inductance (imaginary part of the parallel input impedance)	balanced; at 1770 MHz	–	5	–	nH
RL_{iLO}	return loss on matched input (including standby mode)	note 1	10	15	–	dB
ΔRL_{iLO}	return loss variation between SX, SRX and STX modes	linear S_{11} variation; note 1	–	20	–	mU
P_{iLO}	LO input power level		–10	–6	0	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 2	40	–	–	dB
Transmit section (transmit section enabled)						
Z_{LTX}	TX IF typical load impedance	balanced	–	500	–	Ω
RL_{oTX}	return loss on matched transmitter IF output	note 1	11	15	–	dB
R_{iTX}	TX RF input resistance (real part of the parallel input impedance)	balanced; at 1880 MHz	–	60	–	Ω
C_{iTX}	TX RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1880 MHz	–	1	–	pF
f_{iTX}	TX mixer input frequency		1600	–	2000	MHz
RL_{iTX}	return loss on matched TX input	note 1	10	15	–	dB
G_{CPTX}	conversion power gain	differential transmitter inputs to differential transmitter IF outputs loaded with 500 Ω differential	6	9	12	dB
f_{oTX}	TX output frequency		50	–	400	MHz
$CP1_{TX}$	1 dB input compression point	note 1	–25	–22	–	dBm
$IP2_{TX}$	2nd order intercept point	note 2	–	+22	–	dBm
$IP3_{TX}$	3rd order intercept point	note 2	–20	–16	–	dBm
NF_{TX}	noise figure	double sideband; notes 2 and 3	–	5	9	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2077CM PCS demonstration board at T_{amb} = 25 °C.
2. Measured and guaranteed only on UAA2077CM PCS demonstration board.
3. This value includes printed-circuit board and balun losses.

APPLICATION INFORMATION

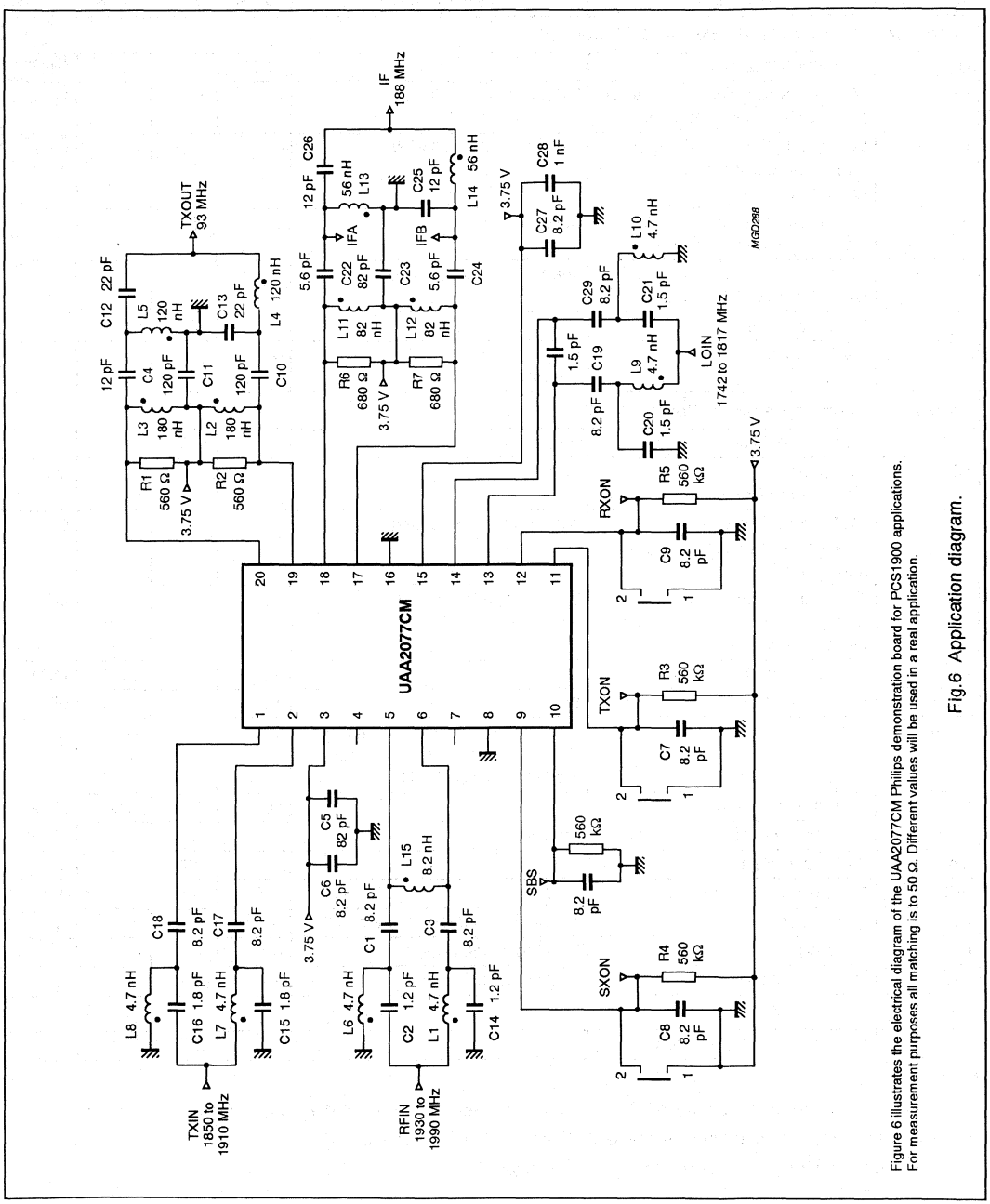


Figure 6 illustrates the electrical diagram of the UAA2077CM Philips demonstration board for PCS1900 applications. For measurement purposes all matching is to 50 Ω. Different values will be used in a real application.

Fig.6 Application diagram.

Advanced pager receiver — UAA2080

FEATURES

- Wide frequency range: VHF, UHF and 900 MHz bands
- High sensitivity
- High dynamic range
- Electronically adjustable filters on chip
- Suitable for data rates up to 2400 bits/s
- Wide frequency offset and deviation range
- Fully POCSAG compatible FSK receiver
- Power on/off mode selectable by the chip enable input
- Low supply voltage; low power consumption
- High integration level
- Interfaces directly to the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.

APPLICATIONS

- Wide area paging
- On-site paging
- Telemetry
- RF security systems
- Low bit-rate wireless data links.

GENERAL DESCRIPTION

The UAA2080 is a high-performance low-power radio receiver circuit primarily intended for VHF, UHF and 900 MHz pager receivers for wide area digital paging systems, employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK).

The receiver design is based on the direct conversion principle where the input signal is mixed directly down to the baseband by a local oscillator on the signal frequency. Two complete signal paths with signals of 90° phase difference are required to demodulate the signal. All channel selectivity is provided by the built-in IF filters. The circuit makes extensive use of on-chip capacitors to minimize the number of external components.

The UAA2080 was designed to operate together with the PCA5000A, PCF5001 or PCD5003 POCSAG decoders, which contain a digital input filter for optimum call success rate.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2080H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
UAA2080T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UAA2080U	28 pads	naked die; see Fig.9	

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current		2.3	2.7	3.2	mA
$I_{P(off)}$	stand-by current		–	–	3	µA
$P_{i(ref)}$	RF input sensitivity	BER ≤ $^3/_{100}$; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C				
		$f_{i(RF)}$ = 173 MHz	–	−126.5	−123.5	dBm
		$f_{i(RF)}$ = 470 MHz	–	−124.5	−121.5	dBm
		$f_{i(RF)}$ = 930 MHz	–	−120.0	−114.0	dBm
$P_{i(mix)}$	mixer input sensitivity	BER ≤ $^3/_{100}$; $f_{i(RF)}$ = 470 MHz; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C	–	−115.0	−110.0	dBm
V_{th}	detection threshold for battery LOW indicator		1.95	2.05	2.15	V
T_{amb}	operating ambient temperature		−10	–	+70	°C

PINNING (LQFP32)

SYMBOL	PIN	DESCRIPTION
TS	1	test switch; connection to ground for normal operation
BLI	2	battery LOW indicator output
DO	3	data output
RE	4	receiver enable input
TPI	5	IF test point; I channel
TPQ	6	IF test point; Q channel
VI1RF	7	pre-amplifier RF input 1
VI2RF	8	pre-amplifier RF input 2
n.c.	9	not connected
RRFA	10	external emitter resistor for pre-amplifier
GND1	11	ground 1 (0 V)
VO2RF	12	pre-amplifier RF output 2
VO1RF	13	pre-amplifier RF output 1
V_P	14	supply voltage
VI2MI	15	I channel mixer input 2
VI1MI	16	I channel mixer input 1
n.c.	17	not connected
VI1MQ	18	Q channel mixer input 1
VI2MQ	19	Q channel mixer input 2
GND2	20	ground 2 (0 V)
COM	21	gyrator filter resistor; common line
RGYR	22	gyrator filter resistor
n.c.	23	not connected
VO1MUL	24	frequency multiplier output 1
VO2MUL	25	frequency multiplier output 2
RMUL	26	external emitter resistor for frequency multiplier
TDC	27	DC test point; no external connection for normal operation
OSC	28	oscillator collector
n.c.	29	not connected
GND3	30	ground 3 (0 V)
OSB	31	oscillator base; crystal input
OSE	32	oscillator emitter

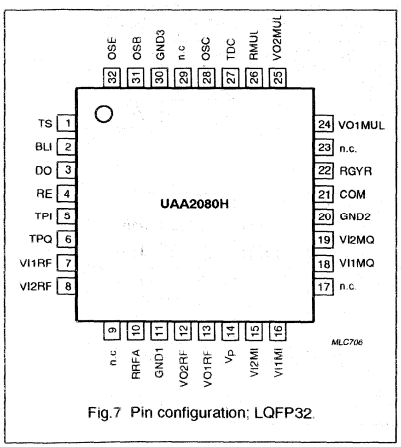


Fig.7 Pin configuration; LQFP32.

PINNING (SO28)

SYMBOL	PIN	DESCRIPTION
TPI	1	IF test point; I channel
TPQ	2	IF test point; Q channel
VI1RF	3	pre-amplifier RF input 1
VI2RF	4	pre-amplifier RF input 2
RRFA	5	external emitter resistor for pre-amplifier
GND1	6	ground 1 (0 V)
VO2RF	7	pre-amplifier RF output 2
VO1RF	8	pre-amplifier RF output 1
V_P	9	supply voltage
VI2MI	10	I channel mixer input 2
VI1MI	11	I channel mixer input 1
VI1MQ	12	Q channel mixer input 1
VI2MQ	13	Q channel mixer input 2
GND2	14	ground 2 (0 V)
COM	15	gyrator filter resistor; common line
RGYR	16	gyrator filter resistor
VO1MUL	17	frequency multiplier output 1
VO2MUL	18	frequency multiplier output 2
RMUL	19	external emitter resistor for frequency multiplier
TDC	20	DC test point; no external connection for normal operation
OSC	21	oscillator collector
GND3	22	ground 3 (0 V)
OSB	23	oscillator base; crystal input
OSE	24	oscillator emitter
TS	25	test switch; connection to ground for normal operation
BLI	26	battery LOW indicator output
DO	27	data output
RE	28	receiver enable input

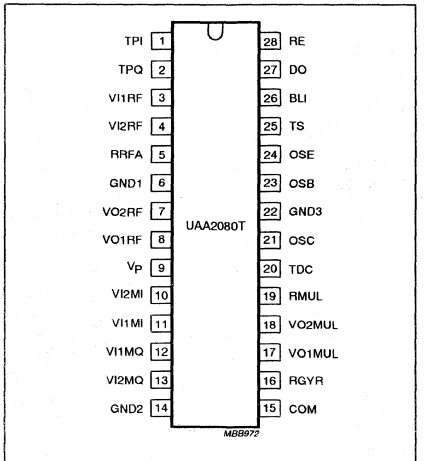


Fig.8 Pin configuration; SO28.

DC CHARACTERISTICS

V_P = 2.05 V; T_{amb} = −10 to +70 °C (typical values at T_{amb} = 25 °C); measurements taken in test circuit Figs 1, 2, 3 or 4 with crystal at pin OSB disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current	V_{RE} = HIGH; $f_{i(RF)}$ = 173 and 470 MHz	2.3	2.7	3.2	mA
		V_{RE} = HIGH; $f_{i(RF)}$ = 930 MHz	2.9	3.4	3.9	mA
$I_{P(off)}$	stand-by current	V_{RE} = LOW	–	–	3	μA
Receiver enable input (pin RE)						
V_{IH}	HIGH level input voltage		1.4	–	V_P	V
V_{IL}	LOW level input voltage		0	–	0.3	V
I_{IH}	HIGH level input current	V_{IH} = V_P = 3.5 V	–	–	20	μA
V_{IL}	LOW level input current	V_{IL} = 0 V	0	–	−1.0	μA
Battery LOW indicator output (pin BLI)						
V_{OH}	HIGH level output voltage	$V_P < V_{th}$; I_{BLI} = −10 μA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	$V_P > V_{th}$; I_{BLI} = +10 μA	–	–	0.5	V
V_{th}	voltage threshold for battery LOW indicator		1.95	2.05	2.15	V
Demodulator output (pin DO)						
V_{OH}	HIGH level output voltage	I_{DO} = −10 μA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	I_{DO} = +10 μA	–	–	0.5	V

AC CHARACTERISTICS (173 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Figs 1 or 2; $f_{i(RF)}$ = 172.941 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ±25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–126.5	–123.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–120.5	dBm
		V_P = 1.9 V	–	–	–117.5	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	69	72	–	dB
		T_{amb} = –10 to +70 °C	67	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	78	85	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (470 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Figs 3 or 4; $f_{i(RF)}$ = 469.950 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–124.5	–121.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–118.5	dBm
		V_P = 1.9 V	–	–	–115.5	dBm
Mixer input						
$P_{i(mix)}$	input sensitivity	BER ≤ $^3/_{100}$; note 3	–	–115.0	–110.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	67	70	–	dB
		T_{amb} = –10 to +70 °C	65	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 4	75	82	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 5	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Test circuit Fig.5. $P_{i(mix)}$ is the maximum available power at the input of the test board. The bit error rate BER is measured using the test facility shown in Fig.13.
4. Δf is the frequency offset between the required signal and the interfering signal.
5. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (930 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.6 (note 1); $f_{i(RF)}$ = 930.500 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 μs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 2	–	−120.0	−114.0	dBm
		V_P = 1.9 V	–	–	−108.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	60	69	–	dB
α_c	co-channel rejection		–	5	10	dB
α_{sp}	spurious immunity		40	60	–	dB
α_{im}	intermodulation immunity		53	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	65	74	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz and a level of −15 dBm.
2. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

Advanced pager receiver UAA2082

FEATURES

- Wide frequency range: VHF, UHF and 900 MHz bands
- High sensitivity
- High dynamic range
- Electronically adjustable filters on chip
- Suitable for data rates up to 2400 bits/s
- Wide frequency offset and deviation range
- Fully POCSAG compatible FSK receiver
- Power on/off mode selectable by the chip enable input
- Low supply voltage; low power consumption
- 1-cell battery-low detection circuit
- High integration level
- Interfaces directly to the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.

APPLICATIONS

- Wide area paging
- On-site paging
- Telemetry
- RF security systems
- Low bit-rate wireless data links.

GENERAL DESCRIPTION

The UAA2082 is a high-performance low-power radio receiver circuit primarily intended for VHF, UHF and 900 MHz pager receivers for wide area digital paging systems, employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK).

The receiver design is based on the direct conversion principle where the input signal is mixed directly down to the baseband by a local oscillator on the signal frequency. Two complete signal paths with signals of 90° phase difference are required to demodulate the signal. All channel selectivity is provided by the built-in IF filters. The circuit makes extensive use of on-chip capacitors to minimize the number of external components.

The battery monitoring circuit has an external sense input and a 1.1 V detection threshold for easy operation in a single-cell supply concept.

The UAA2082 was designed to operate together with the PCA5000A, PCF5001 or PCD5003 POCSAG decoders, which contain a digital input filter for optimum call success rate.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2082H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
UAA2082U	28 pads	naked die; see Fig.8	

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current		2.3	2.7	3.2	mA
$I_{P(off)}$	stand-by current		–	–	3	µA
$P_{i(ref)}$	RF input sensitivity	BER ≤ $^3/_{100}$; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C				
		$f_{i(RF)}$ = 173 MHz	–	–126.5	–123.5	dBm
		$f_{i(RF)}$ = 470 MHz	–	–124.5	–121.5	dBm
		$f_{i(RF)}$ = 930 MHz	–	–120.0	–114.0	dBm
$P_{i(mix)}$	mixer input sensitivity	BER ≤ $^3/_{100}$; $f_{i(RF)}$ = 470 MHz; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C	–	–115.0	–110.0	dBm
V_{th}	detection threshold for battery LOW indicator	T_{amb} = 25 °C	1.05	1.10	1.15	V
		T_{amb} = –10 to +70 °C	1.03	1.10	1.17	V
T_{amb}	operating ambient temperature		–10	–	+70	°C

BLOCK DIAGRAMS (173 MHz)

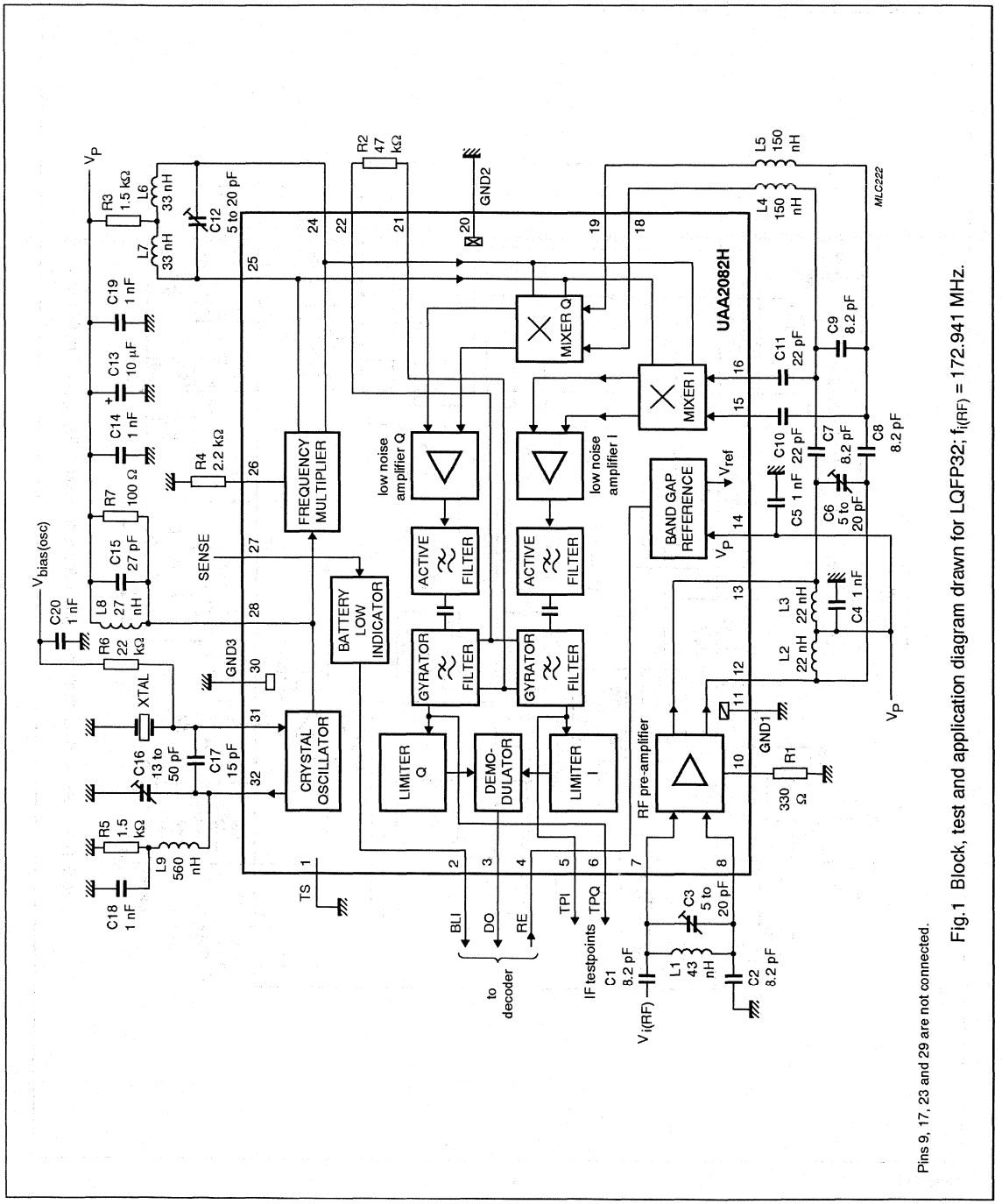


Fig.1 Block, test and application diagram drawn for LQFP32; $f_{i(RF)}$ = 172.941 MHz.

Pins 9, 17, 23 and 29 are not connected.

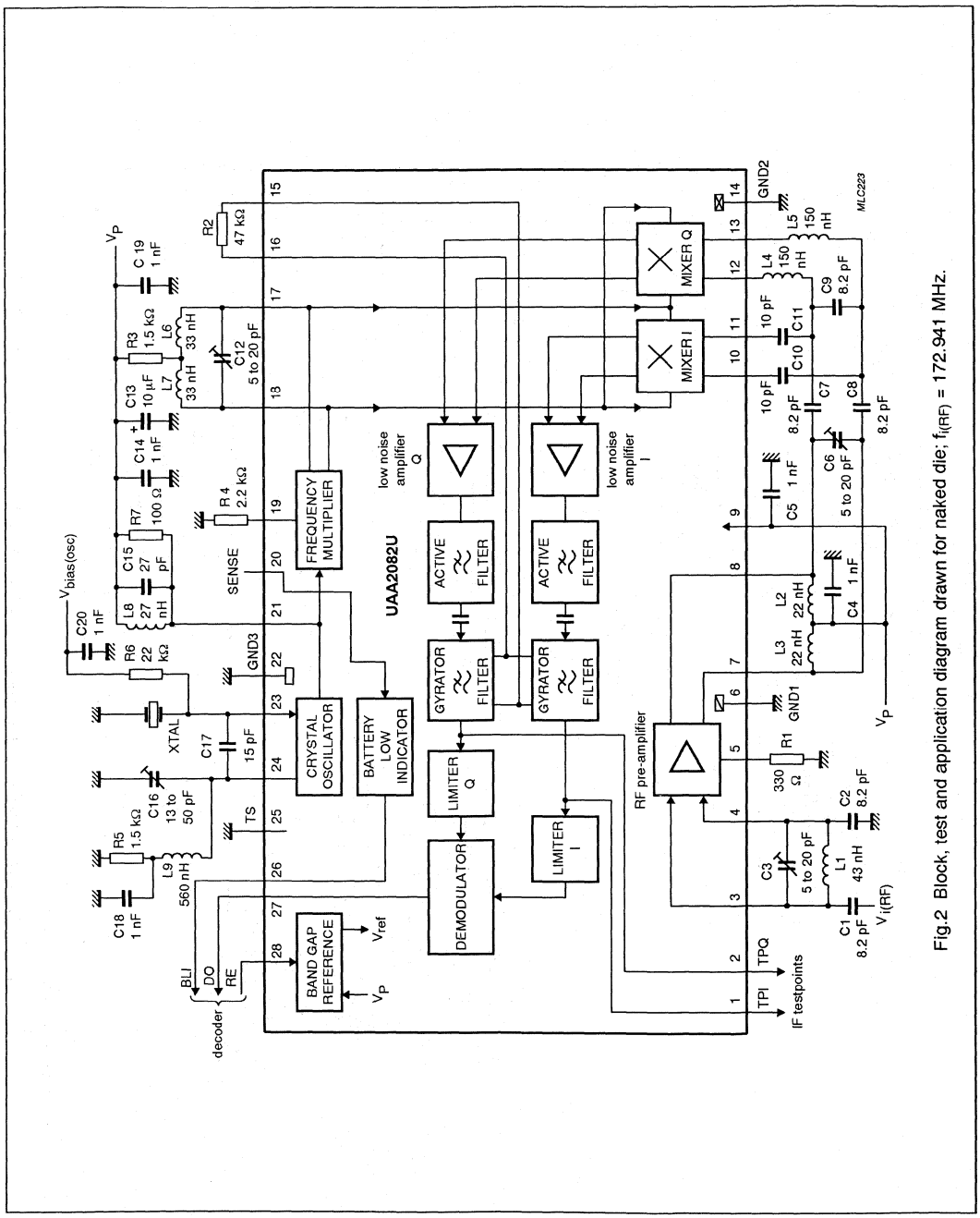


Fig.2 Block, test and application diagram drawn for naked die; $f_{i(RF)}$ = 172.941 MHz.

Table 1 Tolerances of components shown in Figs 1 and 2 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±5	Q_{min} = 100 at 173 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±20	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 30 at 57 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R7	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12	–	TC = (−750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18, C19, C20	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (−1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 57.647 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF series capacitor at 25 °C), dynamic resistance R1 < 40 Ω, Δf = ±5 × 10^{-6} for T_{amb} = −10 to +55 °C with 25 °C reference, calibration plus aging tolerance: −5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAMS (470 MHz)

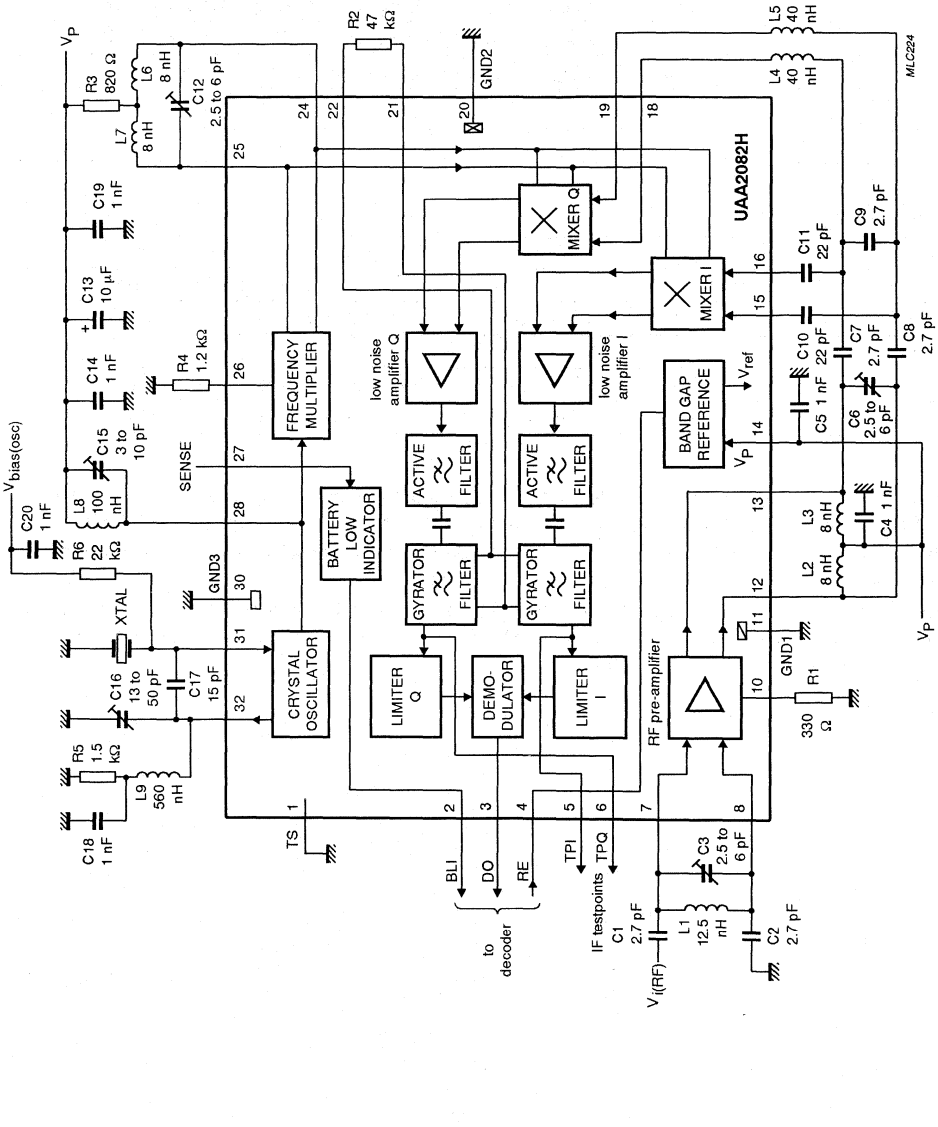


Fig.3 Block, test and application diagram drawn for LQFP32; $f_{i(RF)}$ = 469.95 MHz.

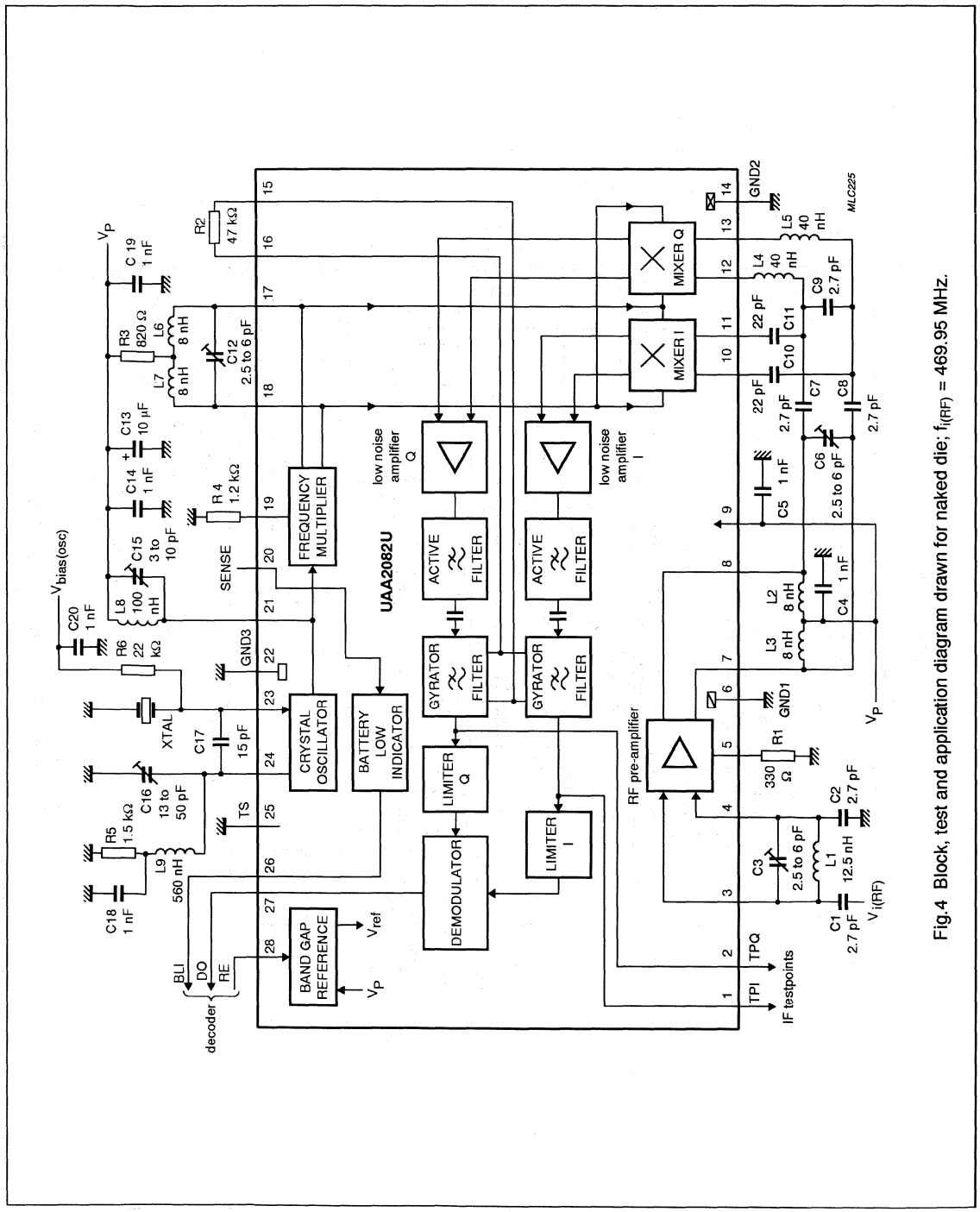


Fig.4 Block, test and application diagram drawn for naked die; $f_{i(RF)}$ = 469.95 MHz.

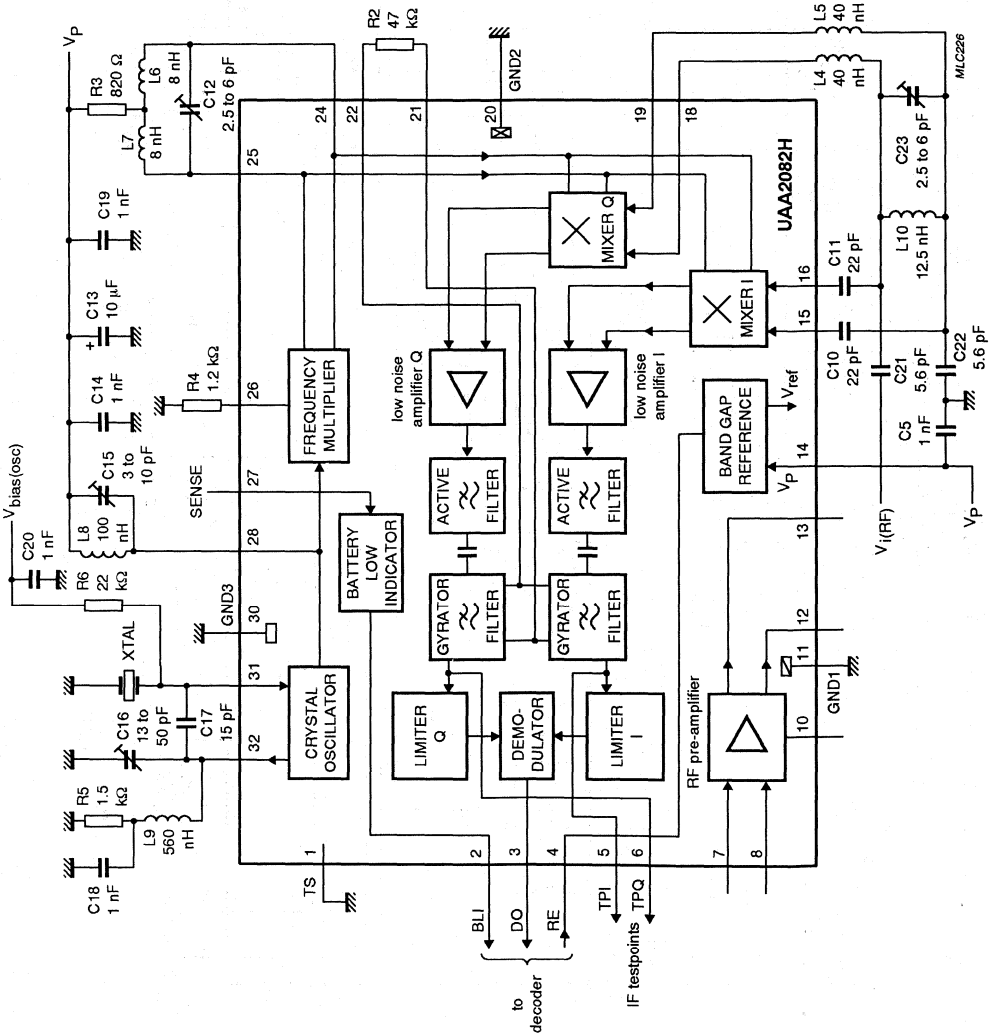


Fig.5 Mixer input sensitivity test circuit; $f_{i(RF)}$ = 469.95 MHz.

Table 2 Tolerances of components shown in Figs 3, 4 and 5 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1, L10	±5	Q_{min} = 145 at 470 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 40 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±10	Q_{min} = 30 at 156 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 40 at 78 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R6	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12, C23	–	TC = (−750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18 to C22	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (−1 700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 78.325 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF capacitor at 25 °C), dynamic resistance R1 < 30 Ω, Δf = ±5 × 10^{-6} for T_{amb} = −10 to +55 °C with 25 °C reference, calibration plus aging tolerance: −5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAM (930 MHz)

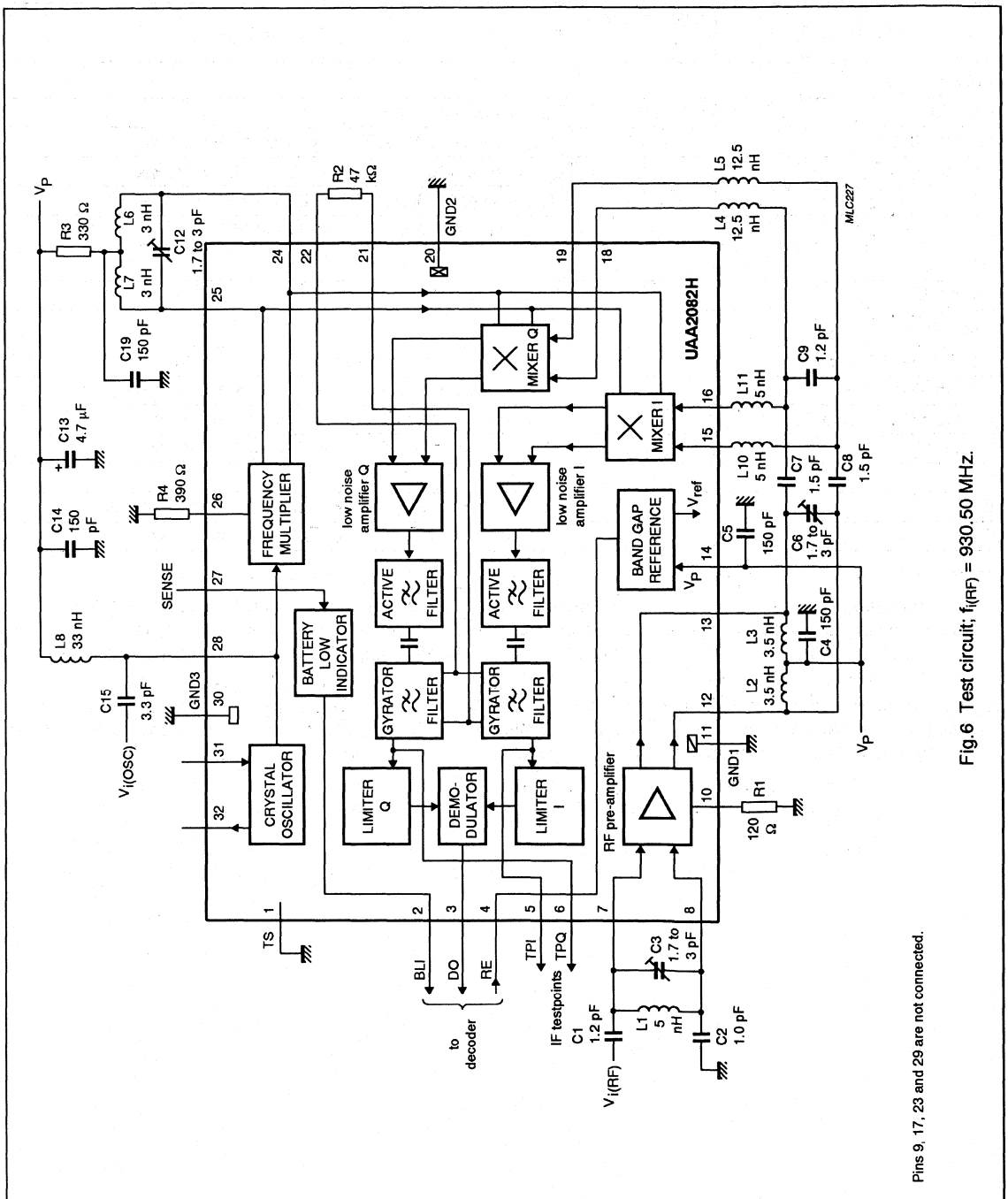


Fig.6 Test circuit; $f_{i(RF)}$ = 930.50 MHz.

Pins 9, 17, 23 and 29 are not connected.

Table 3 Tolerances of components shown in Fig.6 (note 1)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±10	Q_{typ} = 150 at 930 MHz
L2, L3, L6, L7	–	microstrip inductor
L4, L5	±5	Q_{typ} = 100 at 930 MHz
L8	±10	Q_{typ} = 65 at 310 MHz
L10, L11	±10	Q_{typ} = 150 at 930 MHz
Resistors		
R1 to R4	±2	TC = (0 ±200) × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12	–	TC = (0 ±200) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C4, C5, C14, C19	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C13	±20	

Note

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz.

PINNING (LQFP32)

SYMBOL	PIN	DESCRIPTION
TS	1	test switch; connection to ground for normal operation
BLI	2	battery LOW indicator output
DO	3	data output
RE	4	receiver enable input
TPI	5	IF test point; I channel
TPQ	6	IF test point; Q channel
VI1RF	7	pre-amplifier RF input 1
VI2RF	8	pre-amplifier RF input 2
n.c.	9	not connected
RRFA	10	external emitter resistor for pre-amplifier
GND1	11	ground 1 (0 V)
VO2RF	12	pre-amplifier RF output 2
VO1RF	13	pre-amplifier RF output 1
V_P	14	supply voltage
VI2MI	15	I channel mixer input 2
VI1MI	16	I channel mixer input 1
n.c.	17	not connected
VI1MQ	18	Q channel mixer input 1
VI2MQ	19	Q channel mixer input 2
GND2	20	ground 2 (0 V)
COM	21	gyrator filter resistor; common line
RGYR	22	gyrator filter resistor
n.c.	23	not connected
VO1MUL	24	frequency multiplier output 1
VO2MUL	25	frequency multiplier output 2
RMUL	26	external emitter resistor for frequency multiplier
SENSE	27	battery LOW detector sense input
OSC	28	oscillator collector
n.c.	29	not connected
GND3	30	ground 3 (0 V)
OSB	31	oscillator base; crystal input
OSE	32	oscillator emitter

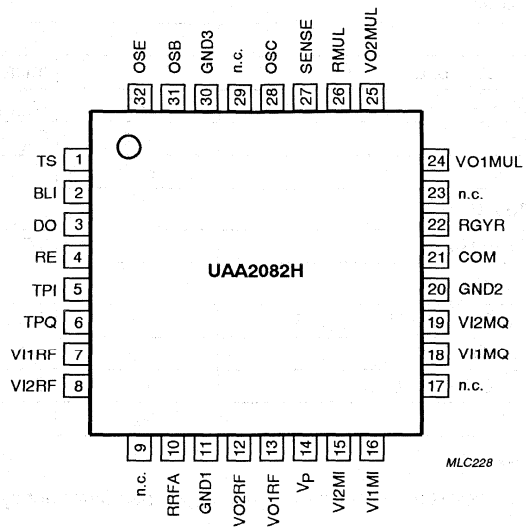
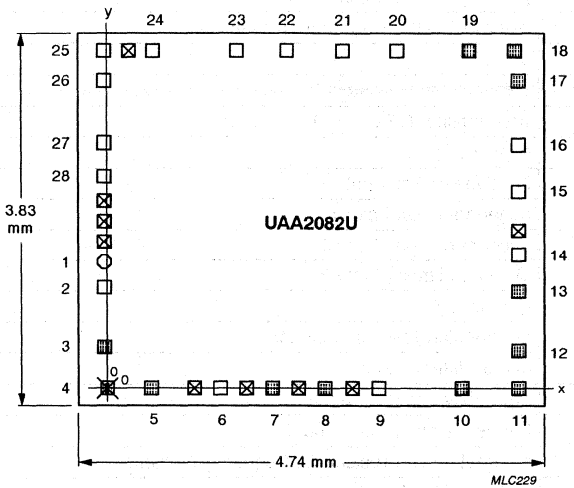


Fig.7 Pin configuration; LQFP32.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

See Table 4 for bonding pad description and locations for x/y co-ordinates.



Where:

- ○ Pad number 1 (diameter 124 μm)
- □ Pad 124 μm x 124 μm
- ⊠ Pad not used
- ▦ Pad 100 μm x 100 μm
- ⊠ Pad 100 μm x 100 μm with reference point

Chip area: 18.15 mm^2
Chip thickness: 380 ±20 μm.
Drawing not to scale.

Fig.8 Bonding pad locations.

Table 4 Bonding pad centre locations (dimensions in μm)

SYMBOL	PAD	DESCRIPTION	x	y
TPI	1	IF test point; I channel	−32	1296
TPQ	2	IF test point; Q channel	−32	1000
VI1RF	3	pre-amplifier RF input 1	−32	360
VI2RF	4	pre-amplifier RF input 2; note 1	0	0
RRFA	5	external emitter resistor for pre-amplifier	472	0
GND1	6	ground 1 (0 V)	1160	0
VO2RF	7	pre-amplifier RF output 2	1688	0
VO1RF	8	pre-amplifier RF output 1	2232	0
V_P	9	supply voltage	2760	0
VI2MI	10	I channel mixer input 2	3608	0
VI1MI	11	I channel mixer input 1	4216	0
VI1MQ	12	Q channel mixer input 1	4216	360
VI2MQ	13	Q channel mixer input 2	4216	960
GND2	14	ground 2 (0 V)	4216	1360
COM	15	gyrator filter resistor; common line	4216	2024
RGYR	16	gyrator filter resistor	4216	2496
VO1MUL	17	frequency multiplier output 1	4216	3136
VO2MUL	18	frequency multiplier output 2	4176	3456
RMUL	19	external emitter resistor for frequency multiplier	3668	3458
SENSE	20	battery LOW detector sense input	2952	3456
OSC	21	oscillator collector	2312	3456
GND3	22	ground 3 (0 V)	1832	3456
OSB	23	oscillator base; crystal input	1328	3456
OSE	24	oscillator emitter	432	3456
TS	25	test switch; connection to ground for normal operation	−32	3456
BLI	26	battery LOW indicator output	−32	3136
DO	27	data output	−32	2512
RE	28	receiver enable input	−32	2152
		lower left corner of chip (typical values)	−278	−186

Note

1. All x/y co-ordinates are referenced to the centre of pad 4 (VI2RF); see Fig.8.

INTERNAL CIRCUITS

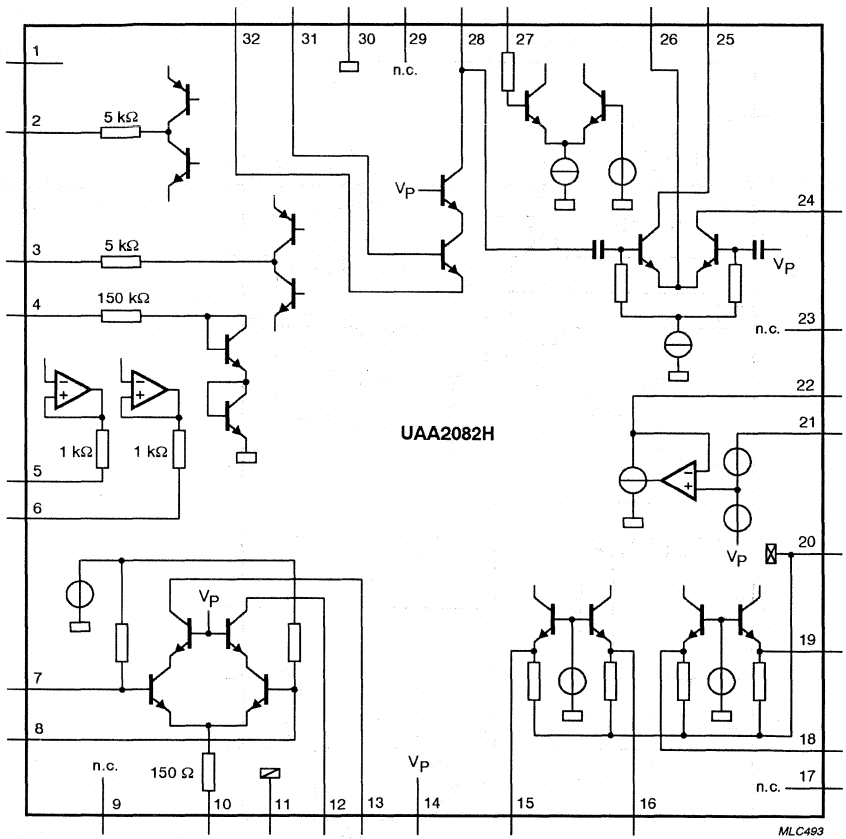


Fig.9 Internal circuits drawn for LQFP32.

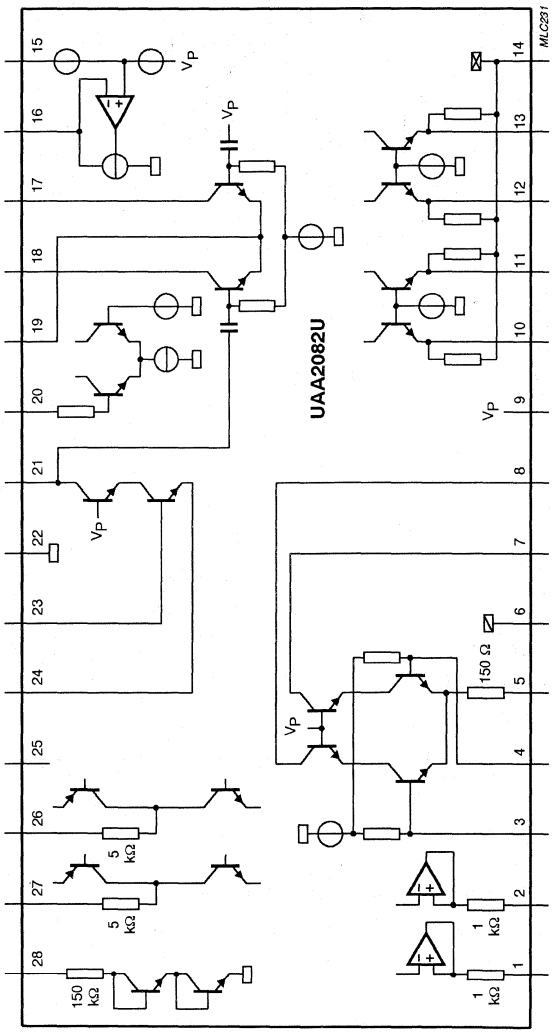


Fig.10 Internal circuits drawn for naked die.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Figs 1 to 6.

Radio frequency amplifier

The RF amplifier is an emitter-coupled pair driving a balanced cascode stage, which drives an external balanced tuned circuit. Its bias current is set by an external 300 Ω resistor R1 to typically 770 μA. With this bias current the optimum source resistance is 1.3 kΩ at VHF and 1.0 kΩ at UHF. At 930 MHz a higher bias current is required to achieve optimum gain. A value of 120 Ω is used for R1, which corresponds with a bias current of approximately 1.3 mA and an optimum source resistance of approximately 600 Ω.The capacitors C1 and C2 transform a 50 Ω source resistance to this optimum value. The output drives a tuned circuit with capacitive divider (C7, C8 and C9) to provide maximum power transfer to the phase-splitting network and the mixers.

Mixers

The double balanced mixers consist of common base input stages and upper switching stages driven from the frequency multiplier. The 300 Ω input impedance of each mixer acts together with external components (C10, C11; L4, L5 respectively) as phase shifter/power splitter to provide a differential phase shift of 90 degrees between the I channel and the Q channel. At 930 MHz all external phase shifter components are inductive (L10, L11; L4, L5).

Oscillator

The oscillator is based on a transistor in common collector configuration. It is followed by a cascode stage driving a tuned circuit which provides the signal for the frequency multiplier. The oscillator transistor requires an external bias voltage $V_{bias(osc)}$ (1.22 V typ.). The oscillator bias current (typically 250 μA) is determined by the 1.5 kΩ external resistor R5. The oscillator frequency is controlled by an external 3rd overtone crystal in parallel resonance mode. External capacitors between base and emitter (C17) and from emitter to ground (C16) make the oscillator transistor appear as having a negative resistance for small signals; this causes the oscillator to start. Inductance L9 connected in parallel with capacitor C16 to the emitter of the oscillator transistor prevents oscillation at the fundamental frequency of the crystal.

The resonant circuit at output pin OSC selects the second harmonic of the oscillator frequency. In other applications a different multiplication factor may be chosen.

At 930 MHz an external oscillator circuit is required to provide sufficient local oscillator signal for the frequency multiplier.

Frequency multiplier

The frequency multiplier is an emitter-coupled pair driving an external balanced tuned circuit. Its bias current is set by external resistor R4 to typically 190 μA (173 MHz), 350 μA (470 MHz) and 1 mA (930 MHz). The oscillator signal is internally AC coupled to one input of the emitter-coupled pair while the other input is internally grounded via a capacitor. The frequency multiplier output signal between pins VO1MUL and VO2MUL drives the upper switching stages of the mixers. The bias voltage on pins VO1MUL and VO2MUL is set by external resistor R3 to allow sufficient voltage swing at the mixer outputs. The value of R3 depends on the operating frequency: 1.5 kΩ (173 MHz), 820 Ω (470 MHz) and 330 Ω (930 MHz).

Low noise amplifiers, active filters and gyrator filters

The low noise amplifiers ensure that the noise of the following stages does not affect the overall noise figure. The following active filters before the gyrator filters reduce the levels of large signals from adjacent channels. Internal AC couplings block DC offsets from the gyrator filter inputs.

The gyrator filters implement the transfer function of a 7th order elliptic filter. Their cut-off frequencies are determined by the 47 kΩ external resistor R2 between pins RGYR and COM. The gyrator filter output signals are available on IF test pins TPI and TPQ.

Limiters

The gyrator filter output signals are amplified in the limiter amplifiers to obtain IF signals with removed amplitude information.

Demodulator

The limiter amplifier output signals are fed to the demodulator. The demodulator output DO is going LOW or HIGH depending upon which of the input signals has a phase lead.

Battery LOW indicator

The battery LOW indicator senses the supply voltage and sets its output HIGH when the voltage at input SENSE is less than V_{th} (typically 1.10 V). Low battery warning is available at BLI.

Band gap reference

The whole chip except the oscillator section can be powered-up and powered-down by enabling and disabling the band gap reference via the receiver enable pin RE.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
Ground pins GND1, GND2 and GND3 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	−0.3	+8.0	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−10	+70	°C
V_{es}	electrostatic handling; note 1			
	pins VI1RF and VI2RF	−1500	+2000	V
	pin RRFA	−500	+2000	V
	pins VO1RF and VO2RF	−2000	+250	V
	pins V_P and OSB	−500	+500	V
	pins OSC and OSE	−2000	+500	V
	other pins	−2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor.

DC CHARACTERISTICS

V_P = 2.05 V; T_{amb} = −10 to +70 °C (typical values at T_{amb} = 25 °C); measurements taken in test circuit Figs 1, 2, 3 or 4 with crystal at pin OSB disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current	V_{RE} = HIGH; $f_{i(RF)}$ = 173 and 470 MHz	2.3	2.7	3.2	mA
		V_{RE} = HIGH; $f_{i(RF)}$ = 930 MHz	2.9	3.4	3.9	mA
$I_{P(off)}$	stand-by current	V_{RE} = LOW	–	–	3	μA
$V_{bias(osc)}$	oscillator bias voltage		1.20	1.22	1.24	V
Receiver enable input (pin RE)						
V_{IH}	HIGH level input voltage		1.4	–	V_P	V
V_{IL}	LOW level input voltage		0	–	0.3	V
I_{IH}	HIGH level input current	V_{IH} = V_P = 3.5 V	–	–	20	μA
V_{IL}	LOW level input current	V_{IL} = 0 V	0	–	−1.0	μA
Battery LOW indicator output (pin BLI)						
V_{OH}	HIGH level output voltage	V_{SENSE} < V_{th}; I_{BLI} = −10 μA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	V_{SENSE} > V_{th}; I_{BLI} = +10 μA	–	–	0.5	V
V_{th}	voltage threshold for battery LOW indicator	V_P = 2.05 V; T_{amb} = 25 °C	1.05	1.10	1.15	V
		V_P = 2.05 to 3.5 V; T_{amb} = −10 to +70 °C	1.03	1.10	1.17	V
Demodulator output (pin DO)						
V_{OH}	HIGH level output voltage	I_{DO} = −10 μA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	I_{DO} = +10 μA	–	–	0.5	V

AC CHARACTERISTICS (173 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Figs 1 or 2; $f_{i(RF)}$ = 172.941 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ±25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–126.5	–123.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–120.5	dBm
		V_P = 1.9 V	–	–	–117.5	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	69	72	–	dB
		T_{amb} = –10 to +70 °C	67	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	78	85	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (470 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Figs 3 or 4; $f_{i(RF)}$ = 469.950 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–124.5	–121.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–118.5	dBm
		V_P = 1.9 V	–	–	–115.5	dBm
Mixer input						
$P_{i(mix)}$	input sensitivity	BER ≤ $^3/_{100}$; note 3	–	–115.0	–110.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	67	70	–	dB
		T_{amb} = –10 to +70 °C	65	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 4	75	82	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 5	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Test circuit Fig.5. $P_{i(mix)}$ is the maximum available power at the input of the test board. The bit error rate BER is measured using the test facility shown in Fig.12.
4. Δf is the frequency offset between the required signal and the interfering signal.
5. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (930 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.6; note 1; $f_{i(RF)}$ = 930.500 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 2	–	–120.0	–114.0	dBm
		V_P = 1.9 V	–	–	–108.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	60	69	–	dB
α_c	co-channel rejection		–	5	10	dB
α_{sp}	spurious immunity		40	60	–	dB
α_{im}	intermodulation immunity		53	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	65	74	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz and a level of –15 dBm.
2. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

TEST INFORMATION

Tuning procedure for AC tests

1. Turn on the signal generator: $f_{gen} = f_{i(RF)} + 4$ kHz, no modulation, $V_{i(RF)} = 1$ mV (RMS).
2. Measure the IF with a counter connected to test pin TPI. Tune C16 to set the crystal oscillator to achieve $f_{IF} = 4$ kHz Change the generator frequency to $f_{gen} = f_{i(RF)} - 4$ kHz and check that f_{IF} is also 4 kHz. For a received input frequency $f_{i(RF)} = 172.941$ MHz the crystal frequency is $f_{XTAL} = 57.647$ MHz, while for $f_{i(RF)} = 469.950$ MHz the crystal frequency is $f_{XTAL} = 78.325$ MHz. For a received input frequency $f_{i(RF)} = 930.500$ MHz an external oscillator signal must be used with $f_{i(OSC)} = 310.1667$ MHz and a level of −15 dBm (for definition of crystal frequency, see Table 1).
3. Set the signal generator to nominal frequency ($f_{i(RF)}$) and turn on the modulation deviation ±4.0 kHz, 600 Hz square wave modulation, $V_{i(RF)} = 1$ mV (RMS). Note that the RF signal should be reduced in the following tests, as the receiver is tuned, to ensure $V_{o(IF)} = 10$ to 50 mV (p-p) on test pins TPI or TPQ.
4. Tune C15 (oscillator output circuit) and C12 (frequency multiplier output) to obtain a peak audio voltage on pin TPI.
5. Tune C3 and C6 (RF input and mixer input) to obtain a peak audio voltage on pin TPI. When testing the mixer input sensitivity tune C23 instead of C3 and C6 (test circuit Fig.5).
6. Check that the output signal on pin TPQ is within 3 dB in amplitude and at 90° (±20°) relative phase of the signal on pin TPI.
7. Check that data signal appears on output pin DO and proceed with the AC test.

AC test conditions

Table 5 Definitions for AC test conditions (see Table 6)

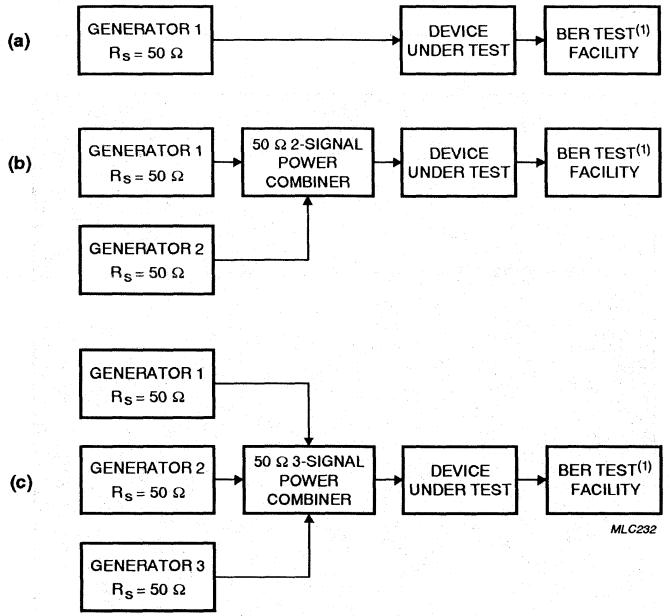
SIGNAL	DESCRIPTION
Modulated test signal 1	
Frequency	172.941, 469.950 or 930.500 MHz
Deviation	±4.0 kHz
Modulation	1200 baud pseudo random bit sequence
Rise time	250 ±25 μs (between 10% and 90% of final value)
Modulated test signal 2	
Deviation	±2.4 kHz
Modulation	400 Hz sine wave
Other definitions	
f_1	frequency of signal generator 1
f_2	frequency of signal generator 2
f_3	frequency of signal generator 3
Δf_{cs}	channel spacing (20 kHz)
P_1	maximum available power from signal generator 1 at the test board input
P_2	maximum available power from signal generator 2 at the test board input
P_3	maximum available power from signal generator 3 at the test board input
$P_{i(ref)}$	maximum available power at the test board input to give a Bit Error Rate (BER) ≤ $^3/_{100}$ for the modulated test signal 1, in the absence of interfering signals and under the conditions as specified in Chapters "AC characteristics (173 MHz)", "AC characteristics (470 MHz)" and "AC characteristics (930 MHz)"

Table 6 AC test conditions; notes 1 and 2

SYMBOL	PARAMETER	CONDITIONS	TEST SIGNALS
α_a	adjacent channel selectivity; Fig.11(b)	$f_2 = f_1 \pm \Delta f_{CS}$	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{a(min)}$
α_c	co-channel rejection; Fig.11(b)	$f_2 = f_1 \pm$ up to 3 kHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 - \alpha_{c(max)}$
α_{sp}	spurious immunity; Fig.11(b)	f_2 = 100 kHz to 2 GHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{sp(min)}$
α_{im}	intermodulation immunity; Fig.11(c)	$f_2 = f_1 \pm \Delta f_{cs}$; $f_3 = f_1 \pm 2\Delta f_{cs}$	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: unmodulated	$P_2 = P_1 + \alpha_{im(min)}$
		generator 3: modulated test signal 2	$P_3 = P_2$
α_{bl}	blocking immunity; Fig.11(b)	$f_2 = f_1 \pm 1$ MHz	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
		generator 2: modulated test signal 2	$P_2 = P_1 + \alpha_{bl(min)}$
f_{offset}	frequency offset range; Fig.11(a)	deviation = ±4.0 kHz, $f_1 = f_{i(RF)} \pm 2$ kHz ($f_{offset(min)}$)	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
Δf_{dev}	deviation range; Fig.11(a)	deviation = ±2.5 to ±7 kHz; ($\Delta f_{dev(min)}$ to $\Delta f_{dev(max)}$)	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 3$ dB
t_{on}	receiver turn-on time; Fig.11(a)	note 3	
		generator 1: modulated test signal 1	$P_1 = P_{i(ref)} + 10$ dB

Notes

1. The tests are executed without load on pins TPI and TPQ.
2. All minimum and maximum values correspond to a bit error rate (BER) ≤ $^3/_{100}$ in the wanted signal (P_1).
3. The BER measurement is started 5 ms ($t_{on(max)}$) after V_{RE} goes HIGH; BER is then measured for 100 bits (BER ≤ $^3/_{100}$).



(a) One generator.
(b) Two generators.
(c) Three generators.
(1) See Fig.12.

Fig.11 Test configurations.

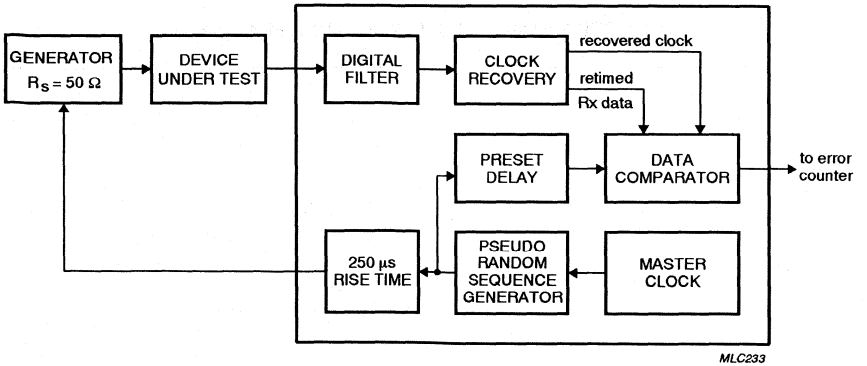


Fig.12 BER test facility.

PRINTED-CIRCUIT BOARDS

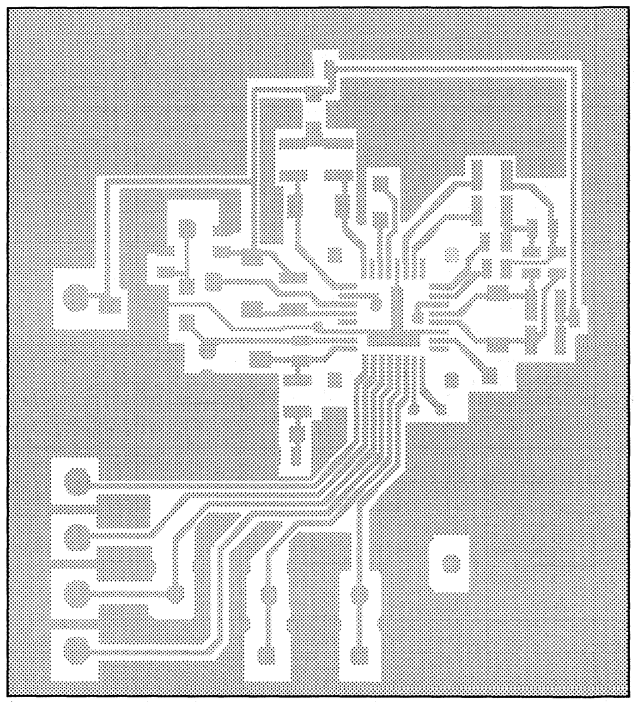


Fig.13 PCB top view for LQFP32; test circuit Figs 1 and 3.

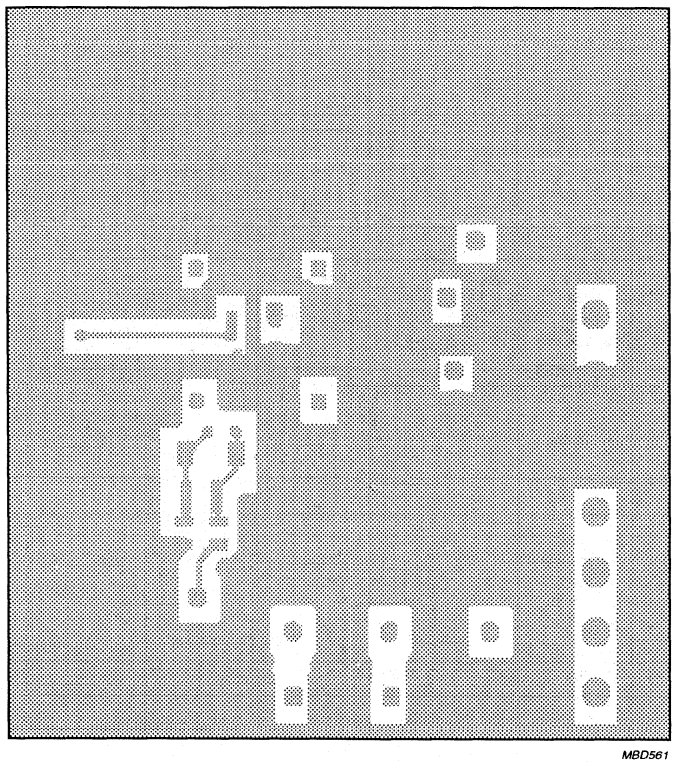
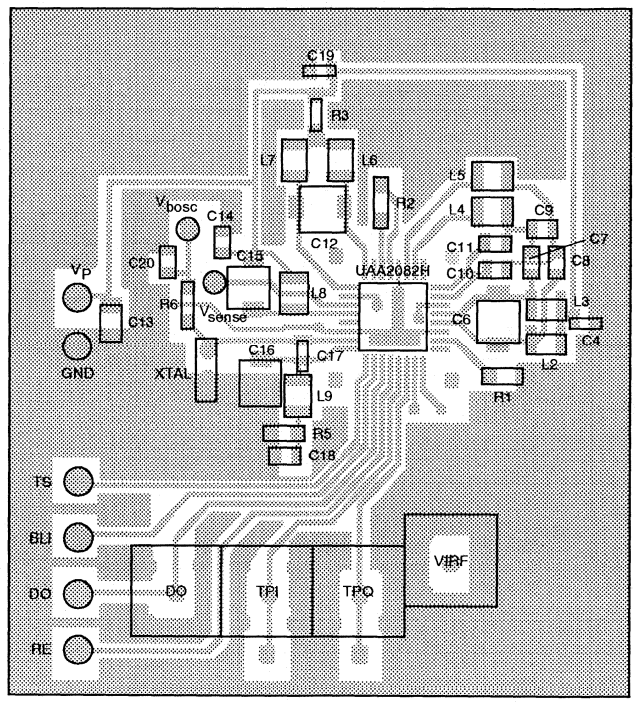


Fig.14 PCB bottom view for LQFP32; test circuit Figs 1 and 3.



V_{EE} = GND; V_C = V_P.

Fig.15 PCB top view with components for LQFP32; test circuit Fig.3.

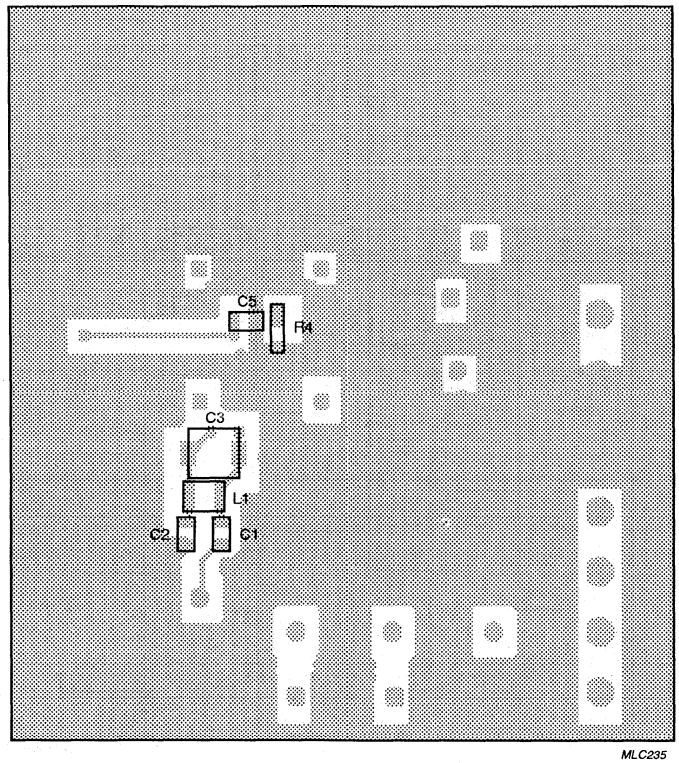


Fig.16 PCB bottom view with components for LQFP32; test circuit Fig.3.

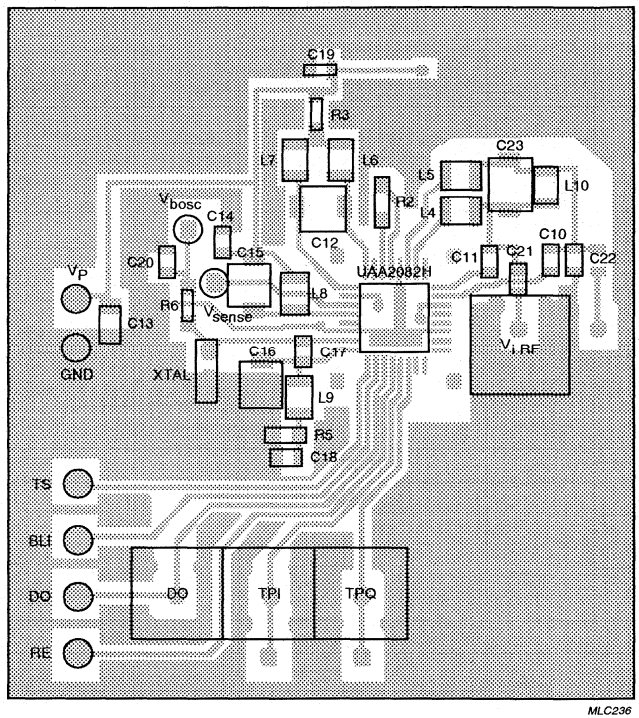


Fig.17 PCB top view with components for LQFP32; test circuit Fig.5.

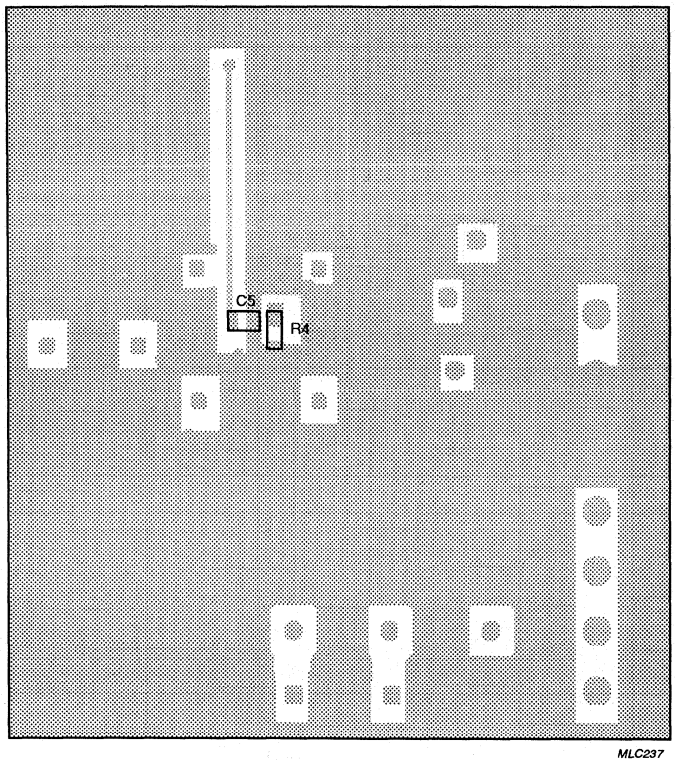


Fig.18 PCB bottom view with components for LQFP32; test circuit Fig.5.

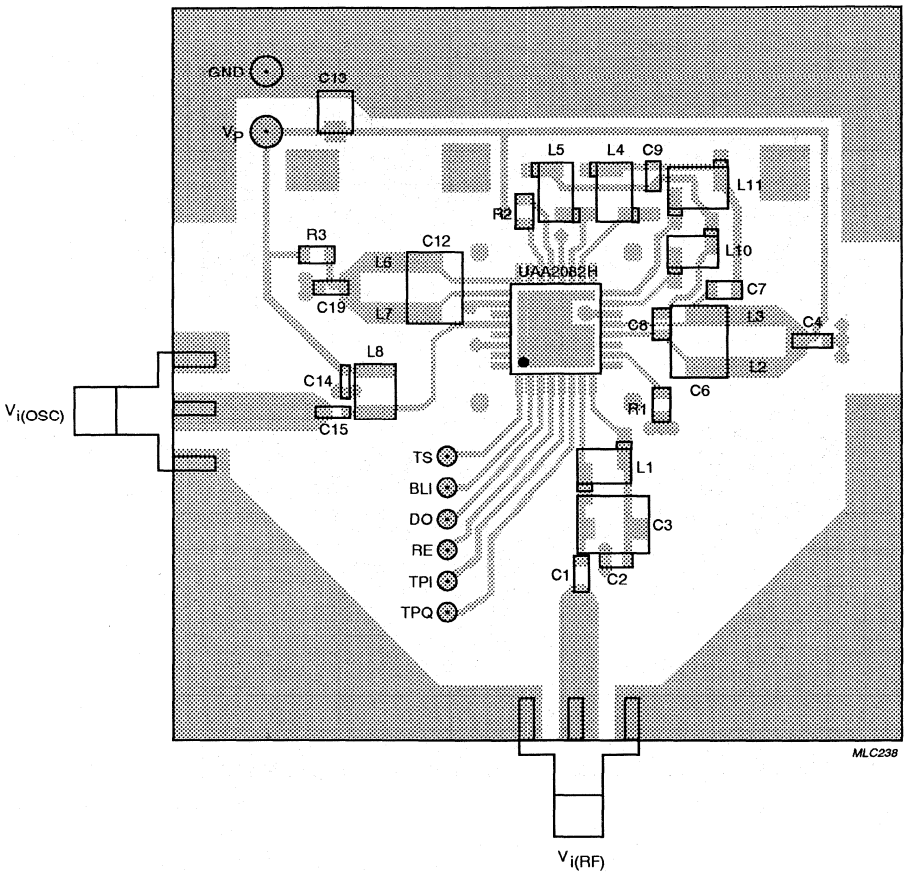


Fig.19 PCB top view with components for LQFP32; test circuit Fig.6.

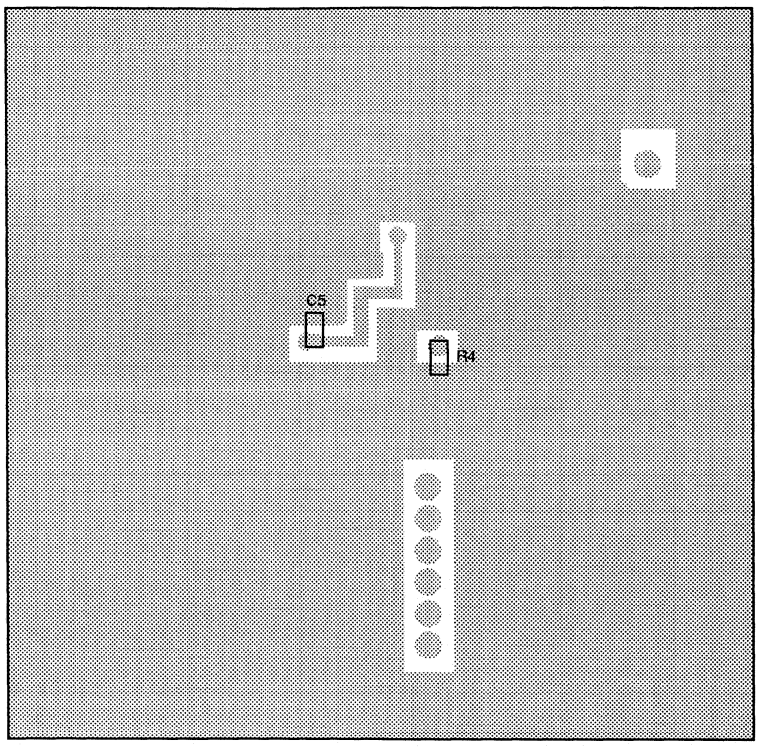


Fig.20 PCB bottom view with components for LQFP32; test circuit Fig.6.

Section 5
Amplifiers

Wireless Communications

	RF Amplifier Selector Guide	5–2
NE/SA5200	RF dual gain-stage	5–3
NE/SA5204A	Wide-band high-frequency amplifier	5–14
NE/SA/SE5205A	Wide-band high-frequency amplifier	5–24
NE/SA5209	Wideband variable gain amplifier	5–34
NE/SA5219	Wideband variable gain amplifier	5–47
TDA8780M	True logarithmic amplifier	5–60

RF Amplifier Family Overview

	NE/SA5200	NE/SA5204A	NE/SA5205A	NE/SA5209	NE/SA5219
Description	**Dual Gain Stage**	**Wideband Amp**	**Wideband Amp**	**Variable Gain Amp**	**Variable Gain Amp**
V_{cc}	4 – 9V	5 – 8V	5 – 8V	4.5 – 7.0V	4.5 – 7.0V
I_{cc}	4.2mA/95μA*@5V (per amplifier)	25mA @ 6V	25mA @ 6V	43mA @ 5V	43mA @ 5V
Bandwidth (3dB)	DC - 1.2GHz	DC - 350MHz	DC - 550MHz	DC - 850MHz	700MHz
Gain (power)	7.5dB/–13.5dB* (per amplifier)	19dB	19dB	25dB (voltage)	25dB (voltage)
Noise Figure	3.6dB	6.0 dB 50Ω 4.8 dB 75Ω	6.0 dB 50Ω 4.8 dB 75Ω	9.3dB	9.3dB
1dB Compression	+3.2dBm	+4dBm	+4dBm	–3dBm	–3dBm
3rd Order Intercept (input)	–1.8dBm	–2dBm	–2dBm	+13dBm (output)	+13dBm (output)
Input Impedance	50Ω	50Ω	50Ω	1.2kΩ	1.2kΩ
Output Impedance	50Ω	50Ω	50Ω	60Ω	60Ω
Package	SO8	DIP8 SO8	DIP8 SO8	DIP16 SO16	DIP16 SO16
Features	+DC to 1.2GHz operation +Power-Down mode	+DC to 350MHz operation	+DC to 550MHz operation	+DC to 850MHz operation +Gain control pin	+DC to 700MHz operation +Gain control pin

*Amplifier: Enabled/Disabled

RF dual gain-stage | NE/SA5200

DESCRIPTION

The NE/SA5200 is a dual amplifier with DC to 1200MHz response. Low noise (NF = 3.6dB) makes this part ideal for RF front-ends, and a simple power-down mode saves current for battery operated equipment. Inputs and outputs are matched to 50Ω.

The enable pin allows the designer the ability to turn the amplifiers on or off, allowing the part to act as an amplifier as well as an attenuator. This is very useful for front-end buffering in receiver applications.

FEATURES

- Dual amplifiers
- DC - 1200MHz operation
- Low DC power consumption (4.2mA per amplifier @ V_{CC} = 5V)
- Power-Down Mode (I_{CC} = 95μA typical)
- 3.6dB noise figure at 900MHz
- Unconditionally stable
- Fully ESD protected
- Low cost

PIN CONFIGURATION

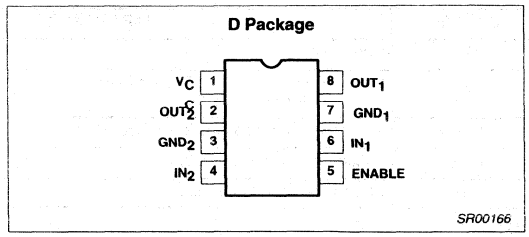


Figure 1. Pin Configuration

- Supply voltage 4-9V
- Gain S_{21} = 7dB at f = 1GHz
- Input and output match S_{11}, S_{22} typically <–14dB

APPLICATIONS

- Cellular radios
- RF IF strips
- Portable equipment

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (Surface–mount)	0-70°C	NE5200D	SOT96-1
8-Pin Plastic Small Outline (Surface–mount)	–40-+85°C	SA5200D	SOT96-1

BLOCK DIAGRAM

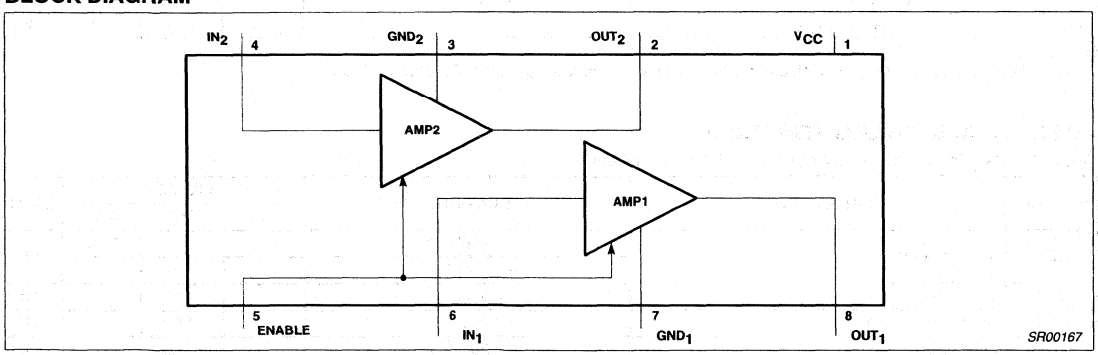


Figure 2. Block Diagram

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.0 to 9.0	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.5 to +9	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 8-Pin Plastic SO	780	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 10.5V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin SO: θ_{JA} = 158°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4	5.0	9.0	V
I_{CC}	Total supply current	V_{CC} = 5V, ENABLE = High	6.4	8.4	10.4	mA
		V_{CC} = 5V, ENABLE = Low		95	255	µA
		V_{CC} = 9V, ENABLE = High		17.8	22.2	mA
		V_{CC} = 9V, ENABLE = Low		320	960	µA
V_T	TTL/CMOS logic threshold voltage[1]			1.25		V
V_{IH}	Logic 1 level	Power-up mode	2.0		V_{CC}	V
V_{IL}	Logic 0 level	Power-down mode	-0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	µA
$V_{IDC,ODC}$	Input and output DC levels		0.6	0.83	1.0	V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the NE/SA5200.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = +5V, T_A = 25°C, either amplifier, enable = 5V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S21	Insertion gain	f = 100MHz	9.2	11	13.2	dB
		f = 900MHz	5.2	7.5		
S22	Output return loss	f = 900MHz		–14.3		dB
S12	Reverse isolation	f = 900MHz		–17.9		dB
S11	Input return loss	f = 900MHz		–16.5		dB
P-1	Output 1dB compression point	f = 900MHz		–4.3		dBm
NF	Noise figure in 50Ω	f = 900MHz		3.6		dB
IP_2	Input second-order intercept point	f = 900MHz		+4.3		dBm
IP_3	Input third-order intercept point	f = 900MHz		–1.8		dBm
ISOL	Amplifier-to-amplifier isolation[2]	f = 900MHz		–25		dB
P_{OUT}	Saturated output power	f = 900MHz		–1.7		dBm
S21	Insertion gain when disabled	f = 100MHz		–13		dB
		f = 900MHz		–13.5		

NOTE:
1. All measurements include the effects of the NE/SA5200 Evaluation Board (see Figure 4). Measurement system impedance is 50Ω.
2. Input applied to one amplifier, output taken at the other output. All ports terminated into 50Ω.

APPLICATIONS

NE/SA5200 is a user-friendly, wide-band, unconditionally stable, low power dual gain amplifier circuit. There are several advantages to using the NE/SA5200 as a high frequency gain block instead of a discrete implementation. First is the simplicity of use. The NE/SA5200 does not need any external biasing components. Due to the higher level of integration and small footprint (SO8) package it occupies less space on the printed circuit board and reduces the manufacturing cost of the system. Also the higher level of integration improves the reliability of the amplifier over a discrete implementation with several components. The power down mode in the NE/SA5200 helps reduce power consumption in applications where the amplifiers can be disabled. And last but not the least is the impedance matching at inputs and outputs. Only those who have toiled through discrete transistor implementations for 50Ω input and output impedance matching can truly appreciate the elegance and simplicity of the NE/SA5200 input and output impedance matching to 50Ω.

A simplified equivalent schematic is shown in 3. Each amplifier is composed of an NPN transistor with an Ft of 13GHz in a classical series-shunt feedback configuration. The two wideband amplifiers are biased from the same bias generator. In normal operation each amplifier consumes about 4mA of quiescent current (at V_{CC} = 5V). In the disable mode the device consumes about 90μA of current, most of it is in the TTL enable buffer and the bias generator. The input impedance of the amplifiers is 50Ω. The amplifiers have typical gain of 11dB at 100MHz and 7dB of gain at 1.2GHz.

It can be seen from 3 that any inductance between Pin 7, 3 and the ground plane will reduce the gain of the amplifiers at higher frequencies. Thus proper grounding of Pins 7 and 3 is essential for maximum gain and increased frequency response. 4 shows the printed circuit board layout and the component placement for the NE/SA5200 evaluation board. The AC coupling capacitors should be selected such that at they are shorts at the desired frequency of operation. Since most low-cost large value surface mount capacitors cease to be simply capacitors in the UHF range and exhibit an inductive behavior, it is recommended that high frequency chip capacitors be utilized in the circuit. A good power supply bypass is also essential for the performance of the amplifier and should be as close to the device as practical.

5 shows the typical frequency response of the two channels of NE/SA5200. The low frequency gain is about 11dB at 100MHz and slowly drops off to 10dB at 500MHz. The gain is about 8dB at 900MHz and 7dB at 1.2 GHz which is typical of NE/SA5200 with a good printed circuit board layout. It can also be seen that both channels have a very well matched frequency response and matched gain to within 0.1dB at 100MHz and 0.2dB at 900MHz.

NE/SA5200 finds applications in many areas of RF communications. It is an ideal gain block for high performance, low cost, low power RF communications transceivers. A typical radio transceiver front-end is shown in 6. This could be the front-end of a cellular phone, a VHF/ UHF hand-held transceiver, UHF cordless telephone or a spread spectrum system. The NE/SA5200 can be used in the receiver path of most systems as an LNA and pre-amplifier. The bandpass filter between the two amplifiers also minimize the noise into the first mixer. In the transmitter path, NE/SA5200 can be used as a buffer to the VCO and isolate the VCO from any load variations due to the power level changes in the power amplifier. This improves the stability of the VCOs. The NE/SA5200 can also be used as a pre-driver to the power amplifier modules.

The two amplifiers in NE/SA5200 can be easily cascaded to have a 13dB gain block at 900MHz. At 100MHz the gain will be 22dB and a noise figure of about 5.5dB. The NE/SA5200 can be operated at a higher voltage up to 9V for much improved 1dB output compression point and higher 3rd order intercept point.

Several stages of NE/SA5200 can also be cascaded and be used as an IF amplifier strip for DBS/TV/GPS receivers. 7 shows a 60dB gain IF strip at 180MHz. The noise figure for the cascaded amplifier chain is given by equation 1.

NF (total) = NF1 + NF2/G1 + NF3/G1*G2 + NF4/G1*G2*G3 + ... (Equation. 1)

NOTE: The noise figure and gain should not be in dB in the above equation.

Since the noise figure for each stage is about 3.6dB and the gain is about 11dB, the noise figure for the 60dB gain IF strip will be about 6.4dB.

In applications where a single amplifier is required with a 7.5dB gain at 900MHz and current consumption is of paramount importance (battery powered receivers), the amplifier A1 can be used and amplifier A2 can be disabled by leaving GND2 (Pin 3) unconnected. This will reduce the total current consumption for the IC to a meager 4mA.

The ENABLE pin is useful for Time-Division-Duplex systems where the receiver can be disabled for a period of time. In this case the overall system supply current will be decreased by 8mA.

The ENABLE pin can also be used to improve the system dynamic range. For input levels that are extremely high, the NE/SA5200 can be disabled. In this case the input signal is attenuated by 13dB. This prevents the system from being overloaded as well as improves the system's overall dynamic range. In the disabled condition the NE/SA5200 IP_3 increases to nearly +20dBm.

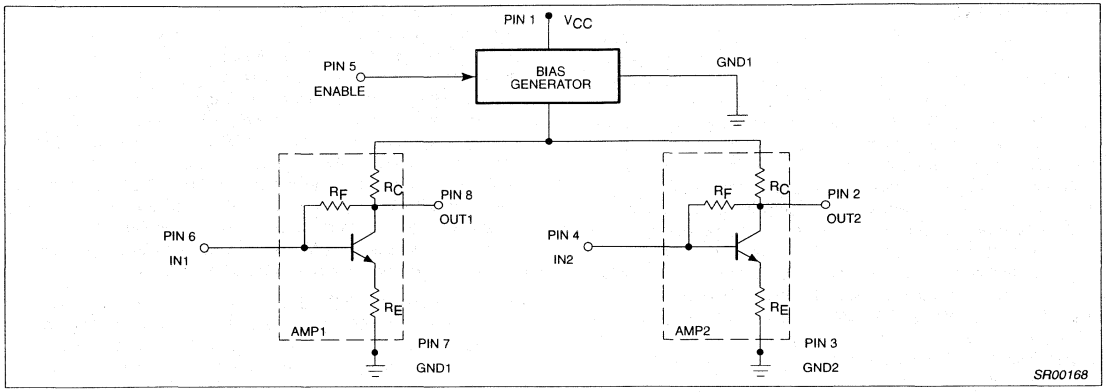


Figure 3. Simplified Equivalent Schematic of NE/SA5200

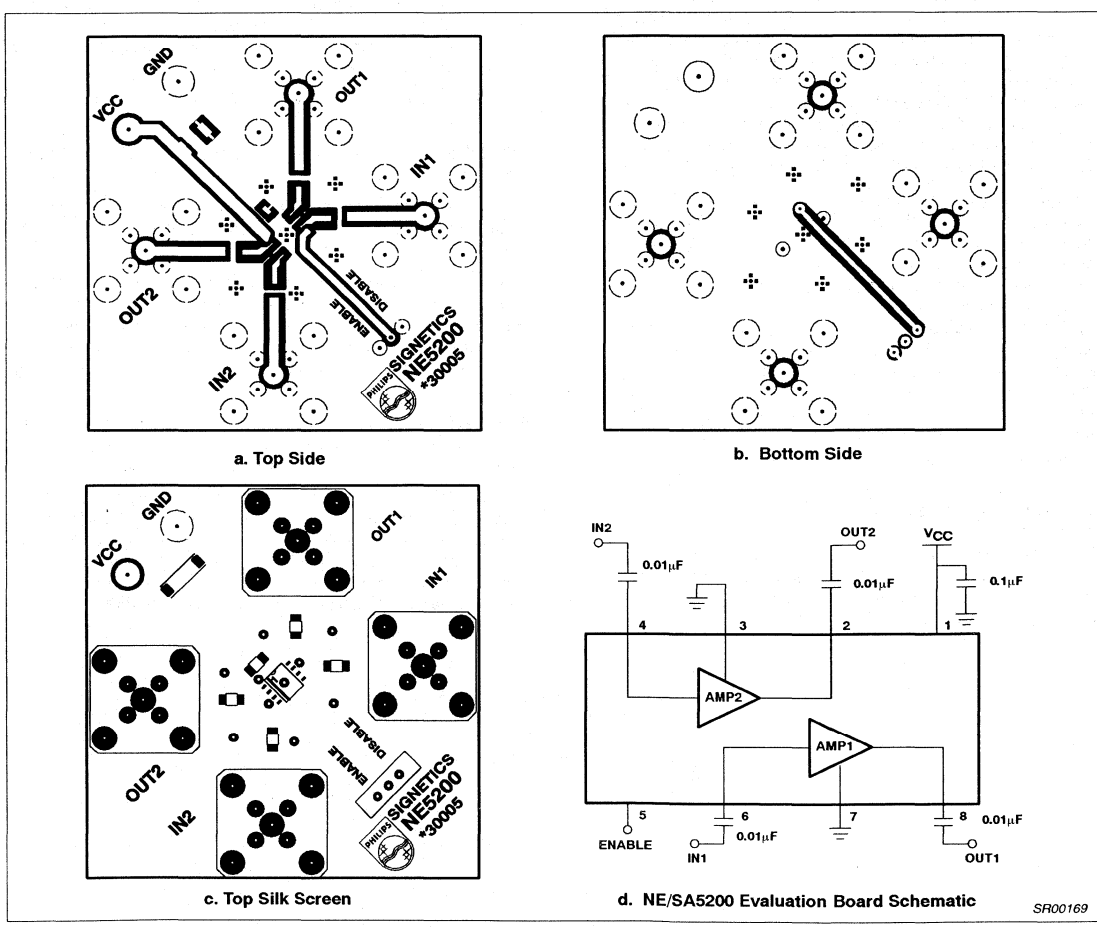


Figure 4. Printed Circuit Board Layout of the NE/SA5200 Evaluation Board

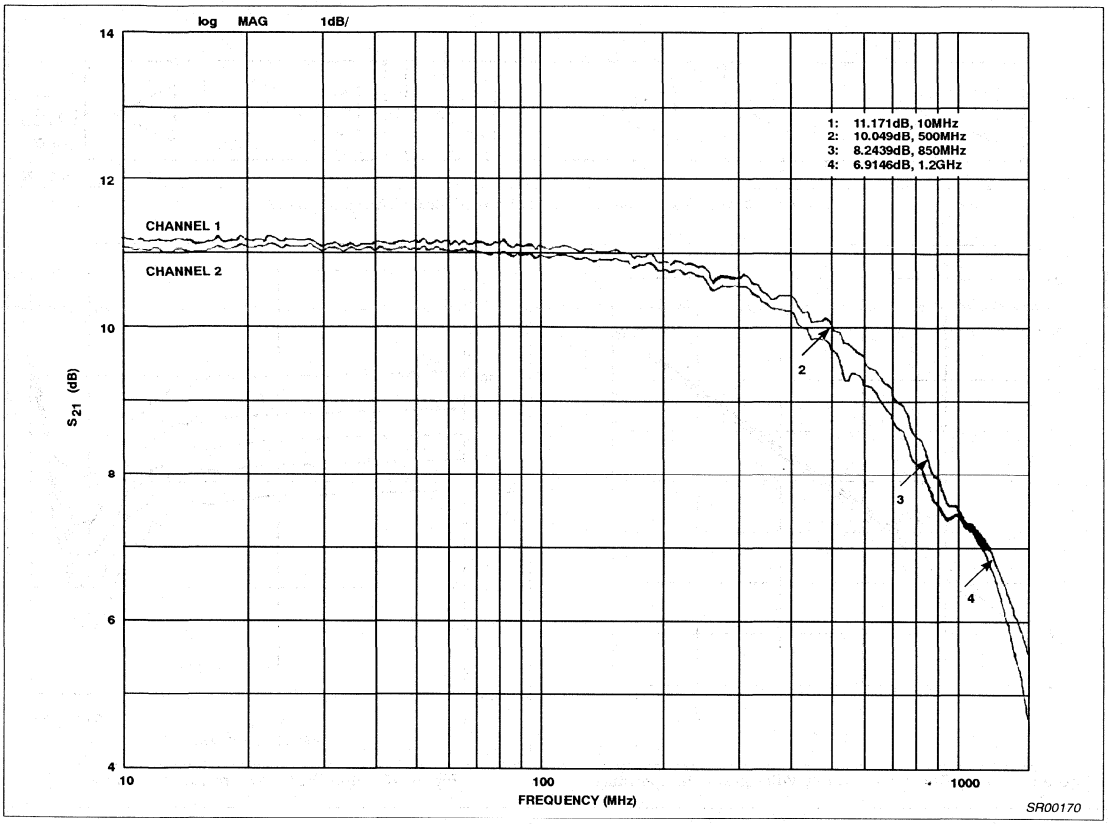


Figure 5. Typical Frequency Response of NE/SA5200 in a 50Ω System

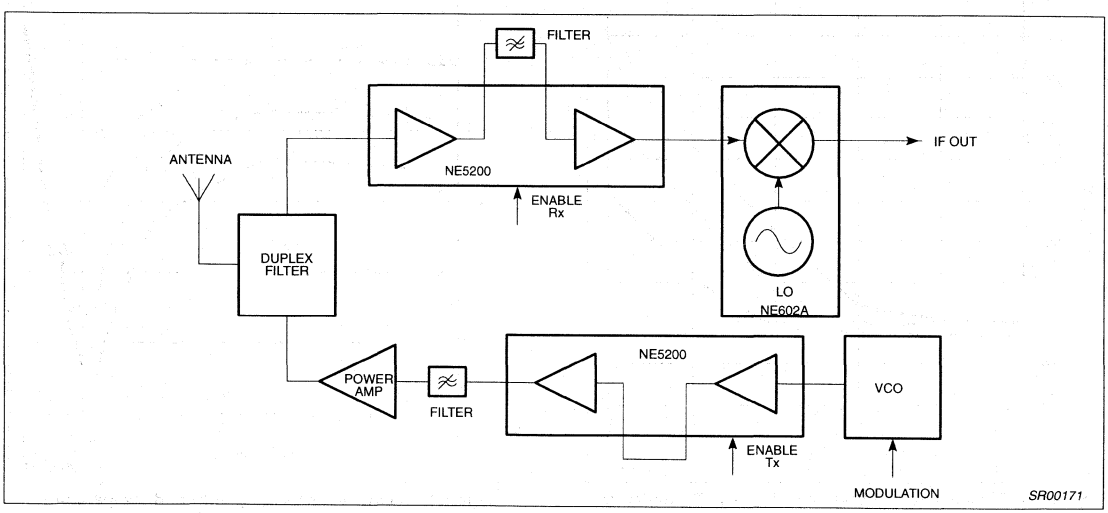


Figure 6. Typical Radio Transceiver Front-End

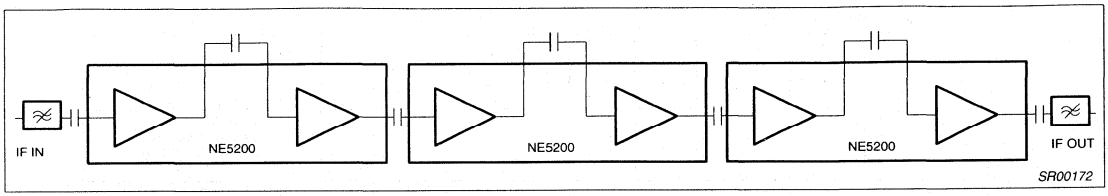


Figure 7. 60dB IF Gain Block for 100-300MHz IF for GPS/DBS Systems

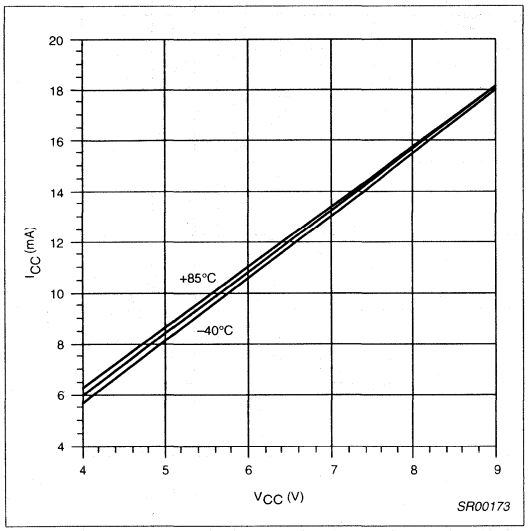


Figure 8. Supply Current vs Supply Voltage and Temperature

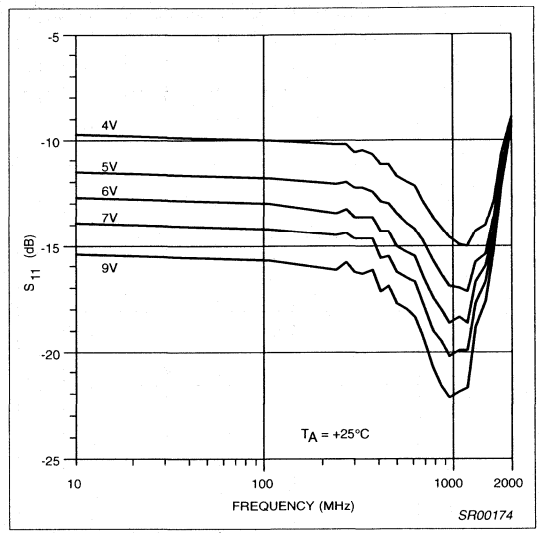


Figure 10. Input Match vs Frequency and V_{CC}

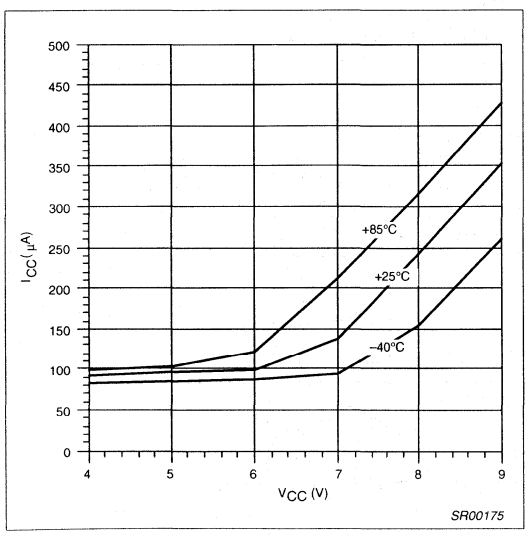


Figure 9. Disabled Supply Current vs V_{CC} and Temperature

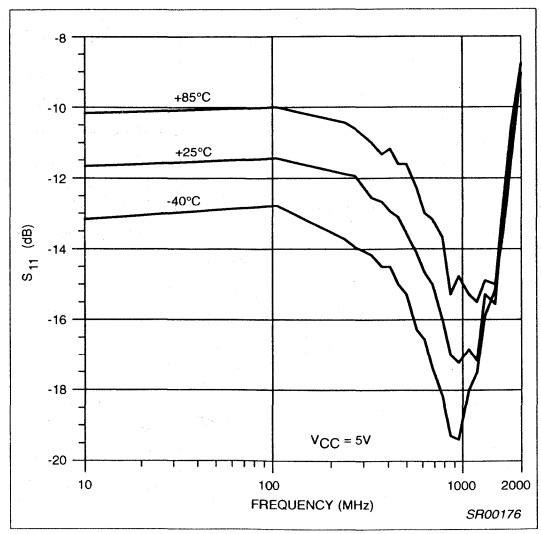


Figure 11. Input Match vs Frequency and Temperature

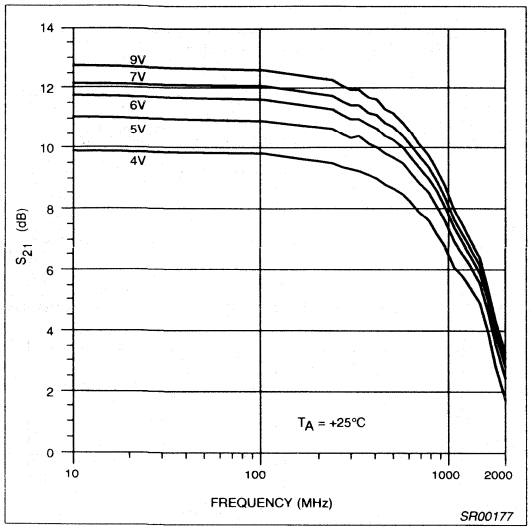


Figure 12. Insertion Gain vs Frequency and V_{CC}

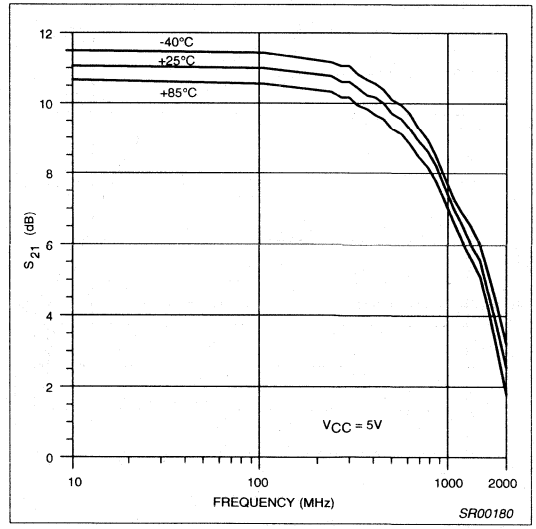


Figure 14. Insertion Gain vs Frequency and Temperature

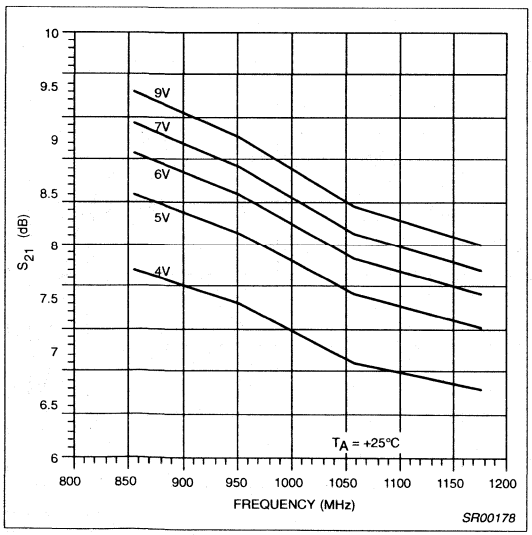


Figure 13. Insertion Gain vs Frequency and V_{CC} — Expanded Detail —

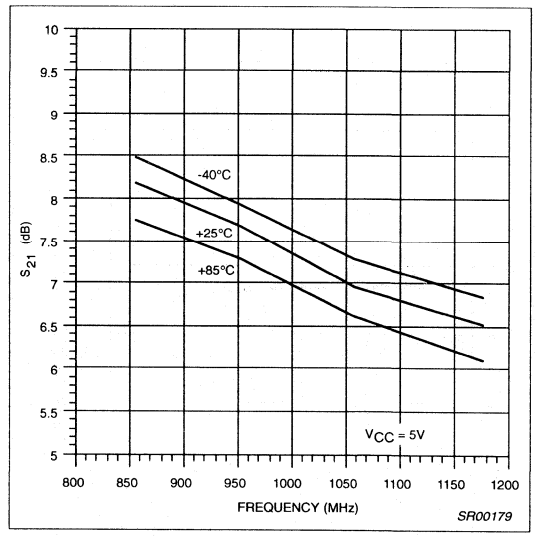


Figure 15. Insertion Gain vs Frequency and Temperature – Expanded Detail –

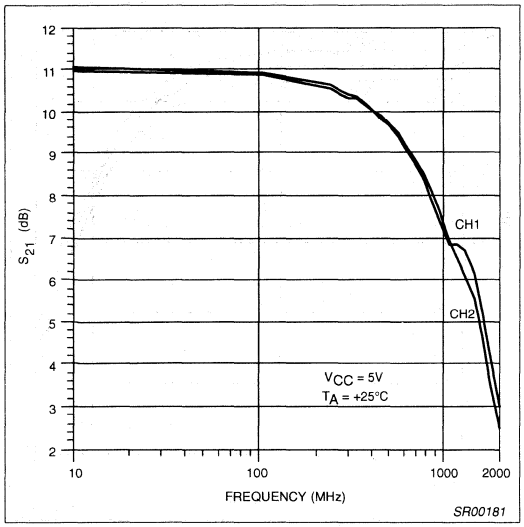


Figure 16. Insertion Gain Matching (CH1 vs CH2) vs Frequency

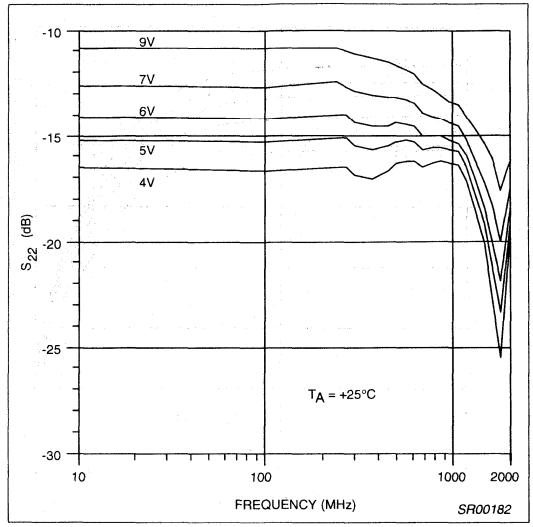


Figure 18. Output Match vs Frequency and V_{CC}

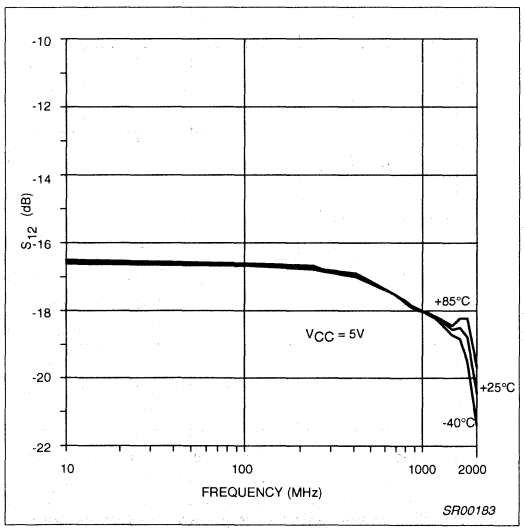


Figure 17. Reverse Insertion Gain vs Frequency and Temperature

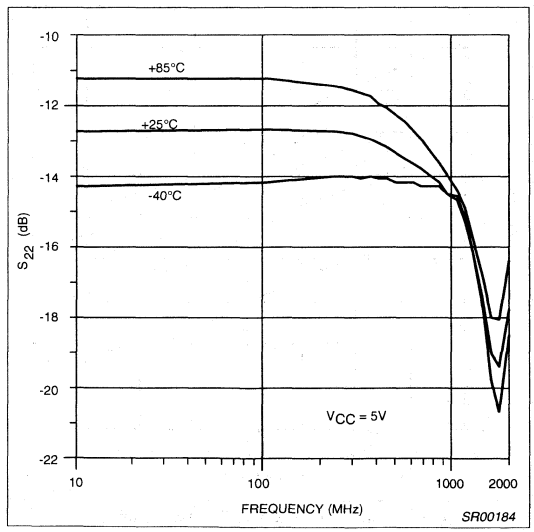


Figure 19. Output Match vs Frequency and Temperature

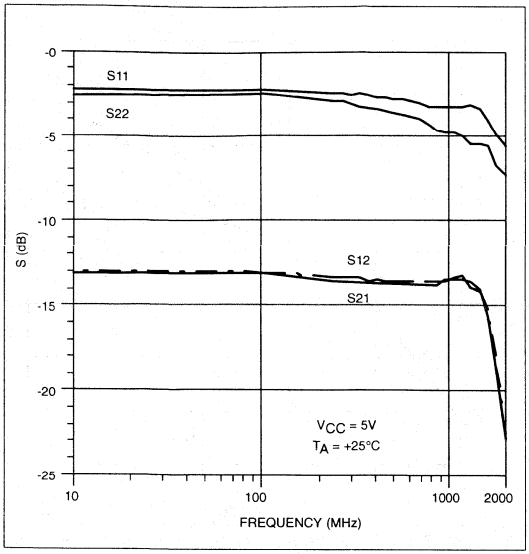


Figure 20. S-parameters vs Frequency for Disabled Amplifier

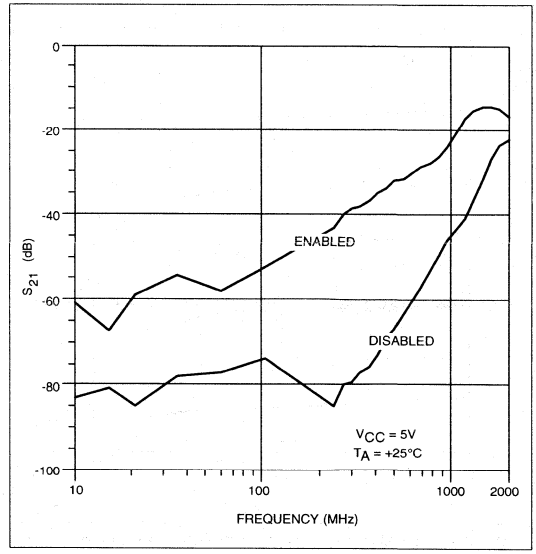


Figure 22. CH1 Input to CH2 Output Isolation vs Frequency

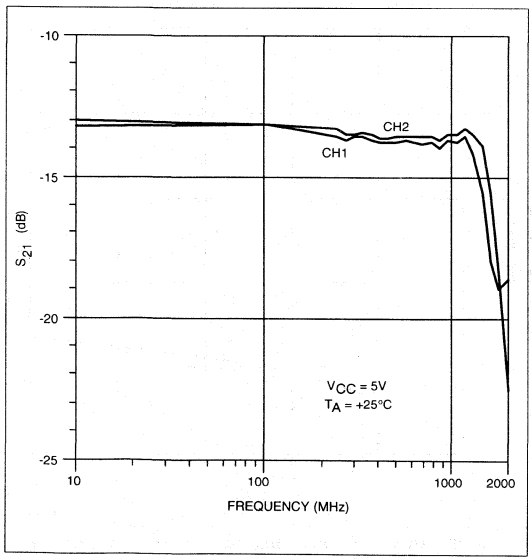


Figure 21. Insertion Gain Matching Disabled (CH1 vs CH2) vs Frequency

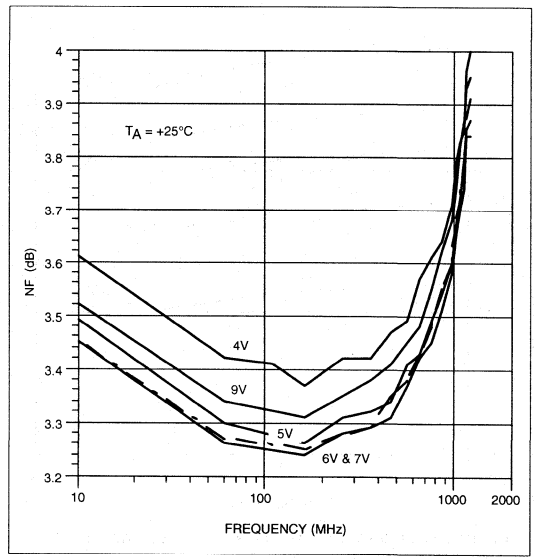


Figure 23. Noise Figure vs Frequency and V_{CC} in a 50Ω System

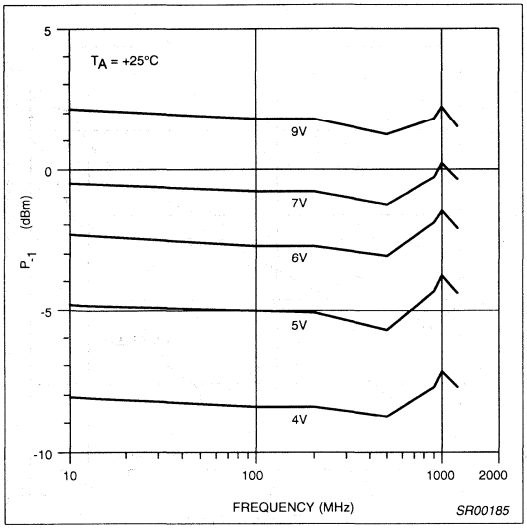


Figure 24. 1dB Output Compression Point vs Frequency and V_{CC}

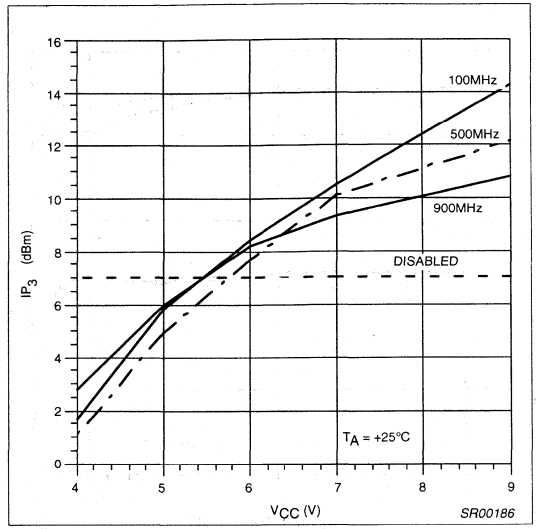


Figure 26. Third-Order Output Intercept vs Frequency and V_{CC}

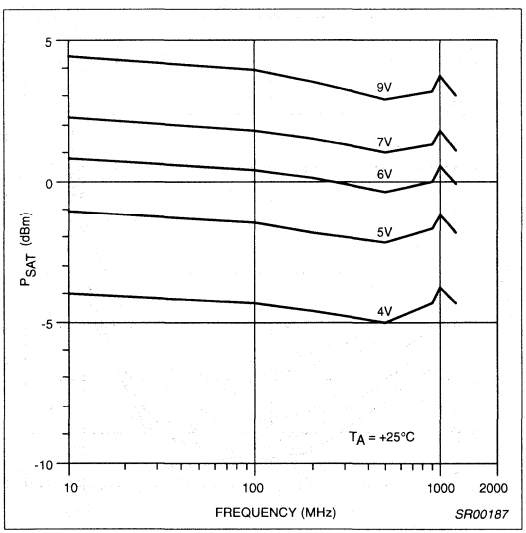


Figure 25. Saturated Output Power vs Frequency and V_{CC}

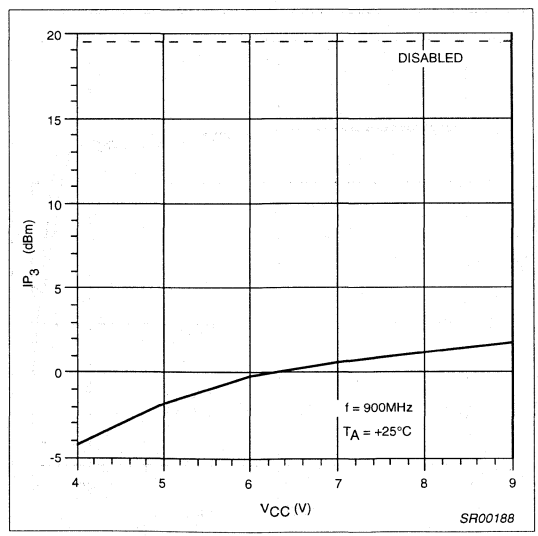


Figure 27. Third-Order Input Intercept vs Frequency and V_{CC}

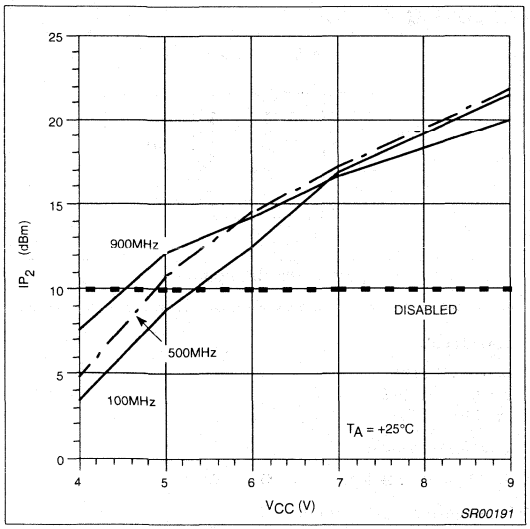


Figure 28. Second-Order Output Intercept vs Frequency and V_{CC}

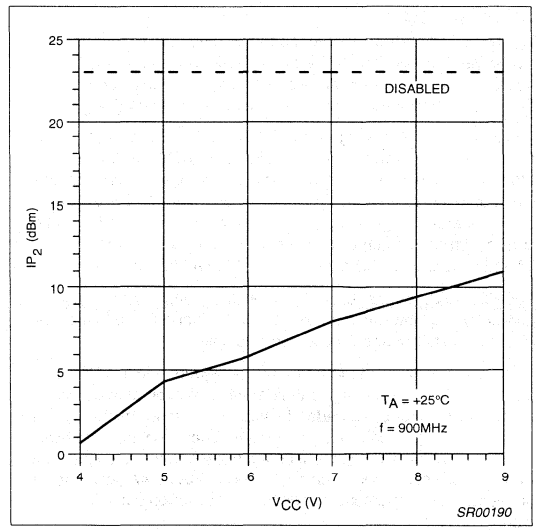


Figure 30. Second-Order Input Intercept vs Frequency and V_{CC}

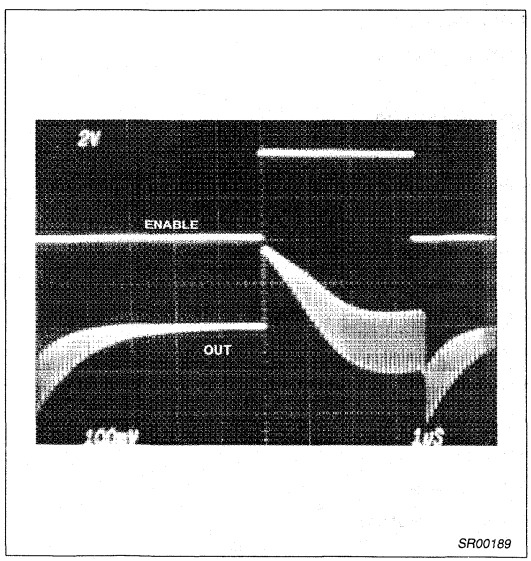


Figure 29. Switching Speed; f_{IN} = 10MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 0.01µF

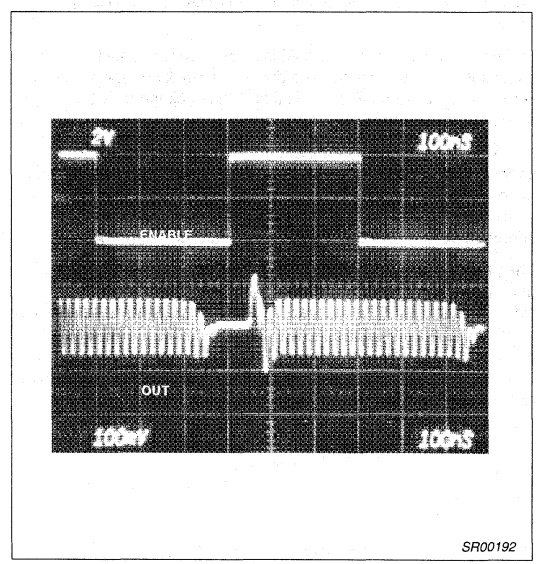


Figure 31. Switching Speed; f_{IN} = 50MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 100pF

Wide-band high-frequency amplifier NE/SA5204A

DESCRIPTION

The NE/SA5204A family of wideband amplifiers replaces the NE/SA5204 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nomically identical to the original parts.

The NE/SA5204A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The -3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204A operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204A is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204A solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC-coupling capacitors because the NE/SA5204A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204As in series as required, without any degradation in amplifier stability.

PIN CONFIGURATION

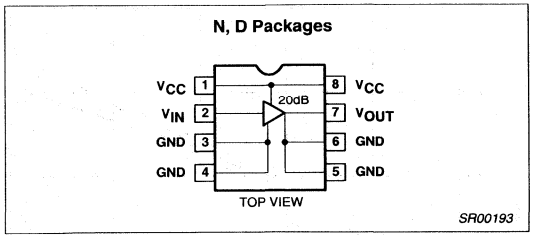


Figure 1. Pin Configuration

FEATURES

- Bandwidth (min.)
  200 MHz, ±0.5dB
  350 MHz, -3dB
- 20dB insertion gain
- 4.8dB (6dB) noise figure Z_O=75Ω (Z_O=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface-mount package available
- Cascadable
- 2000V ESD protection

APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Networks
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5204AN	SOT97-1
8-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5204AD	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	−40 to +85°C	SA5204AN	SOT97-1
8-Pin Plastic Small Outline (SO) package	−40 to +85°C	SA5204AD	SOT96-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	–40 to +85	°C
P_{DMAX}	Maximum power dissipation[1, 2] T_A=25°C(still–air)		
	N package	1160	mW
	D package	780	mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	–55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC

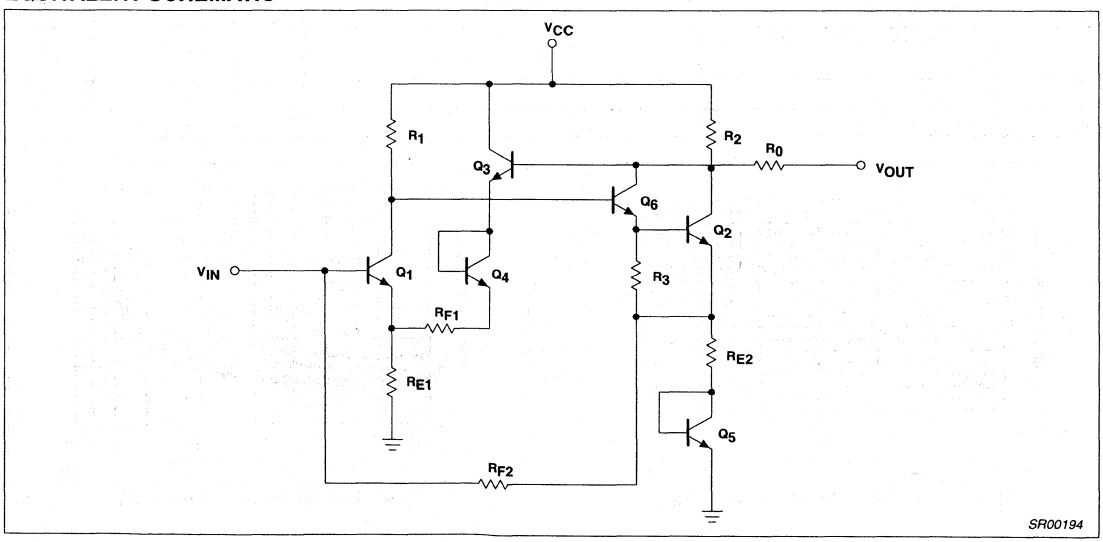


Figure 2. Equivalent Schematic

DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	25	33	mA
S21	Insertion gain	f=100MHz, over temperature	16	19	22	dB
S11	Input return loss	f=100MHz		25		dB
		DC –550MHz		12		
S22	Output return loss	f=100MHz		27		dB
		DC –550MHz		12		
S12	Isolation	f=100MHz		–25		dB
		DC –550MHz		–18		
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f=100MHz		4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0		dB
	Saturated output power	f=100MHz		+7.0		dBm
	1dB gain compression	f=100MHz		+4.0		dBm
	Third–order intermodulation intercept (output)	f=100MHz		+17		dBm
	Second–order intermodulation intercept (output)	f=100MHz		+24		dBm
t_R	Rise time			500		ps
t_P	Propagation delay			500		ps

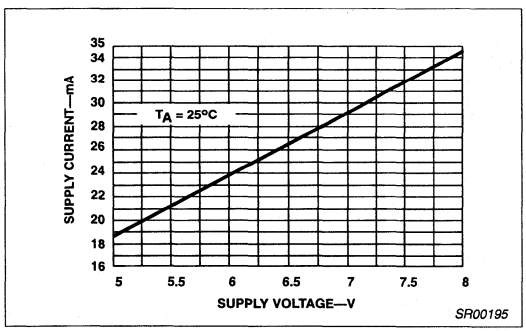


Figure 3. Supply Current vs Supply Voltage

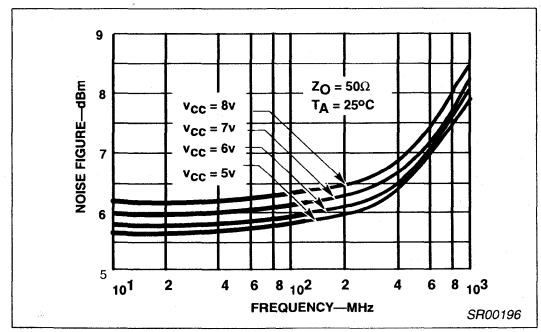


Figure 4. Noise Figure vs Frequency

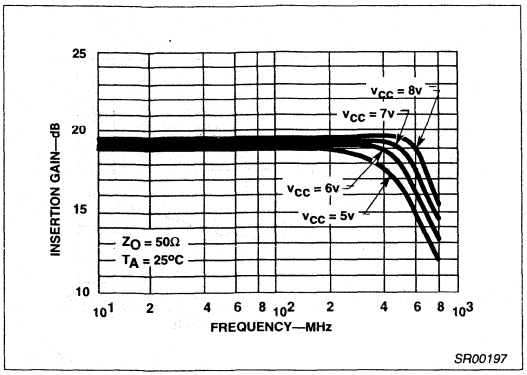


Figure 5. Insertion Gain vs Frequency (S_{21})

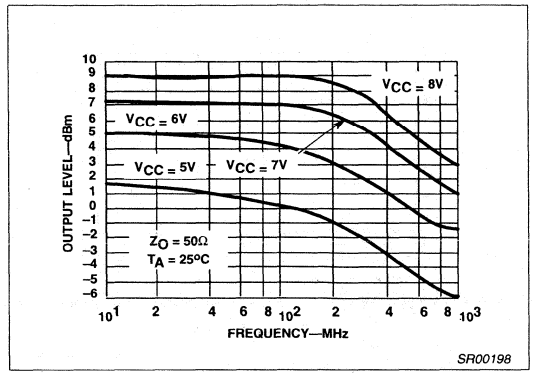


Figure 8. 1dB Gain Compression vs Frequency

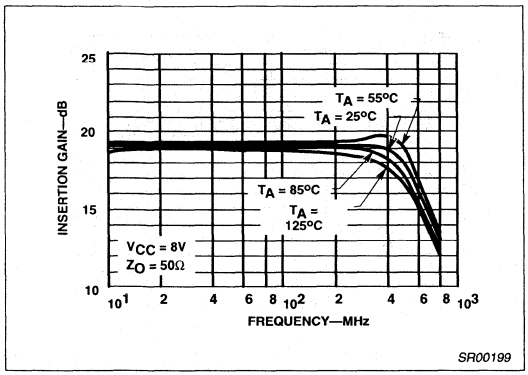


Figure 6. Insertion Gain vs Frequency (S_{21})

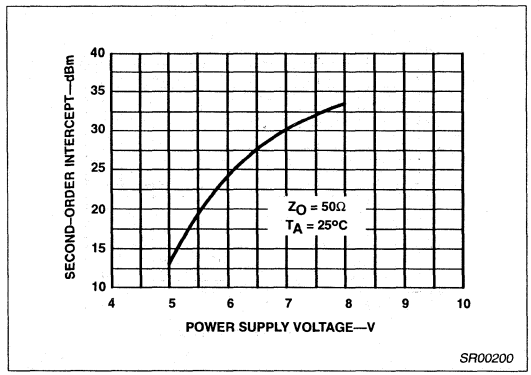


Figure 9. Second-Order Output Intercept vs Supply Voltage

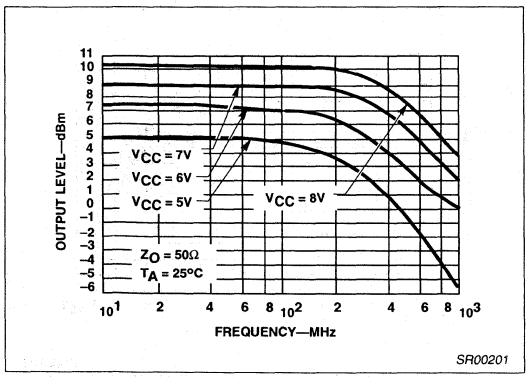


Figure 7. Saturated Output Power vs Frequency

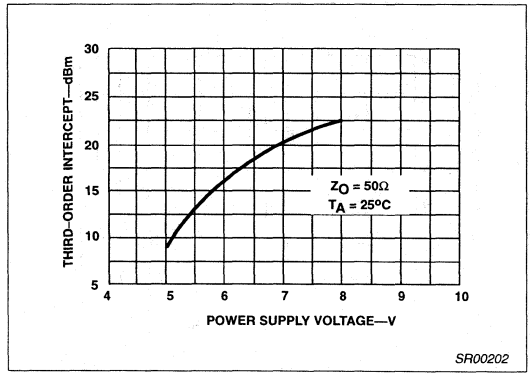


Figure 10. Third-Order Intercept vs Supply Voltage

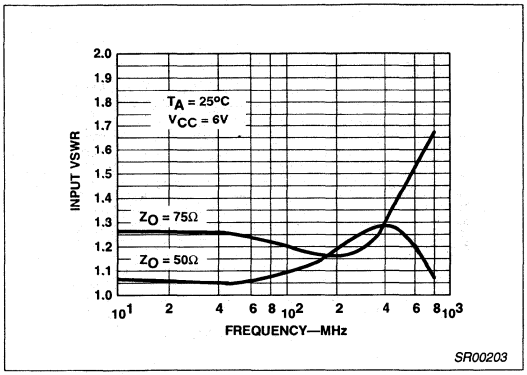


Figure 11. Input VSWR vs Frequency

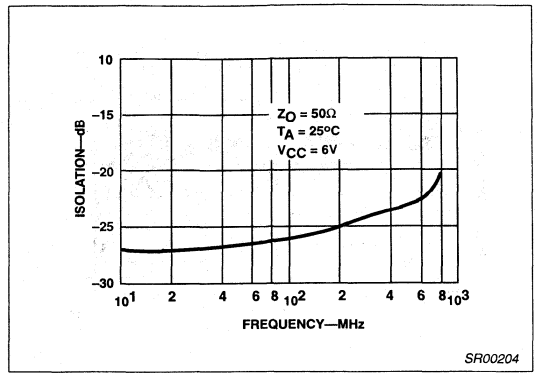


Figure 14. Isolation vs Frequency (S_{12})

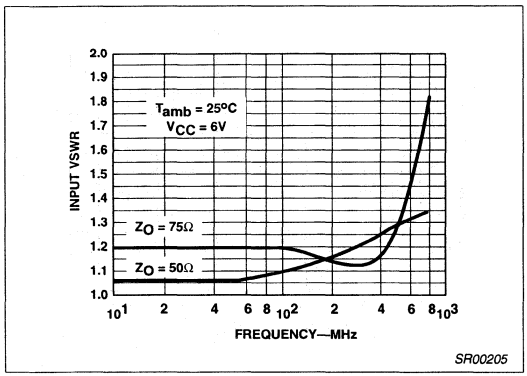


Figure 12. Output VSWR vs Frequency

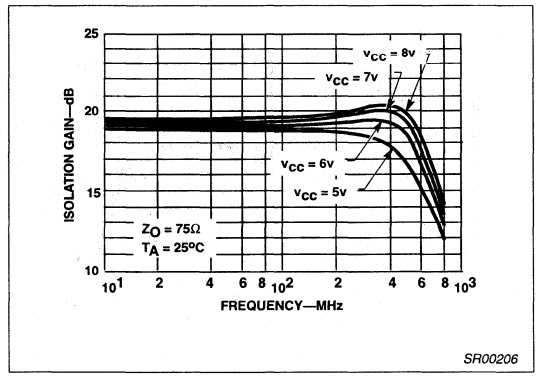


Figure 15. Insertion Gain vs Frequency (S_{21})

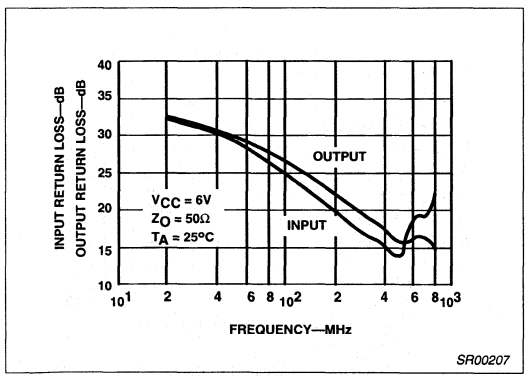


Figure 13. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

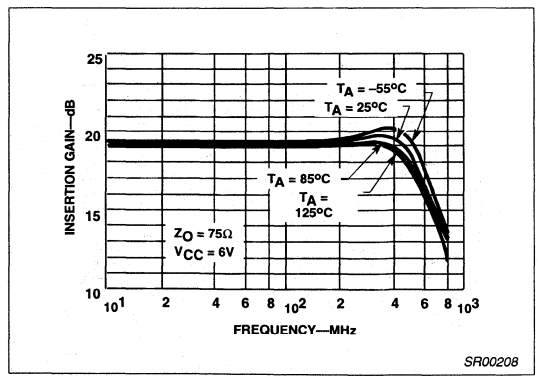


Figure 16. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 17, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1}) / R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\text{Log}\left(1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_O}\right) \text{ dB} \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1} \quad (3)$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2, \quad (4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here, it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA max). For operation at supply voltages other than 6V, see Figure 3 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

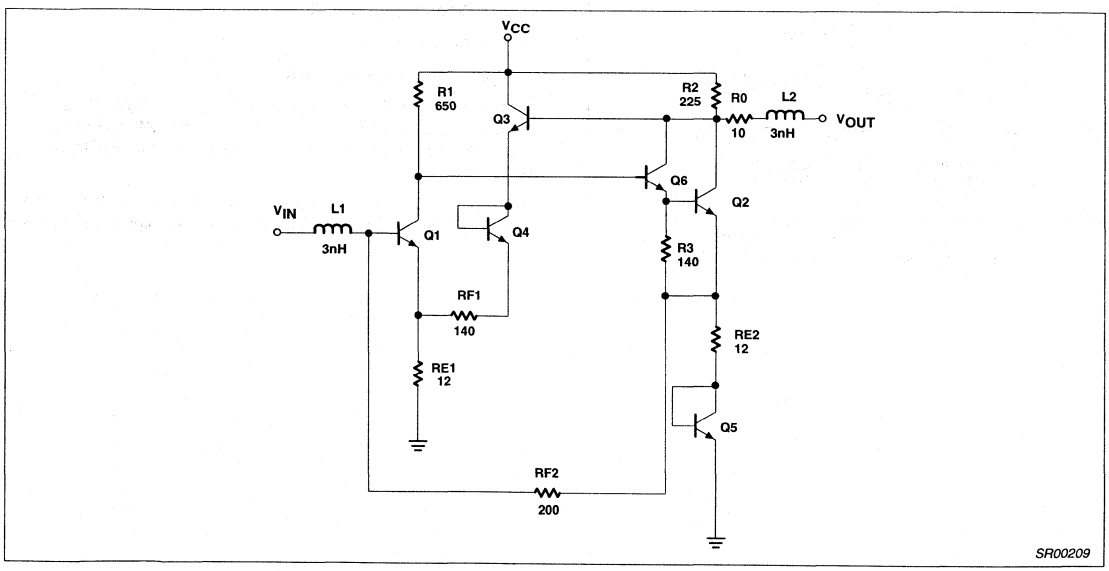


Figure 17. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 18. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE5204A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 19.

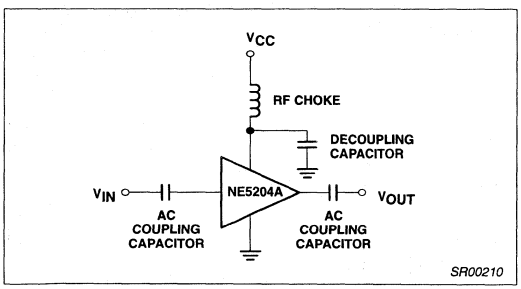
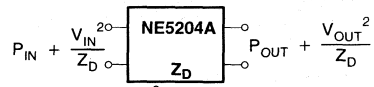


Figure 18. Circuit Schematic for Coupling and Power Supply Decoupling

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 20.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5204A to other high-frequency amplifiers.
The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the NE/SA/SE5204A



$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the
NE/SA/SE5204A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 21. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

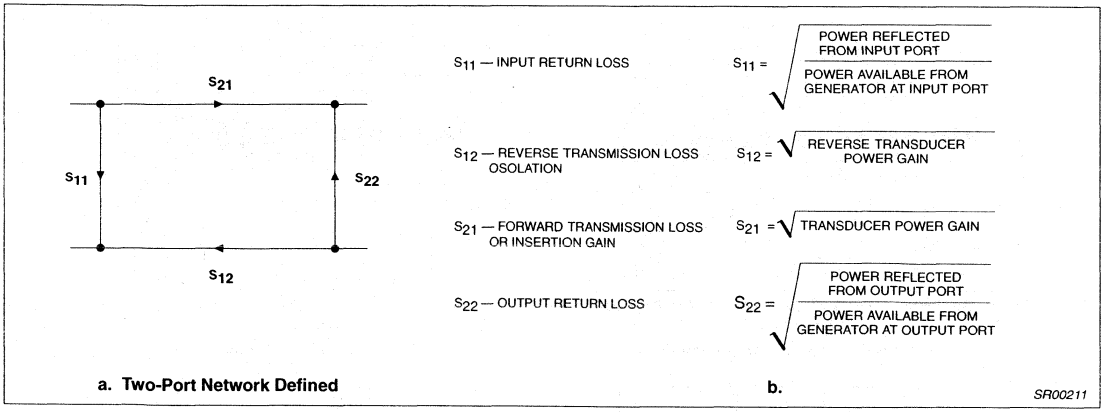

S21
S11
S22
S12
S11 — INPUT RETURN LOSS
S11 = √(POWER REFLECTED FROM INPUT PORT / POWER AVAILABLE FROM GENERATOR AT INPUT PORT)
S12 — REVERSE TRANSMISSION LOSS OSOLATION
S12 = √(REVERSE TRANSDUCER POWER GAIN)
S21 — FORWARD TRANSMISSION LOSS OR INSERTION GAIN
S21 = √(TRANSDUCER POWER GAIN)
S22 — OUTPUT RETURN LOSS
S22 = √(POWER REFLECTED FROM OUTPUT PORT / POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT)
a. Two-Port Network Defined
b.
SR00211

Figure 19.

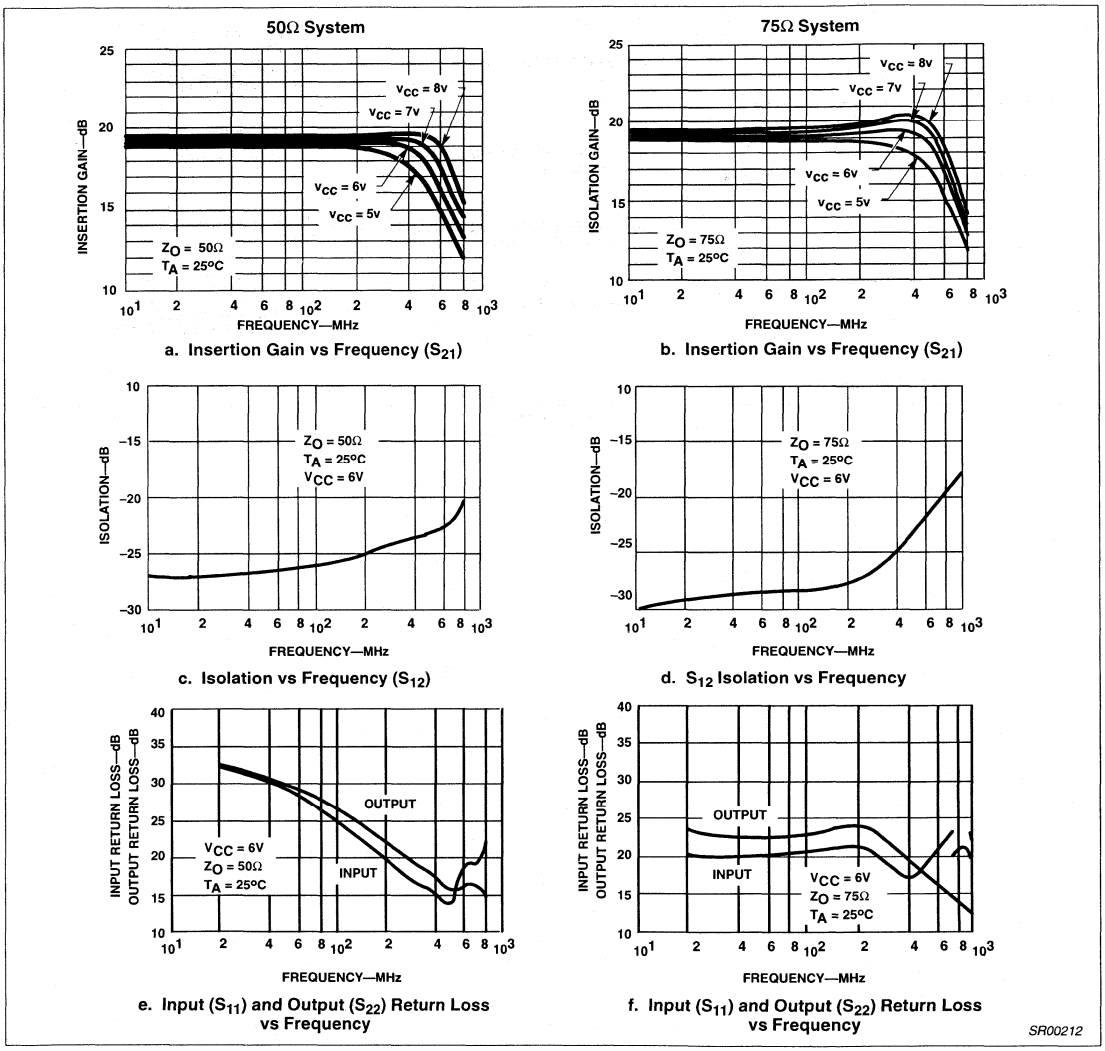


Figure 20.

INPUT RETURN LOSS=S_{11}dB
S_{11}dB=20 Log | S_{11} |

OUTPUT RETURN LOSS=S_{22}dB
S_{22}dB=20 Log | S_{22} |

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1DB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and

intermodulation ratio is illustrated in Figure 22, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA5204A we have chosen an output level of –10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

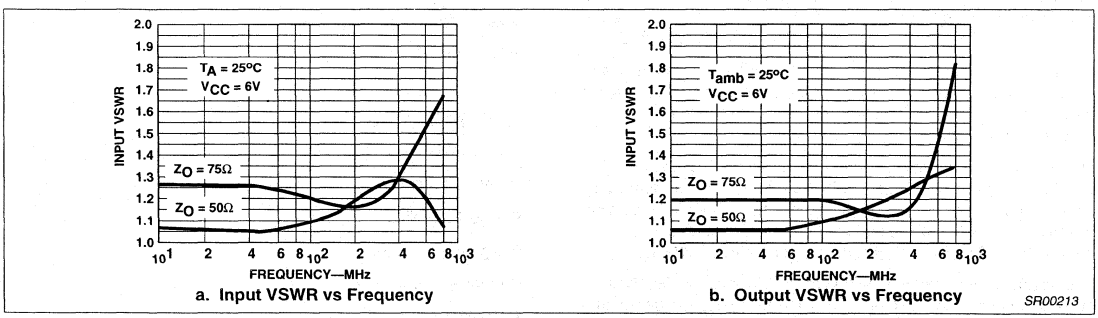


Figure 21. Input/Output VSWR vs Frequency

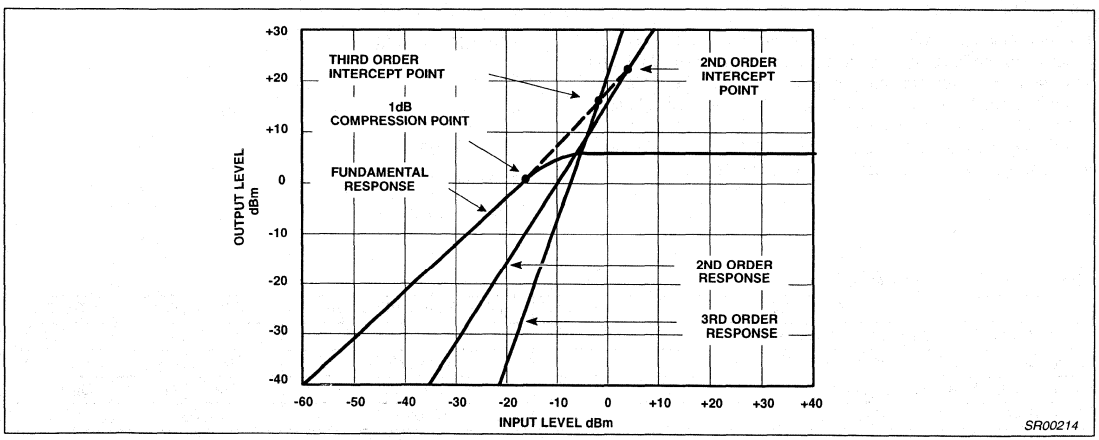


Figure 22.

Wide-band high-frequency amplifier — NE/SA/SE5205A

DESCRIPTION

The NE/SA/SE5205A family of wideband amplifiers replace the NE/SA/SE5205 family. The 'A' parts are fabricated on a rugged 2μm bipolar process featuring excellent statistical process control. Electrical performance is nominally identical to the original parts.

The NE/SA/SE5205A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205A operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205A solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the -3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205As in series as required, without any degradation in amplifier stability.

PIN CONFIGURATIONS

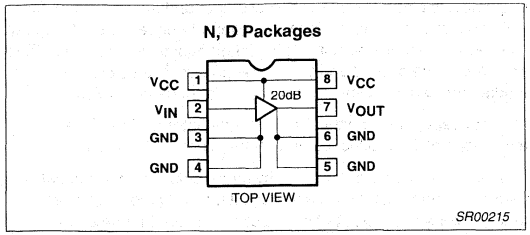


Figure 1. Pin Configuration

FEATURES

- 600MHz bandwidth
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface mount package available
- MIL-STD processing available
- 2000V ESD protection

APPLICATIONS

- 75Ω cable TV decoder boxes
- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broad-band LANs
- Fiber-optics
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5205AD	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5205AN	SOT97-1
8-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5205AD	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5205AN	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	SE5205AN	SOT97-1

EQUIVALENT SCHEMATIC

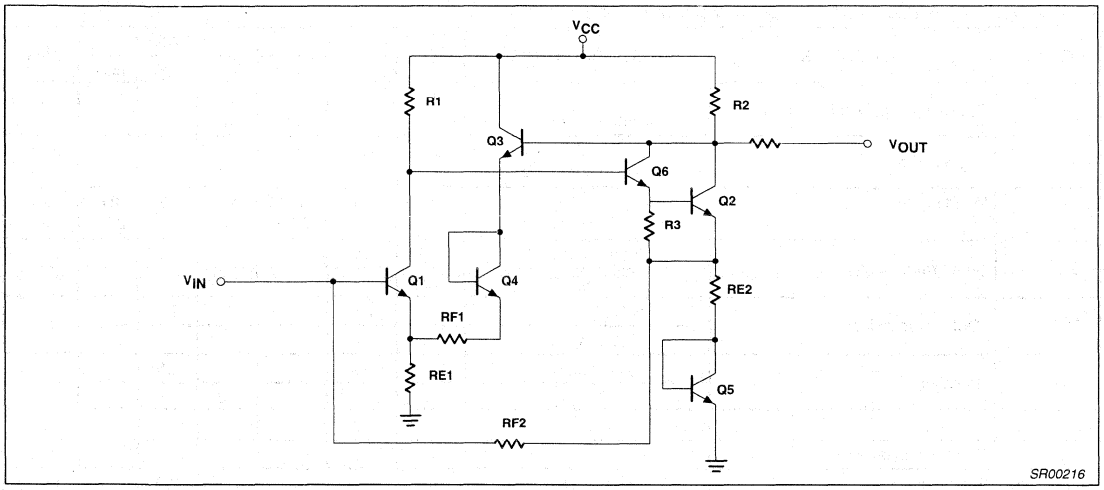


Figure 2. Equivalent Schematic

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	-40 to +85	°C
	SE grade	-55 to +125	°C
P_{DMAX}	Maximum power dissipation, T_A=25°C (still-air)[1, 2]		
	N package	1160	mW
	D package	780	mW

NOTES:
1. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205A			NE/SA5205A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	25 25	32 33	20 19	25 25	32 33	mA mA
S21	Insertion gain	f=100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f=100MHz D, N		25			25		dB
		DC - f_{MAX} D, N	12			12			
S22	Output return loss	f=100MHz D, N		27			27		dB
		DC - f_{MAX}	12			12			
S12	Isolation	f=100MHz		-25			-25		dB
		DC - f_{MAX}	-18			-18			
t_R	Rise time			500			500		ps
t_P	Propagation delay			500			500		ps
BW	Bandwidth	±0.5dB D, N		300			450		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
	Noise figure (75Ω)	f=100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0			6.0		dB
	Saturated output power	f=100MHz		+7.0			+7.0		dBm
	1dB gain compression	f=100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f=100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f=100MHz		+24			+24		dBm

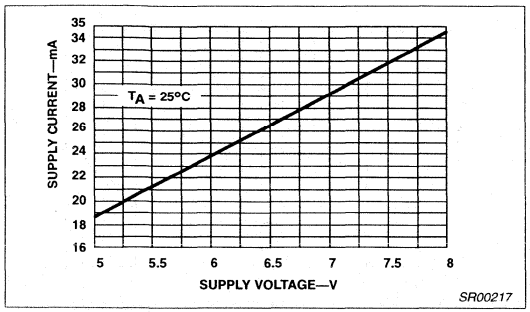


Figure 3. Supply Current vs Supply Voltage

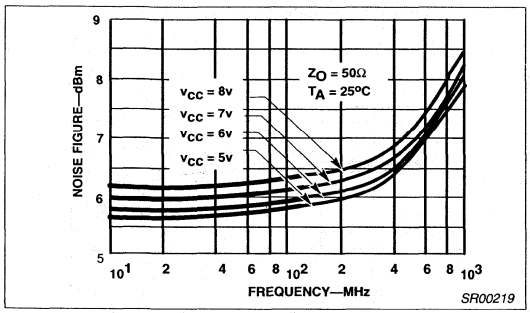


Figure 4. Noise Figure vs Frequency

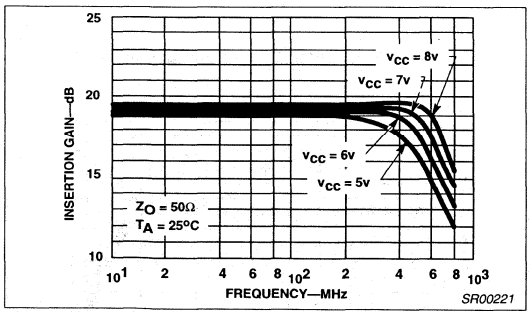


Figure 5. Insertion Gain vs Frequency (S_{21})

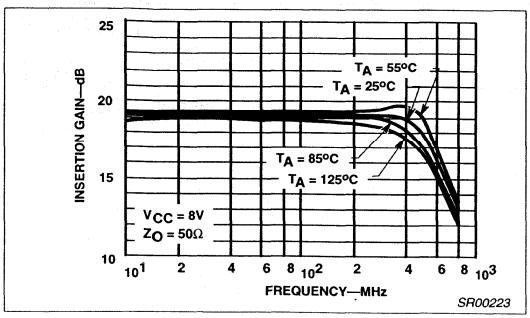


Figure 6. Insertion Gain vs Frequency (S_{21})

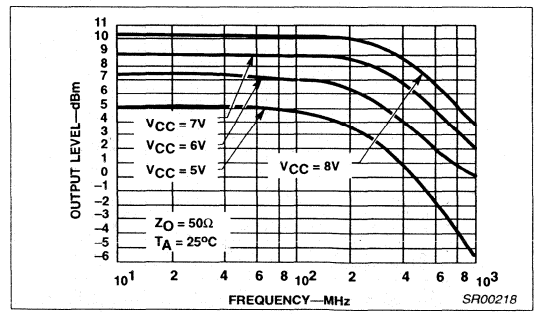


Figure 7. Saturated Output Power vs Frequency

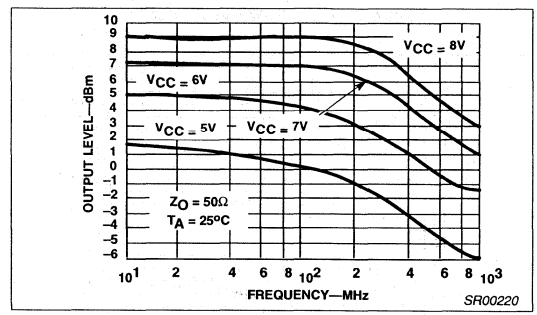


Figure 8. 1dB Gain Compression vs Frequency

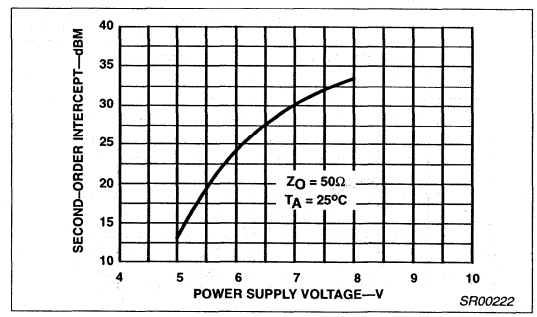


Figure 9. Second-Order Output Intercept vs Supply Voltage

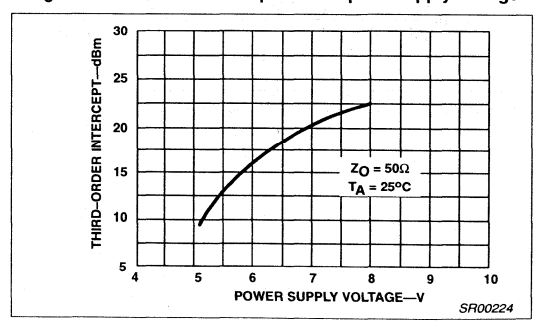


Figure 10. Third-Order Intercept vs Supply Voltage

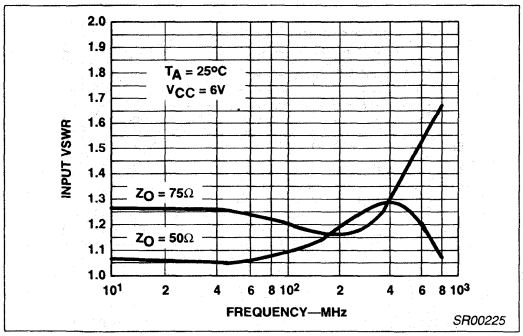


Figure 11. Input VSWR vs Frequency

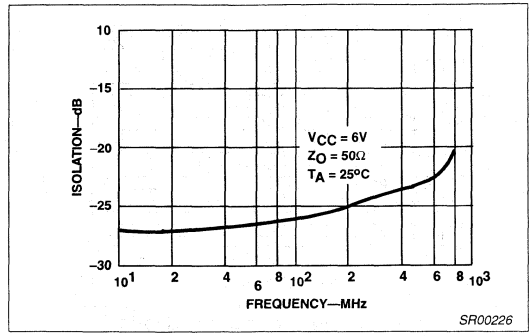


Figure 14. Isolation vs Frequency (S_{12})

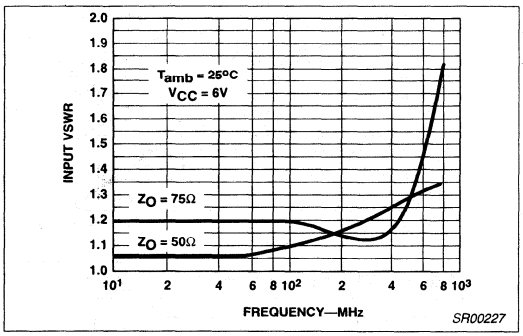


Figure 12. Output VSWR vs Frequency

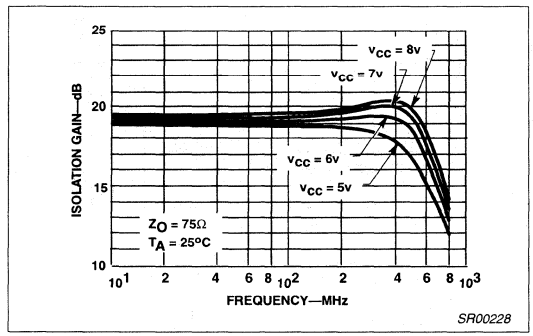


Figure 15. Insertion Gain vs Frequency (S_{21})

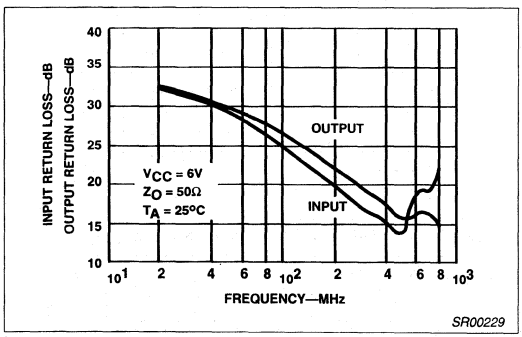


Figure 13. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

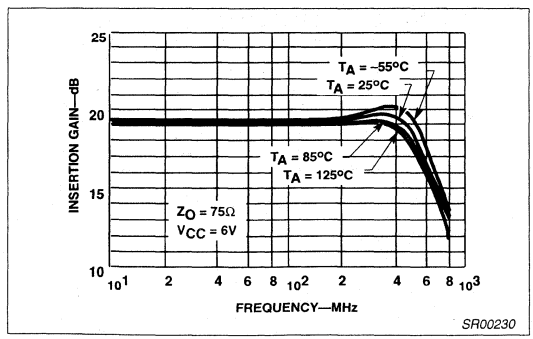


Figure 16. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 17, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{(R_{F1} + R_{E1})}{R_{E1}} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

NF =

$$10 \log \left[1 + \left[\frac{r_b + R_{E1} + \frac{KT}{2qI_{C1}}}{R_O} \right] \right] dB \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1}$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2,(4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

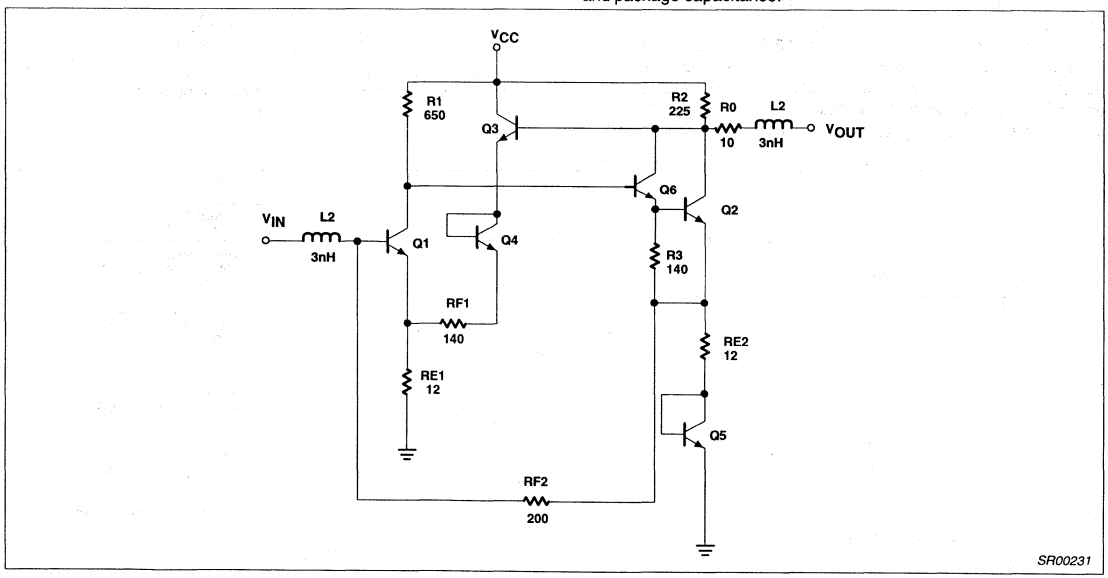


Figure 17. Schematic Diagram

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA Max). For operation at supply voltages other than 6V, see Figure 3 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D package body against the PC board plane.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 18. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 19.

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 20.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205A to other high-frequency amplifiers.

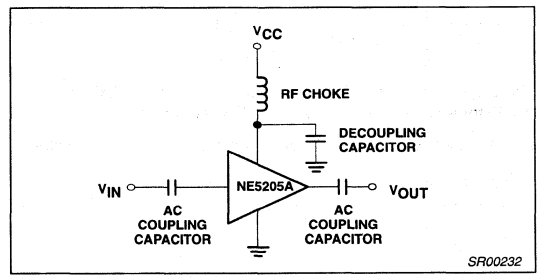


Figure 18. Circuit Schematic for Coupling and Power Supply Decoupling

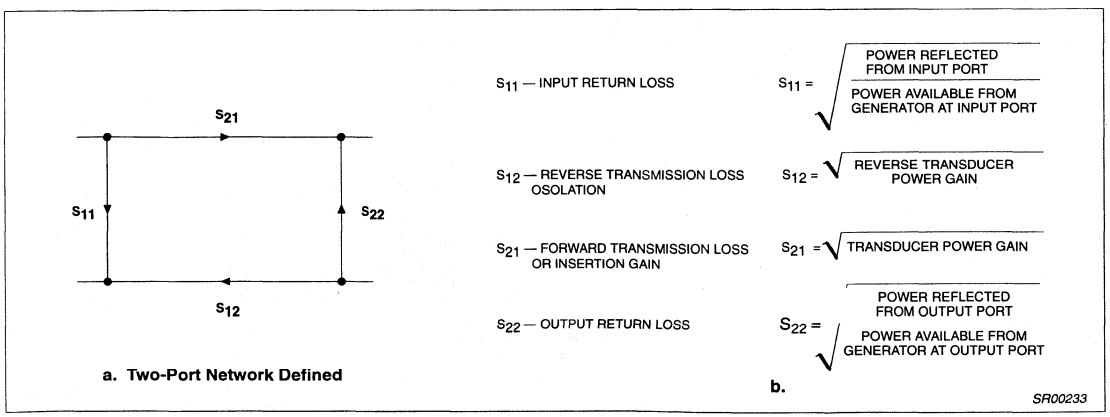
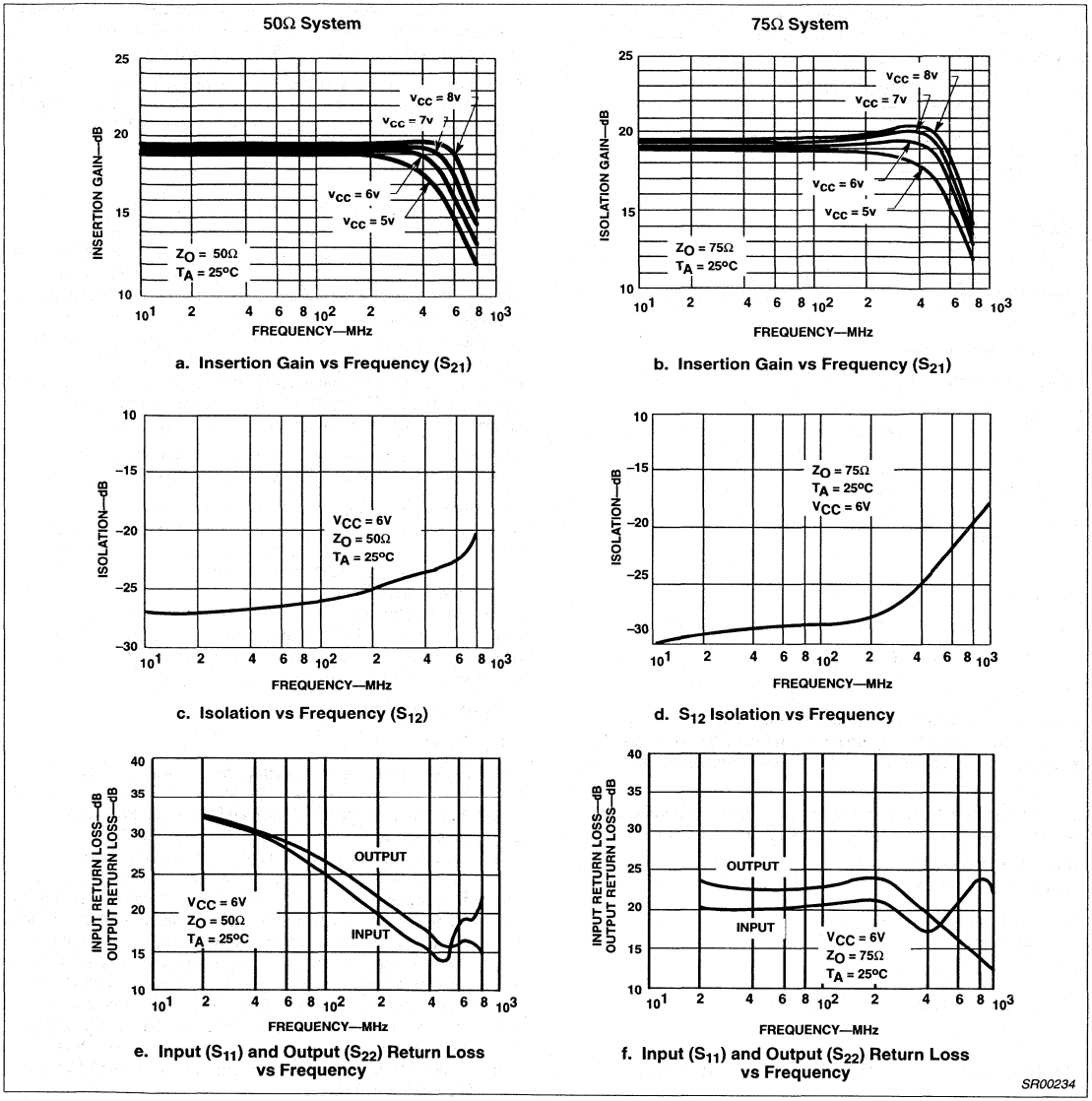


Figure 19.



a. Insertion Gain vs Frequency (S_{21})

b. Insertion Gain vs Frequency (S_{21})

c. Isolation vs Frequency (S_{12})

d. S_{12} Isolation vs Frequency

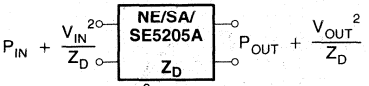
e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 20.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the NE/SA/SE5205A



$$P_{IN} + \frac{V_{IN}^2}{Z_D} \quad P_{OUT} + \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I{}^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the
NE/SA/SE5205A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 21. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS=S_{11}dB
S_{11}dB=20 Log $|S_{11}|$

OUTPUT RETURN LOSS=S_{22}dB
S_{22}dB=20 Log $|S_{22}|$

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 22, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

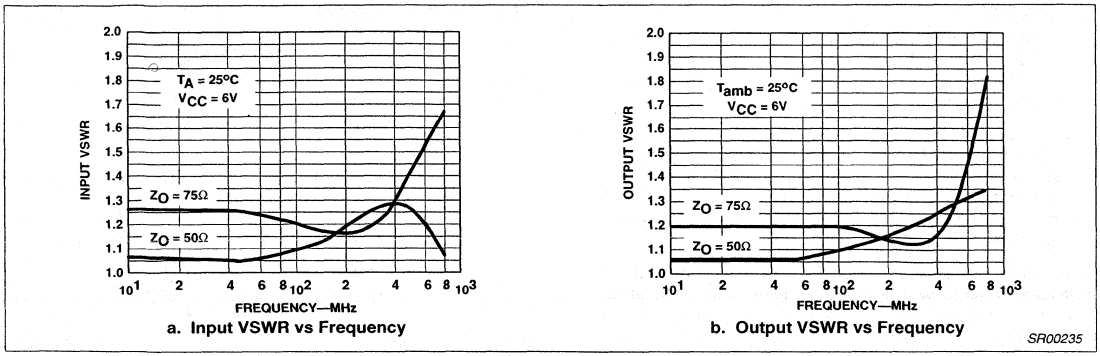
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2=P_{OUT}+IMR_2$

$IP_3=P_{OUT}+IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205A we have chosen an output level of -10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

Figure 21. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

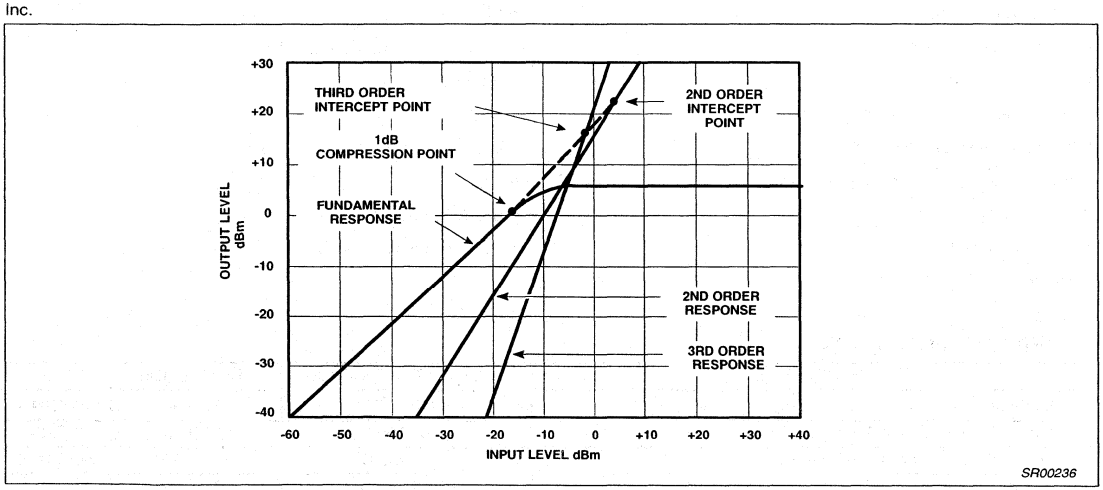


Figure 22.

Wideband variable gain amplifier NE/SA5209

DESCRIPTION

The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

PIN CONFIGURATION

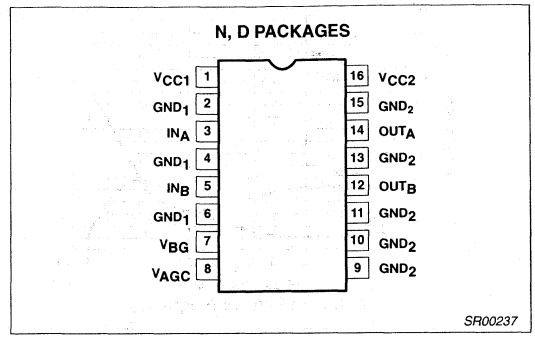


Figure 1. Pin Configuration

FEATURES

- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5209D	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5209N	SOT28-4
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5209D	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5209N	SOT28-4

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	38	43	48	mA
		Over temperature[1]	30		55	
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	17	19	21	dB
		Over temperature[1]	16		22	
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	23	25	27	dB
		Over temperature[1]	22		28	
R_{IN}	Input resistance (single-ended)	DC tested at ±50µA	0.9	1.2	1.5	kΩ
		Over temperature[1]	0.8		1.7	
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	40	60	75	Ω
		Over temperature[1]	35		90	
V_{OS}	Output offset voltage (output referred)			±20	±100	mV
		Over temperature[1]			±250	
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
		Over temperature[1]	1.4		2.6	
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
		Over temperature[1]	1.7		3.1	
PSRR	Output offset supply rejection ratio (output referred)		20	45		dB
		Over temperature[1]	15			
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
		Over temperature[1]	1.1		1.55	

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
R_{BG}	Bandgap loading	Over temperature[1]	2	10		kΩ
V_{AGC}	AGC DC control voltage range	Over temperature[1]		0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	μA
		Over temperature[1]			-10	

NOTES:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth		600	850		MHz
		Over temperature[1]	500			
GF	Gain flatness	DC - 500MHz		±0.4		dB
		Over temperature[1]		±0.6		
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[2]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[2]	R_L = 50Ω		400		mV_{P-P}
		R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.
2. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5209 APPLICATIONS

The NE5209 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 2. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5209 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5209 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5209 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5209 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5209. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5209 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5209 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5209 is shown in Figure 3. Three NE5209s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5209s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5209s will give a dynamic range in excess of 60dB.

The NE5209 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

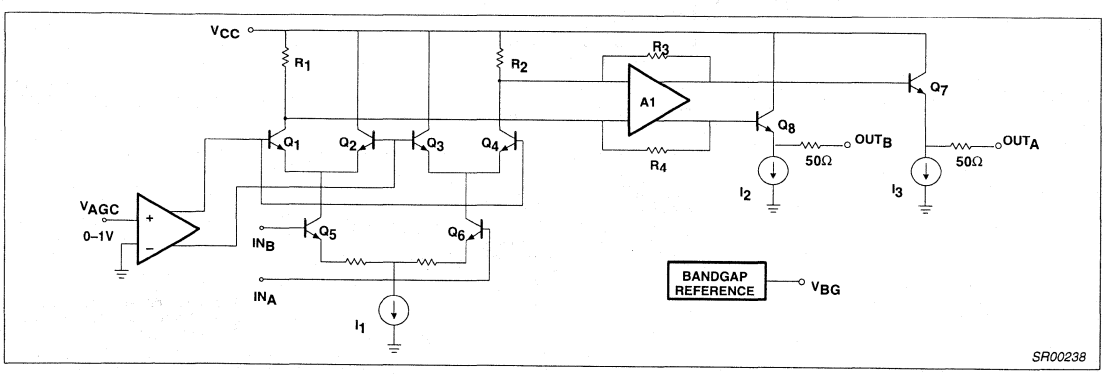


Figure 2. Equivalent Schematic of the VGA

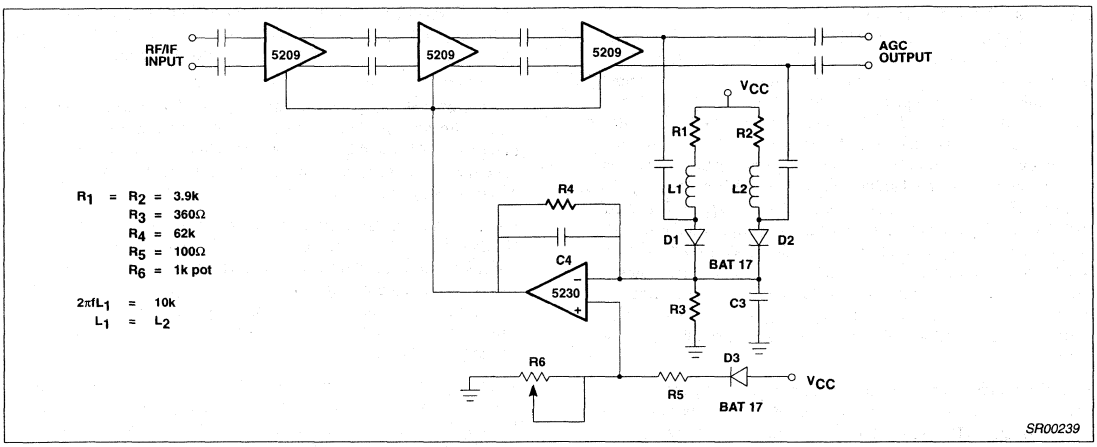


Figure 3. AGC Configuration Using Cascaded NE5209s

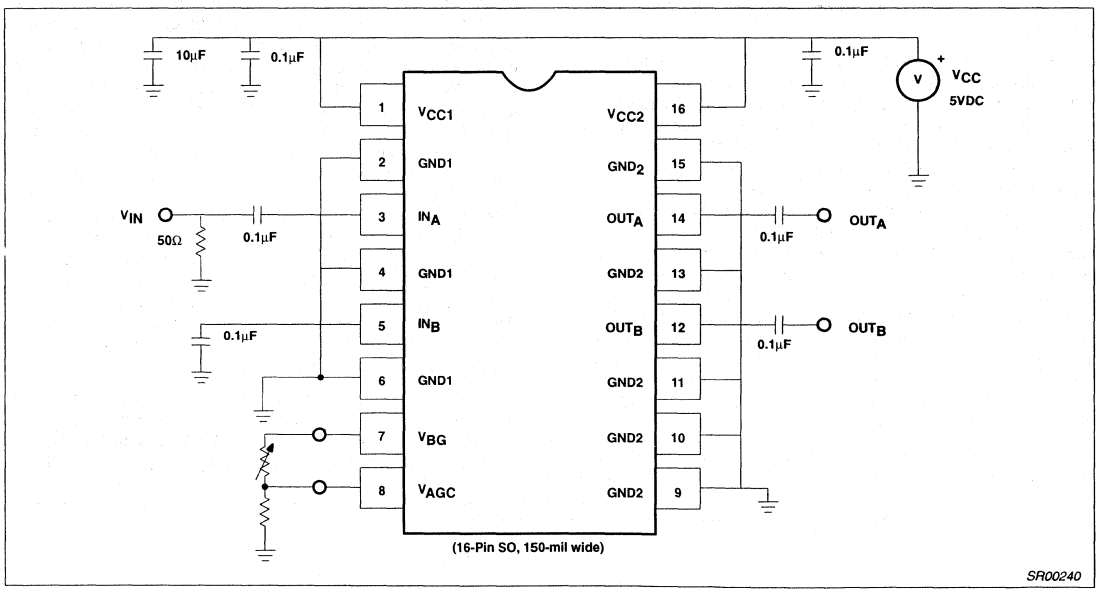


Figure 4. VGA AC Evaluation Board

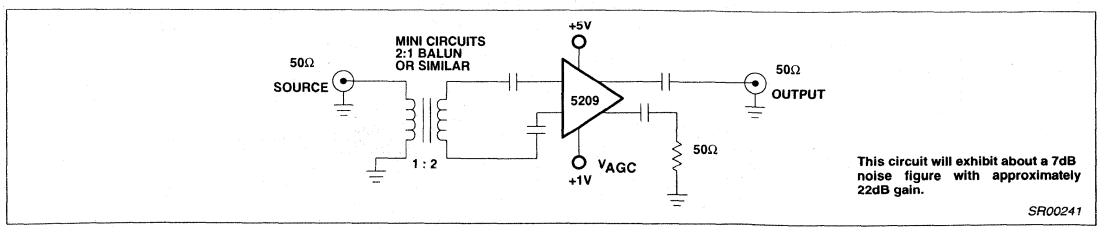


Figure 5. Broadband Noise Optimization

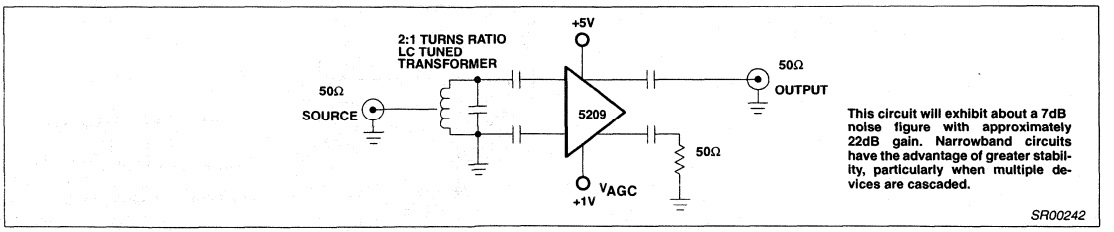


Figure 6. Narrowband Noise Optimization

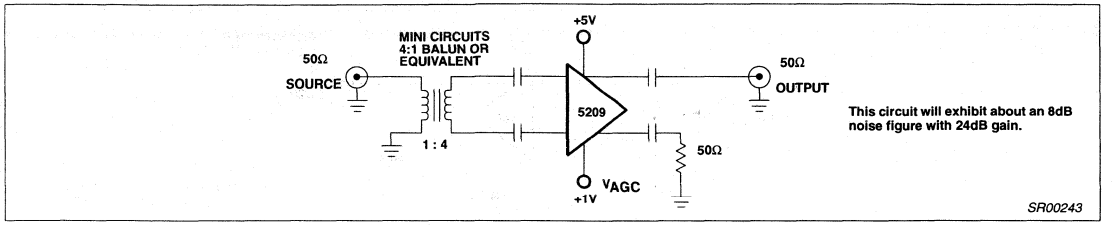


Figure 7. Broadband Gain Optimization

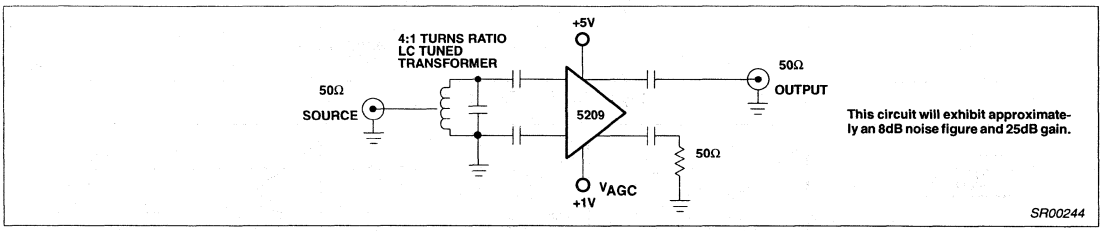


Figure 8. Narrowband Gain Optimization

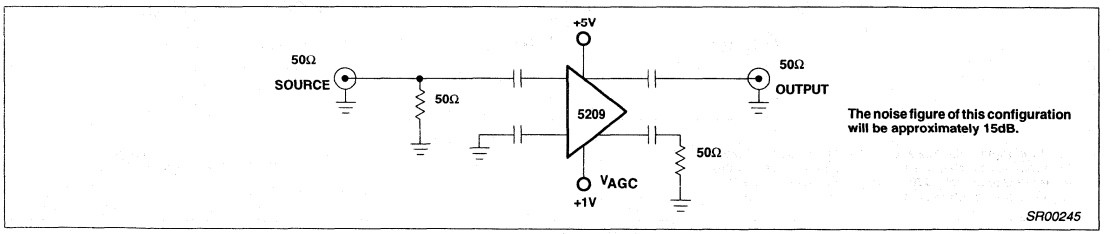


Figure 9. Simple Amplifier Configuration

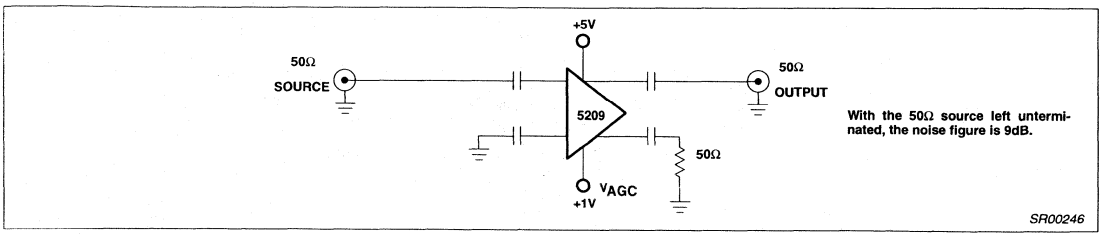


Figure 10. Unterminated Configuration

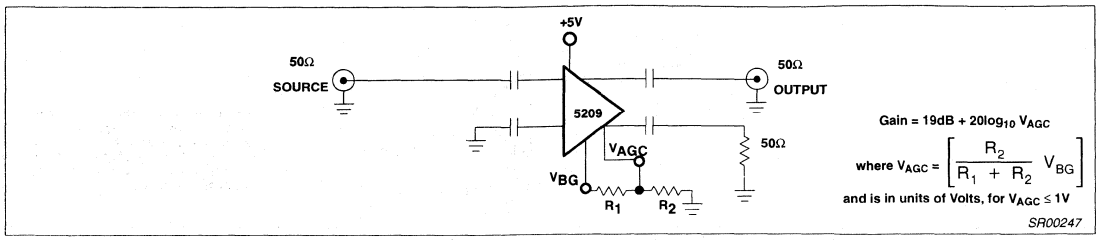


Figure 11. User-Programmable Fixed Gain Block

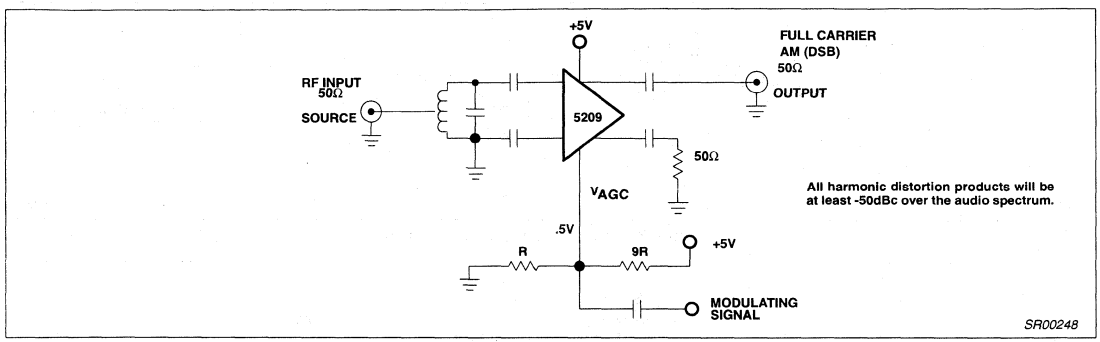


Figure 12. AM Modulator

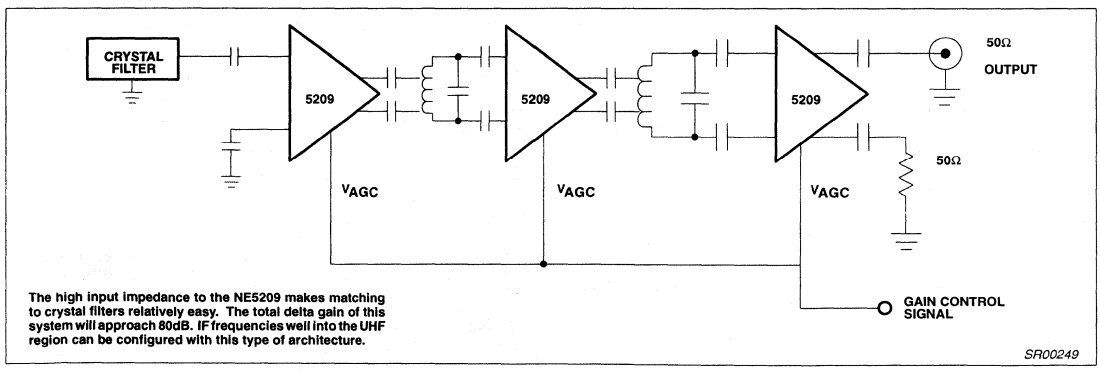


Figure 13. Receiver AGC IF Gain

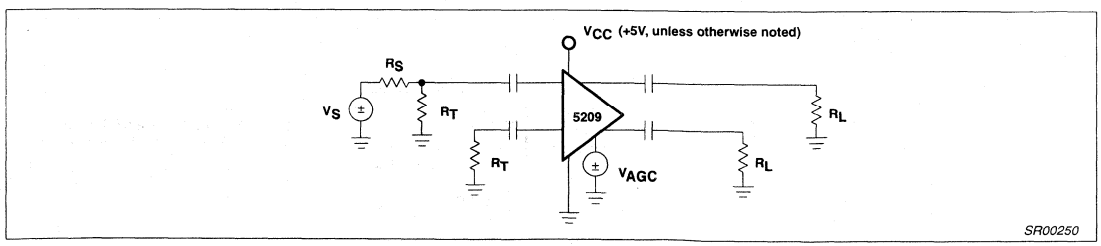


Figure 14. Test Set-up 1 (Used for all Graphs)

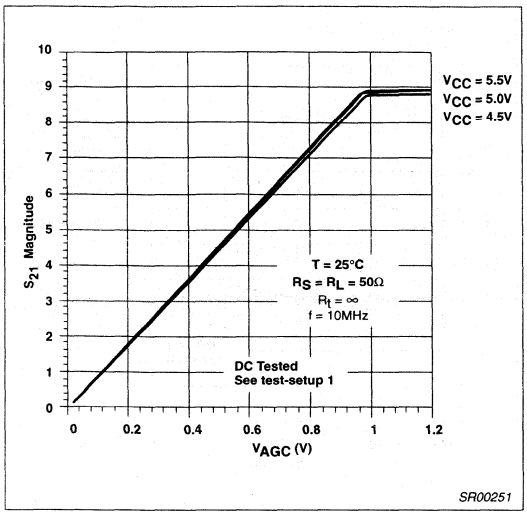


Figure 15. Gain vs V_{AGC} and V_{CC}

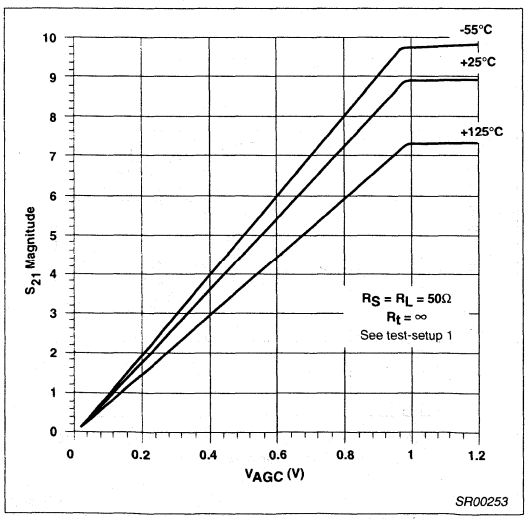


Figure 16. Insertion Gain vs V_{AGC} and Temperature

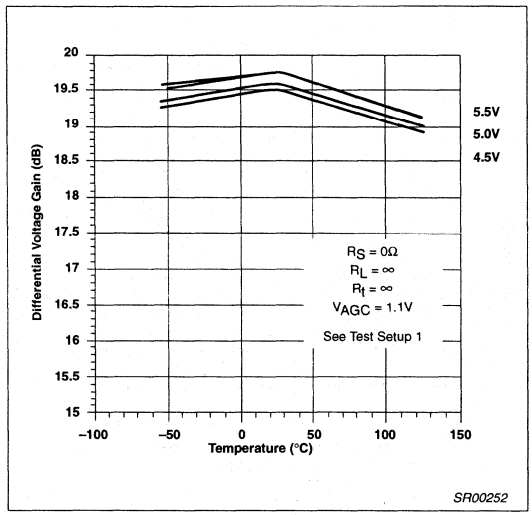


Figure 17. Voltage Gain vs Temperature and V_{CC}

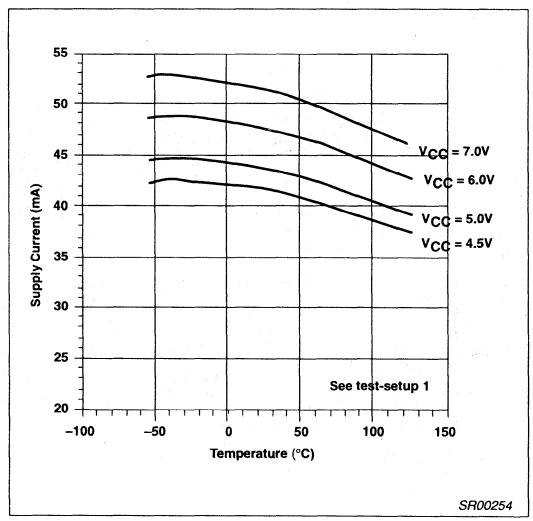


Figure 18. Supply Current vs Temperature and V_{CC}

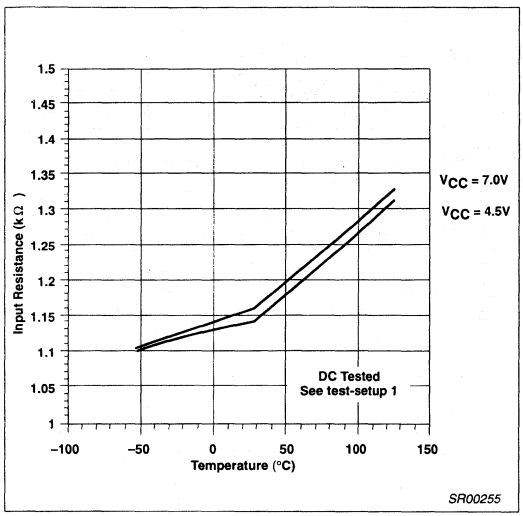


Figure 19. Input Resistance vs Temperature

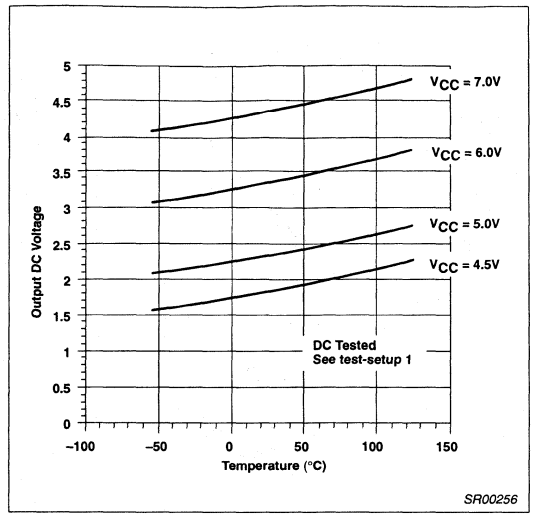


Figure 21. Output Bias Voltage vs Temperature and V_{CC}

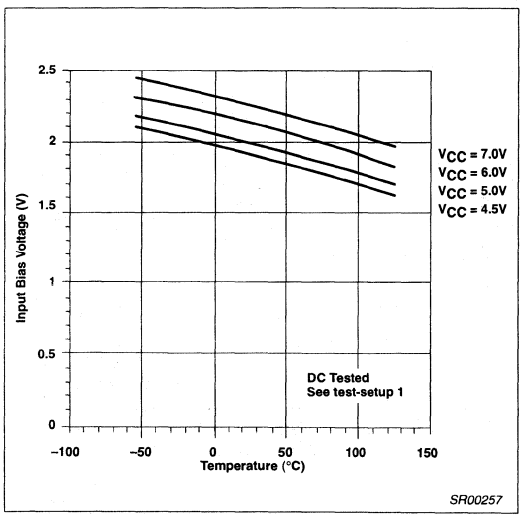


Figure 20. Input Bias Voltage vs Temperature

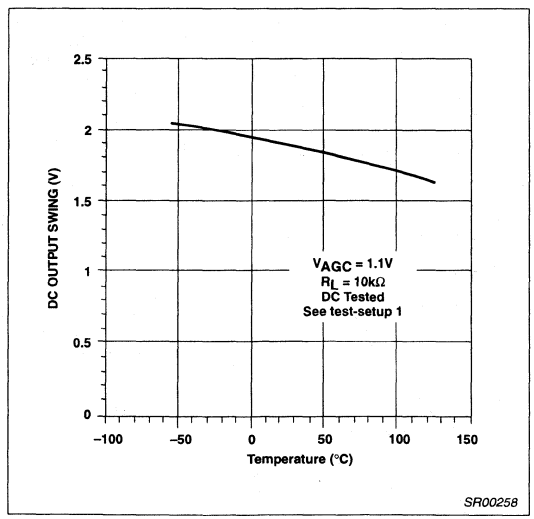


Figure 22. DC Output Swing vs Temperature

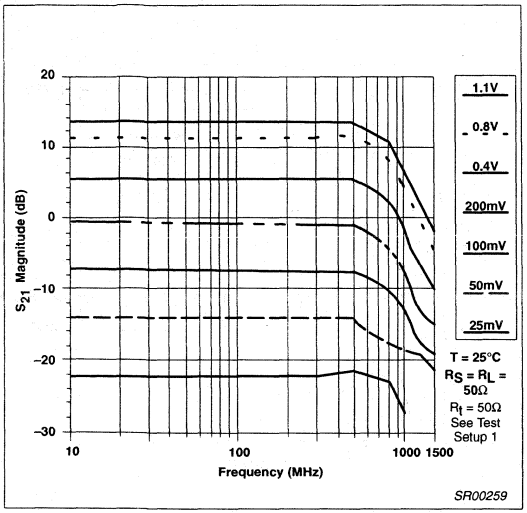


Figure 23. Insertion Gain vs Frequency and V_{AGC}

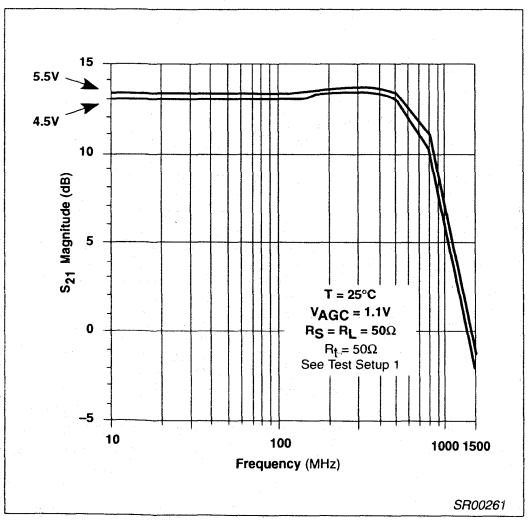


Figure 24. Insertion Gain vs Frequency and V_{CC}

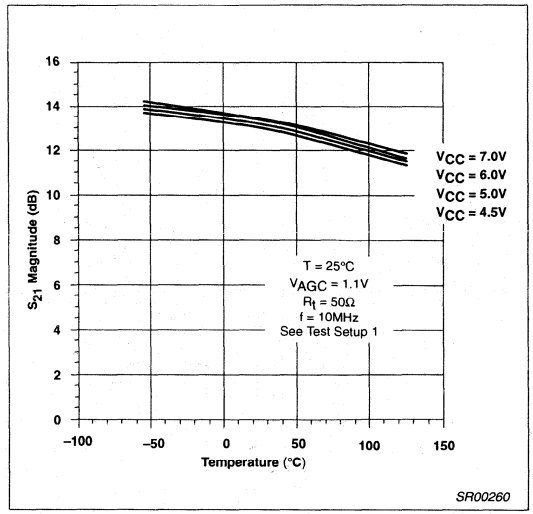


Figure 25. Insertion Gain vs Temperature and V_{CC}

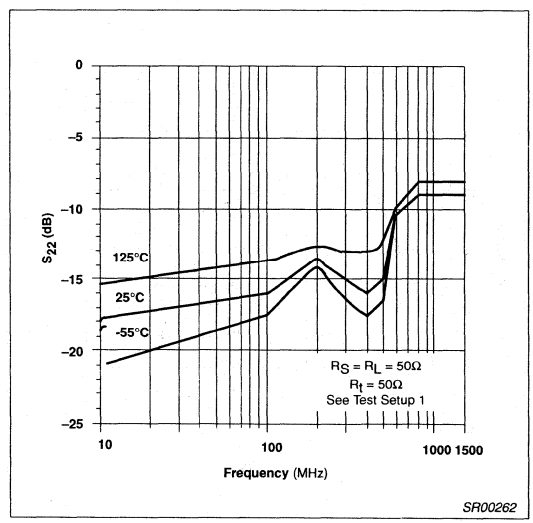


Figure 26. Output Return Loss vs Frequency

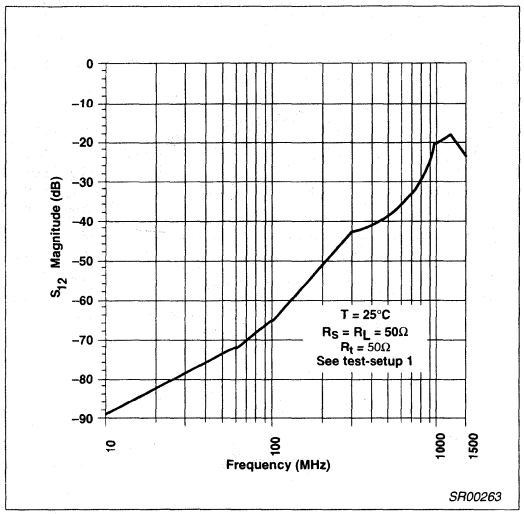


Figure 27. Reverse Isolation vs Frequency

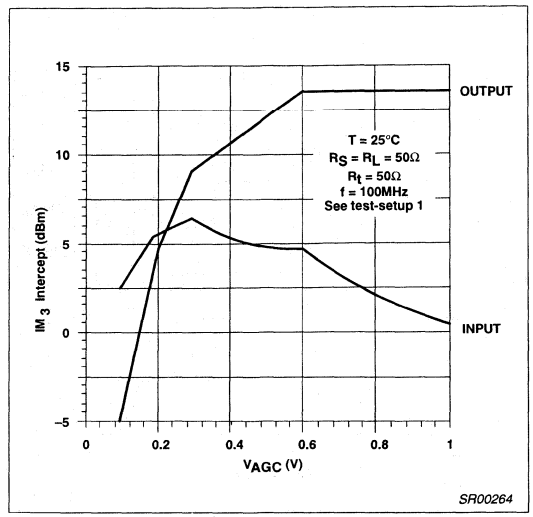


Figure 29. Third-Order Intermodulation Intercept vs V_{AGC}

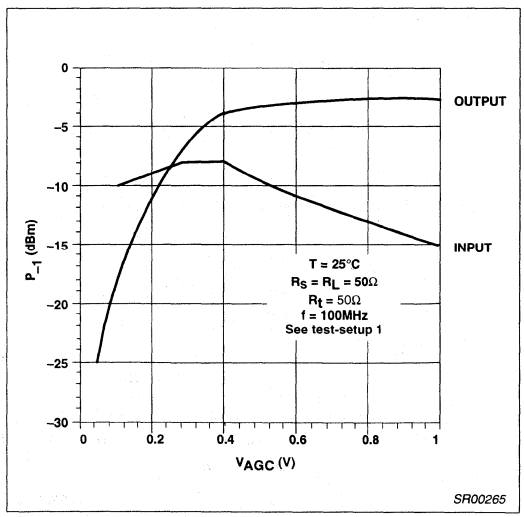


Figure 28. 1dB Gain Compression vs V_{AGC}

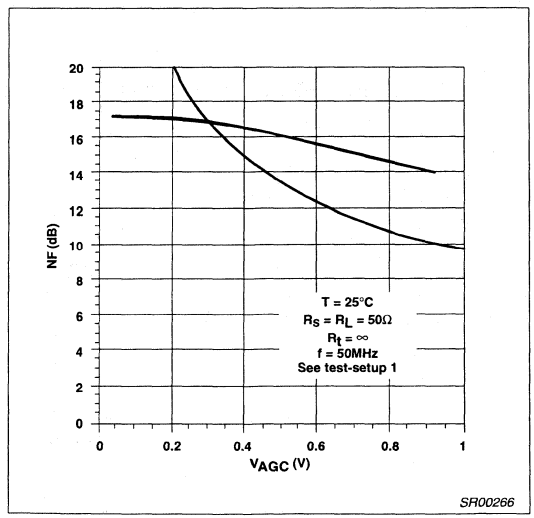


Figure 30. Noise Figure vs V_{AGC}

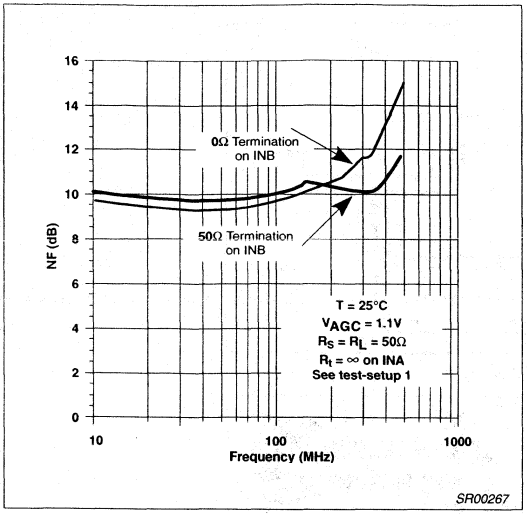


Figure 31. Noise Figure vs Frequency

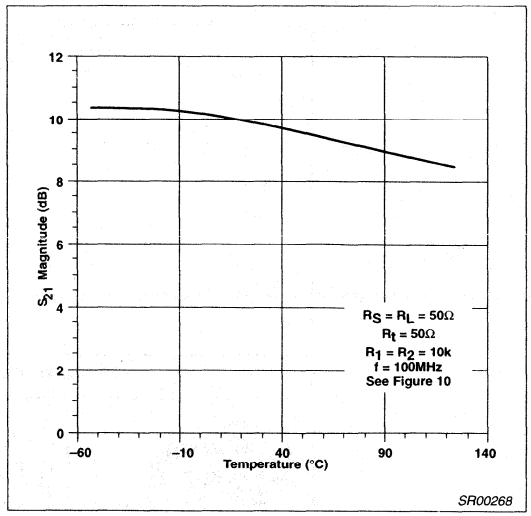


Figure 33. Fixed Gain vs Temperature

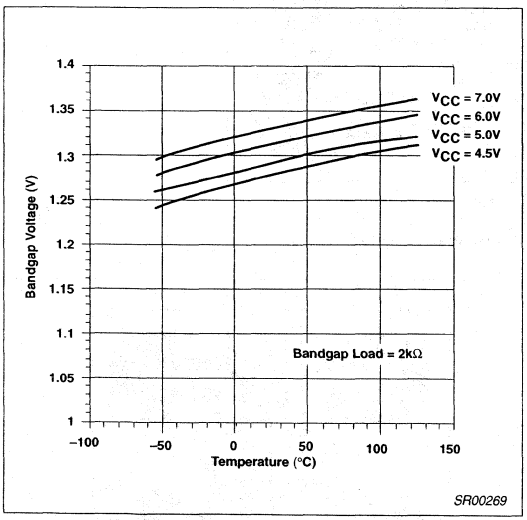


Figure 32. Bandgap Voltage vs Temperature and V_{CC}

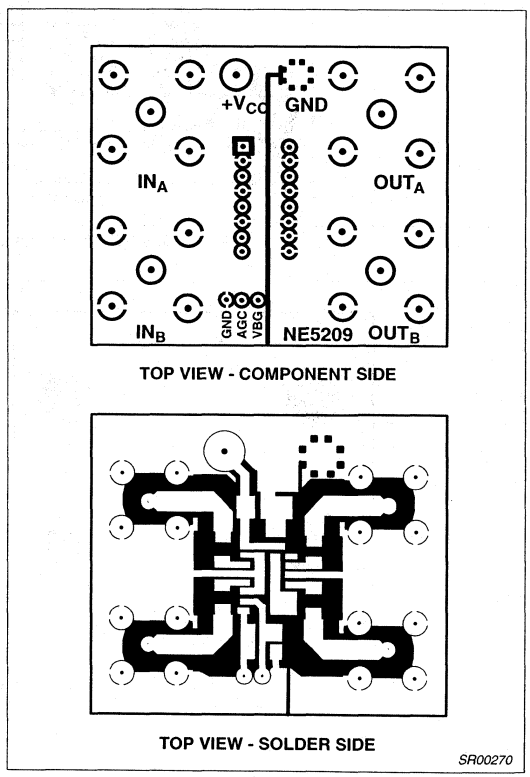
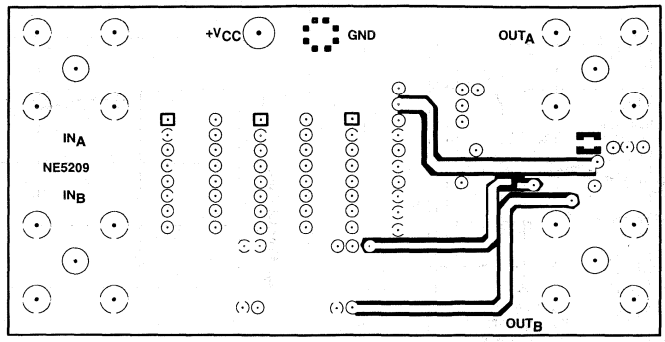
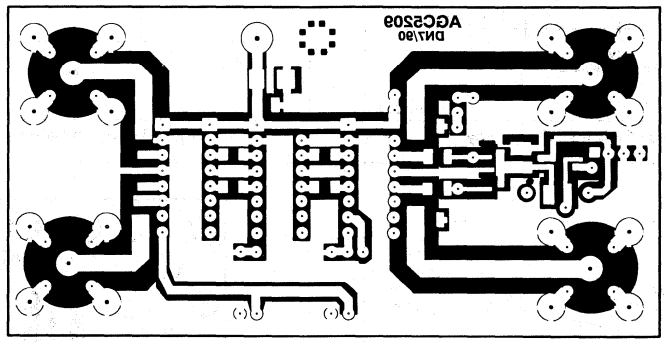


Figure 34. VGA AC Evaluation Board Layout



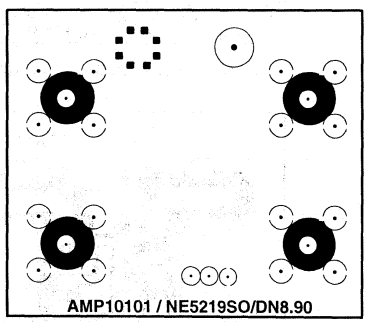
TOP VIEW - COMPONENT SIDE



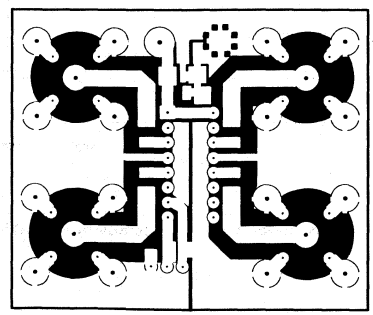
TOP VIEW - SOLDER SIDE

SR00271

Figure 35. AGC Configuration Using Cascaded NE5209s - Layout



TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

SR00272

Figure 36. VGA AC Evaluation Board Layout (DIP Package)

Wideband variable gain amplifier NE/SA5219

DESCRIPTION

The NE5219 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5219 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5219 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

PIN CONFIGURATION

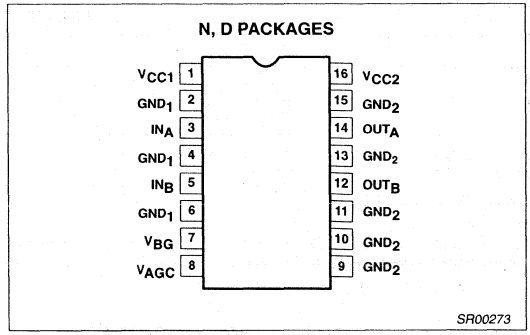


Figure 1. Pin Configuration

FEATURES

- 700MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

Description	Temperature Range	Order Code	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5219D	SOT109-1
16-Pin Plastic Dual In-Line package (DIP)	0 to +70°C	NE5219N	SOT28-4
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5219D	SOT109-1
16-Pin Plastic Dual In-Line package (DIP)	-40 to +85°C	SA5219N	SOT28-4

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	36	43	50	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	16	19	22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	22	25	28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.8	1.2	1.6	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	35	60	80	Ω
V_{OS}	Output offset voltage (output referred)			±20	±150	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
PSRR	Output offset supply rejection ratio		18	45		dB
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
R_{BG}	Bandgap loading		2	10		kΩ
V_{AGC}	AGC DC control voltage range			0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	μA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth			700		MHz
GF	Gain flatness	DC - 500MHz		±0.4		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[1]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[1]	R_L = 50Ω		400		mV_{P-P}
		R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5219 APPLICATIONS

The NE5219 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 2. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5219 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5219 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5219 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5219 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5219. A

maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5219 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5219 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5219 is shown in Figure 3. Three NE5219s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5219s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5219s will give a dynamic range in excess of 60dB.

The NE5219 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

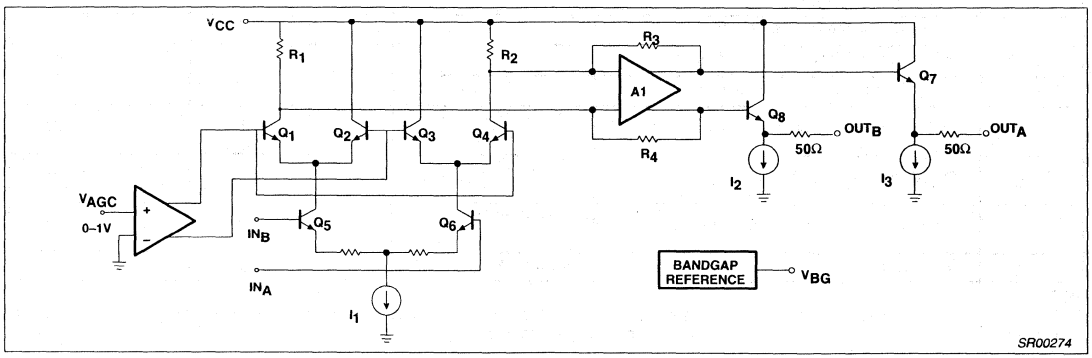


Figure 2. Equivalent Schematic of VGA

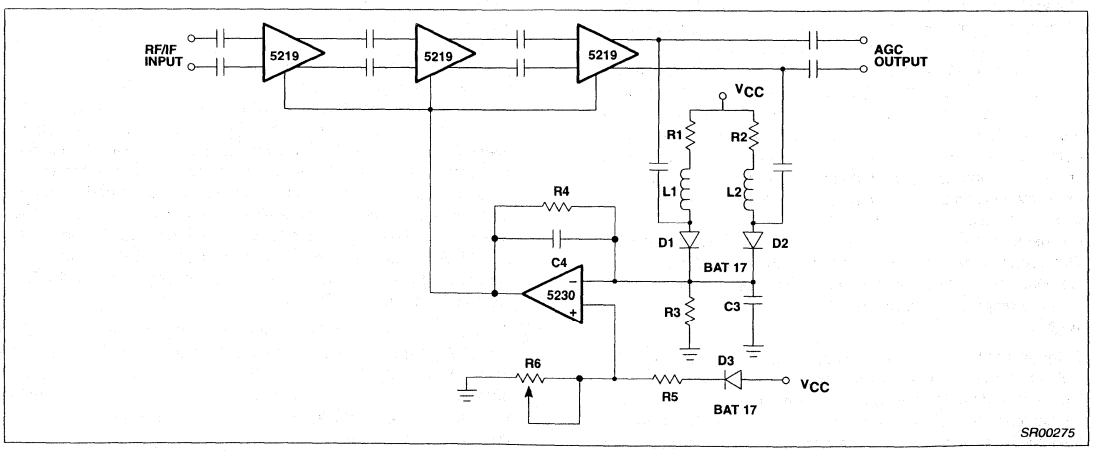


Figure 3. AGC Configuration Using Cascaded NE5219s

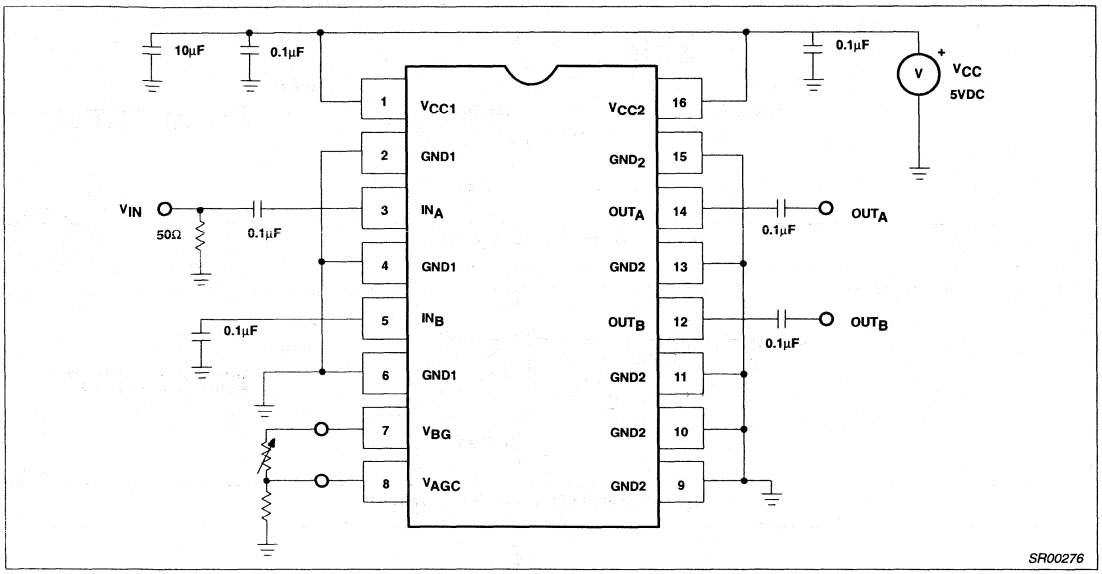


Figure 4. VGA AC Evaluation Board

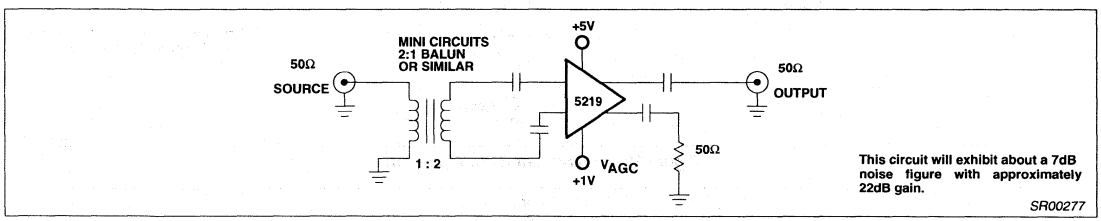


Figure 5. Broadband Noise Optimization

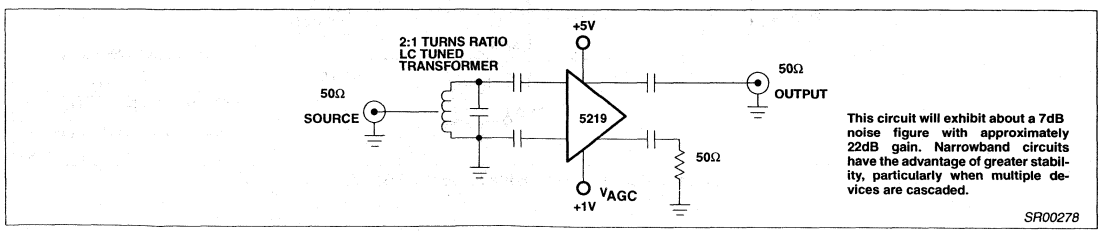


Figure 6. Narrowband Noise Optimization

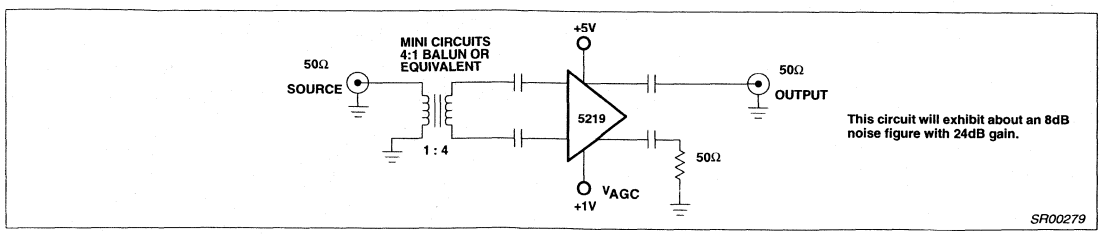


Figure 7. Broadband Gain Optimization

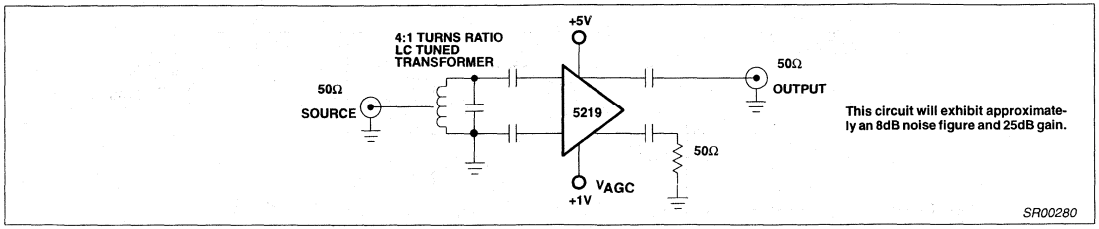


Figure 8. Narrowband Gain Optimization

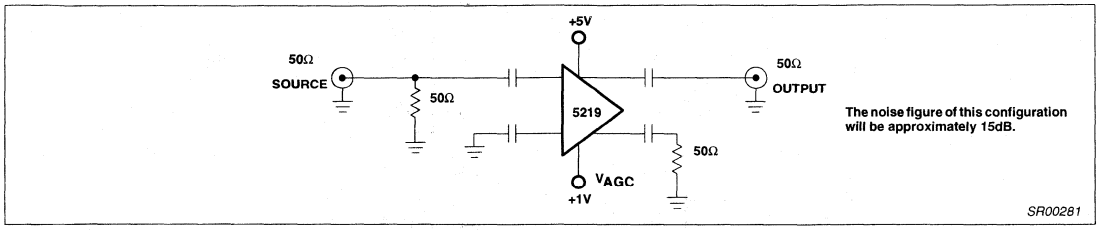


Figure 9. Simple Amplifier Configuration

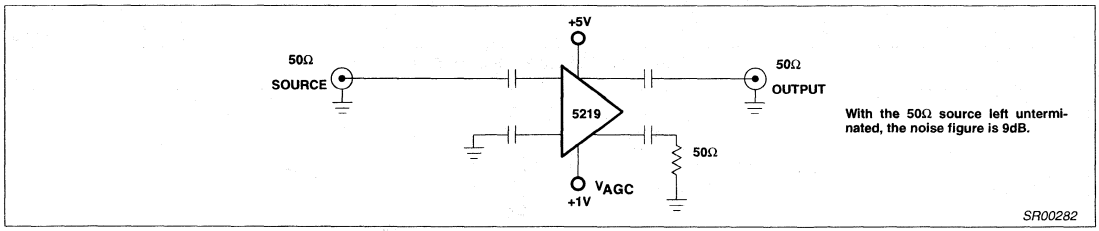


Figure 10. Unterminated Configuration

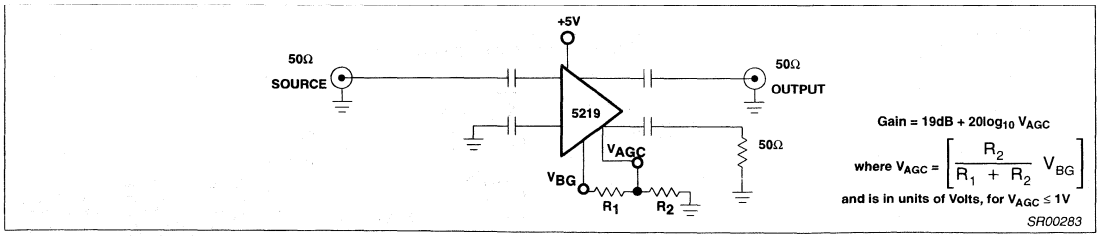


Figure 11. User-Programmable Fixed Gain Block

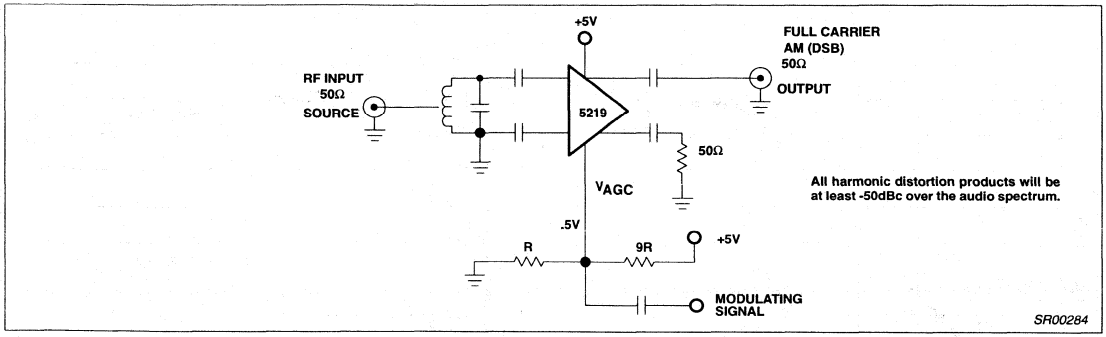


Figure 12. AM Modulator

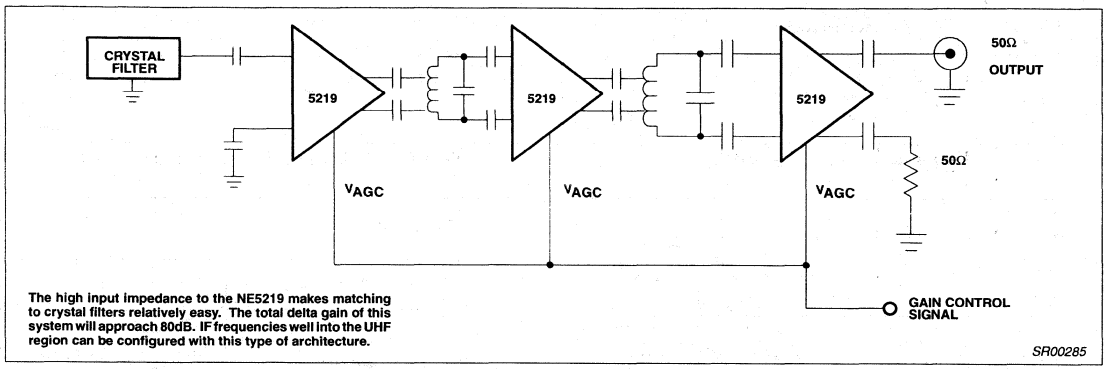


Figure 13. Receiver AGC IF Gain

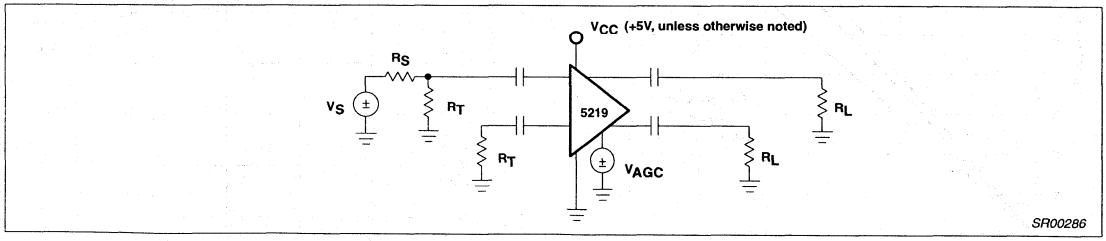


Figure 14. Test Set-up 1 (Used for all Graphs)

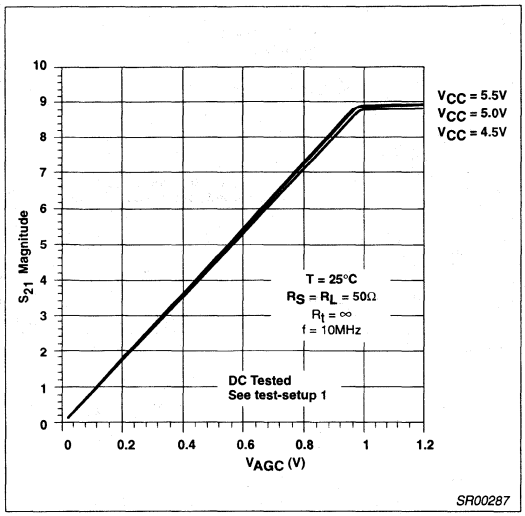


Figure 15. Gain vs V_{AGC} and V_{CC}

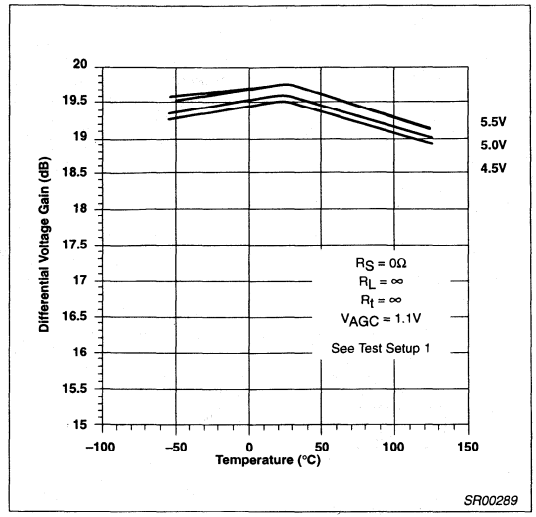


Figure 17. Voltage Gain vs Temperature and V_{CC}

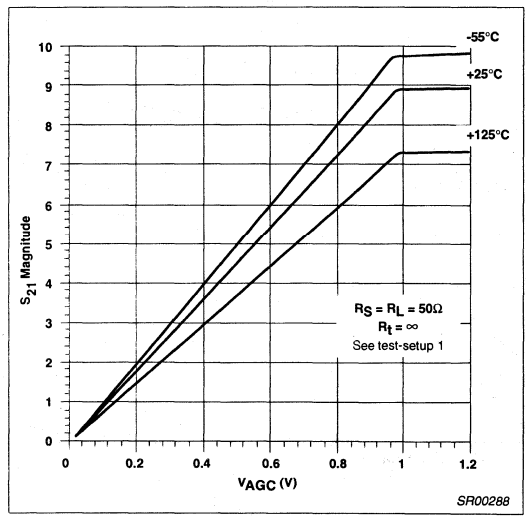


Figure 16. Insertion Gain vs V_{AGC} and Temperature

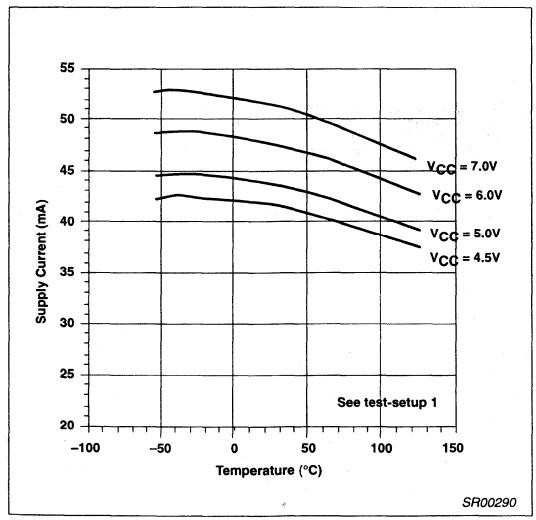


Figure 18. Supply Current vs Temperature and V_{CC}

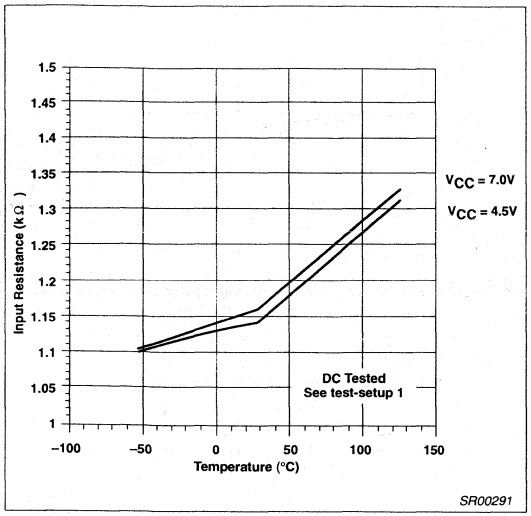


Figure 19. Input Resistance vs Temperature

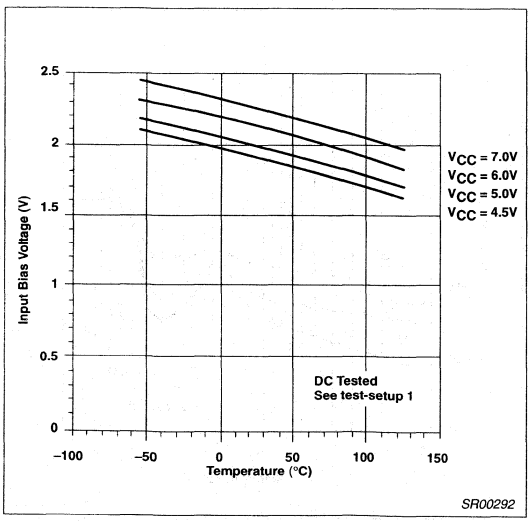


Figure 20. Input Bias Voltage vs Temperature

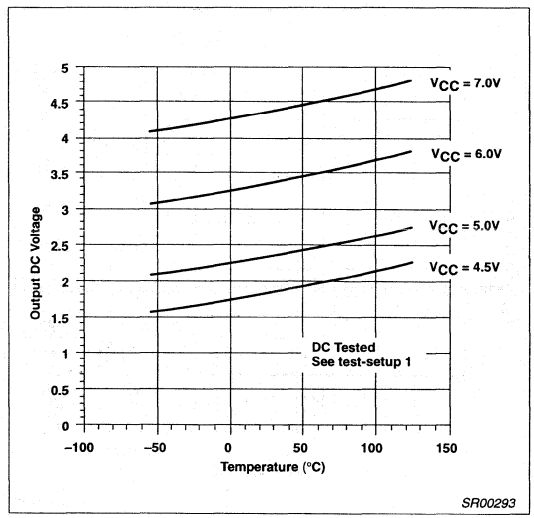


Figure 21. Output Bias Voltage vs Temperature and V_{CC}

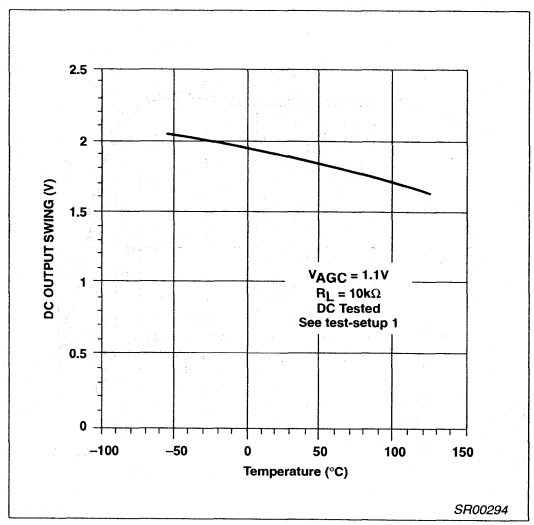


Figure 22. DC Output Swing vs Temperature

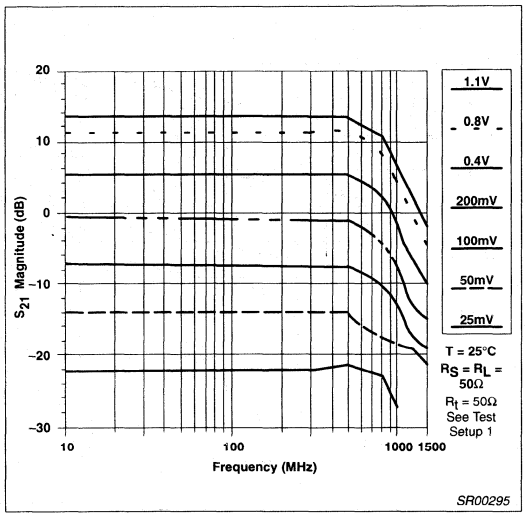


Figure 23. Insertion Gain vs Frequency and V_{AGC}

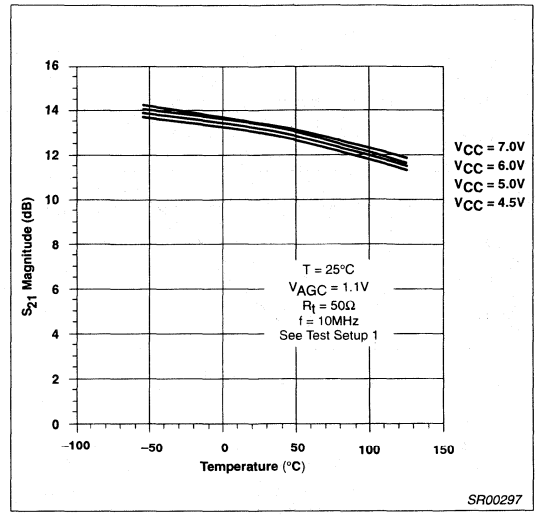


Figure 25. Insertion Gain vs Temperature and V_{CC}

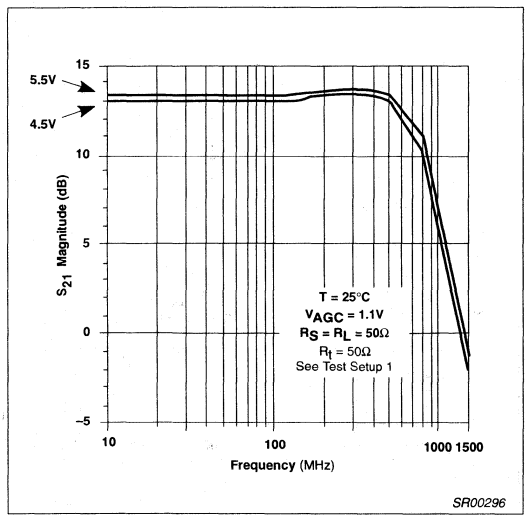


Figure 24. Insertion Gain vs Frequency and V_{CC}

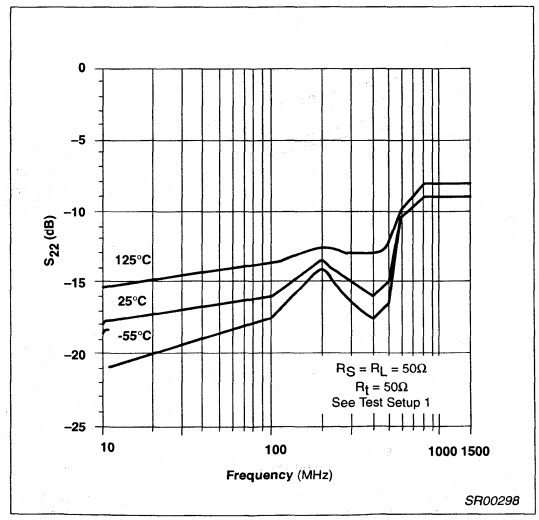


Figure 26. Output Return Loss vs Frequency

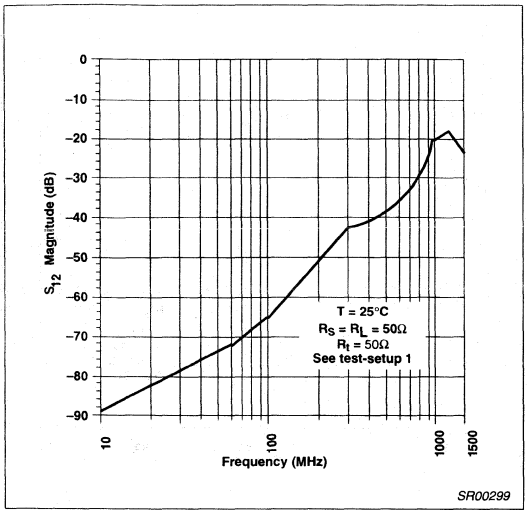


Figure 27. Reverse Isolation vs Frequency

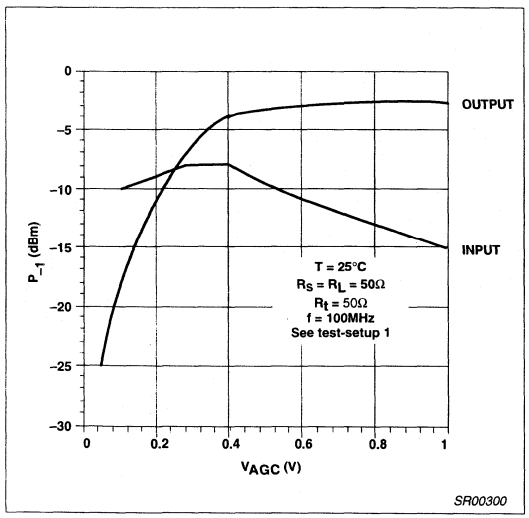


Figure 28. 1dB Gain Compression vs V_{AGC}

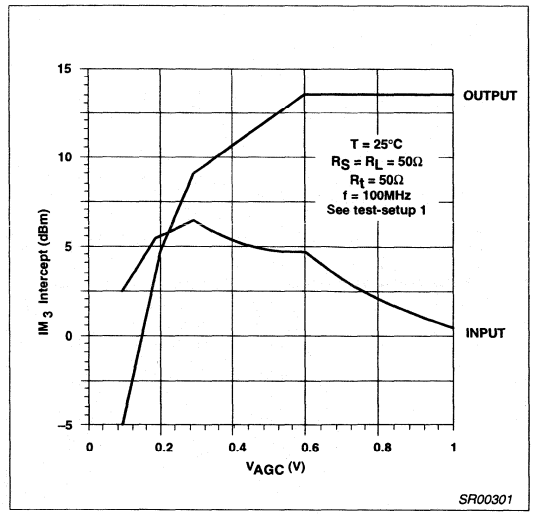


Figure 29. Third-Order Intermodulation Intercept vs V_{AGC}

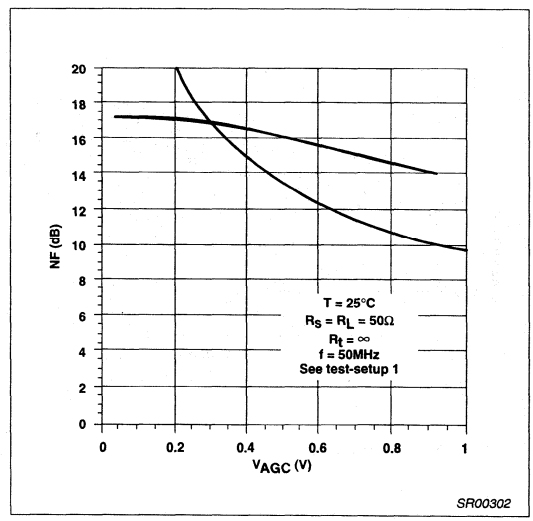


Figure 30. Noise Figure vs V_{AGC}

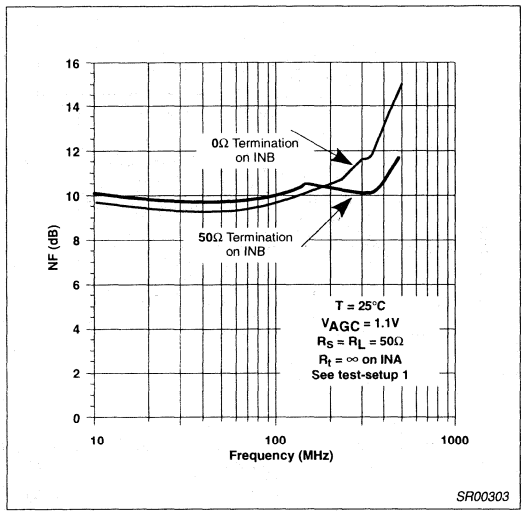


Figure 31. Noise Figure vs Frequency

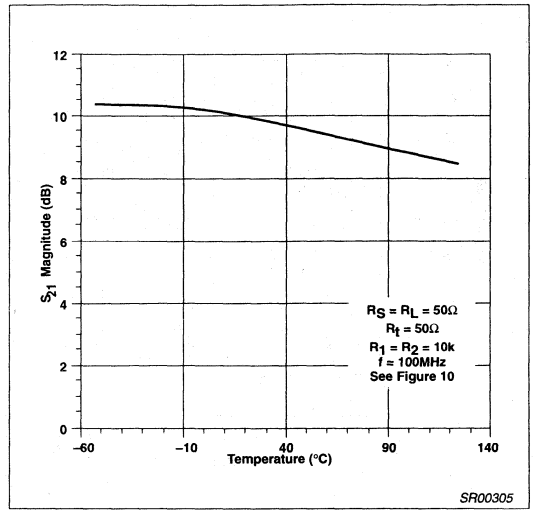


Figure 33. Fixed Gain vs Temperature

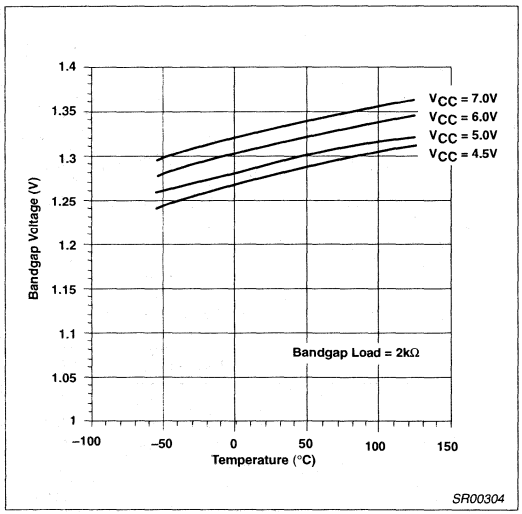
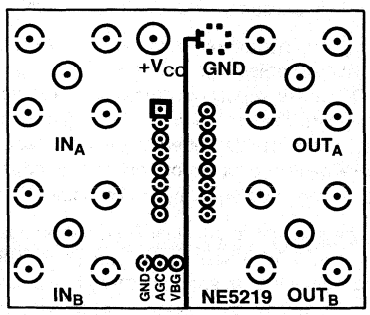
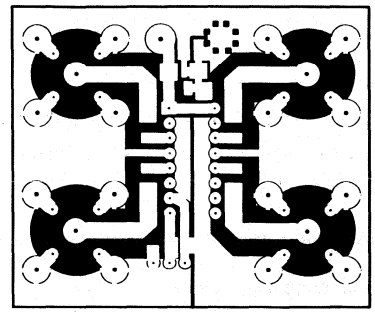


Figure 32. Bandgap Voltage vs Temperature and V_{CC}



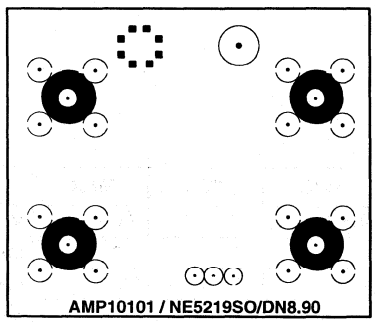
TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

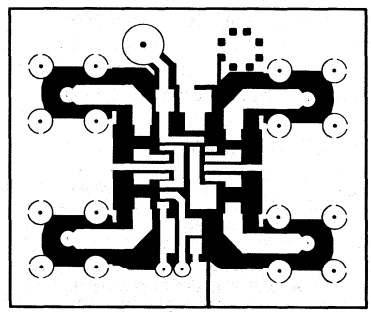
SR00306

Figure 34. VGA AC Evaluation Board Layout (DIP Package)



AMP10101 / NE5219SO/DN8.90

BOTTOM VIEW - D Package



TOP VIEW - D Package

SR00307

Figure 35. VGA AC Evaluation Board Layout (SO Package)

True logarithmic amplifier TDA8780M

FEATURES

- 72 dB true logarithmic dynamic range
- Small-signal gain-adjustment facility
- Constant limiting output voltage
- Temperature and DC power supply voltage independent
- Easy interfacing to analog-to-digital converters
- Output DC level shift facility.

APPLICATIONS

- Dynamic range compression
- IF signal dynamic range reduction in digital receivers
- Compression receivers.

GENERAL DESCRIPTION

The TDA8780M is a true logarithmic amplifier intended for dynamic range reduction of IF signals at 10.7 MHz in digital radio receivers. It offers true logarithmic characteristics over a 72 dB input dynamic range, has a small-signal gain-adjustment facility and a constant limiting output voltage for large input levels.

A unique feature is the smooth "changeover" from linear operation (inputs less than 60 μV) to logarithmic mode.

The device is manufactured in an advanced BiCMOS process which enables high performance being obtained with low DC power supply consumption. The true logarithmic amplifier can be driven by single-ended or differential inputs. The DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors, which define the low-frequency cut-off point.

The performance of the amplifier is stabilized against temperature and DC power supply variations. The differential output is converted internally to a single-ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. A power-down facility allows the circuit to be disabled from a control input.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	4.5	5.0	5.5	V
I_P	supply current	–	–	6.7	mA
$I_{P(PD)}$	supply current in power-down mode	–	–	250	μA
f_{in}	operating input frequency	–	–	15	MHz
$V_{in(M)}$	dynamic logarithmic input voltage (peak value)	0.06	–	300	mV
T_{amb}	operating ambient temperature	–20	–	+75	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8780M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

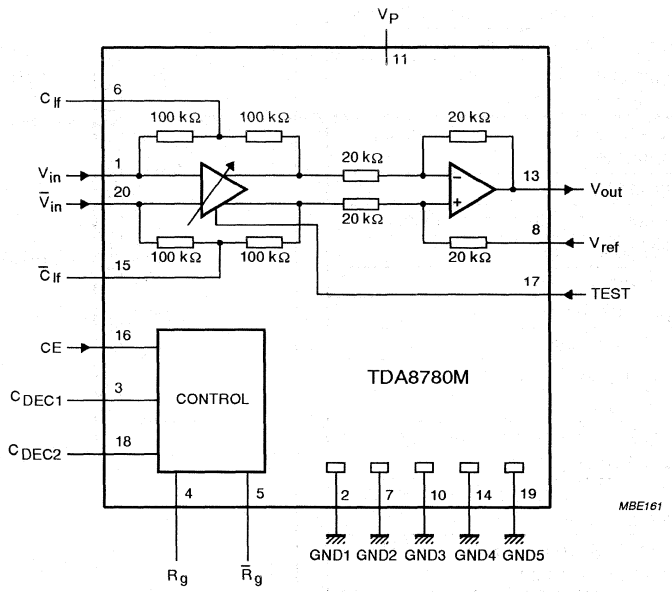


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{in}	1	signal voltage input
GND1	2	ground 1
C_{DEC1}	3	control circuit first decoupling and optional start-up capacitor connection
R_g	4	small-signal gain-setting resistor
$\overline{R}_g$	5	small-signal complementary gain-setting resistor
C_{lf}	6	low-frequency cut-off point setting capacitor
GND2	7	ground 2
V_{ref}	8	external reference voltage input
n.c.	9	not connected
GND3	10	ground 3 (main ground)
V_P	11	power supply
n.c.	12	not connected
V_{out}	13	true logarithmic voltage output
GND4	14	ground 4
$\overline{C}_{lf}$	15	complementary low-frequency cut-off point setting capacitor
CE	16	TTL-level-compatible circuit enable input (active HIGH)
TEST	17	test input; connected to ground in normal operation
C_{DEC2}	18	control circuit second decoupling and optional start-up capacitor
GND5	19	ground 5
$\overline{V}_{in}$	20	complementary signal voltage input

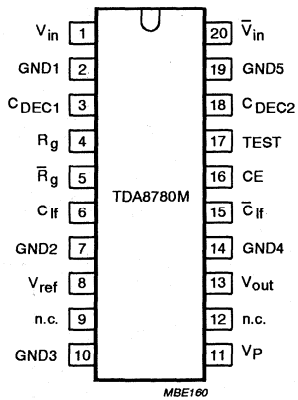


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

A true logarithmic amplifier can be realized from a cascade of similar stages each stage consisting of a pair of amplifiers whose inputs and outputs are connected in parallel. One of these amplifiers can be formed by an undegenerated long-tailed pair which provides high gain but limited linear input signal-handling capability. The other amplifier can be formed by a degenerated long-tailed pair which provides a gain of unity and a much larger linear input signal-handling capability.

The overall cascade amplifies very small input signals but, once these reach the level at which the undegenerated long-tailed pair in the last stage is at the limit of its linear signal-handling capability, the output voltage becomes logarithmically dependent on the input signal level. This behaviour continues until the input signal reaches the level at which undegenerated long-tailed pair in the first stage is at the limit of its linear input signal-handling capability. The transfer characteristic beyond this point then depends on the exact configuration of the degenerated long-tailed pair in the first stage.

Five stages are used in the TDA8780M to provide a 72 dB true logarithmic dynamic range. The DC bias current in the undegenerated long-tailed pair in the first stage is made externally adjustable, using an off-chip resistor, to provide a small-signal gain adjustment facility. The small signal gain defined by this resistor is valid when the IC is operating in the "linear" mode, for input signals typically less than 60 μV.

A high-level limiter is inserted between the first and second stages to provide a constant limiting output voltage which is essentially independent of the value of the gain setting resistor. These stages can be driven by single-ended or differential inputs. The DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance is stabilized against temperature and DC power supply variations. The input to the true logarithmic amplifier is protected against damage due to excessive differential input signals by diodes.

The differential output from the true logarithmic amplifier is converted internally to a single-ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. The output is capable of driving loads down to 10 kΩ. The limiting output voltage and the output drive capability have been chosen to facilitate interfacing to analog-to-digital converters. A major part of the DC power supply current consumption of the device is associated with provision of this output drive capability. The DC power supply consumption is significantly less when the device is driving smaller loads.

A power-down facility allows the circuit to be disabled from a TTL-level compatible control input.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	−0.3	+6.0	V
V_i	input voltage all other pins referenced to ground	−0.3	V_P + 0.3	V
T_{amb}	operating ambient temperature	−20	+75	°C
T_{stg}	IC storage temperature	−55	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

ESD in accordance with *"MIL STD 883C" - "Method 3015"*.

CHARACTERISTICS

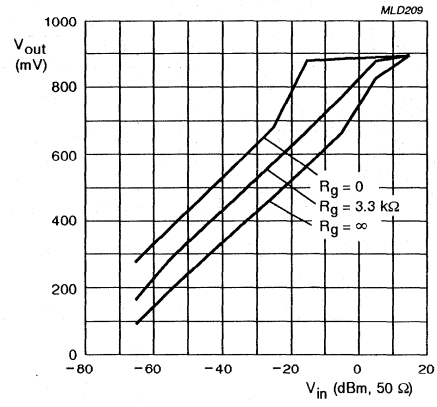
V_P = 5 V; T_{amb} = 25 °C; V_{ref} = 2.5 V; V_{in} at f_{in} = 10.7 MHz; R_g = 3.3 kΩ; output not loaded; unless otherwise specified. Signal values expressed as peak voltages mV (peak), μV (peak) or dBm (50 Ω).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current	V_P = 5.5 V; V_{in} = 1 V	–	5.4	6.7	mA
		V_P = 5.0 V; V_{in} = 1 V	–	4.9	6.2	mA
$I_{P(PD)}$	supply current in power-down	output not loaded	–	40	200	μA
		R_L = 10 kΩ	–	100	250	μA
t_{sw}	switching time	see Fig.6	–	70	–	μs
Reference input (pin 8)						
V_{ref}	external reference voltage input		2.0	2.5	V_P − 2.0	V
R_{ref}	external reference resistance input		–	40	–	kΩ
Inputs (pins 1 and 20)						
f_{in}	input operating frequency	note 1	1.0	10.7	15	MHz
R_{diff}	differential small-signal input resistance	V_{in} = 10 mV	–	10	–	kΩ
C_{diff}	differential input capacitance		–	2	–	pF
$V_{in(min)}$	input voltage level at start of logarithmic characteristic		–	60	–	μV
$V_{in(top)}$	input voltage level at top end of logarithmic characteristic		–	300	–	mV
$V_{in(max)}$	maximum input signal voltage	input protection diodes not conducting	–	1	–	V
ΔV_{in}	input voltage level spread across logarithmic range	over whole T_{amb} and V_P range	–	±2.5	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output (pin 13)						
V_{os}	DC offset voltage (V_{out} to V_{ref})	no input signal	−60	+40	+140	mV
V_{out}	output voltage level across logarithmic range	V_{in} = 60 μV (−71.4 dBm)	45	80	115	mV
		V_{in} = 400 μV (−54.9 dBm)	200	245	290	mV
		V_{in} = 3 mV (−37.4 dBm)	365	440	495	mV
		V_{in} = 25 mV (−19.0 dBm)	530	610	690	mV
		V_{in} = 200 mV (−1.0 dBm)	680	780	880	mV
		V_{in} = 300 mV (+2.6 dBm)	710	820	930	mV
		R_g = 0; V_{in} = 3 mV; see Fig.3	−	530	−	mV
		R_g = ∞; V_{in} = 3 mV; see Fig.3	−	360	−	mV
$V_{out(lim)}$	limiting output voltage	V_{in} = 1 V (+13.0 dBm)	750	950	1050	mV
$\Delta\varphi$	spread in output phase transfer characteristic across logarithmic range		−	15	−	
f_{lf}	low frequency cut-off point (3 dB)	see Fig.6	−	−	0.1	MHz
G_{flat}	gain flatness at 1 to 15 MHz	V_{in} = 10 mV	−	0.5	1.5	dB
R_{13}	output resistance		−	150	−	Ω
Logic input (pin 16)						
V_{IL}	LOW level input voltage		0	−	0.8	V
V_{IH}	HIGH level input voltage		2	−	V_P	V
I_{LI}	input leakage current	V_{IL} = 0 to V_P	−1	−	+1	μA

Note

1. With some changes in application the lower input frequency limit can be lowered.



V_{CC} = 5 V; V_{ref} = 2.5 V; f_{in} = 10 MHz; T_{amb} = 25 °C.

Fig.3 Output voltage dependence on R_g.

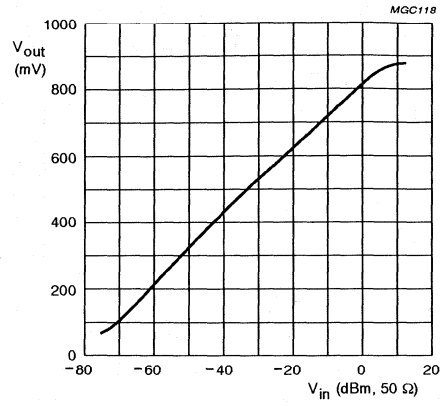


Fig.4 Typical transfer characteristics.

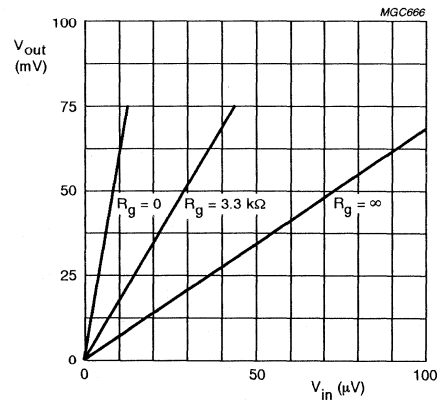


Fig.5 Typical small signal gain.

APPLICATION INFORMATION

The circuit is typically connected as shown in Fig.6. The single-ended 10.7 MHz input IF signal is applied (arbitrarily) to one of the two input pins via a ceramic filter. These inputs should not be DC coupled as this will disable the on-chip feedback which sets the DC operating point of the true logarithmic amplifier. The relatively high impedance of these inputs facilitates correct termination of the ceramic filter by an off-chip resistor.

The low-frequency cut-off point is determined by the value of capacitors connected to pins 6 and 15 which decouple the overall DC feedback and the value of the input coupling capacitors. The output is coupled to an analog-to-digital converter thus the value of the voltage fed to the reference voltage input is not critical. It could be useful in other applications, where the output may be DC coupled to an alternative analog-to-digital converter, to derive this reference voltage from the centre of the input resistor chain of the analog-to-digital converter.

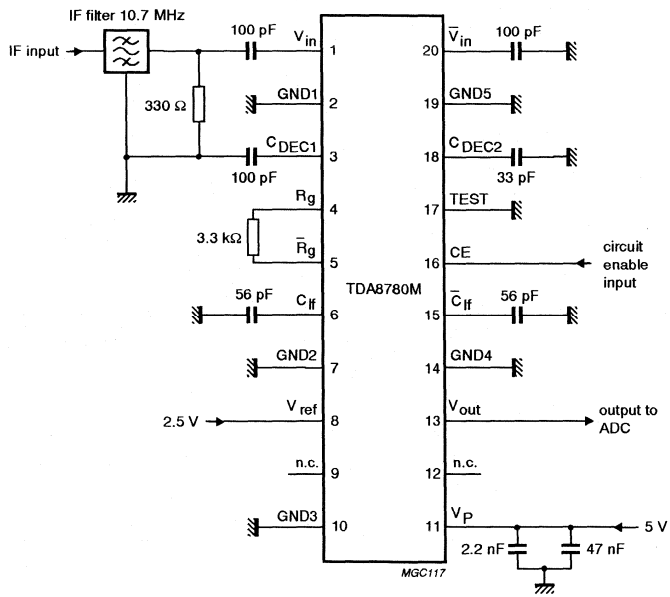


Fig.6 Typical application diagram.

Section 6
IF Systems

Wireless Communications

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THE PHILIPS FAMILY OF HIGH PERFORMANCE IF SYSTEMS

	V_{CC}	I_{CC}	Pins	Package	Input Freq	IF Freq	f_{RF}=45MHz			RSSI Range	Fast RSSI	Freq Check Pin	IF Filter Match	Output Op Amps	Feature Highlights
							Input Sensitivity	Mixer Gain	Input IP[3]						
FM IF															
NE/SA604A	4.5–8V	3.3mA@6V	16	D,N	25MHz	25MHz	0.22μV[1]	–	–	90dB	–	–	455kHz	–	–High Sensitivity
NE/SA614A	4.5–8V	3.3mA@6V	16	D,N	25MHz	25MHz	0.22μV[1]	–	–	80dB	–	–	455kHz	–	
NE/SA624	4.5–8V	3.3mA@6V	16	D,N	25MHz	25MHz	0.22μV[1]	–	–	90dB	✓	–	455kHz	–	–Wide IF BW
Mixer/FM IF															
NE/SA605	4.5–8V	5.7mA@6V	20	D,DK,N	500MHZ	25MHz	0.22μV[1]	13dB	–10dBm	90dB	–	–	455kHz	–	–High Sensitivity
NE/SA615	4.5–8V	5.7mA@6V	20	D,DK,N	500MHZ	25MHz	0.22μV[1]	13dB	–10dBm	80dB	–	–	455kHz	–	–High Input Frequency
NE/SA625	4.5–8V	5.7mA@6V	20	D,DK,N	500MHZ	25MHz	0.22μV[1]	13dB	–10dBm	90dB	✓	–	455kHz	–	
NE/SA627	4.5–8V	5.7mA@6V	20	D,DK,N	500MHZ	25MHz	0.22μV[1]	13dB	–10dBm	90dB	✓	✓	455kHz	–	–Wide IF BW
LowVoltage Mixer/FM IF															
SA606	2.7–7V	3.5mA@3V	20	D,DK,N	150MHZ	2MHz	0.31μV[1]	17dB	–9dBm	90dB	–	–	455kHz	Audio Op Amp RSSI Op Amp	–High Sensitivity –Low Power –Audio/RSSI output Op Amps –Power–Down Mode (SA626/636/639)
SA616	2.7–7V	3.5mA@3V	20	D,DK,N	150MHZ	2MHz	0.31μV[1]	17dB	–9dBm	80dB	–	–	455kHz	Audio Op Amp RSSI Op Amp	
SA607	2.7–7V	3.5mA@3V	20	D,DK,N	150MHZ	2MHz	0.31μV[1]	17dB	–9dBm	90dB	–	✓	455kHz	Audio Op Amp RSSI Op Amp	
SA617	2.7–7V	3.5mA@3V	20	D,DK,N	150MHZ	2MHz	0.31μV[1]	17dB	–9dBm	80dB	–	✓	455kHz	Audio Op Amp RSSI Op Amp	
SA608	2.7–7V	3.5mA@3V	20	D,DK,N	150MHZ	2MHz	0.31μV[1]	17dB	–9dBm	90dB	–	✓	455kHz	Audio Op Amp RSSI Op Amp	
SA626	2.7–5.5V	6.5mA@3V	20	D,DK,N	500MHZ	2MHz	0.54μV[2]	11dB[2]	–16dBm	90dB	✓	–	10.7MHz	RSSI Op Amp	
SA636	2.7–5.5V	6.5mA@3V	20	D,DK,N	500MHZ	2MHz	0.54μV[2]	11dB[2]	–16dBm	90dB	✓	–	10.7MHz	RSSI OP AMP	
SA639	2.7–5.5V	8.5mA@3V	24	DH	500MHZ	25MHz	2.24μV[4]	$12dB_4$	–12.5dBm[4]	90dB	✓	–	10.7MHz	Audio Buffered RSSI Op Amp Post–detect Amp Data Switch	
SA676	2.7–5.5V	3.5mA@3V	20	D,DK	100MHZ	25MHz	0.45μV	17dB	–10dBm	70dB	–	–	455kHz		
Low Voltage Mixer/Digital IF															
SA637	2.7–5.5V	3.5mA@3V	20	D,DK	200MHZ	2MHz	$\frac{-117dBm[3]}{0.31\mu V}$	15dB	–10dBm	90dB	✓		455kHz	RSSI Op Amp	

Part	Description	V_{CC}	I_{CC}	Pins	Pkg	Input Freq	Gain (power)	Noise Figure	Input IP3	1dB Comp	Input Imped.	Out Imped.	Features
IF Transceiver													
SA1638	R_X: IF amp+I/Q mixers+buffers T_X: I/Q Mixers+buffers+IF Synthesizer	3.3–5.5V	R_X: 16mA T_X: 19.5mA	48	BE	70–400MHz				In–Band –53dBv Other –47dBv		1kΩ	–Internal IF PLL –Tunable IF BW=50–850 kHz –Two DC regulators
SA1630	R_X: 74dB VGA+I/Q mixers+buffers T_X: I/Q mixers+buffers	2.7–5.5V	Rx: 33.5mA Tx: 26.5mA	48	BE	70–400MHz							–Internal IF PLL 74dB VGA

Temperature Ranges
NE: 0 to 70°C
SA: –40 to +85°C

Package Descriptions
D: Small Outline–16
Small Outline–20
DK: Shrink Small Outline Package (SSOP)–20
N: Dual In–Line Plastic–16, 20

IF Filter Match
455kHz=1.5kΩ
10.7MHz=330Ω

High performance low power FM IF system NE/SA604A

DESCRIPTION

The NE/SA604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA604A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA604A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA604A meets cellular radio specifications

PIN CONFIGURATION

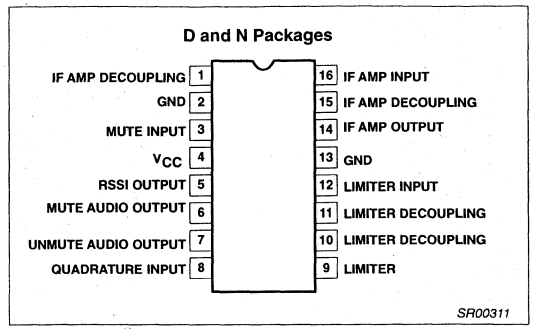


Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE604AN	SOT28-4
16-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to +70°C	NE604AD	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA604AN	SOT28-4
16-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA604AD	SOT109-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE604A SA604A	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

BLOCK DIAGRAM

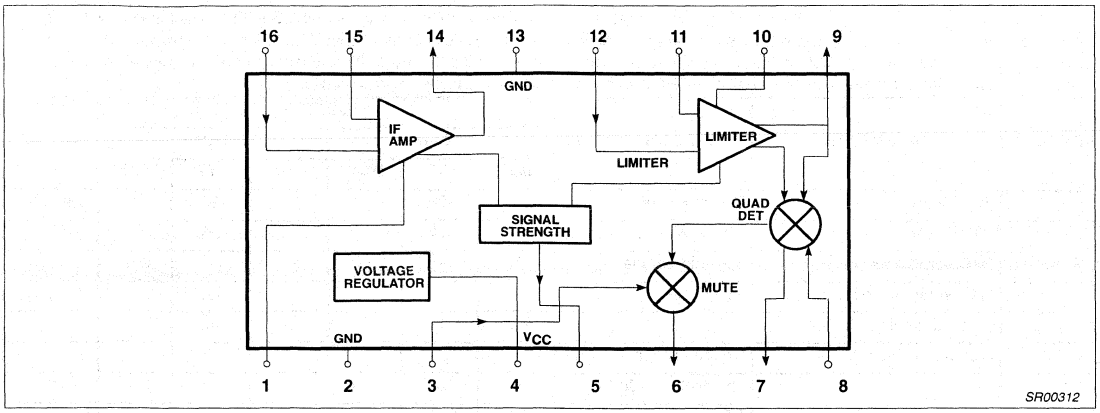


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

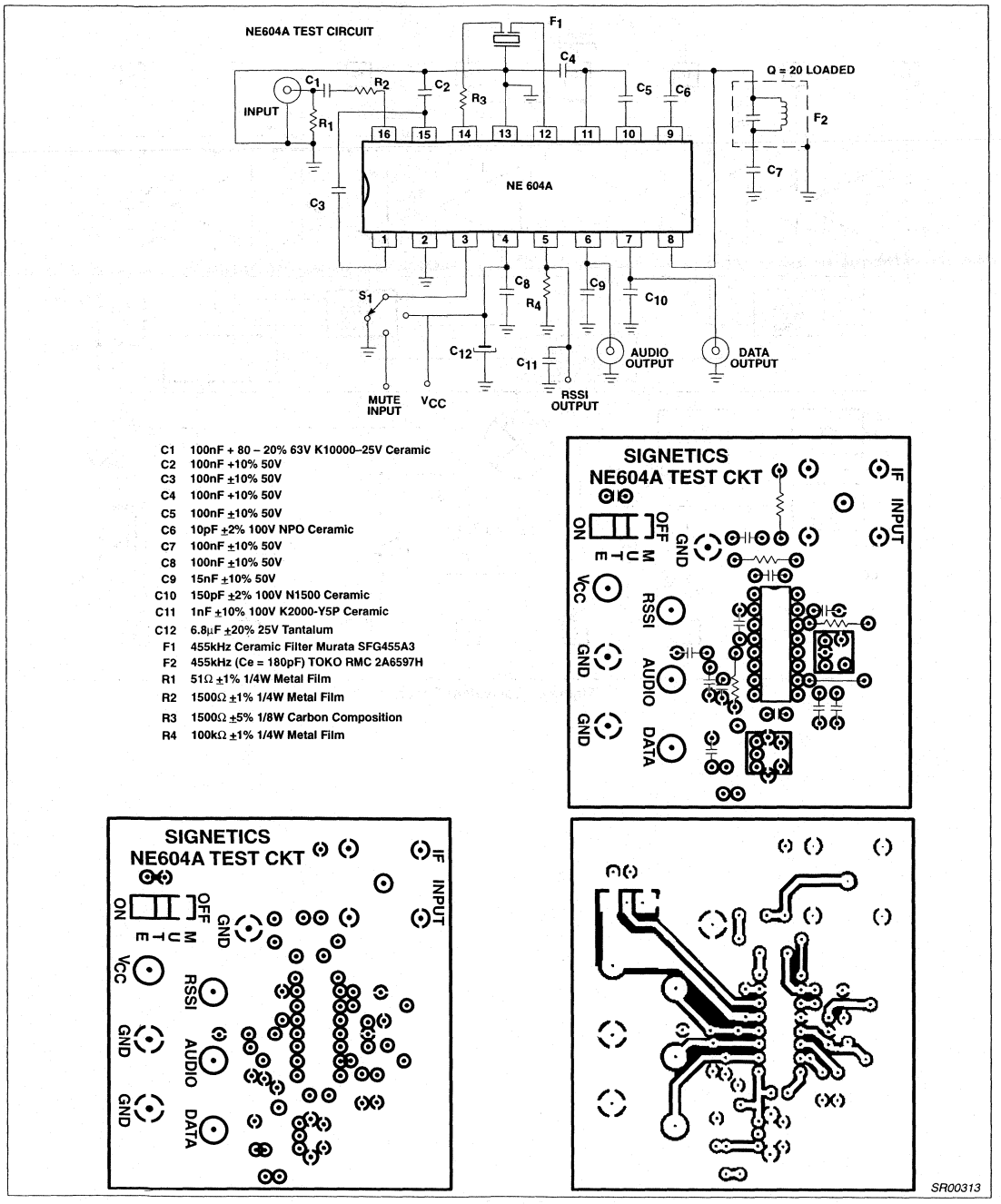
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92			-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530			530		mV_{RMS}
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = -118dBm	0	160	550	0	160	650	mV
		RF level = -68dBm	2.0	2.65	3.0	1.9	2.65	3.1	V
		RF level = -18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI range	R_4 = 100k (Pin 5)		90			90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

NOTE:

1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE604 (50)	NE604A (1.5k)/NE605 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

The NE605 and NE604A are both derived from the same basic die. The NE605 performance plots are directly applicable to the NE604A.



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film

Figure 3. NE/SA604A Test Circuit

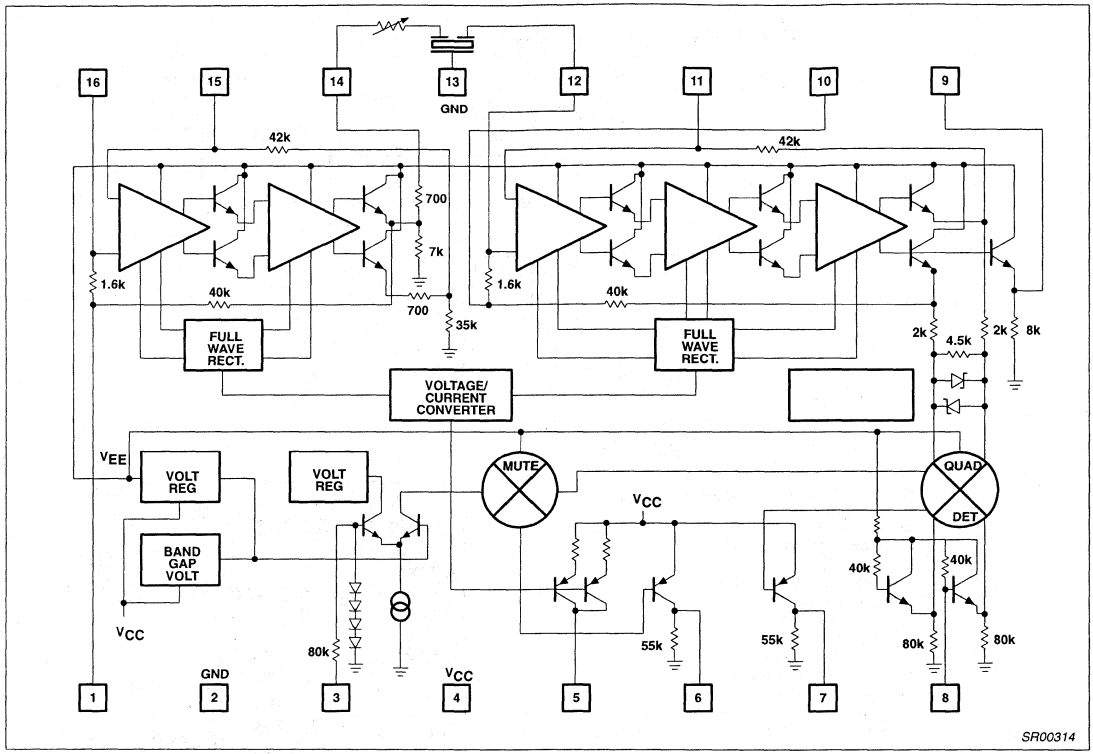


Figure 4. Equivalent Circuit

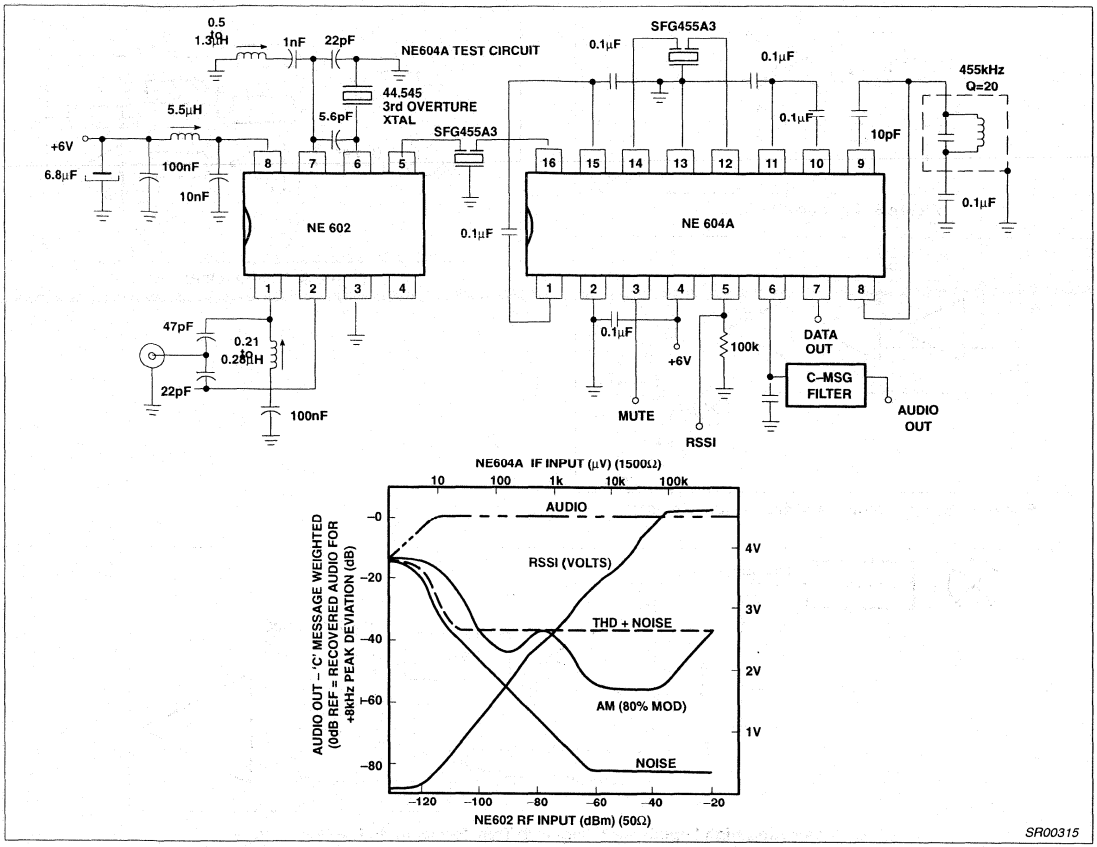


Figure 5. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA604A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 3. This configuration can be used as the basis for production layout.

The NE/SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 4. A typical application with 45MHz input and 455kHz IF is shown in Figure 5.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 4, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 8. Distributed feedback (capacitance, inductance and radiated fields)

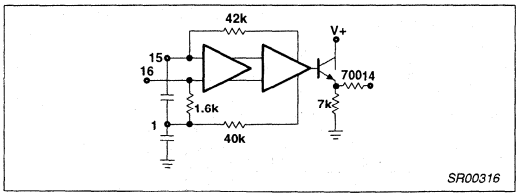


Figure 6. First Limiter Bias

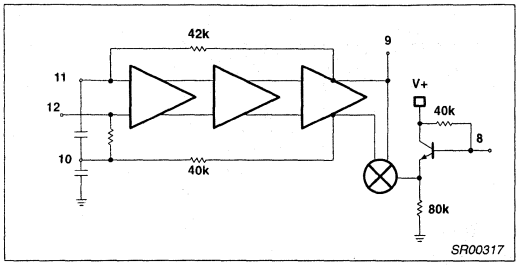


Figure 7. Second Limiter and Quadrature Detector

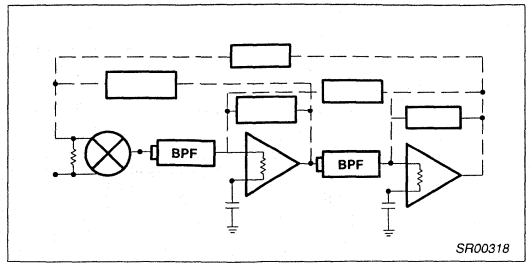


Figure 8. Feedback Paths

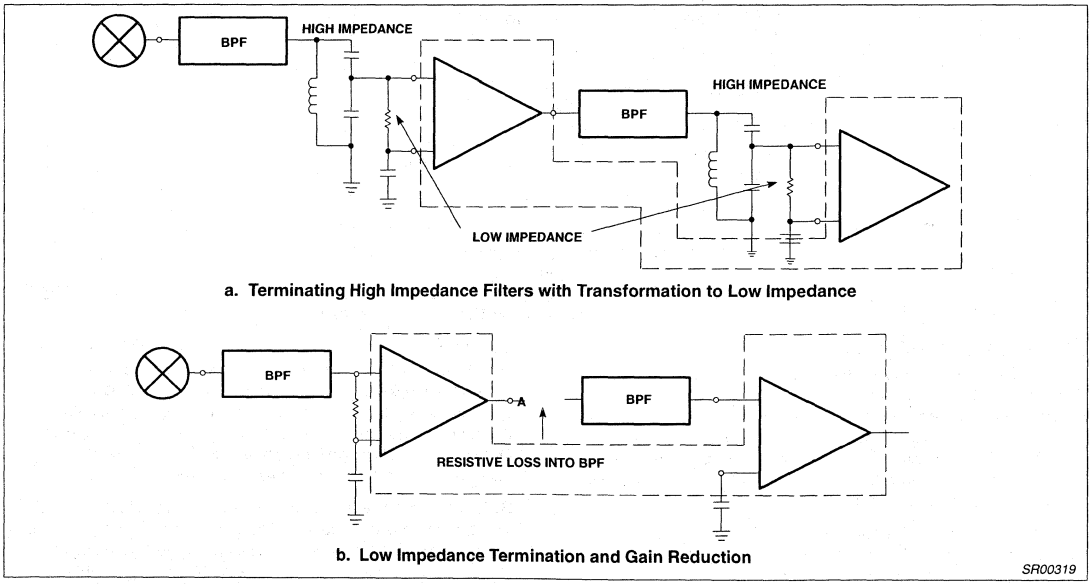


Figure 9. Practical Termination

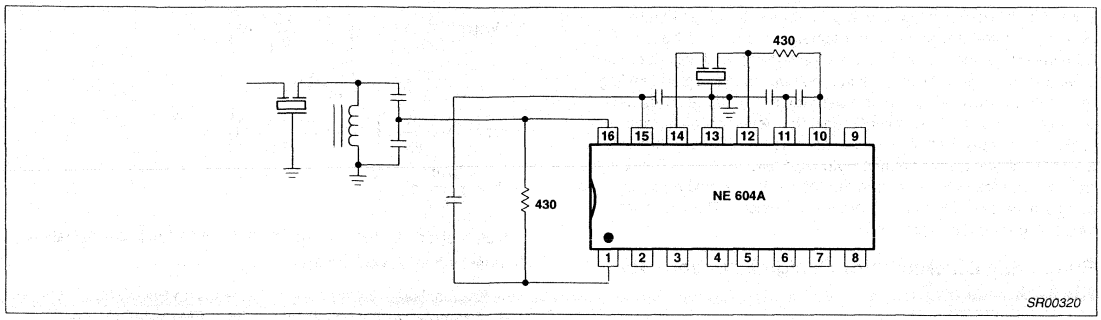


Figure 10. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 9. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE604A IF amplifiers, which is not specified, is low phase shift. The NE604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

Stability Considerations

The high gain and bandwidth of the NE604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 3, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 3 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 9 demonstrates a practical means.

As illustrated in Figure 10, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 7 shows an equivalent circuit of the NE604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 12. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE604A

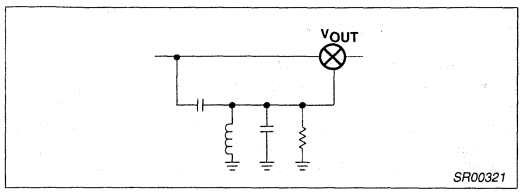


Figure 11.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 12 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \sin \omega t \Rightarrow V_O = A$ (3)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$V_{IN} \bullet V_O = A^2 \sin \omega t$ (4)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega}{\omega_1} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 12) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and $L = 0.7\text{mH}$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a C_S = 10pF and C_P = 164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of C_S = 1pF is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output

differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 5) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

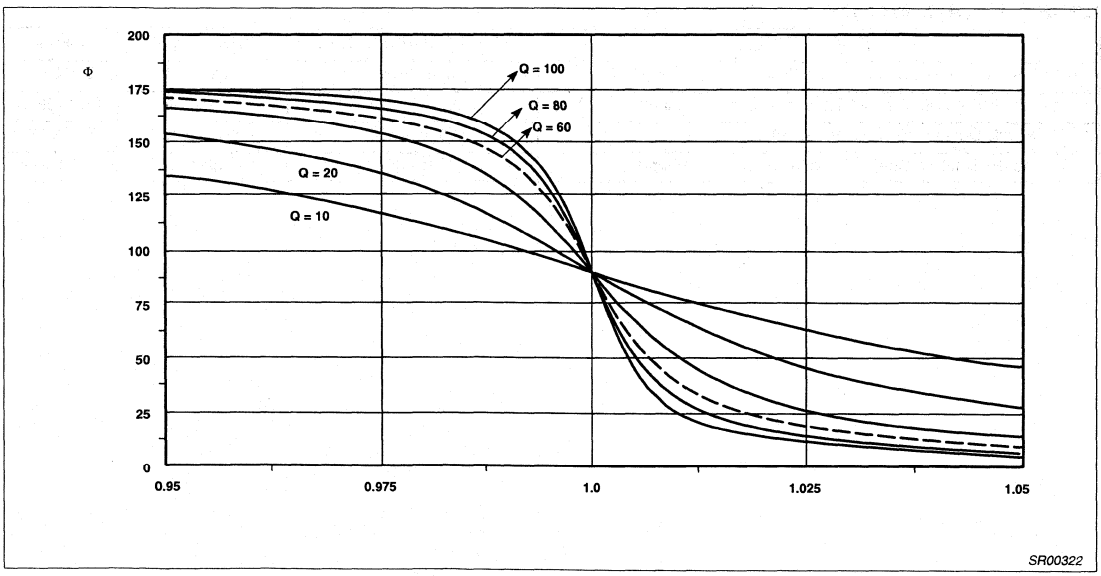


Figure 12. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

Low power FM IF system | NE/SA614A

DESCRIPTION

The NE/SA614A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA614A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA614A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA614A meets cellular radio specifications

PIN CONFIGURATION

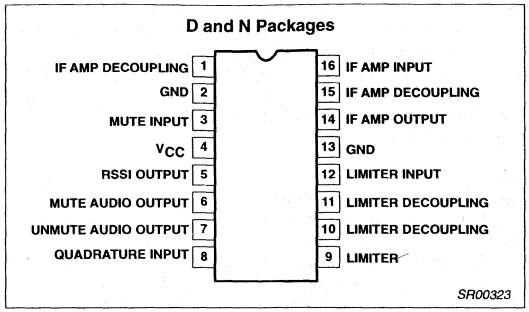


Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE614AN	SOT28-4
16-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to +70°C	NE614AD	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA614AN	SOT28-4
16-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA614AD	SOT109-1

BLOCK DIAGRAM

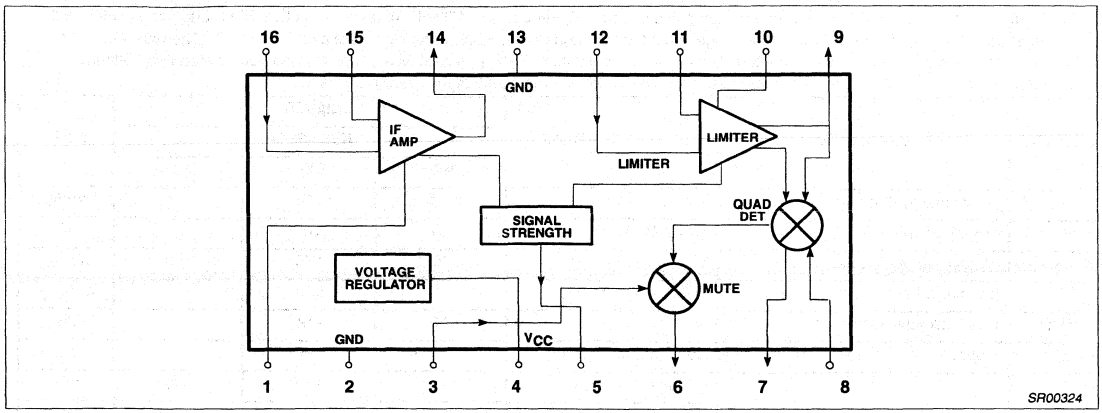


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE614A SA614A	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE614A			SA614A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

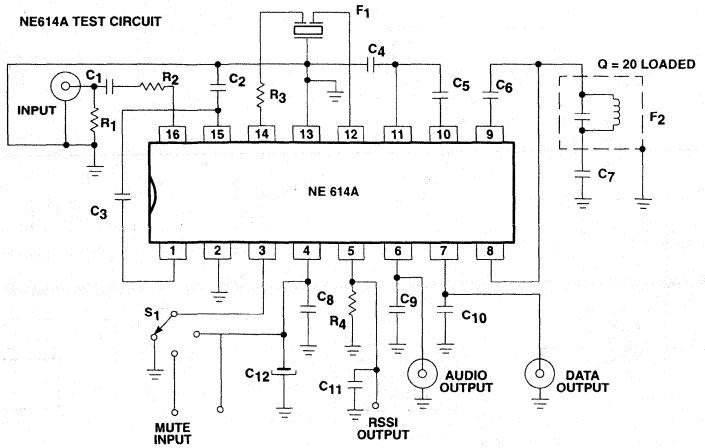
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA614A			
			MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92		dBm/50Ω
	AM rejection	80% AM 1kHz	25	33		dB
	Recovered audio level	15nF de-emphasis	60	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530		mV_{RMS}
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	RSSI output[1]	RF level = -118dBm	0	160	800	mV
		RF level = -68dBm	1.7	2.50	3.3	V
		RF level = -18dBm	3.6	4.80	5.8	V
	RSSI range	R_4 = 100k (Pin 5)		80		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±2.0		dB
	IF input impedance		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ

NOTE:

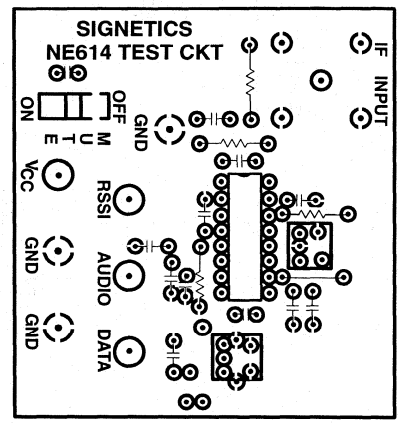
1. NE614A data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

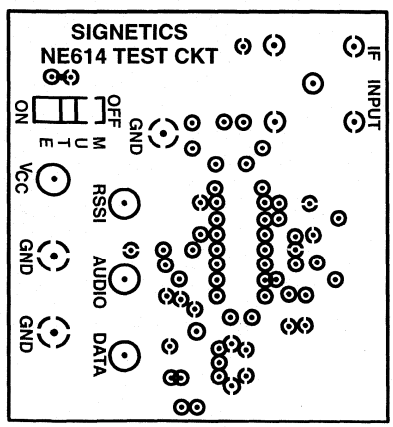
NE614A (50)	NE614A (1.5k)/NE615 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

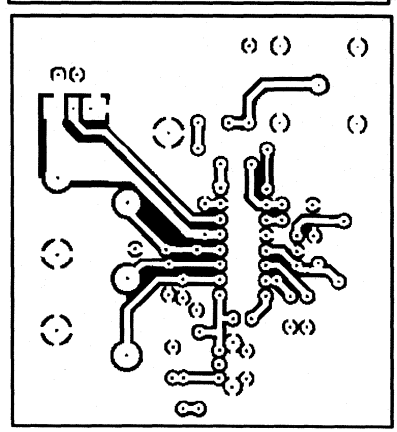
The NE615 and NE614A are both derived from the same basic die. The NE615 performance plots are directly applicable to the NE614A.



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film







SR00325

Figure 3. NE/SA614A Test Circuit

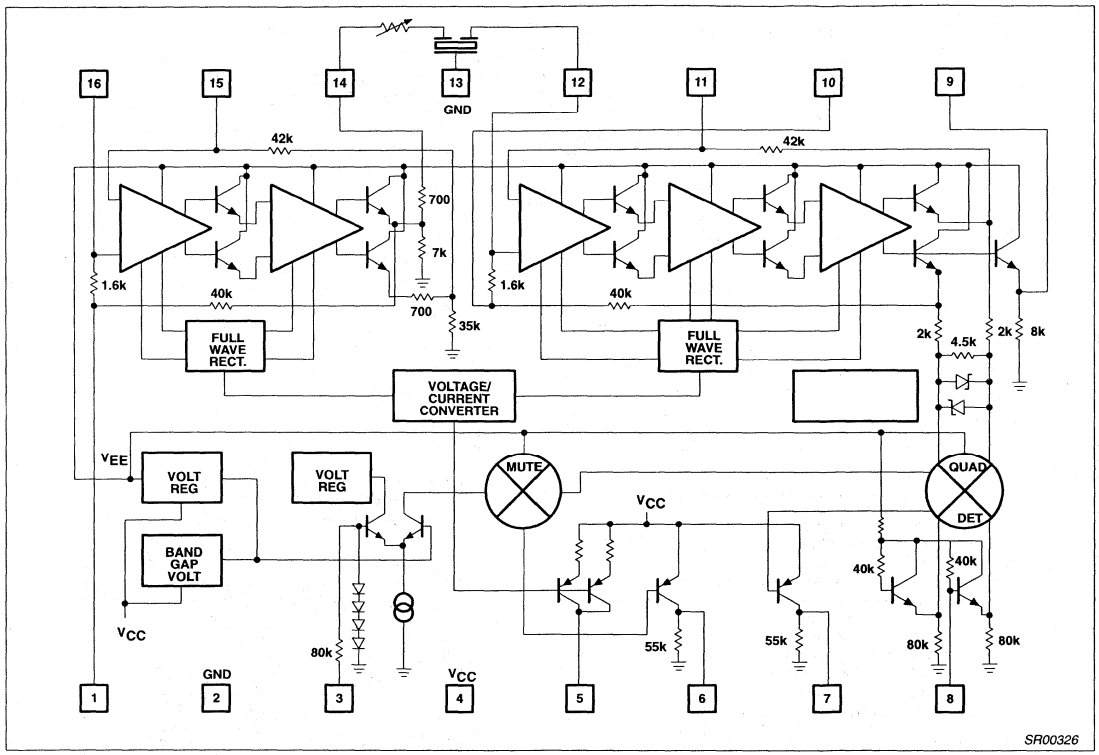


Figure 4. Equivalent Circuit

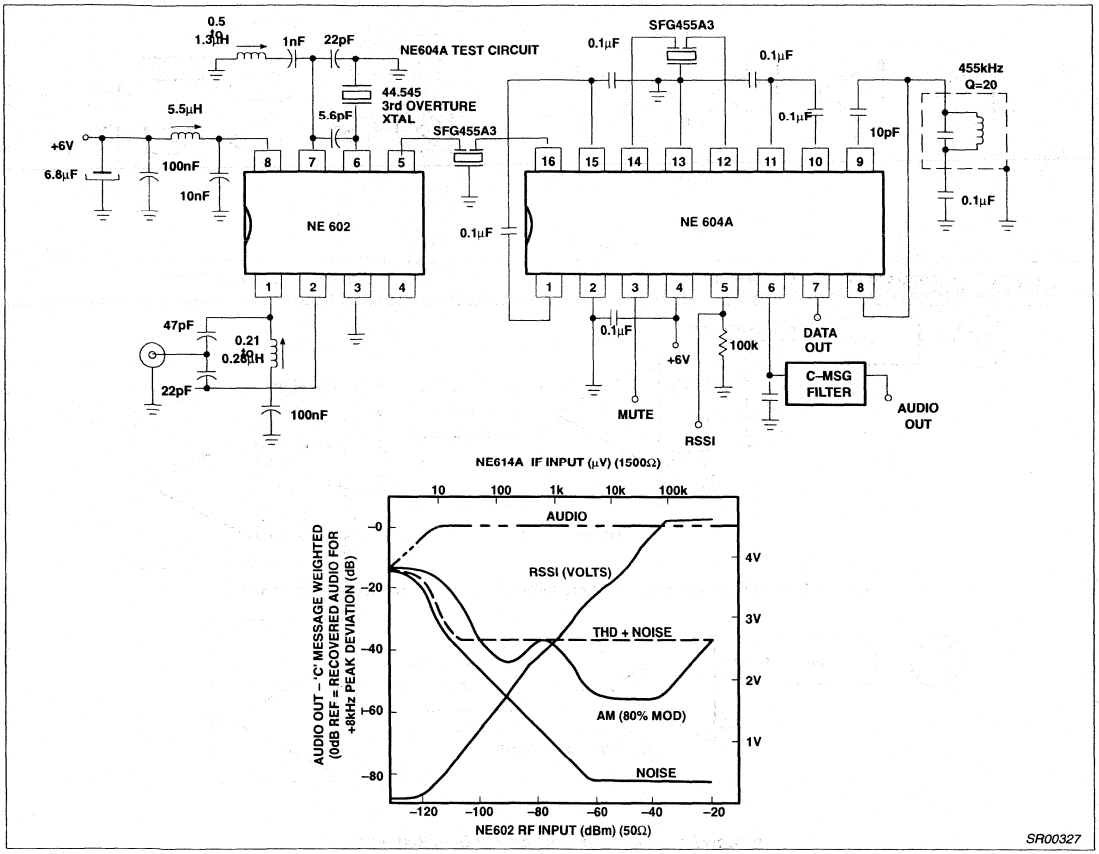


Figure 5. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA614A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA614A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 3. This configuration can be used as the basis for production layout.

The NE/SA614A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 4. A typical application with 45MHz input and 455kHz IF is shown in Figure 5.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 4, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

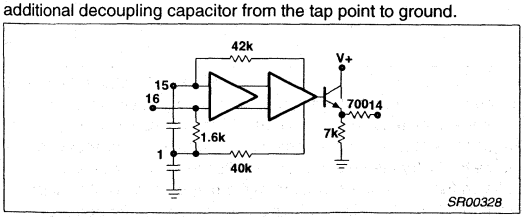


Figure 6. First Limiter Bias

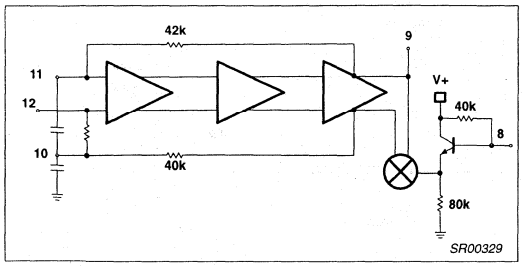


Figure 7. Second Limiter and Quadrature Detector

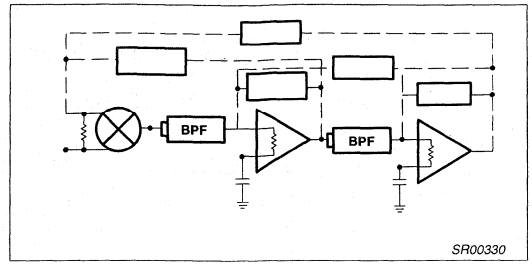


Figure 8. Feedback Paths

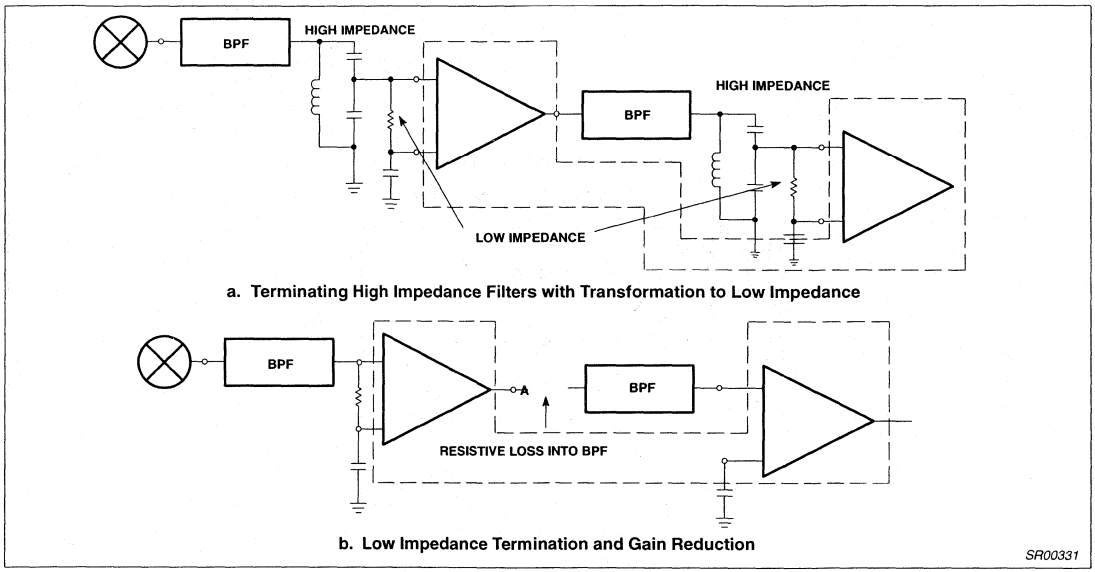


Figure 9. Practical Termination

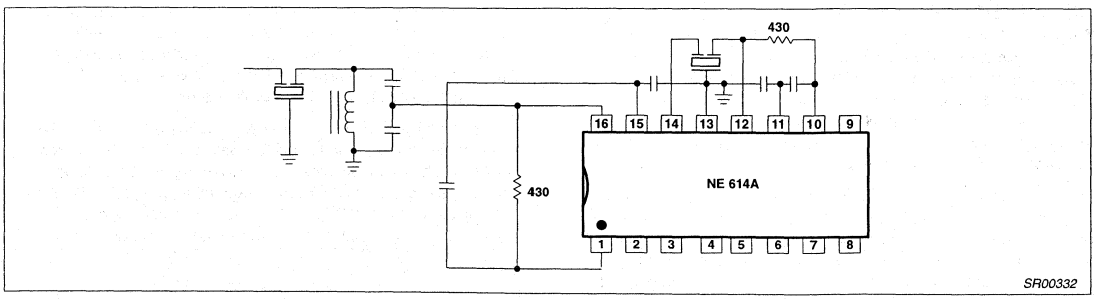


Figure 10. Crystal Input Filter with Ceramic Interstage Filter

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 8. Distributed feedback (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain

input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 9. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE614A IF amplifiers, which is not specified, is low phase shift. The NE614A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

Stability Considerations

The high gain and bandwidth of the NE614A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 3, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 3 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 9 demonstrates a practical means.

As illustrated in Figure 10, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 7 shows an equivalent circuit of the NE614A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 12. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE614A

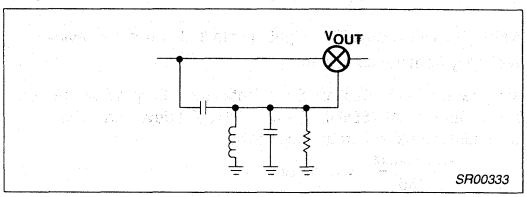


Figure 11.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1-\left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 12 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \sin \omega t \Rightarrow V_O = A$ (3)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$V_{IN} \bullet V_O = A^2 \sin \omega t$ (4)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2}A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] \quad (5)$$

$$= \frac{1}{2}A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1\frac{\omega}{\omega_1} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 12) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 614A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and $L = 0.7\text{mH}$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a C_S = 10pF and C_P = 164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of C_S = 1pF is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE614A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 5) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was

optimized at 0.22µV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE614A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

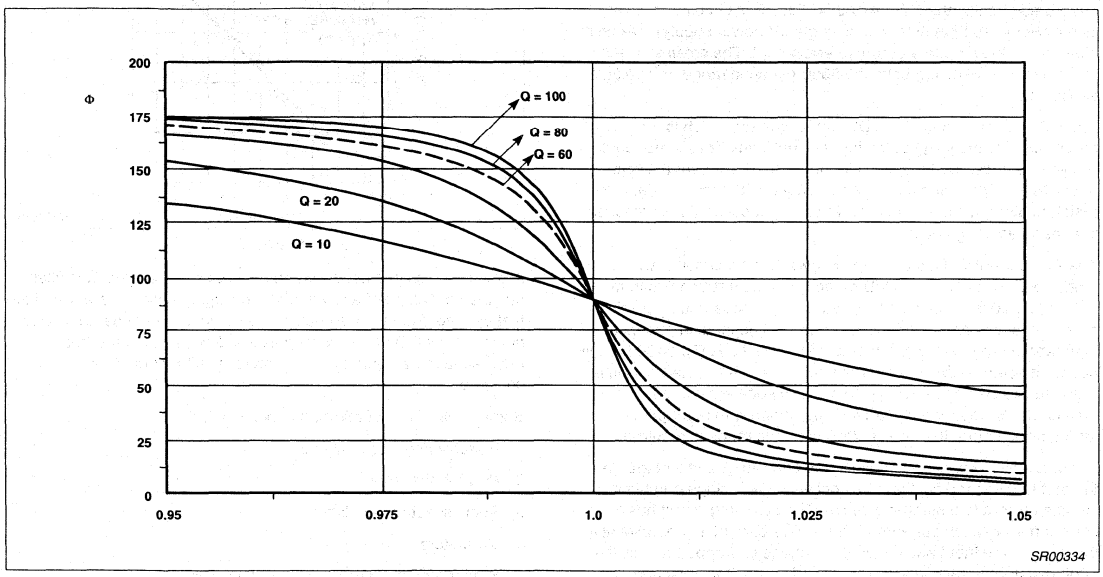


Figure 12. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_I} = 1 + \frac{\Delta\omega}{\omega_I}$

Audio decibel level detector with meter driver AN1991

Author: Robert J. Zavrel Jr.

DESCRIPTION

Although the NE604 was designed as an RF device intended for the cellular radio market, it has features which permit other design configurations. One of these features is the Received Signal Strength Indicator (RSSI). In a cellular radio, this function is necessary for continuous monitoring of the received signal strength by the radio's microcomputer. This circuit provides a logarithmic response proportional to the input signal level. The NE604 can provide this logarithmic response over an 80dB range up to a 15MHz operating frequency. This paper describes a technique which optimizes this useful function within the audio band.

A sensitive audio level indicator circuit can be constructed using two integrated circuits: the NE604 and NE532. This circuit draws very little power (less than 5mA with a single 6V power supply) making it ideal for portable battery operated equipment. The small size and low-power consumption belie the 80dB dynamic range and 10.5μV sensitivity.

The RSSI function requires a DC output voltage which is proportional to the $\log_{10}$ of the input signal level. Thus a standard 0-5 voltmeter can be linearly calibrated in decibels over a single 80dB range. The entire circuit is composed of 9 capacitors and two resistors along with the two ICs. No tuning or calibration is required in a manufacturing setting.

The Audio Input vs Output Graph shows that the circuit is within 1.5dB tolerance over the 80dB range for audio frequencies from 100Hz to 10kHz. Higher audio levels can be measured by placing an attenuator ahead of the input capacitor. The input impedance is high (about 50k), so lower impedance terminations (50 or 600Ω) will not be affected by the input impedance. If very accurate tracking is required (<0.5dB accuracy), a 40 or 50dB segment can be "selected". A range switch can then be added with appropriate attenuators if more than 40 or 50dB dynamic range is required.

There are two amplifier sections in the 604 with 2 and 3 stages in the first and second sections respectively. Each stage outputs a sample current to a summing circuit. The summing circuit has a current mirror which appears at Pin 5. This current is proportional to the $\log_{10}$ of the input audio signal. A voltage is dropped across the 100k resistor by the current, and a 0.1μF capacitor is used to bypass and filter the output signal. The 532 op amp is used as a buffer and meter driver, although a digital voltmeter could replace both the op amp and the meter shown. The rest of the capacitors are used for power supply and amplifier input bypassing.

The RC circuit between Pins 14 and 12 forms a low-pass filter which can be adjusted by changing the value of C1. Raising the capacitance will lower the cut-off frequency and also lower the zero signal output resting voltage (about 0.6V). Lowering the capacitance value will have the opposite effect with some reduction in dynamic range, but will raise the frequency response. The 2kΩ resistor value provides the near-ideal inter-stage loss for maximum RSSI linearity. C2 can also be changed. The trade-off here is between output damping and ripple. Most analog and digital metering methods will tend to cancel the effects of small or moderate ripple voltages through integration, but high ripple voltages should be avoided.

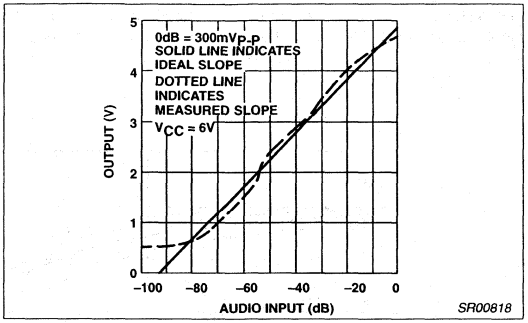


Figure 1.

A second op amp is used with an optional second filter. This filter has the advantage of a low impedance signal source by virtue of the first op amp. Again, a trade-off exists between meter damping and ripple attenuation. If very low ripple and low damping are both required, a more complex active low-pass filter should be constructed.

Some applications of this circuit might include:

1. Portable acoustic analyzer
2. Microphone tester
3. Audio spectrum analyzer
4. VU meters
5. S-meter for direct conversion radio receiver
6. Audio dynamic range testers
7. Audio analyzers (THD, noise, separation, response, etc.)

Audio decibel level detector with meter driver AN1991

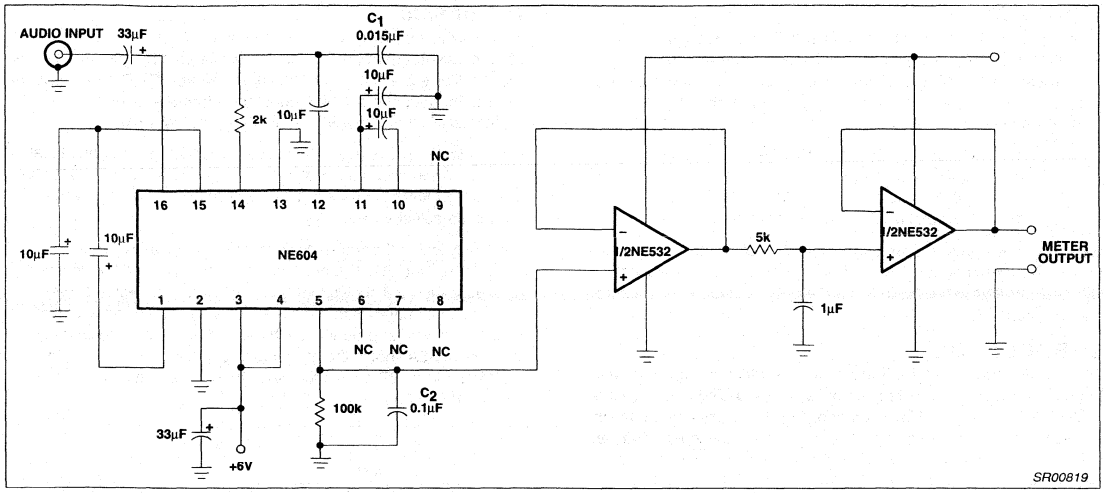


Figure 2.

High sensitivity applications of low-power RF/IF integrated circuits

AN1993

ABSTRACT

This paper discusses four high sensitivity receivers and IF (Intermediate Frequency) strips which utilize intermediate frequencies of 10.7MHz or greater. Each circuit utilizes a low-power VHF mixer and high-performance low-power IF strip. The circuit configurations are

1. 45 or 49MHz to 10.7MHz narrowband,
2. 90MHz to 21.4MHz narrowband,
3. 100MHz to 10.7MHz wideband, and
4. 152.2MHz to 10.7MHz narrowband.

Each circuit is presented with an explanation of component selection criteria, (to permit adaptation to other frequencies and bandwidths). Optional configurations for local oscillators and data demodulators are summarized.

INTRODUCTION

Traditionally, the use of 10.7MHz as an intermediate frequency has been an attractive means to accomplish reasonable image rejection in VHF/UHF receivers. However, applying significant gain at a high IF has required extensive gain stage isolation to avoid instability and very high current consumption to get adequate amplifier gain bandwidth. By enlightened application of two relatively new low power ICs, Philips Semiconductors NE602 and NE604A, it is possible to build highly producible IF strips and receivers with input frequencies to several hundred megahertz, IF frequencies of 10.7 or 21.4MHz, and sensitivity less than 2μV (in many cases less than 1μV). The Philips Semiconductors new NE605 combines the function of the NE602 and the NE604A. All of the circuits described in this paper can also be implemented with the NE605. The NE602 andNE604A were utilized for this paper to permit optimum gain stage isolation and filter location.

THE BASICS

First let's look at why it is relevant to use a 10.7 or 21.4MHz intermediate frequency. 455kHz ceramic filters offer good selectivity and small size at a low price. Why use a higher IF? The fundamental premise for the answer to this question is that the receiver architecture is a hetrodyne type as shown in Figure 1.

A pre-selector (bandpass in this case) precedes a mixer and local oscillator. An IF filter follows the mixer. The IF filter is only supposed to pass the difference (or sum) of the local oscillator (LO) frequency and the preselector frequency.

The reality is that there are always two frequencies which can combine with the LO: The pre-selector frequency and the "image" frequency. Figure 2 shows two hypothetical pre-selection curves. Both have 3dB bandwidths of 2MHz. This type of pre-selection is typical of consumer products such as cordless telephone and FM radio. Figure 2A shows the attenuation of a low side image with 10.7MHz. Figure 2B shows the very limited attenuation of the low side 455kHz image.

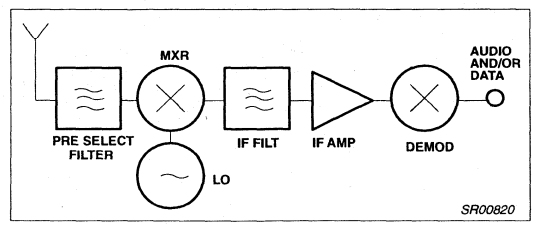


Figure 1. Basic Hetrodyne Receiver

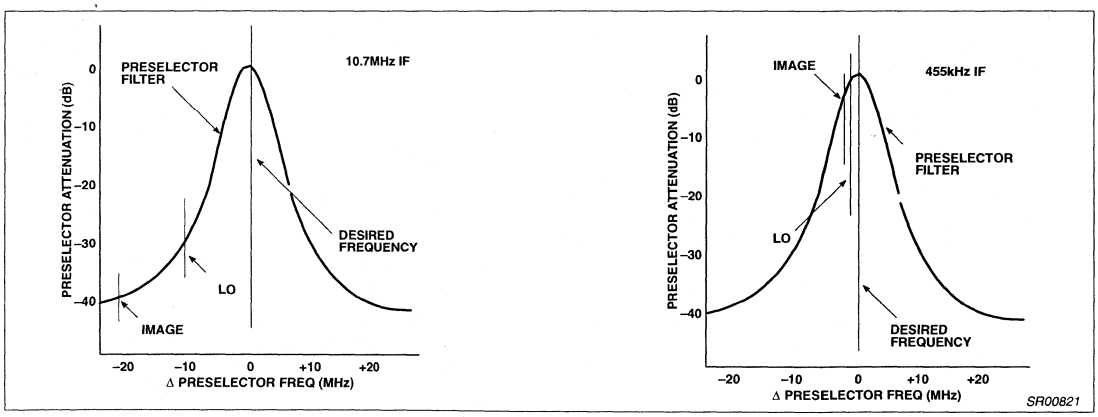


Figure 2. Effects of Preselection on Images

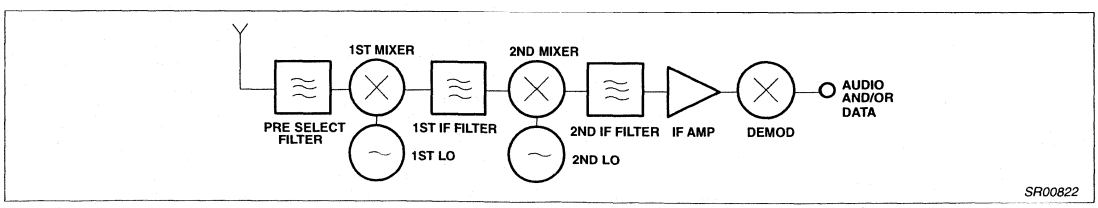


Figure 3. Dual Conversion

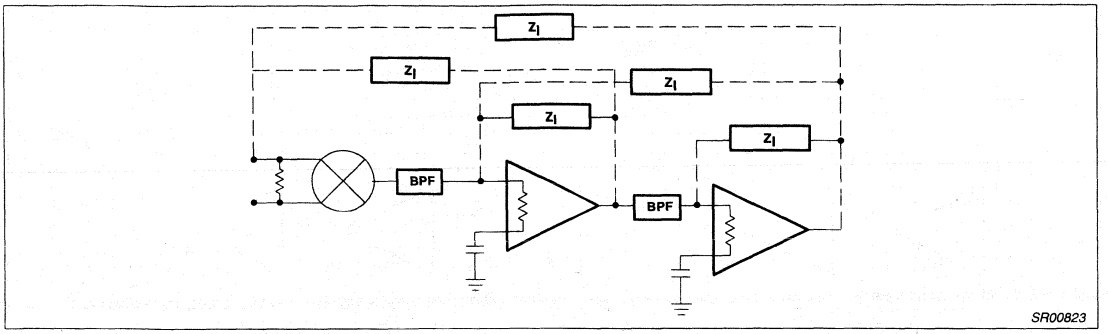


Figure 4. Feedback Paths

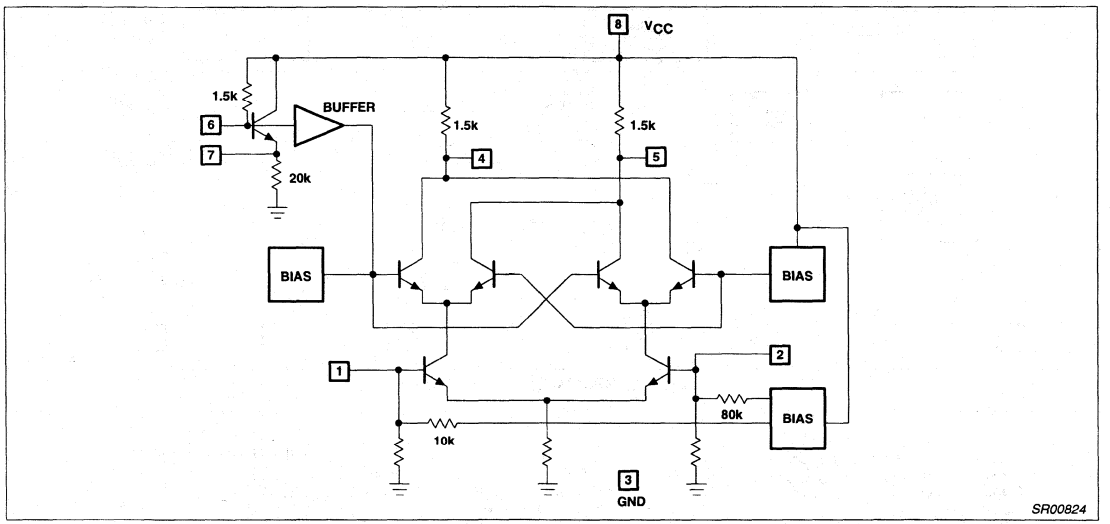


Figure 5. NE602 Equivalent Circuit

If the single conversion architecture of Figure 1 were implemented with a 455kHz IF, any interfering image would be received almost as well as the desired frequency. For this reason, dual conversion, as shown in Figure 3, has been popular.

In the application of Figure 3, the first IF must be high enough to permit the pre-selector to reject the images of the first mixer and must have a narrow enough bandwidth that the second mixer images and the intermod products due to the first mixer can be attenuated. There's more to it than that, but those are the basics. The multiple conversion hetrodyne works well, but, as Figure 3 suggests, compared to Figure 2 it is more complicated. Why, then, don't we use the approach of Figure 2?

THE PROBLEM

Historically there has been a problem: Stability! Commercially available integrated IF amplifiers have been limited to about 60dB of gain. Higher discrete gain was possible if each stage was carefully shielded and bypassed, but this can become a nightmare on a production line. With so little IF gain available, in order to receive signals of less than 10μV it was necessary to add RF gain and this, in turn, meant that the mixer must have good large signal handling capability. The RF gain added expense, the high level mixer added expense, both added to the potential for instabilities, so the multiple conversion started looking good again.

But why is instability such a problem in a high gain high IF strip? There are three basic mechanisms. First, ground and the supply line are potentially feedback mechanisms from stage-to-stage in any amplifier. Second, output pins and external components create fields which radiate back to inputs. Third, layout capacitances become feedback mechanisms. Figure 4 shows the fields and capacitances symbolically.

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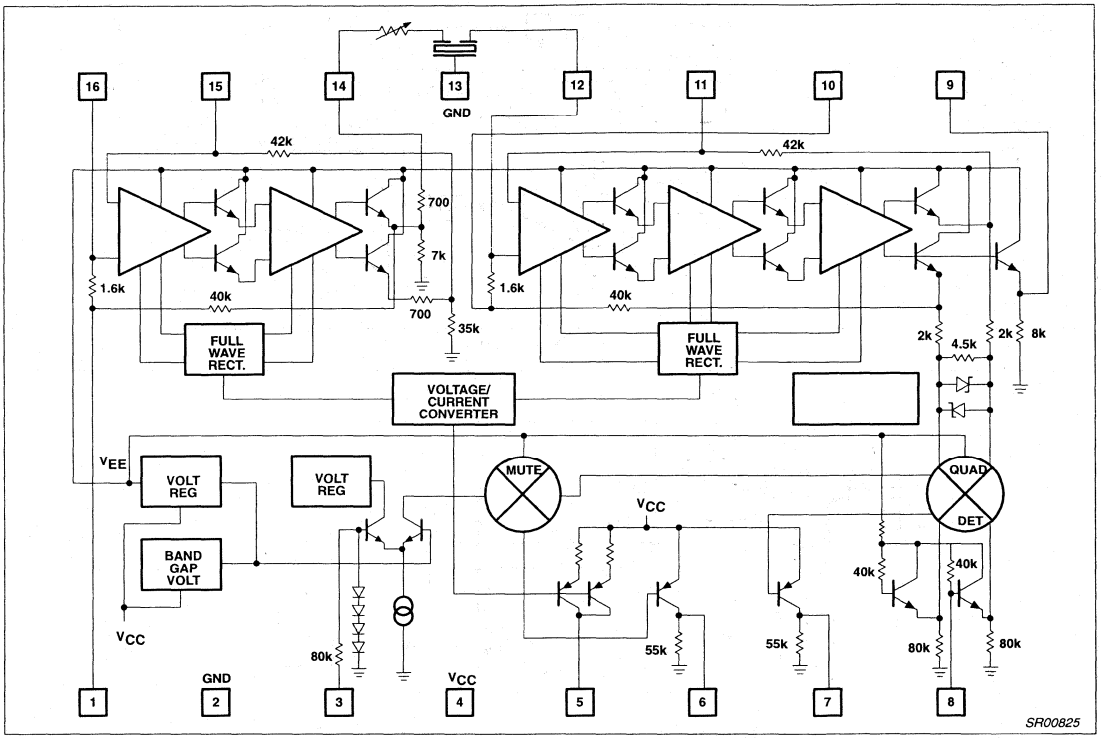

Figure 6. NE604A Equivalent Circuit

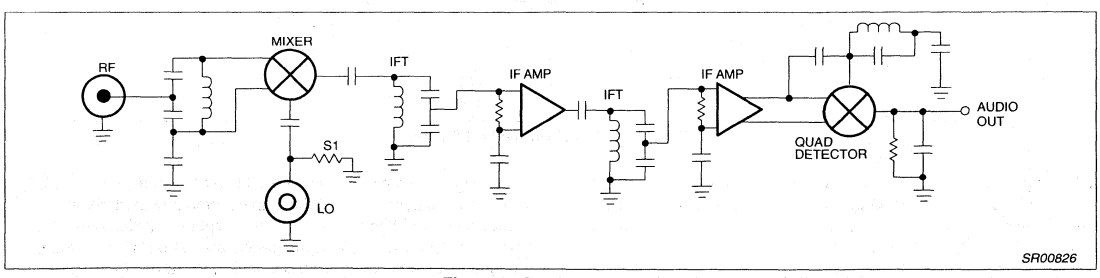

Figure 7. Symbolic Circuit

If Z_F represents the impedance associated with the circuit feedback mechanisms (stray capacitances, inductances and radiated fields), and Z_{IN} is the equivalent input impedance, a divider is created. This divider must have an attenuation factor greater than the gain of the amplifier if the amplifier is to remain stable.

- If gain is increased, the input-to-output isolation factor must be increased.
- As the frequency of the signal or amplifier bandwidth increases, the impedance of the layout capacitance decreases thereby reducing the attenuation factor.

The layout capacitance is only part of the issue. In order for traditional 10.7MHz IF amplifiers to operate with reasonable gain bandwidth, the amount of current in the amplifiers needed to be quite high. The CA3089 operates with 25mA of typical quiescent current. Any currents which are not perfectly differential must be carefully bypassed to ground. The higher the current, the more difficult the challenge. And limiter outputs and quadrature components make excellent field generators which add to the feedback scenario. The higher the current, the larger the field.

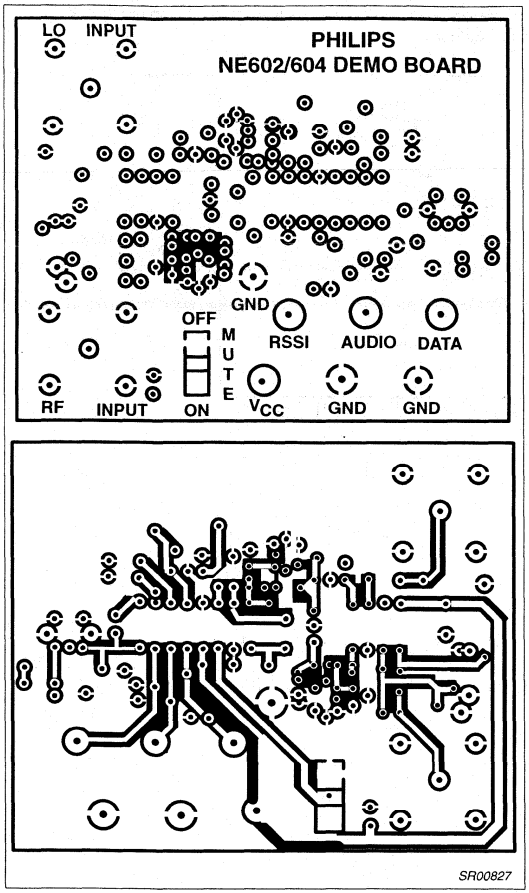

Figure 8. Circuit Board Layout

THE SOLUTION

The NE602 is a double balanced mixer suitable for input frequencies in excess of 500MHz. It draws 2.5mA of current. The NE604A is an IF strip with over 100dB of gain and a 25MHz small signal bandwidth. It draws 3.5mA of current. The circuits in this paper will demonstrate ways to take advantage of this low current and 75dB or more of the NE604A gain in receivers and IF strips that would not be possible with traditional integrated circuits. No special tricks are used, only good layout, impedance planning and gain distribution.

THE MIXER

The NE602 is a low power VHF mixer with built-in oscillator. The equivalent circuit is shown in Figure 5. The basic attributes of this mixer include conversion gain to frequencies greater than 500MHz, a noise figure of 4.6dB @ 45MHz, and a built-in oscillator which can be used up to 200MHz. LO can be injected.

For best performance with any mixer, the interface must be correct. The input impedance of the NE602 is high, typically 3kΩ in parallel with 3pF. This is not an easy match from 50Ω. In each of the examples which follow, an equivalent 50:1.5k match

was used. This compromise of noise, loss, and match yielded good results. It can be improved upon. Match to crystal filters will require special attention, but will not be given focus in this paper.

This oscillator is a single transistor with an internal emitter follower driving the mixer. For best mixer performance, the LO level needs to be approximately 220mV$_{RMS}$ at the base of the oscillator transistor (Pin 6). A number of oscillator configurations are presented at the end of this paper. In each of the prototypes for this paper, the LO source was a signal generator. Thus, a 51Ω resistor was used to terminate the signal generator. The LO is then coupled to the mixer through a DC blocking capacitor. The signal generator is set for 0dBm. The impedance at the LO input (Pin 6) is approximately 20kΩ. Thus, required power is very low, but 0dBm across 51Ω does provide the necessary 220mV$_{RMS}$.

The outputs of the NE602 are loaded with 1.5kΩ internal resistors. This makes interface to 455kHz ceramic filters very easy. Other filter types will be addressed in the examples.

THE IF STRIP

The basic functions of the NE604A are ordinary at first glance: Limiting IF, quadrature detector, signal strength meter, and mute switch. **However, the performance of each of these blocks is superb.** The IF has 100dB of gain and 25MHz bandwidth. This feature will be exploited in the examples. The signal strength indicator has a 90dB log output characteristic with very good linearity. There are two audio outputs with greater than 300kHz bandwidth (one can be muted greater than 70dB). The total supply current is typically 3.5mA. This is the other factor which permits high gain and high IF.

Figure 6 shows an equivalent circuit of the NE604A. Each of the IF amplifiers has a 1.6kΩ input impedance. The input impedance is achieved by splitting a DC feedback bias resistor. The input impedance will be manipulated in each of the examples to aid stability.

BASIC CONSIDERATIONS

In each of the circuits presented, a common layout and system methodology is used. The basic circuit is shown symbolically in Figure 7.

At the input, a frequency selective transformation from 50Ω to 1.5kΩ permits analysis of the circuit with an RF signal generator. A second generator provides LO. This generator second generator provides LO. This generator is terminated with a 51Ω resistor. The output of the mixer and the input of the first limiter are both high impedance (1.5Ω nominal). As indicated previously, the input impedance of the limiter must be low enough to attenuate feedback signals. So, the input impedance of the first limiter is modified with an external resistor. In most of the examples, a 430Ω external resistor was used to create a 330Ω input impedance (430//1.5kΩ). The first IF filter is thus designed to present 1.5kΩ to the mixer and 330Ω to the first limiter.

The same basic treatment was used between the first and second limiters. However, in each of the 10.7MHz examples, this interstage filter is not an L/C tank; it is a ceramic filter. This will be explained in the first example.

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After the second limiter, a conventional quadrature detector demodulates the FM or FSK information from the carrier and a simple low pass filter completes the demodulation process at the audio outputs.

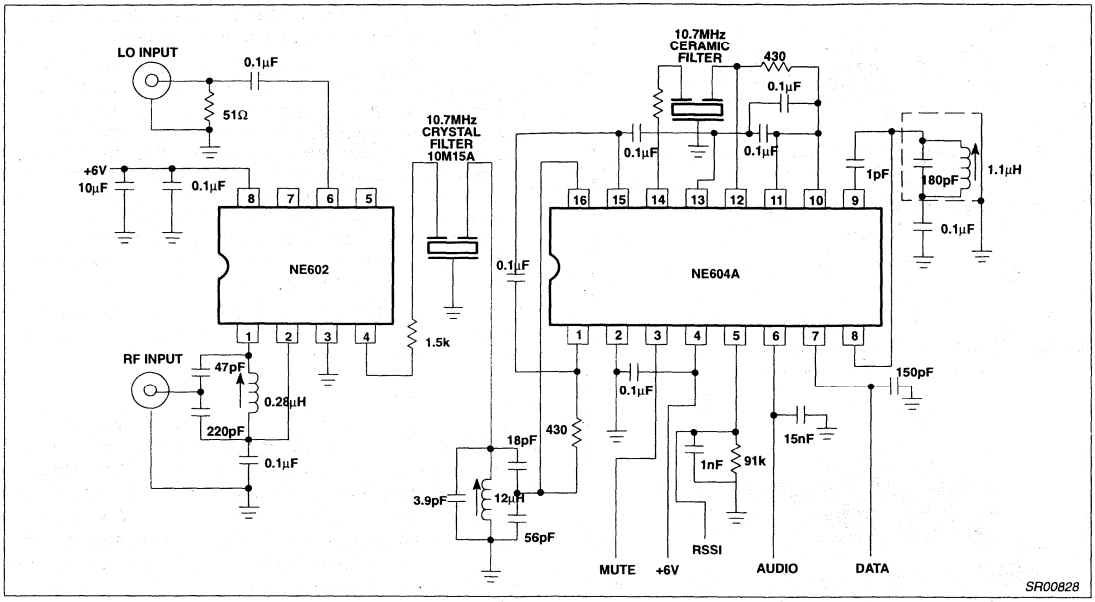

Figure 9. NE602/604A Demonstration Circuit with RF Input of 45MHz and IF of 10.7MHz ±7.5kHz

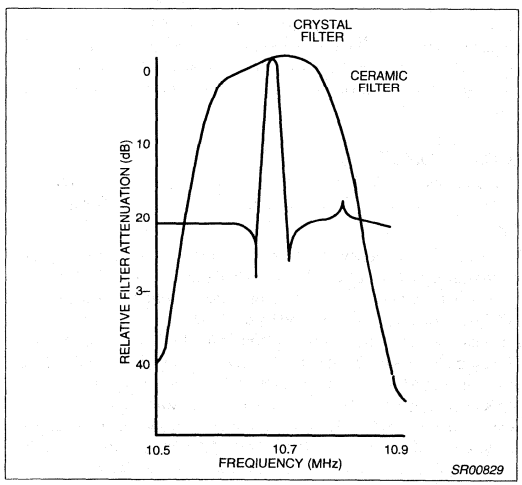

Figure 10. Passband Relationship

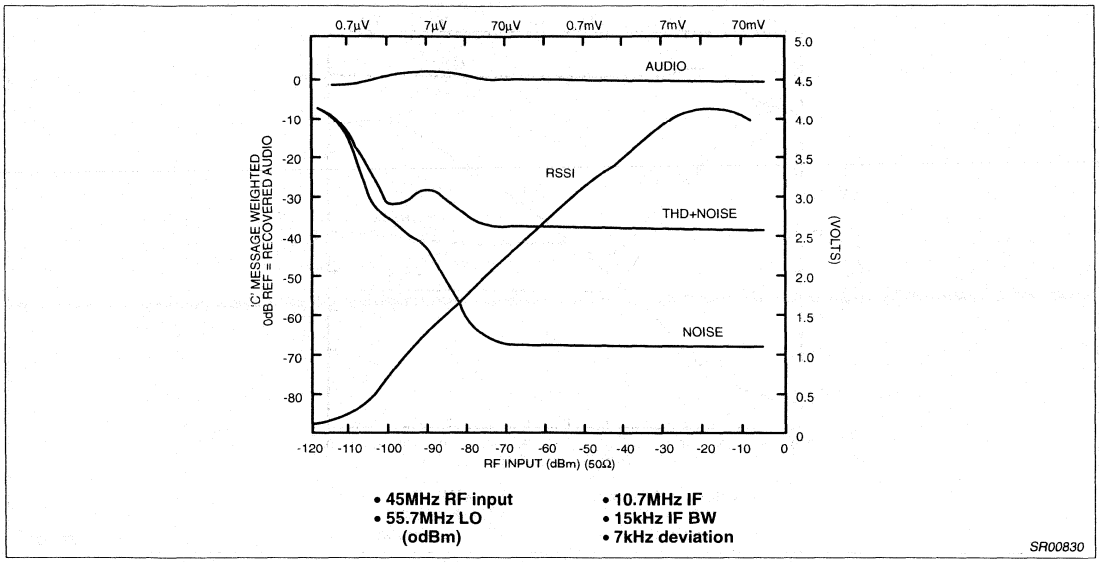

Figure 11. VHF or UHF 2nd Conversion (Narrow Band)

As mentioned, a single layout was used for each of the examples. The board artwork is shown in Figure 8. Special attention was given to: (1) Creating a maximum amount of ground plane with connection of the component side and solder side ground at locations all over the board; (2) careful attention was given to keeping a ground ring around each of the gain stages. The objective was to provide a shunt path to ground for any stray signal which might feed back to an input; (3) leads were kept short and relatively wide to minimize the potential for them to radiate or pick up stray signals; finally (and very important), (4) RF bypass was done as close as possible to supply pins and inputs, with a good (10µF) tantalum capacitor completing the system bypass.

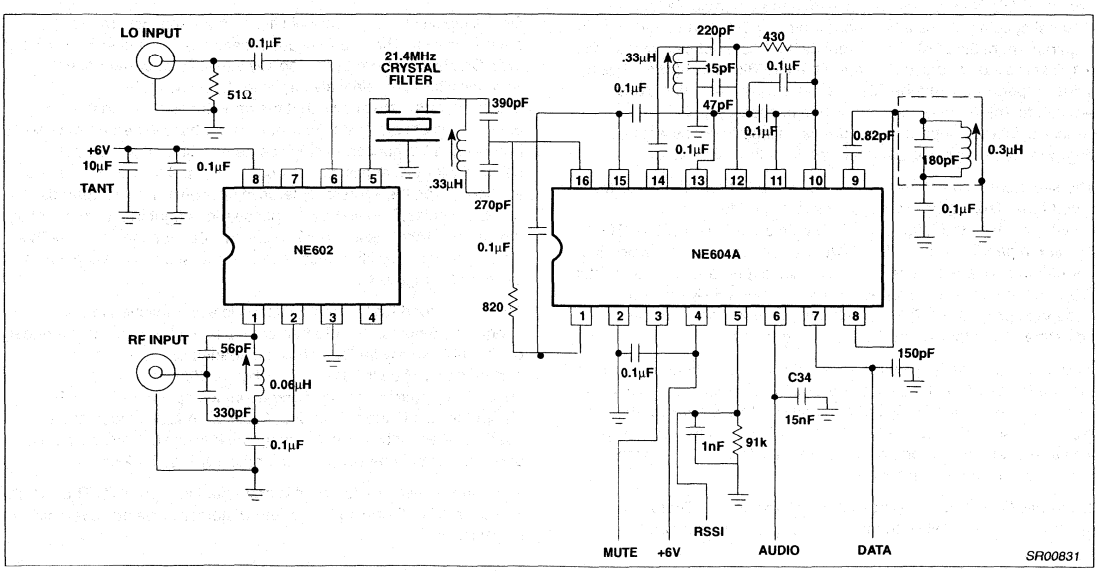

Figure 12. NE602/604A Demonstration Circuit with RF Input of 90MHz and IF of 21.4MHz ±7.5kHz

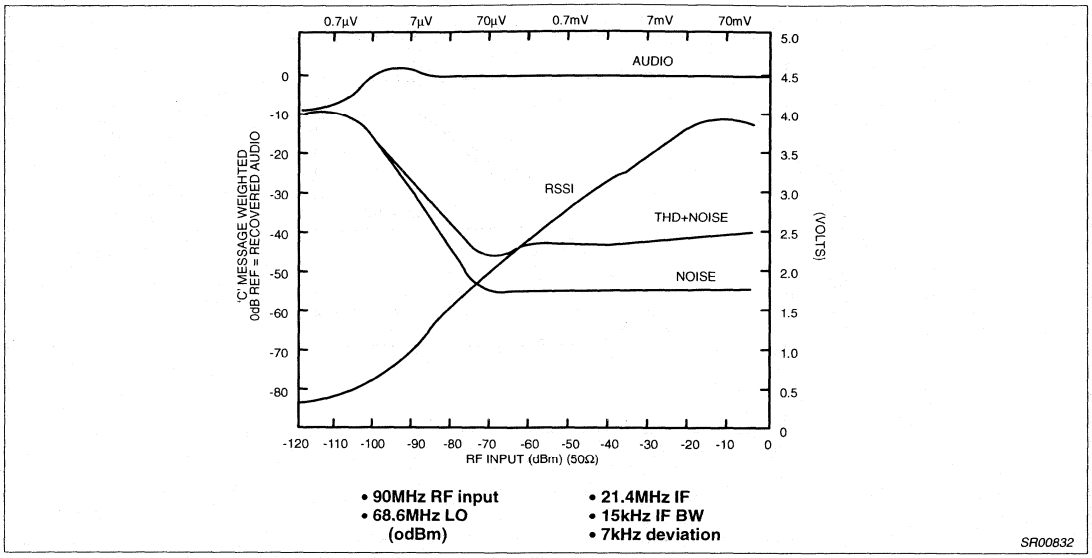

Figure 13. UHF Second Conversion (Narrow Band) or VHF Single Conversion (Narrow Band)

EXAMPLE: 45MHZ TO 10.7MHZ NARROWBAND

As a first example, consider conversion from 45MHz to 10.7MHz. There are commercially available filters for both frequencies so this is a realistic combination for a second IF in a UHF receiver. This circuit can also be applied to cordless telephone or short range communications at 46 or 49MHz. The circuit is shown in Figure 9.

The 10.7MHz filter chosen is a type commonly available for 25kHz channel spacing. It has a 3dB bandwidth of 15kHz and a termination requirement of 3kΩ/2pF. To present 3kΩ to the input side of the filter, a 1.5kΩ resistor was used between the NE602 output (which has a 1.5kΩ impedance) and the filter. Layout capacitance was close enough to 2pF that no adjustment was necessary. This series-resistance approach introduces an insertion loss which degrades the sensitivity, but it has the benefit of simplicity.

The secondary side of the crystal filter is terminated with a 10.7MHz tuned tank. The capacitor of the tank is tapped to create a transformer with the ratio for 3k:330. With the addition of the 430Ω resistor in parallel with the NE604A 1.6kΩ internal input resistor, the correct component of resistive termination is presented to the crystal filter. The inductor of the tuned load is adjusted off resonance enough to provide the 2pF capacitance needed. (Actual means of adjustment was for best audio during alignment).

If appropriate or necessary for sensitivity, the same type of tuned termination used for the secondary side of the crystal filter can also be used between the NE602 and the filter. If this is desired, the capacitors should be ratioed for 1.5k:3k. Alignment is more complex with tuned termination on both sides of the filter. This approach is demonstrated in the fourth example.

A ceramic filter is used between the first and second limiters. It is directly connected between the output of the first limiter and the input of the second limiter. Ceramic filters act much like ceramic capacitors, so direct connection between two circuit nodes with different DC levels is acceptable. At the input to the second limiter, the impedance is again reduced by the addition of a 430Ω external resistor in parallel with the internal 1.6kΩ input load resistor. This presents the 330Ω termination to the ceramic filter which the manufacturers recommend.

On the input side of the ceramic filter, no attempt was made to create a match. The output impedance of the first limiter is nominally 1kΩ. Crystal filters are tremendously sensitive to correct match. Ceramic filters are relatively forgiving. A review of the manufacturers' data shows that the attenuation factor in the passband is affected with improper match, but the degree of change is small and the passband stays centered. Since the principal selectivity for this application is from the crystal filter at the input of the first limiter, the interstage ceramic filter only has to suppress wideband noise. The first filter's passband is right in the center of the ceramic filter passband. (The crystal filter passband is less than 10% of the ceramic filter passband). This passband relationship is illustrated in Figure 10.

After the second limiter, demodulation is accomplished in the quadrature detector. Quadrature criteria is not the topic of this paper, but it is noteworthy that the choice of loaded Q will affect performance. The NE604A is specified at 455kHz using a quadrature capacitor of 10pF and a tuning capacitor of 180pF. (180pF gives a loaded Q of 20 at 455kHz). A careful look at the quadrature equations (Ref 3.) suggests that at 10.7MHz a value of about 1pF should be substituted for the 10pF at 455kHz.

The performance of this circuit is presented in Figure 11. The –12dB SINAD (ratio of Signal to Noise And Distortion) was achieved with a 0.6µV input.

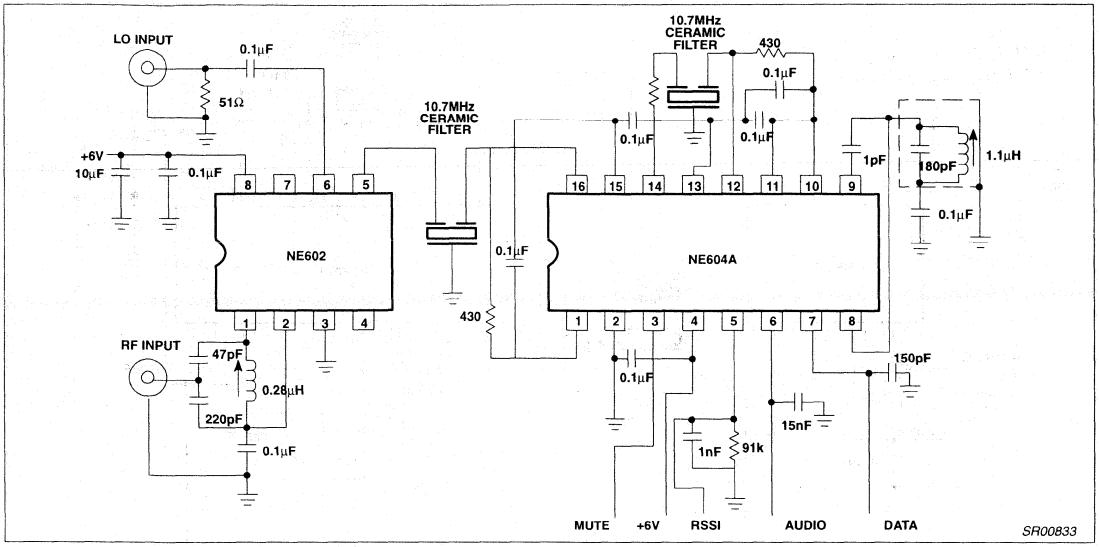

Figure 14. NE602/604A Demonstration Circuit with RF Input of ~100MHz and IF of 10.7MHz ±140kHz

EXAMPLE: 90MHZ TO 21.4MHZ NARROWBAND

This second example, like the first, used two frequencies which could represent the intermediate frequencies of a UHF receiver. This circuit can also be applied to VHF single conversion receivers if the sensitivity is appropriate. The circuit is shown in Figure 12.

Most of the fundamentals are the same as explained in the first example. The 21.4MHz crystal filter has a 1.5kΩ/2pF termination requirement so direct connection to the output of the NE602 is possible. With strays there is probably more than 2pF in this circuit, but the performance is good nonetheless. The output of the crystal filter is terminated with a tuned impedance-step-down transformer as in the previous example. Interstage filtering is accomplished with a 1kΩ:330 step-down ratio. (Remember, the output of the first limiter is 1kΩ and a 430Ω resistor has been added to make the second limiter input 330Ω). A DC blocking capacitor is needed from the output of the first limiter. The board was not laid out for an interstage transformer, so an "XACTO" knife was used to make some minor mods. Figure 13 shows the performance. The +12dB SINAD was with 1.6µV input.

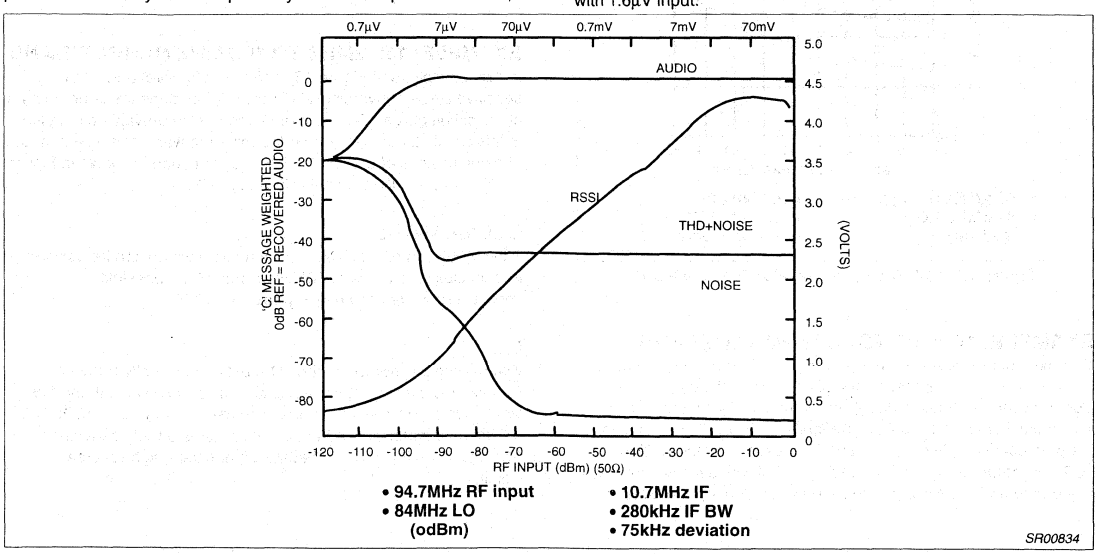

Figure 15. FM Broadcast Receiver (Wide Band)

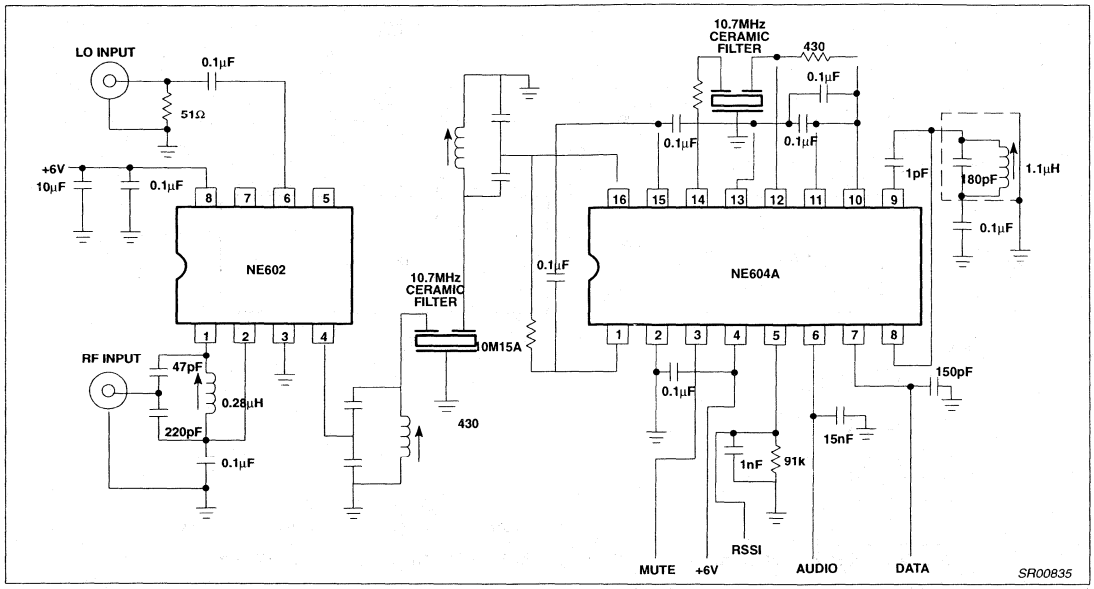

Figure 16. NE602/604A Demonstration Circuit with RF Input of 152.2MHz and IF of 10.7MHz ±7.5kHz

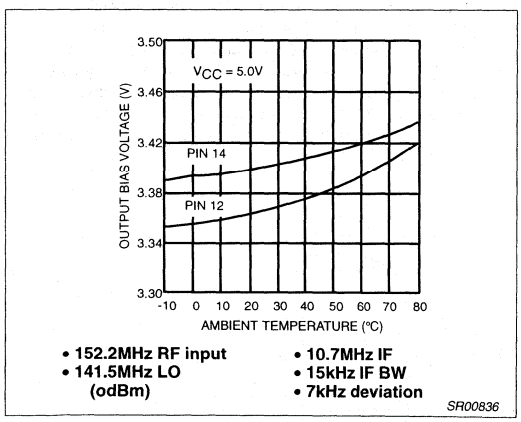

Figure 17. VHF Single Conversion (Narrow Band)

EXAMPLE: 100MHZ TO 10.7MHZ WIDEBAND

This example represents three possible applications: (1) low cost, sensitive FM broadcast receivers, (2) SCA (Subsidiary Communications Authorization) receivers and (3) data receivers. The circuit schematic is shown in Figure 14. While this example has the greatest diversity of application, it is also the simplest. Two 10.7MHz ceramic filters were used. The first was directly connected to the output of the NE602. The second was directly connected to the output of the first IF limiter. The secondary sides of both filters were terminated with 330Ω as in the two previous examples. While the filter bandpass skew of this simple single conversion receiver might not be tolerable in some applications, to a first order the results are excellent. (Please note that sensitivity is measured at +20dB in this wideband example.) Performance is illustrated in Figure 15. +20dB SINAD was measured with 1.8µV input.

EXAMPLE: 152.2MHZ TO 10.7MHZ NARROWBAND

In this example (see Figure 16) a simple, effective, and relatively sensitive single conversion VHF receiver has been implemented. All of the circuit philosophy has been described in previous examples. In this circuit, tuned-transformed termination was used on the input and output sides of the crystal filter. Performance is shown in Figure 17. The +12dB SINAD sensitivity was 0.9µV.

OSCILLATORS

The NE602 contains an oscillator transistor which can be used to frequencies greater than 200MHz. Some of the possible configurations are shown in Figures 18 and 19.

L/C

When using a synthesizer, the LO must be externally buffered. Perhaps the simplest approach is an emitter follower with the base connected to Pin 7 of the NE602. The use of a dual-gate MOSFET will improve performance because it presents a fairly constant capacitance at its gate and because it has very high reverse isolation.

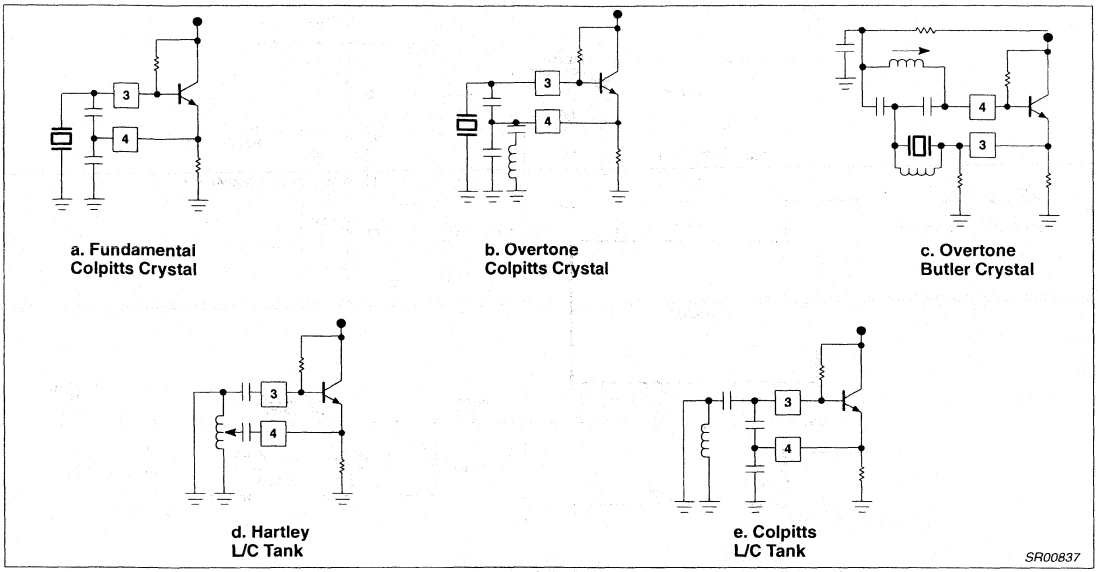

Figure 18. Oscillator Configurations

CRYSTAL

With both of the Colpitts crystal configurations, the load capacitance must be specified. In the overtone mode, this can become a sensitive issue since the capacitance from the emitter to ground is actually the equivalent capacitive reactance of the harmonic selection network. The Butler oscillator uses an overtone crystal specified for series mode operation (no parallel capacitance). It may require an extra inductor (L_o) to null out C_o of the crystal, but otherwise is fairly easy to implement (see references).

The oscillator transistor is biased with only 220μA. In order to assure oscillation in some configurations, it may be necessary to increase transconductance with an external resistor from the emitter to ground. 10kΩ to 20kΩ are acceptable values. Too small a resistance can upset DC bias (see references).

DATA DEMODULATION

It is possible to change any of the examples from an audio receiver to an amplitude shift keyed (ASK) or frequency shift keyed (FSK) receiver or both with the addition of an external op amp(s) or comparator(s). A simple example is shown in Figure 20. ASK decoding is accomplished by applying a comparator across the received signal strength indicator (RSSI). The RSSI will track IF level down to below the limits of the demodulator (–120dBm RF input in most of the examples). When an in-band signal is above the comparator threshold, the output logic level will change.

FSK demodulation takes advantage of the two audio outputs of the NE604A. Each is a PNP current source type output with 180° phase relationship. With no signal present, the quad tank tuned for the center of the IF passband, and both outputs loaded with the same value of capacitance, if a signal is received which is frequency shifted from the

IF passband, and both outputs loaded with the same value of capacitance, if a signal is received which is frequency shifted from the IF center, one output voltage will increase and the other will decrease by a corresponding absolute value. Thus, if a comparator is differentially connected across the two outputs, a frequency shift in one direction will drive the comparator output to one supply rail, and a frequency shift in the opposite direction will cause the comparator output to swing to the opposite rail. Using this technique, and L/C filtering for a wide IF bandwidth, NRZ data at rates greater than 4Mb have been processed with the new NE605.

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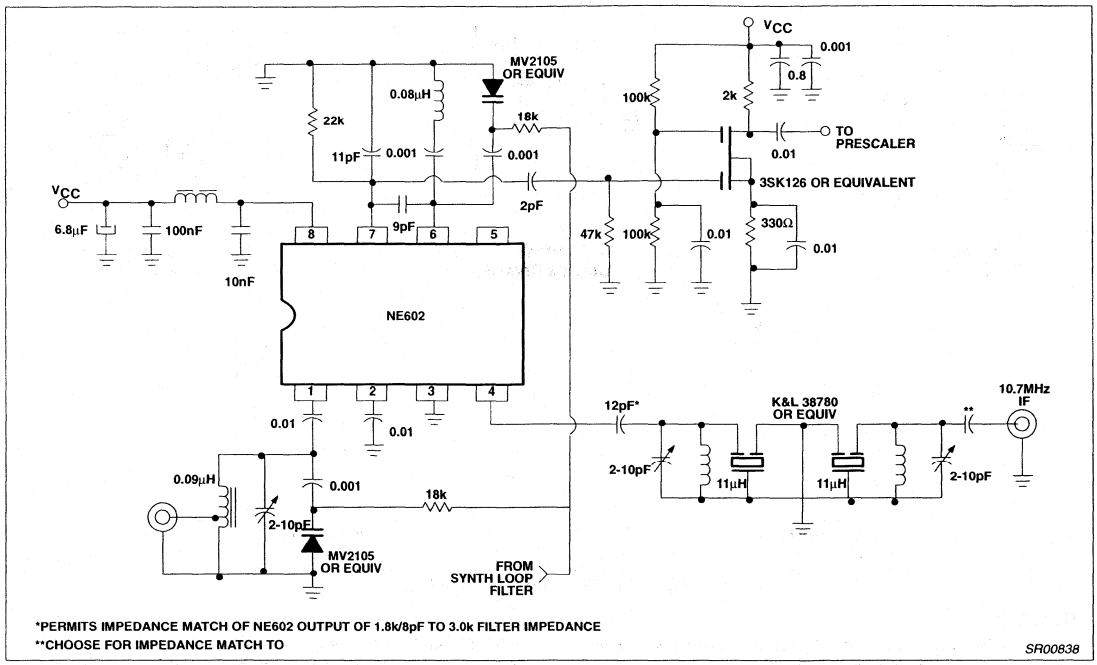

Figure 19. Typical Varactor Tuned Application

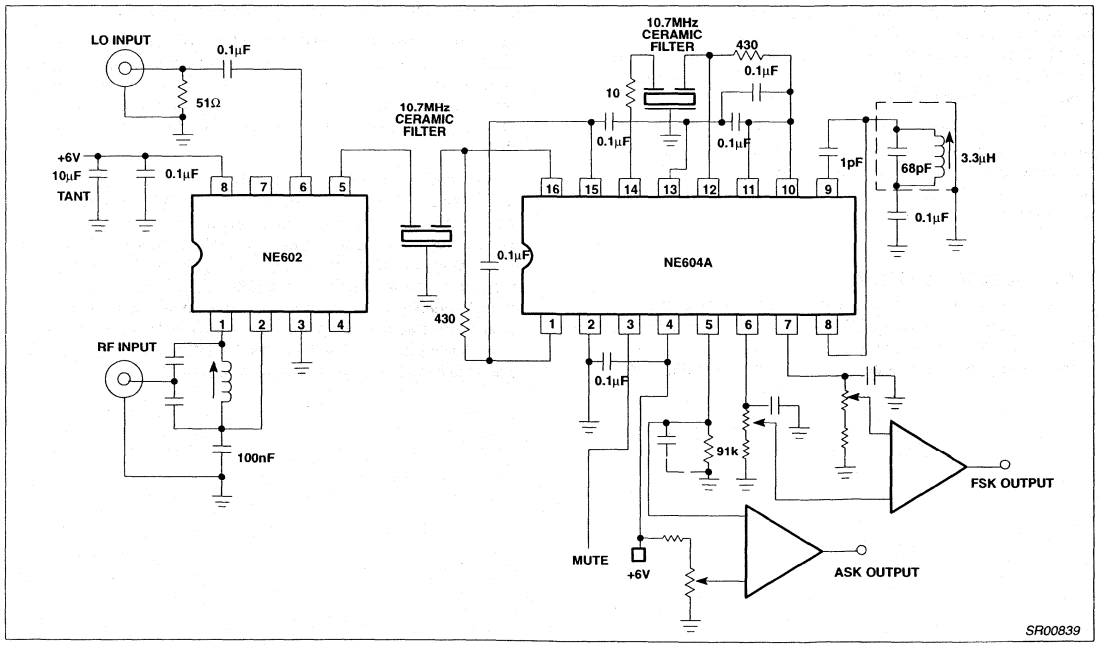

Figure 20. Basic NE602/604A Data Receiver

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SUMMARY

The NE602, NE604A and NE605 provide the RF system designer with the opportunity for excellent receiver or IF system sensitivity with very simple circuitry. IFs at 455kHz, 10.7MHz and 21.4MHz with 75 to 90dB gain are possible without special shielding. The flexible configuration of the built-in oscillator of the NE602/605 add to ease of implementation. Either data or audio can be recovered from the NE604A/605 outputs.

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3) Matthys, R.: "Survey of VHF Crystal Oscillator Circuits," RF Technology Expo Proceedings, pp 371-382, February, 1987.

4) Philips Semiconductors: "NE/SA604A High Performance Low Power FM IF System", Linear Data and Applications Manual, Philips Semiconductors, 1987.

5) Philips Semiconductors; "NE/SA602 Double Balanced Mixer and Oscillator", Linear Data and Applications Manual, Philips Semiconductors, 1985.

6) Philips Semiconductors: "AN1982–Applying the Oscillator of the NE602 in Low Power Mixer Applications", Linear Data and Applications Manual, Philips Semiconductors, 1985.

High performance low power mixer FM IF system NE/SA605

DESCRIPTION

The NE/SA605 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA605 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA605 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA605. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

PIN CONFIGURATION

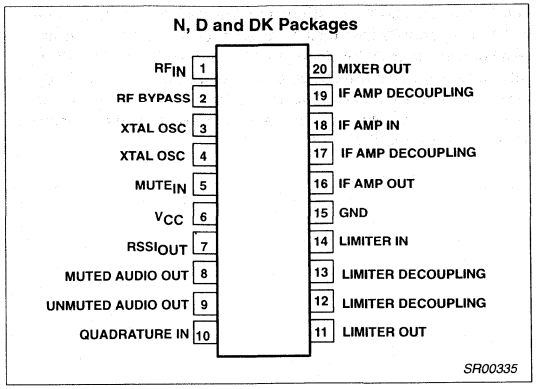


Figure 1. Pin Configuration

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA605 meets cellular radio specifications
- ESD hardened

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE605N	SOT146-1
20-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA605N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package	0 to +70°C	NE605D	SOT163-1
20-Pin Plastic Small Outline Large (SOL) package	–40 to +85°C	SA605D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	0 to +70°C	NE605DK	SOT266-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA605DK	SOT266-1

BLOCK DIAGRAM

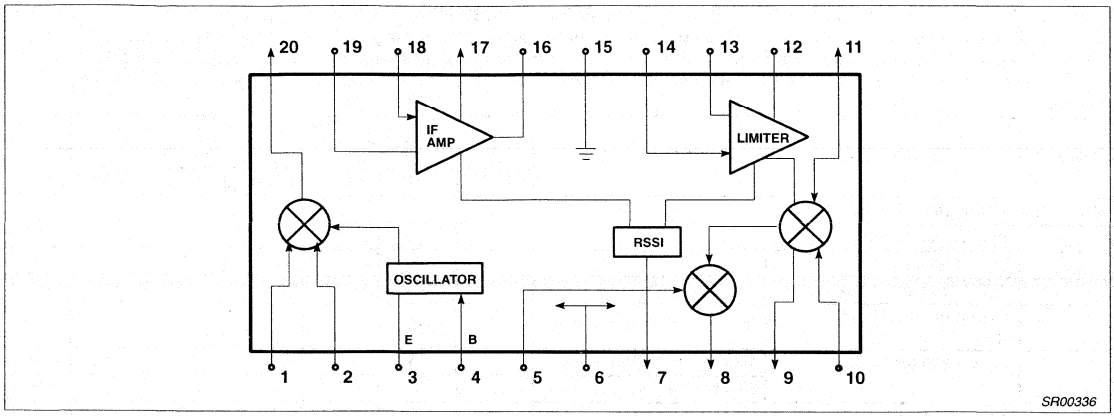


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range NE605		0 to +70	°C
	SA605		-40 to +85	°C
θ_{JA}	Thermal impedance	D package N package SSOP package	90 75 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.7	6.5	4.55	5.7	6.55	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480			480		mV
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		1.40	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ
RF/IF section (int LO)									
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450			450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:

1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA605 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

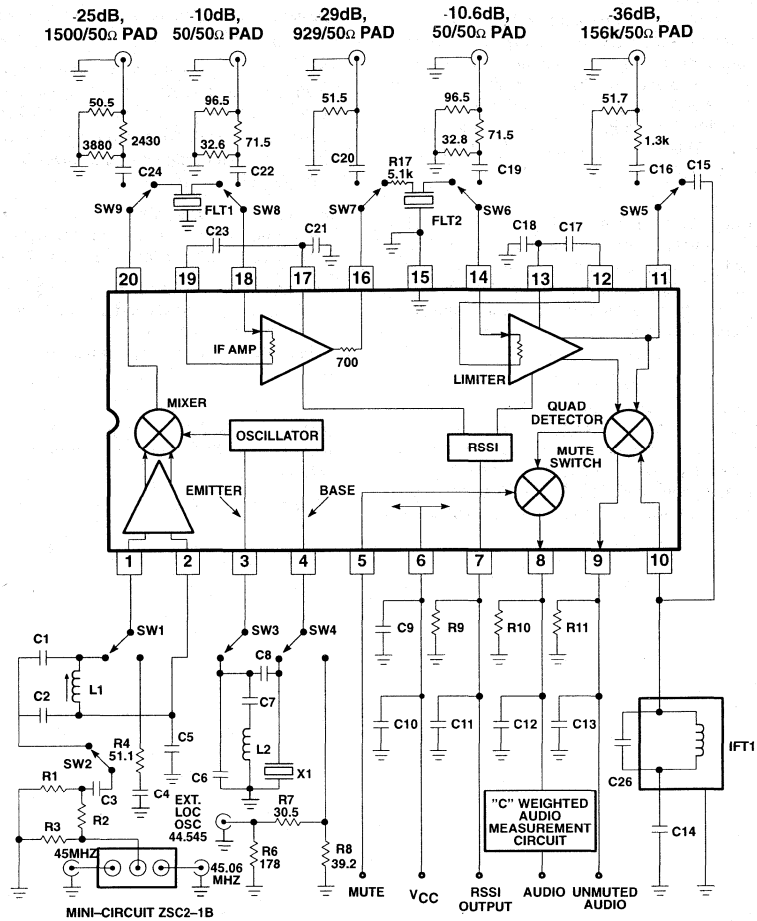
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



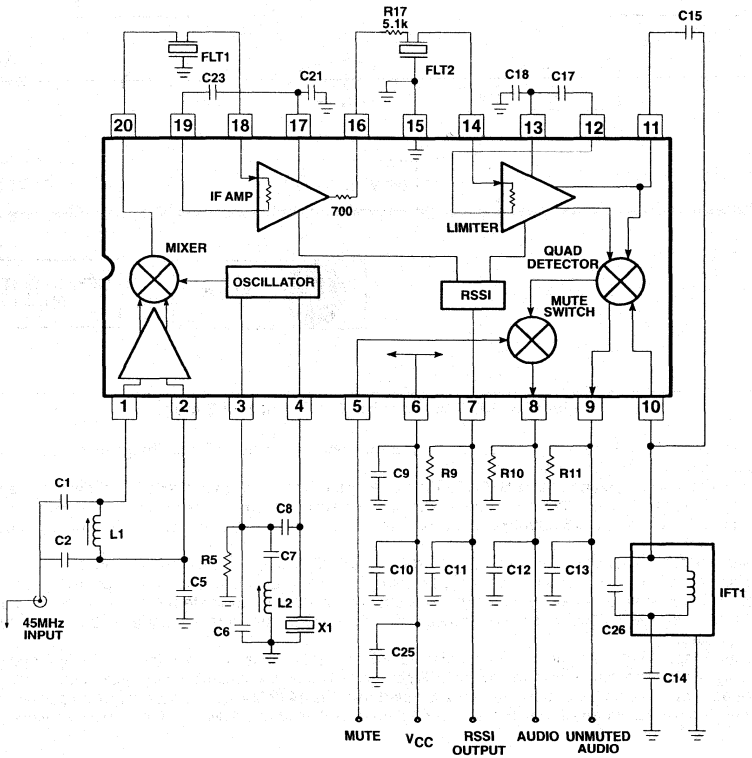
Automatic Test Circuit Component List

C1	47pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	180pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	C26	390pF ±10% Monolithic Ceramic
C7	1nF Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C9	100nF ±10% Monolithic Ceramic	IFT 1	455kHz 270µH TOKO #303LN-1129
C10	6.8µF Tantalum (minimum) *	L1	300nH TOKO #5CB-1055Z
C11	100nF ±10% Monolithic Ceramic	L2	0.8µH TOKO 292CNS–T1038Z
C12	15nF ±10% Ceramic	X1	44.545MHz Crystal ICM4712701
C13	150pF ±2% N1500 Ceramic	R9	100k ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C15	10pF NPO Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

* NOTE: This value can be reduced when a battery is the power source.

SR00337

Figure 3. NE/SA605 45MHz Test Circuit (Relays as shown)



Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270µH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8µH TOKO 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

* NOTE: This value can be reduced when a battery is the power source.

SR00338

Figure 4. NE/SA605 45MHz Application Circuit

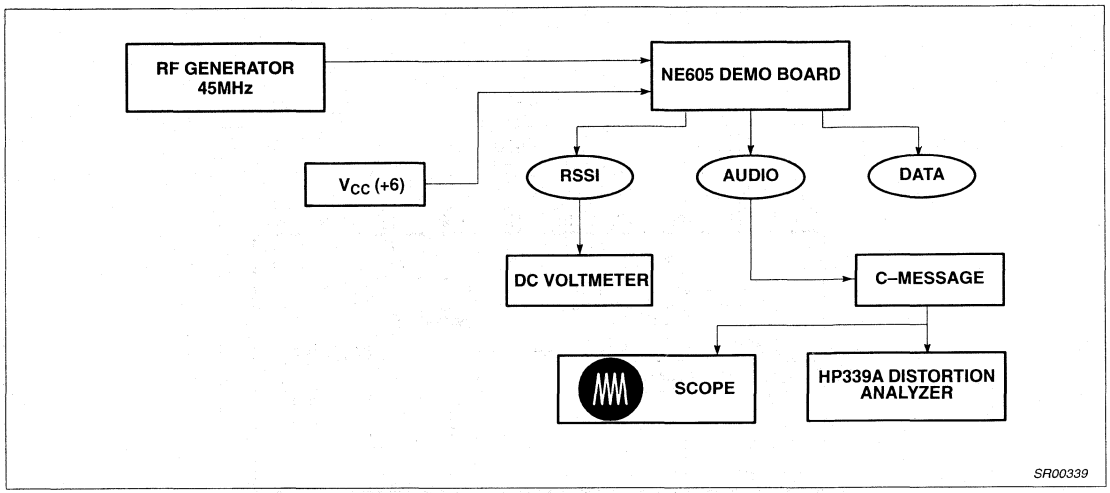


Figure 5. NE/SA605 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

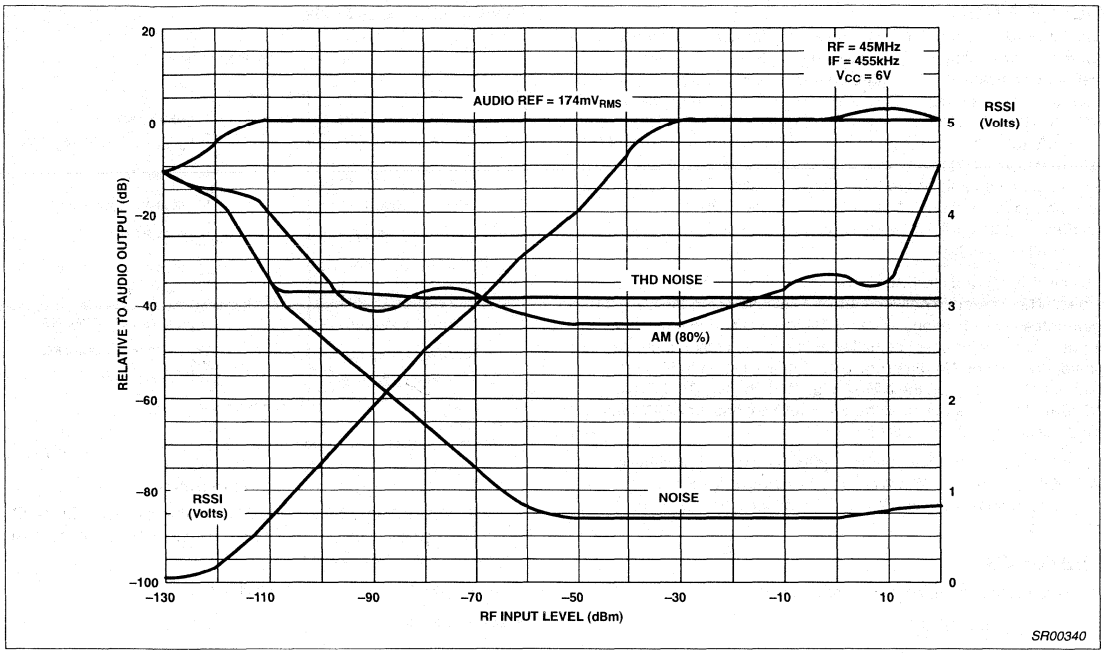


Figure 6. NE605 Application Board at 25°C

High performance low power mixer FM IF system NE/SA615

DESCRIPTION

The NE/SA615 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA615 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA615 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA615. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs – muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters

PIN CONFIGURATION

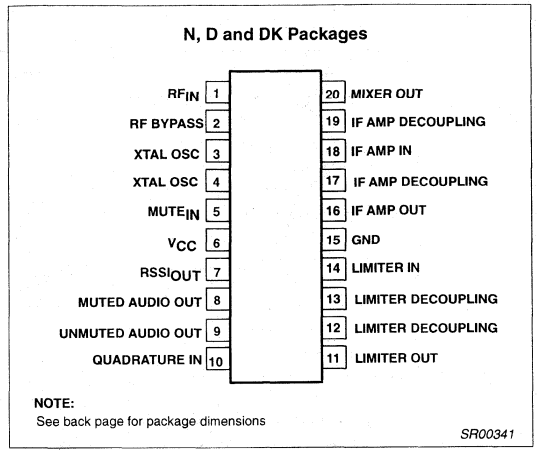


Figure 1. Pin Configuration

- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA615 meets cellular radio specifications
- ESD hardened

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE615N	SOT146-1
20-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA615N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package	0 to +70°C	NE615D	SOT108-1
20-Pin Plastic Small Outline Large (SOL) package	–40 to +85°C	SA615D	SOT108-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	0 to +70°C	NE615DK	SOT266-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA615DK	SOT266-1

BLOCK DIAGRAM

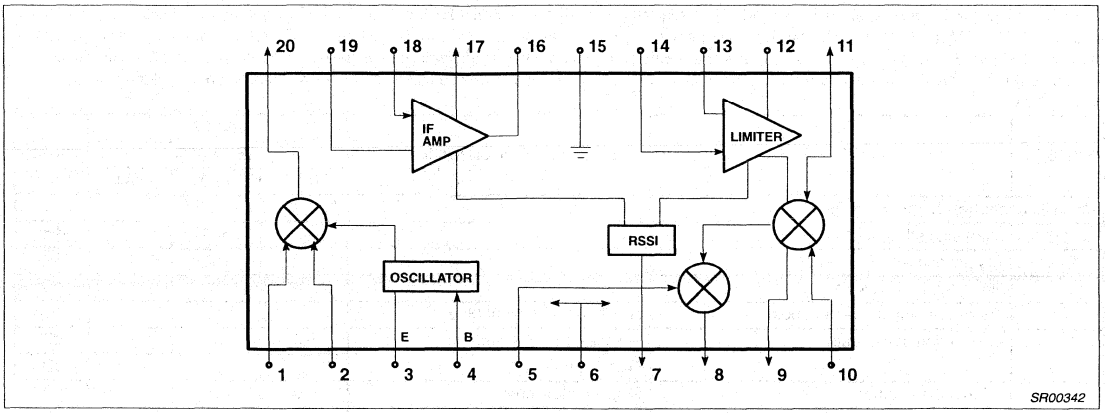


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range NE615	0 to +70	°C
	SA615	–40 to +85	°C
θ_{JA}	Thermal impedance D package N package SSOP package	90 75 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA615			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain			5.7	7.4	mA
	Mute switch input threshold (ON)		1.7			V
	(OFF)				1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step–up; IF frequency = 455kHz; R17 = 5.1k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA615			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.00; f2 = 45.06MHz		-12		dBm
	Conversion power gain	Matched 14.5dBV step-up	8.0	13		dB
		50Ω source		-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.50		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz	25	33	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	60	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		530		mV
	SINAD sensitivity	RF level -118dB		12		dB
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	800	mV
		IF level = -68dBm	1.7	2.5	3.3	V
		IF level = -18dBm	3.6	4.8	5.8	V
	RSSI range	R_9 = 100kΩ Pin 16		80		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±2		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ
RF/IF section (int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3		V

NOTE:

1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA615 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source.

However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of −10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

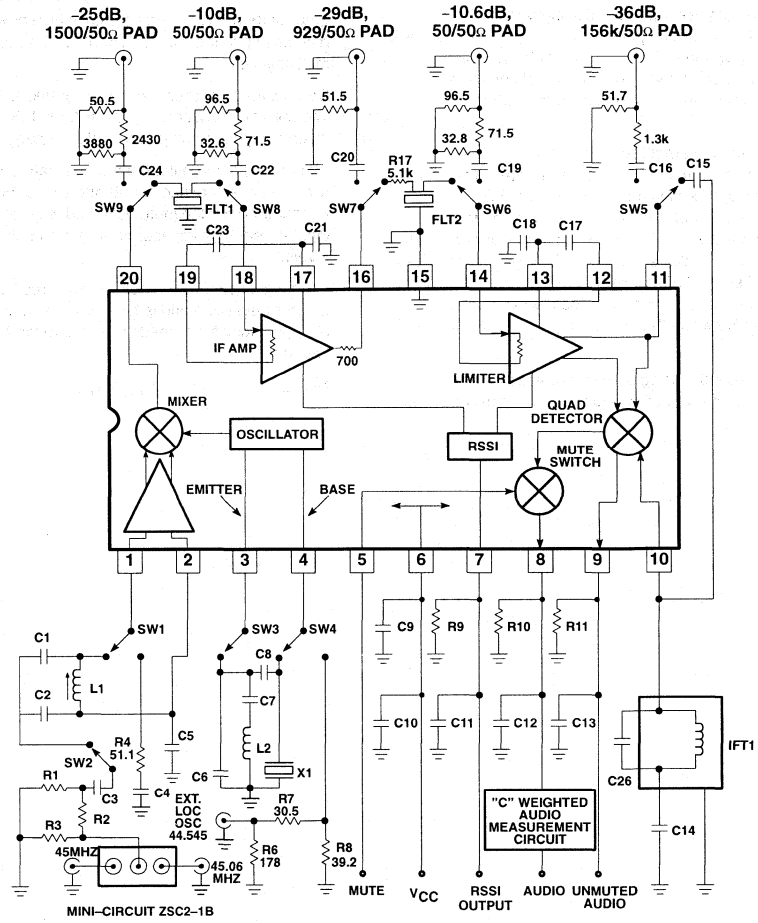
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



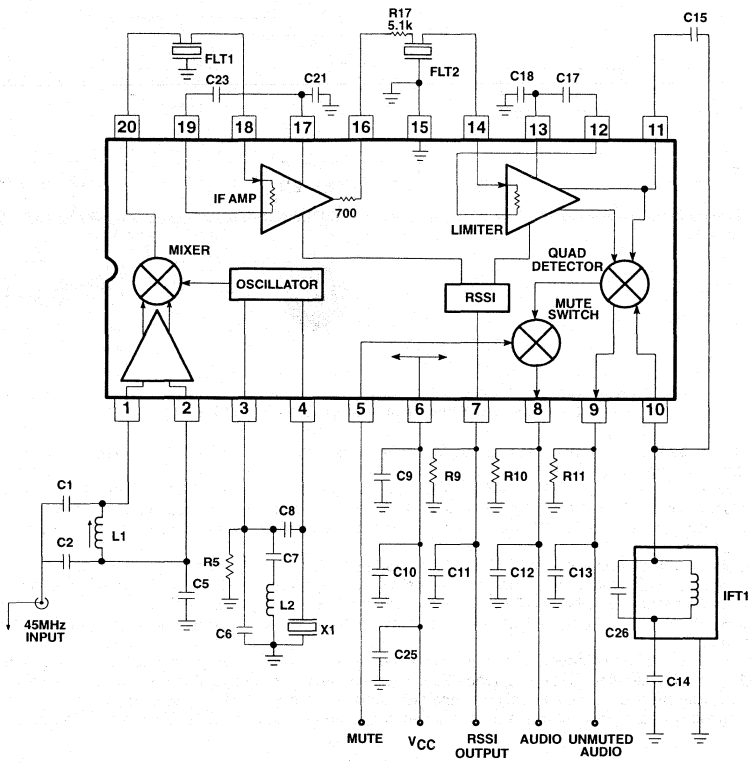
Automatic Test Circuit Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270µH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8µH TOKO 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

SR00343

Figure 3. NE/SA615 45MHz Test Circuit (Relays as shown)



NE/SA615N
Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270μH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8μH TOKO 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

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Figure 4. NE/SA615 45MHz Application Circuit

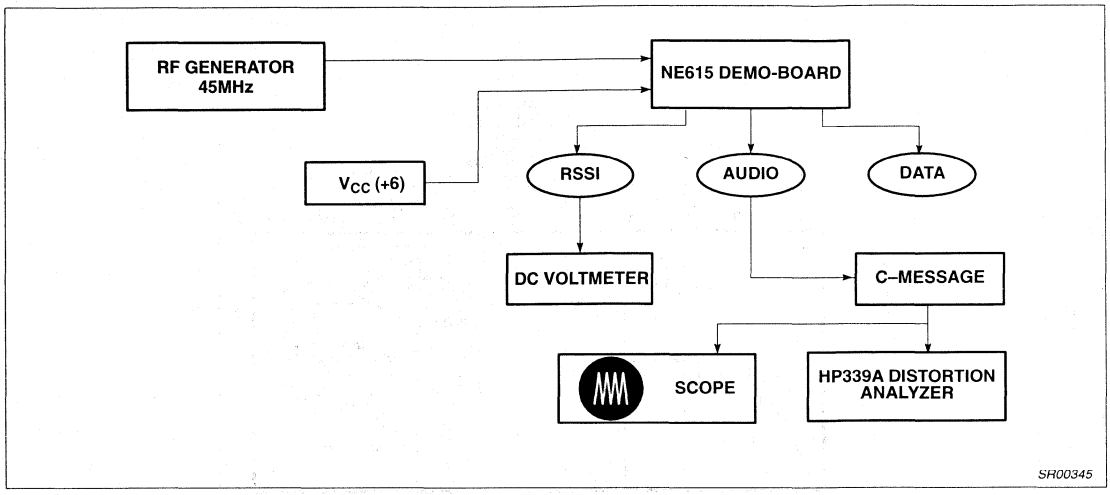


Figure 5. NE/SA615 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or –120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10–15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2–3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

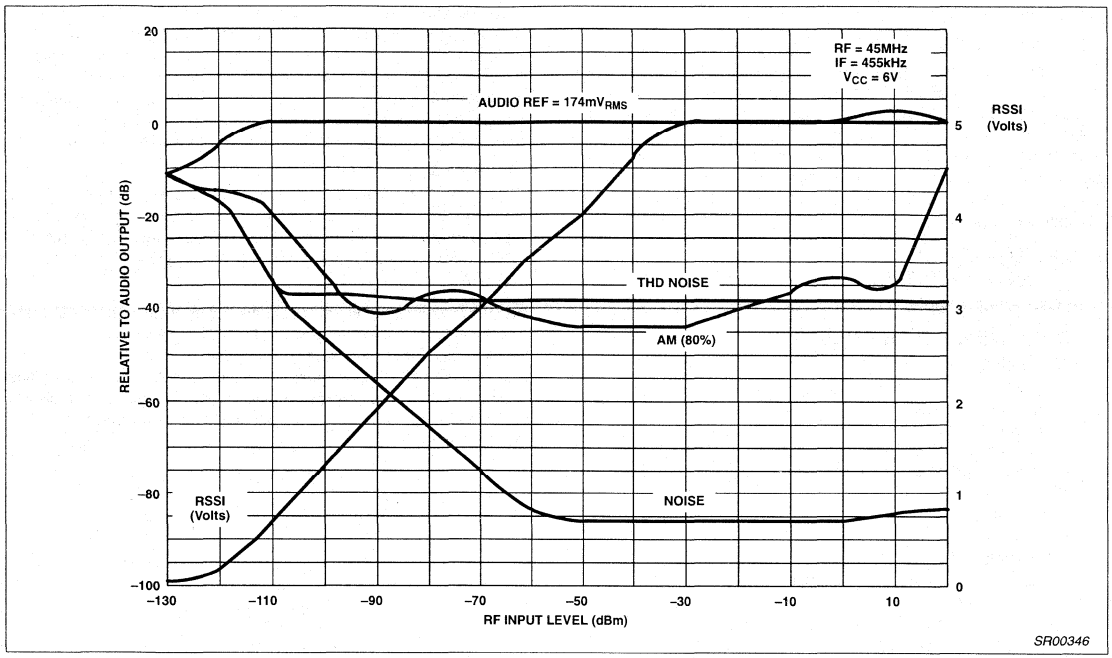


Figure 6. NE615 Application Board at 25°C

Reviewing key areas when designing with the NE605 AN1994

Author: Alvin K. Wong

INTRODUCTION

This application note addresses key information that is needed when designing with the NE605. Since the NE602 and the NE604 are closely related to the NE605, a brief overview of these chips will be helpful. Additionally, this application note will divide the NE605 into four main blocks where a brief theory of operation, important parameters, specifications, tables and graphs of performance will be given. A question & answer section is included at the end. Below is an outline of this application note:

I. BACKGROUND

- History of the NE605
- Related app. notes

II. OVERVIEW OF THE NE605

- Mixer Section
  - RF section
  - Local osc. section
  - Output of mixer
  - Choosing the IF frequency
  - Performance graphs of mixer
- IF Section
  - IF amplifier
  - IF limiter
  - Function of IF section
  - Important parameters of IF section
    3. Limiting
    4. AM rejection
    5. AM to PM conversion
    6. Interstage loss
  - IF noise figure
  - Performance graphs of IF section
- Demodulator Section
- Output Section
  - Audio and unmuted audio
  - RSSI output
  - Performance graphs of output section

III.Question & Answers

I. BACKGROUND

History of the NE605

Before the NE605 was made, the NE602 (double-balanced mixer and oscillator) and the NE604 (FM IF system) existed. The combination of these two chips make up a high performance low cost receiver. Soon after the NE605 was created to be a one chip solution, using a newer manufacturing process and design. Since the newer process and design in the NE605 proved to be better in performance and reliability, it was decided to make the NE602 and the NE604 under this new process. The NE602A and the NE604A were created. To assist the cost-conscious customer, Philips Semiconductors also offered an inexpensive line of the same RF products: the NE612, NE614, and NE615.

Because the newer process and design proved to be better in performance and reliability, the older chips are going to be discontinued. Therefore, only the NE602A, NE612A, NE604A, NE614A, NE605 and NE615 will be available.

Figure 1 shows a brief summary of the RF chips mentioned above. Under the newer process, minor changes were made to improve the performance. A designer, converting from the NE602 to the NE602A, should have no problem with a direct switch. However, switching from the NE604 to the NE604A, might require more attention. This will depend on how good the original design was in the system. In the "Questions & Answers" section, the NE604 and NE604A are discussed in greater detail. This will help the designer, who used the NE604 in their original design, to switch to the "A" version. In general, a direct switch to the NE604A is simple.

Related Application Notes

There have been many application notes written on the NE602 and NE604A. Since the combination of those parts is very similar to the NE605, many of the ideas and applications still apply. In addition, many of the topics discussed here will also apply to the NE602A and NE604A.

Table 1 (see back of app note) shows the application notes available to the designer. They can be found in either the Philips Semiconductors Linear Data Manual, Volume 1, or the Philips Semiconductors RF Communications Handbook. Your local Philips Semiconductos sales representative can provide you with copies of these publications, or you can contact Philips Semiconductors Publication Services.

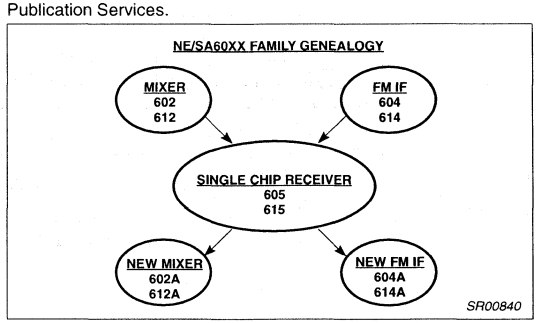


Figure 1. Overview of Selected RF Chips

II. OVERVIEW OF THE NE605

In Figure 2, the NE605 is broken up into four main areas; the mixer section, the IF section, the demodulator section and the output section. The information contained in each of the four areas focuses on important data to assist you with the use of the NE605 in any receiver application.

Mixer Section

There are three areas of interest that should be addressed when working with the mixer section. The RF signal, LO signal and the output. The function of the mixer is to give the sum/difference of the RF and LO frequencies to get an IF frequency out. This mixing of frequencies is done by a Gilbert Cell four quadrant multiplier. The Gilbert Cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell.

The RF input impedance of the mixer plays a vital role in determining the values of the matching network. Figure 3 shows the RF input impedance over a range of frequency. From this information, it can be determined that matching 50Ω at 45MHz requires matching to a 4.5kΩ resistor in parallel with a 2.5pF capacitor. An equivalent model can be seen in Figure 4 with its component values given for selected frequencies. Since there are many questions from the designer on how to match the RF input, an example is given below.

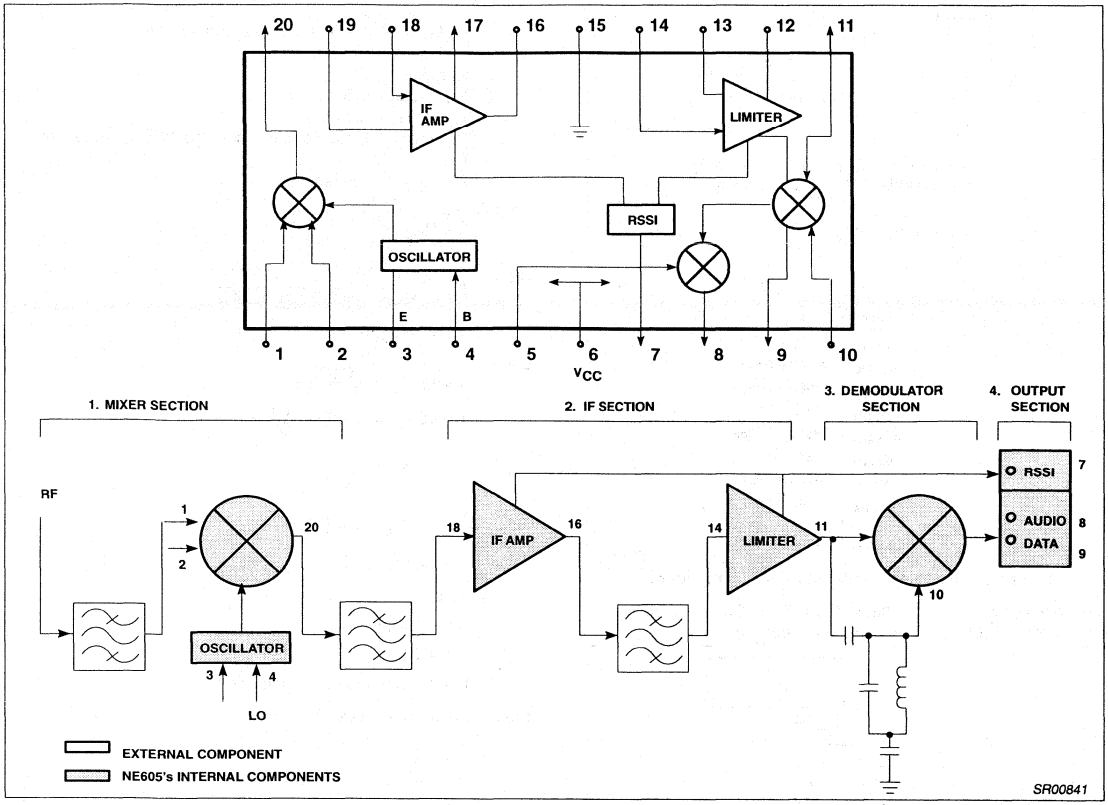


Figure 2. NE605 Broken Down into Four Areas

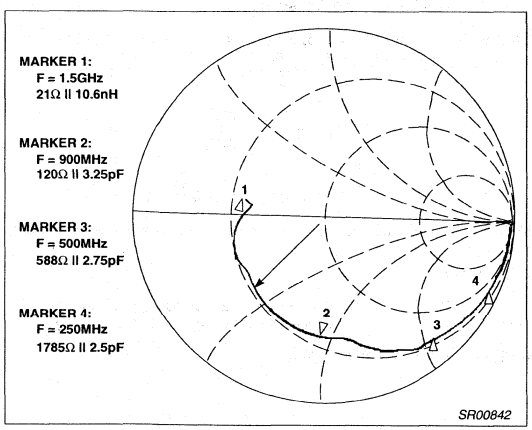


Figure 3. Smith Chart of NE605's RF Input Impedance (Pin 1 or 2)

RF Section of Mixer

The mixer has two RF input pins (Pin 1 and 2), allowing the user to choose between a balanced or unbalanced RF matching network. Table 2 (see back of app note) shows the advantages and disadvantages for either type of matching. Obviously, the better the matching network, the better the sensitivity of the receiver.

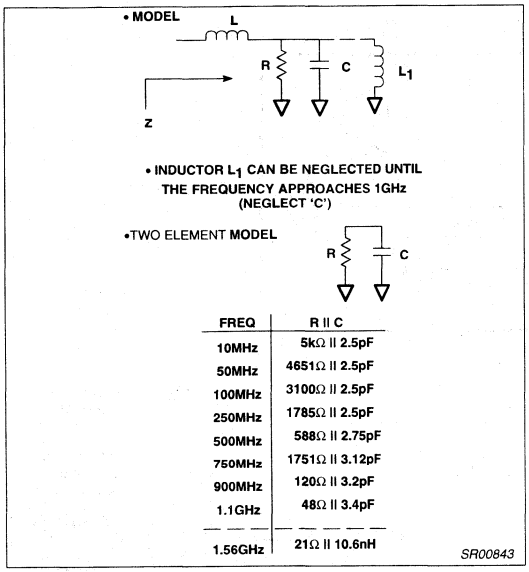


Figure 4. Equivalent Model of RF Input Impedance

Example: Using a tapped-C network, match a 50Ω source to the RF input of the NE605 at 45MHz. (refer to Figure 5)

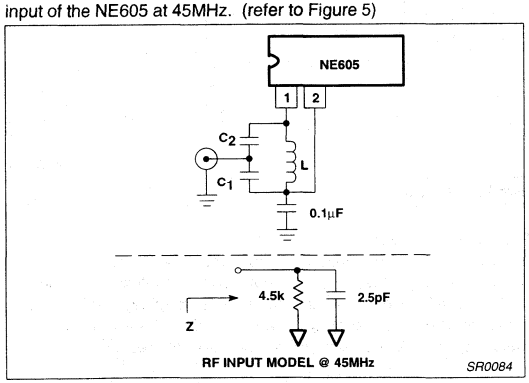


Figure 5. Tapped-C Network

Step 1. Choose an inductor value and its "Q" L = 0.22μH Q_P = 50 (specified by manufacturer)

Step 2. Find the reactance of the inductor

$X_P = 2\pi FL$

$= 2\pi\ (45MHz)\ (0.22\mu H)$

$\therefore\ X_P = 62.2\Omega$

Step 3. Then,

$R_P = Q_P X_P$

$= (50)(62.2)$

$\therefore\ R_P = 3.11k\Omega$ (the inductance resistance)

Step 4. $Q = R_{TOTAL}/X_P$

$= (R_S' // R_L // R_P) / X_P$

where $R_S' = R_L$

$= 4.5k // 4.5k // 3.11k / 62.2$

$= 21.39$

$\therefore\ Q \cong 21$ (the Q of the matching network)

where:

R_S = source resistance;

R_L = load resistance;

R_S' = what the source resistance should look like to match R_L;

R_P = inductance resistance

Step 5. $\frac{C1}{C2} = \sqrt{\frac{R_S'}{R_S}} - 1 = 8.6$

Step 6. $C_T = \frac{1}{X_P\ \omega} = \frac{1}{(62.2)\ 2\pi\ 45MHz}$

$= 56.86pF$

Step 7. using $C_T = \frac{C1C2}{C1 + C2}$

where $C_T = 56.86pF$, $\frac{C1}{C2} = 8.6$

$$C_T = \frac{C1}{\frac{C1}{C2} + 1}$$

$$\therefore\ C_1 = C_T\left(\frac{C1}{C2} + 1\right)$$

and $C_2 = \frac{C1}{8.6}$

thus...

C1 = 539pF

C2 = 64pF

L = 0.22μH (value started with)

Step 8. Frequency check

$$\omega = \frac{1}{\sqrt{LC}}$$

$$2\pi F = \frac{1}{\sqrt{LC}}$$

F = 45MHz (...so far so good)

Step 9. Taking care of the 2.5pF capacitor that is present at the RF input at 45MHz $\frac{C2_A}{C1_A} = \frac{64pF}{540pF}$ Eq. 1.

$$C_{TN} = \frac{C1_A C2_A}{C1_A + C2_A}$$ Eq. 2.

where $C_{TN} = C_T - 2.5pF$
(recall value of C_T from Step 6.)

Making use of Equations 1 and 2, the new values of C1 and C2 are:

$C1_A = 524pF$

$C2_A = 60.6pF$

[NOTE: At this frequency the 2.5pF capacitor could probably be ignored since its value at 45MHz has little effect on C1 and C2.]

Step 10. Checking the bandwidth $Q = \frac{F}{BW}$

$$BW = F_U - F_L$$

BW = bandwidth

F_U = upper 3dB frequency

F_L = lower 3dB frequency

Using the above formulas results in
F_U = 46MHz
F_L = 44MHz
BW = 2MHz

The above shows the calculations for a single-ended match to the NE605. For a balanced matching network, a transformer can be used. The same type of calculations will still apply once the input impedance of the NE605 is converted to the primary side of the transformer (see Figure 6). But before we transform the input impedance to the primary side, we must first find the new input impedance of the NE605 for a balanced configuration. Because we have a balanced input, the 4.5kΩ transforms to 9kΩ (4.5k + 4.5k = 9k) while the capacitor changes from 2.5pF to 1.3pF (2.5pF in series with 2.5pF is 1.3pF). Notice that the resistor values double while the capacitor values are halved. Now the 9kΩ resistor in parallel with the 1.3pF capacitor must be transformed to the primary side of the transformer (see Figure 6).

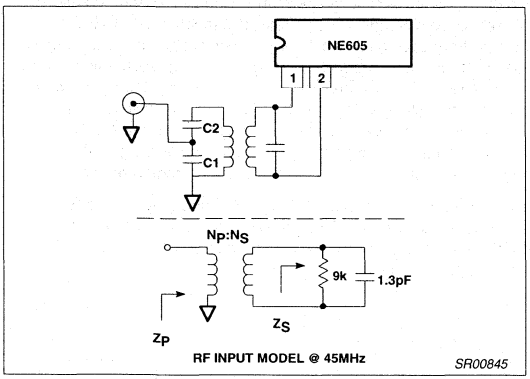


Figure 6. Using a Transformer to Achieve a Balanced Match

Procedure:

Step 1. $\frac{Z_P}{Z_S} = \left(\frac{N_P}{N_S}\right)^2$

where:
Z_P = impedance of primary side
Z_S = impedance of secondary side
N_P = number of turns on primary side
N_S = number of turns on secondary side

Step 2. Recall,

$Z_S = R \parallel X_C$
$Z_S = 9k \parallel j2.7k$
where
$R = 9k$ $X_C = \frac{1}{2\pi FC} = 2.7k$ at $F = 45MHz$

Step 3. Assume 1:N turns ratio for the transformer

$Z_P = \frac{Z_S}{N^2} = 2.25k \parallel j\ 680$

(assuming N = 2)

Step 4. $\therefore C = \frac{1}{2\pi\ FX_C} = 5.2pF$

R = 2.25k
(these are the new values to match using the formulas in tapped-C)

Step 5. Because the transformer has a magnetization inductance L_M, (inductance presented by the transformer), we can eliminate the inductor used in the previous example and tune the tapped-C network with the inductance presented by the transformer.
Lets assume L_M = 0.22μH (Q=50) Therefore
C1 = 381pF
C2 = 66.8pF
F_U = 46.7MHz
F_L = 43.3MHz
BW = 3.4MHz
taking the input capacitor into consideration
C1 = 347pF
C2 = 61pF
L = 0.22μH (Q=50)

Because of leakage inductance, the transformer is far from ideal. All of these leakages affect the secondary voltage under load which will seem like the indicated turns ratio is wrong. The above calculations show one method of impedance matching. The values calculated for C1 and C2 do not take into account board parasitic capacitance, and are, therefore, only theoretical values. There are many ways to configure and calculate matching networks. One alternative is a tapped-L configuration. But the ratio of the tapped-C network is easier to implement than ordering a special inductor. The calculations of these networks can be done on the Smith Chart. Furthermore, there are many computer programs available which will help match the circuit for the designer.

Local Oscillator Section of Mixer

The NE605 provides an NPN transistor for the local oscillator where only external components like capacitors, inductors, or resistors need to be added to achieve the LO frequency. The oscillator's transistor base and emitter (Pins 4 and 3 respectively) are available to be configured in Colpitts, Butler or varactor controlled LC forms. Referring to Figure 7, the collector is internally connected directly to V_{CC}, while the emitter is connected through a 25kΩ resistor to ground. Base bias is also internally supplied through an 18kΩ resistor. A buffer/divider reduces the oscillator level by a factor of three before it is applied across the upper tree of the Gilbert Cell. The divider de-sensitizes the mixer to oscillator level variations with temperature and voltage. A typical value for the LO input impedance is approximately 10kΩ.

The highest LO frequency that can be achieved is approximately 300MHz with a 200mV_{RMS} signal on the base (Pin 4). Although it is possible to exceed the 300MHz LO frequency for the on-board oscillator, it is not really practical because the signal level drops too low for the Gilbert Cell. If an application requires a higher LO frequency, an external oscillator can be used with its 200mV_{RMS} signal injected at Pin 4 through a DC blocking capacitor. Table 3 (see back of app note) can be used as a guideline to determine which configuration is best for the required LO frequency.

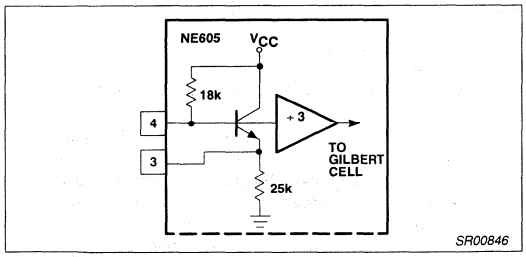


Figure 7. On-board NPN Transistor for Local Oscillator

Because the Colpitts configuration is for parallel resonance mode, it is important to know, when ordering crystals, that the load capacitance of the NE605 is 10pF. However, for the Butler configuration, the load capacitance is unimportant since the crystal will be in the series mode. Figure 8 shows the different types of LO configurations used with NE605.

If a person decides to use the Colpitts configuration in their design, they will probably find that most crystal manufacturers have their own set of standards of load capacitance. And in most cases, they are unwilling to build a special test jig for an individual's needs. If this occurs, the designer should tell them to go ahead with the design. But, the designer should also be ready to accept the crystal's frequency to be off by 200–300Hz from the specified frequency. Then a test jig provided by the designer and a 2nd iteration will solve the problem.

Output of Mixer

Once the RF and LO inputs have been properly connected, the output of the mixer supplies the IF frequency. Knowing that the mixer's output has an impedance of 1.5kΩ, matching to an IF filter should be trivial.

Choosing the Appropriate IF Frequency

Some of the standard IF frequencies used in industry are 455kHz, 10.7MHz and 21.4MHz. Selection of other IF frequencies is possible. However, this approach could be expensive because the filter manufacturer will probably have to build the odd IF filter from scratch.

There are several advantages and disadvantages in choosing a low or high IF frequency. Choosing a low IF frequency like 455kHz can provide good stability, high sensitivity and gain. Unfortunately, it can also present a problem with the image frequency (assuming single conversion). To improve the image rejection problem, a higher IF frequency can be used. However, sensitivity is decreased and the gain of the IF section must be reduced to prevent oscillations.

If the design requires a low IF frequency and good image rejection, it is best to use the double conversion method. This method allows the best of both worlds. Additionally, it is much easier to work with a lower IF frequency because the layout will not be as critical and will be more forgiving in production. The only drawback to this method is that it will require another mixer and LO. But, a transistor can be used for the first mixer stage (which is an inexpensive approach) and the NE605 can be used for the second mixer stage. The NE602A can also be used for the first conversion stage if the transistor approach does not meet the design requirements.

If the design requires a high IF frequency, good layout and RF techniques must be exercised. If the layout is sound and instability still occurs, refer to the "RSSI output" section which suggests solutions to these types of problems.

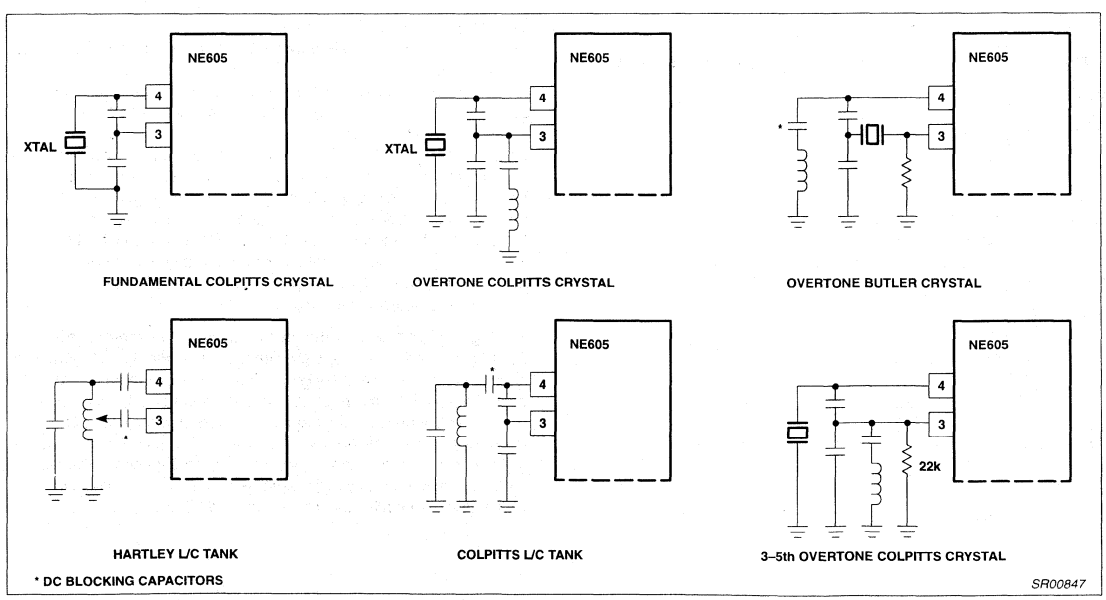


Figure 8. Oscillator Configurations

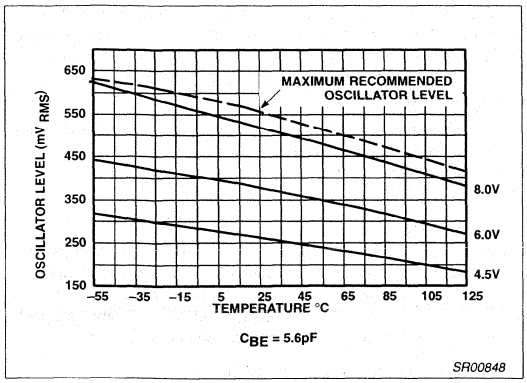


Figure 9. NE605 Application Oscillator Level

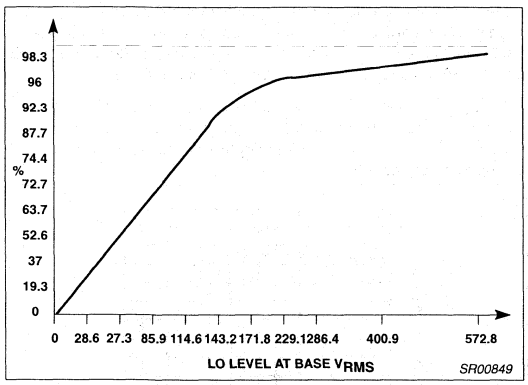


Figure 10. Mixer Efficiency vs Normalized LO Level

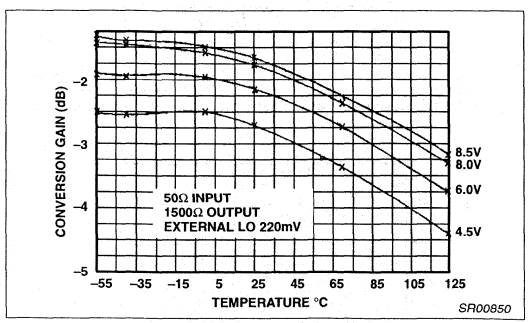


Figure 11. 50Ω Conversion Gain

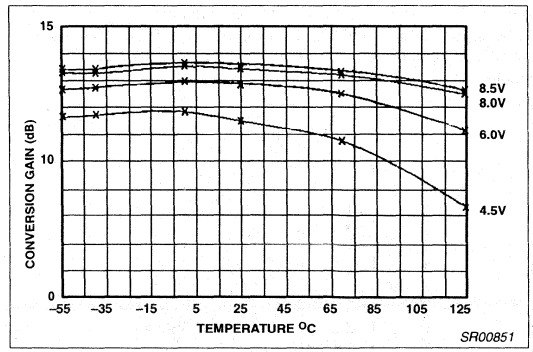


Figure 12. Single-Ended Matched Input Conversion Gain (50Ω to 1.5kΩ, 14.5dB Matching Step-up Network)

Performance Graphs of Mixer

Fig.	Description
9	Oscillator Levels vs. Temperature with Different Supply Voltages for the 44.545MHz Crystal Colpitts Applications
10	LO Efficiency vs. Normalized Peak Level at the Base of the Oscillator Transistor
11	50Ω Conversion Gain vs. Temperature with Different Supply Voltages Using an External LO
12	Mixer Matched Input Conversion Gain vs. Temperature with Different Supply Voltages
13	IF Output Power vs. RF Input Level (3rd-order Intercept Point) 1st mixer = diode mxr, 2nd mixer = 605 mxr
14	NE605 and Diode Mixer Test Set Up
15	NE605 LO Power Requirements vs. Diode Mixer
16	NE605 Conversion Gain vs. Diode Mixer
17	Comparing Intercept Points with Different Types of Mixers

Another issue to consider when determining an IF frequency is the modulation. For example, a narrowband FM signal (30kHz IF bandwidth) can be done with an IF of 455kHz. But for a wideband FM signal (200kHz IF bandwidth), a higher IF is required, such as 10.7MHz or 21.4MHz.

IF Section

The IF section consists of an IF amplifier and IF limiter. With the amplifier and limiter working together, 100dB of gain with a 25MHz bandwidth can be achieved (see Figure 18). The linearity of the RSSI output is directly affected by the IF section and will be discussed in more detail later in this application note.

IF Amplifier

The IF amplifier is made up of two differential amplifiers with 40dB of gain and a small signal bandwidth of 41MHz (when driven by a 50Ω source). The output is a low impedance emitter follower with an

output resistance of about 230Ω, and an internal series build out of 700Ω to give a total of 930Ω. One can expect a 6dB loss in each amplifier's input since both of the differential amplifiers are single-ended.

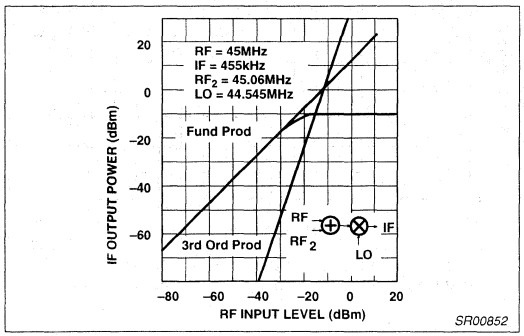


Figure 13. Third-Order Intercept and Compression

The basic function of the IF amp is to boost the IF signal and to help handle impulse noise. The IF amp will not provide good limiting over a wide range of input signals, which is why the IF limiter is needed.

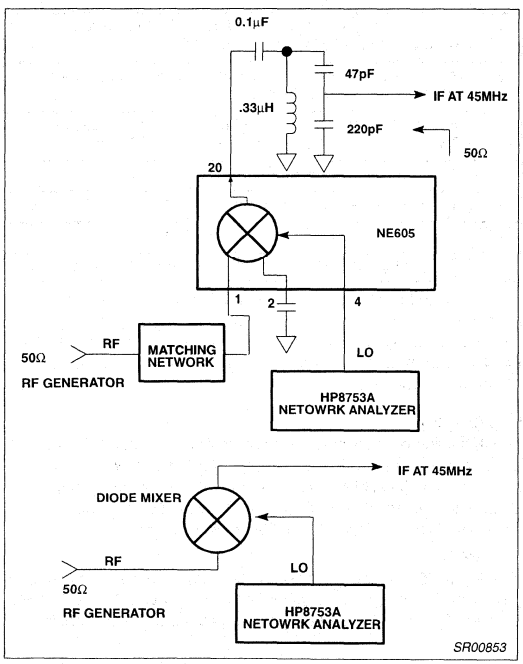


Figure 14. Test Circuits for NE605 Mixer vs Diode Mixer

IF Limiter

The IF limiter is made up of three differential amplifiers with a gain of 63dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. The IF limiter's output resistance is about 260Ω with no internal build-out. The limiter's output signal (Pin 9 onNE604A, Pin 11 on NE605) will vary from a good approximation of a square wave at lower IF frequencies like 455kHz, to a distorted sinusoid at higher IF frequencies, like 21.4MHz.

The basic function of the IF limiter is to apply a tremendous amount of gain to the IF frequency such that the top and bottom of the waveform are clipped. This helps in reducing AM and noise presented upon reception.

Function of IF Section

The main function of the IF section is to clean up the IF frequency from noise and amplitude modulation (AM) that might occur upon reception of the RF signal. If the IF section has too much gain, then one could run into instability problems. This is where crucial layout and insertion loss can help (also addressed later in this paper).

Important Parameters for the IF Section

Limiting: The audio output level of an FM receiver normally does not change with the RF level due to the limiting action. But as the RF signal level continues to decrease, the limiter will eventually run out of gain and the audio level will finally start to drop. The point where the IF section runs out of gain and the audio level decreases by 3dB with the RF input is referred to as the –3dB limiting point.

In the application test circuit, with a 5.1kΩ interstage resistor, audio suppression is dominated by noise capture down to about the –120dBm RF level at which point the phase detector efficiency begins to drop (see Interstage Loss section below).

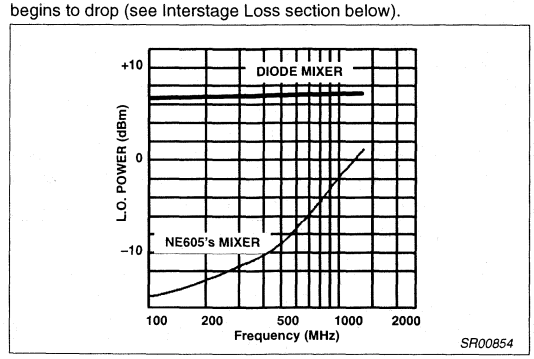


Figure 15. LO Power Requirements (Matched Input)

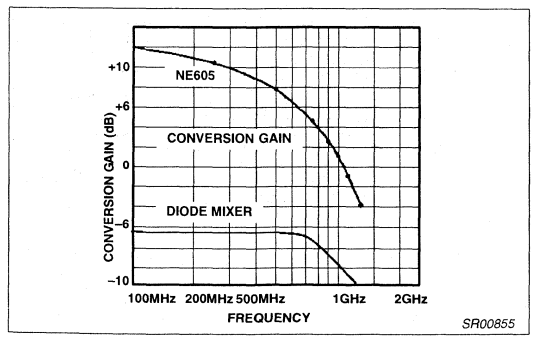


Figure 16. NE605 Conversion Gain vs. Diode Mixer

The audio drop that occurs is a function of two types of limiting. The first type is as follows: As the input signal drops below a level which is sufficient to keep the phase detector compressed, the efficiency of the detector drops, resulting in premature audio attenuation. We will call this "gain limiting". The second type of limiting occurs when there is sufficient amount of gain without de-stabilizing regeneration (i.e. keeping the phase detector fully limited), the audio level will eventually become suppressed as the noise captures the receiver. We will call this "limiting due to noise capture".

Figure 19 shows the 3dB drop in audio at about 0.26μV_{RMS}, with a −118.7dBm/50Ω RF level for the NE605. Note that the level has not improved by the 11dB gain supplied by the mixer/filter since noise capture is expected to slightly dominate here.

AM rejection: The AM rejection provided by the NE605/604A is extremely good even for 80% modulation indices as depicted in Figures 20a through 20d. This performance results from the 370mV peak signal levels set at the input of each IF amplifier and limiter stage. For this level of compression at the inputs, even better performance could be expected except that finite AM to PM conversion coefficients limit ultimate performance for high level inputs as indicated in Figure 20b.

Low level AM rejection performance degrades as each stage comes out of limiting. In particular as the quadrature phase detector input drops below 100mV peak, all limiting will be lost and AM modulation will be present at the input of the quad detector (See Figure 20d).

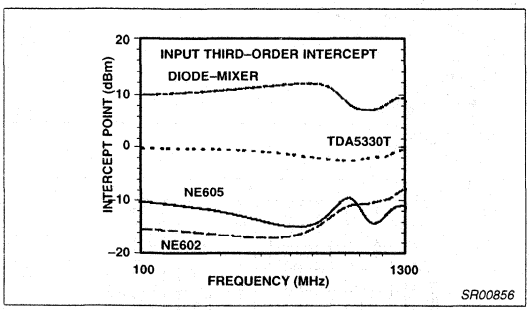


Figure 17. Comparing Different Types of Mixers

AM to PM conversion: Although AM rejection should continue to improve above −95dBm IF inputs, higher order effects, lumped under the term AM to PM conversion, limit the application rejection to about 40dB. In fact this value is proportional to the maximum frequency deviation. That is lower deviations producing lower audio outputs result directly in lower AM rejection. This is consistent with the fact that the interfering audio signal produced by the AM/PM conversion process is independent of deviation within the IF bandwidth and depends to a first estimate on the level of AM modulation present. As an example reducing the maximum frequency deviation to 4kHz from 8kHz, will result in 34dB AM rejection. If the AM modulation is reduced from 80% to 40%, the AM rejection for higher level IFs will go back to 40dB as expected. AM to PM conversion is also not a function of the quad tank Q, since an increase in Q increases both the audio and spurious AM to PM converted signal equally.

As seen above, these relationships and the measured results on the application board (Figure 36) can be used to estimate high level IF AM rejection. For higher frequency IFs (such as 21.4MHz), the limiter's output will start to deviate from a true square wave due to lack of bandwidth. This causes additional AM rejection degradation.

Interstage Loss: Figure 21 plots the simulated IF RSSI magnitude response for various interstage attenuation. The optimum interstage loss is 12dB. This has been chosen to allow the use of various types of filters, without upsetting the RSSI's linearity. In most cases, the filter insertion loss is less than 12dB from point A to point B. Therefore, some additional loss must be introduced externally. The easiest and simplest way is to use an external resistor in series with the internal build out resistor (Pin 14 in the NE604A, Pin 16 in the NE605). Unfortunately, this method mismatches the filter which might be important depending on the design. To achieve the 12dB insertion loss and good matching to the filter, an L-pad configuration can be used. Figure 22 shows the different set-ups.

Below is an example on how to calculate the resistors values for both Figures 22a and 22b.

Step 1.

$$X_{dB} = 20\log\frac{\sqrt{(960 + R_{EXT})\,R_{FLT}}}{960 + R_{EXT} + R_{FLT}} - FIL\ [dB]$$

(just solve for R_{EXT})

where
X = the insertions loss wanted in dB
R_{EXT} = the external resistor
R_{FLT} = the filter's input impedance
FIL = insertion loss of filter in dB

2. For our application board
X=12dB
R_{FLT} = 1.5k
FIL = 3dB
Therefore, using the above eq. gives
R_{EXT} = 5.1K

$$R_{EXT} = \left| 960 - \frac{R_{FLT}}{2 \times 10^{\left(\frac{-X_{dB}}{20}\right)}} \right|$$

Step 2.

$$R_{SHUNT} = \frac{R_{FLT}}{1 - 2 \times 10^{\left(\frac{-X_{dB}}{20}\right)}}$$

3. In this case, lets assume: FIL = −2dB therefore, X_{dB} = +10, R_{FLT} = 1.5k. The results are: R_{EXT} = 1.41k, R_{SHUNT} = 4.08k

IF noise figure

The IF noise figure of the receiver may be expected to provide at best a 7.7dB noise figure in a 1.5kΩ environment from about 25kHz to 100MHz. From a 25Ω source the noise figure can be expected to degrade to about 15.4db.

Performance Graphs of IF Section

Fig.	Description
24	IF Amp Gain vs. Temperature with Various Supply Voltages
25	IF Limiter Gain vs. Temperature with Various Supply Voltages
26	IF Amp 20MHz Response vs. Temperature
27	IF Limiter 20MHz Response vs. Temperature

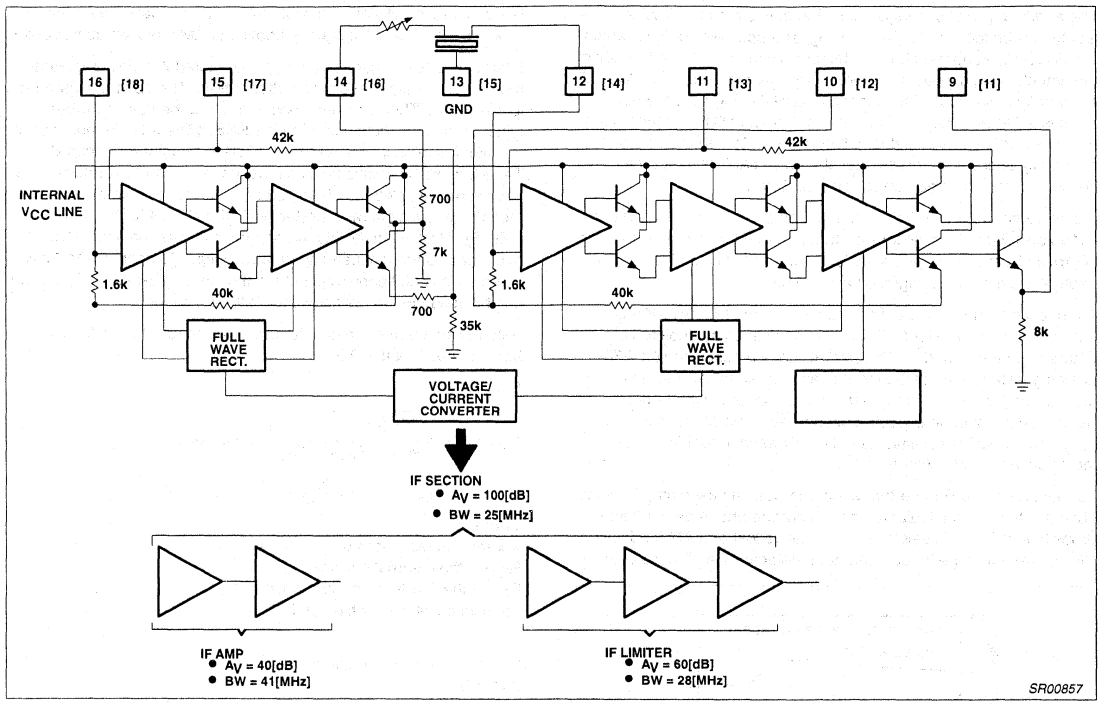


Figure 18. IF Section of NE604A [NE605]

Demodulator Section

Once the signal leaves the IF limiter, it must be demodulated so that the baseband signal can be separated from the IF signal. This is accomplished by the quadrature detector. The detector is made up of a phase comparator (internal to theNE605) and a quadrature tank (external to theNE605).

The phase comparator is a multiplier cell, similar to that of a mixer stage. Instead of mixing two different frequencies, it compares the phases of two signals of the same frequency. Because the phase comparator needs two input signals to extract the information, the IF limiter has a balanced output. One of the outputs is directly connected to the input of the phase comparator. The other signal from the limiter's output (Pin 11) is phase shifted 90 degrees (through external components) and frequency selected by the quadrature tank. This signal is then connected to the other input of the phase comparator (Pin 10 of the NE605). The signal coming out of the quadrature detector (phase detector) is then low-passed filtered to get the baseband signal. A mathematical derivation of this can be seen in the NE604A data sheet.

The quadrature tank plays an important role in the quality of the baseband signal. It determines the distortion and the audio output amplitude. If the "Q" is high for the quadrature tank, the audio level will be high, but the distortion will also be high. If the "Q" is low, the distortion will be low, but the audio level will become low. One can conclude that there is a trade-off.

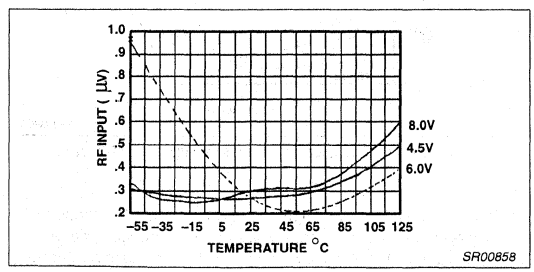


Figure 19. NE605 Application Board, –3dB Limiting (Drop in Audio)

Output Section

The output section contains an RSSI, audio, and data (unmuted audio) outputs which can be found on Pins 7, 8, and 9, respectively, on the NE605. However, amplitude shift keying (ASK), frequency shift keying (FSK), and a squelch control can be implemented from these pins. Information on ASK and FSK can be found in Philips Semiconductors application note AN1993.

Although the squelch control can be implemented by using the RSSI output, it is not a good practice. A better way of implementing squelch control is by comparing the bandpassed audio signal to high

frequency colored FM noise signal from the unmuted audio. When no baseband signal is present, the noise coming out of the unmuted audio output will be stronger, due to the nature of FM noise. Therefore, the output of the external comparator will go high (connected to Pin 5 of the NE605) which will mute the audio output. When a baseband signal is present, the bandpassed audio level will dominate and the audio output will now unmute the audio.

Audio and Unmuted Audio (Data)

The audio and unmuted audio outputs (Pin 8 and 9, respectively, on the NE605) will be discussed in this section because they are basically the same. The only difference between them is that the unmuted audio output is always "on" while the audio output can either be turned "on" or "off". The unmuted audio output (data out) is for signaling tones in systems such as cellular radio. This allows the tones to be processed by the system but remain silent to the user. Since these tones contain information for cellular operation, the unmuted audio output can also be referred to as the "data" output. Grounding Pin 5 on the NE605 mutes the audio on Pin 8 (connecting Pin 5 to V_{CC} unmutes it).

Both of these outputs are PNP current-to-voltage converters with a 55kΩ nominal internal load. The nominal frequency response of the audio and data outputs are 300kHz. However, this response can be increased with the addition of an external resistor (<58kΩ) from the output pins to ground. This will affect the time constant and lower the audio's output amplitude. This technique can be applied to SCA receivers and data transceivers (as mentioned in the NE604A data sheet).

RSSI Output

RSSI (Received Signal Strength Indicator) determines how well the received signal is being captured by providing a voltage level on its output. The higher the voltage, the stronger the signal.

The RSSI output is a current-to-voltage converter, similar to the audio outputs. However, a 91kΩ external resistor is needed to get an output characteristic of 0.5V for every 20dB change in the input amplitude.

As mentioned earlier, the linearity of the RSSI curve depends on the 12dB insertion loss between the IF amplifier and IF limiter. The reason the RSSI output is dependent on the IF section is because of the V/I converters. The amount of current in this section is monitored to produce the RSSI output signal. Thus, the IF amplifier's rectifier is internally calibrated under the assumption that the loss is 12dB.

Because unfiltered signals at the limiter inputs, spurious products, or regenerated signals will affect the RSSI curve, the RSSI is a good indicator in determining the stability of the board's layout. With no signal applied to the front end of the NE605, the RSSI voltage level should read 250mV_{RMS} or less to be a good layout. If the voltage output is higher, then this could indicate oscillations or regeneration in the design.

Referring to the NE/SA604A data sheet, there are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can be accomplished by adding attenuation between stages. More details on regeneration and stability considerations can be found in the NE/SA604A data sheet.

Performance Graphs of Output Section

Fig.	Description
28	51kΩ Thermistor in Series with 100kΩ Resistor Across Quad Tank (Thermistor Quad Q Compensation)
29a	NE605 Application Board at –55°C
29b	NE605 Application Board at –40°C
29c	NE605 Application Board at +25°C
29d	NE605 Application Board at +85°C
29e	NE605 Application Board at +125°C
30a	NE604A for –68dBm RSSI Output vs. Temperature at Different Supply Voltages
30b	NE604A for –18dBm RSSI Output vs. Temperature at Different Supply Voltages
30c	NE605 for –120dBm RSSI Output vs. Temperature at Different Supply Voltages
30d	NE605 for –76dBm RSSI Output vs. Temperature at Different Supply Voltages
30e	NE605 for –28dBm RSSI Output vs. Temperature at different Supply Voltages
31	NE605 Audio level vs. Temperature and Supply Voltage
32	NE605 Data Output at –76dBm vs. Temperature

III. QUESTIONS & ANSWERS:

Q.–Bypass. How important is the effect of the power supply bypass on the receiver performance?

A. While careful layout is extremely critical, one of the single most neglected components is the power supply bypass in applications of NE604A or NE605. Although increasing the value of the tantalum capacitor can solve the problem, more careful testing shows that it is actually the capacitor's ESR (Equivalent Series Resistance) that needs to be checked. The simplest way of screening the bypass capacitor is to test the capacitor's dissipation factor at a low frequency (a very easy test, because most of the low frequency capacitance meters display both C, and Dissipation factor).

Q.–On-chip oscillator. We cannot get the NE605 on-chip oscillator to work. What is the problem?

A. The on board oscillator is just one transistor with a collector that is connected to the supply, an emitter that goes to ground through a 25k resistor, and a base that goes to the supply through an 18k resistor. The rest of the circuit is a buffer that follows the oscillator from the transistor base (this buffer does not affect the performance of the oscillator).

Fundamental mode Colpitts crystal oscillators are good up to 30MHz and can be made by a crystal and two external capacitors. At higher frequencies, up to about 90MHz, overtone crystal oscillators (Colpitts) can be made like the one in the cellular application circuit. At higher frequencies, up to about 170MHz, Butler type oscillators (the crystal is in series mode) have been successfully demonstrated. Because of the 8GHz peak f_T of the transistors, LC Colpitts oscillators have been shown to work up to 900MHz. The problem encountered above 400MHz is that the on-chip oscillator level is not sufficient for optimum conversion gain of the mixer. As a result, an external oscillator should be used at those frequencies.

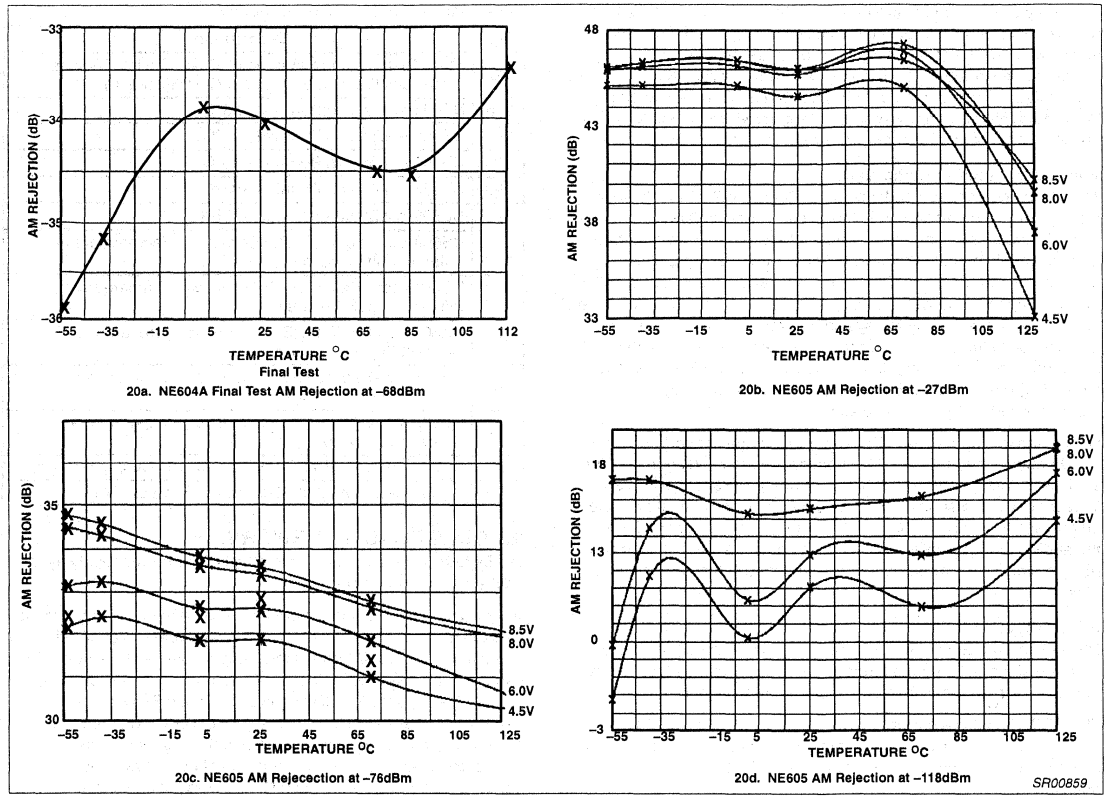


Figure 20. AM Rejection Results at Different Input Levels

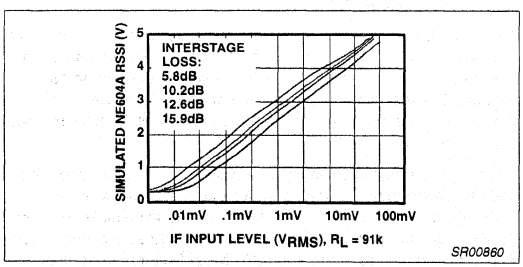


Figure 21. NE604A's RSSI Curve at Different Interstage Losses

Generally, about 220mV$_{RMS}$ is the oscillator level needed on Pin 4 for maximum conversion gain of the mixer. An external oscillator driving Pin 4 can be used throughout the band. Finally, since the NE605's oscillator is similar to the NE602, all of the available application notes on NE602 apply to this case (assuming the pin out differences are taken into account by the user).

Below are a couple of points to help in the oscillator design. The oscillator transistor is biased around 250μA which makes it very hard to probe the base and emitter without disturbing the oscillator (a high impedance, low capacitance active FET probe is desirable).

To solve these problems, an external 22k resistor (as low as 10k) can be used from Pin 3 to ground to double the bias current of the oscillator transistor. This external resistor is put there to ensure the start up of the crystal in the 80MHz range, and to increase the f_T of the transistor for above 300–400MHz operation. Additionally, this resistor is required for operations above 80–90MHz. When a 1k resistor from Pin 1 to ground is connected on the NE605, half of the mixer will shut off. This causes the mixer to act like an amplifier. As a result, Pin 20 (the mixer, now amplifier output) can be probed to measure the oscillator frequency. Furthermore, the signal at Pin 20 relates to the true oscillator level . This second resistor is just for optimizing the oscillator of course. Without the 1k resistor, the signal at Pin 20 will be a LO feedthrough which is very small and frequency dependent.

Finally in some very early data sheets, the base and emitter pins of the oscillator were inadvertently interchanged. The base pin is Pin 4, and the emitter pin is Pin 3. Make sure that your circuit is connected correctly.

Q.–Sensitivity at higher input frequencies. We cannot get good sensitivity like the 45MHz case at input frequencies above 70MHz. Do you have any information on sensitivity vs. input frequency?

A. The noise figure and the gain of the mixer degrade by less than 0.5dB, going from 50 to 100MHz. Therefore, this does not explain the poor degradation in sensitivity. If other problems such as layout, supply bypass etc. are already accounted for, the source of the problem can be regeneration due to the 70MHz oscillator. What is probably happening is that the oscillator signal is feeding through the IF, getting mixed with the 455kHz signal, causing spurious regeneration. The solution is to reduce the overall gain to stop the regeneration.

This gain reduction can be done in a number of places. Two simple points are the attenuator network before the second filter and the LO level (see Figure 22). The second case will reduce the mixer's noise figure which is not desirable. Therefore, increasing the Interstage loss, despite minimal effect on the RSSI linearity, is the correct solution. As the Interstage loss is increased, the regeneration problem is decreased, which improves sensitivity, despite lowering of the over-all gain (the lowest RSSI level will keep decreasing as the regeneration problem is decreased). For an 81MHz circuit it was found that increasing the Interstage loss from 12dB to about 17dB produced the best results (–119dBm sensitivity). Of course, adding any more Interstage loss will start degrading sensitivity.

Conversely, dealing with the oscillator design, low LO levels could greatly reduce the mixer conversion gain and cause degradation of the sensitivity. For the 81MHz example, a 22k parallel resistor from Pin 3 to ground is required for oscillator operation where a Colpitts oscillator like the one in the cellular application circuit is used. The LO level at Pin 4 should be around $220mV_{RMS}$ for good operation. Lowering the LO level to approximately $150mV_{RMS}$ may be a good way of achieving stability if increasing Interstage attenuation is not acceptable. In that case the 22k resistor can be made a thermistor to adjust the LO level vs. temperature for maintaining sensitivity and ensuring crystal start-up vs. temperature. At higher IF frequencies (above 30MHz), the interstage gain reduction is not needed. The bandwidth of the IF section will lower the overall gain. So, the possibility of regeneration decreases.

Q.–Mixer noise figure. How do you measure the mixer noise figure in NE605, and NE602?

A. We use the test circuit shown in the NE602 data sheet. The noise figure tester is the HP8970A. The noise source we use is the HP346B (ENR = 15.46dB). Note that the output is tuned for 10.7MHz. From that test circuit the NF-meter measures a gain of approximately 15dB and 5.5dB noise figure.

More noise figure data is available in the paper titled "Gilbert-type Mixers vs. Diode Mixers" presented at RF Expo '89 in Santa Clara, California. (Reprints available through Philips Semiconductors Publication Services.)

Q.– What is the value of the series resistor before the IF filter in the NE605 or NE604A applications?

A. A value of 5.1kΩ has been used by us in our demo board. This results in a maximally straight RSSI curve. A lower value of about 1k will match the filter better. A better solution is to use an L pad as discussed earlier in this application note.

Q.– What is the low frequency input resistance of the NE605?

A. The data sheets indicated a worst case absolute minimum of 1.5k. The typical value is 4.7k.

Q.– What are BE-BC capacitors in the NE605 oscillator transistor?

A. The oscillator is a transistor with the collector connected to the supply and the emitter connected to the ground through a 25k resistor. The base goes to the supply through an 18k resistor. The junction capacitors are roughly about 24fF (fempto Farads) for CJE (Base-emitter capacitors), and 44fF for CJC (Collector-base capacitors). There is a 72fF capacitor for CJS (Collector-substrate capacitor). This is all on the chip itself. It should be apparent that the parasitic packaging capacitors (1.5–2.5pF) are the dominant values in the oscillator design.

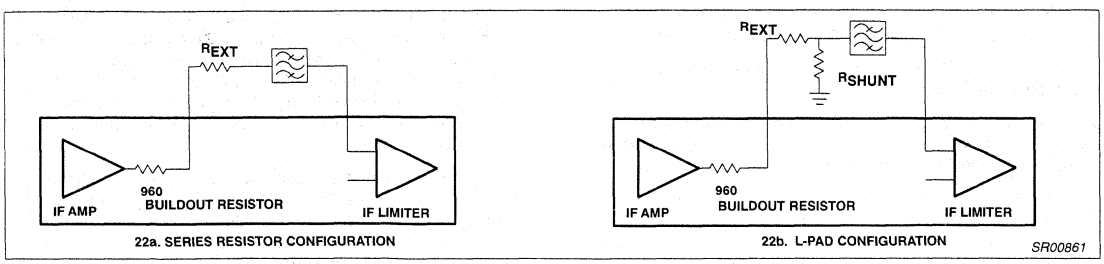


Figure 22. Implementing the 12dB Insertion Loss

Summary of Differences for NE/SA604/604A

	NE/SA604	NE/SA604A
RSSI	No temperature compensation	Internally temperature compensated
IF Bandwidth	15MHz	25MHz
IF Limiter Output	No buffer	Emitter follower buffer output with 8k in the emitter
Current Drain	2.7mA	3.7mA

Reviewing key areas when designing with the NE605

AN1994

Q.– What are the differences between the NE604 and NE604A? (see Table below)

A. The NE/SA604A is an improved version of the NE/SA604. Customers, who have been using the NE604 in the past, should have no trouble doing the conversion.

The main differences are that the small signal IF bandwidth is 25MHz instead of 15MHz, and the RSSI is internally temperature compensated. If external temperature compensation was used for the NE604, the designer can now cut cost with the NE604A. The designer can either get rid of these extra parts completely or replace the thermistor (if used in original temperature compensated design) with a fixed resistor.

Those using the NE604 at 455kHz should not see any change in performance. For 10.7MHz , a couple of dB improvement in performance will be observed. However, there may be a few cases where instability will occur after using NE604A. This will be the case if the PC-board design was marginal for the NE604 in the first place. This problem, however, can be cured by using a larger than 10µF tantalum bypass capacitor on the supply line, and screening the capacitors for their ESR (equivalent series resistance) as mentioned earlier. The ESR at 455kHz should be less than 0.2Ω. Since ESR is a frequency dependent value, the designer can correlate good performance with a low frequency dissipation factor, or ESR measurement, and screen the tantalum capacitors in production. There are some minor differences as well. The NE/SA604A uses about 1mA more current than the NE/SA604. An emitter follower has been added at the limiter output to present a lower and more stable output impedance at Pin 9. The DC voltage at the audio and data outputs is approximately 3V instead of 2V in the NE604, but that should not cause any problems. The recovered audio level, on the other hand, is slightly higher in the NE604A which should actually be desirable. Because of these changes, it is now possible to design 21.4MHz IFs using the NE604A, which was not possible with the NE604.

The two chips are identical, otherwise. The customers are encouraged to switch to the NE604A because it is a more advanced bipolar process than the previous generation used in theNE604. As a result we get much tighter specifications on the NE604A.

Q.– How does the NE605 mixer compare with a typical double balanced diode mixer?

A. Some data on the comparison of the conversion gain and LO power requirements are shown in this application note. These two parameters reveal the advantages in using the NE605 mixer.

The only drawback of the NE605 may seem to be its lower third-order intercept point in comparison to a diode mixer. But, this is inherent in the NE605 as a result of the low power consumption. If one compares the conversion gain of the NE605 with the conversion loss of a low cost diode mixer, it turns out that the third-order intercept point, referred to the output, is the same or better in the NE605. Another point to take into account is that a diode mixer cannot be used in the front end of a receiver without a preamp due to its poor noise figure. A third-order intercept analysis shows that the intercept point of the combination of the diode mixer and preamp will be degraded at least by the gain of the preamp. A preamp may not be needed with NE605 because of its superior noise figure.

For more detailed discussion of this topic please refer to the paper titled "Gilbert-type Mixers vs. Diode Mixers").

Q.– How can we use the NE605 for SCA FM reception?

A. The 10.7MHz application circuit described in AN1993 can be used in this case. The LO frequency should be changed and the RF front-end should be tuned to the FM broadcast range. The normal FM signal, coming out of Pin 8 of the NE605, could be expected to have about 1.5µV (into 50Ω) sensitivity for 20dB S/N. This signal should be band-pass filtered and amplified to recover the SCA sub-carrier. The output of that should then go to a PLL SCA decoder, shown on the data sheet of Philips Semiconductors NE565 phase lock loop, to demodulate the base-band audio. The two outputs of the NE605 Pins 8 and 9 can be used to receive SCA data as well as voice, or features such as simultaneous reception of both normal FM, and SCA. The RSSI output, with its 90dB dynamic range, is useful for monitoring signal levels.

Q.– What is the power consumption of the NE605 or NE604A vs. temperature and V_{CC}?

A. The NE605 consumes about 5.6mA of current at 6V. This level is slightly temperature and voltage dependent as shown in Figure 33. Similar data for the NE604A is shown in Figure 34.

Q.– How can you minimize RF and LO feedthroughs

A. The RF and LO feedthroughs are due to offset voltages at the input of the mixer's differential amplifiers and the imbalance of the parasitic capacitors. A circuit, such as the one shown in Figure 35, can be used to adjust the balance of the differential amplifiers. The circuit connected to Pins 1 and 2 will minimize RF feedthrough while the circuit shown connected to Pin 6 will adjust the LO feedthrough. The only limitation is that if the RF and LO frequencies are in the 100MHz range or higher, these circuits will probably be effective for a narrow frequency range.

Q.– Distortion vs. RF input level. We get a good undistorted demodulated signal at low RF levels, but severe distortion at high RF levels. What is happening?

A. This problem usually occurs at 10.7MHz or at higher IF's. The IF filters have not been properly matched on both sides causing a sloping IF response. The resulting distortion can be minimized by adjusting the quad tank at the FM threshold where the IF is out of limiting. As the RF input increases, the IF stages will limit and make the IF response flat again. At this point, the effect of the bad setting of the quad tank will show itself as distortion. The solution is to always tune the quad tank for distortion at a medium RF level, to make sure that the IF is fully limited. Then, to avoid excessive distortion for low RF levels, one should make sure that the IF filters are properly matched.

Q.–The most commonly asked questions: "Why doesn't the receiver sensitivity meet the specifications?"; "Why is the RSSI dynamic range much less than expected?"; "Why does the RSSI curve dip at 0.9V and stay flat at 1V as the RF input decreases?"; "Why does the audio output suddenly burst into oscillation, or output wideband noise as the RF input goes down, instead of dying down slowly?"; "When looking at the IF output with a spectrum analyzer, why do high amplitude spurs become visible near the edge of the IF band as the RF level drops?"

A. These are the most widely observed problems with the NE605. They are all symptoms of the same problem; instability. The instability is due to bad layout and grounding.

Regenerative instability occurs when the limiter's output signals are radiated and picked up by the high impedance inputs of the mixer and IF amp. This signal is amplified by both the IF amp and limiter. Positive feedback causes the signal to grow until the signal at the limiter's output becomes limited. Due to the nature of FM, this

instability will dominate any low RF input levels and capture the receiver (see Figure 23).

Since the receiver behaves normally for high RF inputs, it misleads the designer into believing that the design is okay. Additionally the RSSI circuit cannot determine whether the signal being received is coming from the antenna or the result of regenerative instability. Therefore, RSSI will be a good instability indicator in this instance because the RSSI will stay at a high level when the received signal decreases. Looking at the IF spectrum (Pin 11 for 605, Pin 9 for 604A) with the RF carrier present (no modulation), the user will see a shape as shown below. When regenerative instability occurs, the receiver does not seem to have the ultimate sensitivity of which it is capable.

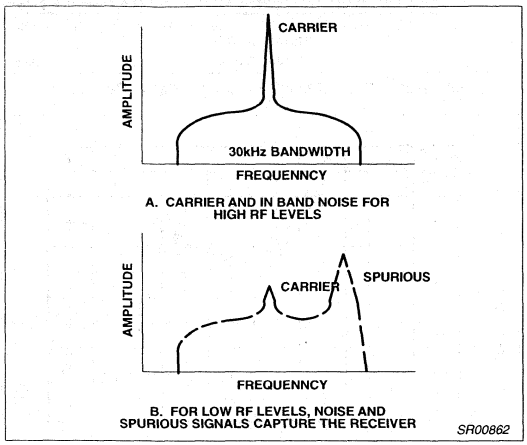


Figure 23.

Make sure that a double sided layout with a good ground plane on both sides is used. This will have RF/IF loops on both sides of the board. Follow our layouts as faithfully as you can. The supply bypass should have a low ESR 10–15µF tantalum capacitor as discussed earlier. The crystal package, the inductors, and the quad tank shields should be grounded. The RSSI output should be used as a progress monitor even if is not needed as an output. The lowest RSSI level should decrease as the circuit is made more stable. The overall gain should be reduced by lowering the input impedance of the IF amplifier and IF limiter, and adding attenuation after the IF amplifier, and before the 2nd filter. A circuit that shows an RSSI of 250mV or less with no RF input should be considered close to the limit of the performance of the device. If the RSSI still remains above 250mV, the recommendations mentioned above should be revisited.

Q.– Without the de-emphasis network at the audio output, the –3dB bandwidth of the audio output is limited to only 4.5kHz. The maximum frequency deviation is 8kHz, and the IF bandwidth is 25kHz. What is the problem?

A. What is limiting the audio bandwidth in this case is not the output circuit, but the IF filters. Remember that Carson's rule for FM IF bandwidth requires the IF bandwidth to be at least:

2(Max frequency Dev. + Audio frequency)

With a 25kHz IF bandwidth and 8kHz frequency deviation, the maximum frequency that can pass without distortion is approximately 4.5kHz. 2(8kHz + 4.5kHz) is 25kHz as expected.

REFERENCES:

"High-Performance Low-Power FM IF System" (NE604A data sheet), Philips Semiconductors Linear Data Manual, Philips Semiconductors, 1988.

"AN199-Designing with the NE/SA604", Philips Semiconductors Linear Data Manual, 1987.

"AN1981–New Low Power Single Sideband Circuits", Philips Semiconductors Linear Data Manual, 1988.

"Applying the Oscillator of the NE602 in Low Power Mixer Applications", Philips Semiconductors Linear Data Manual, 1988.

"AN1993–High Sensitivity Applications of Low-Power RF/IF Integrated Circuits", Philips Semiconductors Linear Data Manual, 1988.

"RF Circuit Design", Bowick. C., Indiana: Howard W. Sams & Company, 1982.

"The ARRL Handbook for the Radio Amateur", American Radio Relay League, 1986.

"Communications Receivers: Principles & Design", Rohde, U., Bucher, T.T.N., McGraw Hill, 1988.

"Gilbert-type Mixers vs. Diode Mixers", proceedings of R.F. Expo 1989, Fotowat, A., Murthi, E., pp. 409-413.

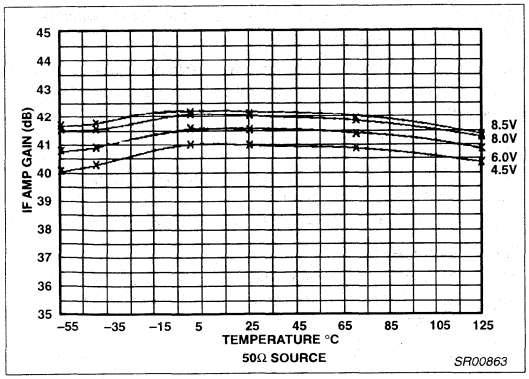


Figure 24. IF Amplifier Gain

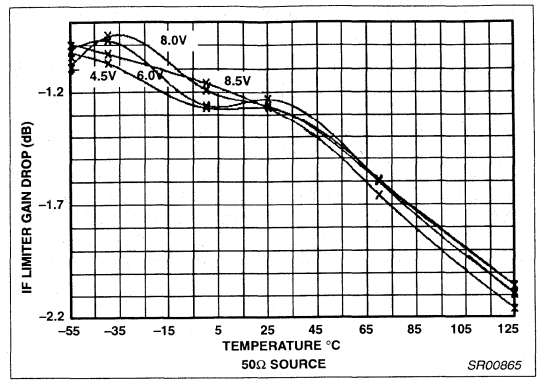


Figure 26. IF Amplifier Gain Drop, 20MHz Response

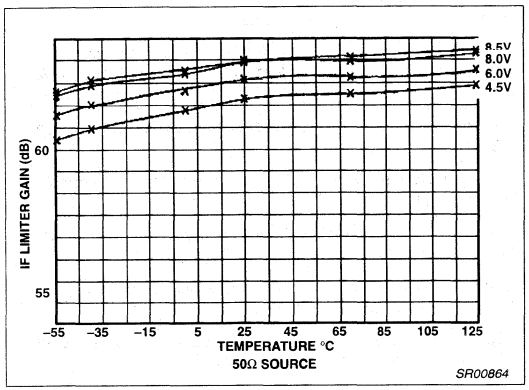


Figure 25. IF Limiter Gain

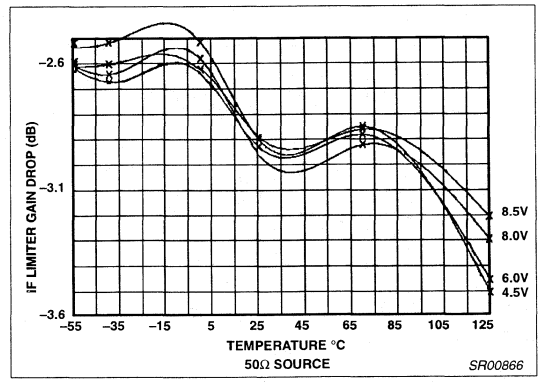


Figure 27. IF Limiter Drop, 20MHz Response

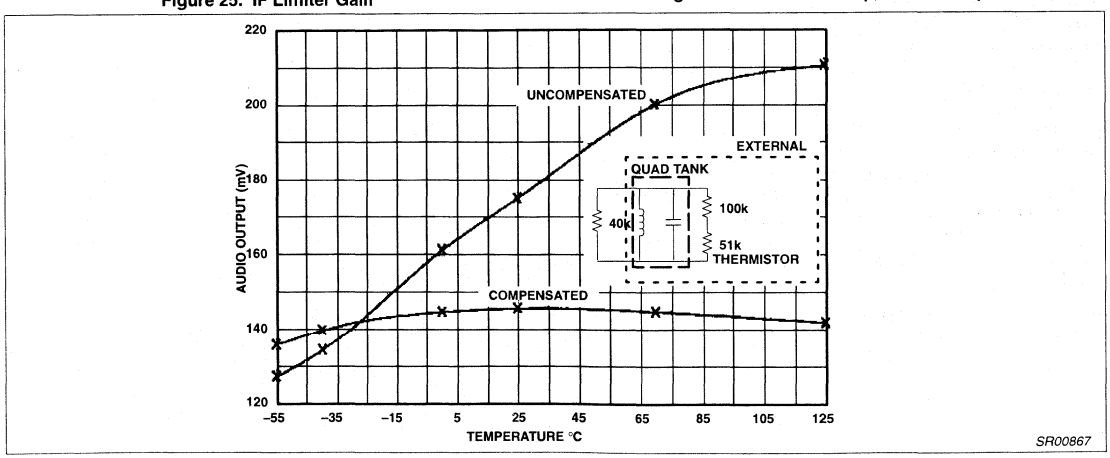
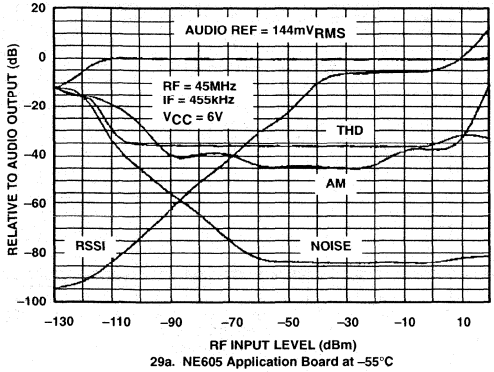
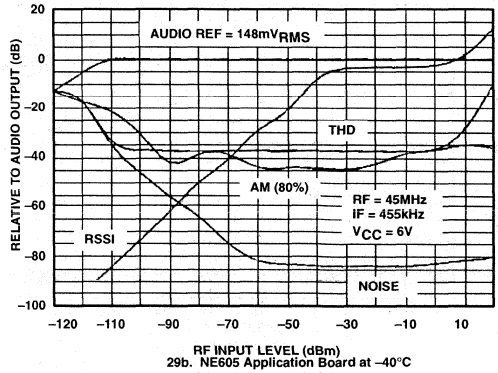


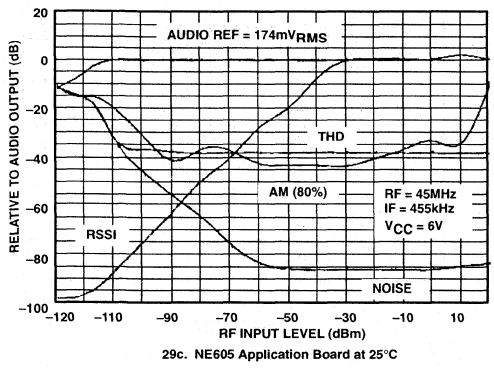
Figure 28. Audio Output: Compensated vs Uncompensated



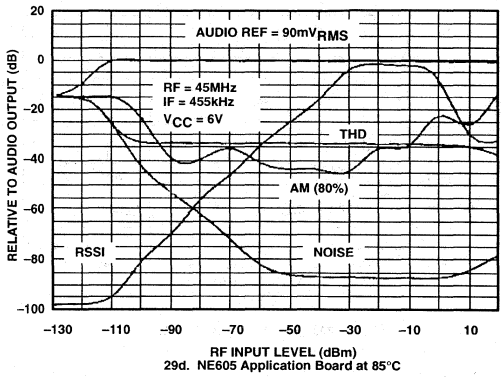
29a. NE605 Application Board at –55°C



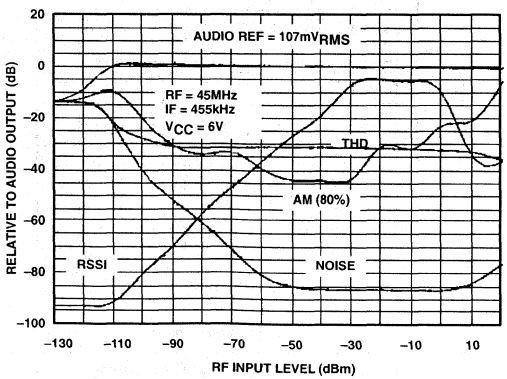
29b. NE605 Application Board at –40°C



29c. NE605 Application Board at 25°C



29d. NE605 Application Board at 85°C



29e. NE605 Application Board at 125°C

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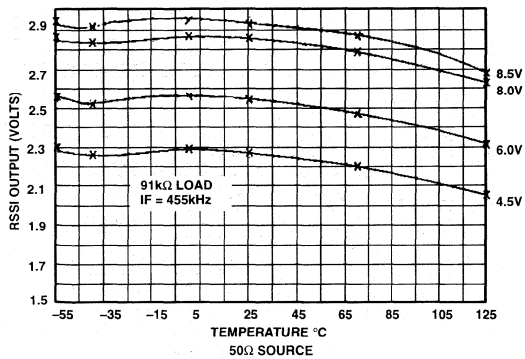
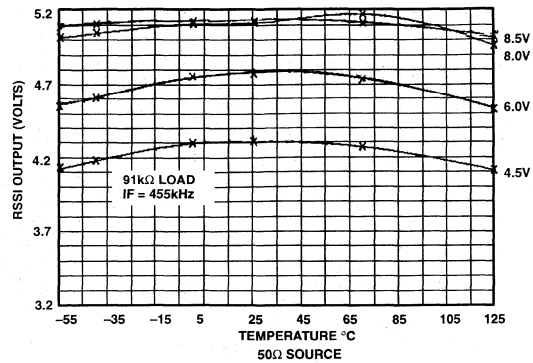
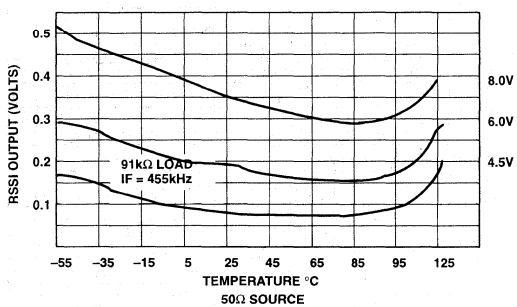
Figure 29. Performance of the NE605 Application Board at Different Temperatures



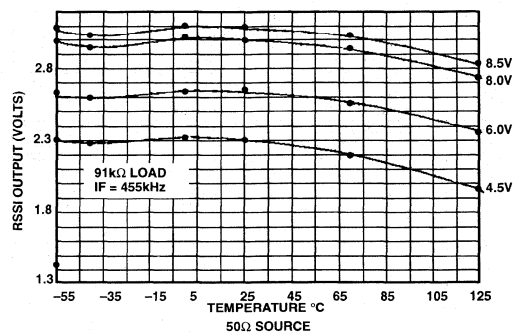
30a. NE604A for –68dBm, RSSI Output



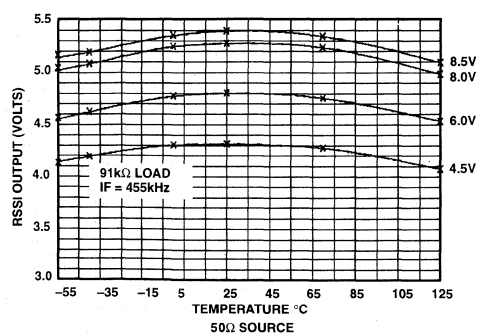
30b. NE604A for –18dBm, RSSI Output



30c. NE605 RSSI at –120dBm



30d. NE605 RSSI, –76dBm



30e. NE605 RSSI at –28dBm

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Figure 30. RSSI Response for Different Inputs

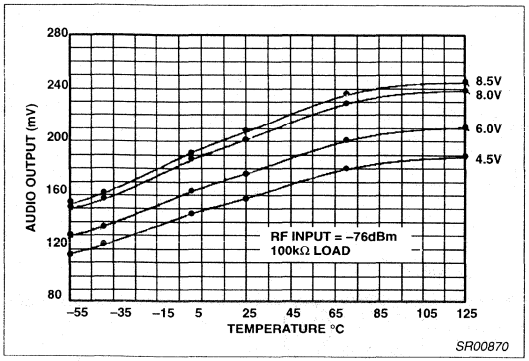


Figure 31. Audio Level vs Temperature and Supply Voltage

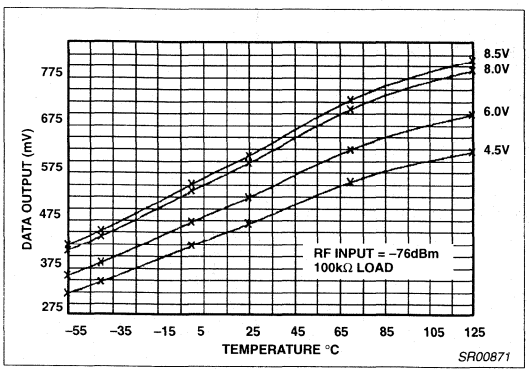


Figure 32. Data Level vs Temperature and Supply Voltage

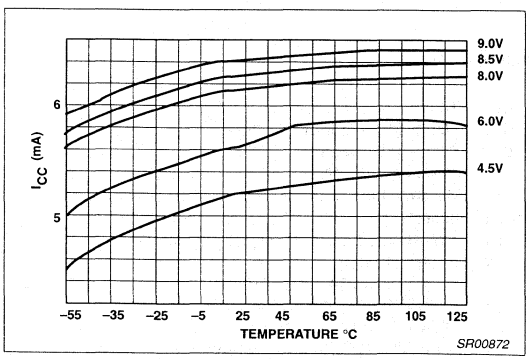


Figure 33. NE605 I_{CC} vs Temperature

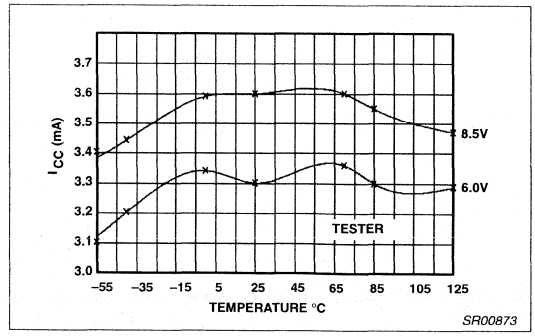


Figure 34. NE604A I_{CC} vs Temperature

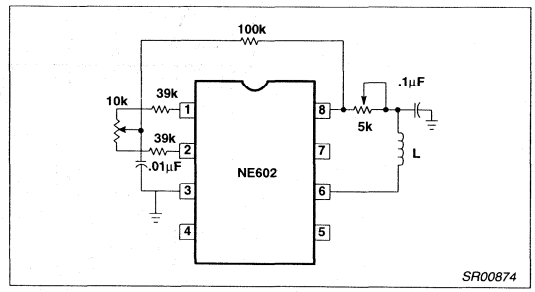
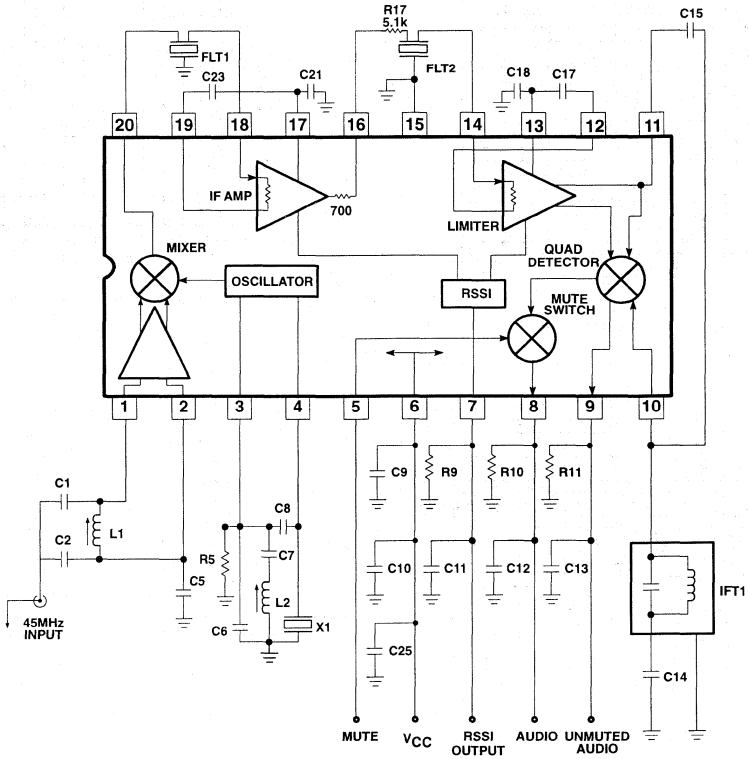


Figure 35. Minimizing RF and LO Feedthrough



Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	3.3μH nominal Toko 292CNS–T1046Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

* NOTE: This value can be reduced when a battery is the power source.

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Figure 36. NE/SA605 45MHz Application Circuit

Table 1. Related Application Notes

App. Note	Date	Title	Main Topics
AN198	Feb. 1987	Designing with the NE/SA602	– Advantages/Disadvantages to single-ended or balanced matching
AN1981	Dec. 1988	New Low Power Single Sideband Circuits	– General discussion on SSB circuits – Audio processing – Phasing-filter technique
AN1982	Dec. 1988	Applying the Oscillator of the NE602 in Low Mixer Applications	– Oscillator configurations
AN199	Feb. 1987	Designing with the NE/SA604	Circuits of: – AM synchronous det. – Temp. compensated RSSI circuit – Field strength meter – Product detector
AN1991	Dec. 1988	Audio Decibel Level Detector with Meter Driver	– Uses of the 604 in application
AN1993	Dec. 1988	High Sensitivity Application Low-Power RF/IF Integrated Circuits	– An overview of the NE602 and NE604 in typical applications – Good information before getting started

Table 2. Comparing Balanced vs Unbalanced Matching

NE605 or NE602	Matching	Advantages	Disadvantages
Pins 1 and 2 (RF input)	Single-ended (unbalanced)	– Very simple circuit – No sacrifice in 3rd-order performance	– Increase in 2nd-order products
	Balanced	– Reduce 2nd-order products	– Impedance match difficult to achieve

Table 3. LO Configurations

LO (MHz)	Suggested Configuration Using On-board Oscillator
0 - 30	Fundamental mode, use Colpitts
30 - 70	3rd overtone mode, use Colpitts
70 - 90	3-5th overtone mode, use Colpitts with 22kΩ resistor connected from the emitter pin to ground
90 - 170	Use Butler, crystal in series mode, and a 22kΩ resistor connected from the emitter pin to ground
170 - 300	LC configuration

Evaluating the NE605 SO and SSOP demo-board AN1995

Author: Alvin K. Wong

INTRODUCTION

With the increasing demand for smaller and lighter equipment, designers are forced to reduce the physical size of their systems. There are several approaches to solving the size problem. A designer needs to look for sophisticated integrated single chip solutions, chips that are smaller in size, and chips that require minimum external components.

Philips Semiconductors offers all of these solutions in their NE605. The NE605 single-chip receiver converts the RF signal to audio and is available in three packages: DIP,SO, and SSOP. This offers total flexibility for layout considerations. The SSOP package is the smallest 20 pin package available in the market today, and allows the designer the flexibility to reduce the overall size of a layout.

When working with a smaller and tighter layout in a receiver design, it becomes important to follow good RF techniques. This application note shows the techniques used in the SO and SSOP demo-board. It does not cover the basic functionality of the NE605 but instead focuses more on the layout constraints. This application note also has a trouble-shooting chart to aid the designer in evaluating the SO and SSOP demo-board. For a complete explanation of the NE605, please refer to application note AN1994 which describes the basic block diagrams, reviews the common problems encountered with the NE605, and suggests solutions to them. Reading AN1994 is highly recommended before attempting the SO and SSOP layout.

The recommended layout demonstrates how well the chip can perform. But it should be pointed out that the combination of external parts with their tolerances plays a role in achieving maximum sensitivity.

The minimum and maximum 12dB SINAD measurement for both boards is -118dBm and -119.7dBm, respectively. A typical reading taken in the lab for both SO and SSOP demo-boards is -119dBm.

There were two different design approaches for both layouts. For the SO layout, there are inductive tuning elements (except for the LO section); for the SSOP layout there are capacitive tuning elements. This approach was taken to show the designer that both ways can be used to achieve the same 12dB SINAD measurement. However, it is worth mentioning that capacitive tuning elements are less expensive than the inductive tuning elements.

Packages Available

As mentioned above, there are three packages available for the NE605. See the "Package Outline" section of the Philips Semiconductors 1992 RF Handbook for the physical dimensions of all three packages. Notice that the DIP package is the largest of the three in physical size; the SSOP is the smallest. The recommended layout and performance graphs for the DIP package are shown in the NE605 data sheet and AN1994. But the SO and SSOP recommended layout and performance graphs are shown in this application note.

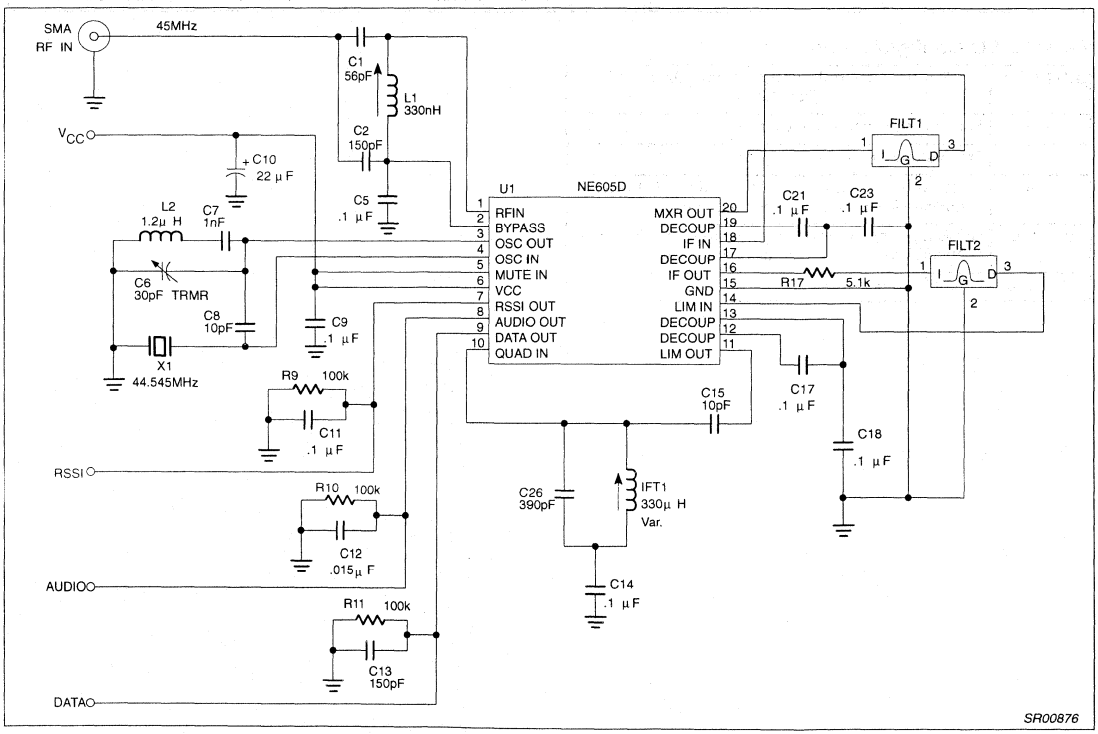


Figure 1. NE605 Schematic for the SO Layout

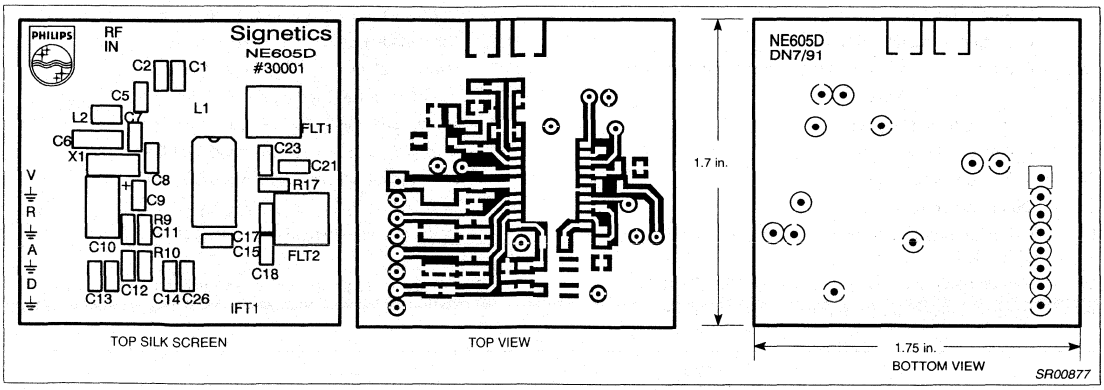


Figure 2. NE605 SO Demo-board Layout (Not Actual Size)

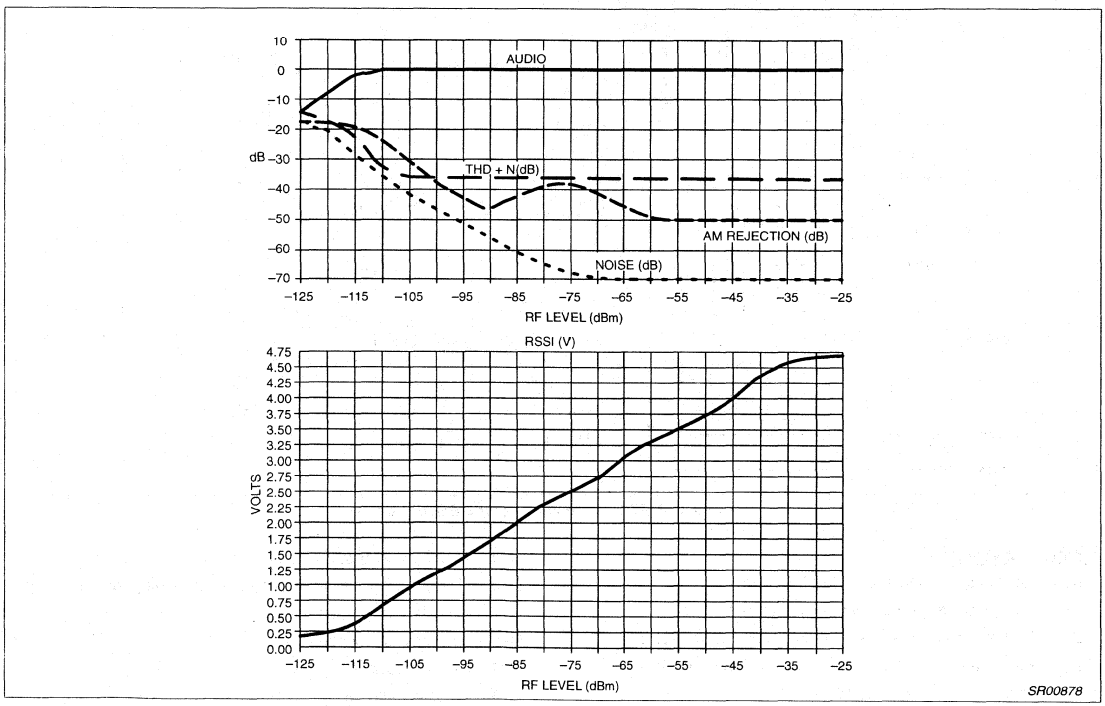


Figure 3. NE605 SO Performance Curves

SO LAYOUT:

Figure 1 shows the schematic for the SO layout. Listed below are the basic functions of each external component for Figure 1.

C1 – Part of the tapped-C network to match the front-end

C2 – Part of the tapped-C network to match the front-end

C5 – Used as an AC short to Pin 2

C6 – Used to tune the LO for the Colpitts oscillator

C7 – Used as part of the Colpitts oscillator

C8 – Used as part of the Colpitts oscillator

C9 – Supply bypassing

C10 – Supply bypassing

C11 – Used as filter

C12 – Used as filter

C13 – Used as filter
C14 – Used to AC ground the Quad tank
C15 – Used to provide the 90° phase shift to the phase detector
C17 – IF limiter decoupling cap
C18 – IF limiter decoupling cap
C21 – IF amp decoupling cap
C23 – IF amp decoupling cap
C26 – Quad tank component
L1 – Part of tapped-C network to match the front-end TOKO 5CB-1320Z
L2 – Part of the Colpitts oscillator Coilcraft 1008CS-122
R9 – Used to convert the current into the RSSI voltage
R10 – Converts the audio current to a voltage
R11 – Converts the data current to a voltage
R17 – Used to achieve the –12dB insertion loss
IFT1 – Inductor for the Quad tank TOKO 303LN-1130
FILT1 – Murata SFG455A3 455kHz bandpass filter
FILT2 – Murata SFG455A3 455kHz bandpass filter
X1 – Standard 44.545MHz crystal in QC38 package

The recommended SO layout can be found in Figure 2 and should be used as an example to help designers get started with their projects.

The SO NE605 board performance graphs can be found in Figure 3.

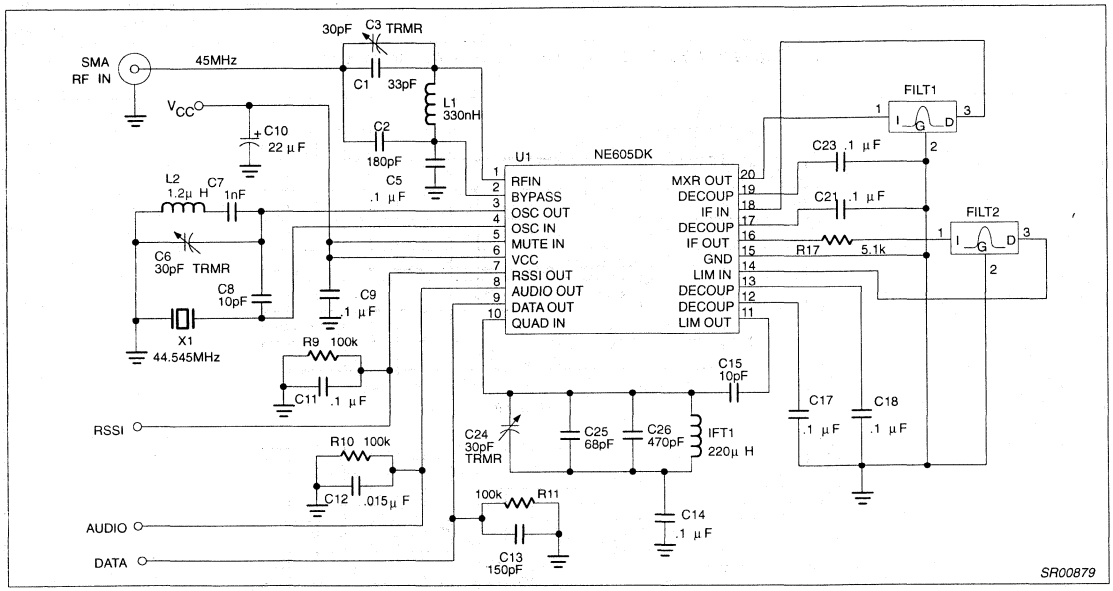


Figure 4. NE605 Schematic for the SSOP Layout

SSOP LAYOUT:

Figure 4 shows the schematic for the SSOP layout.

C1 – Part of the tapped-C network to match the front-end
C2 – Part of the tapped-C network to match the front-end
C3 – Part of the tapped-C network to match the front-end
C5 – Used as an AC short to Pin 2
C6 – Used to tune the LO for the Colpitts oscillator
C7 – Used as part of the Colpitts oscillator
C8 – Used as part of the Colpitts oscillator
C9 – Supply bypassing
C10 – Supply bypassing
C11 – Used as filter
C12 – Used as filter
C13 – Used as filter
C14 – Used to AC ground the Quad tank
C15 – Used to provide the 90° phase shift to the phase detector
C17 – IF limiter decoupling cap
C18 – IF limiter decoupling cap
C21 – IF amp decoupling cap
C23 – IF amp decoupling cap
C24 – Part of the Quad tank
C25 – Part of the Quad tank
C26 – Part of the Quad tank
L1 – Part of tapped-C network to match the front-end Coilcraft 1008CS-331
L2 – Part of the Colpitts oscillator Coilcraft 1008CS-122
R9 – Used to convert the current into the RSSI voltage
R10 – Converts the audio current to a voltage

R11 – Converts the data current to a voltage

R17 – Used to achieve the –12dB insertion loss

IFT1 – Inductor for the Quad tank Mouser ME435-2200

FILT1 – Murata SFGCC455BX 455kHz bandpass filter

FILT2 – Murata SFGCC455BX 455kHz bandpass filter

X1 – Standard 44.545MHz crystal

The SSOP layout can be found in Figure 5. The SSOP NE605 board performance graphs can be found in Figure 6.

The main difference between the SO and SSOP demo-boards is that the SSOP demo-board incorporates the low profile 455kHz Murata ceramic filter. It has an input and output impedance of 1.0kΩ. This presents a mismatch to our chips, but we have found that the overall performance is similar to that when we use the "blue" Murata filters that have the proper 1.5kΩ input and output impedance.

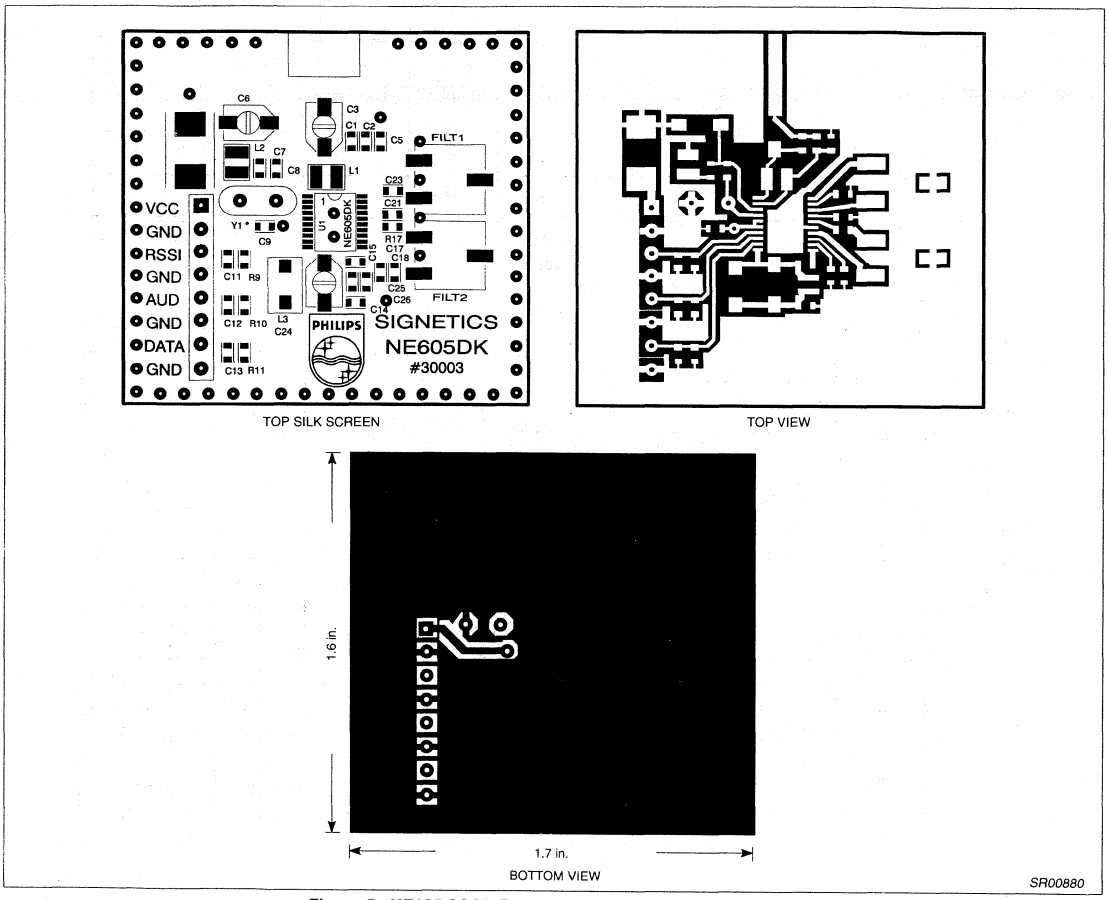


Figure 5. NE605 SSOP Demo-board Layout (Not Actual Size)

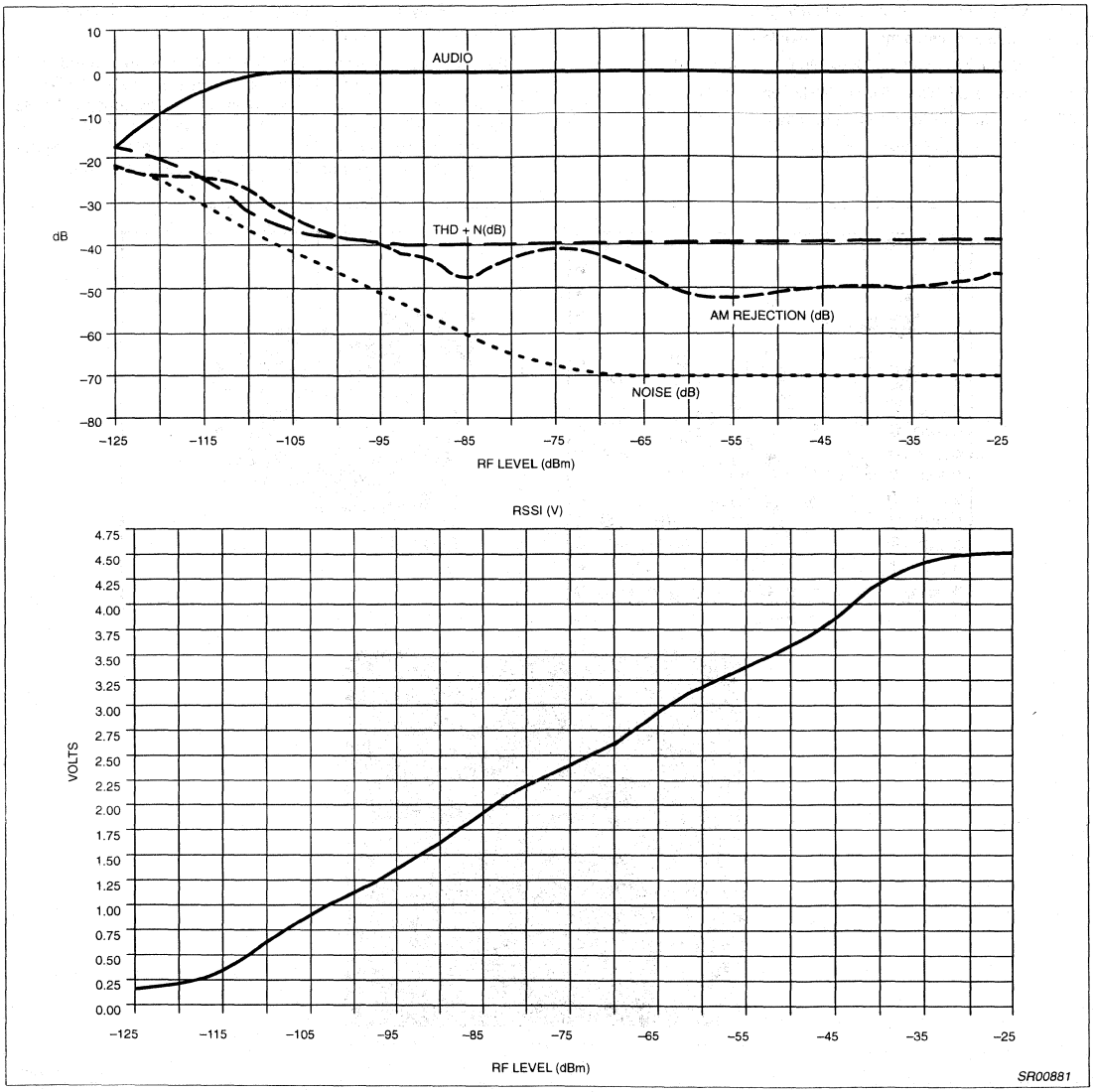


Figure 6. NE605 SSOP Performance Graphs

HOW TO TUNE THE NE605 DEMO-BOARD

Figure 7 shows a trouble-shooting chart for the NE605. It can be used as a general guide to tune the DIP, SO, and SSOP demo-boards. Below are some of the highlights from the trouble shooting chart that are explained in more detail.

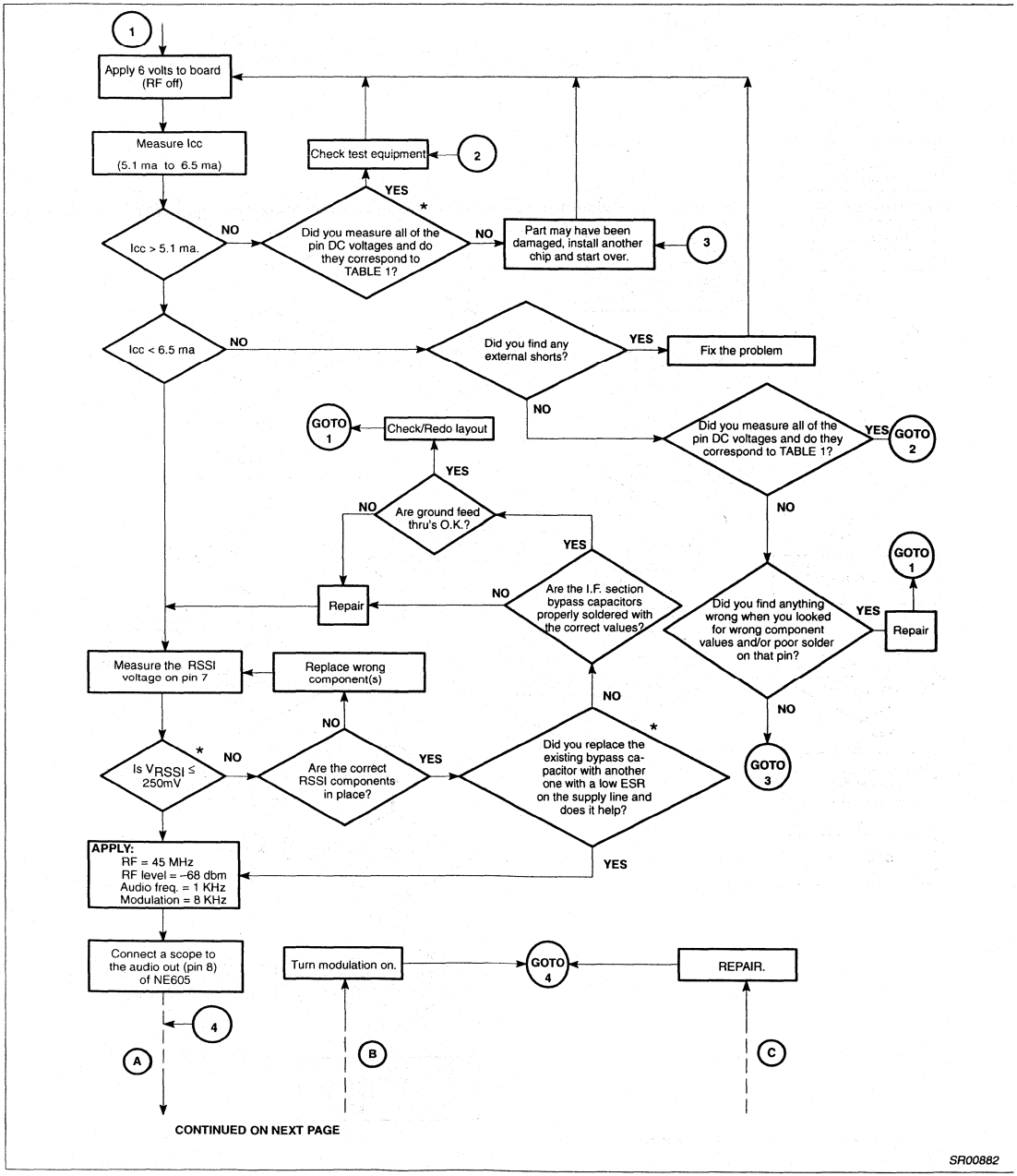
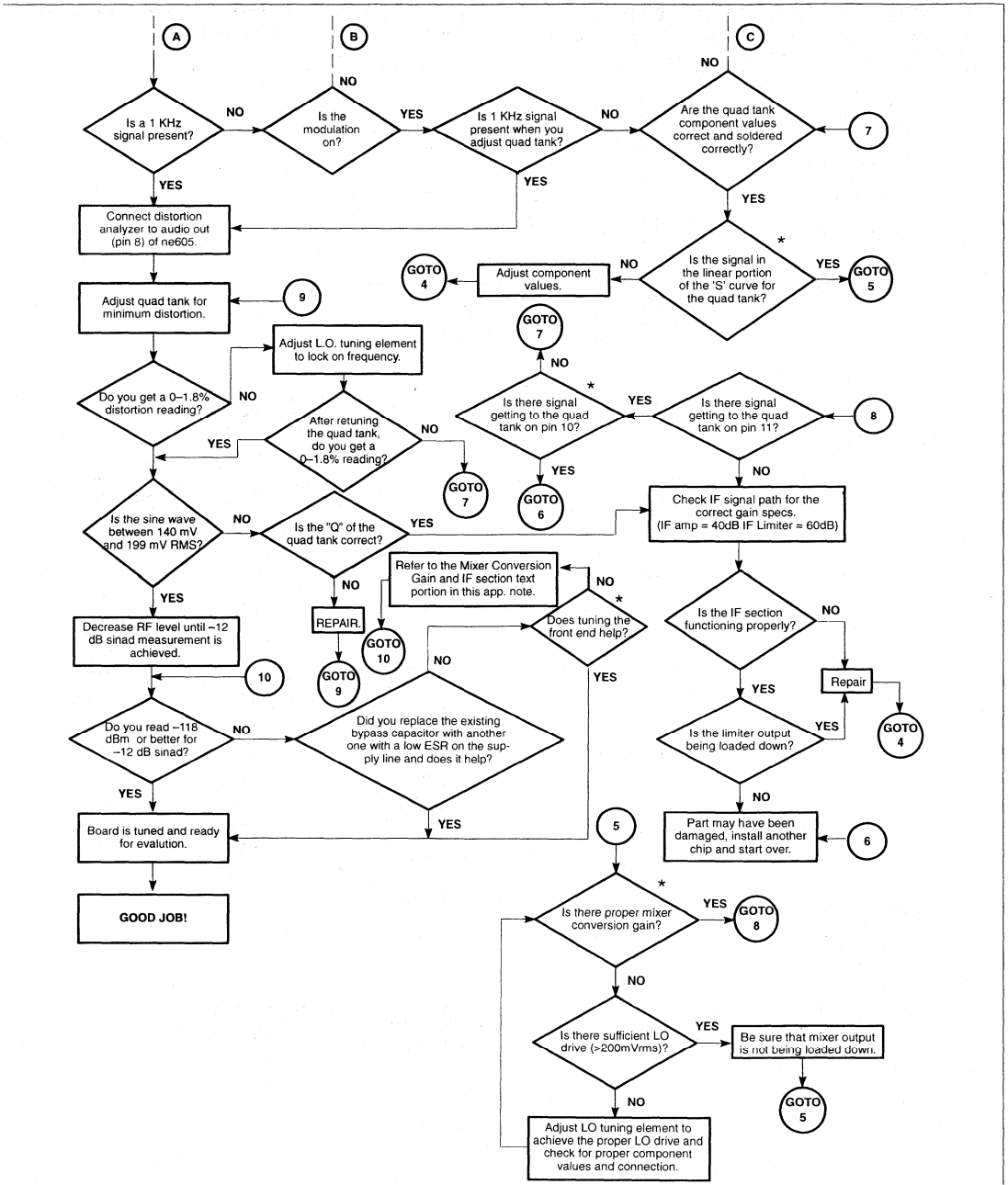


Figure 7. Trouble-shooting Chart for the NE605 Demo-board



*NOTE: Refer to the appropriate text section of the app. note for further details.

SR00883

How to tell when a part is damaged

Since most SO and SSOP sockets hinder the maximum performance of the NE605, it is advisable to solder the packages directly to the board. By this approach, one will be able to evaluate the part correctly. However, it can be a tedious chore to switch to another part using the same layout. Therefore, to be absolutely certain that the chip is damaged, one can measure the DC voltages on the NE605. Table 11 shows the DC voltages that each pin should roughly have to be a good part.

Table 11. Approximate DC Voltages for the NE605

Pin Number	DC Voltage (V)
1	1.37
2	1.37
3	5.16
4	5.94
5	N/A
6	6.00 (V_{CC})
7	N/A
8	2.00
9	2.00
10	3.49
11	1.59
12	1.59
13	1.59
14	1.65
15	0.00 (GND)
16	1.60
17	1.60
18	1.60
19	1.60
20	4.87

Note: The DC voltage on Pin 5 is not specified because it can either be V_{CC} or ground depending if the audio is muted or not (Connecting ground on Pin 5 mutes the audio on Pin 8, while V_{CC} on Pin 5 unmutes the audio).

The DC voltage on Pin 7 is not specified because its DC voltage depends on the strength of the RF signal getting to the input of the NE605. It also can be used as a stability indicator.

If any of the DC voltages are way off in value, and you have followed the trouble-shooting chart, the part needs to be changed.

RSSI Indicator

The next important highlight is using the RSSI pin as a stability indicator. With power connected to the part and no RF signal applied to the input, the DC voltage should read 250mV or less on Pin 7. Any reading higher than 250mV, indicates a regeneration problem. To correct for the regeneration problem, one should check for poor layout, poor bypassing, and/or poor solder joints. Bypassing the NE605 supply line with a low equivalent series resistance (ESR) capacitor to reduce the RSSI reading can improve the 12dB SINAD measurement by 8dB, as found in the lab. If the regeneration problem still exists, read AN1994.

Quad tank and S-Curve

As briefly mentioned in the chart, it is important to measure the Q of the quad tank if a distortion reading of 1.8% or less cannot be measured. Recall that if the Q of the quad tank is too high for the deviation, then premature distortion will occur. However, if the Q is too low for the deviation, the audio level will be too low. The audio level coming out of the audio pin should be 140mV$_{RMS}$ to 190mV$_{RMS}$.

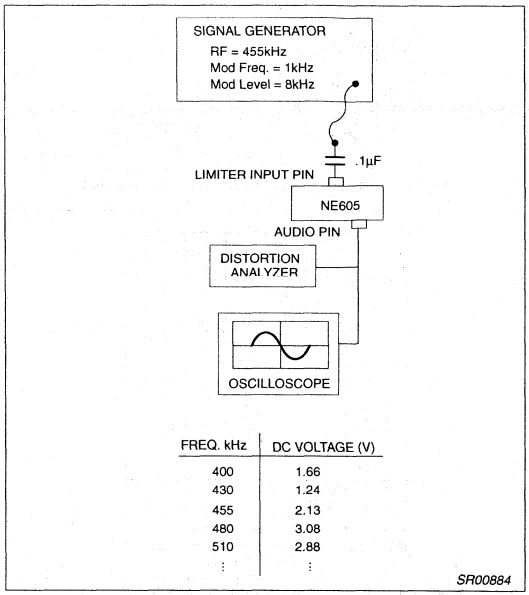


Figure 8. Test Set-up to Measure S-Curve of the Quad Tank

If the distortion reading is too high and/or the audio level is too low, then it is important to measure and plot the S-curve of the quad tank. The test set-up used in the lab can be seen in Figure 8.

The following steps were taken to measure the S-curve for the SO and SSOP demo-boards.

Step 1. Remove the second IF ceramic filter from the demo-board.

Step 2. Connect a signal generator to the limiters input through a DC blocking capacitor.

Step 3. Connect a DC voltmeter and an oscilloscope to the audio output pin.

Step 4. Set the signal generator to a 455kHz signal and be sure that the modulation is on (RF=455kHz Mod Freq = 1kHz Mod Level=8kHz). Apply this 455Khz signal to the limiter input such that there is a sinewave on the oscilloscope screen. Adjust the quad tank for maximum sinewave amplitude on the oscilloscope or for lowest distortion. Additionally, adjust the supply input signal to the NE605 such that the 1kHz sinewave reaches its maximum amplitude.

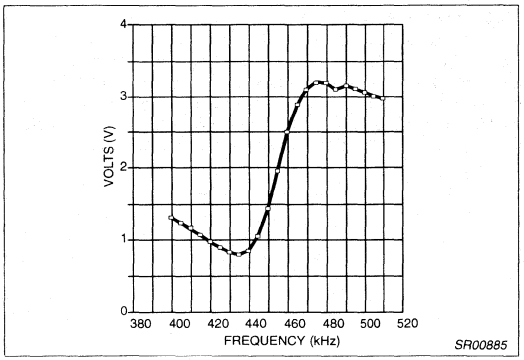


Figure 9. S-Curve for NE605 SO Demo-board

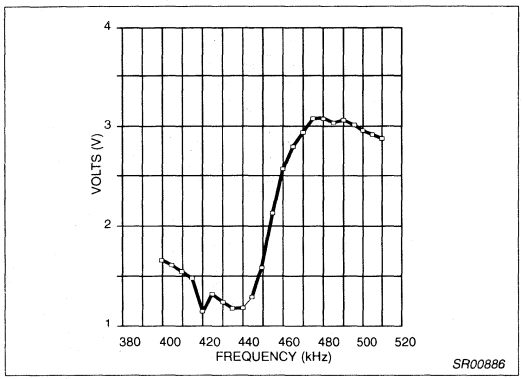


Figure 10. S-Curve for NE605 SSOP Demo-board

Step 5. Turn off the modulation and start taking data. Measure the Frequency vs DC voltage. Vary the frequency incrementally and measure the DC voltage coming out of the audio pin. Remember that once the modulation is turned off, the sine-wave will disappear from the oscilloscope screen.

Step 6. Plot the S-curve.

Figures 9 and 10 show the S-curve measurements for the SO and SSOP demo-boards. Notice that the center of the S-curve is at 455kHz. The overall linearity determines how much deviation is allowed before premature distortion. Since our application requires ±8kHz of deviation, our S-curve is good because it exceeds the linear range of 447kHz to 463kHz.

If the Q of the quad tank needs to be lowered, a designer should put a resistor in parallel with the inductor. The lower the resistor value, the more the Q will be lowered. If the Q needs to be increased, choose a higher Q component. More information on the Quad tank can be found in the NE604A data sheet.

If the linear section of the S-curve is not centered at 455kHz, the quad tank component values need to be recalculated. The way to determine the component values is by using $F = \frac{1}{2\pi\sqrt{LC}}$ where F should be the IF frequency. In the case of the demo-boards, the IF = 455kHz.

Front End Tuning

The best way to tell if the front end of the NE605 is properly matched is to use a network analyzer in a S11 setting. The lower the dip, the greater the absorption of the wanted frequency. Figures 11 and 12 show the S11 dip for the front end matching of the SO and SSOP demo-boards, respectively.

We have found in the lab that a -8dB to -10dB dip is usually sufficient to get the maximum signal transfer such that a good 12dB SINAD reading is met. The front end circuit uses a tapped-C impedance transformation circuit which matches the 50Ω source with the input impedance of the mixer.

In the process of matching the front end, we have found that the ratio of the two capacitors play an important role in transferring the signal from the source to the mixer input. There should be approximately a 4:1 or 5:1 ratio.

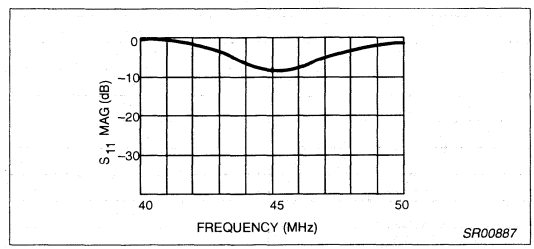


Figure 11. S11 Front-End Response for SO Demo-board

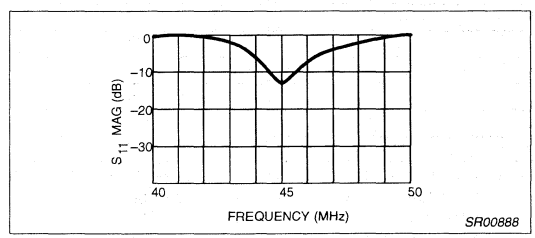


Figure 12. S11 Front-End Response for SSOP Demo-board

Checking the Conversion Gain of the Mixer

Once the front end has been properly matched, a designer should check the conversion gain if there are problems with the SINAD measurement. Be sure to turn off the modulation when making this measurement.

The method of measuring conversion gain on the bench is fairly simple. For our demo-boards, measure the strength of the 455kHz signal on the matching output network of the mixer with a FET probe. Then measure the 45MHz RF input signal on the matching input network of the mixer. Subtract the two numbers and the measured conversion gain should be around 13dB. Make sure that the input and output matching networks for the mixer have the same impedance since we are measuring voltage gain to get power gain ($P = V^2/R$). Of course this conversion gain value will change if there is a different RF input. In AN1994, Figure 16 shows how the conversion gain varies with different RF input frequencies.

Checking the gains in the IF Section

If the IF section does not give 100dB of gain, then the -118dBm SINAD measurement cannot be achieved. In fact some symptoms of low or no audio level can be due to the IF section.

One way of checking the function of the IF section is to check the gain of the IF amplifier and the IF limiter. The IF amplifier gain should be around 40dB and the IF limiter gain should be around 60dB.

To check this, connect a FET probe to the output of the amplifier. Apply a strong input signal with no modulation and then slowly lower the input signal and wait for the output of the amplifier to decrease. Measure the strength of the output signal in dB and then subtract from it the strength of the input signal in dB. This resulting number indicates the maximum gain of that section. (This method assumes matched input and output impedance.)

If a designer finds one of the sections with lower gain, then one area to check are the IF bypass capacitors. Be sure that the IF bypass capacitors have a good solid connection to the pad. It was also found in the lab that the RSSI stability reading improves when the IF bypass is properly installed.

QUESTION & ANSWER SECTION

Q: When I measure the bandpass response of the IF filters on the SSOP demo-board, it appears to have a little hump compared to the SO demo-board which has a flat filter response. Why is there a difference in the bandpass response when the SO and SSOP 605 chips are similar?

A: The answer has to do with the ceramic filters and not the package of the NE605. The reason why the SO demo-board has a flat bandpass response is because it is matched properly with the filter. The SSOP demo board uses the new Murata low profile ceramic 455kHz filter. Unfortunately, the input and output impedance is now 1kΩ instead of 1.5kΩ. This presents an impedance mismatch which creates the hump to occur in the bandpass response. But one does not have to worry too much about this response because the situation does not affect the overall performance that much. Additionally, the 12 SINAD measurement is similar whether using the "blue" (1.5kΩ) or "white" (1.0kΩ) Murata filters.

If you are worried about this, then switch to the correct "blue" Murata filters. The SSOP package will work with those filters as well. But if your design has strict height requirements, the white filters are a good solution.

Q: How much LO signal do you see at the RF port?

A: The worst LO leakage seen at the RF input on the SO and SSOP demo-board is -40dBm/441mV. This seems to vary with the LO level into the base of the on board transistor. This measurement will also vary with different LO frequencies. The NE605 SO and SSOP demo-boards have a LO frequency of 44.545MHz. Since there are so many variables, a designer needs to measure his/her own board for an accurate LO-RF isolation measurement.

There are several ways to improve the LO leakage from getting to the antenna. One can choose a higher IF frequency and tighten up the bandwidth of the front-end filter. Another solution is to add a low noise amplifier between the antenna and the mixer, and/or design a double conversion receiver and make sure the 1st mixer has a LO-RF isolation which meets the system specifications.

Q: On the SO and SSOP demo-board, the LO oscillator circuit is tunable with a variable capacitor. Is this a requirement?

A: No. The variable capacitor is used to tune the LO freq., but one can use a fixed value. The advantage of going with a fixed value capacitor is that it is a cheaper component part and there is no need for tuning. The only advantage with a tunable LO is that a designer can optimize the performance of the receiver.

Q: I know that the IF bandwidth of the NE605 allows me to build an IF of 21.4MHZ. Will the NE605 SSOP package perform just as good at 21.4MHz IF as it does at 455kHz?

A: Although we have not worked with NE605 SSOP at 21.4MHZ, we believe that it would be difficult to get a 12dB SINAD measurement at -120dBm. The wavelengths are much smaller at 21.4MHz than 455kHz. Since the wavelengths are smaller, there is a higher probability of regeneration occurring in the IF section. Therefore, a designer will probably have to reduce the gain in the IF section. Additionally, the SSOP package has pins that are physically closer together than with the normal type of packaged parts which can contribute to the unstable state with higher IF frequencies.

Demodulating at 10.7MHz IF with the NE/SA605/625 AN1996

Author: Alvin K. Wong

INTRODUCTION

The need for high speed communications is increasing in the market place. To meet these needs, high performance receivers must demodulate at higher IF frequencies to accommodate for the wider deviations in FM systems.

The standard 455kHz IF frequency, which is easier to work with, and thus more forgiving in production, no longer satisfies the high speed communication market. The next higher standard IF frequency is 10.7MHz. This frequency offers more potential bandwidth than 455kHz, allowing for faster communications.

Since the wavelength at 10.7MHz is much smaller than 455kHz, the demand for a good RF layout and good RF techniques increases. These demands aid in preventing regeneration from occuring in the IF section of the receiver. This application note will discuss some of the RF techniques used to obtain a stable receiver and reveal the excellent performance achieved in the lab.

BACKGROUND

If a designer is working with the NE/SA605 for the first time, it is highly recommended that he/she reads AN1994 and AN1995. These two application notes discuss the NE/SA605 in great detail and provide a good starting point in designing with the chip.

Before starting a design, it is also important to choose the correct part. Philips Semiconductors offers an extensive receiver line to meet the growing demands of the wireless market. Table 1 (see end of app note) displays the different types of receivers and their key features. With the aid of this chart, a designer will get a good idea for choosing a chip that best fits their design needs.

If low voltage receiver parts are required in a design, a designer can choose between a NE/SA606, SA607, SA608, or SA626. All of these low voltage receivers are designed to operate at 3V while still providing high performance to meet the specifications for cellular radio. All of these parts can operate with an IF frequency as high as 2MHz. However, the SA626 can operate with a standard IF frequency of 10.7MHz and also provide fast RSSI speed. Additionally the SA626 has a power down mode to conserve battery power.

A close look at Table 1 will also show that there are subtle differences between the 3V receivers. The main differences between the NE/SA606, SA607, and SA608 can be seen in the audio and RSSI output structure. Additionally the SA607 and SA608 provide a frequency check pin which can aid in locking in the desired received frequency over temperature.

OBJECTIVE

The objective of this application note is to show that the NE/SA605 can perform well at an IF frequency of 10.7MHz. Since most Philips Semiconductors receiver demo-boards are characterized at RF = 45MHz/IF = 455kHz, we decided to continue to characterize at this frequency. This way we could compare how much degradation (for different IFs) there was with a RF = 45MHz/IF = 455kHz vs RF = 45MHz/ IF = 10.7MHz. As we will discuss later, there was minimal degradation in performance.

We also tested at RF = 240MHz/IF = 10.7MHz. The 240MHz RF is sometimes referred to as the first IF for double conversion receivers. Testing the board at RF=83.16MHz (which is also a common first IF for analog cellular radio) and IF = 10.7MHz was not done because the conversion gain and noise figure does not change that much compared to 45MHz input. Therefore, we can probably expect the same type of performance at 83.16MHz.

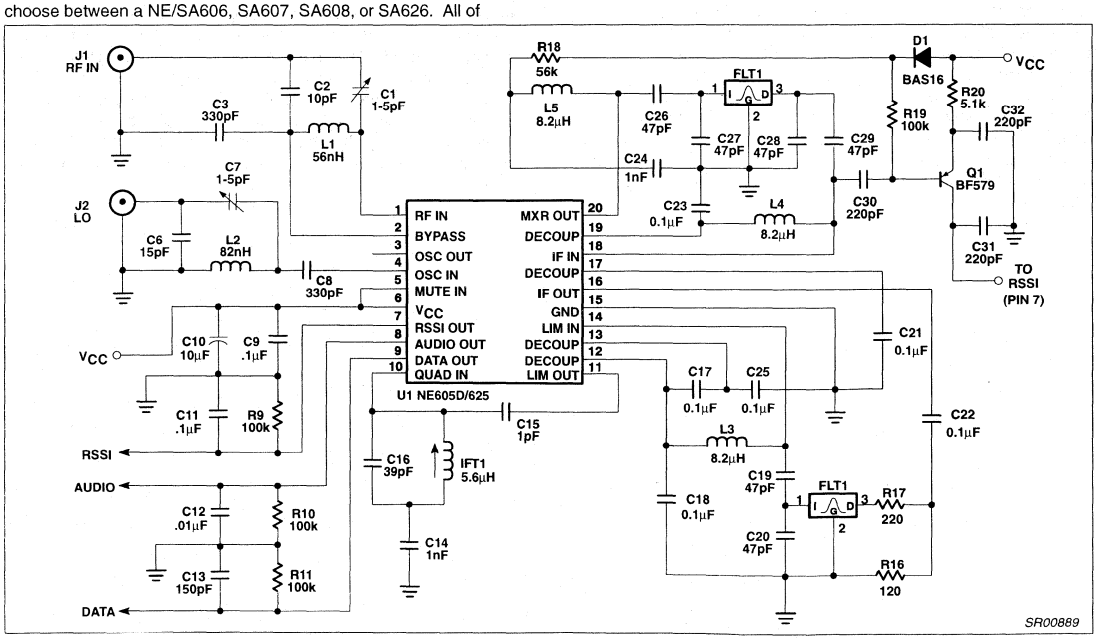


Figure 1. NE/SA605/625 Schematic: RF = 240MHz, LO = 229.3MHz, IF = 10.7MHz

Demodulating at 10.7MHz IF with the NE/SA605/625 AN1996

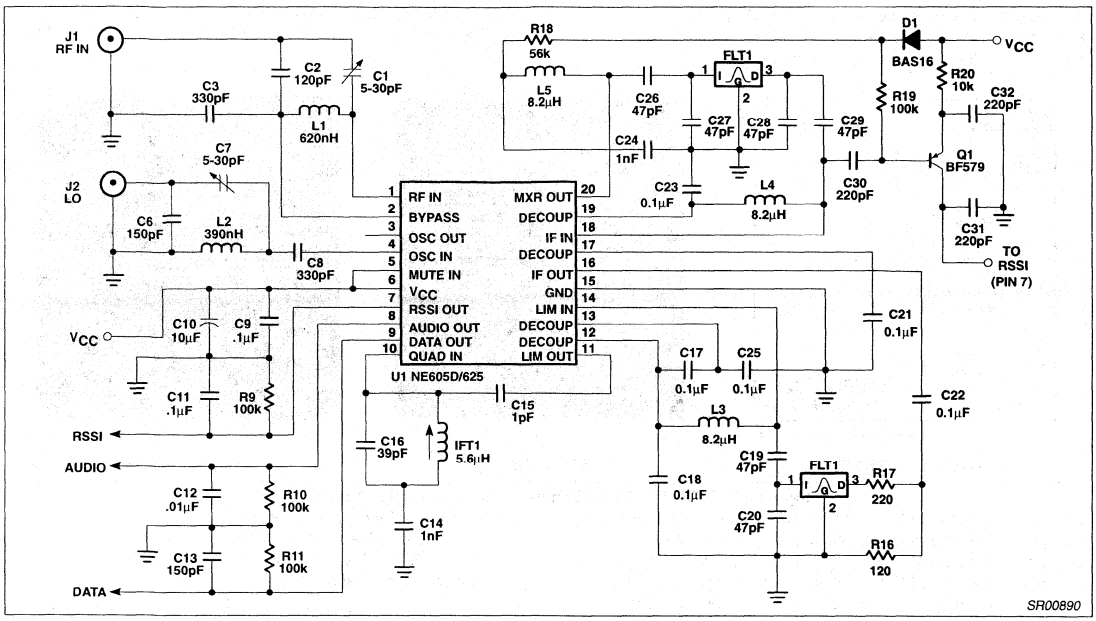


Figure 2. NE/SA605/625 Schematic: RF = 45MHz, LO = 55.7MHz, IF = 10.7MHz

The RF = 240MHz/IF = 10.7MHz demo-board is expected to perform less than the RF = 45MHz/IF = 10.7MHz demo-board because the mixer conversion gain decreases while the noise figure increases. These two parameters will decrease the performance of the receiver as the RF frequency increases.

With the new demands for fast RSSI time, Philips Semiconductors has also designed receiver chips with fast RSSI speed: The NE/SA624, NE/SA625 and SA626. The NE/SA625 can also be used in this layout because it is pin-for-pin compatible with the NE/SA605. The RSSI circuitry was the only change done for the NE/SA625, so performance will be similar to the NE/SA605. Performance graphs shown in this application note will reveal the similarities.

For systems requiring low voltage operation, IF=10.7MHz and fast RSSI speed, the SA626 will be the correct choice, however, this application note does not address the performance of the SA626 because the SA626 was not available at this writing.

Board Set-Up and Performance Graphs

Figures 1 and 2 show the NE/SA605/625 schematics for the 240MHz and 45MHz boards, respectively. Listed below are the basic functions of each external components for both Figures 1 and 2.

SO Layout Schematic List

U1- NE/SA605 or NE/SA625
FLT1-10.7MHz ceramic filter Murata SFE10.7MA5-A (280kHz BW)
FLT2-10.7MHz ceramic filter Murata SFE10.7MA5-A (280kHz BW)

Note: If a designer wants to use different IF bandwidth filters than the ones used in this application note, the quad tank's S-curve may need to be adjusted to accommodate the new bandwidth.

C1- Part of the tapped-C network to match the front-end mixer
C2- Part of the tapped-C network to match the front-end mixer
C3- Used as an AC short to Pin 2 and to provide a DC block for L1 which prevents the upsetting of the DC biasing on Pin 1
C6- part of the tapped-C network to match the LO input
C7- part of the tapped-C network to match the LO input
C8- DC blocking capacitor
C9- Supply Bypassing
C10- Supply bypassing (this value can be reduced if the NE/SA605/625 is used with a battery)
C11- used as a filter, cap value can be adjusted when higher RSSI speed is preferred over lower RSSI ripple
C12- used as a filter
C13- used as a filter
C14- used to AC ground the quad tank
C15- used to provide the 90° phase shift to the phase detector
C16- quad tank component to resonant at 10.7MHz with IFT1 and C15
C17- IF limiter decoupling capacitor
C18- DC block for L3 which prevents the upsetting of the DC biasing on Pin 14
C19- part of the tapped-C network for FLT2
C20- part of the tapped-C network for FLT2
C21- IF amp decoupling cap
C22- DC blocking cap
C23- IF amp decoupling cap and DC block for L3 which prevents the upsetting of the DC biasing on Pin 14
C24- provides DC block for L5 which prevents the upsetting of the DC biasing on Pin 20
C25- IF limiter decoupling capacitor
C26- part of the tapped-C network for FLT1
C27- part of the tapped-C network for FLT1
C28- part of the tapped-C network for FLT1
C29- part of the tapped-C network for FLT1

R9- used to convert the current into the RSSI voltage
R10-converts the audio current to a voltage
R11-converts the data current to a voltage
R16-used to kill some of the IF signal for stability purposes
R17-used in conjunction with R16 for a matching network for FLT2

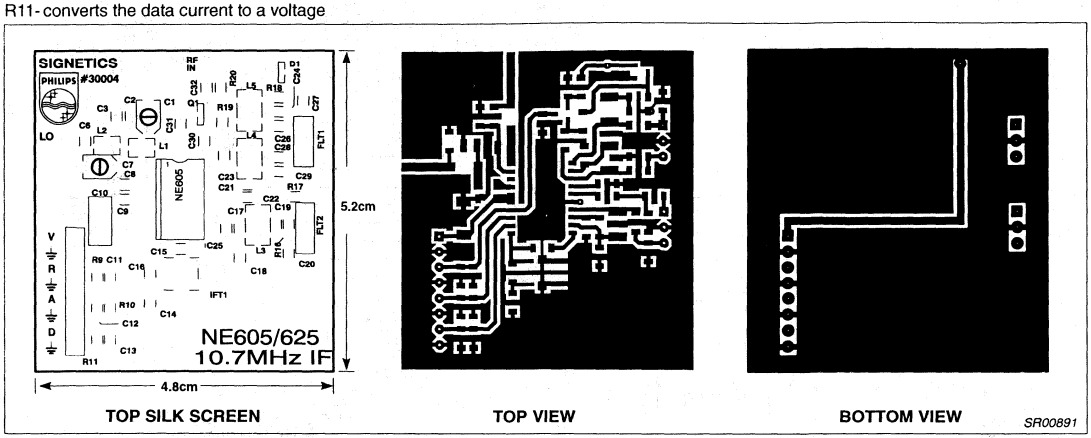


Figure 3. NE/SA605/625 SO Demo-Board Layouts (Not Actual Size)

L1 - part of the tapped-C network to match the front-end mixer
L2 - part of the tapped-C network to match the front-end mixer
L3- part of the tapped-C network to match the input of FLT2
L4- part of the tapped-C network to match the input of FLT1
L5- part of the tapped-C network to match the input of FLT1

RSSI Extender Circuit

R18-provides bias regulation, the gain will stay constant over varying V_{CC}
R19-for biasing, buffer RF DC voltage
R20-provides the DC bias, RSSI gain (when R20 increases, RSSI gain decreases
C30-DC blocking capacitor which connects the ceramic filter's output to the PNP transistor's input
C31-decoupling capacitor, and should be removed for measuring RSSI systems speed
C32-peak detector charge capacitor
D1- diode to stabilize the bias current
Q1- Philips BF579 PNP transistor
IFT1-part of the quad tank circuit

There are minor differences between Figures 1 and 2. The RF and LO tapped-C component values are changed to accommodate for the different RF and LO test frequencies (RF=240MHz and 45MHz and LO = 229.3MHz and 55.7MHz). The other difference is the value of R20. This resistor value was changed to optimize the RSSI curve's linearity (see RSSI extender section in this application note for further details).

The recommended NE/SA605/625 layout is shown in Figure 3. This layout can be integrated with other systems.

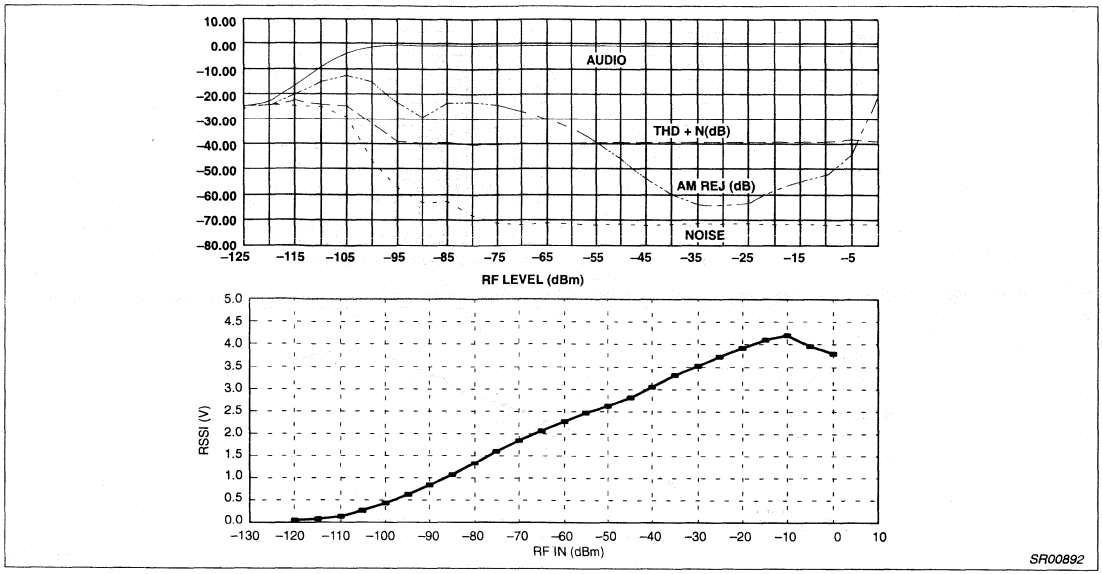


Figure 4. NE/SA625 SO Performance Graphs at 240MHz

Figures 4 through 7 show the performance graphs for the NE/SA605 & NE/SA625 at 240MHz and 45MHz RF inputs. There was no real noticeable difference in performance between a NE/SA605 or NE/SA625 except for AM rejection. The NE/SA605 appears to have a little better AM rejection, but from the end user's point of view, there is no difference between the receiver. All the other measurements were perfect, including SINAD.

RF Input

The NE/SA605/625 board is set up to receive an RF input of 240MHz (see Figure 1). This is achieved by implementing a tapped-C network. The deviation should be set to ±70kHz to achieve ***-110dBm to -112dBm for -12dB SINAD***. However, the deviation can be increased to ±100kHz, depending on the bandwidth of the IF filter and the Q of the quad tank.

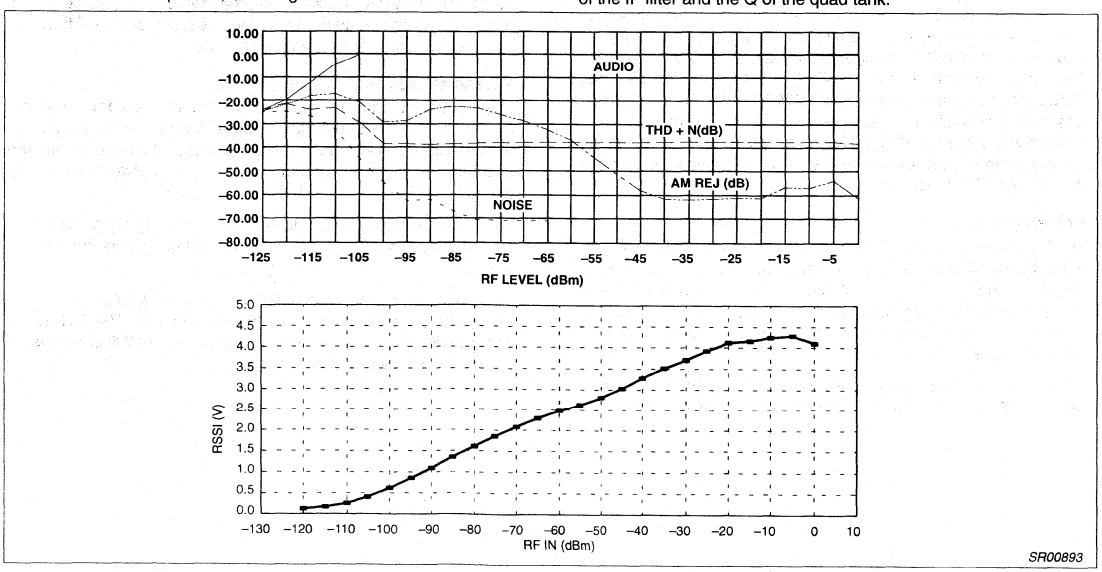


Figure 5. NE/SA625 SO Performance Graphs at 45MHz

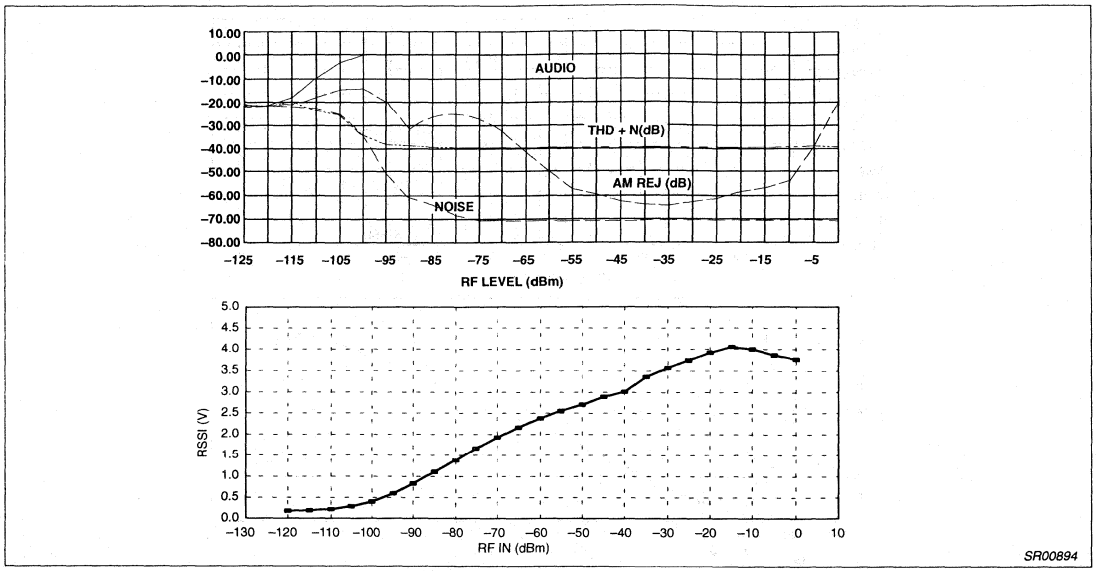


Figure 6. NE/SA605SO Performance Graphs at 240MHz

Because we wanted to test the board at 45MHz, we changed the values of the tapped-C network for the RF and LO ports (see Figure 2). We found that a ***-116dBm to -118dBm for -12dB SINAD*** could be achieved. With these results, we were pretty

close to achieving performance similar to our standard 455kHz IF board.

A designer can also make similar RF and LO component changes if he/she needs to evaluate the board at a different RF frequency. *It should be noted that if a designer purchases a stuffed NE/SA605/625 demo-board from Philips Semiconductors its set up will be for an RF input frequency of 240MHz.* AN1994 will aid the designer in calculating the tapped-C values for other desired frequencies, while AN1995 will be of value for making S11 bench measurements. Just remember that the input impedance will differ for different RF frequencies.

LO Input

The LO frequency should be 229.3MHz for the RF = 240MHz demo-board and have a drive level of -10dBm to 0dBm (this also applies for the RF = 45MHz and LO = 55.7MHz). The drive level is important to achieve maximum conversion gain. The LO input also has a matched tapped-C network for efficiency purposes which makes for good RF practices.

If a designer wanted to change the matching network to inject a different LO frequency, he/she could follow the steps in AN1994 and assume that the input impedance is around 10kΩ for low frequency inputs. The main goal is to get maximum voltage transfer from the signal generator to the inductor.

An external oscillator circuit was used to provide greater flexibility in choosing different RF and LO frequencies; however, an on-board oscillator can be used with the NE/SA605/625. New high frequency fundamental crystals, now entering the market, can also be used for high LO frequency requirements. Most receiver systems, however, will use a synthesizer to drive the LO port.

10.7MHz Ceramic Filters

The input and output impedance of the 10.7MHz ceramic IF filters are 330Ω. The NE/SA605/625's input and output impedances are roughly 1.5KΩ. Therefore, a matching circuit had to be implemented to obtain maximum voltage transfer. Tapped-C networks were used to match the filters input and output impedance.

But in this case, we decided to go with non-tuning elements to reduce set-up time. Figure 8 shows the values chosen for the network.

Although our total deviation is 140kHz, we used 280kHz IF bandwidth filters to maximize for fast RSSI speed. The SINAD performance difference between using 180kHz BW filter versus 280kHz BS filter was insignificant.

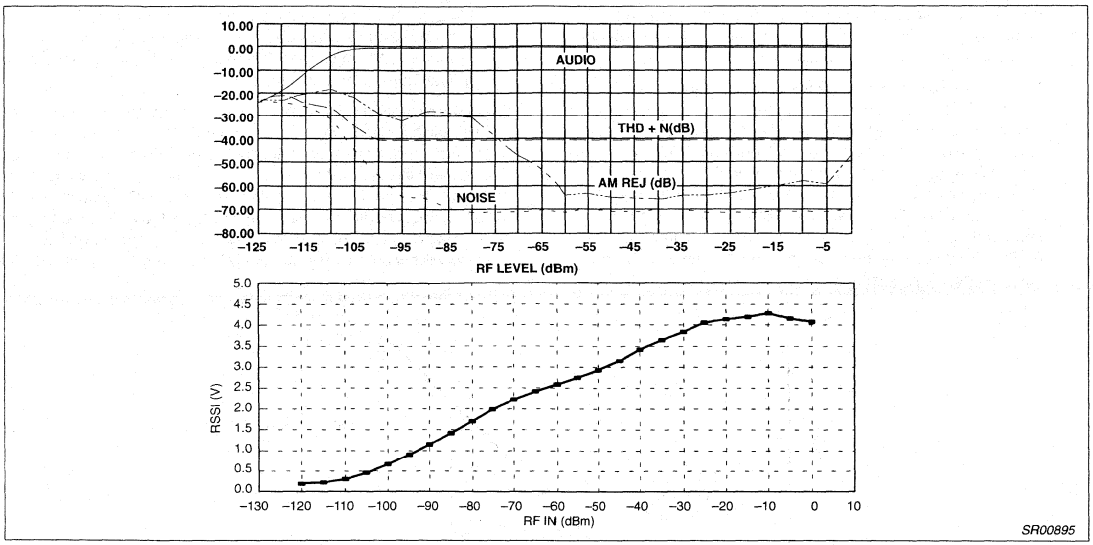


Figure 7. NE/SA605 SO Performance Graphs at 45MHz

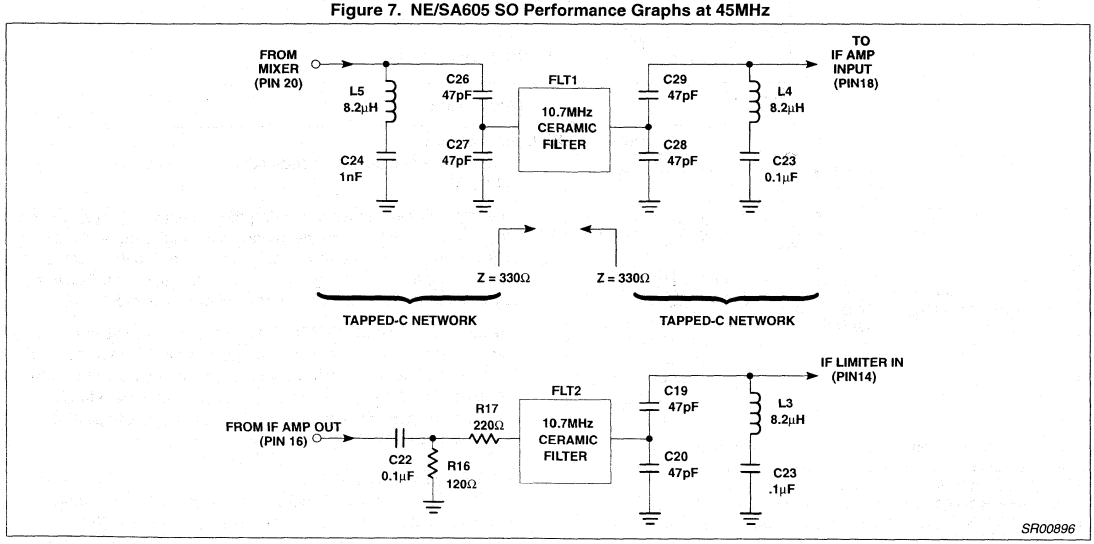


Figure 8. Matching Configuration for FLT1 and FLT2

Stabilizing the IF Section From Regeneration

Because the gain in the IF section is 100dB and the wavelength for 10.7MHz is small, the hardest design phase of this project was to stabilize the IF section.

The steps below show the methods used to obtain a stable layout.

1. The total IF section (IF amp and limiter) gain is 100dB which makes it difficult to stabilize the chip at 10.7MHz. Therefore, a 120Ω (R16 of Figure 1) resistor was used to kill some of the IF gain to obtain a stable system. (NOTE: Expect AM rejection performance to degrade as you decrease the IF gain externally.)
2. Since the tapped-C inductors for FLT1 and FLT2 are not shielded, it is important not to place them too close to one another. Magnetic coupling will occur and may increase the probability of regeneration.
3. It was also found that if the IF limiter bypass capacitors do not have the same physical ground, the stability worsens. Referring to Figure 1, the IF limiter bypass capacitors (C17, C25) are connected to assure a common ground.
4. The positioning of ground feedthroughs are vital. A designer should put feedthroughs near the IF bypass capacitors ground

points. In addition, feedthroughs are needed underneath the chip. Other strategic locations are important for feedthroughs where insufficient grounding occurs.

5. Shielding should be used after the best possible stability is achieved. The NE/SA605/625 demo-board is stable, so shielding was not used. However, if put into a bigger system, shielding should be used to keep out unwanted RF frequencies. As a special note, if a good shield is used, it can increase the R16 resistor value such that there is less IF gain to kill to achieve stability. This means the RSSI dynamic range is improved. So if a designer does not want to implement the RSSI extender circuit, but is still concerned with SINAD and RSSI range, he/she can experiment with R16 and shielding because there is a correlation between them (see RSSI extender section in this application note for more information). In addition, AM rejection performance will improve due to the greater availability of the total IF gain.

The key to stabilizing the IF section is to kill the gain. This was done with a resistor (R16 in Figure 8) to ground. All the other methods mentioned above are secondary compared to this step. Lowering the value of this resistor reduces the gain and the increasing resistor value kills less gain. For our particular layout, 120Ω was chosen to obtain a stable board, but we were careful not to kill too much gain. One of the downfalls of killing too much gain is that the SINAD reading will become worse and the RSSI dynamic range is reduced.

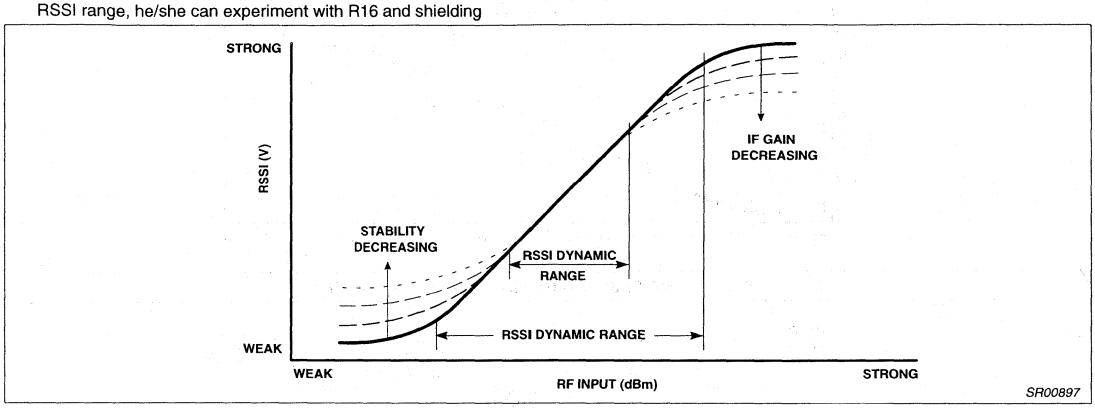


Figure 9. RSSI Dynamic Range

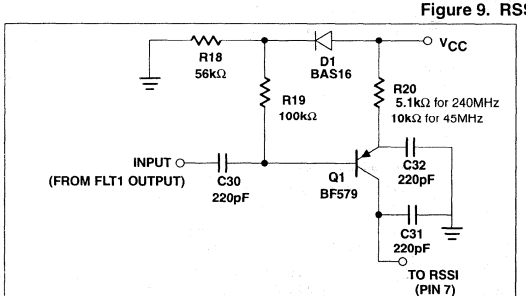


Figure 10. External RSSI Extender Circuit

RSSI Dynamic Range

There are two main factors which determine the RSSI dynamic range. These two factors are 1.) how stable is the board, and 2.) how much gain is killed externally. If the board is unstable, a high RSSI voltage reading will occur at the bottom end of the curve. If too much gain is taken away, the upper half of the curve is flattened. Thus the dynamic range can be affected. Figure 9 shows how the linear range can be decreased under the conditions mentioned above.

It is important to choose the appropriate resistor to kill enough gain to get stability but not too much gain to affect the upper RSSI curve dynamic range. Because we had to kill some IF gain to achieve good board stability and good SINAD readings, our RSSI overall dynamic range was reduced on the upper end of the curve.

Because SINAD and the RSSI dynamic range are two important parameters for most of our customers, we decided to add an "RSSI extender" modification to the board to get the best of both worlds. Together with the RSSI external modification and the "stability resistor", we can now achieve excellent SINAD readings and maintain a wide RSSI dynamic range.

RSSI Extender Circuit

The RSSI extender circuit increases the upper dynamic range roughly about 20-30dB for the 240MHz demo-board. The NE/SA605/625 demo-board has 90-100dB of linear dynamic range when the RSSI modification is used.

Referring to Figure 10, one can see that one transistor is used with a few external components. The IF input signal to the PNP transistor is tapped after the ceramic filter to ensure a clean IF signal. The circuit then senses the strength of the signal and converts it to current, which is then summed together with the RSSI output of the chip.

The PNP transistor stage has to be biased as a class B amplifier. The circuit provides two functions. It is a DC amplifier and an RF detector. The gain of the RSSI extender can be controlled by R20 and R9 (Gain = R9/R20). Adjusting R20 is preferable because it

controls the upper half of the RSSI curve, whereas adjusting R9 shifts the whole RSSI curve.

If a different RF frequency is supplied to the mixer input, it is important to set the external RSSI gain accordingly. When the RF input was changed from 240MHz to 45MHz, the conversion gain of the mixer increased. Therefore, the earlier gain settings for the RSSI extender was too much. A lower gain setting had to be implemented such that a smoother transition would occur.

Quad Tank

The quad tank is tuned for 10.7MHz ($F=1/2\pi\sqrt{LC}$). Figure 1 shows the values used (C14,C15, C16, IFT1) and Figure 11 shows the S-curve. The linear portion of the S-curve is roughly 200kHz. Therefore, it is a good circuit for a total deviation of 140kHz. It is possible to deviate at 200kHz, but this does not leave much room for part tolerances.

If more deviation is needed, a designer can lower the S-curve with a parallel resistor connected to the quadrature tank. A designer should play with different value resistors and plot the S-curve to pick the best value for the design. To key in on the resistor value with minimum effort, a designer can put a potentiometer in parallel with the quad tank and tune it for best distortion. Then the designer can use fixed value resistors that are close to the potentiometer's value.

Fixed quad tank component values can be used to eliminate tuning, but a designer must allow for part tolerances and temperature considerations. For better performance over temperature, a resonator/discriminator can be used. Thus, no tuning is required for the quad tank section, which will save on production costs.

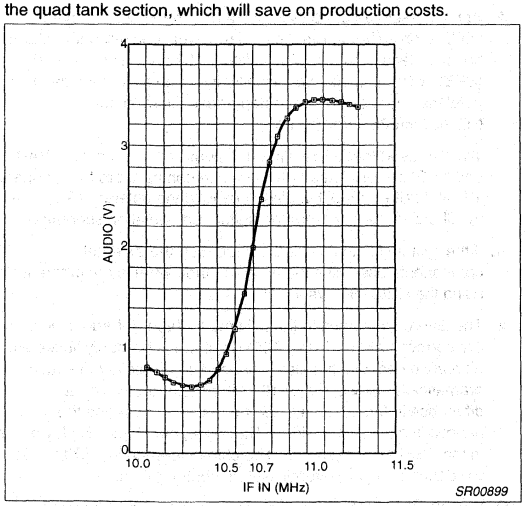


Figure 11. 10.7MHz Quad Tank S-Curve

RSSI System Speed

The RSSI rise and fall times are important in applications that use pulsed RF in their design. The way we define the speed is how fast the RSSI voltage can travel up and down the RSSI curve. Figure 12 shows a representation of this. Five different pulsed RF levels were tested to get a good representation of the RSSI speed. One can predict that the stronger the pulsed signal, the higher the RSSI voltage and the longer it will take for the fall time to occur. Generally speaking, the rise time is determined by how long it takes to charge up an internal capacitor. The fall time depends on how long it takes to discharge this capacitor.

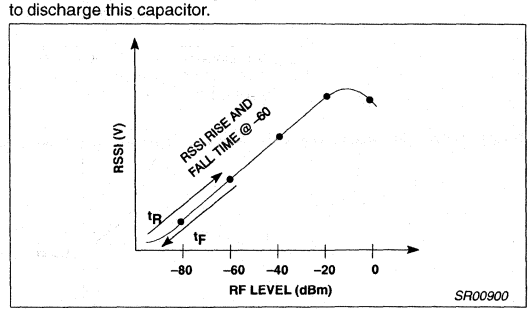


Figure 12. RSSI Cuve with Pulsed RF Levels

It is also important to understand that there are two types of RSSI speeds. The first type is the RSSI *chip* speed and the second is the RSSI *system* speed. The RSSI *chip* speed will be faster than the *system* speed. The bandwidth of the external filters and other external parts can slow down the RSSI system speed dramatically.

Figure 13 shows the bench set up for the RSSI system speed measurements. The pulsed RF was set for 10kHz and and the RSSI output was monitored with a digital oscilloscope. Figure 14 shows how the rise and fall times were measured on the oscilloscope.

The modifications done on the NE/SA625 board are shown in Figure 15. The RSSI caps C11 and C31 were eliminated, and the RSSI resistor values were changed. We wanted to see how much time was saved by using a smaller RSSI resistor value.

The RSSI system speed for the 240MHz NE/SA625 demo board is shown in Figure 16. Again, the only modification was that the RSSI caps (C11 and C31) were taken out and the RSSI resistor value (R9) was varied. For different RF levels, the speed seems to vary slightly, but this is expected. The higher the RSSI voltage, the longer it will take to come back down the RSSI curve for the fall time.

Looking more closely at Figure 16, one can note that the 0dBm input level has a faster fall time than the -20dBm level. This occurs because of the limited dynamic range of the test equipment. The equipment does not have sufficient on/off range, so at 0dBm the 'off' mode is actually still on. Therefore, you don't get a true reading.

At 0dBm the RSSI voltage is lower than –20dBm. The reason why this happens is because the RSSI linearity range stops at -10dBm. When the RF input drive is too high (e.g., 0dBm), the mixer conversion gain decreases, which causes the RSSI voltage to drop.

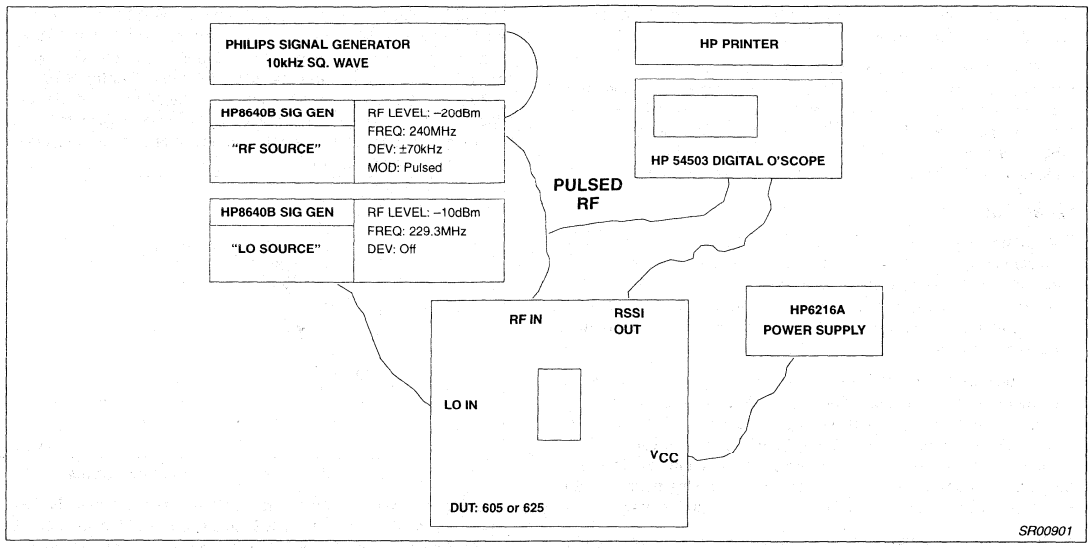


Figure 13. RSSI Speed Set-Up

QUESTION AND ANSWER SECTION

Q. What should the audio level at Pin 8 be?

A. The audio level is at 580mV$_{P-P}$ looking directly at the audio output pin and does not include a C-message filter. However, the audio output level will depend on two factors: the "Q" of the quadrature tank and the deviation used. The higher the quad tanks "Q", the larger the audio level. Additionally, the more deviation applied, the larger the audio output. But the audio output will be limited to a certain point.

Q. Am I required to use the 10µF supply capacitor?

A. No, a smaller value can be used. The 10µF capacitor is a suggested value for evaluation purposes. Most of the time a power supply is used to evaluate our demo boards. If the supply is noisy, it will degrade the receiver performance. We have found that a lower value capacitor can be used when the receiver is powered by a battery. But it is probably safer to stay at a reasonable capacitor size.

Q. Can I use different IF filters for my required bandwidth specifications?

A. Yes, you can order different IF filters with different bandwidths. Some of the standard manufacturers have 180kHz, 230kHz, and 280kHz bandwidths for 10.7MHz ceramic filters. Just be sure that the quad tank "S-curve" is linear for your required bandwidth. The NE/SA605/625 demo-board has a 200kHz linearity for the quad tank. So ±70kHz deviation is perfect.

We have also found that even though the IF filter's bandwidth might be more than our requirements, it does not really degrade overall receiver performance. But to follow good engineering practices, a designer should order filters that are closest to their requirements. Going with wider bandwidth filters will give you better RSSI system speed.

Q. I want to use part of your demo board for my digital receiver project. Can you recommend a good 10.7MHz filter with accurate 10.7MHz center frequency which can provide minimum phase delay?

A. At the present time, I only know of one manufacturer that is working on a filter to meet digital receiver requirements. Murata has a surface mount 10.7MHz filter. The number is FX-6502 (SFECA 10.7). It was specifically designed for Japanese digital cordless phones. You can adapt these filters to our NE/SA605/625 demo board.

We also used these filters in our layout and got similar SINAD and RSSI system speed performance compared to the standard 10.7MHz filters (280kHz BW). I believe the difference between the filters will be apparent for digital demodulation schemes.

Q. If the system RSSI time is dependent on the external components used, like the IF filters, then what is the difference in using the NE/SA605 vs the NE/SA625?

A. The difference comes in the fall time for high IF frequencies. You are correct that for IFs like 455kHz, there is probably little delta difference because the filter's bandwidth prohibits the speed dramatically. However, for 10.7MHz IFs, there will be a difference in the fall time between the chips because the bandwidths are much wider. Therefore, the chips will play a role in the RSSI system speed. The chip difference in RSSI speed will depend on your overall system configuration.

Q. Why does the AM rejection performance look better on the NE/SA605, 455kHz IF board than the NE/SA605/625 10.7MHz IF demo-board?

A. For the 455kHz IF demo-board there is more IF gain available compared to the 10.7MHz IF board. Recall that for the 10.7MHz IF board, some of the IF gain was killed externally for stability reasons. Since the IF gain helps improve AM rejection performance, by killing IF gain, AM rejection is decreased.

Demodulating at 10.7MHz IF with the NE/SA605/625 AN1996

Q. The NE/SA605/625 10.7MHz IF demo-board is made for the SO package. Can I use your SSOP package and expect the same level of performance?

A. We have not done a SSOP layout yet. But if the same techniques are used, I am sure the SSOP package will work. The SA626 demo-board will be done in SSOP, and probably be available in the future.

Q. I tried to duplicate your RSSI system reading measurements using your demo-board and I get slower times. What am I doing wrong?

A. The RSSI system speed measurements are very tricky. Make sure your cable lengths are not too long. I have found that when making microsecond measurements, lab set-up is of utmost importance. Also, make sure the RSSI caps (C11 and C31) are removed from the circuit.

Also be sure that the bandwidth of your IF filters is not slowing down the RSSI system speed (Cf: section on RSSI system speed).

Q. I am going to use your design in my NTT cordless digital phone. Can you recommend a 240.05MHz filter?

A. Murata SX-4896 (SAMAFC 240.05) is a filter you can use for your application.

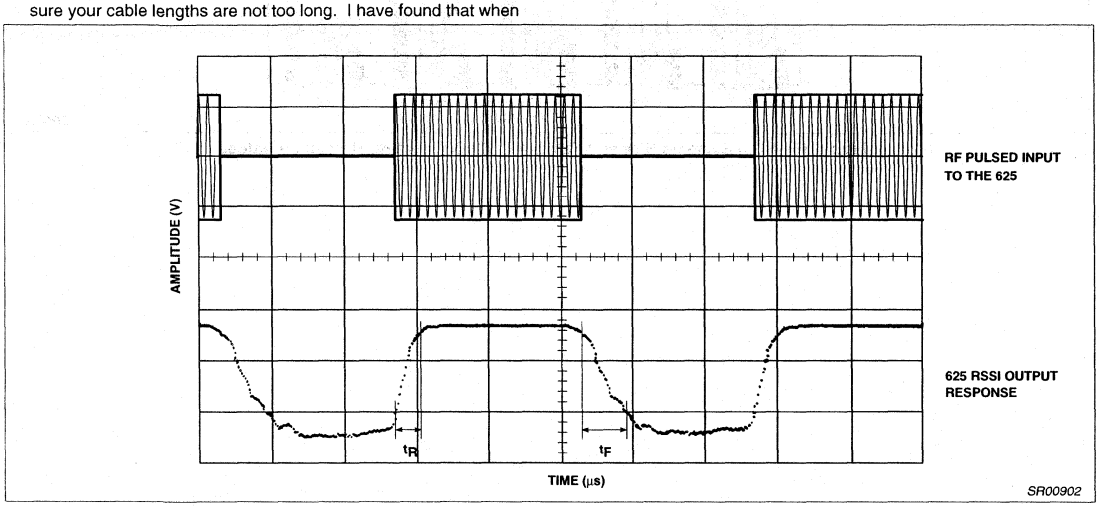


Figure 14. Oscilloscope Display of RSSI System Rise and Fall Time

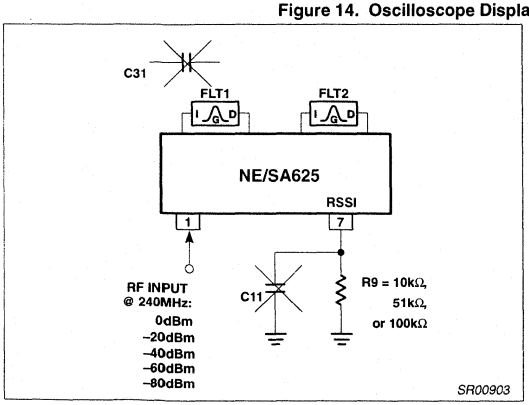


Figure 15. NE/SA625 RSSI Test Circuit Configuration

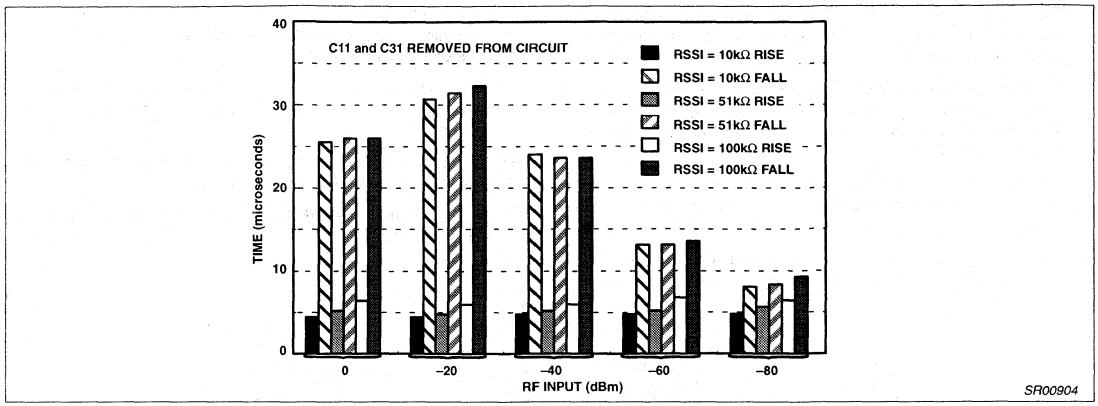


Figure 16. RSSI Systems Rise and Fall Time with Different RSSI Resistor Values

Table 1. FM/IF Family Overview

		NE602A/604A		NE605	SA606	SA607	SA608	NE624	NE625	SA626	NE627
V_{CC}		4.5–8V	4.5–8V	4.5–8V	2.7–7V	2.7–7V	2.7–7V	4.5-8.0V	4.5-8.0V	2.7–5.5V	4.5-8.0V
I_{CC}		2.4mA@6V	3.3mA @ 6V	5.7mA @ 6V	3.5mA @ 3V	3.5mA @ 3V	3.5mA @ 3V	3.4mA @ 6V	5.8mA @ 6V	6.5mA @ 3V	5.8mA @ 6V
Number of Pins		8	16	20	20	20	20	16	20	20	20
Packages NE: 0 to +70°C SA: –40 to +85°C N: Plastic DIP D: Plastic SO FE: Ceramic DIP DK: SSOP		NE602AN NE602AD NE602AFE SA602AN SA602AD SA602AFE	NE604AN NE604AD SA604AN SA604AD	NE605N NE605D NE605DK SA605N SA605D SA605DK	SA606N SA606D SA606DK	SA607N SA607D SA607DK	SA608N SA608D SA608DK	NE624N NE624D SA624N SA624D	NE625N NE625D NE625DK SA625N SA625D SA625DK	SA626D SA626DK	NE627N NE627D NE627DK SA627N SA627D SA627DK
–12dB SINAD (RF = 45MHz), IF = 455kHz) 1kHz Tone, 8kHz Dev.		–120dBm / .22uV		–120dBm / .22uV	–117dBm / .31uV	–117dBm / .31uV	–117dBm / .31uV	–120dBm / .22uV	–120dBm / .22uV	–112dBm / .54uV (RF = 240MHz) (IF = 10.7MHz) 1kHz Tone, +/–70kHz Dev.	–120dBm / .22uV
Process f_t		8GHz		8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz
For lower cost version and less performance		612A & 614A		615	616	617	—	—	—	—	—
Features		– Audio & Data pins – IF BW of 25MHz – No external matching required for standard 455kHz IF filter		– Audio & Data pins – IF BW of 25MHz – No external matching required for standard 455kHz IF filter	– Low voltage – Internal RSSI and audio op amps – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Freq check pin – Low voltage – Internal RSSI and audio op amps – Unity gain RSSI output – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Freq check pin – Low voltage – Internal RSSI and audio op amps – Unity gain audio output – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Fast RSSI Time – Pin-to-Pin compatible with 604A – No external matching required for standard 455kHz IF filter	– Fast RSSI Time – Pin-to-Pin compatible with 605 – No external matching required for standard 455kHz IF filter	– Power down mode – Low voltage – Fast RSSI Time – IF BW of 25MHz – Internal RSSI & audio op amps – No external matching required for standard 10.7MHz IF filter	– Fast RSSI Time – Freq check pin – IF BW of 25MHz – Internal RSSI & audio op amps – No external matching required for standard 455kHz IF filter
RSSI OUTPUT SECTION	**Dynamic Range**	90dB		90dB	90dB	90dB	90dB	90dB	90dB	90dB	90dB
	Accuracy	+/–1.5dB		+/–1.5dB	+/–1.5cB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB
	455kHz IF **Rise * Time**	—	1.4us	—	—	—	—	1.1us	1.2us	—	1us
	455kHz IF **Fall * Time**	—	21.3us	—	—	—	—	1.3us	2.1us	—	1.7us
	10.7MHz IF **Rise * Time**	—	1.5us	—	—	—	—	1.2us	1.2us	1.2us	0.9us
	10.7MHz IF **Fall * Time**	—	19.4us	—	—	—	—	1.6us	2us	2us	1.4us

*NOTE: No IF filters in the circuit

SR00905

Table 1. (cont.) FM/IF Family Overview

			NE602A/604A		NE605	NE606	SA607	SA608	NE624	NE625	SA626	NE627
MIXER	Max Conversion Power Gain (RF = 45MHz; IF = 455kHz)		17dB	—	13dB	17dB	17dB	17dB	—	13dB	13dB	13dB
	3rd Order Intercept Point (Input) f1 = 45MHz f2 = 45.06MHz		−13dB	—	−10dBm	−9dBm	−9dBm	−9dBm	—	−10dBm	−11dBm f1 = 240.05 f2 = 240.35	−10dBm
	Noise Figure @45MHz		5dB	—	5dB	6.2dB	6.2dB	6.2dB	—	5dB	11dB @ 240MHz	5dB
	RF Input Resistance and Capacitance @45MHz		1.5k 3pF	—	4.7k 3.5pF	8k 3pF	8k 3pF	8k 3pF	—	4.7k 3.5pF	4.7k 3.5pF @ 240MHz	4.7k 3.5pF
	Output Resistance		1.5k	—	1.5k	1.5k	1.5k	1.5k	—	1.5k	330	1.5k
IF SECTION	IF AMP	Input Impedance	—	1.6k	1.6k	1.5k	1.5k	1.5k	1.6k	1.6k	330	1.5k
		Output Impedance	—	1.0k	1.0k	330	330	330	1.0k	1.0k	330	1.0k
		Gain	—	40dB	40dB	44dB	44dB	44dB	40dB	40dB	44dB	40dB
		BW	—	41MHz	41MHz	5.5MHz	5.5MHz	5.5MHz	41MHz	41MHz	40MHz	40MHz
	IF LIMITER	Input Impedance	—	1.6k	1.6k	1.5k	1.5k	1.5k	1.6k	1.6k	330	1.5k
		Output * Impedance	—	330	330	330	330	330	330	330	330	330
		Gain	—	60dB	60dB	58dB	58dB	58dB	40dB	60dB	58dB	60dB
		BW	—	28MHz	28MHz	4.5MHz	4.5MHz	4.5MHz	28MHz	28MHz	28MHz	28MHz
	Total IF Gain		—	100dB	100dB	100dB	100dB	100dB	100dB	100dB	96dB (includes −6dB pad)	100dB
	Total IF BW		—	25MHz	25MHz	2MHz	2MHz	2MHz	25MHz	25MHz	25MHz	25MHz

NOTE: *Not designed to drive a matched load

SR00906

Low-voltage high performance mixer FM IF system SA606

DESCRIPTION

The SA606 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA606 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The SA606 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to level adjust the outputs or add filtering.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA606 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs

PIN CONFIGURATION

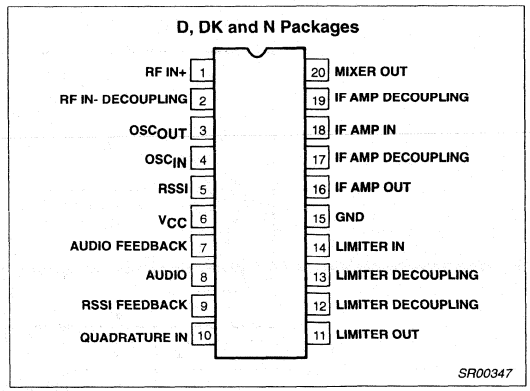


Figure 1. Pin Configuration

- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA606N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA606D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA606DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		7	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range		-40 to +85	°C
θ_{JA}	Thermal impedance	D package DK package N package	90 117 75	°C/W

BLOCK DIAGRAM

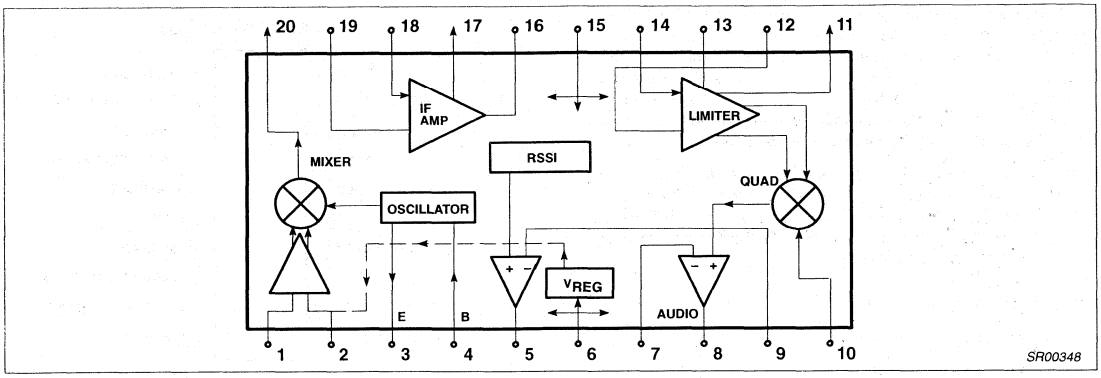


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third-order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = -52dBm		-9		dBm
	Conversion voltage gain	Matched 14.5dBV step-up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single-ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting -3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	IF level -110dBm		17		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
THD	Total harmonic distortion		-35	-50		dB
S/N	Signal-to-noise ratio	No modulation for noise		62		dB
	RF RSSI output, R_9 = 2kΩ	RF level = -118dBm		0.3	.80	V
		RF level = -68dBm	.70	1.1	1.80	V
		RF level = -23dBm	1.20	1.8	2.50	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = -27dBm		120		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = -27dBm		2.2		V
	System SINAD sensitivity	RF level = -117dBm		12		dB

CIRCUIT DESCRIPTION

The SA606 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of -9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

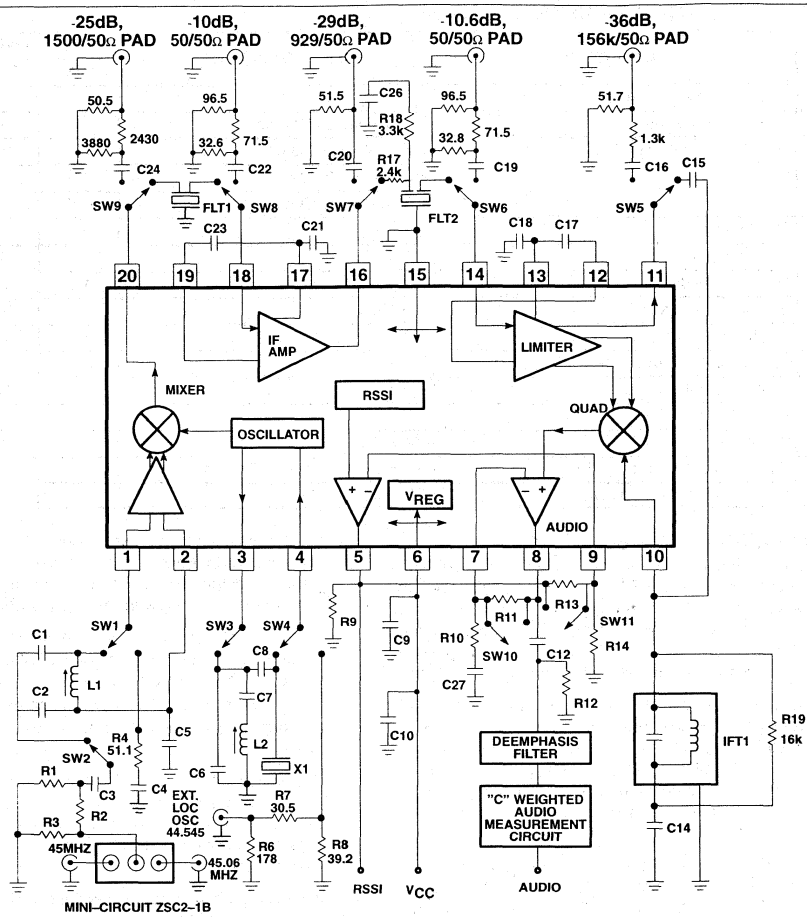
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



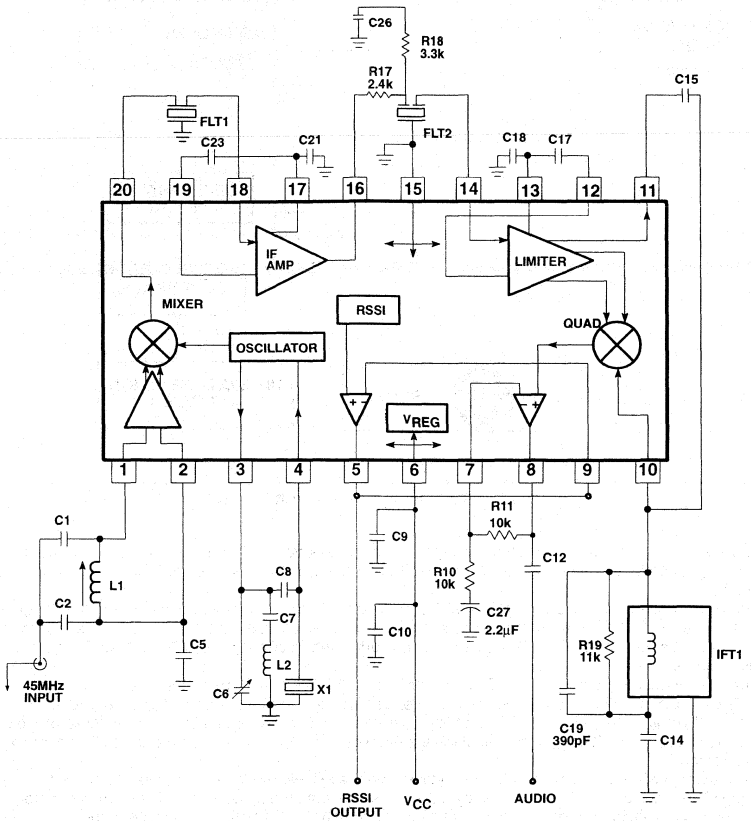
Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	2.2μF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C8	10.0pF NPO Ceramic	L2	0.8μH nominal Toko 292CNS–T1038Z
C9	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C10	10μF Tantalum (minimum) *	R9	2kΩ ±1% 1/4W Metal Film
C12	2.2μF	R10	10kΩ ±1%
C14	100nF ±10% Monolithic Ceramic	R11	10kΩ ±1%
C15	10pF NPO Ceramic	R12	2kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C23	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C25	100nF ±10% Monolithic Ceramic	R19	16kΩ
C26	100nF ±10% Monolithic Ceramic		

*NOTE: This value can be reduced when a battery is the power source.

SR00349

Figure 3. SA606 45MHz Test Circuit (Relays as shown)



NE606D/DK Demo Board
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

* NOTE: This value can be reduced when a battery is the power source.

SR00350

Figure 4. SA606 45MHz Application Circuit

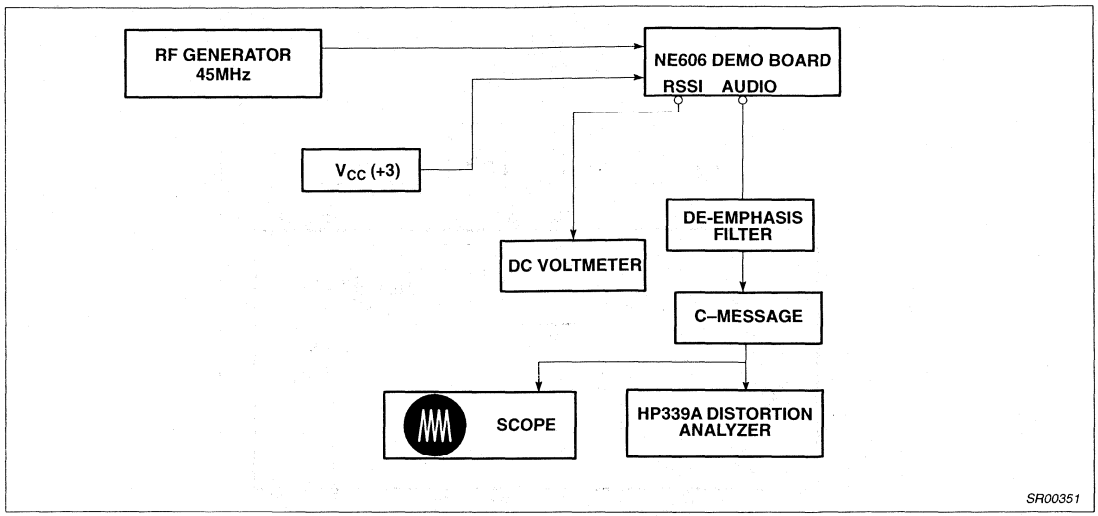


Figure 5. SA606 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or -116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 10kΩ.

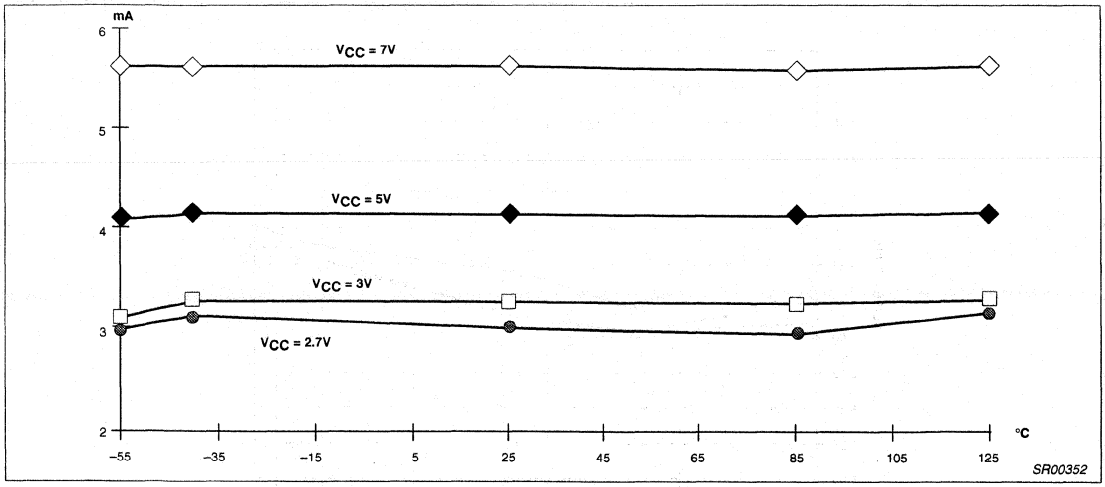


Figure 6. I_{CC} vs Temperature

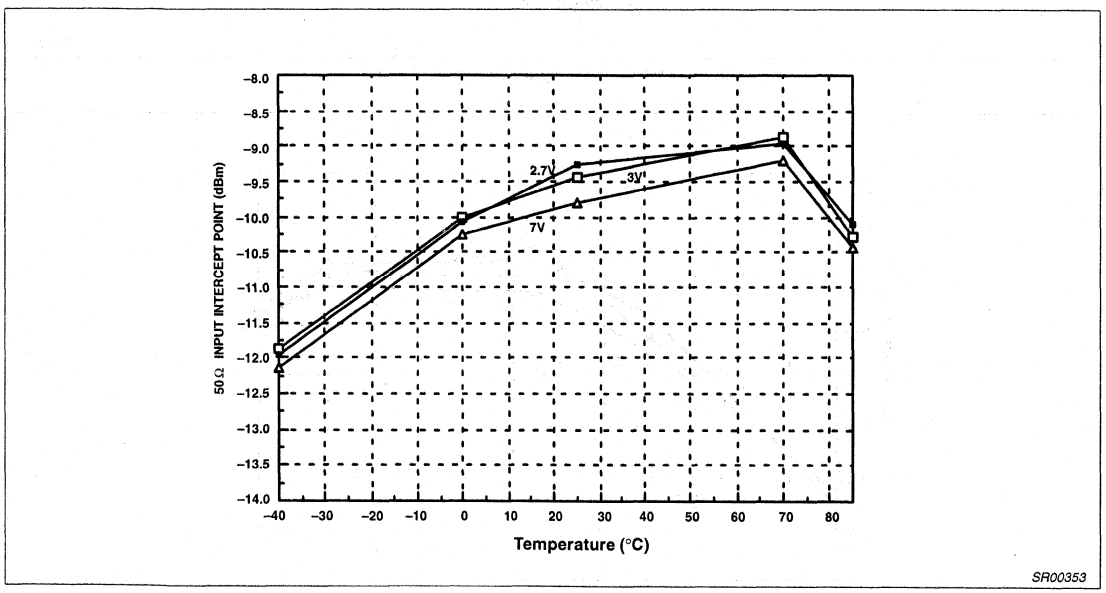


Figure 7. Third Order Intercept Point vs Supply Voltage

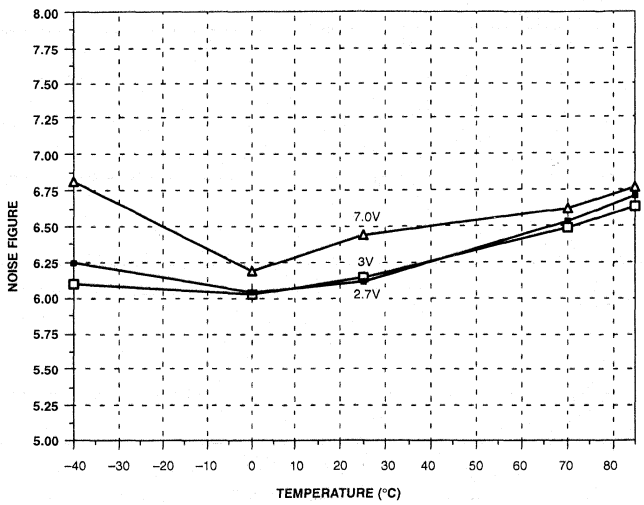


Figure 8. Mixer Noise Figure vs Supply Voltage

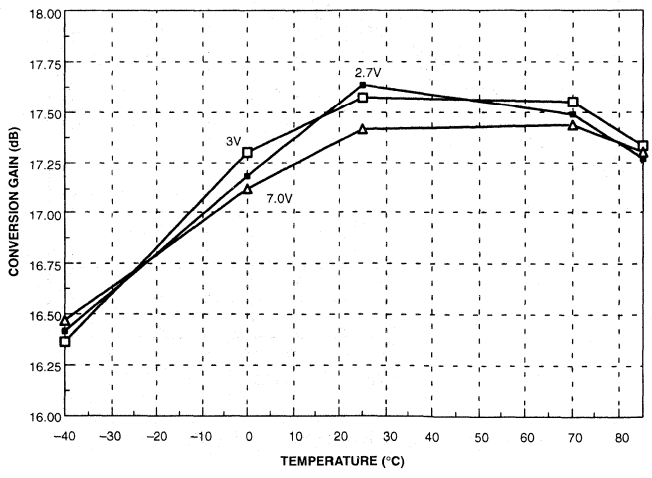


Figure 9. Conversion Gain vs Supply Voltage

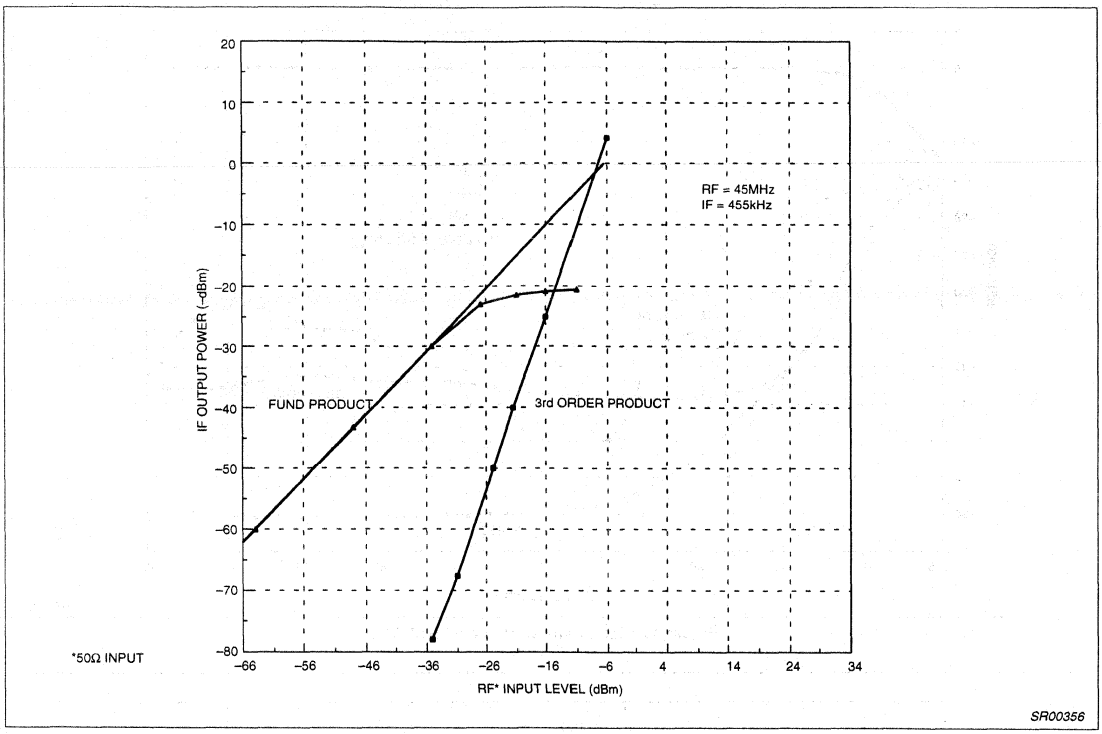


Figure 10. Mixer Third Order Intercept and Compression

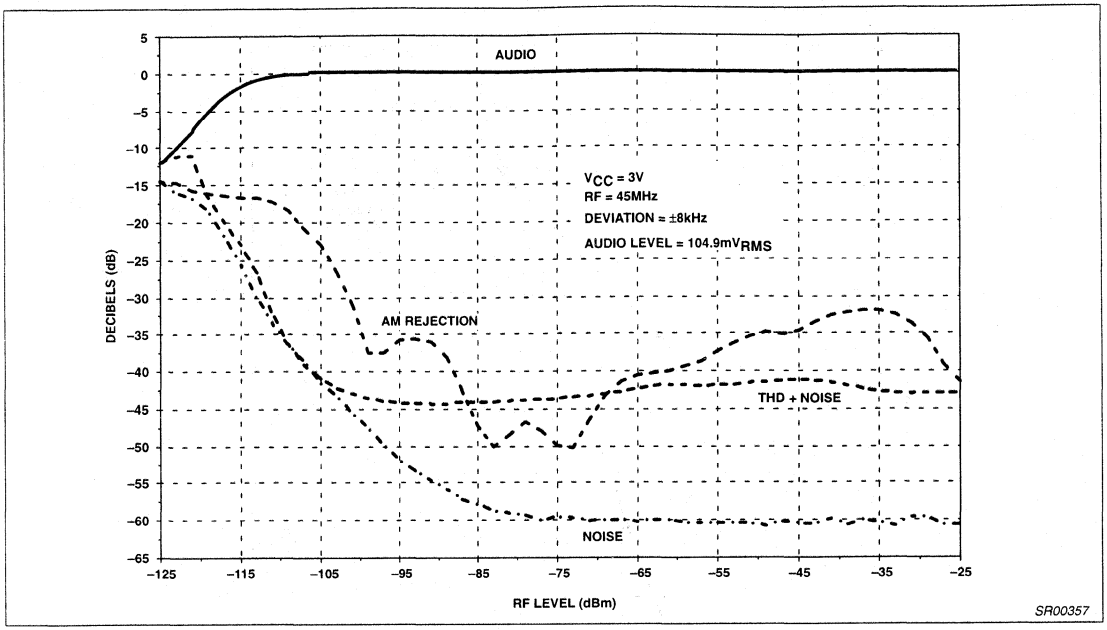


Figure 11. Sensitivity vs RF Level (-40°C)

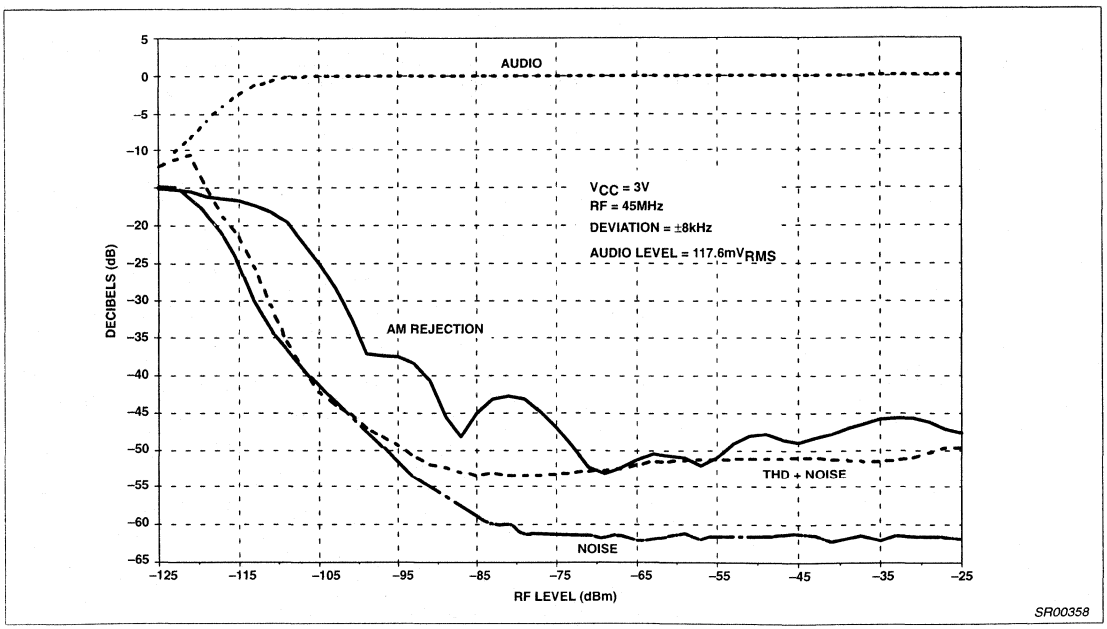


Figure 12. Sensitivity vs RF Level (+25°C)

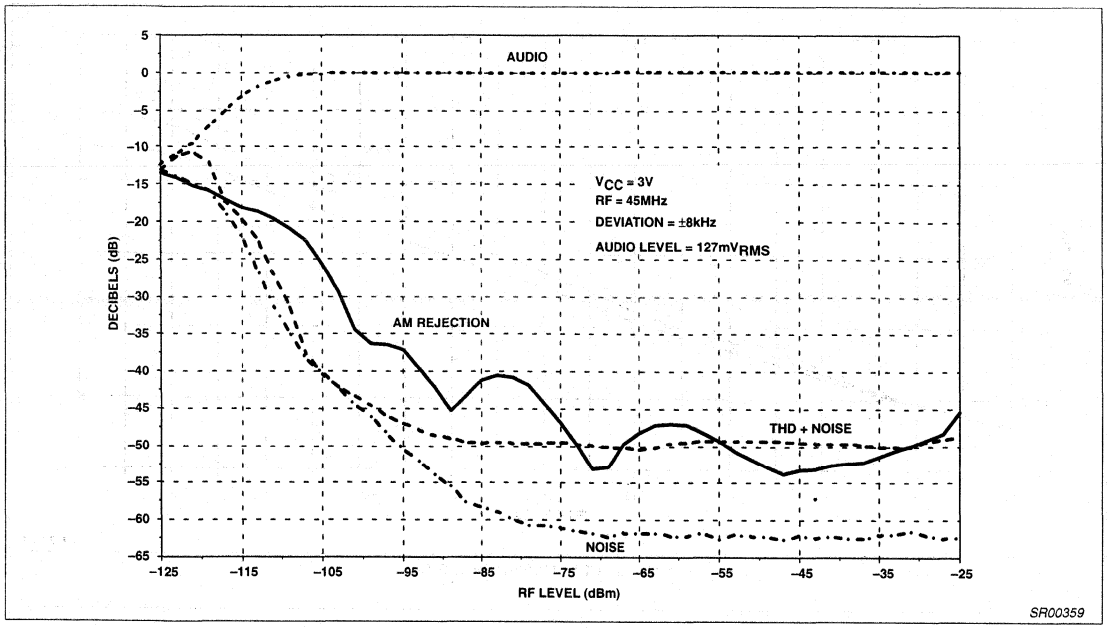


Figure 13. Sensitivity vs RF Level (Temperature 85°C)

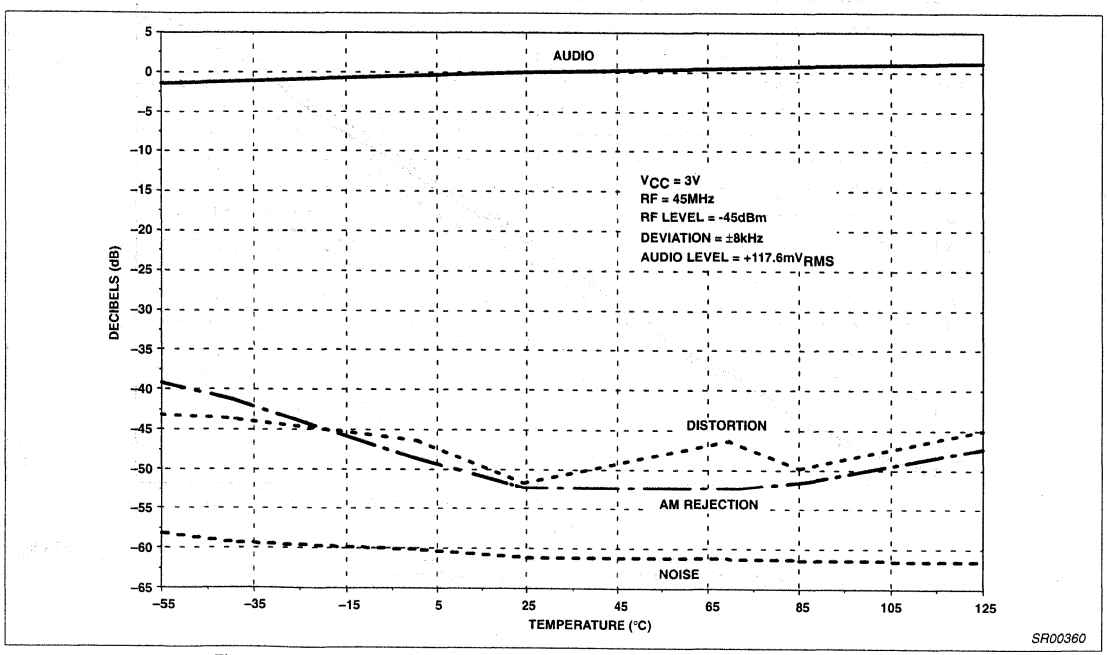


Figure 14. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

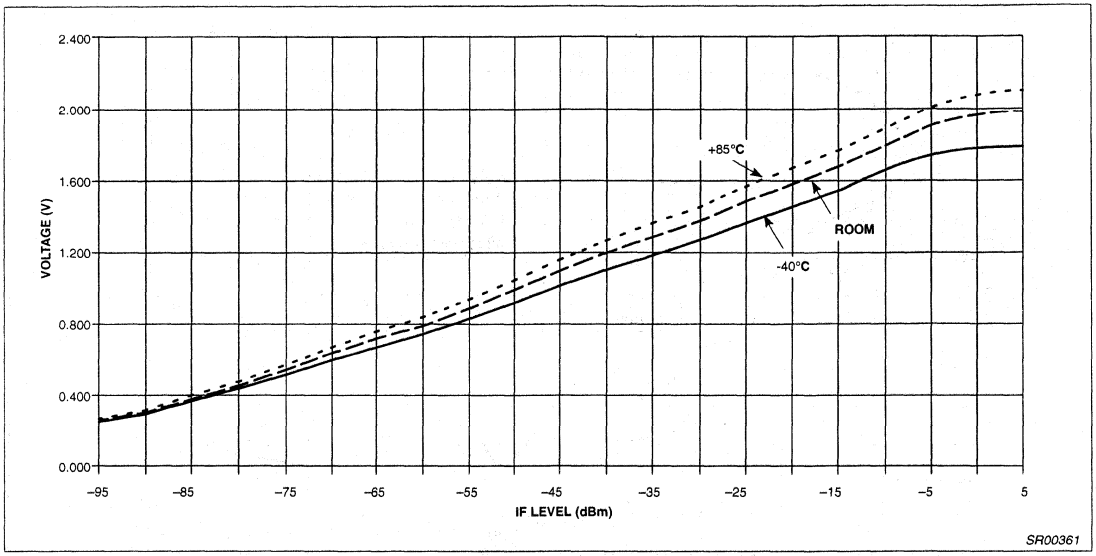


Figure 15. RSSI (455kHz IF @ 3V)

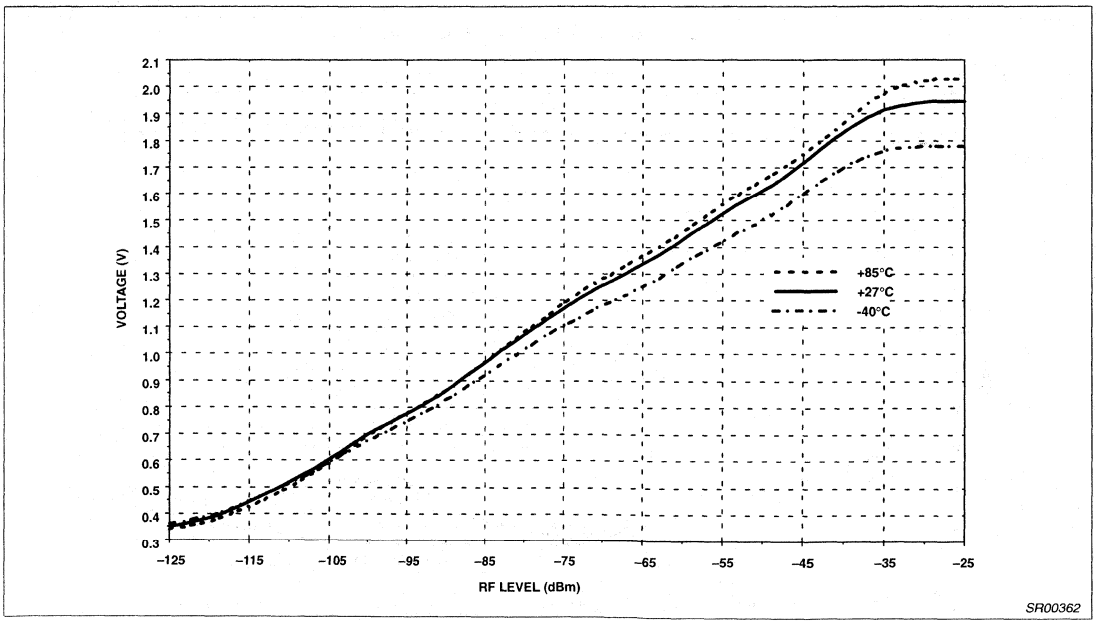


Figure 16. RSSI vs RF Level and Temperature - V_{CC} = 3V

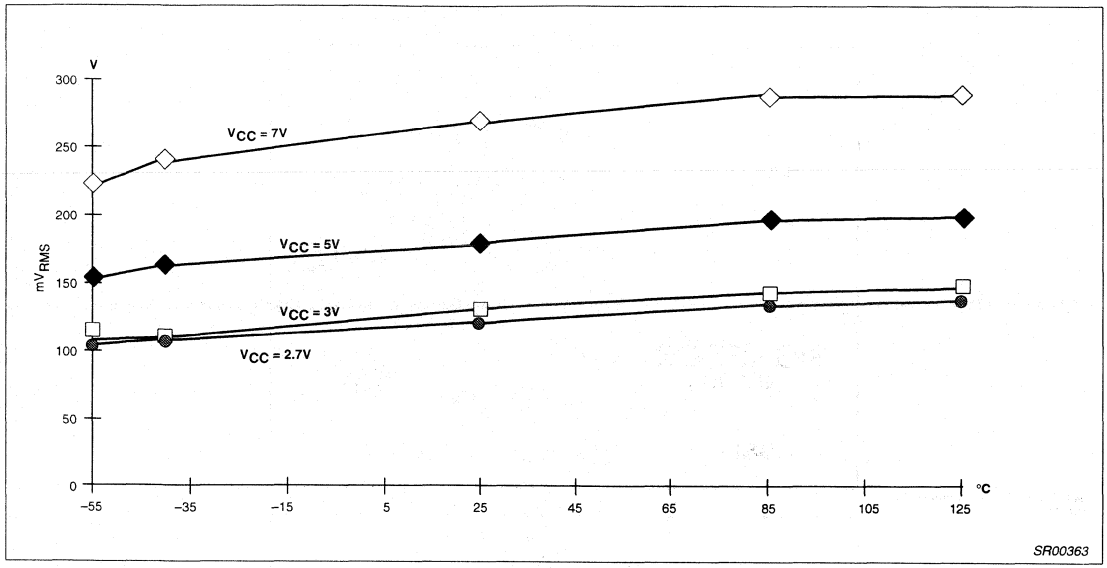
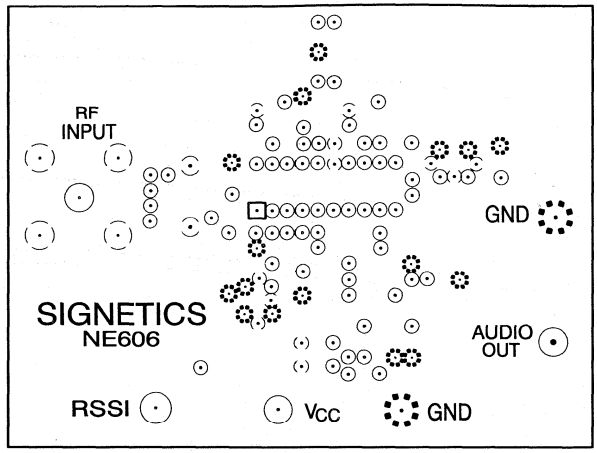
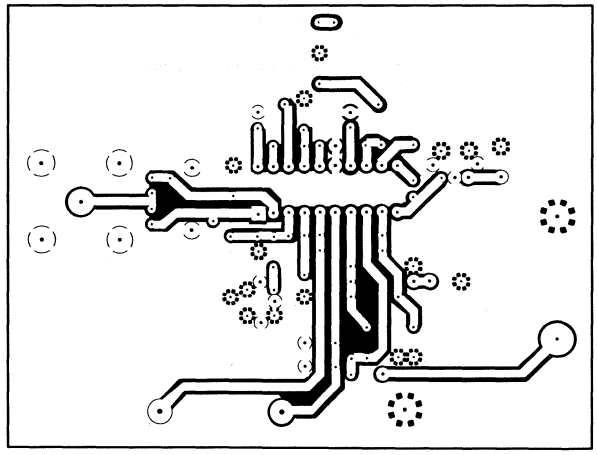


Figure 17. Audio Output vs Temperature

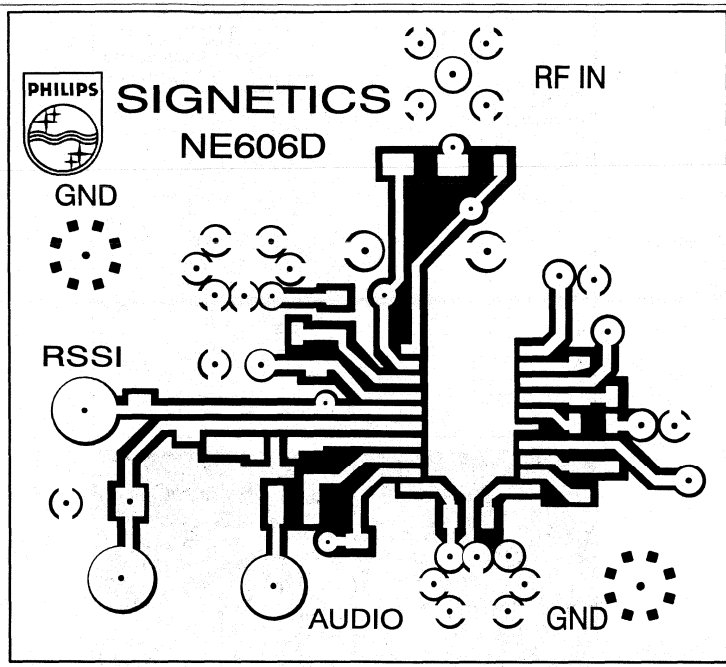


*Applies to Stand-Alone data sheets only.

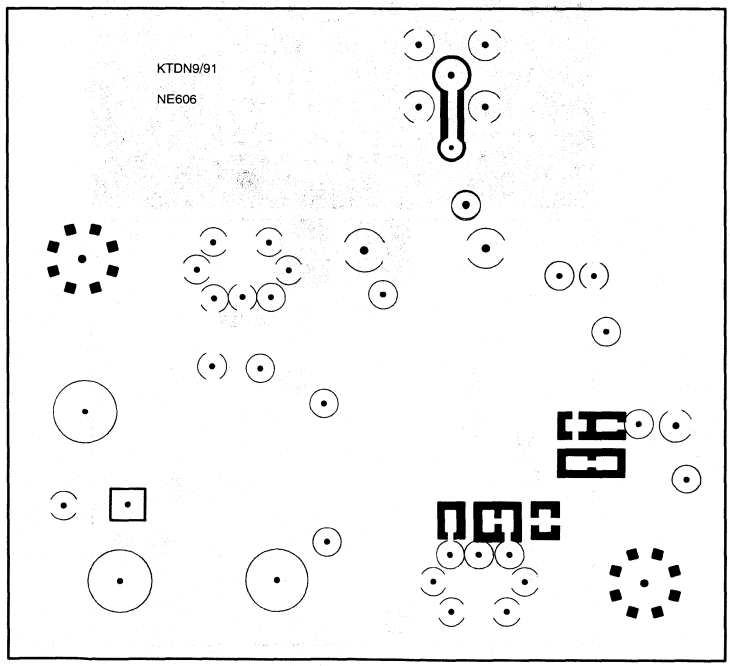


SR00364

Figure 18. SA606N DIP Product Board Layout (Actual Size* — For Reference Use Only)



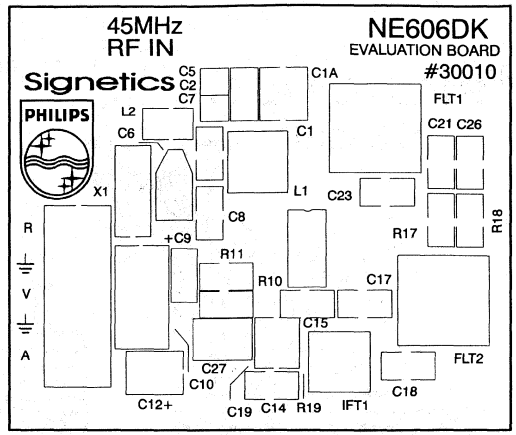
*Applies to Stand-Alone data sheets only.



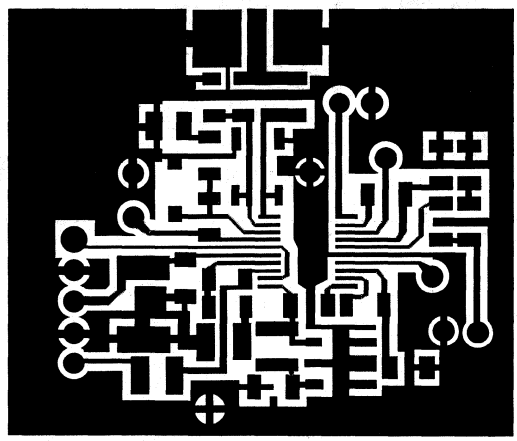
SR00365

Figure 19. SA606D SOL Product Board Layout (2X Actual Size* — For Reference Use Only)

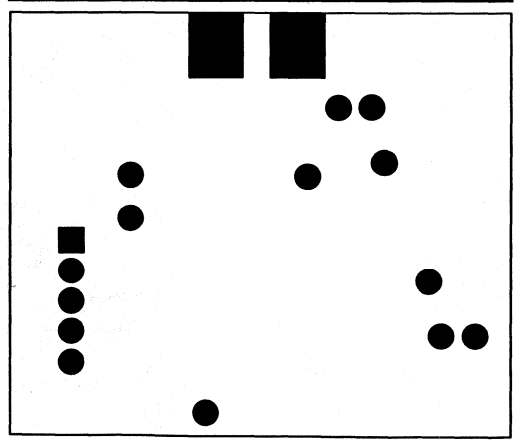
606 Silk Screen



606 TOP



606 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

SR00366

Figure 20.

Low-voltage high performance mixer FM IF system SA616

DESCRIPTION

The SA616 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA616 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The SA616 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE615. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to adjust the output levels or add filtering.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA616 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

PIN CONFIGURATION

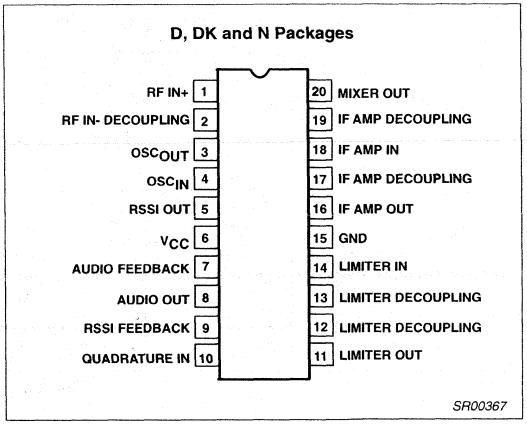


Figure 1. Pin Configuration

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA616N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA616D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA616DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		7	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range		-40 to +85	°C
θ_{JA}	Thermal impedance	D package DK package N package	90 117 75	°C/W

BLOCK DIAGRAM

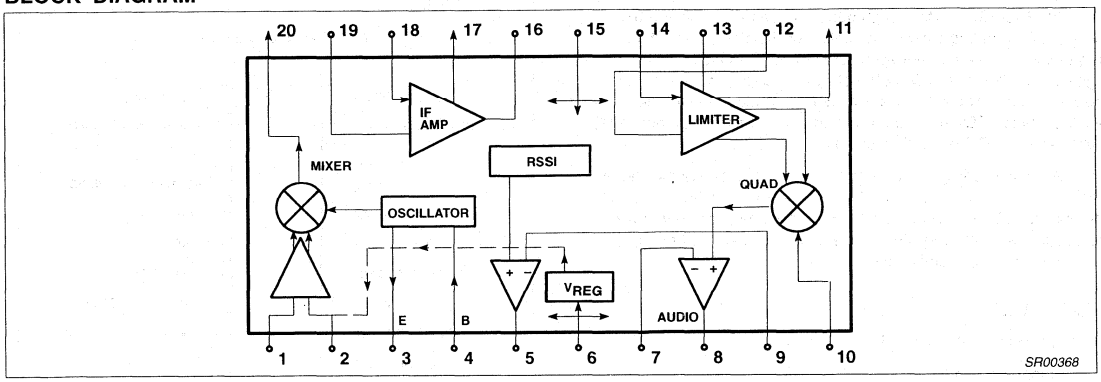


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third-order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = -52dBm		-9		dBm
	Conversion power gain	Matched 14.5dBV step-up	11	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single-ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting -3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		-105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	120		mV
	SINAD sensitivity	IF level -110dBm		17		dB
THD	Total harmonic distortion		-30	-45		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S/N	Signal-to-noise ratio	No modulation for noise		62		dB
	RF RSSI output, R_g = 2kΩ	RF level = -118dBm		0.3	.80	V
		RF level = -68dBm	.70	1.1	2	V
		RF level = -23dBm	1.0	1.8	2.50	V
	RSSI range			80		dB
	RSSI accuracy			±2		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = -27dBm		120		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = -27dBm		2.2		V
	System SINAD sensitivity	RF level = -117dBm		12		dB

CIRCUIT DESCRIPTION

The SA616 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of -9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

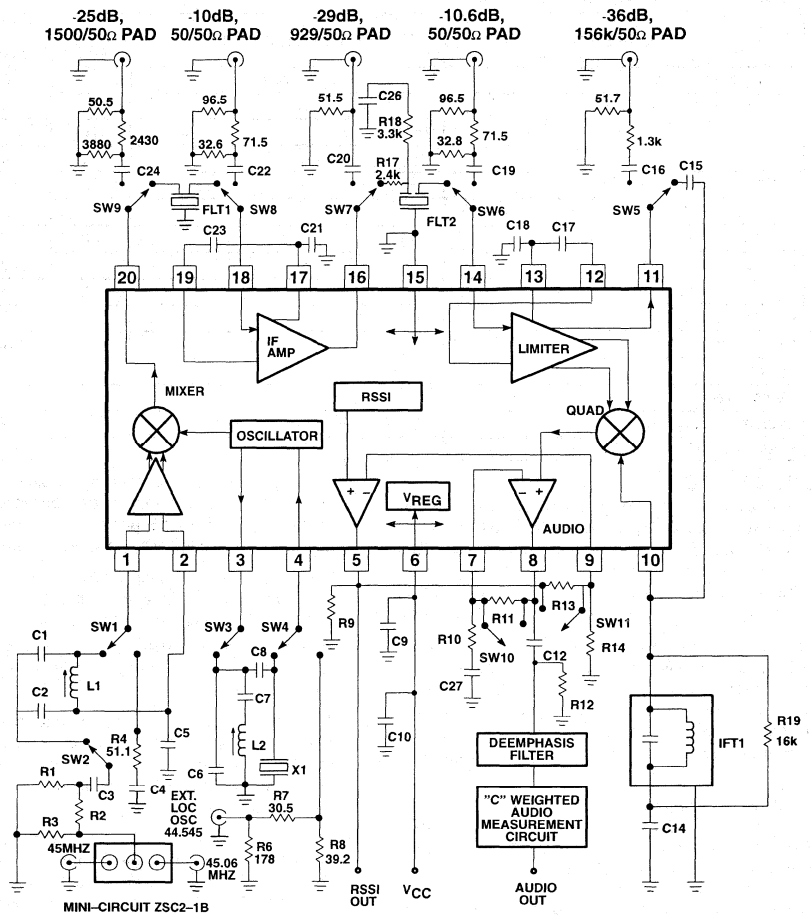
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C8	10.0pF NPO Ceramic	L2	0.8μH nominal
C9	100nF ±10% Monolithic Ceramic		Toko 292CNS–T1038Z
C10	15μF Tantalum (minimum)	X1	44.545MHz Crystal ICM4712701
C12	2.2μF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	8.2kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C23	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C26	100nF ±10% Monolithic Ceramic	R19	16kΩ

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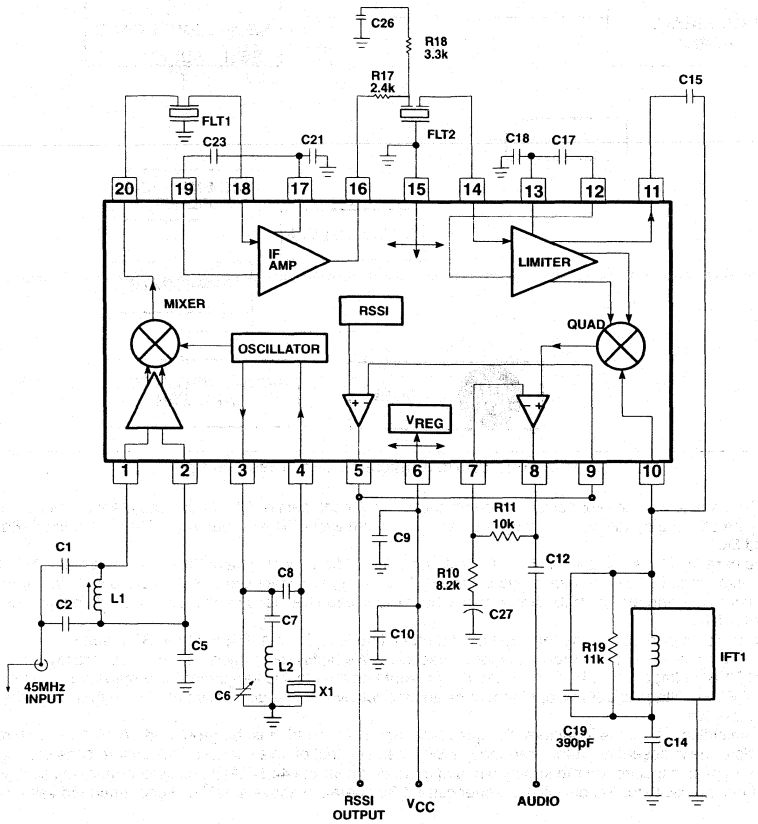
Figure 3. SA616 45MHz Test Circuit (Relays as shown)



NE616D/DK Demoboard
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15µF Tantalum (minimum)
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

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Figure 4. SA616 45MHz Application Circuit

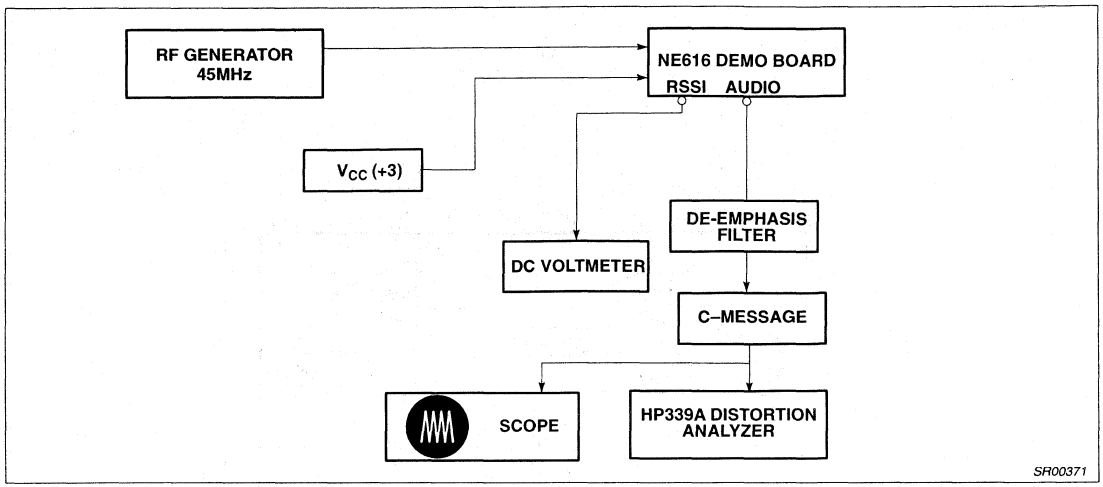


Figure 5. SA616 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or -116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

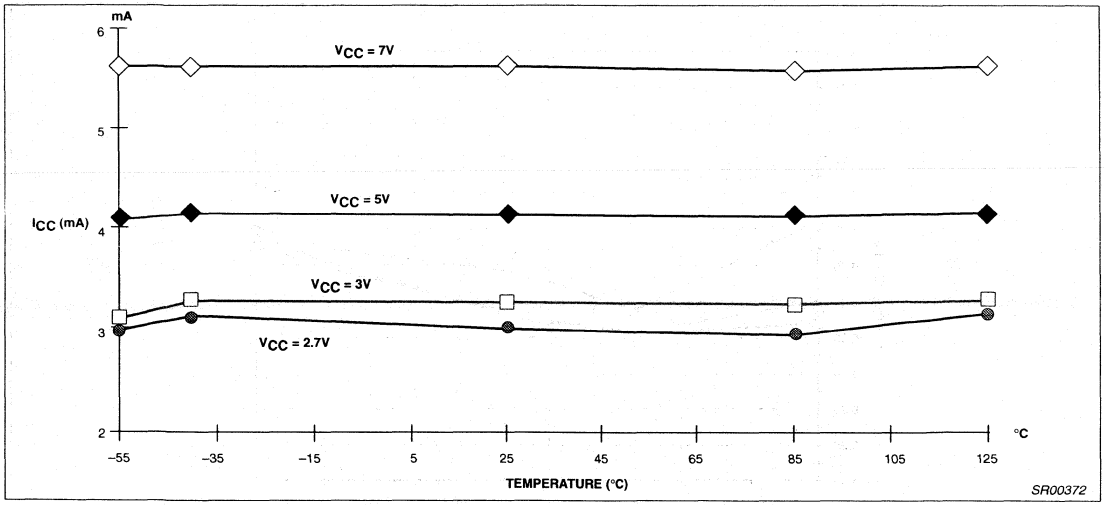


Figure 6. I_{CC} vs Temperature

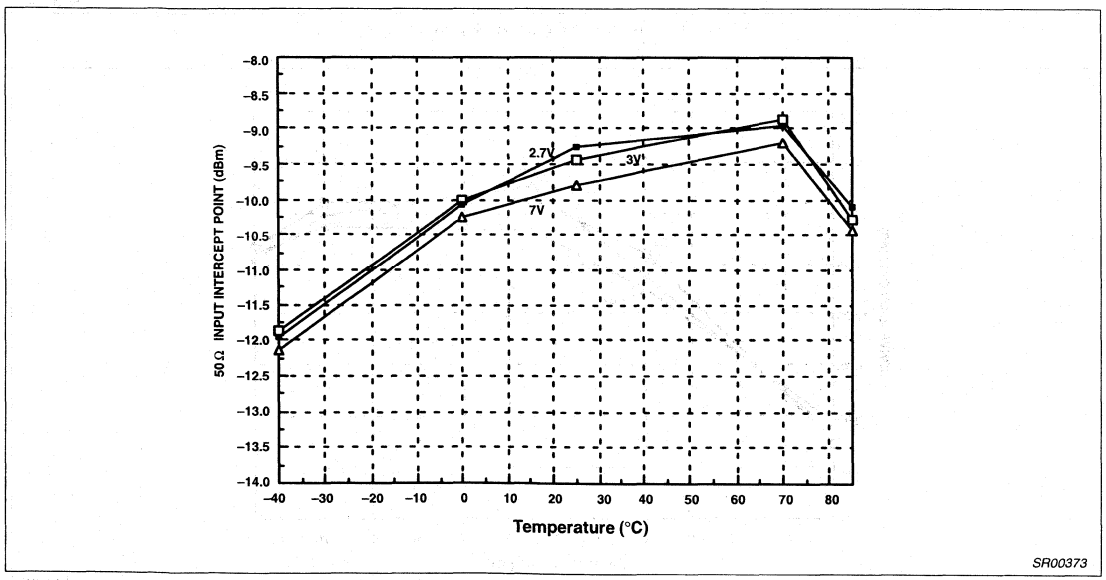


Figure 7. Third Order Intercept Point vs Supply Voltage

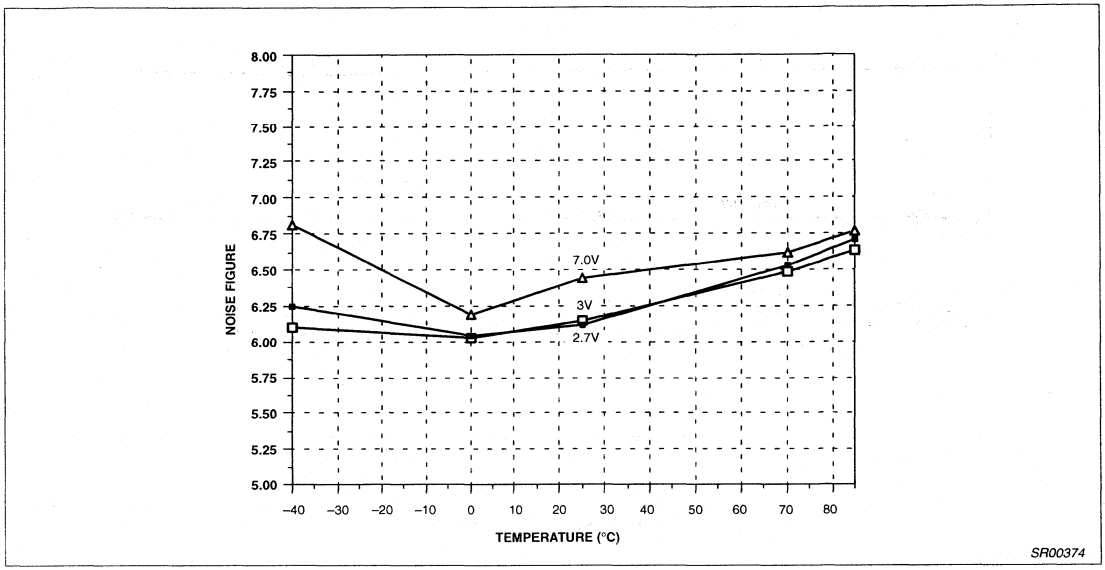


Figure 8. Mixer Noise Figure vs Supply Voltage

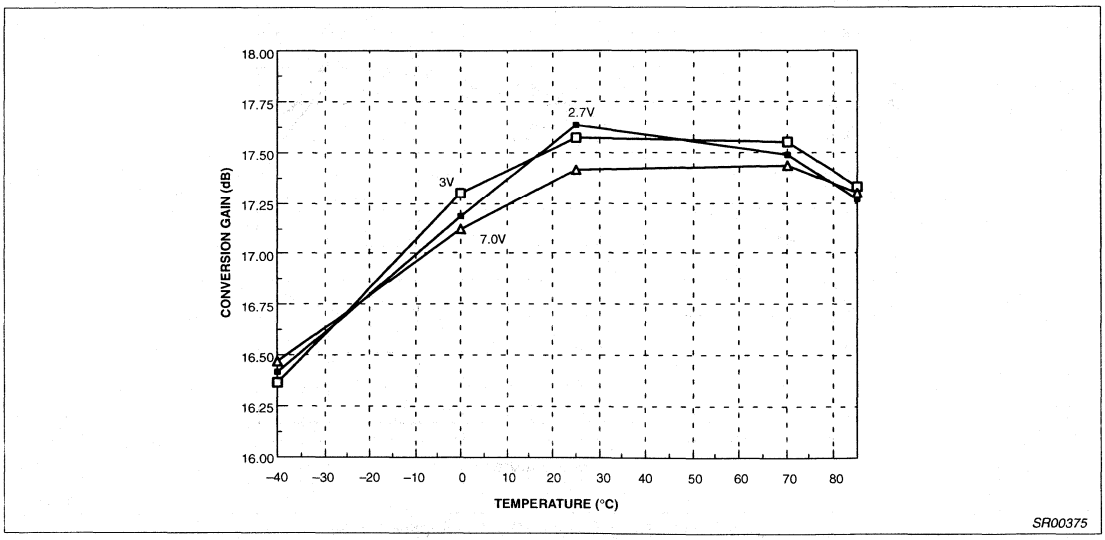


Figure 9. Conversion Gain vs Supply Voltage

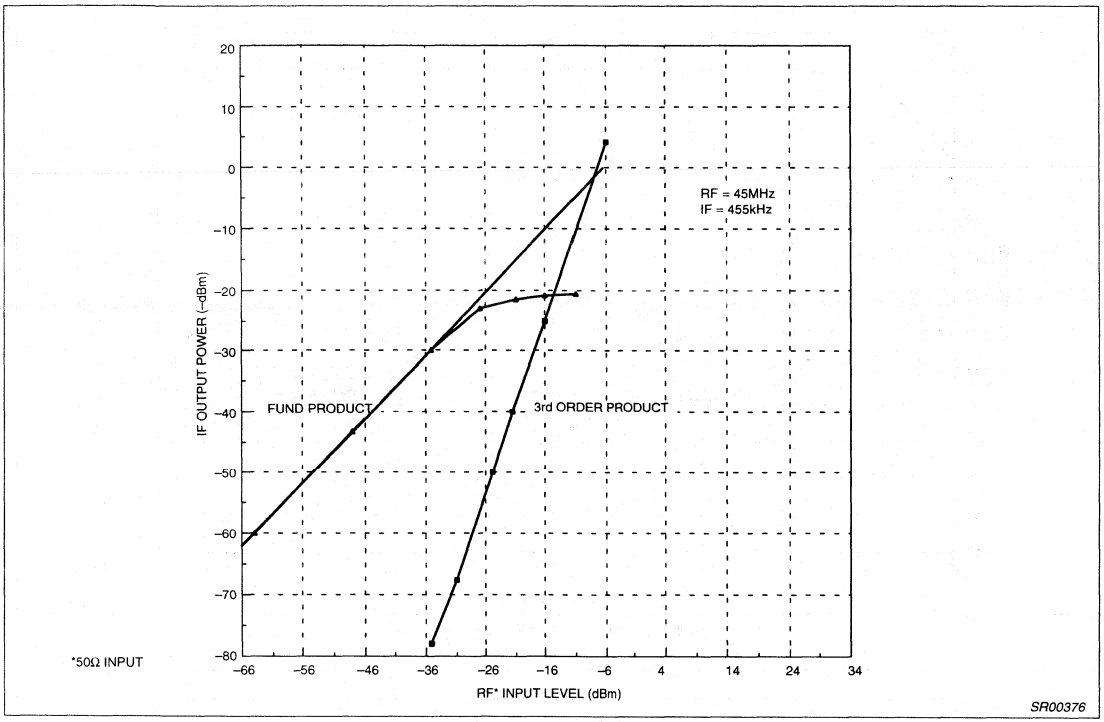


Figure 10. Mixer Third Order Intercept and Compression

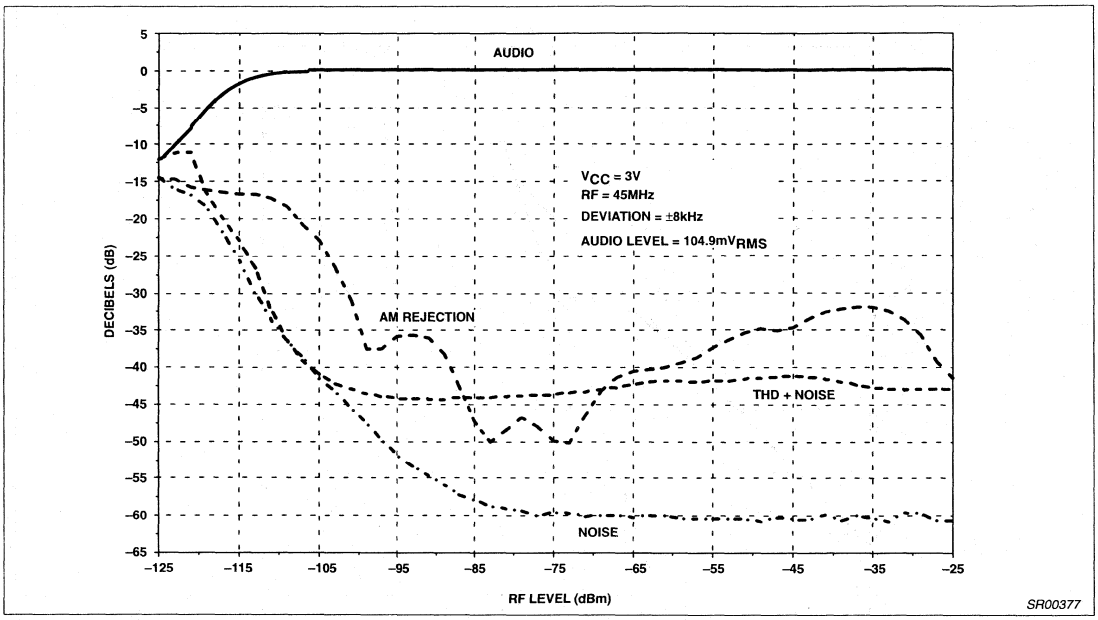


Figure 11. Sensitivity vs RF Level (-40°C)

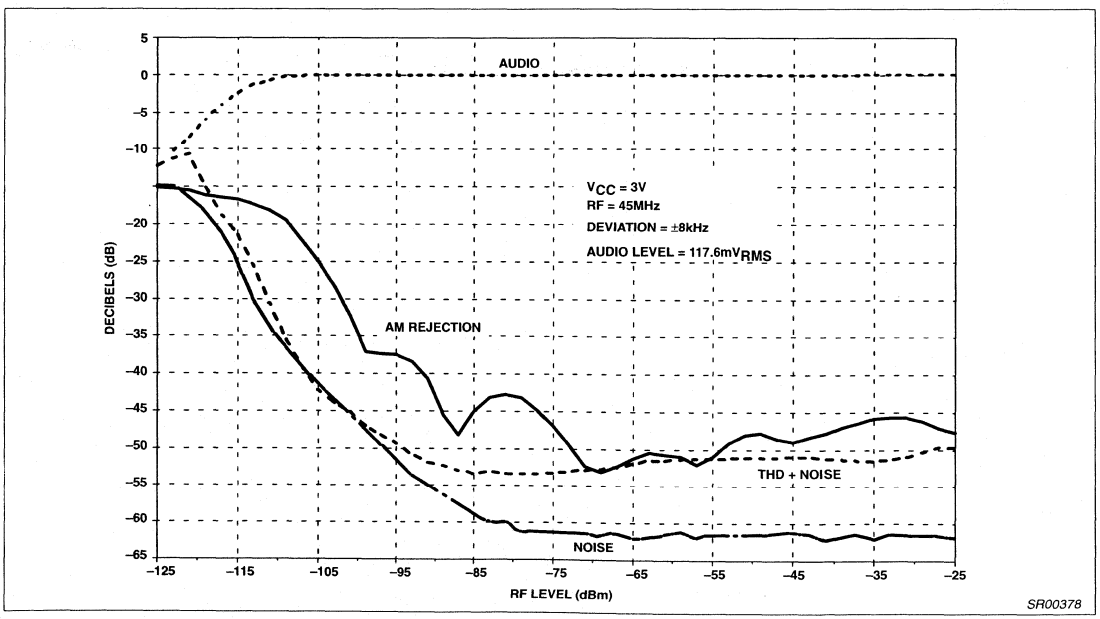


Figure 12. Sensitivity vs RF Level (+25°C)

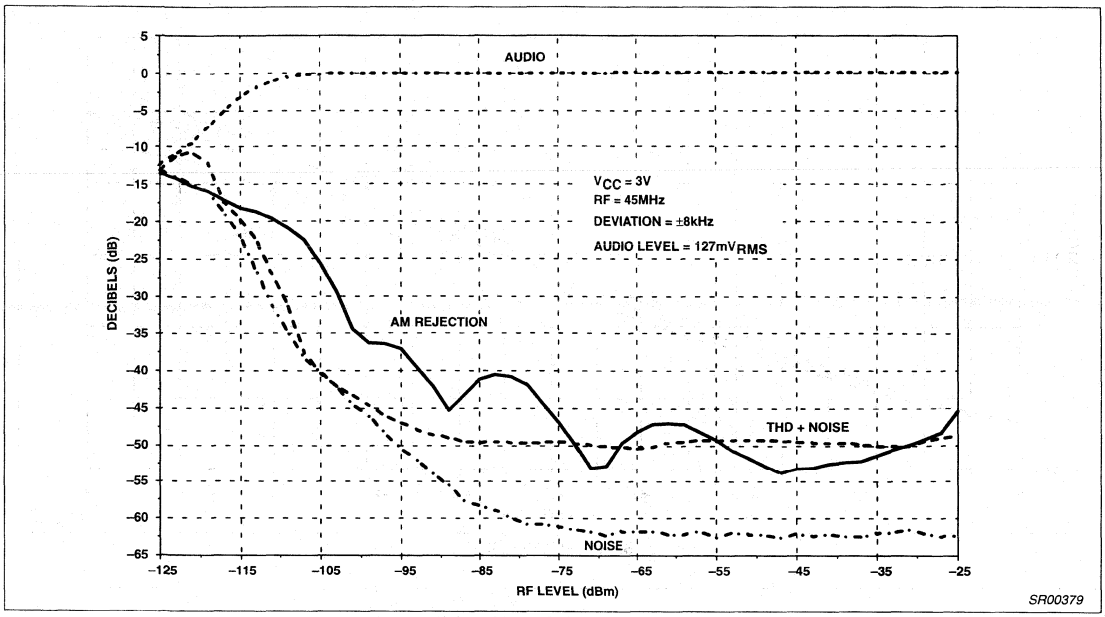


Figure 13. Sensitivity vs RF Level (Temperature 85°C)

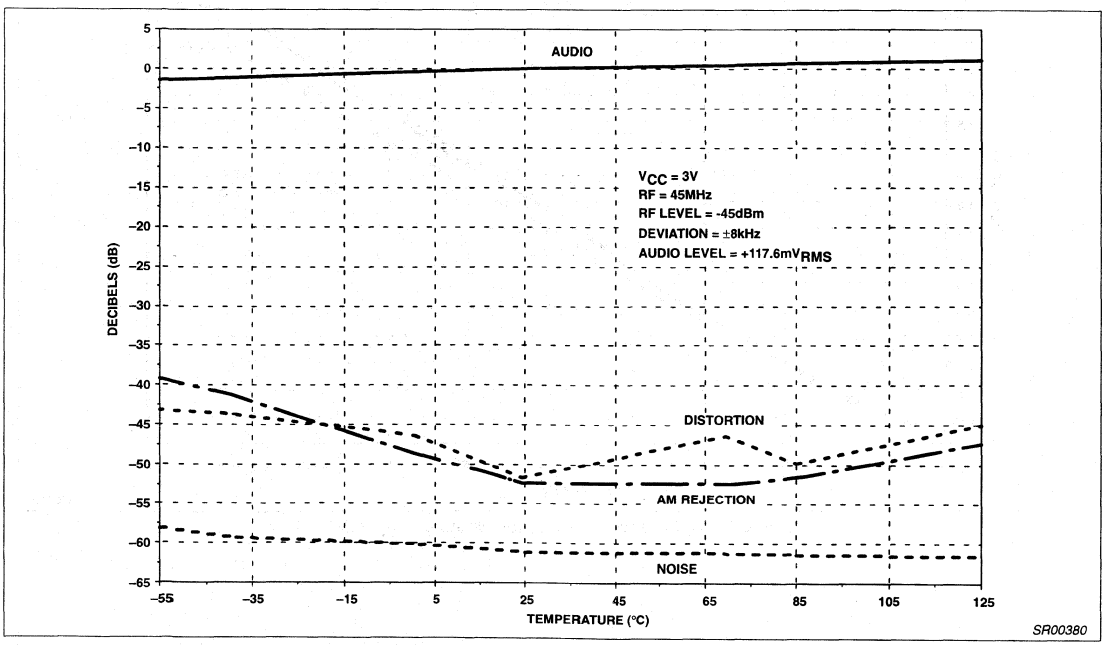


Figure 14. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

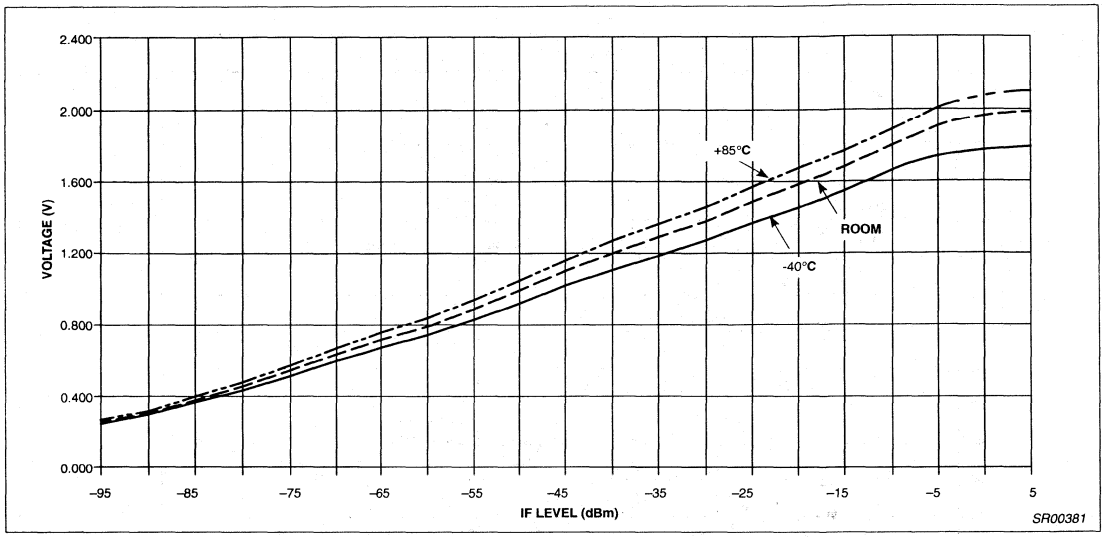


Figure 15. RSSI (455kHz IF @ 3V)

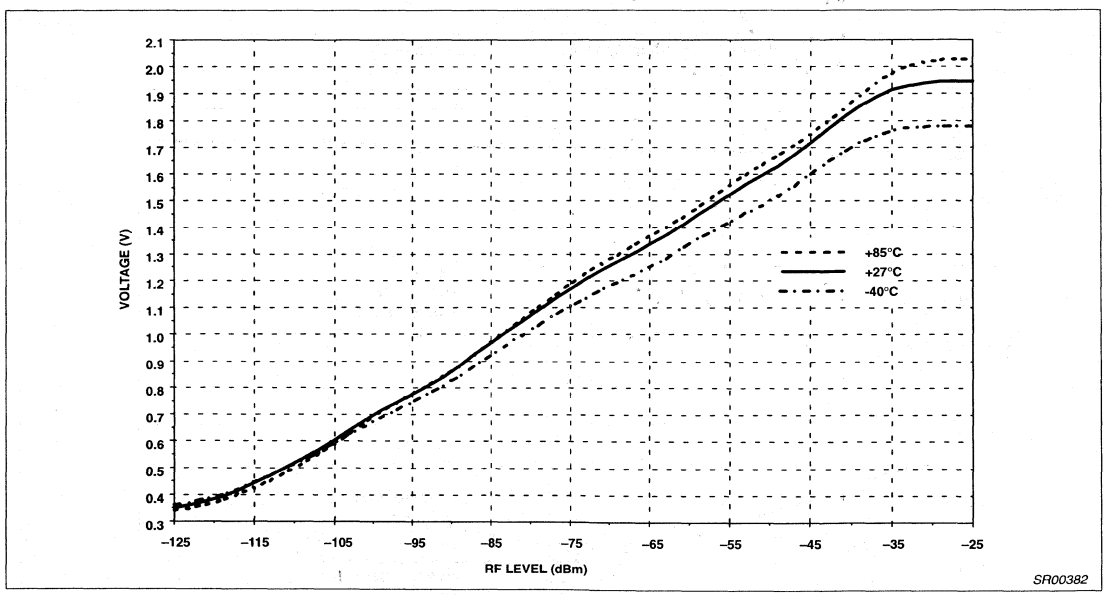


Figure 16. RSSI vs RF Level and Temperature - V_{CC} = 3V

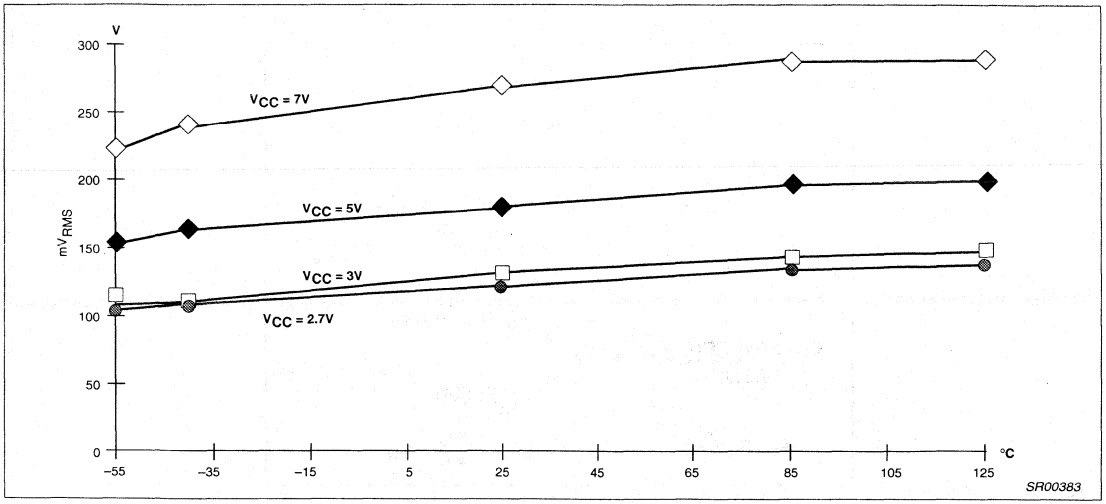
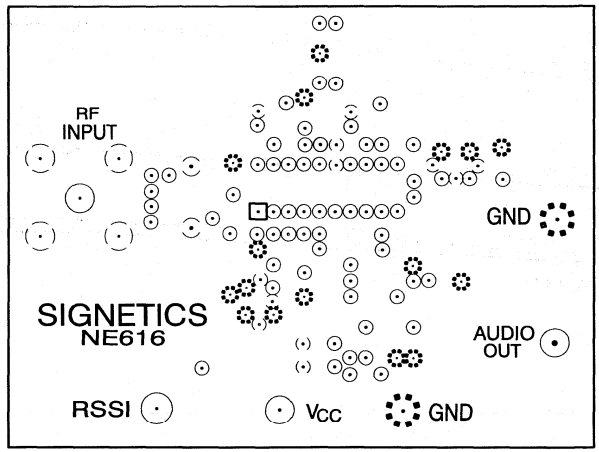
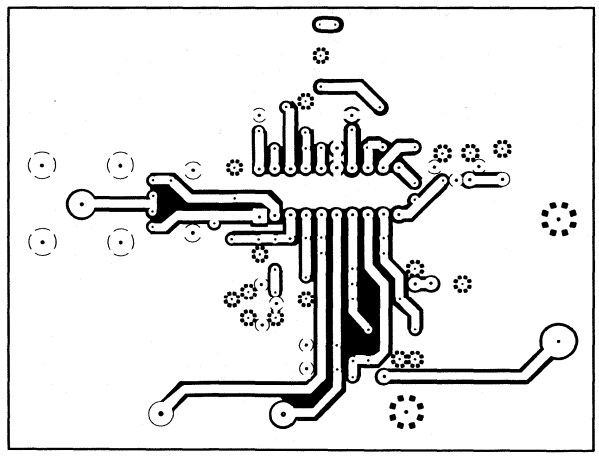


Figure 17. Audio Output vs Temperature

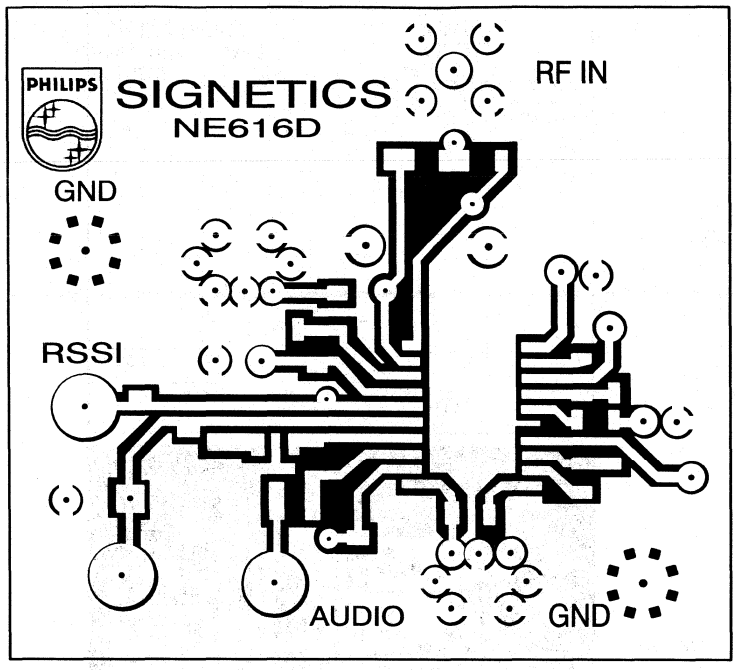


*Applies to Stand-Alone data sheets only.

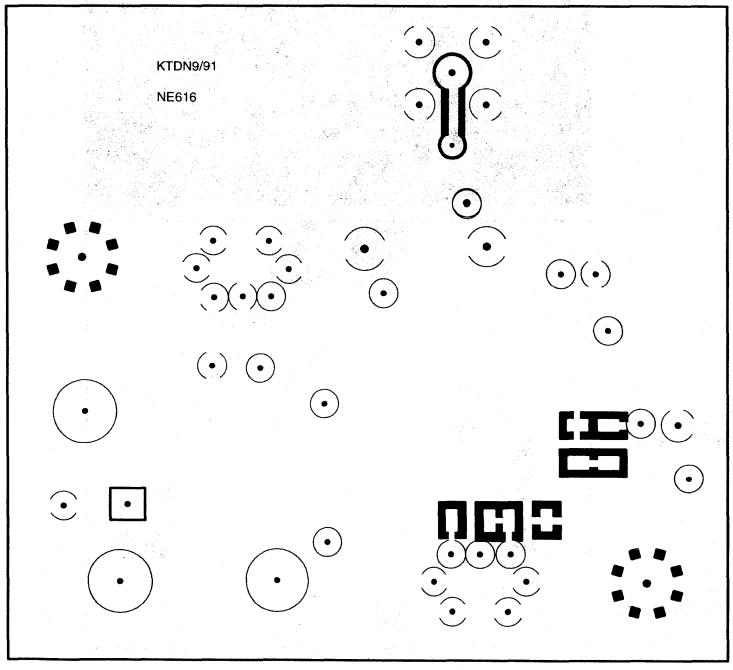


SR00384

Figure 18. SA616N DIP Product Board Layout (Actual Size* — For Reference Use Only)



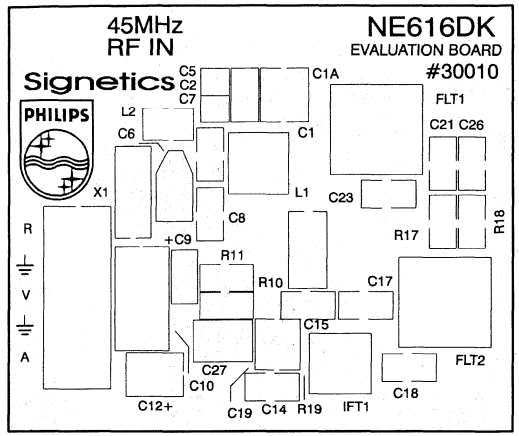
*Applies to Stand-Alone data sheets only.



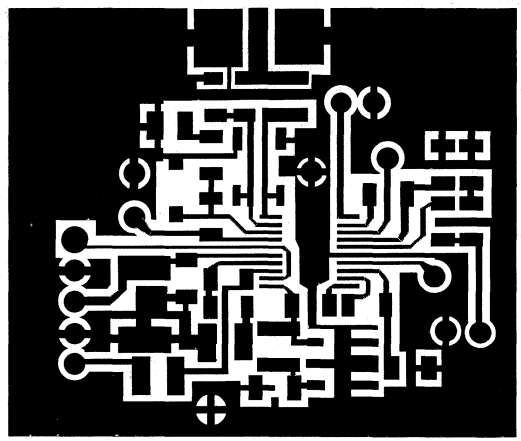
SR00385

Figure 19. SA616D SOL Product Board Layout (2X Actual Size* — For Reference Use Only)

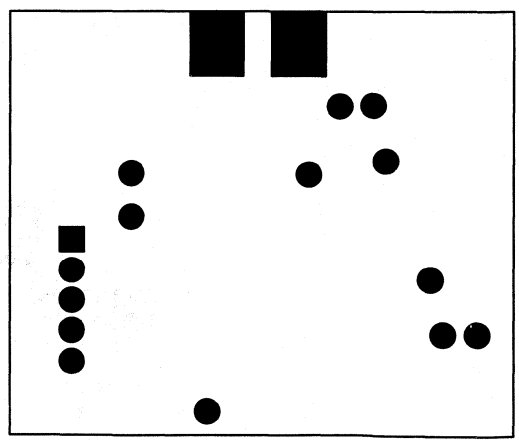
616 Silk Screen



616 TOP



616 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

SR00386

Figure 20.

Low-voltage mixer FM IF system SA676

DESCRIPTION

The SA676 is a low-voltage monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA676 is available in a 20-pin SSOP (shrink small outline package).

The SA676 was designed for cordless telephone applications in which efficient and economic integrated solutions are required and yet high performance is desirable. Although the product is not targeted to meet the stringent specifications of high performance cellular equipment, it will exceed the needs for analog cordless phones. The minimal amount of external components and absence of any external adjustments makes for a very economical solution.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >100MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 100MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 70dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters

PIN CONFIGURATION

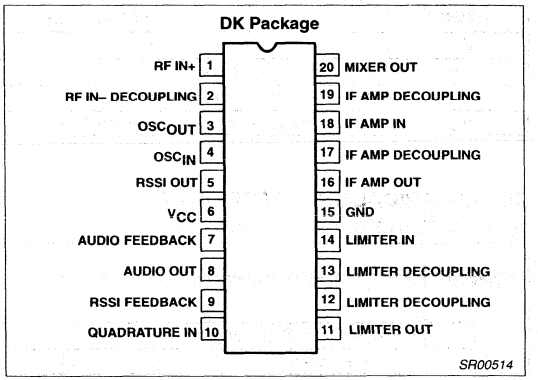


Figure 1. Pin Configuration

- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATION

- Cordless phones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA676DK	SOT266-1

BLOCK DIAGRAM

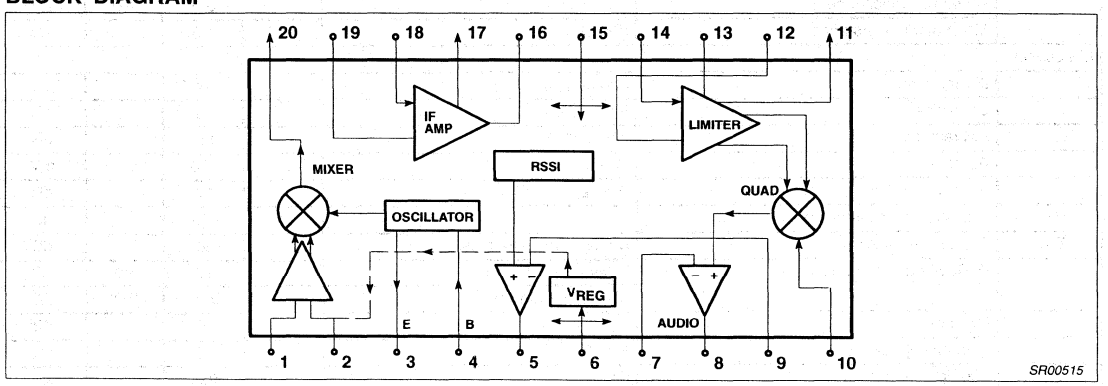


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range	–40 to +85	°C
θ_{JA}	Thermal impedance DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA676			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz; +14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = –45dBm; FM modulation = 1kHz with ±5kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV_{RMS})						
f_{IN}	Input signal frequency			100		MHz
f_{OSC}	Crystal oscillator frequency			100		MHz
	Noise figure at 45MHz			7.0		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = –52dBm		–10		dBm
	Conversion power gain	Matched 14.5dBV step–up	10	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	AM rejection	30% AM 1kHz		50		dB
	Audio level	Gain of two	60	120		mV
	SINAD sensitivity	IF level –110dBm		17		dB
THD	Total harmonic distortion			–55		dB
S/N	Signal–to–noise ratio	No modulation for noise		60		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –110dBm		0.5	.90	V
		IF level = –50dBm		1.7	2.2	V
	RSSI range			70		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
RF/IF section (int LO)						
	System SINAD sensitivity	RF level = –114dBm		12		dB

NOTE:
1. The generator source impedance is 50Ω, but the SA676 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA676 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA676 is an IF signal processing system suitable for second IF systems with input frequency as high as 100MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 7.0dB, conversion gain of 17dB, and input third-order intercept of –10dBm. The oscillator will operate in excess of 100MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations.

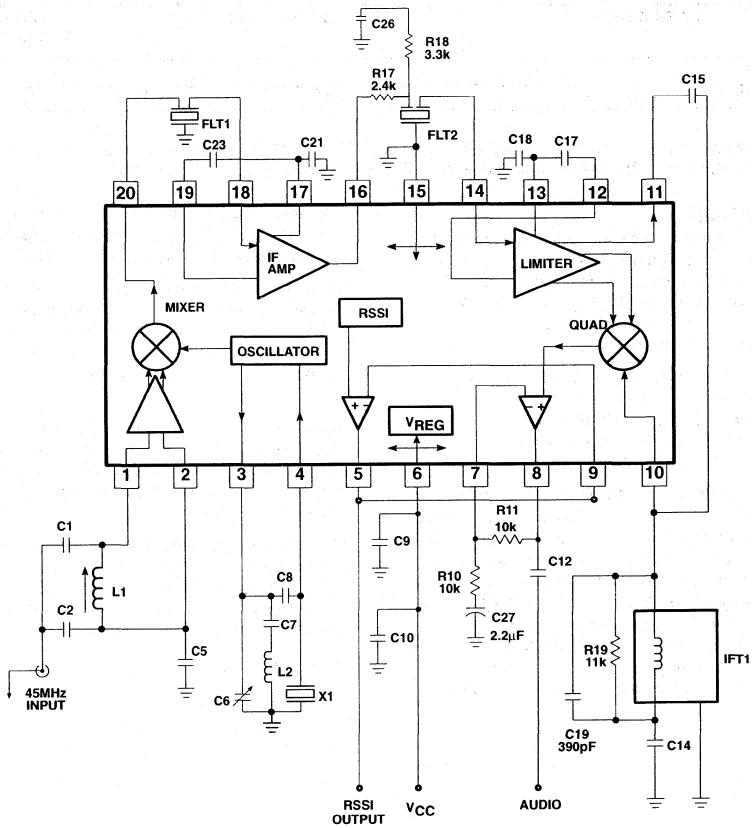
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 44dB of gain and 5.5MHz bandwidth. The IF limiter has 58dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 10kΩ with a rail-to-rail output.

A log signal strength indicator completes the circuitry. The output range is greater than 70dB and is temperature compensated. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



SA676DK Demoboard
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF +10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
FLT 1	Ceramic Filter Murata SFG455A3 or equiv
FLT 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	330nH Coilcraft UNI-10/142-04J08S
L2	0.8µH nominal TOKO 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

* NOTE: This value can be reduced when a battery is the power source.

SR00516

Figure 3. SA676 45MHz Application Circuit

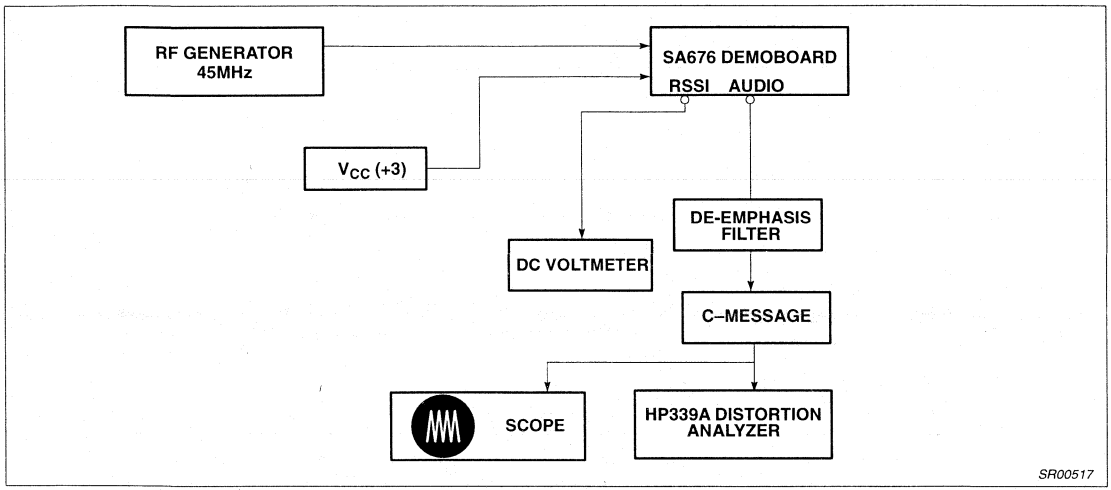


Figure 4. SA676 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339A analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All specifications and testing are done with the wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.45μV or –114dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

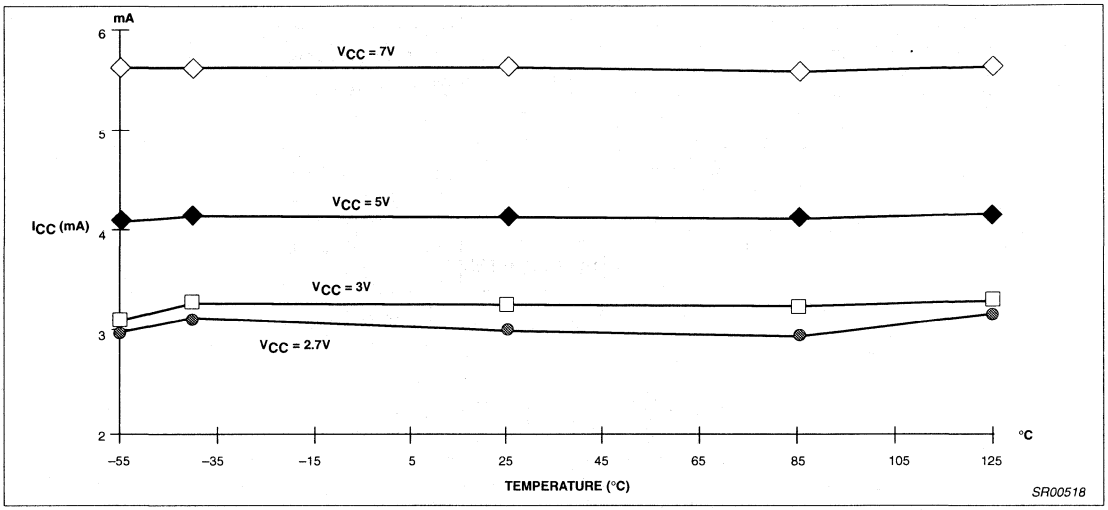


Figure 5. I_{CC} vs Temperature and Supply Voltage

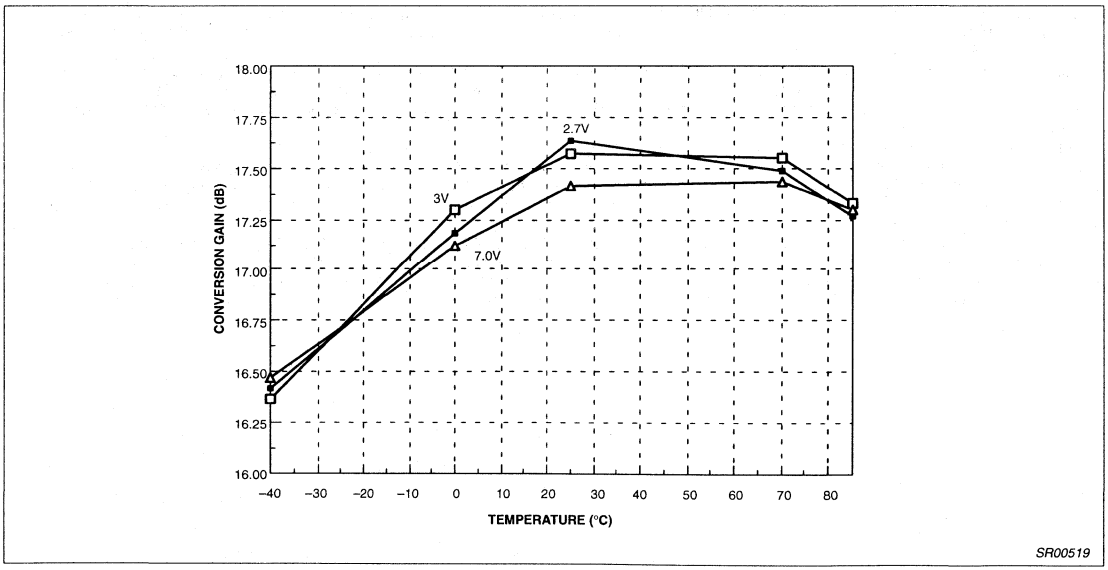


Figure 6. Conversion Gain vs Temperature and Supply Voltage

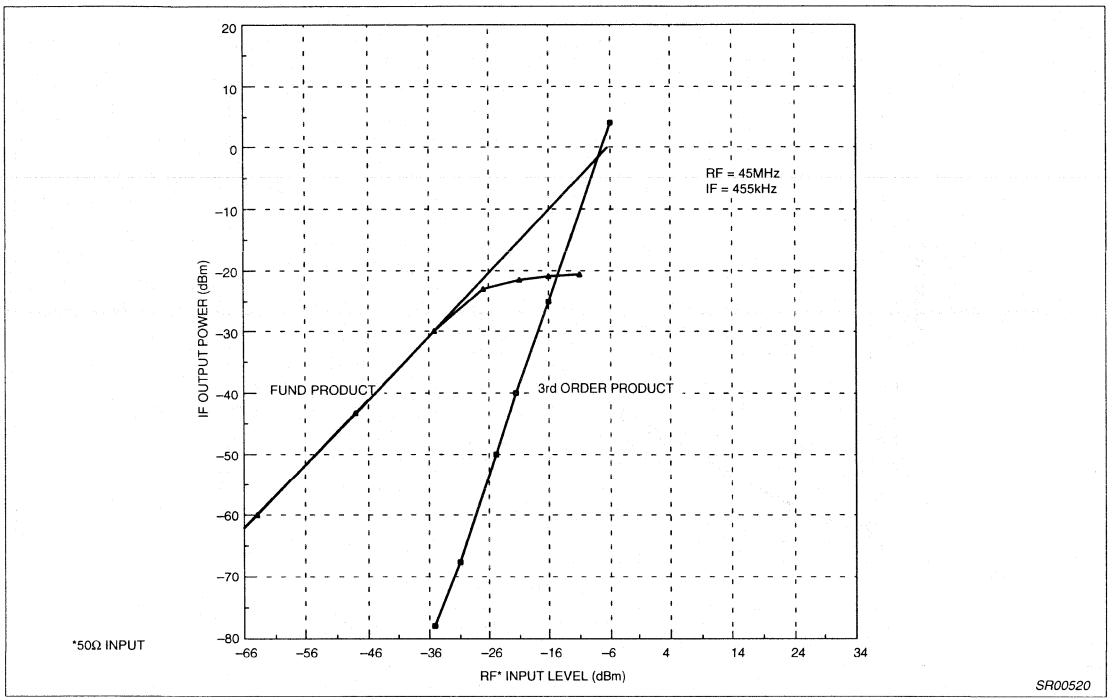


Figure 7. Mixer Third Order Intercept and Compression

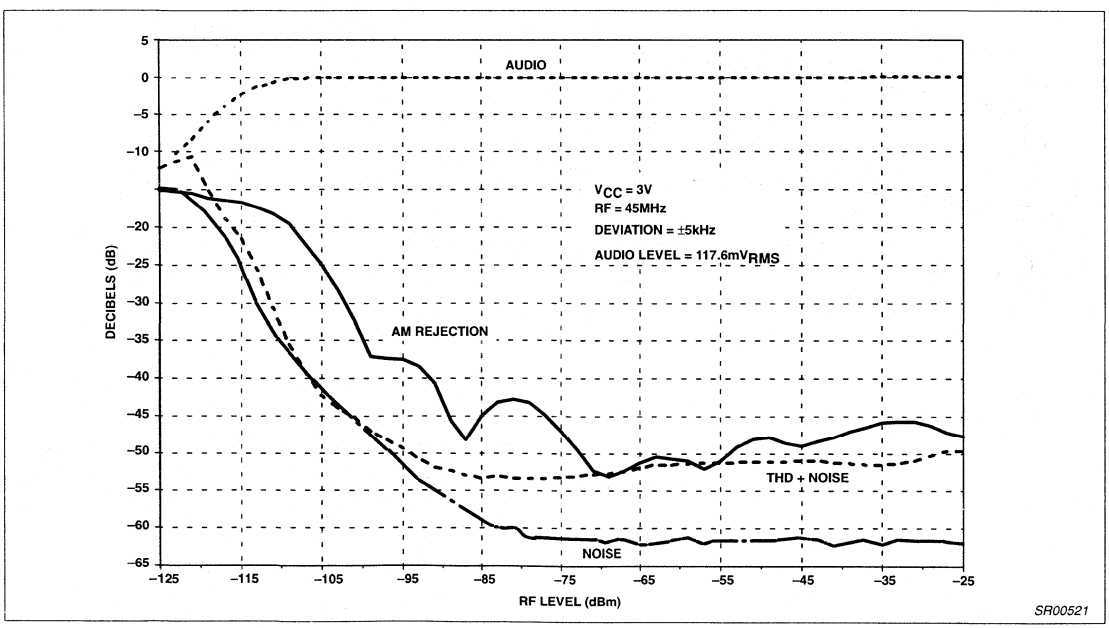


Figure 8. Sensitivity vs RF Level (+25°C)

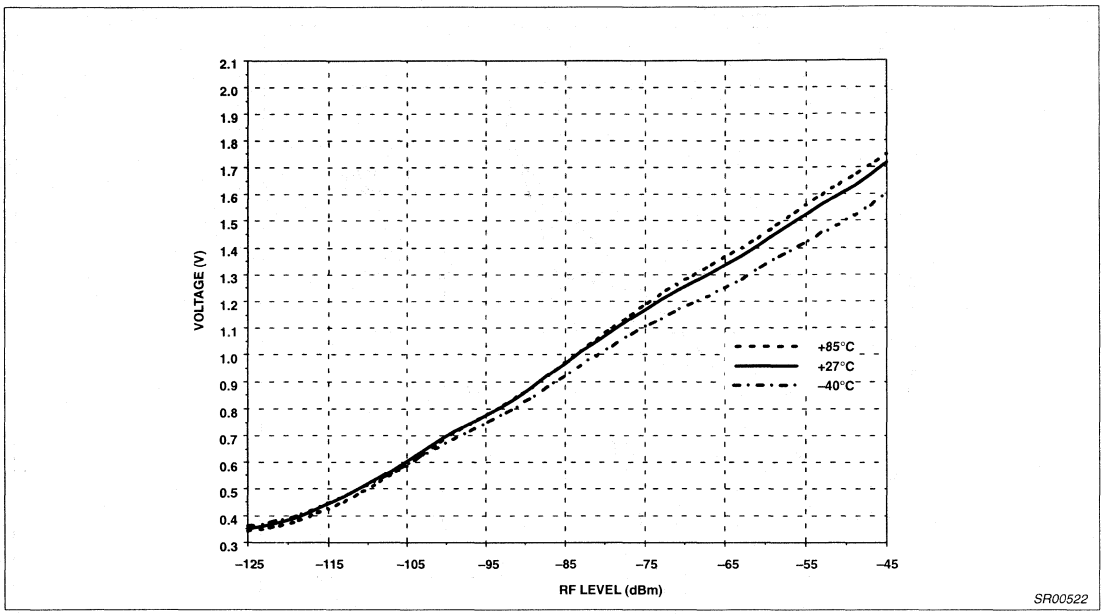


Figure 9. RSSI vs RF Level and Temperature - V_{CC} = 3V

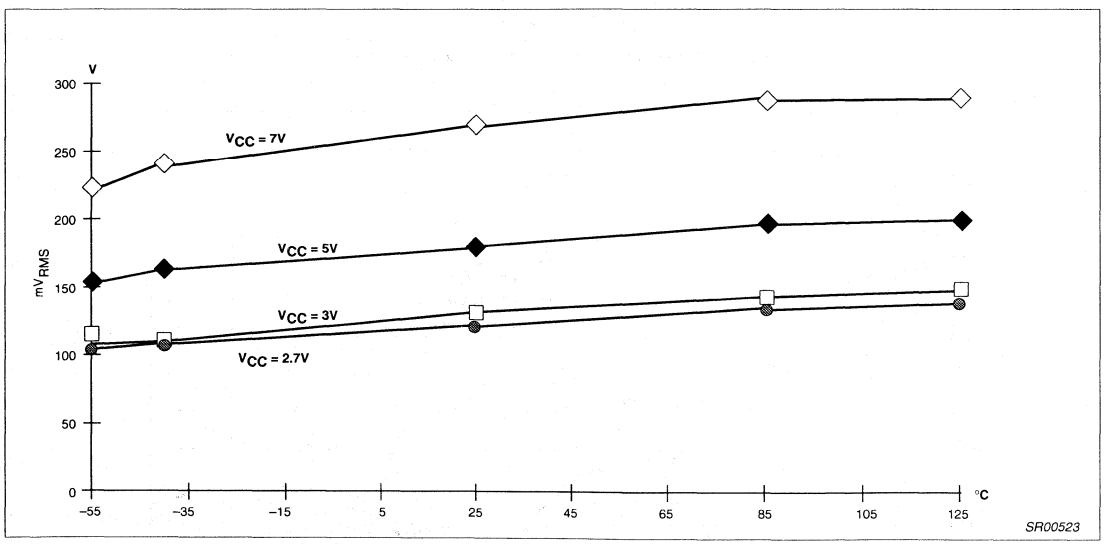


Figure 10. Audio Output vs Temperature and Supply Voltage

Low voltage high performance mixer FM IF system SA607

DESCRIPTION

The SA607 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA607 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA607 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The SA607 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA607 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp

PIN CONFIGURATION

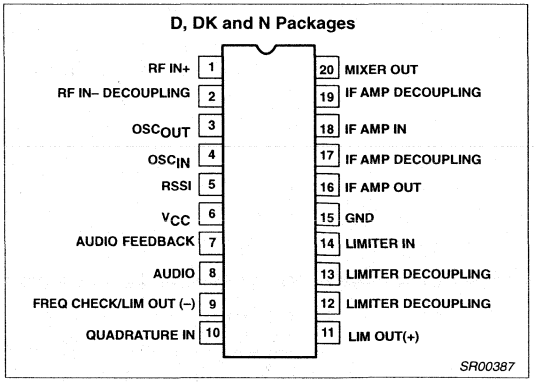


Figure 1. Pin Configuration

- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA607N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA607D	SOT163-1
20-Pin Plastic Shirnk Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA607DK	SOT266-1

BLOCK DIAGRAM

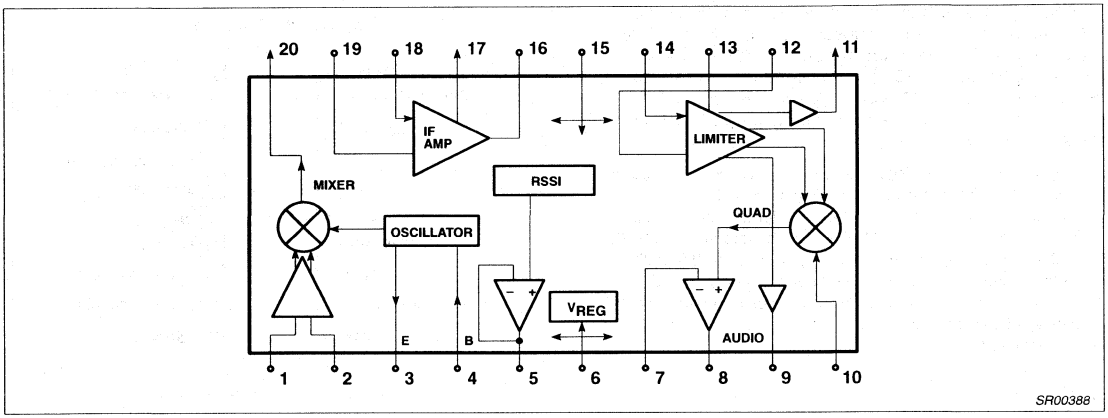


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range SA607	−40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA607			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA607 MIN	LIMITS SA607 TYP	LIMITS SA607 MAX	UNITS
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) No load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/limiter output impedance	(Pin 9)		200		Ω
	Frequency check/limiter output level	(Pin 9) No load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA607 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA607 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA607 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

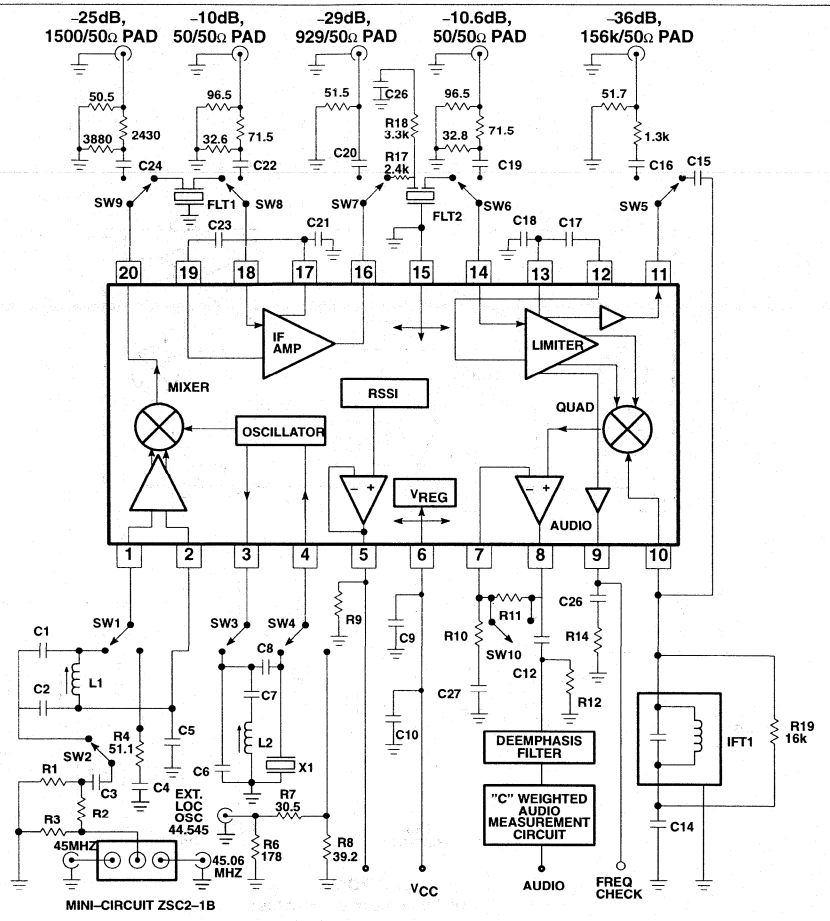
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter output or Frequency Check output has drive capability of a load minimum of 2kΩ or higher to obtain 115mV output level.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



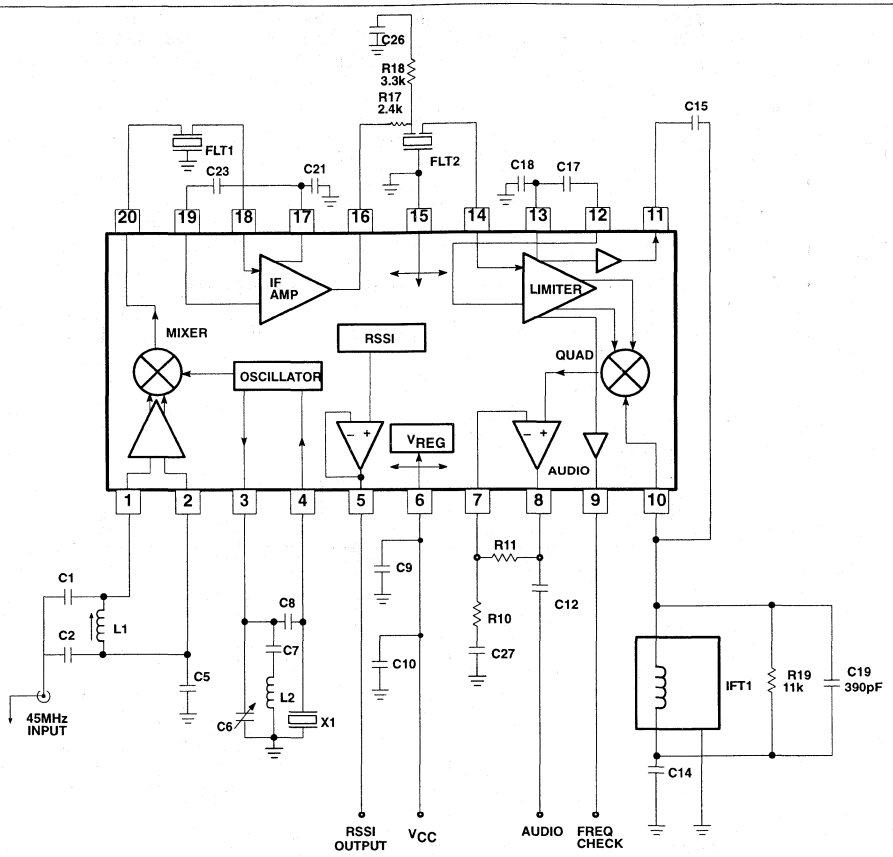
Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R12	2kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

SR00389

Figure 3. SA607 45MHz Test Circuit (Relays as shown)



SA607D/DK
Application Component List

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C5	100nF ±10% Monolithic Ceramic
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C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2μF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330μH TOKO 303LN-1130
L1	.33μH TOKO SCB-1320Z
L2	1.2μH Coilcraft 1008C S-122
X1	44.545MHz Crystal Hy–Q
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

SR00390

Figure 4. SA607 45MHz Application Circuit

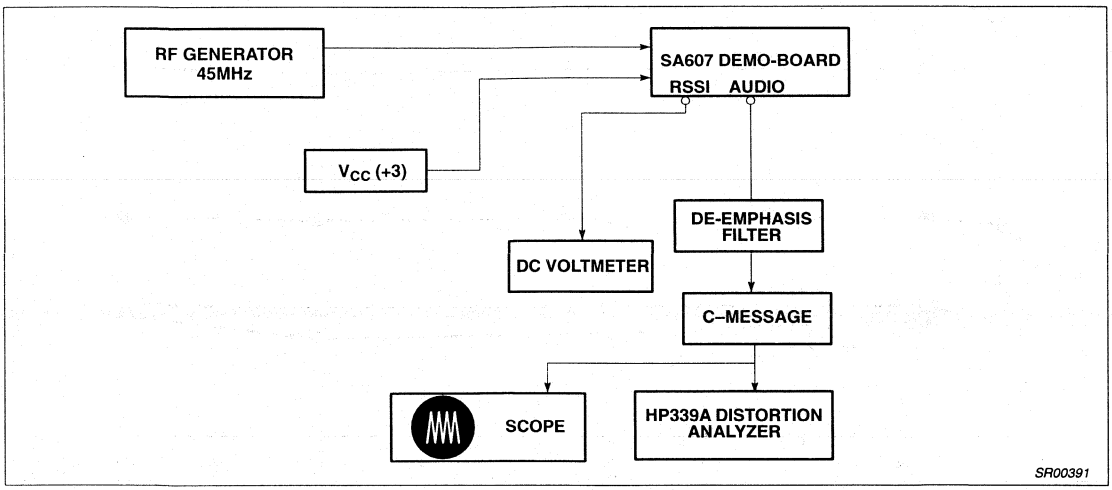


Figure 5. SA607 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

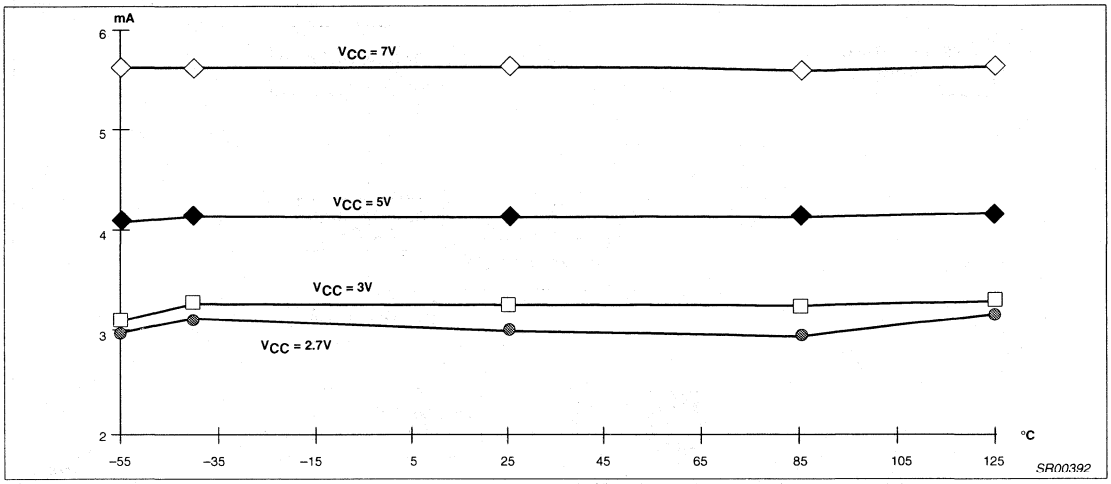


Figure 6. I_{CC} vs Temperature

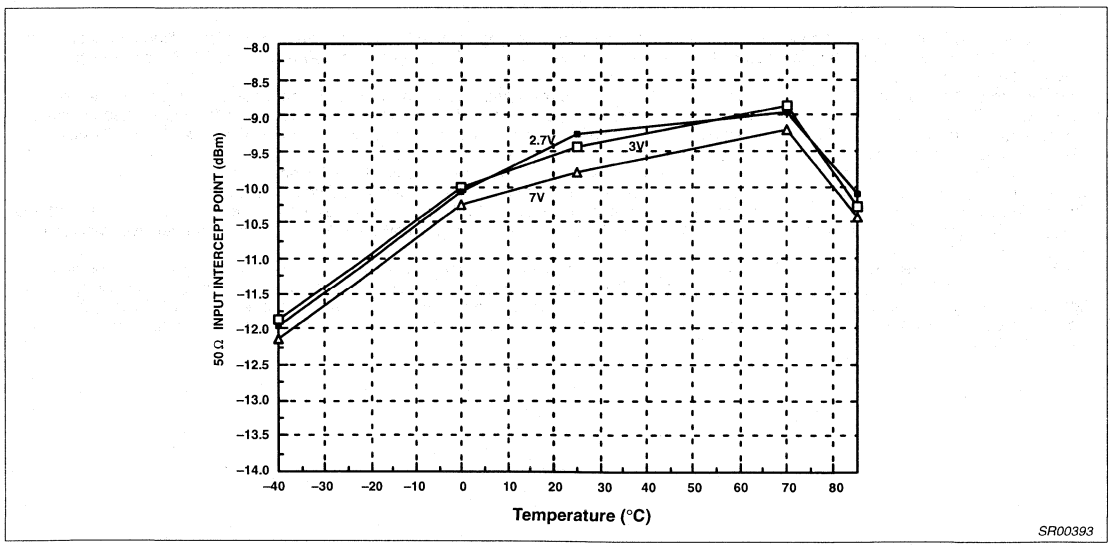


Figure 7. Third Order Intercept Point vs Supply Voltage

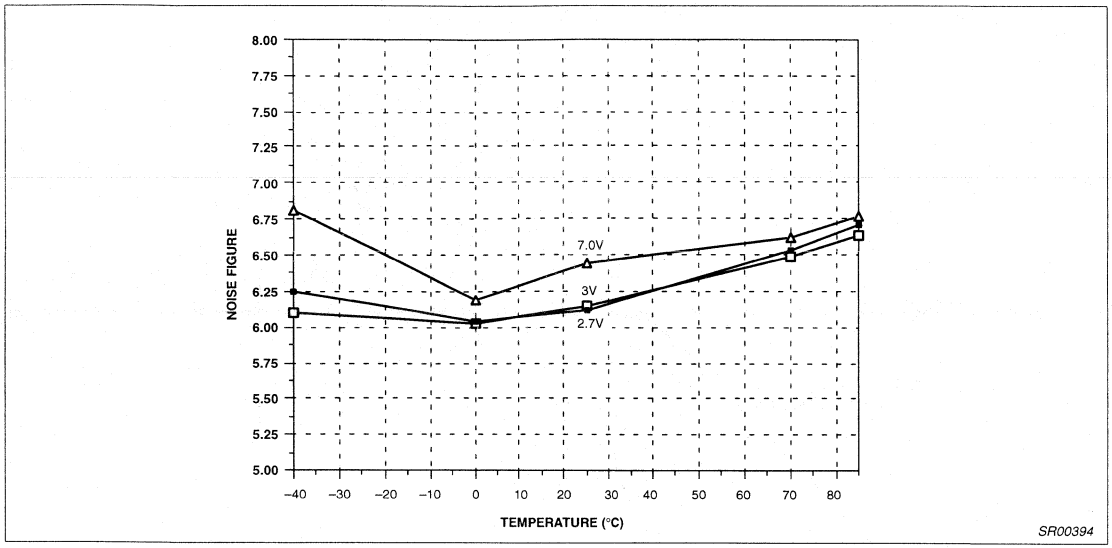


Figure 8. Mixer Noise Figure vs Supply Voltage

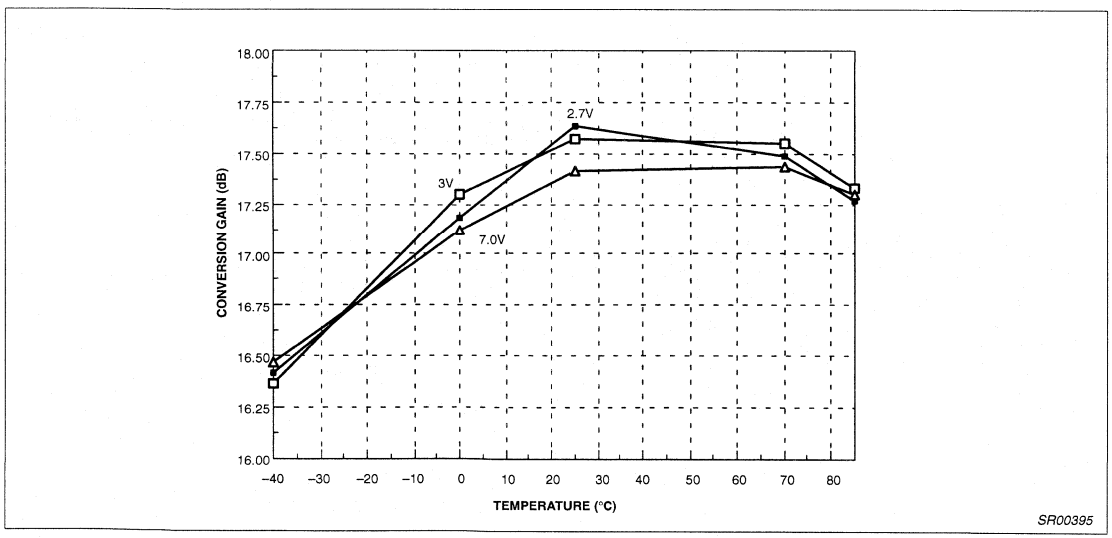


Figure 9. Conversion Gain vs Supply Voltage

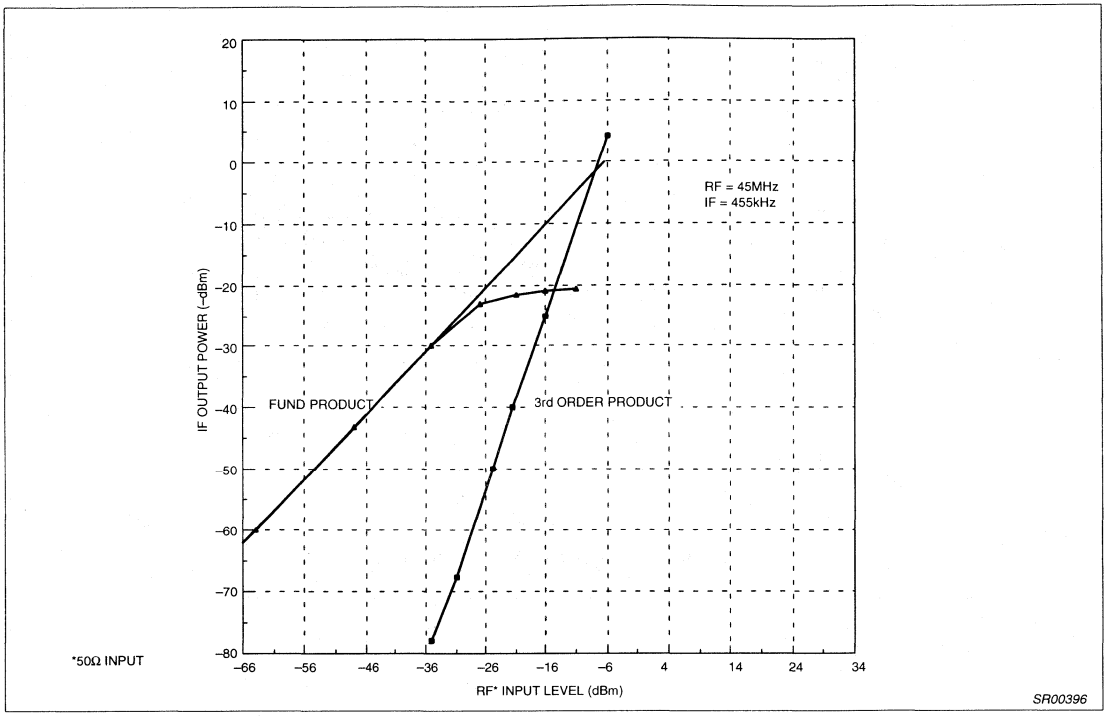


Figure 10. Mixer Third Order Intercept and Compression

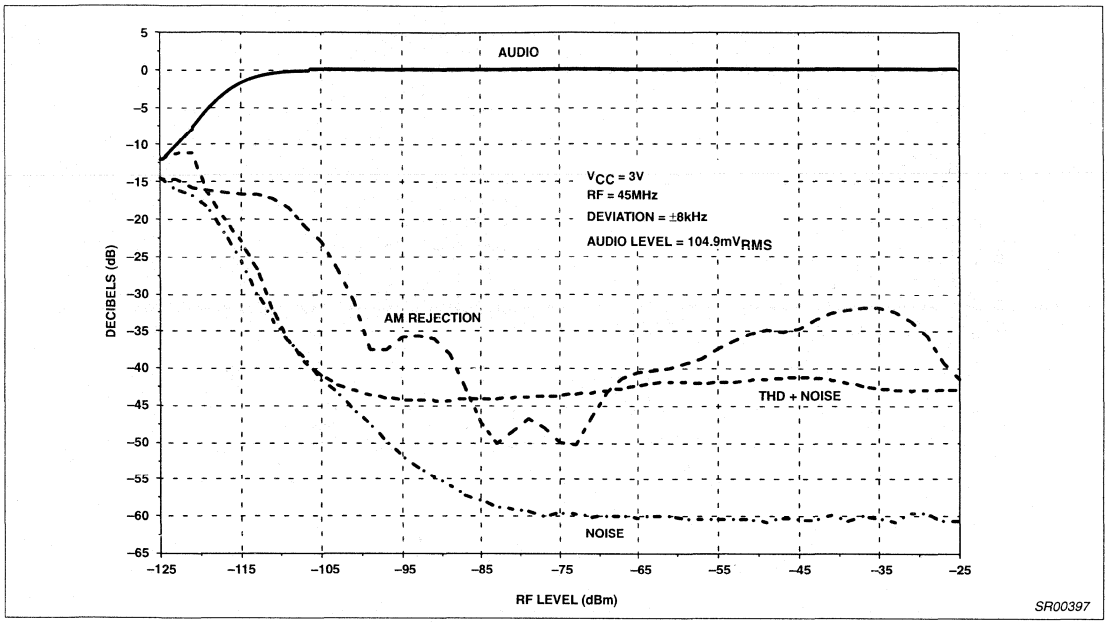


Figure 11. Sensitivity vs RF Level (–40°C)

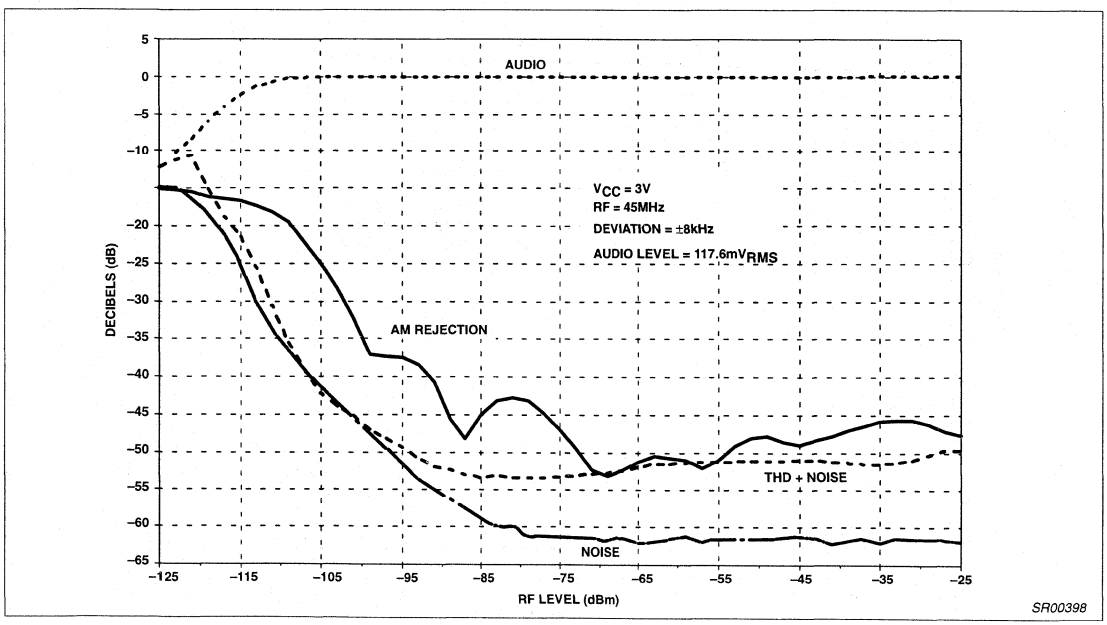


Figure 12. Sensitivity vs RF Level (+25°C)

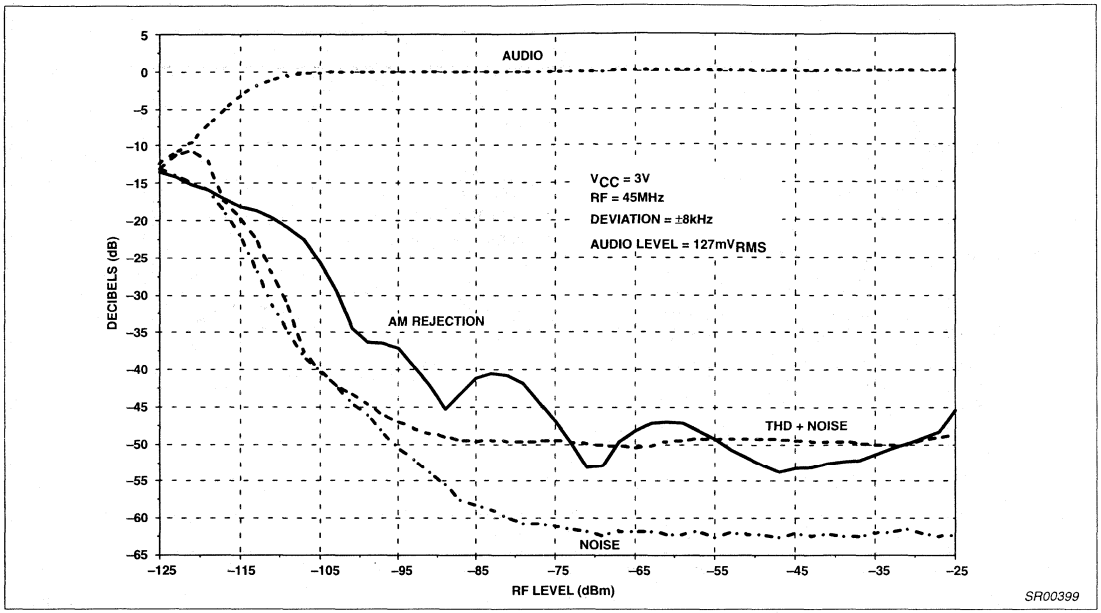


Figure 13. Sensitivity vs RF Level (Temperature 85°C)

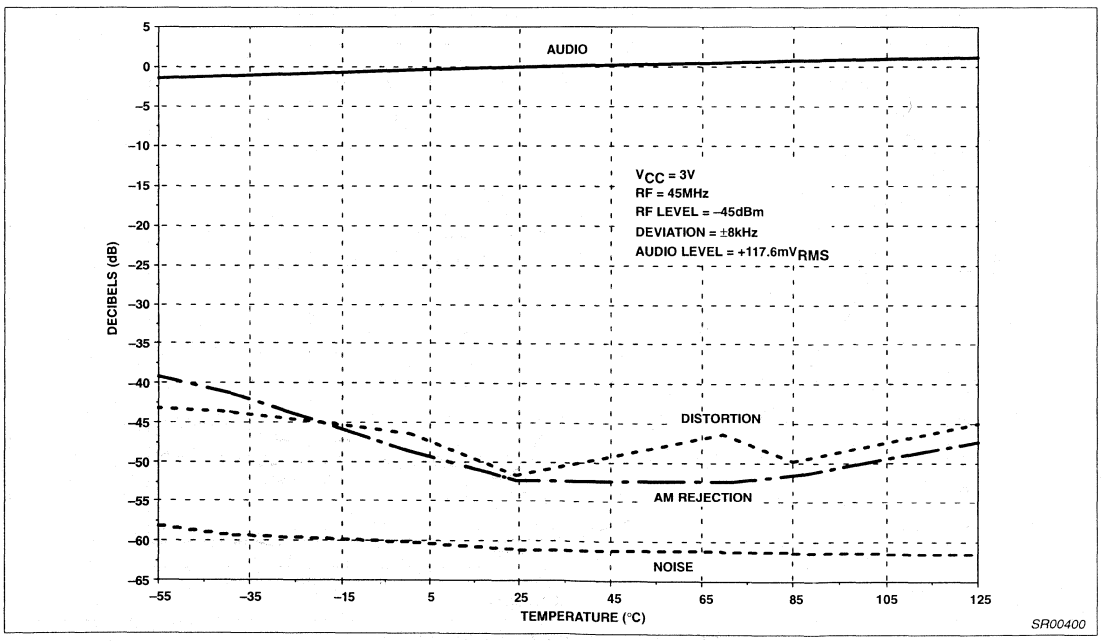


Figure 14. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

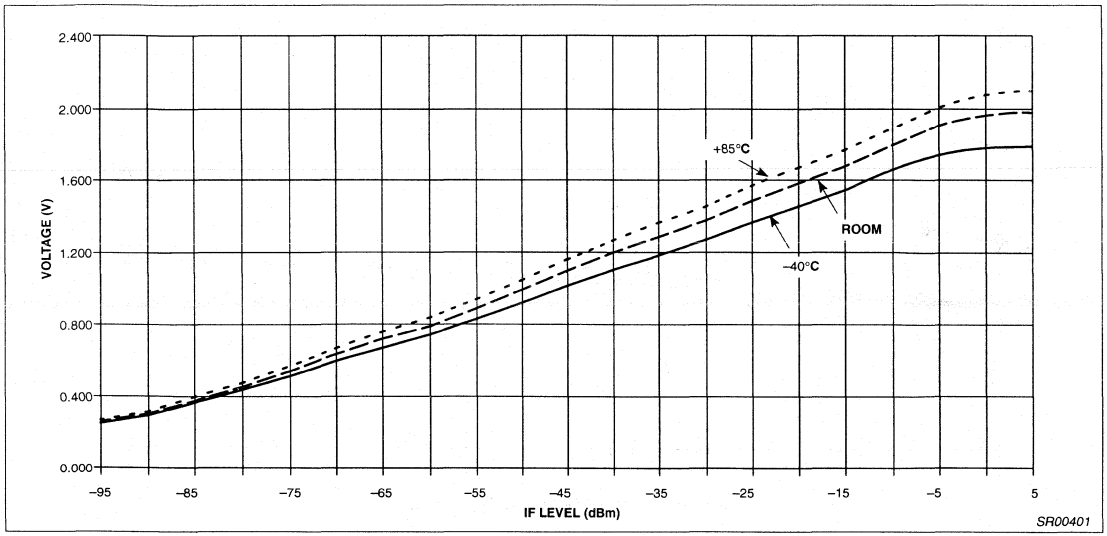


Figure 15. RSSI (455kHz IF @ 3V)

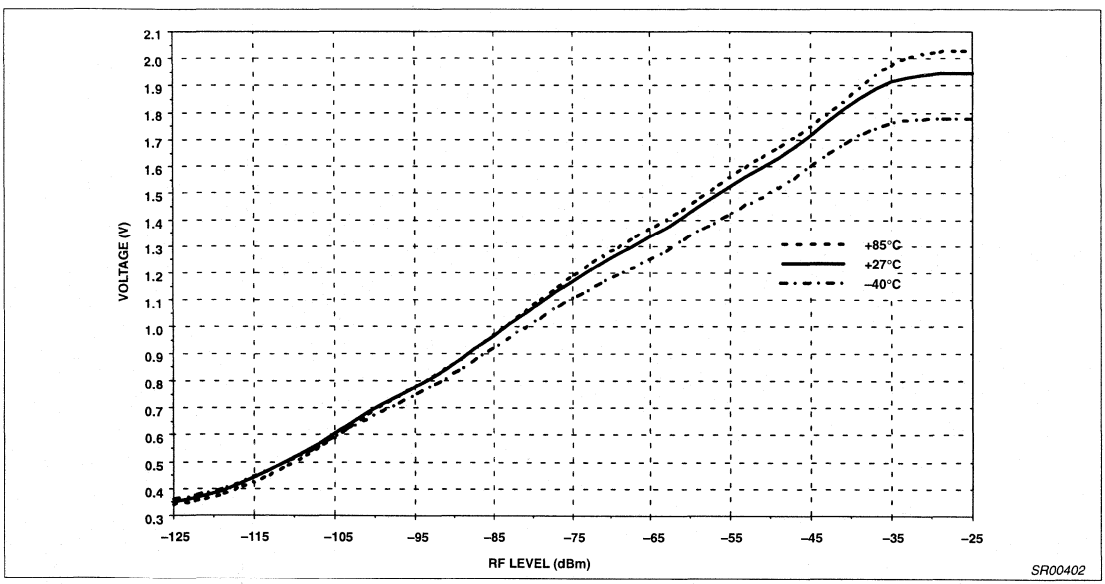


Figure 16. RSSI vs RF Level and Temperature - V_{CC} = 3V

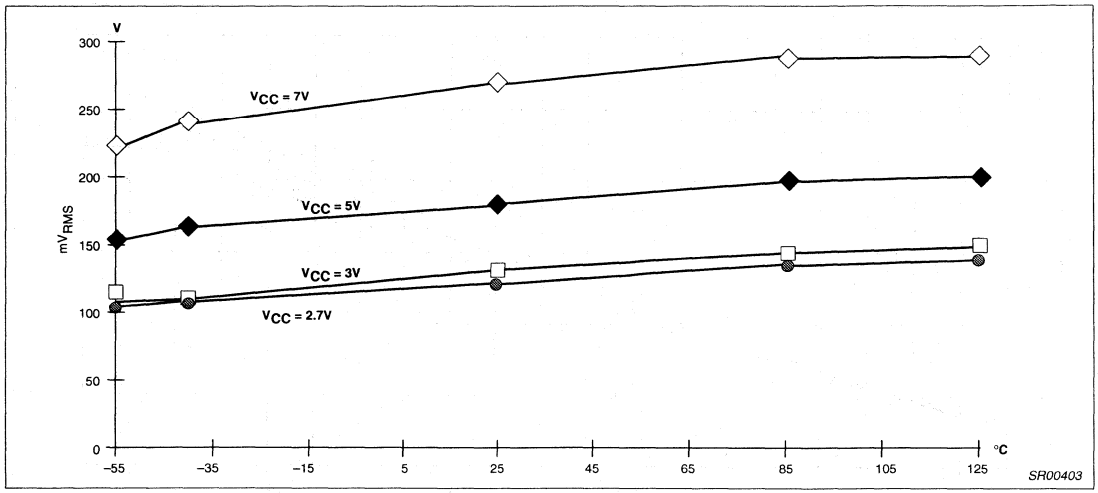
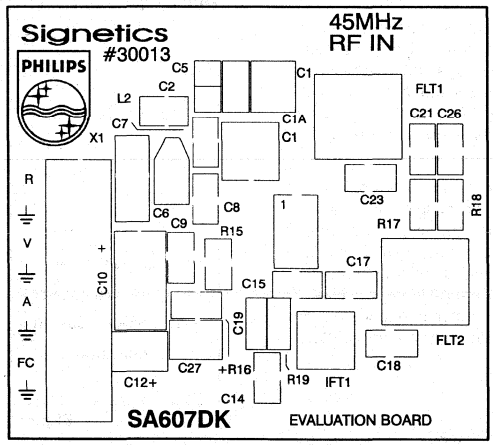
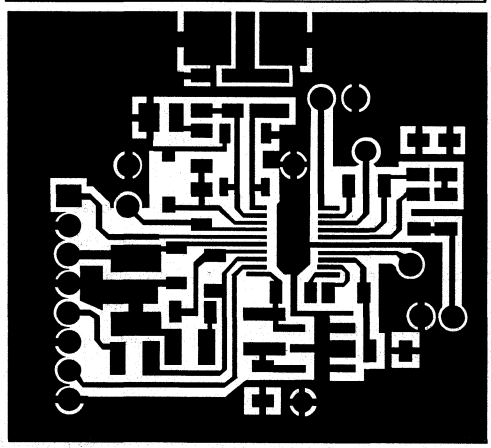


Figure 17. Audio Output vs Temperature

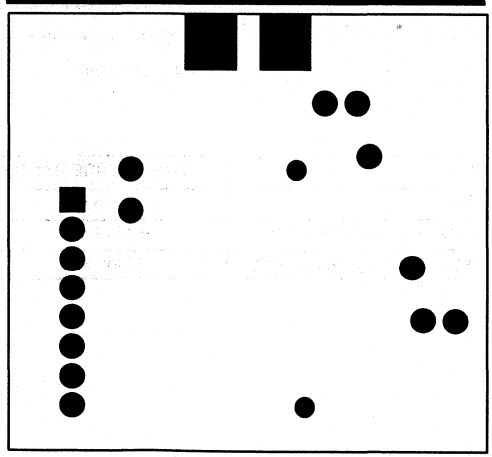
607 Silk Screen



607 TOP



607 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

SR00404

Figure 18.

Low-voltage high performance mixer FM IF system SA617

DESCRIPTION

The SA617 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA617 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA617 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The SA617 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA617 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output

PIN CONFIGURATION

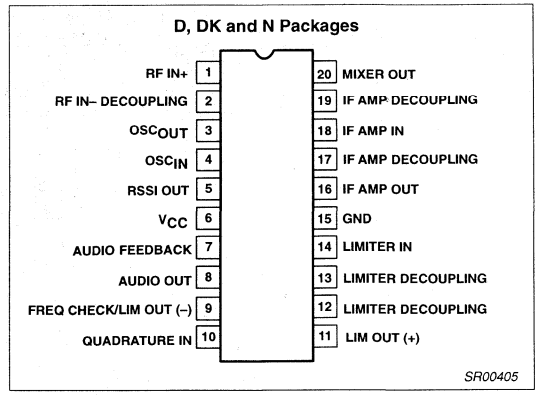


Figure 1. Pin Configuration

- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA617N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA617D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA617DK	SOT266-1

BLOCK DIAGRAM

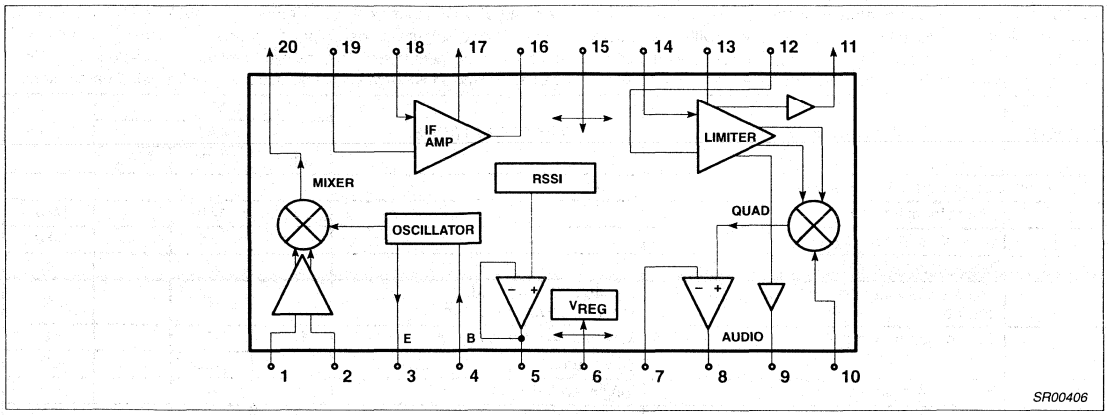


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range SA617	−40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA617			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

$T_A = 25^{\circ}C$; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA617 MIN	LIMITS SA617 TYP	LIMITS SA617 MAX	UNITS
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	11.0	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	114		mV
	SINAD sensitivity	RF level –110dB		13		dB
THD	Total harmonic distortion		–30	–45		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	2.0	V
		IF level = –23dBm	1.0	1.8	2.5	V
	RSSI range			80		dB
	RSSI accuracy			±2.0		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) No load 2.4kΩ load		130 115		mV$_{RMS}$
	Frequency Check/limiter output impedance	(Pin 9)		200		Ω
	Frequency Check/limiter output level	(Pin 9) No load 2.4kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		240		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA617 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA617 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA617 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

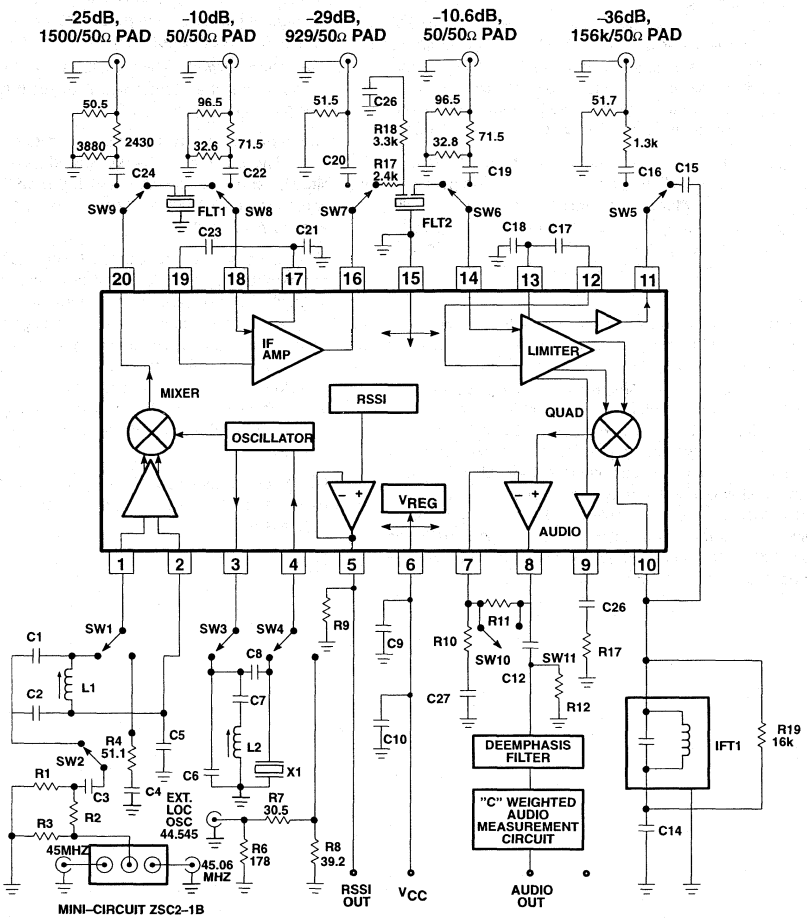
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 2kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter output or Frequency Check output has drive capability of a load minimum of 2kΩ or higher to obtain 115mV output level.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

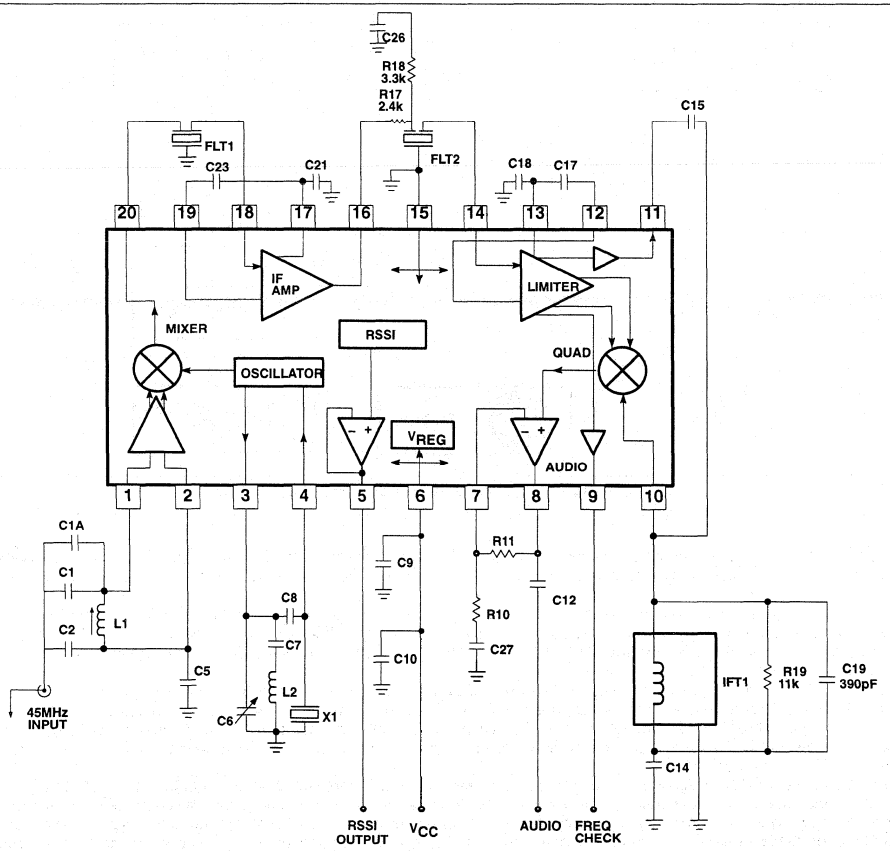


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	3.3μH nominal Toko 292CNS–T1046Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R12	2kΩ ±1%
R14	10kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

SR00407

Figure 3. SA617 45MHz Test Circuit (Relays as shown)



SA617DK
Application Component List

C1A	18pF NPO Ceramic
C1	33pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C12	2.2μF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2μF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330μH TOKO 303LN-1130
L1	.33μH TOKO SCB-1320Z
L2	1.2μH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

SR00408

Figure 4. SA617 45MHz Application Circuit

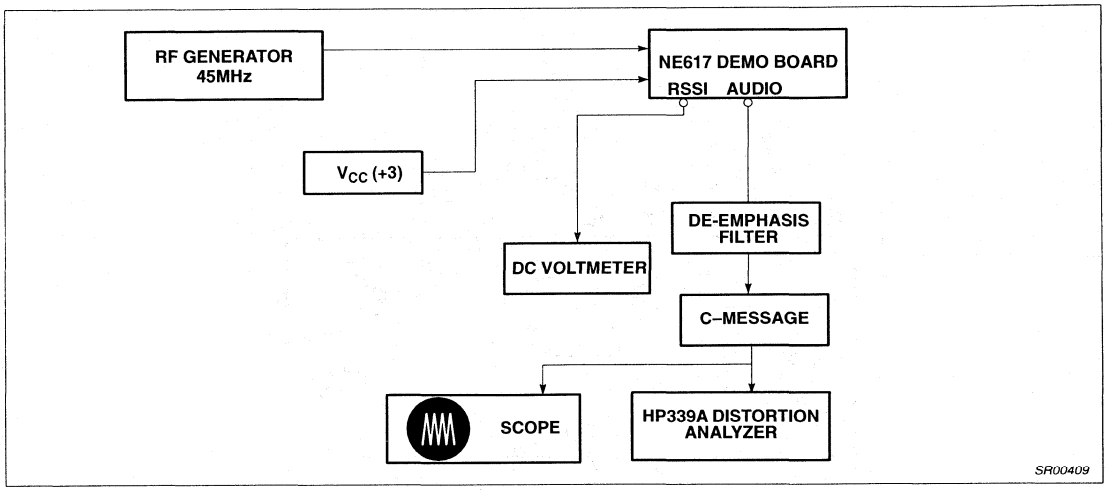


Figure 5. SA617 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

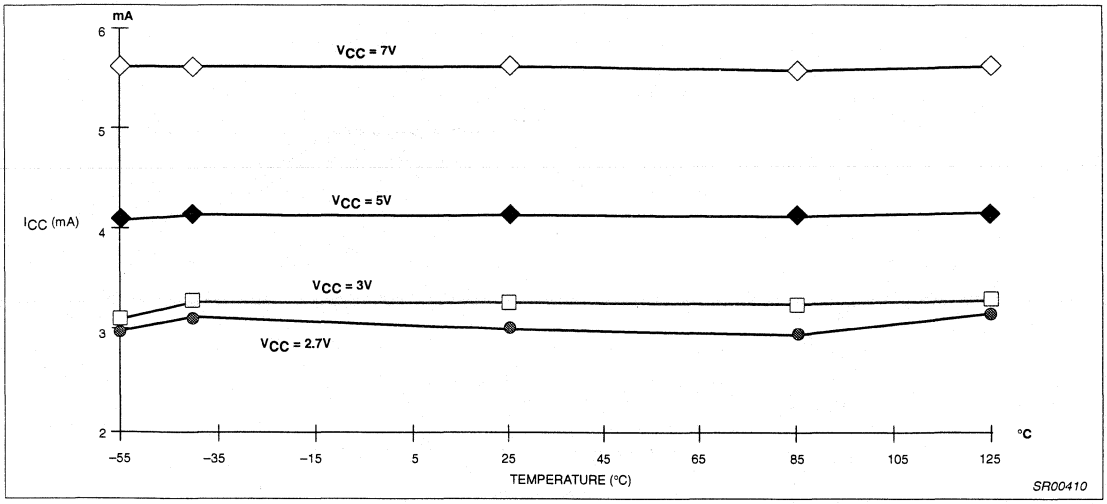


Figure 6. I_{CC} vs Temperature

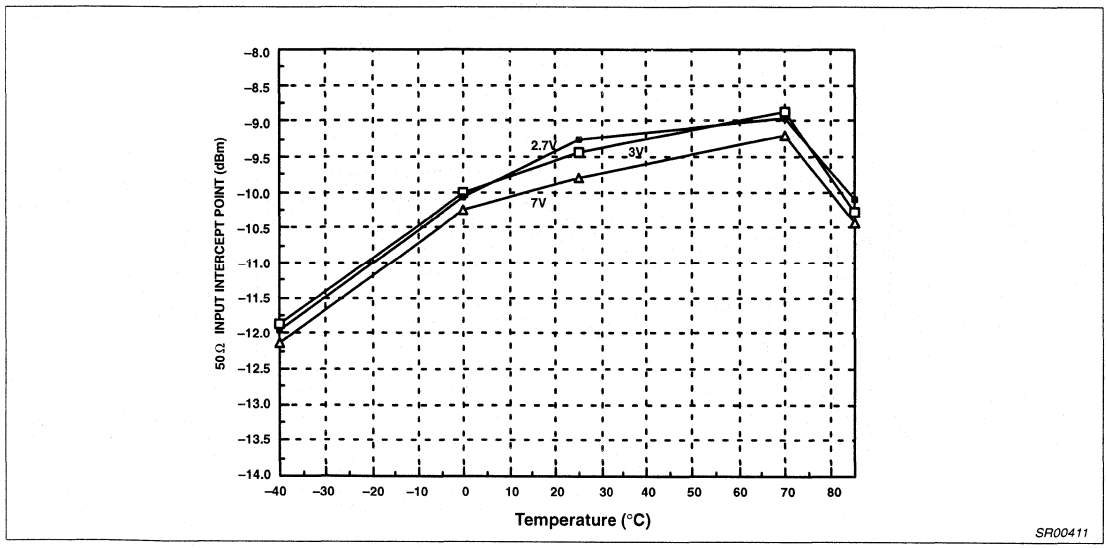


Figure 7. Third Order Intercept Point vs Supply Voltage

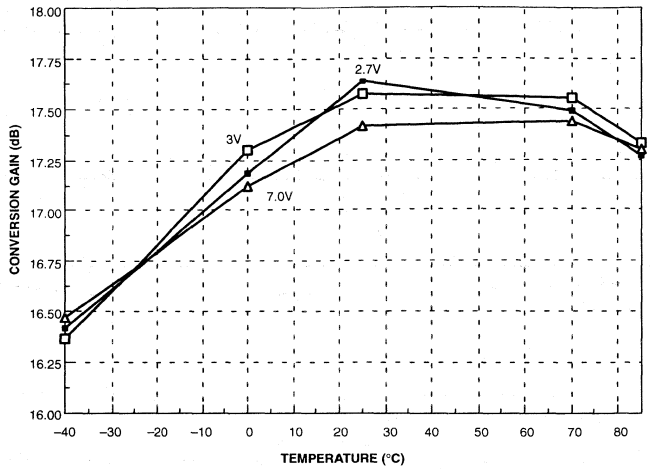


Figure 8. Mixer Noise Figure vs Supply Voltage

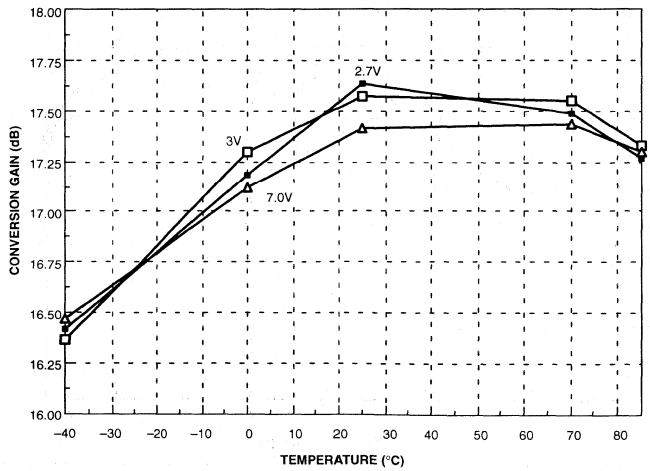


Figure 9. Conversion Gain vs Supply Voltage

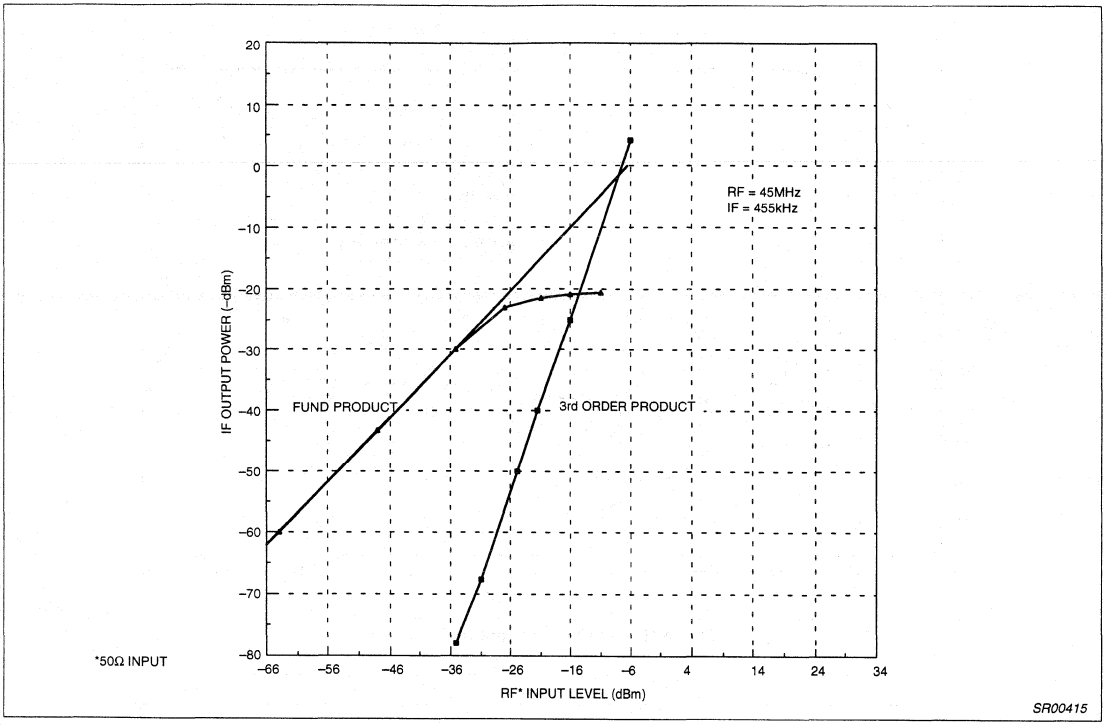


Figure 10. Mixer Third Order Intercept and Compression

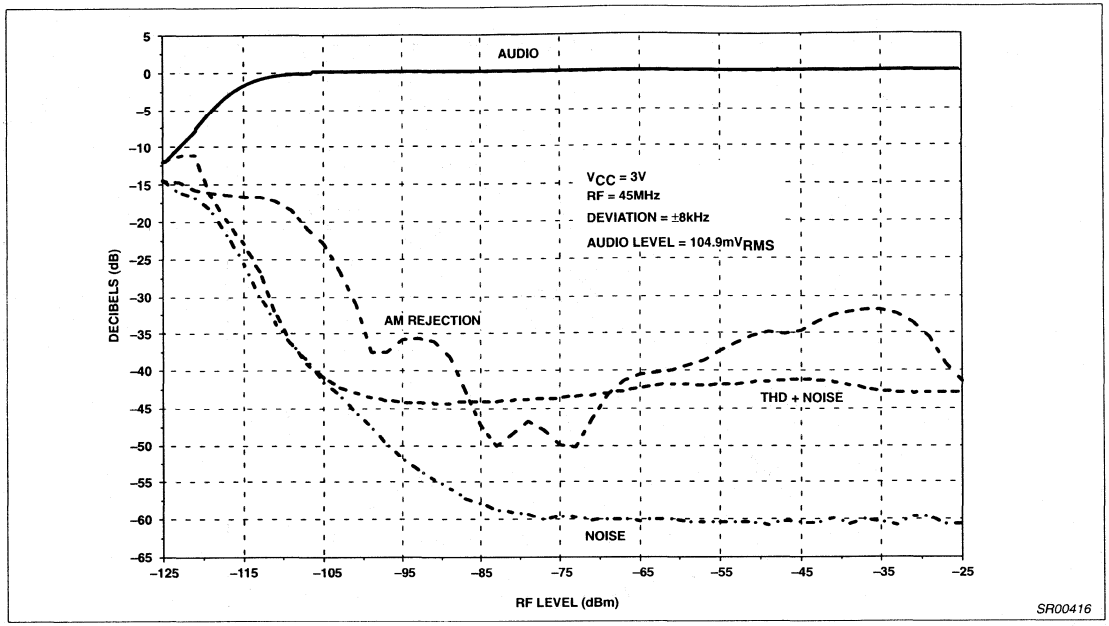


Figure 11. Sensitivity vs RF Level (–40°C)

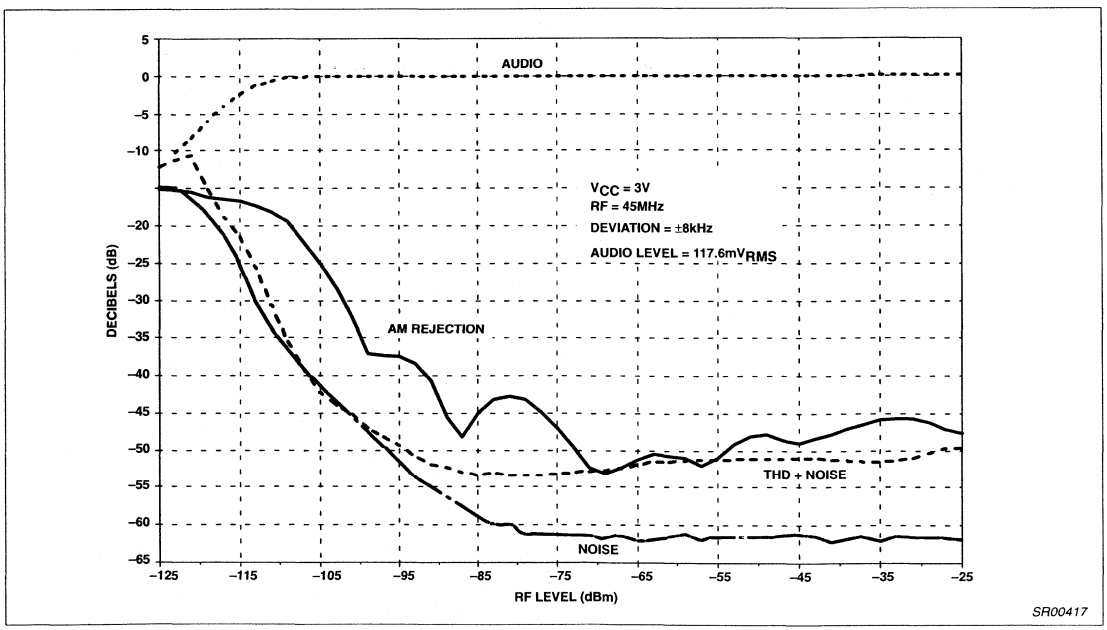


Figure 12. Sensitivity vs RF Level (+25°C)

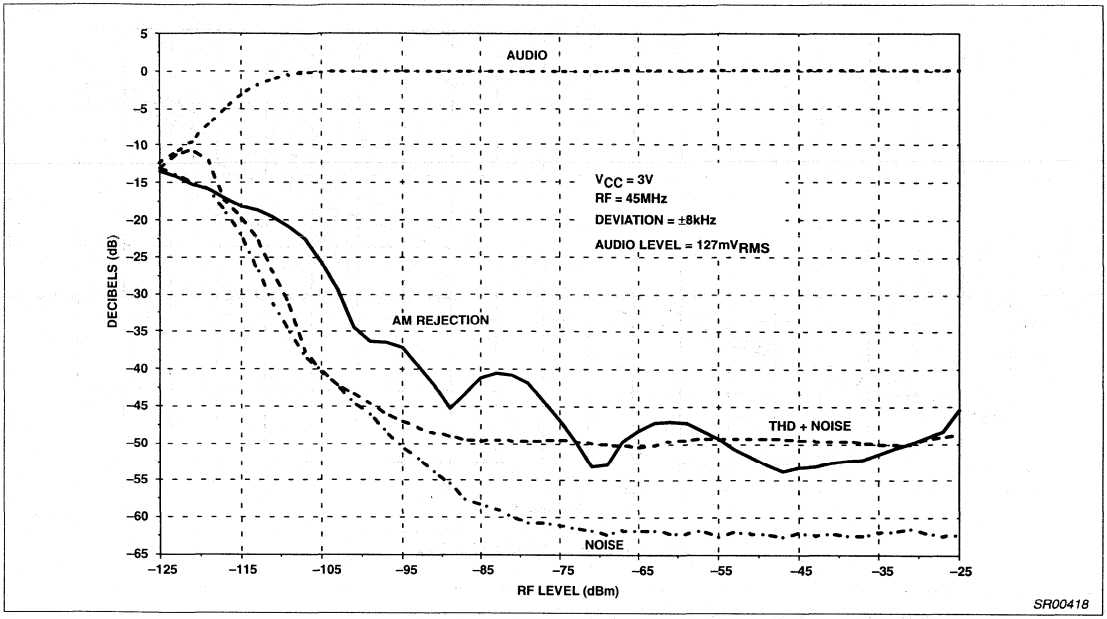


Figure 13. Sensitivity vs RF Level (Temperature 85°C)

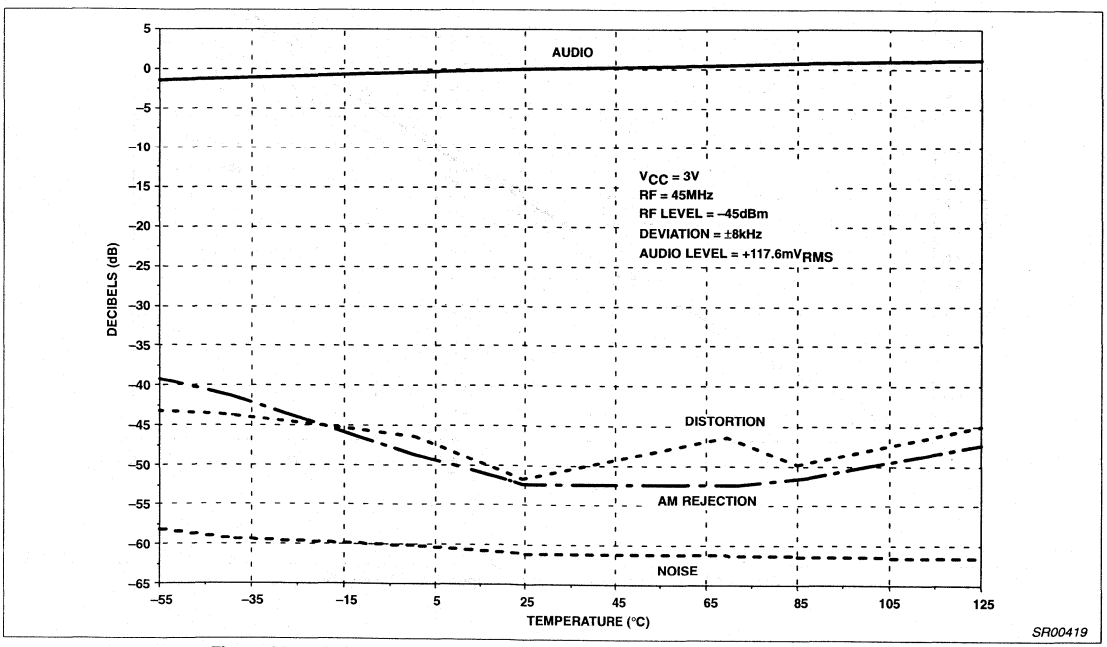


Figure 14. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

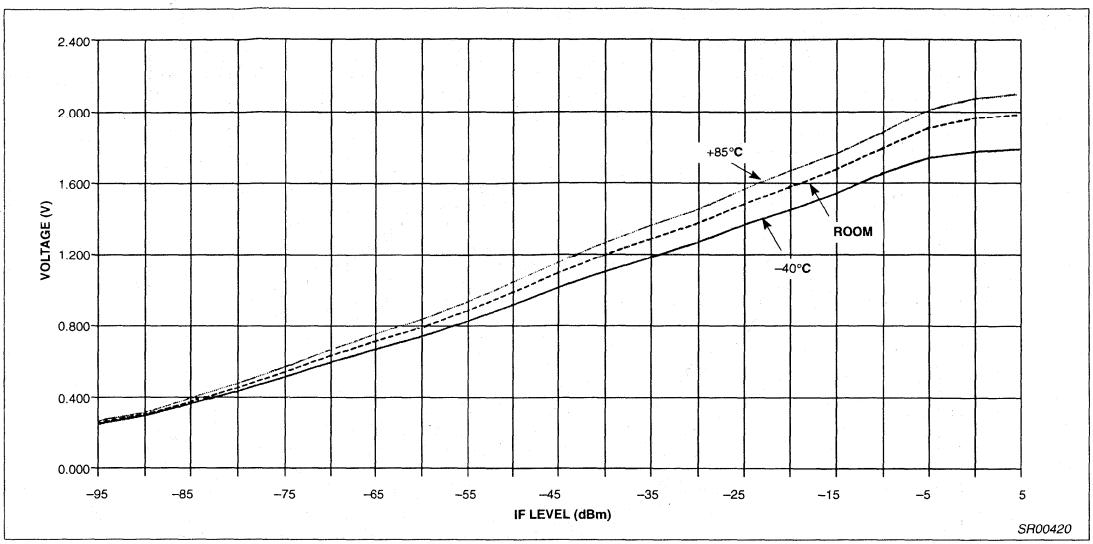


Figure 15. RSSI (455kHz IF @ 3V)

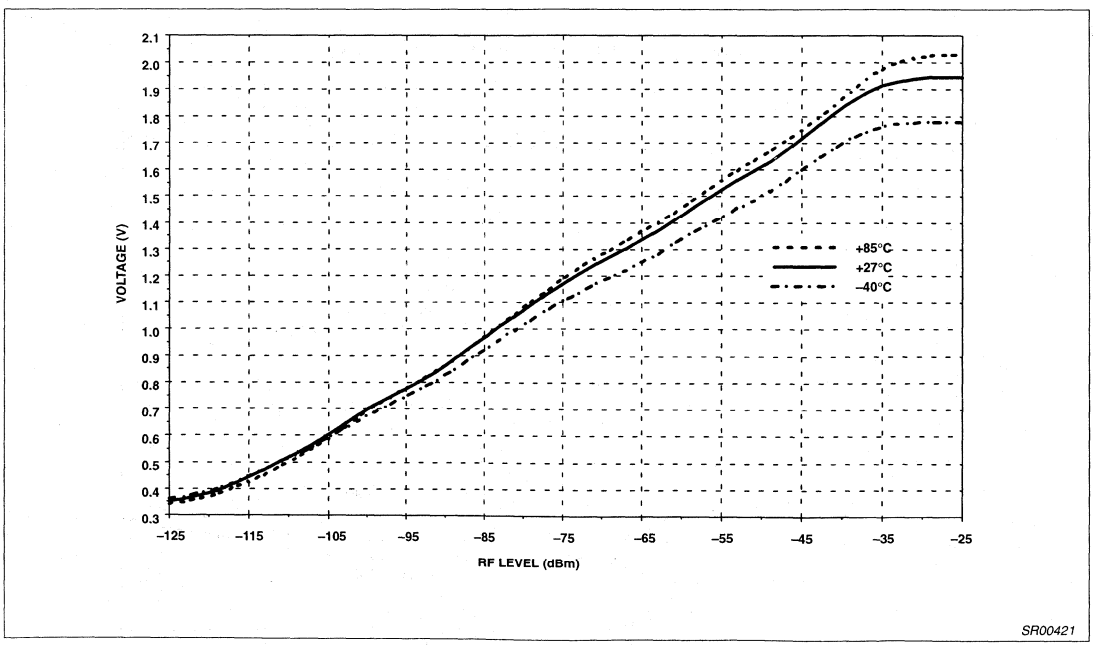


Figure 16. RSSI vs RF Level and Temperature - V_{CC} = 3V

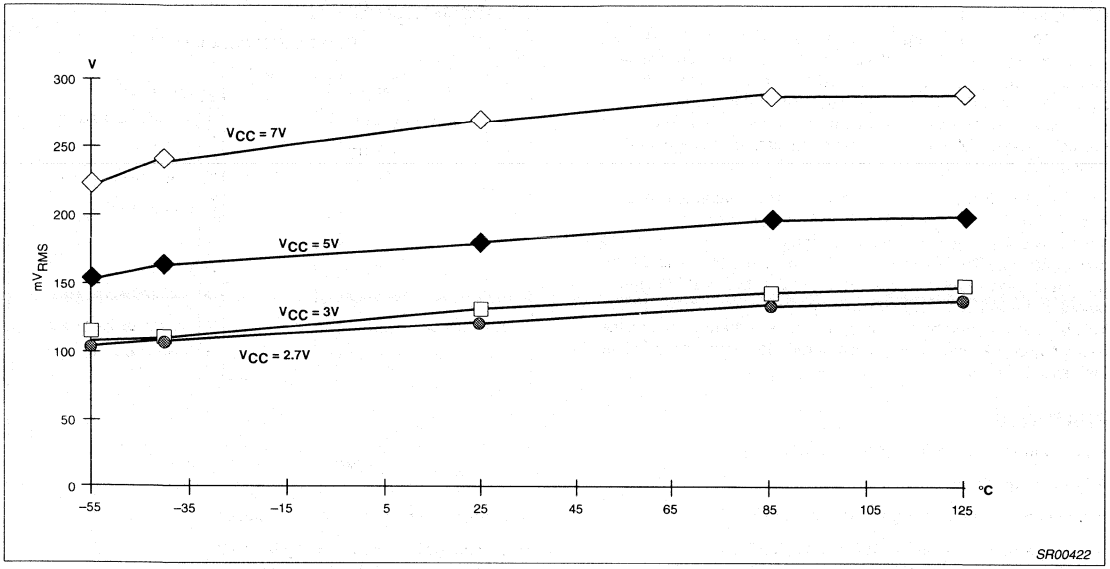


Figure 17. Audio Output vs Temperature

Low voltage high performance mixer FM IF system SA608

DESCRIPTION

The SA608 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA608 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA608 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output is buffered. The RSSI output has an internal amplifier with the feedback pin accessible. The SA608 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA608 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output

PIN CONFIGURATION

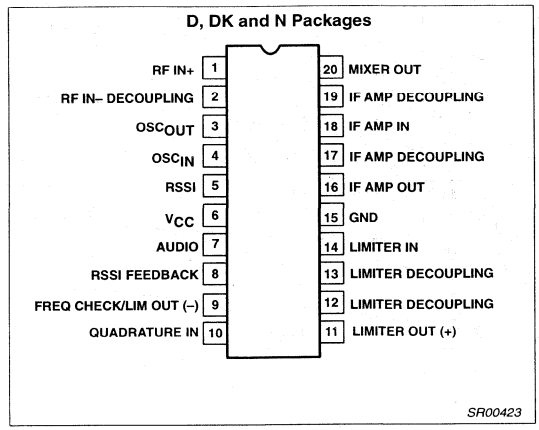


Figure 1. Pin Configuration

- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA608N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA608D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA608DK	SOT266-1

BLOCK DIAGRAM

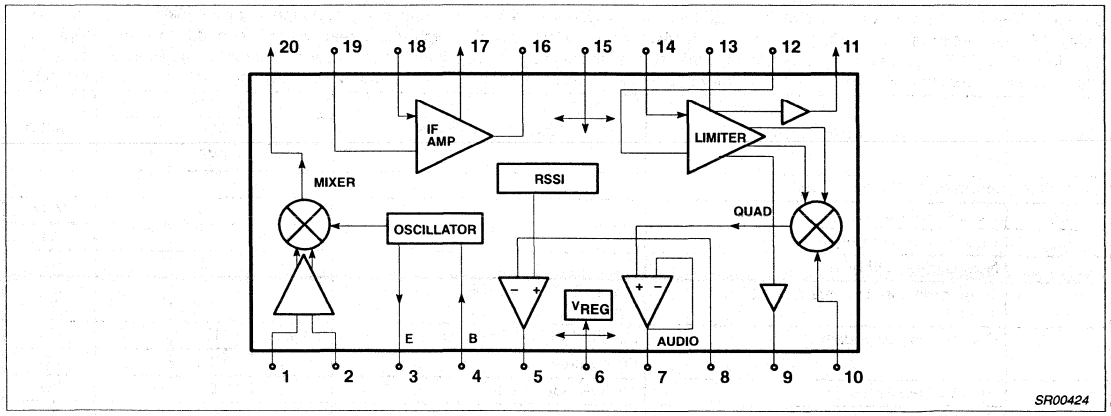


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA608	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA608			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA608 MIN	LIMITS SA608 TYP	LIMITS SA608 MAX	UNITS
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level[2]		35	60	80	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) no load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/lim (–) output impedance	(Pin 9)		200		Ω
	Frequency check/lim (–) output level	(Pin 9) no load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA608 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA608 input (Pin 18) which is about 21dB less than the "available power" at the generator.
2. By using 45kΩ load across the Quad detector coil, you will have Audio output at 115mV with –42dB distortion.

CIRCUIT DESCRIPTION

The SA608 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

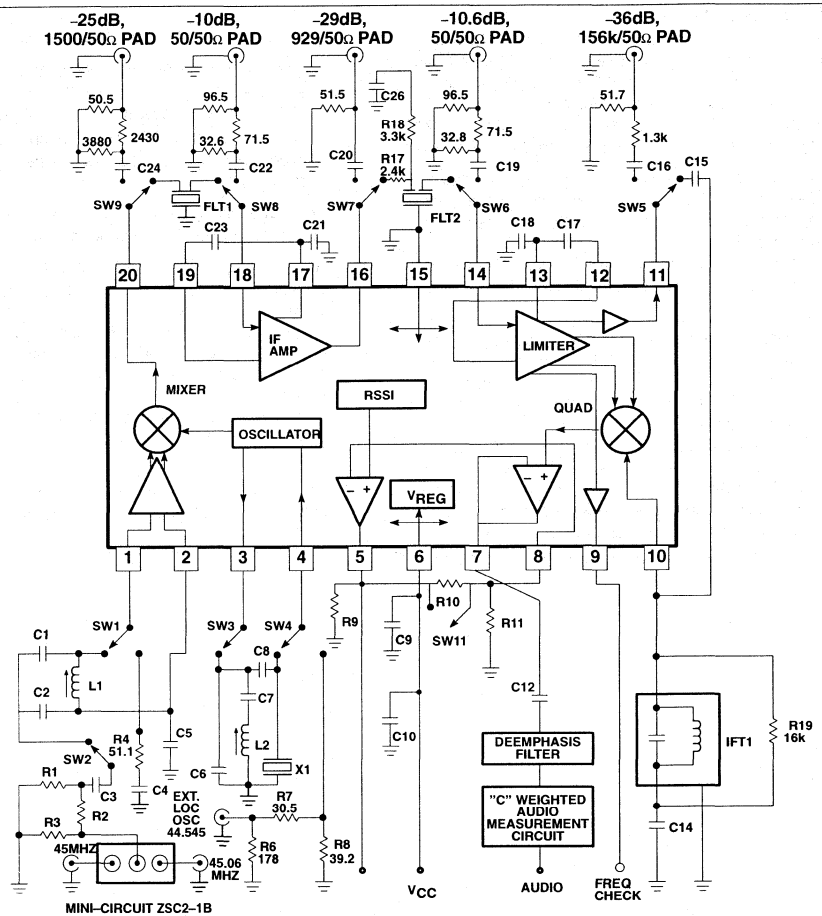
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp is configured as a unity gain buffer.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter or Frequency Check output has drive capability of a 5kΩ minimum or higher in order to obtain $120mV_{RMS}$ output level.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



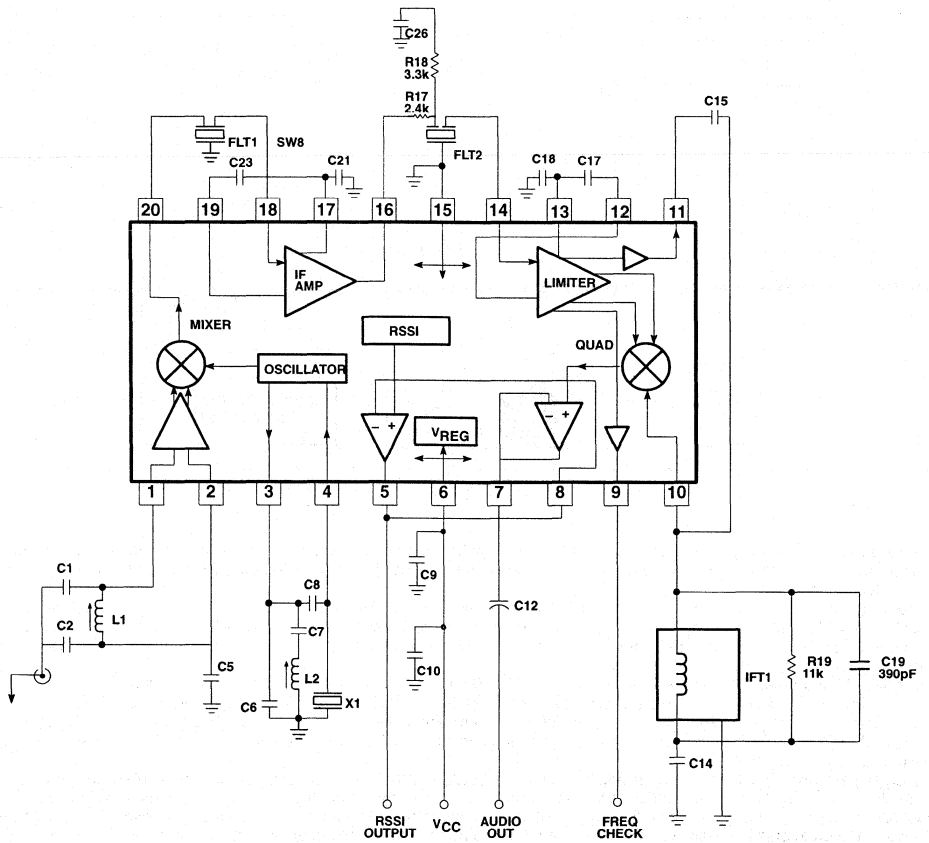
Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147–160nH Coilcraft UNI-10/142-04J08S
L2	0.8μH nominal Toko 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	10kΩ ±1%
R11	10kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

SR00425

Figure 3. SA607 45MHz Test Circuit (Relays as shown)



Product Board SA608D/DK Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330μH TOKO 303LN–1130
L1	0.33μH TOKO SCB–1320Z
L2	1.2μH Coilcraft 1008CS–122
X1	44.545MHz Crystal Hy-Q
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R14	10kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

SR00426

Figure 4. SA608 45MHz Test Circuit (Relays as shown)

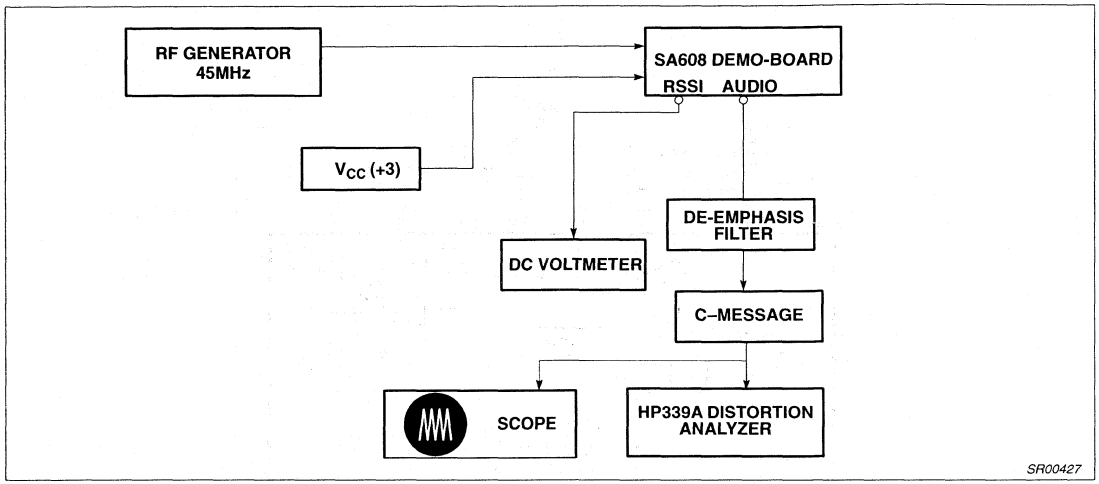


Figure 5. SA608 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

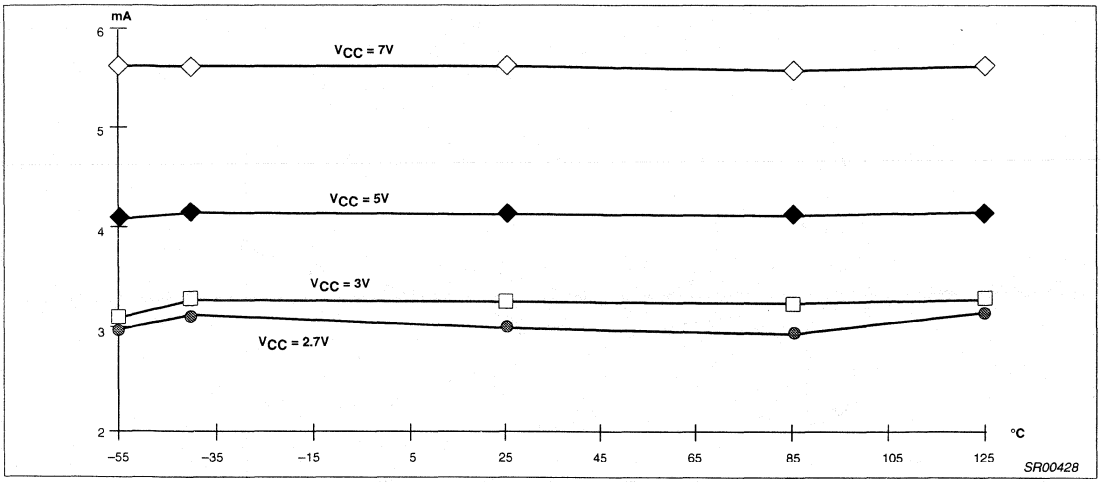


Figure 6. I_{CC} vs Temperature

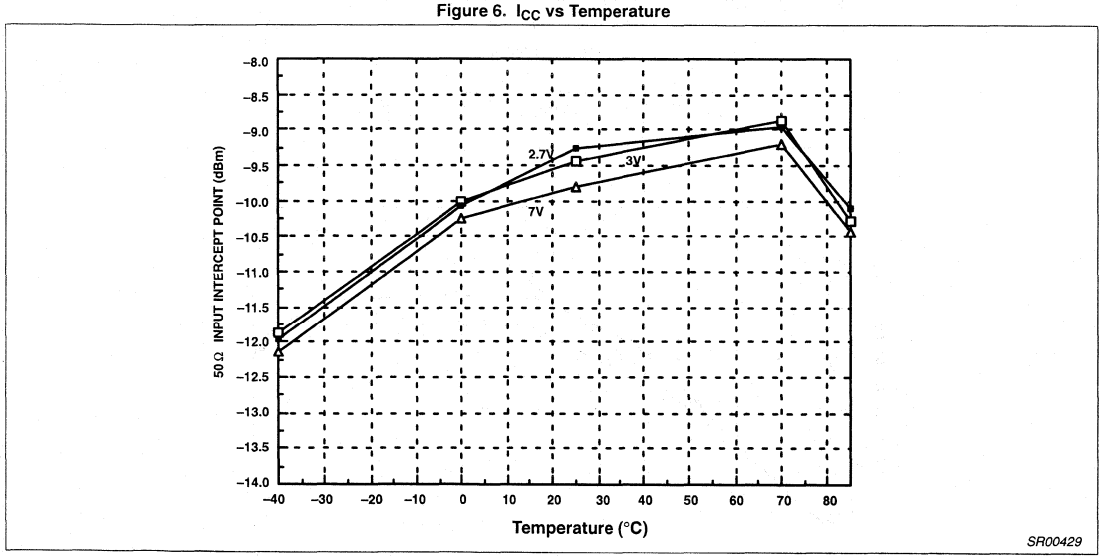


Figure 7. Third Order Intercept Point vs Supply Voltage

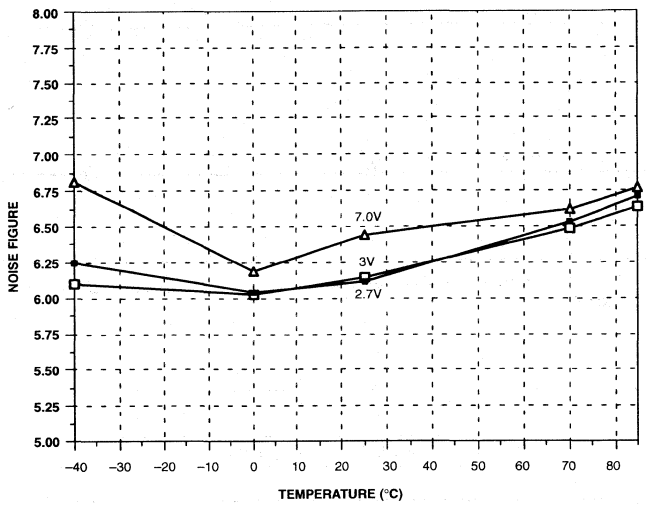


Figure 8. Mixer Noise Figure vs Supply Voltage

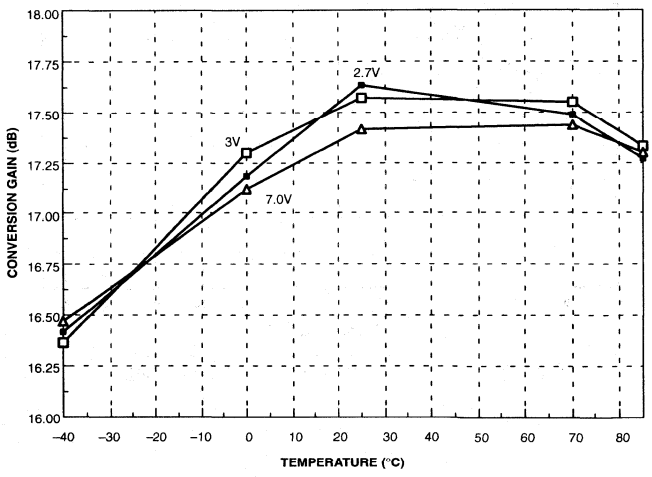


Figure 9. Conversion Gain vs Supply Voltage

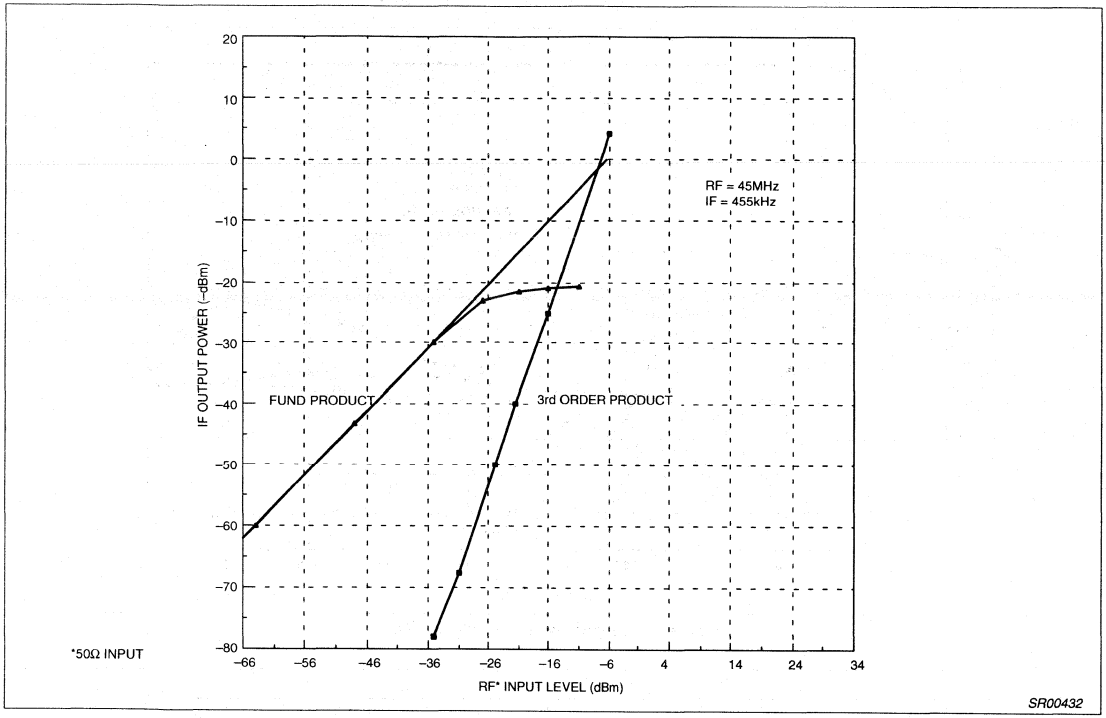


Figure 10. Mixer Third Order Intercept and Compression

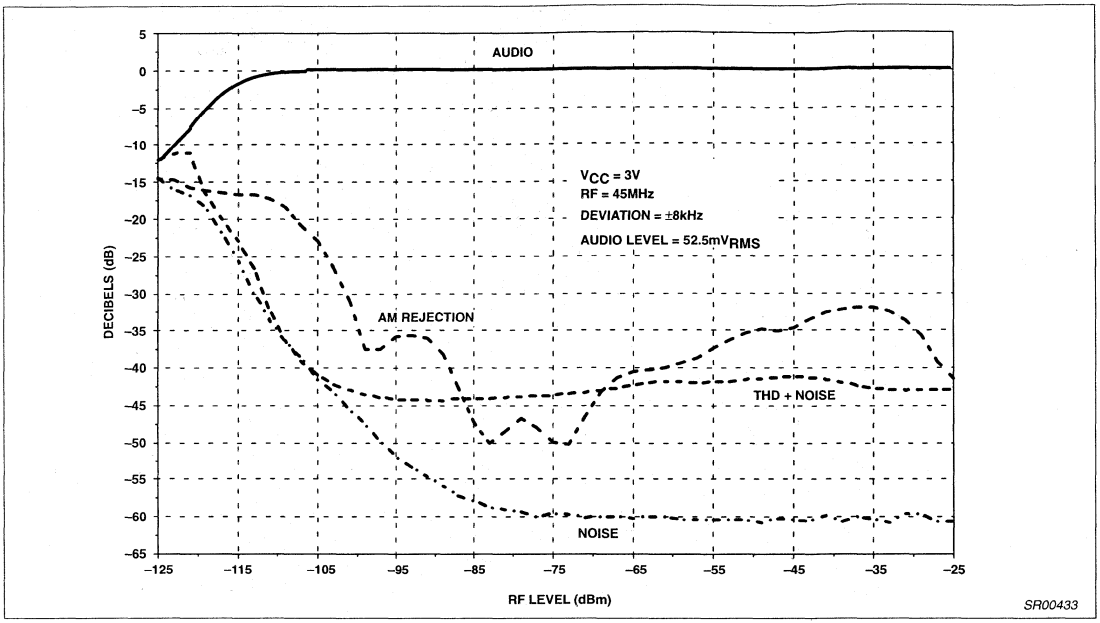


Figure 11. Sensitivity vs RF Level (–40°C)

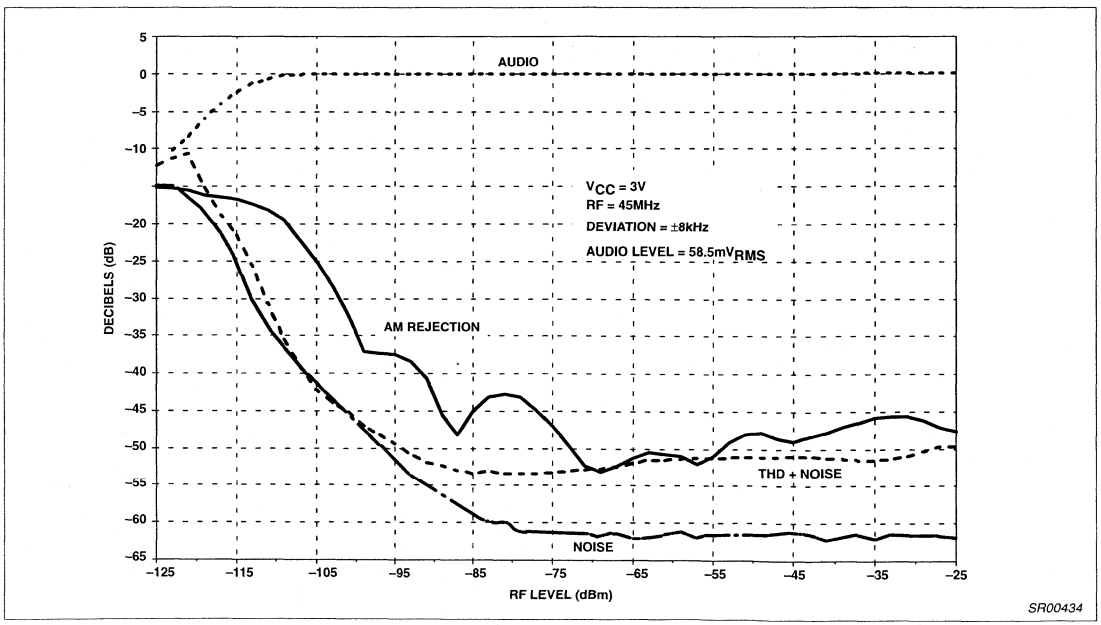


Figure 12. Sensitivity vs RF Level (+25°C)

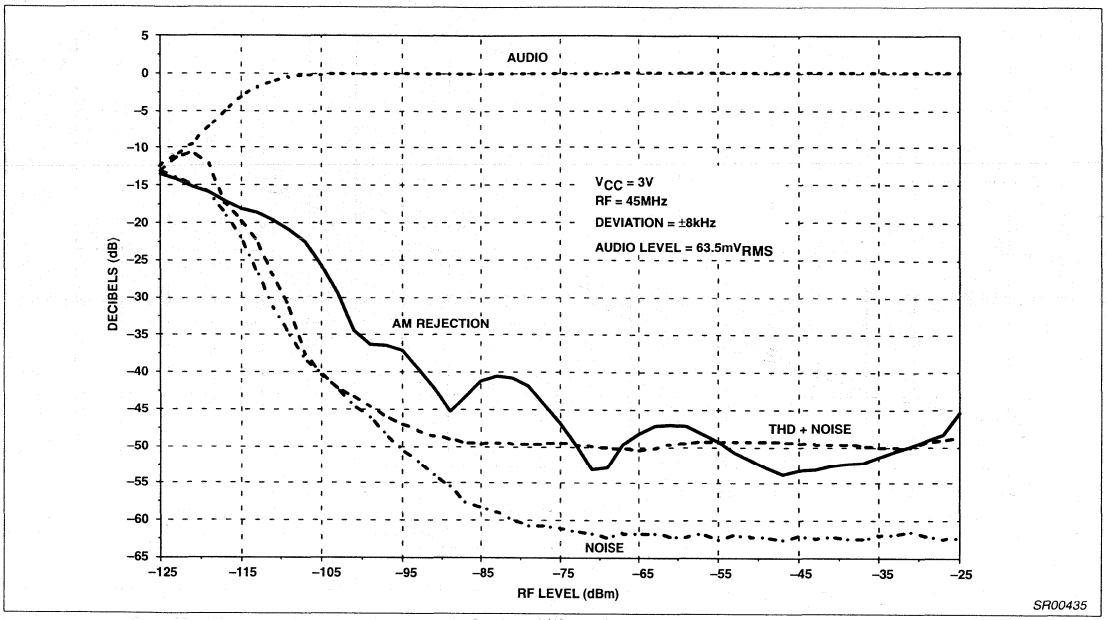


Figure 13. Sensitivity vs RF Level (Temperature 85°C)

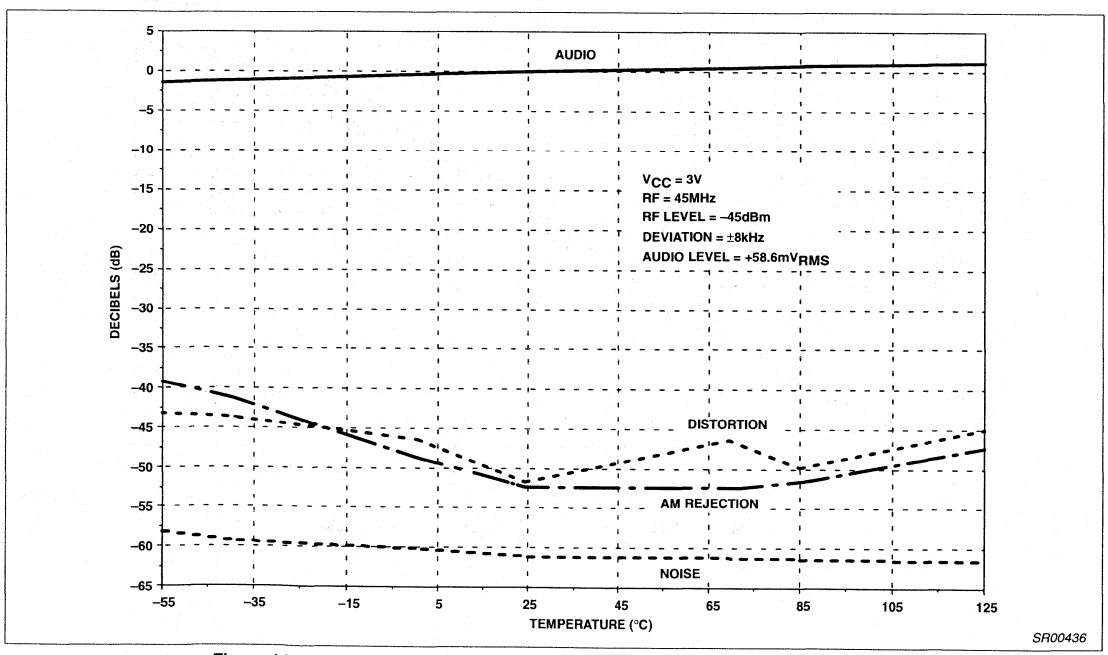


Figure 14. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

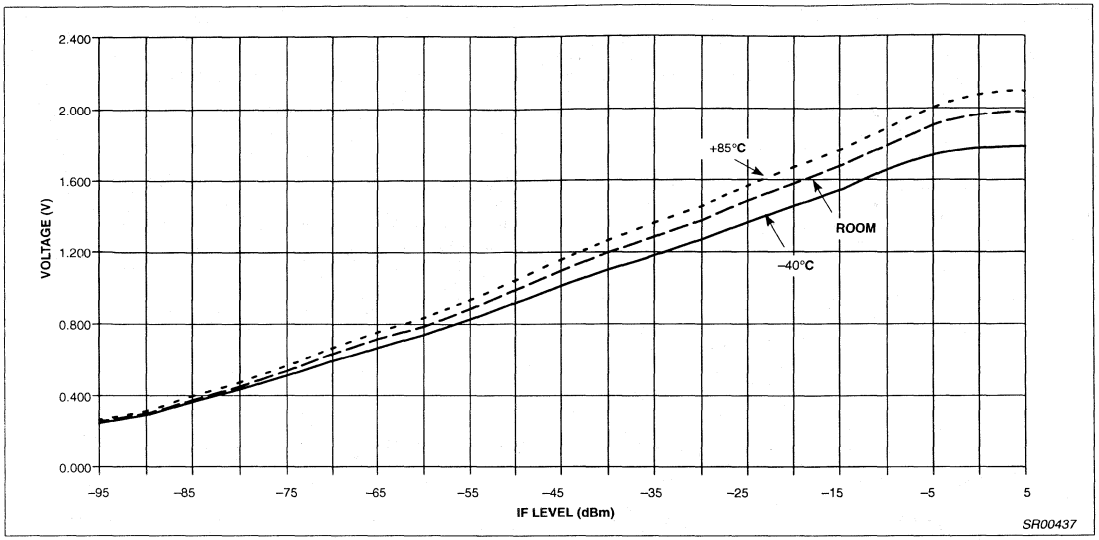


Figure 15. RSSI (455kHz IF @ 3V)

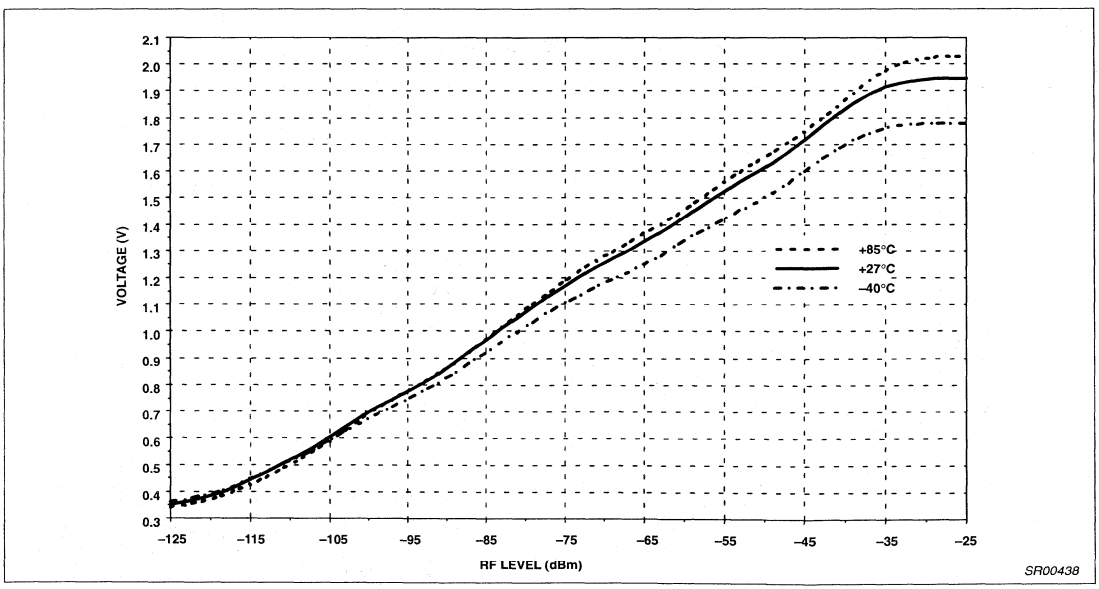


Figure 16. RSSI vs RF Level and Temperature - V_{CC} = 3V

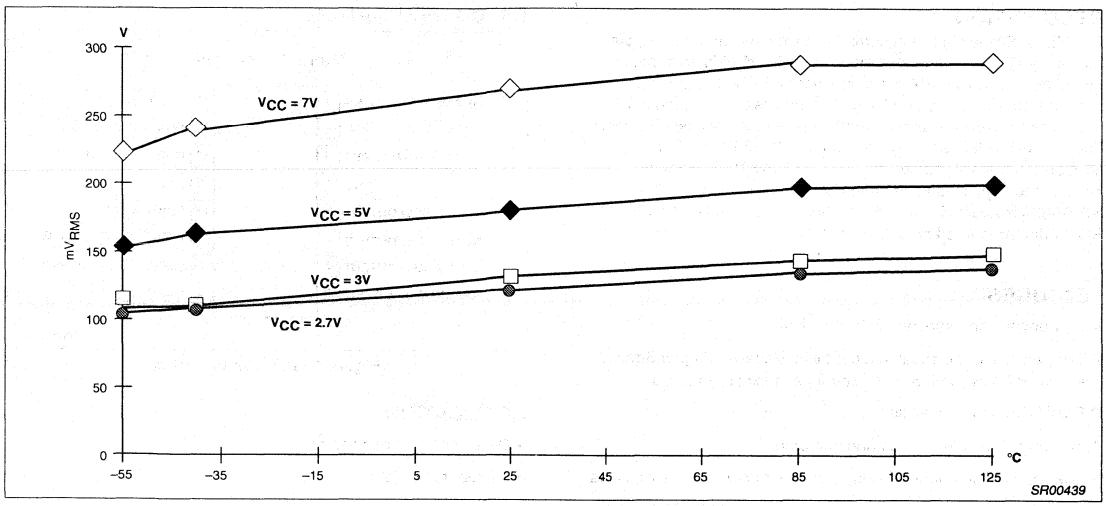


Figure 17. Audio Output vs Temperature

High performance low power FM IF system with high-speed RSSI

NE/SA624

DESCRIPTION

The NE/SA624 is pin-to-pin compatible with the NE/SA604A, but has faster RSSI rise and fall time. The NE/SA624 is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA624 features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA624 is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.4mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Fast RSSI rise and fall time
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA624 meets cellular radio specifications

PIN CONFIGURATION

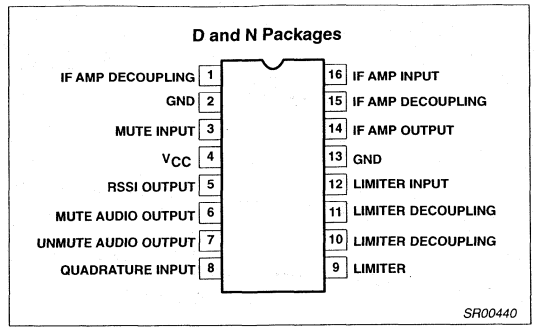


Figure 1. Pin Configuration

APPLICATIONS

- Digital cellular base station
- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE624N	SOT38-4
16-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to +70°C	NE624D	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA624N	SOT38-4
16-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA624D	SOT109-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE624 SA624	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

BLOCK DIAGRAM

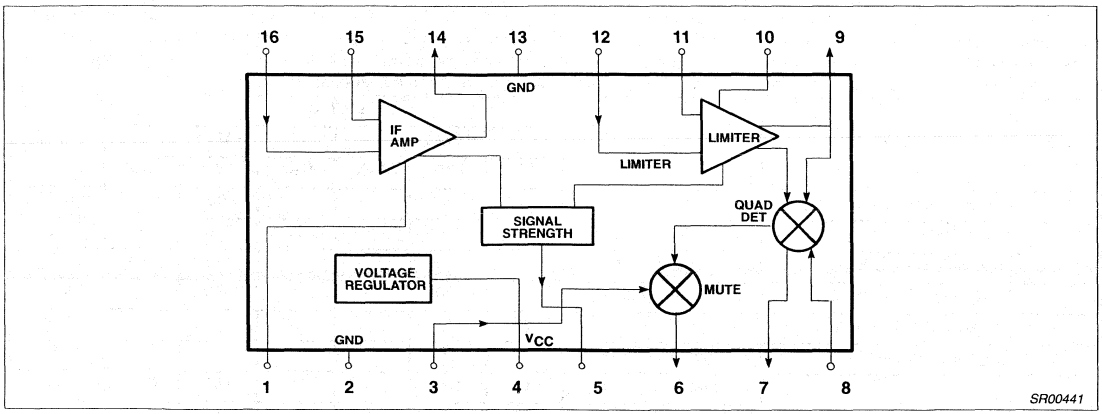


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE624			SA624			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.4	4.2	2.5	3.4	4.2	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

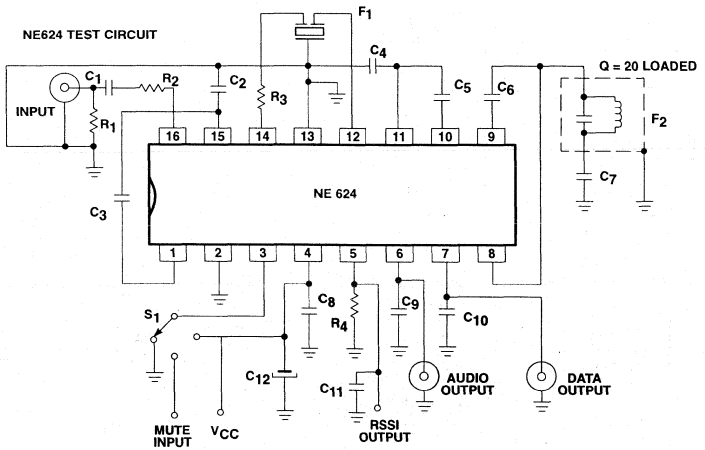
Typical reading at $T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE624			SA624			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92			-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530			530		mV_{RMS}
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = -118dBm	0	160	550	0	160	650	mV
		RF level = -68dBm	2.0	2.65	3.0	1.9	2.65	3.1	V
		RF level = -18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI output rise time (10kHz pulse, no IF filter)	IF freq. = 455kHz							
		IF level = -44dBm		1.1			1.1		µs
		IF level = -16dBm		1.2			1.2		µs
		IF freq. = 10.7MHz							
		IF level = -44dBm		1.2			1.2		µs
		IF level = -16dBm		1.1			1.1		µs
	RSSI output fall time (10kHz pulse, no IF filter)	IF freq. = 455kHz							
		IF level = -44dBm		1.3			1.3		µs
		IF level = -16dBm		4.7			4.7		µs
		IF freq. = 10.7MHz							
		IF level = -44dBm		1.6			1.6		µs
		IF level = -16dBm		4.2			4.2		µs
	RSSI range	R_4 = 100k (Pin 5)		90			90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Limiter output impedance			300			300		Ω
	Limiter output level no load			280			280		mV_{RMS}
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

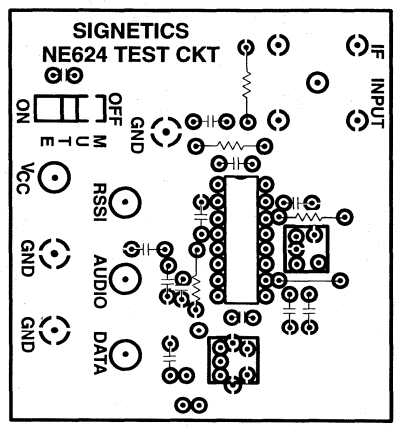
NOTE:

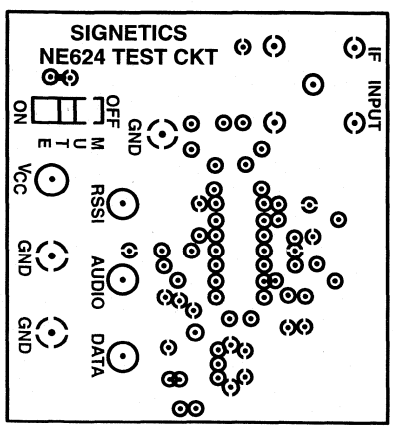
1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE604 (50)	NE624 (1.5k)/NE605 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





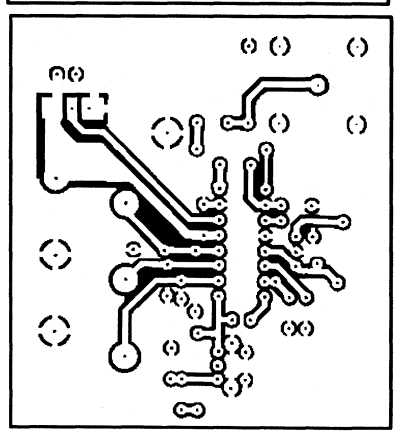


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Figure 3. NE/SA624 Test Circuit

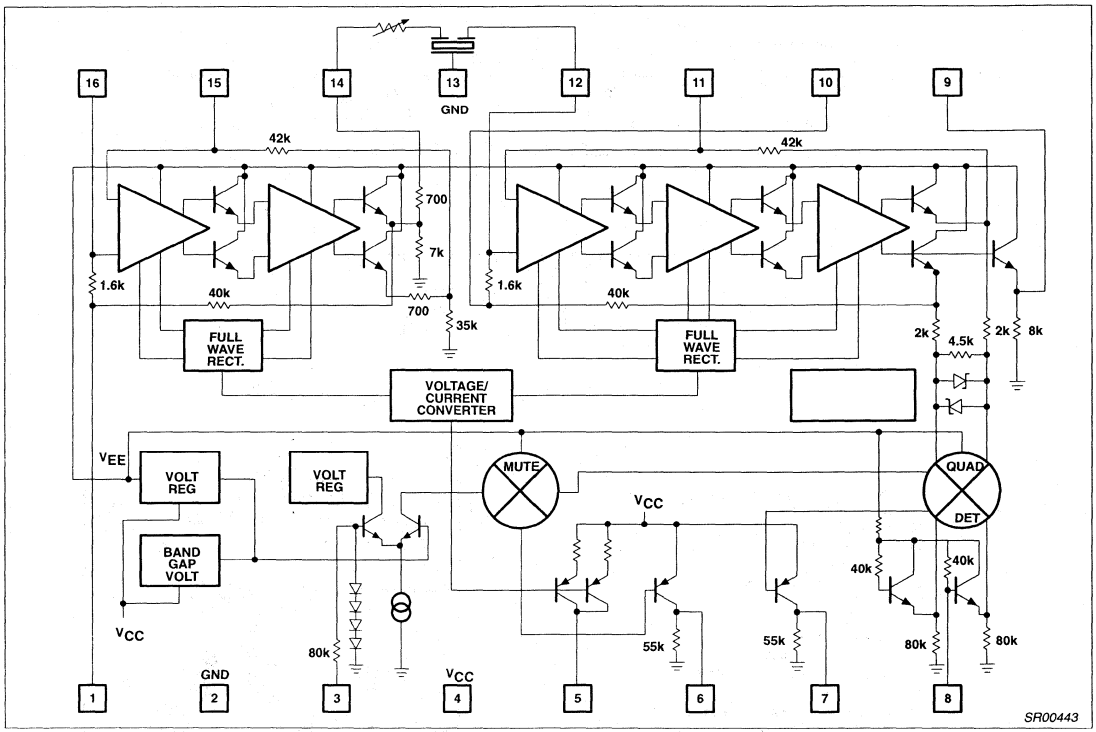


Figure 4. Equivalent Circuit

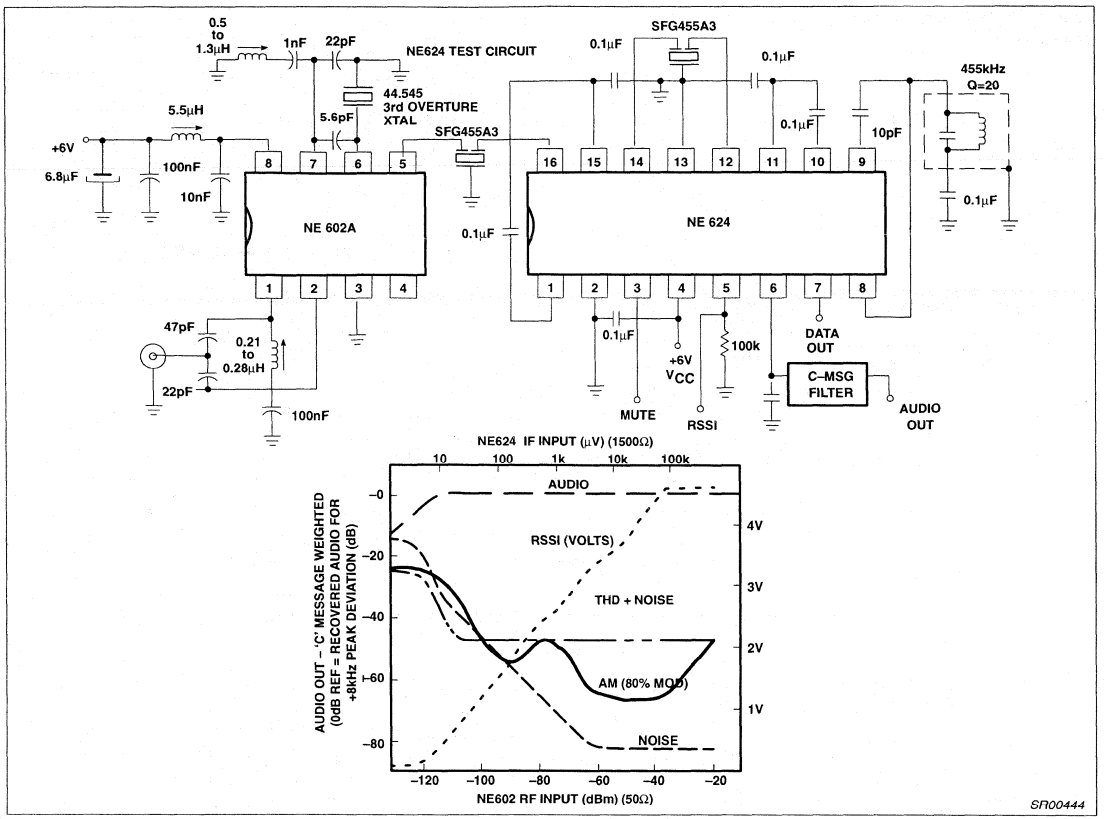


Figure 5. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA624 is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA624 cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 3. This configuration can be used as the basis for production layout.

The NE/SA624 is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 4. A typical application with 45MHz input and 455kHz IF is shown in Figure 5.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 4, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

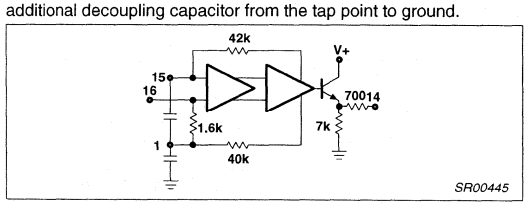


Figure 6. First Limiter Bias

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in

Figure 8. Distributed feedback (capacitance, inductance and radiated fields)

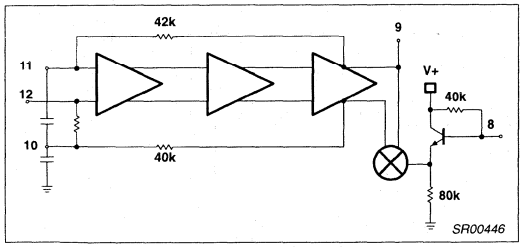


Figure 7. Second Limiter and Quadrature Detector

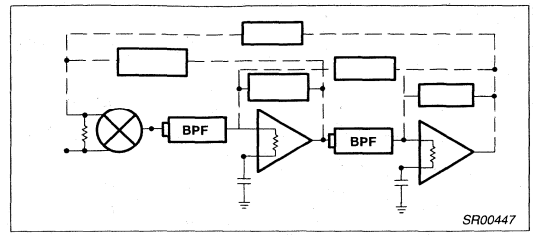


Figure 8. Feedback Paths

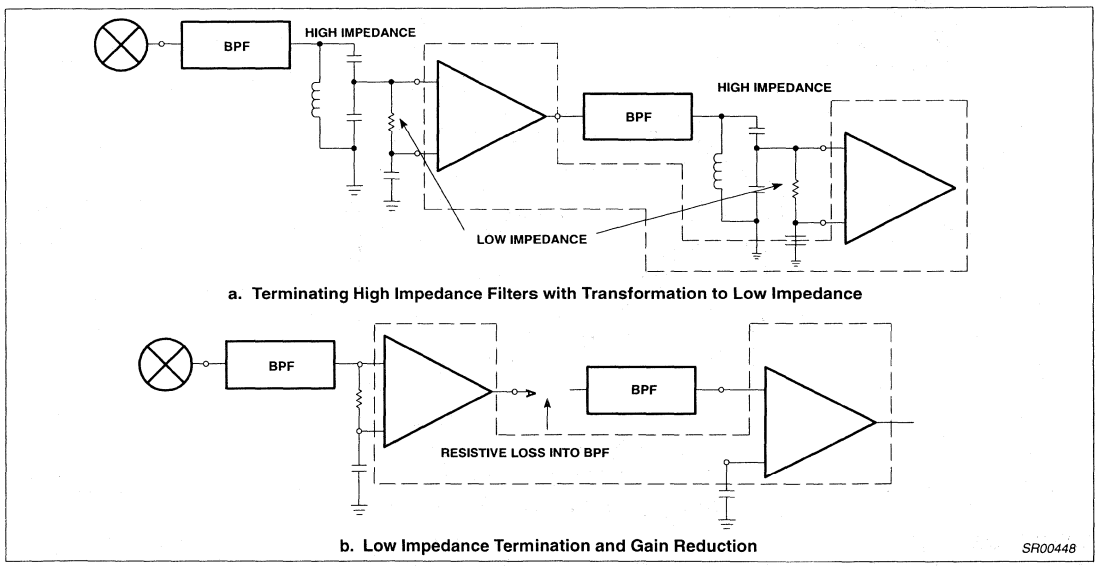


Figure 9. Practical Termination

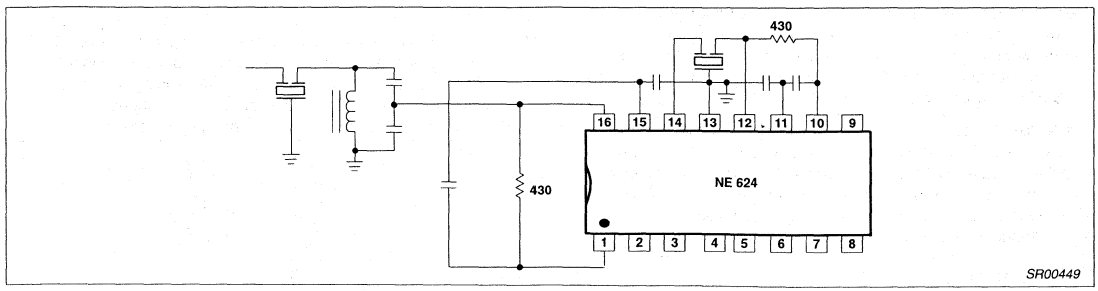


Figure 10. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 9. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE624 IF amplifiers, which is not specified, is low phase shift. The NE624 is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

Stability Considerations

The high gain and bandwidth of the NE624 in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 3, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{CC} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 3 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 9 demonstrates a practical means.

As illustrated in Figure 10, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 7 shows an equivalent circuit of the NE624 quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 12. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE624

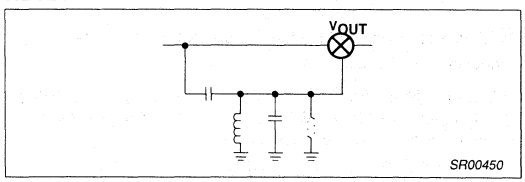


Figure 11.

$$V_O = \frac{C_S}{C_P + C_S} \cdot \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \cdot V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1-\left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 12 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \sin \omega t \Rightarrow V_O = A$ (3)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$V_{IN} \bullet V_O = A^2 \sin \omega t$ (4)

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2}A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] \quad (5)$$

$$= \frac{1}{2}A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1\frac{\omega_1}{\omega} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 12) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 624 is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and $L = 0.7\text{mH}$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10\text{pF}$ and $C_P = 164\text{pF}$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1\text{pF}$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. SInge the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE624 demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 5) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was

optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE624 are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

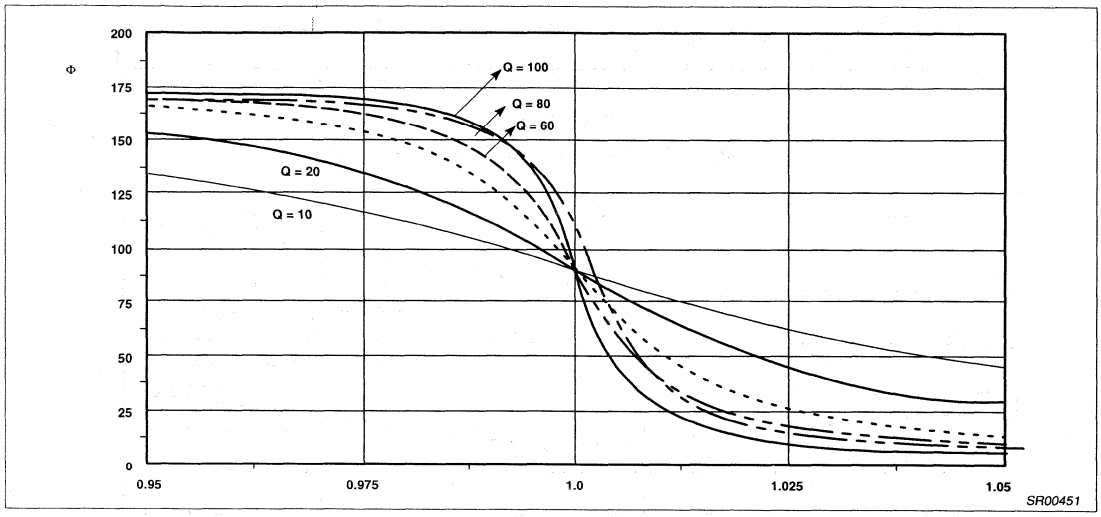


Figure 12. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

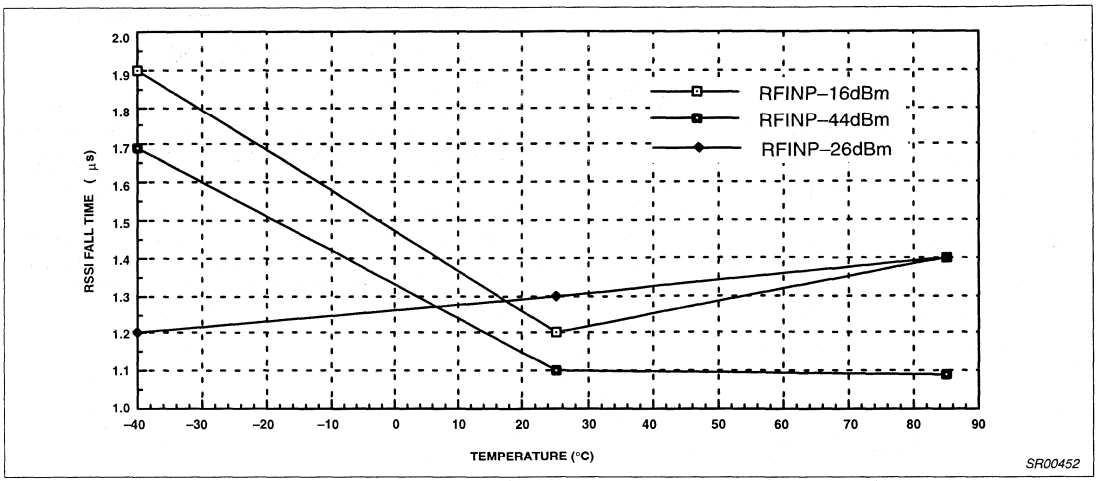


Figure 13. NE/SA624 Rise Time 455kHz IF Frequency

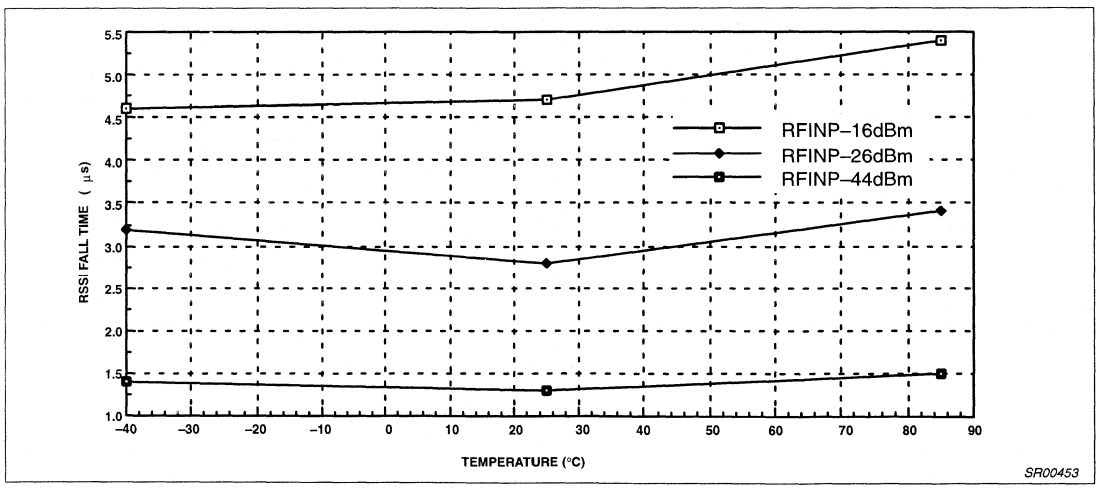


Figure 14. NE/SA624 Fall Time 455kHz IF Frequency

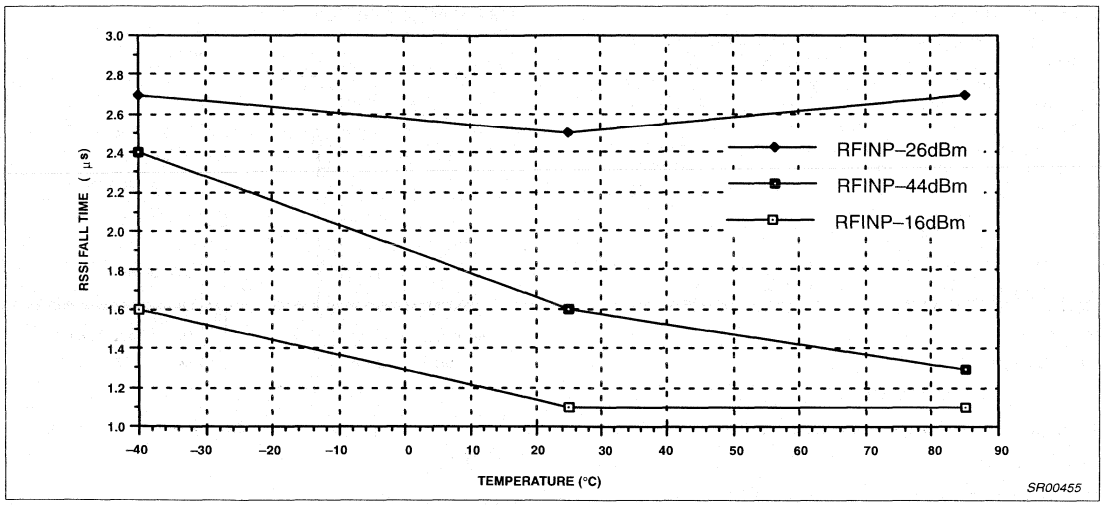


Figure 15. NE/SA624 Rise Time 10.7MHz IF Frequency

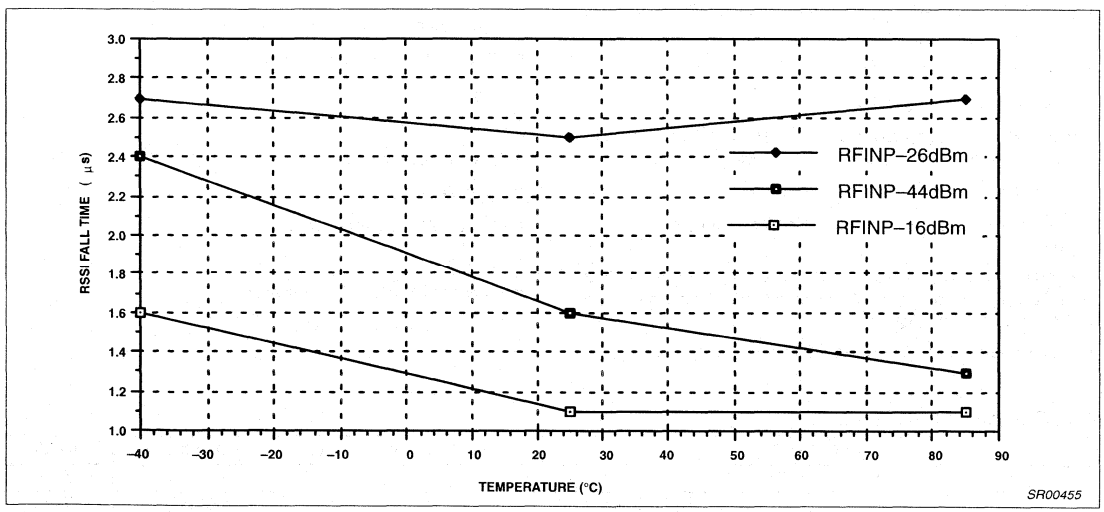


Figure 16. NE/SA624 Fall Time 10.7MHz IF Frequency

High performance low power mixer FM IF system with high-speed RSSI

NE/SA625

DESCRIPTION

The NE/SA625 is pin-to-pin compatible with the NE/SA605, but has faster RSSI rise and fall times. The NE/SA625 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI) with fast rise and fall time, and voltage regulator. The NE/SA625 combines the functions of Signetics' NE602A and NE624. The NE/SA625 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product and artwork for reference.

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 5.8mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA625 meets cellular radio specifications

PIN CONFIGURATION

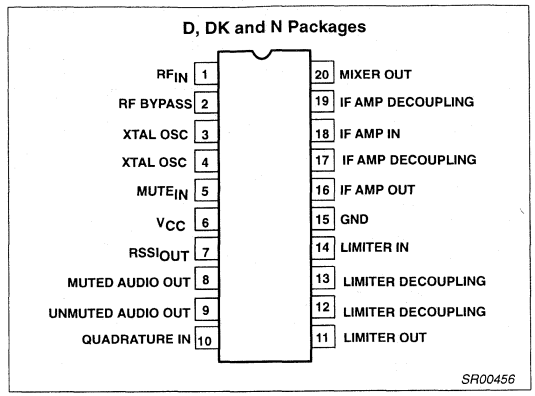


Figure 1. Pin Configuration

- ESD hardened

APPLICATIONS

- Digital cellular base stations
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification
- Digital cordless telephones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE625N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	0 to +70°C	NE625D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	0 to +70°C	NE625DK	SOT266-1
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA625N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA625D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA625DK	SOT266-1

BLOCK DIAGRAM

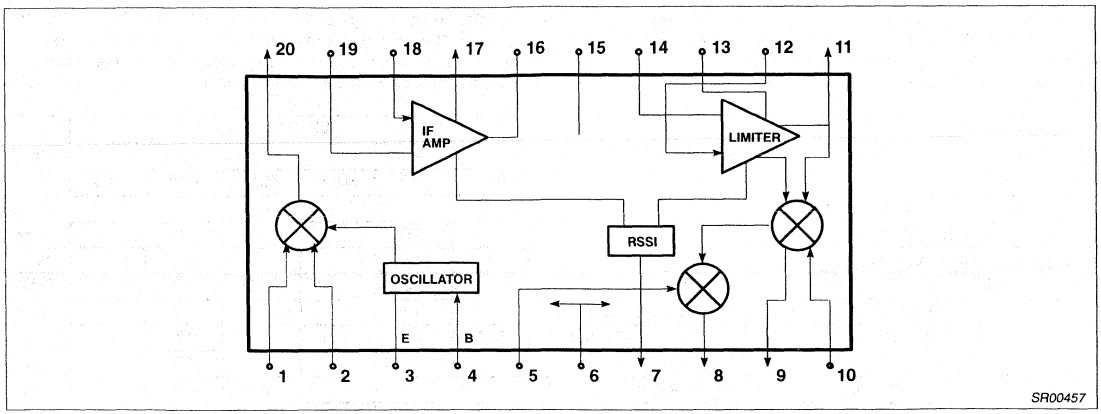


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range NE625		0 to +70	°C
	SA625		-40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W
		DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.8	6.7	4.55	5.8	6.75	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480			480		mV
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	IF RSSI output rise time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.2			1.2		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.1			1.1		µs
	IF RSSI output fall time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		2.1			2.1		µs
		RF level = -28dBm		7.6			7.6		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		2.0			2.0		µs
		RF level = -28dBm		7.3			7.3		µs
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		1.40	1.6		kΩ
	Limiter output impedance			300			300		Ω
	Limiter output level with no load			280			280		mV_{RMS}

AC ELECTRICAL CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
IF section (continued)									
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ
RF/IF section (int LO)									
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450			450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA625 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA625 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA625 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

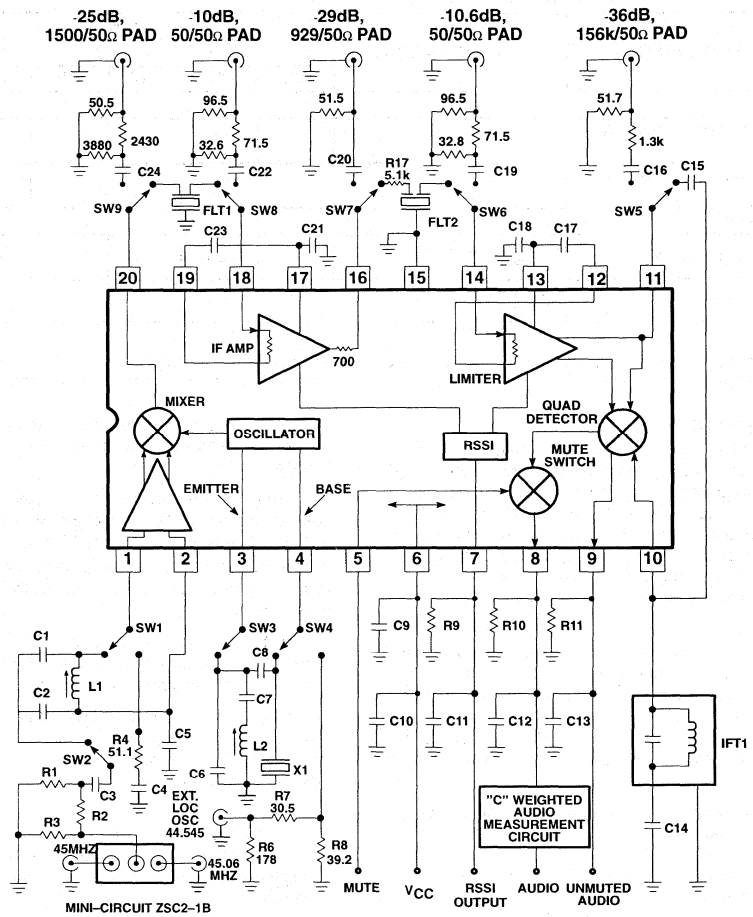
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



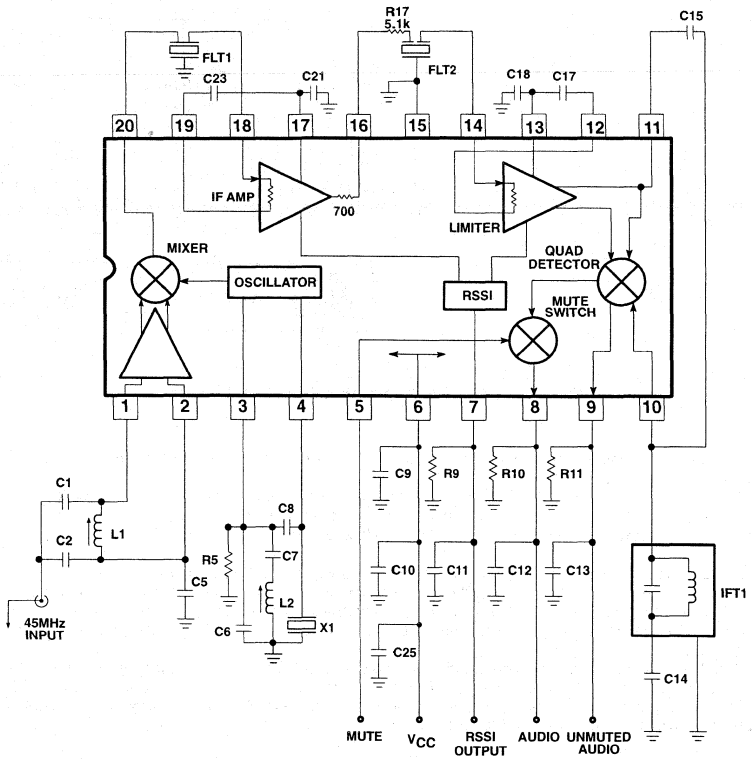
Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8µH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

SR00458

Figure 3. NE/SA625 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8µH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

SR00459

Figure 4. NE/SA625 45MHz Application Circuit

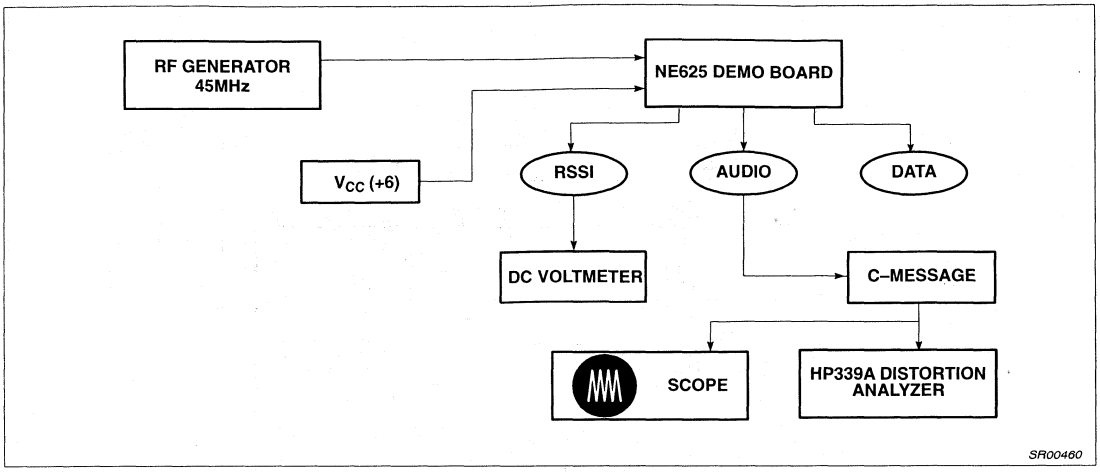


Figure 5. NE/SA625 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

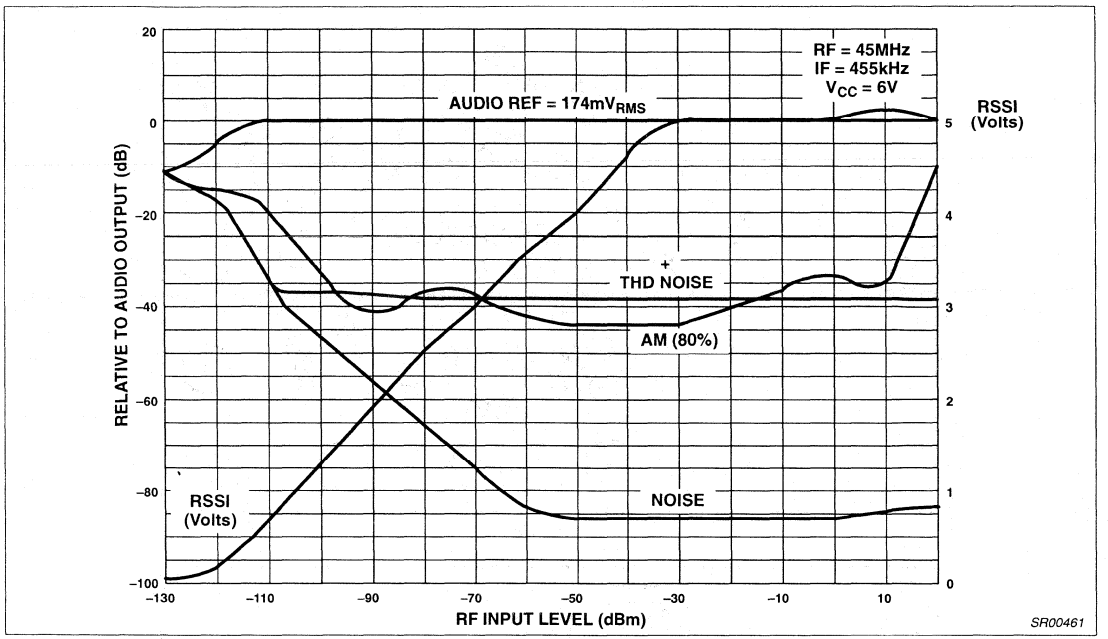


Figure 6. NE625 Application Board at 25°C

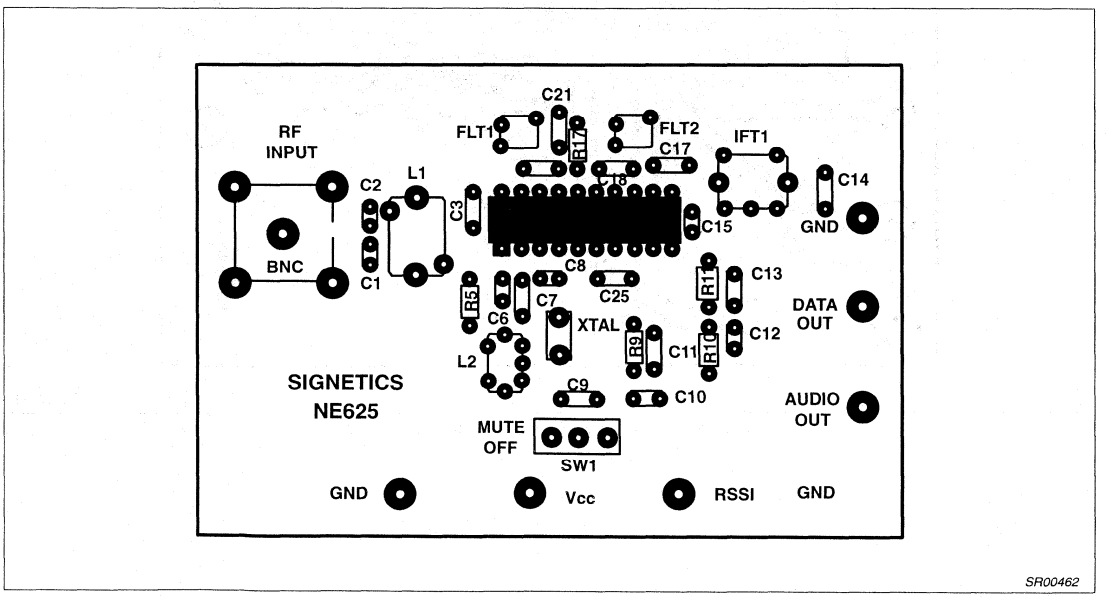
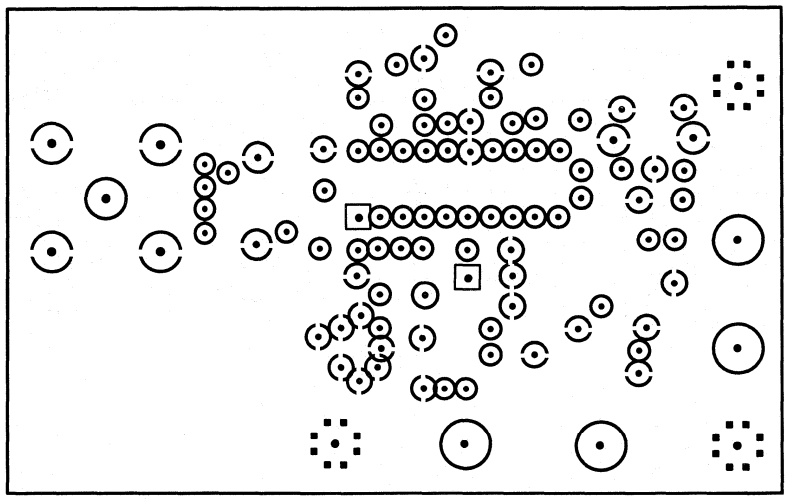
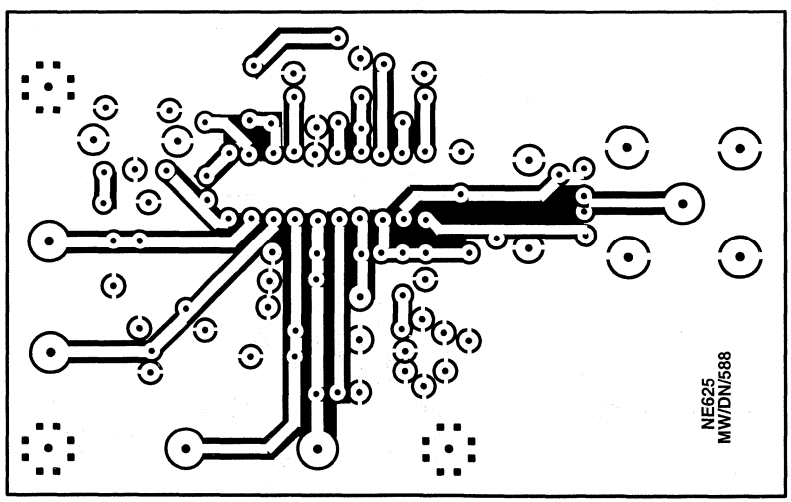


Figure 7. Component Placement for NE625 Application Circuit



TOP VIEW



BOTTOM VIEW

SR00463

Figure 8. Layout for NE/SA625 Application Board

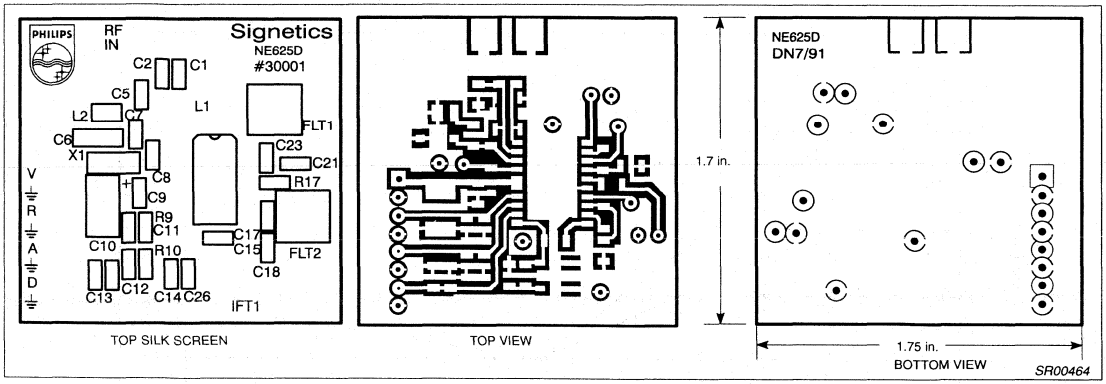


Figure 9. NE625 SO Demo-board Layout (Not Actual Size)

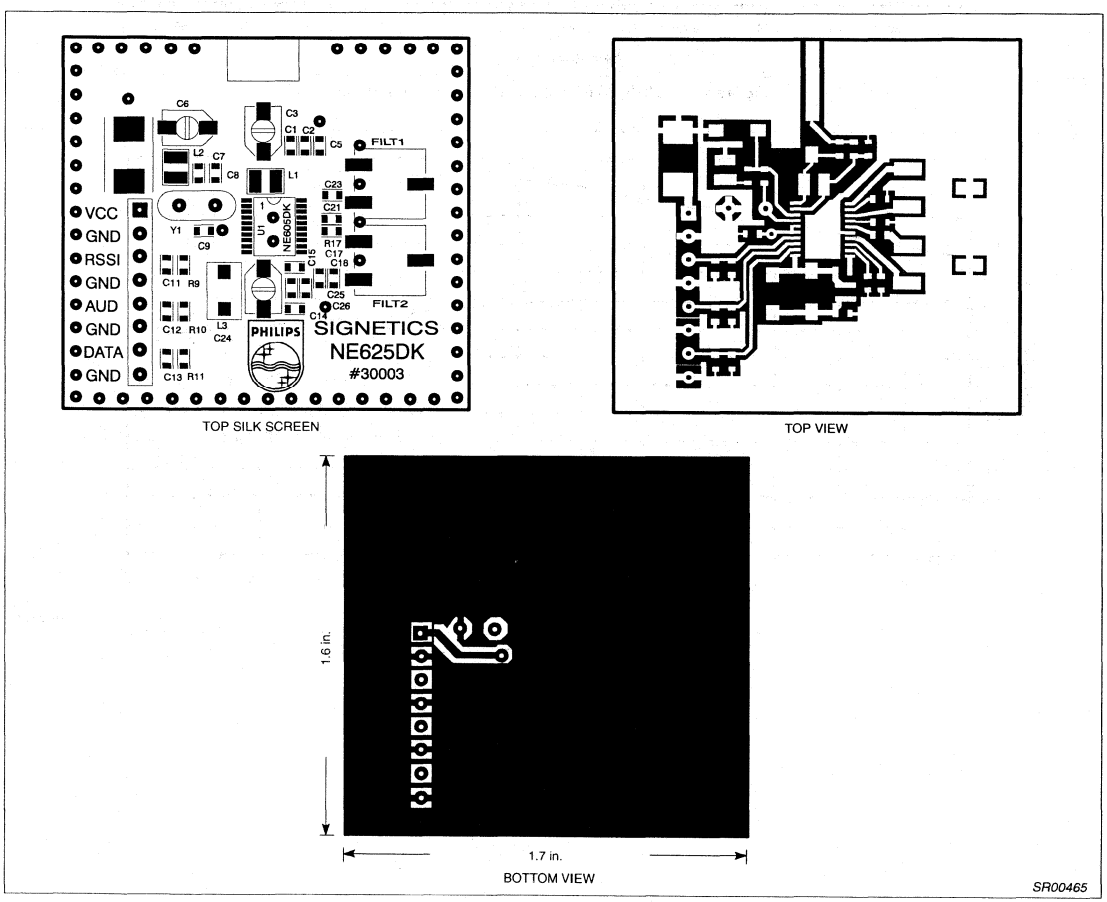


Figure 10. NE625 SSOP Demo-board Layout (Not Actual Size)

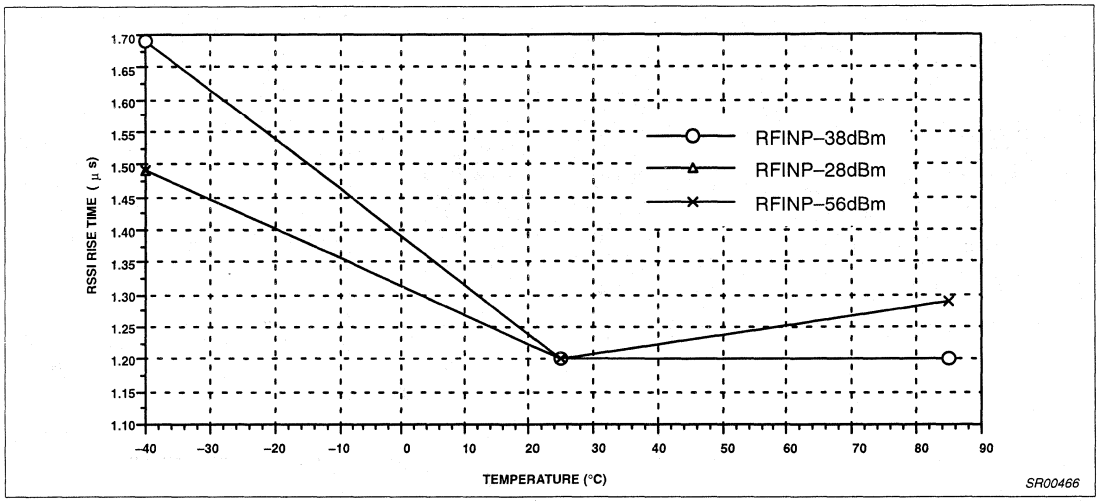


Figure 11. NE/SA625 Rise Time 455kHz IF Frequency

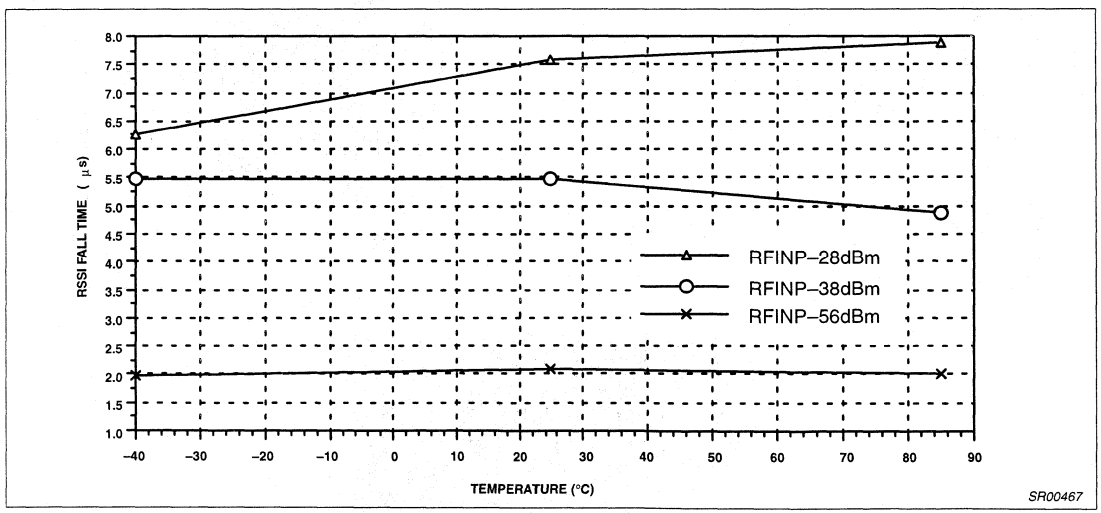


Figure 12. NE/SA625 Fall Time 455kHz IF Frequency

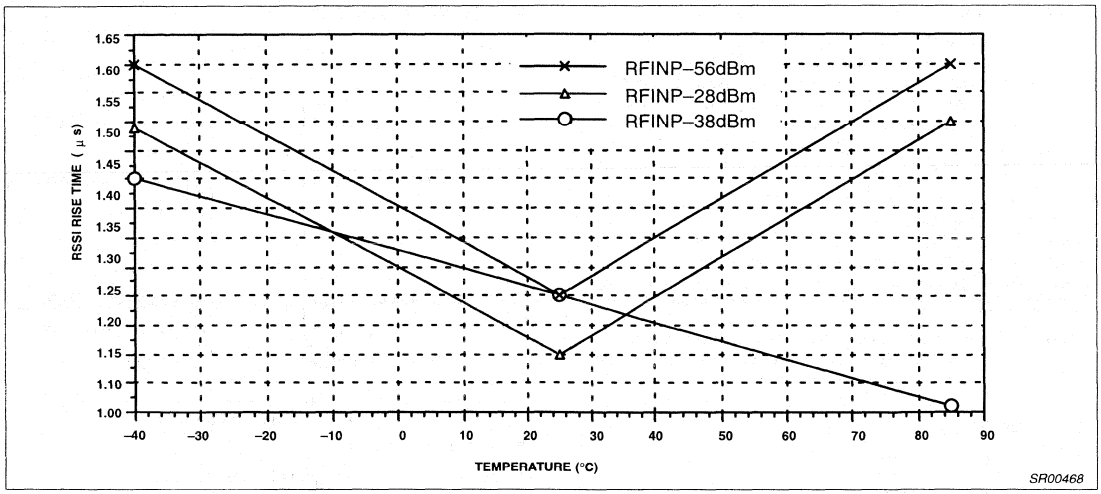


Figure 13. NE/SA625 Rise Time 10.7MHz IF Frequency

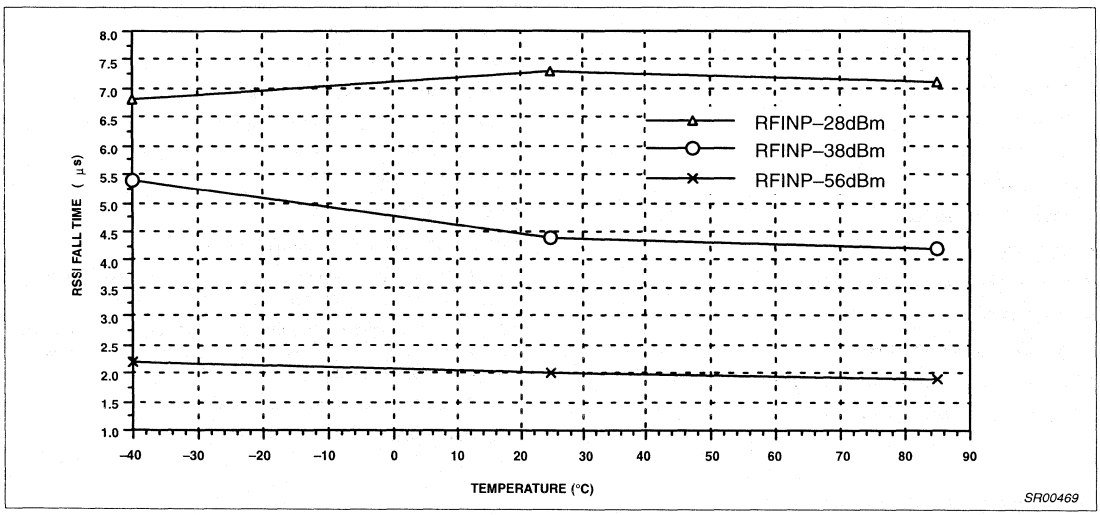


Figure 14. NE/SA625 Fall Time 10.7MHz IF Frequency

Low voltage high performance mixer FM IF system with high-speed RSSI

SA626

DESCRIPTION

The SA626 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, high speed logarithmic received signal strength indicator (RSSI), voltage regulator and audio and fast RSSI op amps. The SA626 is available in 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The SA626 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio and RSSI outputs have amplifiers. The RSSI output has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

SA626 incorporates a power down mode which powers down the device when Pin 8 is low. Power down logic levels are CMOS and TTL compatible with high input impedance.

APPLICATIONS

- Digital cordless telephones
- Digital cellular telephones
- Digital cellular base stations
- Portable high performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 6.5mA typ at 3V
- Power down mode (I_{CC} = 200µA)

PIN CONFIGURATION

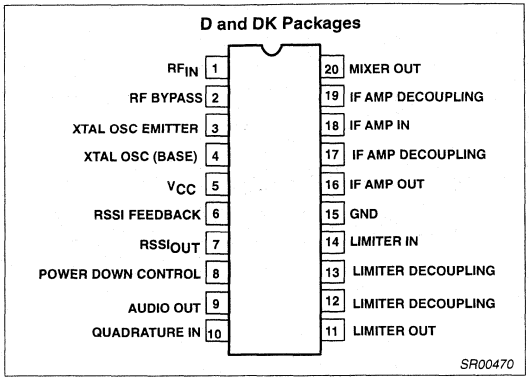


Figure 1. Pin Configuration

- Mixer input to >500MHz
- Mixer conversion power gain of 11dB at 240MHz
- Mixer noise figure of 14dB at 240MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz, local oscillator can be injected)
- 92dB of IF Amp/Limiter power gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Audio output internal buffer
- RSSI output internal buffer
- Internal op amps with rail-to-rail outputs
- 10.7MHz filter matching (330Ω) reduces external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.54µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 240MHz and IF at 10.7MHz
- SA626 meets cellular radio specifications
- ESD hardened

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA626D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA626DK	SOT266-1

BLOCK DIAGRAM

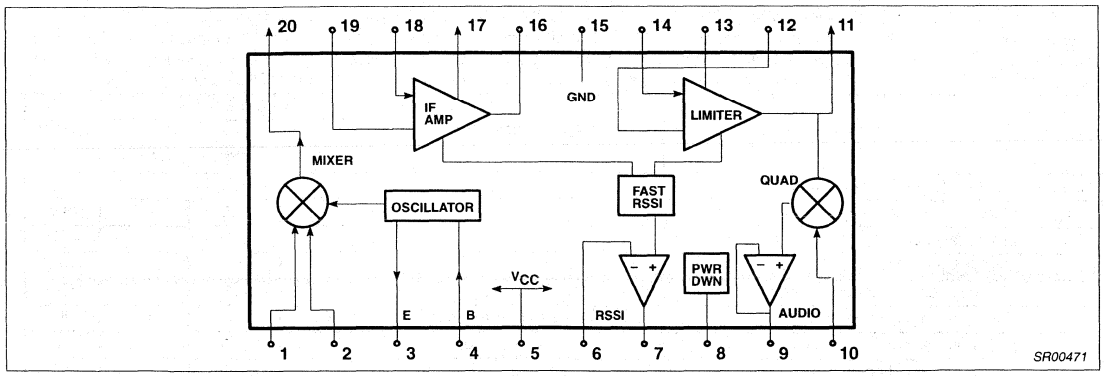


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	0.3 to 7	V
V_{IN}	Voltage applied to any other pin	–0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA626	–40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

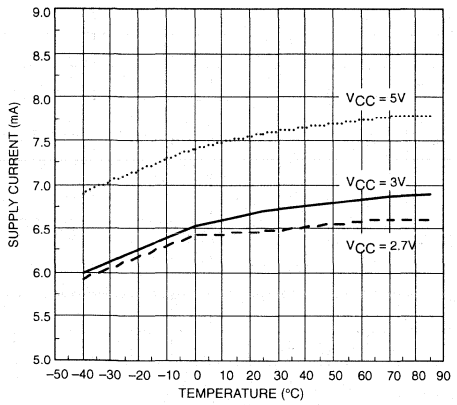
V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA626 MIN	LIMITS SA626 TYP	LIMITS SA626 MAX	UNITS
V_{CC}	Power supply voltage range		2.7	3.0	5.5	V
I_{CC}	DC current drain	Pin 8 = HIGH	5.5	6.5	7.5	mA
I_{CC}	Standby	Pin 8 = LOW		0.2	0.5	mA
	Input current	Pin 8 LOW	–10		10	µA
		Pin 8 HIGH	–10		10	µA
	Input level	Pin 8 LOW	0		$0.3V_{CC}$	V
		Pin 8 HIGH	$0.7V_{CC}$		V_{CC}	V
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

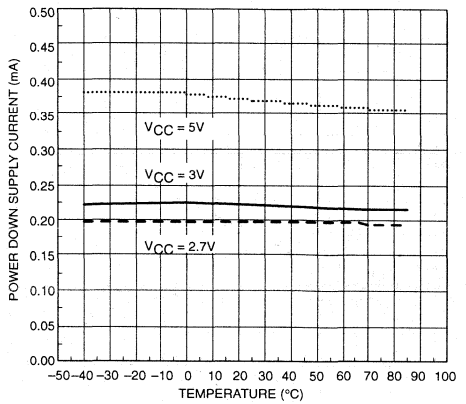
AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 240.05MHz + 14.5dBV RF input step-up; IF frequency = 10.7MHz; RF level = -68dBm; FM modulation = 1kHz with ±125kHz peak deviation. Audio output with C-message weighted filter and de-emphasis filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

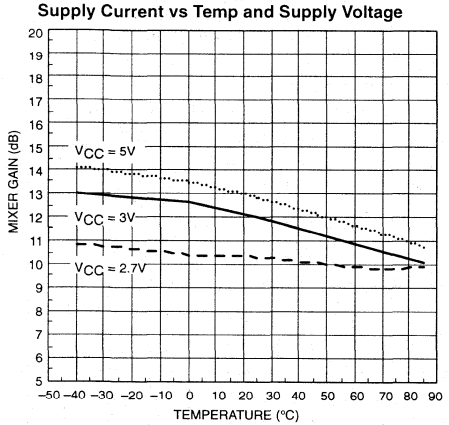
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA626 MIN	LIMITS SA626 TYP	LIMITS SA626 MAX	UNITS
Mixer/Osc section (ext LO = 160mV$_{RMS}$)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	External oscillator (buffer)			500		MHz
	Noise figure at 240MHz			14		dB
	Third-order input intercept point	Matched f1=240.05; f2=240.35MHz		-16		dBm
	Conversion power gain	Matched 14.5dBV step-up	8	11	14	dB
	RF input resistance	Single-ended input		700		Ω
	RF input capacitance			3.5		pF
	Mixer output resistance	(Pin 20)		330		Ω
IF section						
	IF amp power gain			38		dB
	Limiter amp power gain			54		dB
	Input limiting -3dB	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		50		dB
	Audio level	Unity gain	120	160	200	mV$_{RMS}$
	Audio DC level	Pin 9, no signal		1.0		V
	SINAD sensitivity	IF level = -111dBm		16		dB
THD	Total harmonic distortion			-43	–38	dB
S/N	Signal-to-noise ratio	No modulation for noise		60		dB
	IF RSSI output with buffer	IF level = -118dBm		0.2	0.5	V
		IF level = -68dBm	0.3	0.6	1.0	V
		IF level = -10dBm	0.9	1.3	1.8	V
	IF RSSI output rise time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		1.2		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		1.1		µs
	IF RSSI output fall time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		2.0		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		7.3		µs
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance			330		Ω
	IF output impedance			330		Ω
	Limiter input impedance			330		Ω
	Limiter output impedance			300		Ω
	Limiter output level with no load			130		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	RF level = -10dBm		160		mV$_{RMS}$
	System RSSI output	RF level = -10dBm		1.4		V
	System SINAD	RF level = -106dBm		12		dB



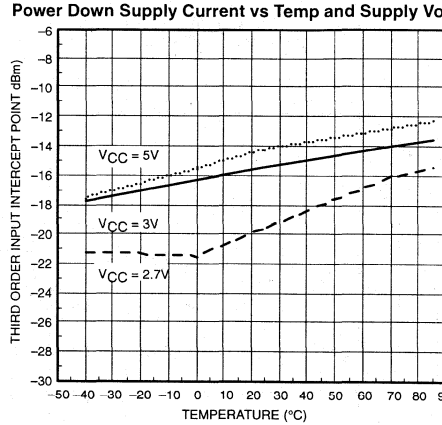
Supply Current vs Temp and Supply Voltage



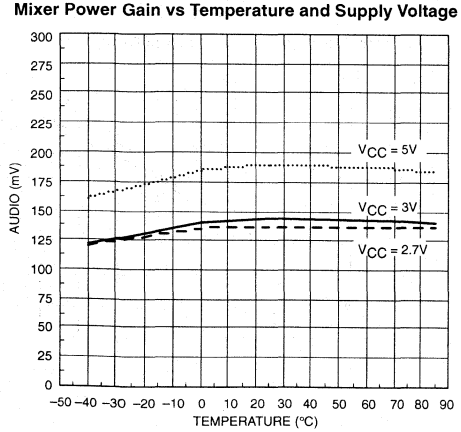
Power Down Supply Current vs Temp and Supply Voltage



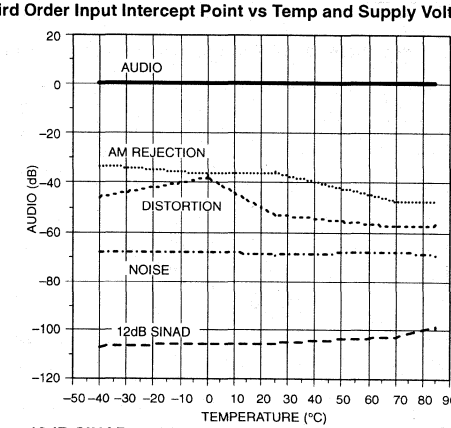
Mixer Power Gain vs Temperature and Supply Voltage



Third Order Input Intercept Point vs Temp and Supply Voltage

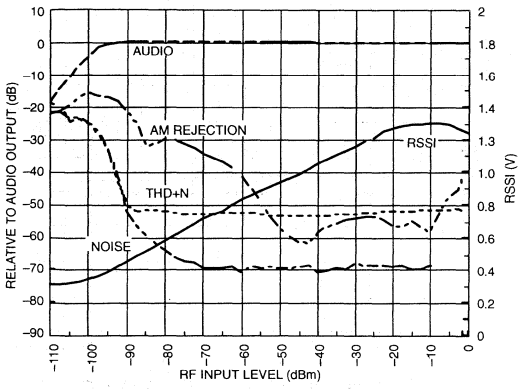


Audio Output Level vs. Temp and Supply Voltage

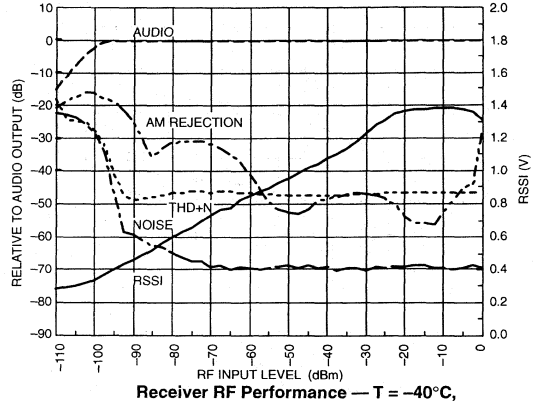


12dB SINAD and Relative Audio, THD, Noise and AM Rejection for VCC = 3V vs Temperature RF = 240MHz, Level = –68dBm, Deviation = 125kHz *SR00472*

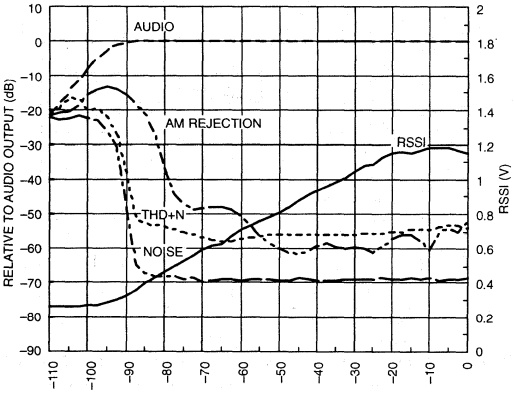
Figure 3. Performance Characteristics



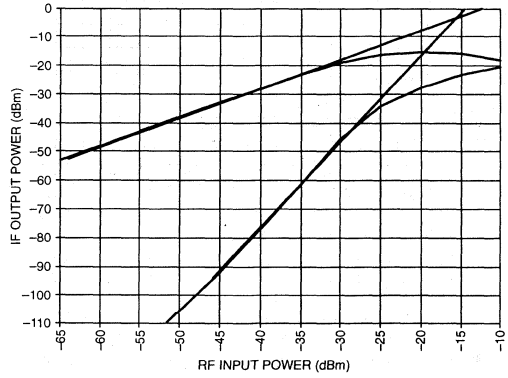
Receiver RF Performance — T = 25°C, Audio Level = 129mV$_{RMS}$



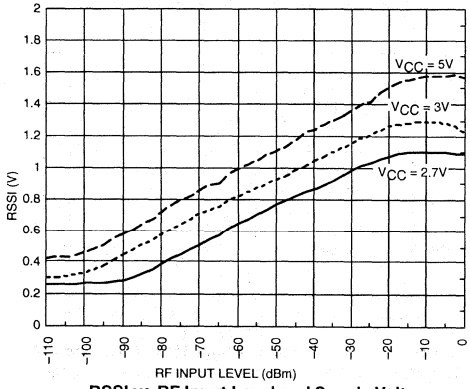
Receiver RF Performance — T = –40°C, Audio Level = 118mV$_{RMS}$



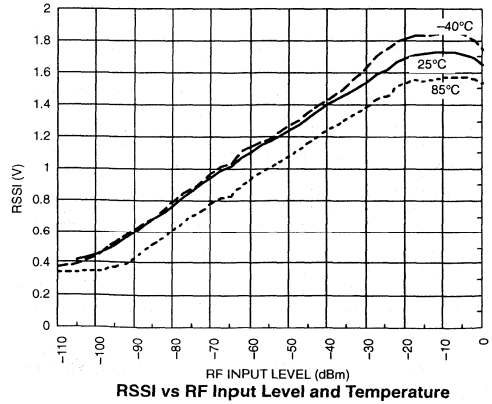
Receiver RF Performance – T = 85°C, Audio Level = 131mV$_{RMS}$



Mixer Third Order Intercept and Compression



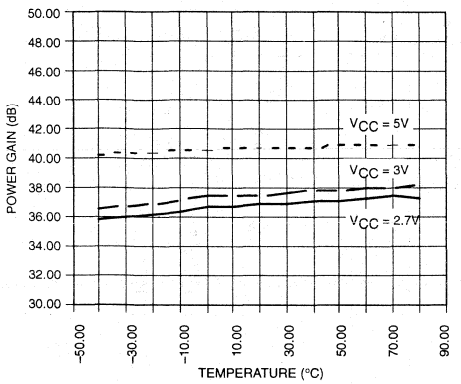
RSSI vs RF Input Level and Supply Voltage



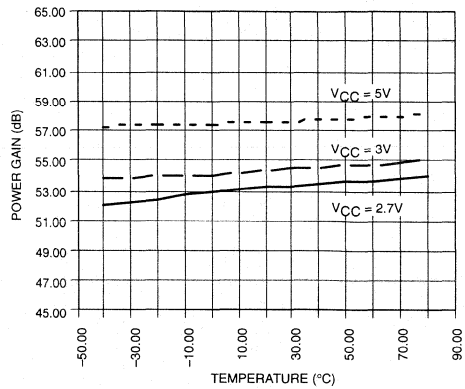
RSSI vs RF Input Level and Temperature

SR00473

Figure 4. Performance Characteristics



SA626 IF Amplifier Gain vs Temperature vs Supply Voltage



SA626 Limiting Amplifier Gain vs Temperature vs Supply Voltage

SR00474

Figure 5. Performance Characteristics

CIRCUIT DESCRIPTION

The SA626 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 38dB of power gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 54dB of power gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 10.7MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as cordless and cellular hand-held phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 14dB, conversion power gain of 11dB, and input third-order intercept of -16dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 10.7MHz ceramic filter. The input resistance of the limiting IF amplifiers is also 330Ω. With most 10.7MHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 3dB insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 3dB insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

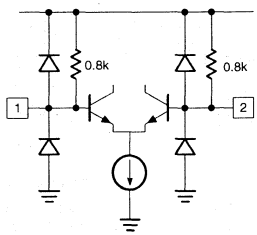
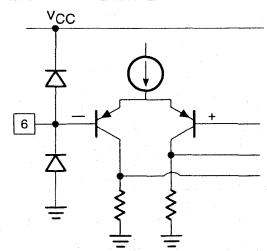
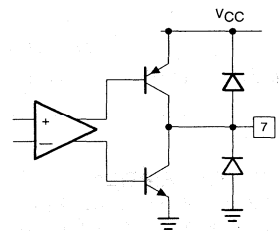
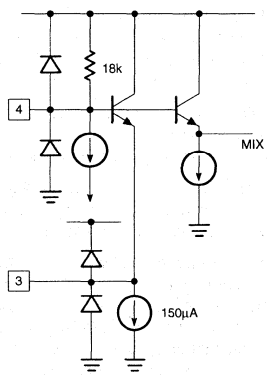
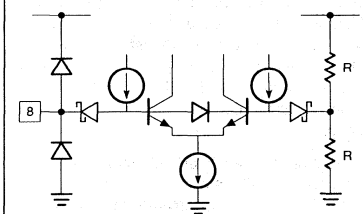
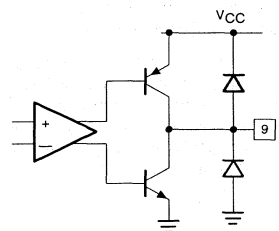
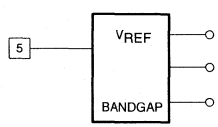
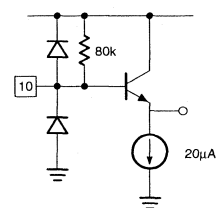
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a power gain of 92dB. For operation at intermediate frequency at 10.7MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature drives an internal op amp. This op amp is configured as a unity gain buffer. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength indicator completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone, and RCR-28 cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	+2.75	
4	XTAL OSC	+2.32		9	AUDIO OUT	+1.09	
5	VCC	+3.00		10	QUAD. IN	+3.00	

SR00475

Figure 6. Pin Functions

PIN FUNCTIONS (continued)

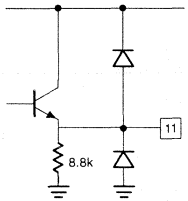
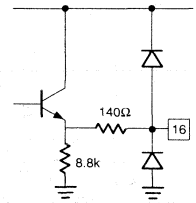
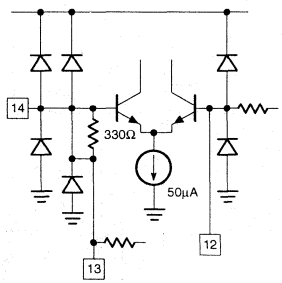
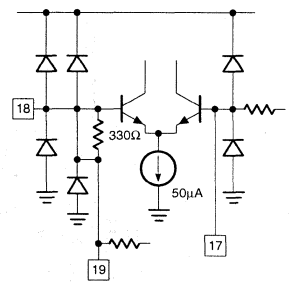
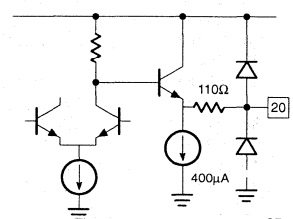
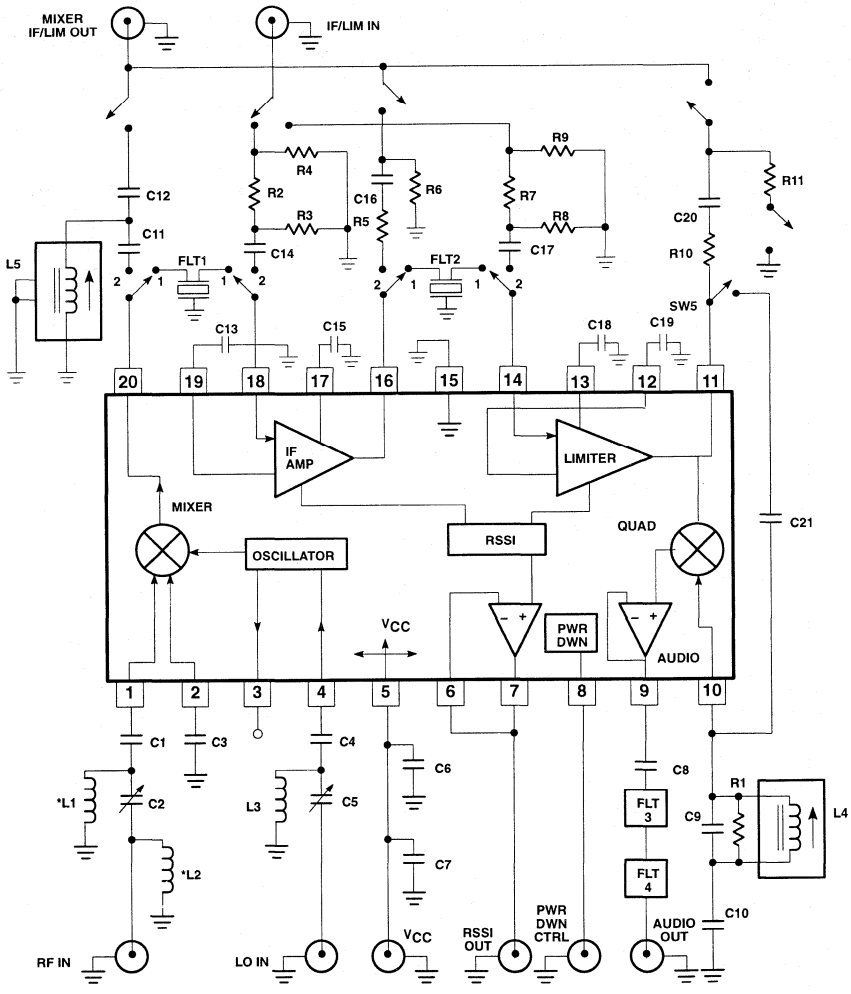
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	LIMITER OUT	+1.35		16	IF AMP OUT	+1.22	
12	LIMITER DECOUP	+1.23		17	IF AMP DECOUP	+1.22	
13	LIMITER COUPLING	+1.23		18	IF AMP IN	+1.22	
14	LIMITER IN	+1.23		19	IF AMP DECOUP	+1.22	
15	GND	0		20	MIXER OUT	+1.03	

Figure 7. Pin Functions (cont.)



Automatic Test Circuit Component List

R1	8.2kΩ select	C1	0.1μF	C12	160pF select	L1	150nH select for input match
R2	6.42kΩ	C2	1–5pF select for input match	C13	1000pF	L2	22nH select for input match
R3	347.8Ω	C3	0.1μF	C14	0.1μF	L3	47nH select for input match
R4	49.9Ω	C4	0.1μF	C15	1000pF	L4	5.6μH select for input match
R5	1kΩ	C5	1–5pF select for input match	C16	0.1μF	L5	1.27–2.25μH select for mixer output match
R6	49.9Ω	C6	100pF	C17	0.1μF		
R7	6.42kΩ	*C7	6.8μF 10V	C18	1000pF	FLT1	10.7MHz (Murata SFE10.7MA5-A)
R8	347.8Ω	C8	1μF	C19	1000pF	FLT2	10.7MHz (Murata SFE10.7MA5-A)
R9	49.9Ω	C9	39pF select	C20	0.1μF	FLT3	"C" message weighted
R10	1kΩ	C10	0.1μF	C21	1pF	FLT4	Active de-emphasis
R11	49.9Ω	C11	0.1μF				

*NOTE: This value can be reduced when a battery is the power source.

SR00477

Figure 8. SA626 240.5MHz (RF) / 10.7MHz (IF) Test Circuit

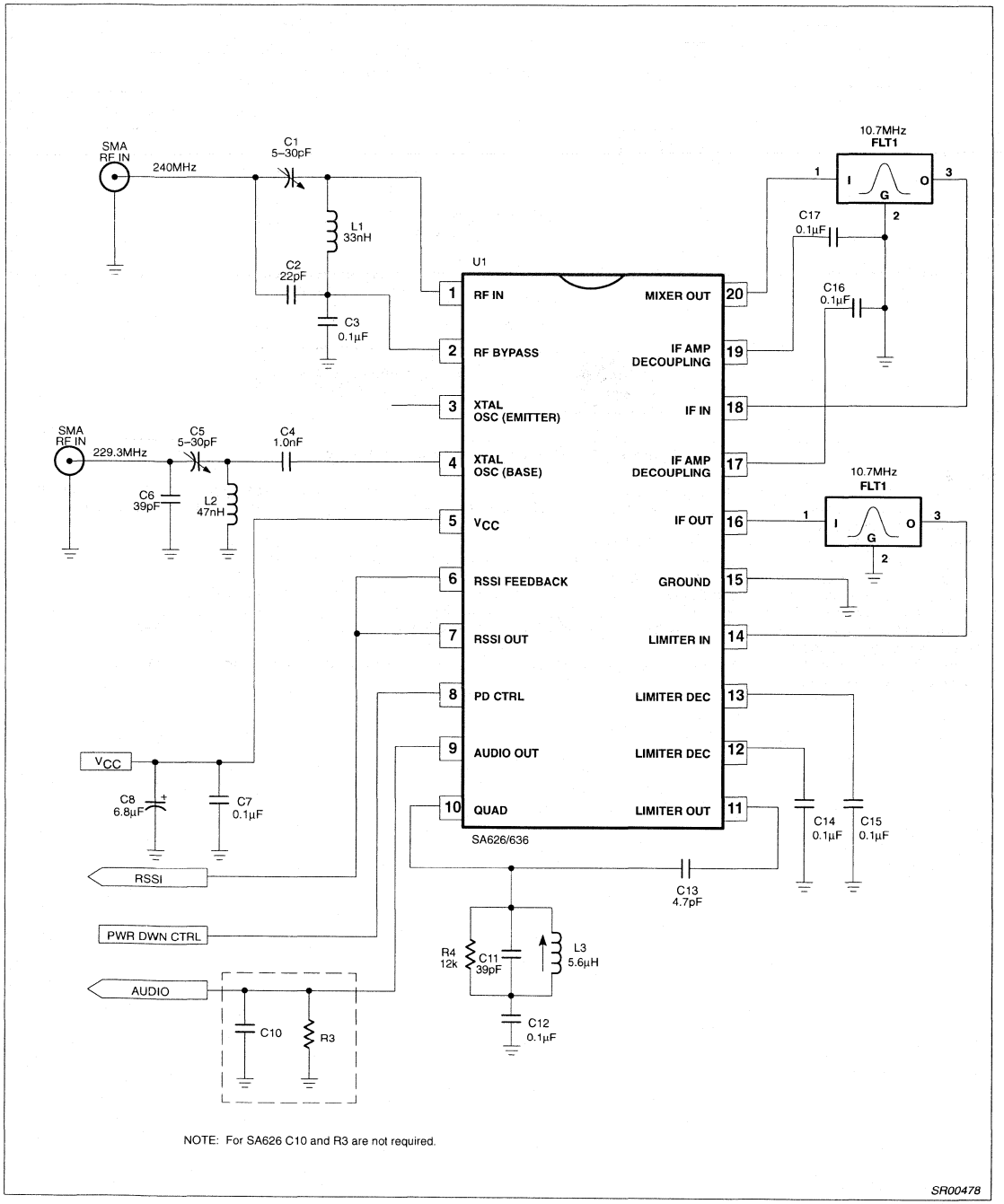


Figure 9. SA626 240MHz (RF) / 10.7MHz (IF) Application Circuit

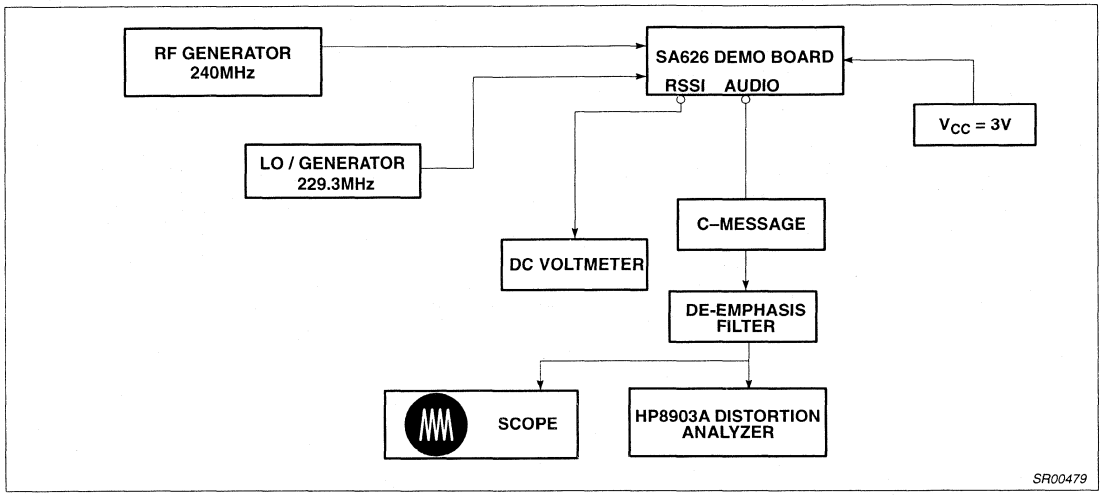
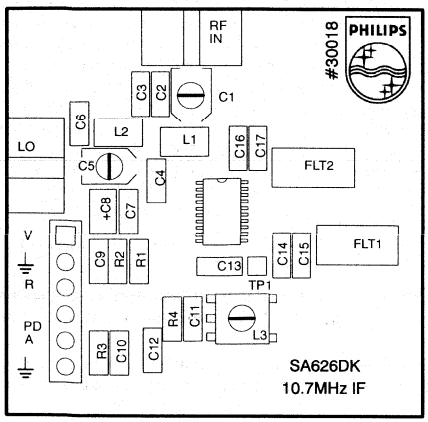


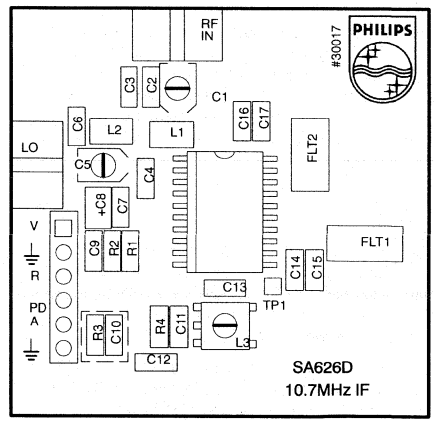
Figure 10. SA626 Application Circuit Test Set Up

NOTES:

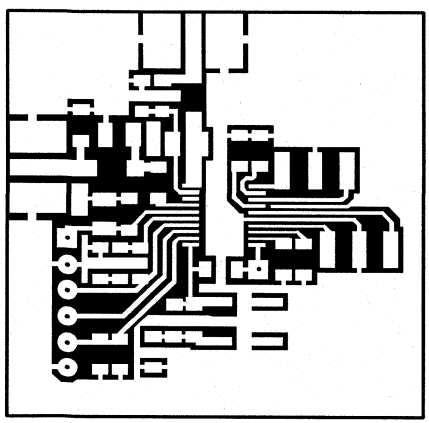
1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP8903A analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filter can be SFE10.7MA5-A made by Murata which has 280kHz IF bandwidth.
3. RF generator: Set your RF generator at 240.000MHz, use a 1kHz modulation frequency and a 125kHz deviation.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.54μV or –112dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1μF bypass capacitor on the supply pin improves sensitivity.



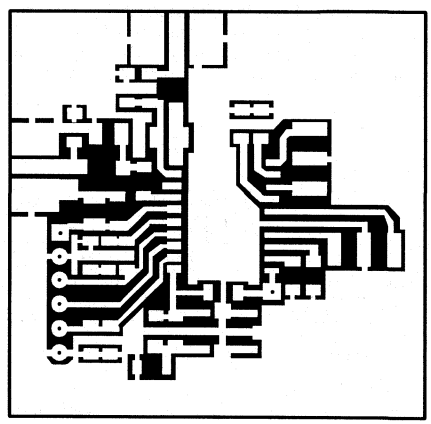
TOP SILK SCREEN (SSOP)



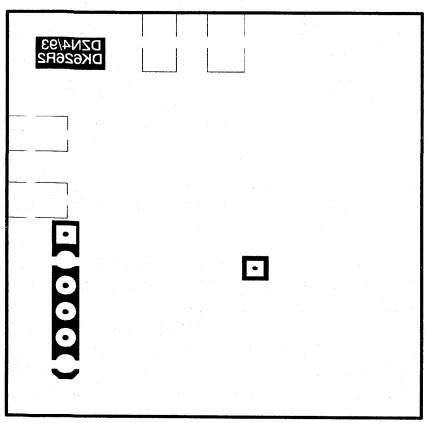
TOP SILK SCREEN (SOL)



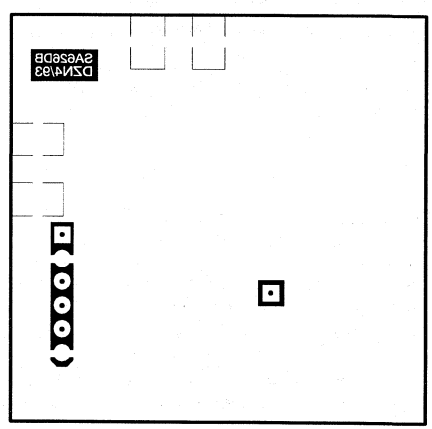
TOP VIEW (SSOP)



TOP VIEW (SOL)



BOTTOM VIEW (SSOP)



BOTTOM VIEW (SOL)

SR00480

Figure 11. SA626 Demoboard Layout (Not Actual Size)

Philips FM/IF systems for GMSK/GFSK receivers AN1997

Author: Yanpeng Guo

ABSTRACT

To assist Philips Semiconductors customers in digital cellular and wireless/PCS system design, a Philips FM/IF system-based GMSK/GFSK demoboard has been developed based on CT-2 specifications. This application note presents a detailed description of this board including circuits, design information, and measured BER performance. The circuit diagram, component list, and board layout are also included.

INTRODUCTION

In order to meet the rapidly increasing demand for mobile radio and wireless/PCS services, digital cellular and digital wireless systems have become the new generation of mobile communications for higher capacity. It is a new challenge for engineers to find IC solutions for these digital wireless applications.

In worldwide digital cellular, wireless/PCS standards, GMSK/GFSK modulation techniques have been widely employed as illustrated in Table 1. In order to assist the applications of Philips ICs in these digital systems, a Philips FM/IF system-based GMSK/GFSK demoboard has been developed. The purpose of this application note is to provide a detailed description of this board, to help customers achieve the best performance using Philips SA626, and also to provide suggestions for the applications of other Philips FM/IF systems.

Table 1. A Summary of Digital Cellular and Cordless Standards

Standard	Access	Modulation	Bit Rate	Ch. Spacing
IS-54	TDMA	π/4-DQPSK	48 kb/s	30 kHz
GSM	TDMA	GMSK	270 kb/s	200 kHz
CT-2	TDMA	GFSK	72 kb/s	100 kHz
DECT	TDMA	GFSK	1.152 Mb/s	1.728 MHz

This application note is organized as follows:

- Introduction.
- Review of GMSK/GFSK modulation: advantages of GMSK/GFSK modulation techniques and implementation methods.
- Overview of the demoboard: general block diagram and detailed description of each part of the board.
- BER measurements: measurement set-up, procedures, and measured results.
- Questions & Answers.

REVIEW OF GMSK/GFSK MODULATION

GMSK(Gaussian Minimum Shift Keying) is a premodulation Gaussian filtered binary digital frequency modulation scheme with modulation index of 0.5. The following features make GMSK very suitable for digital cellular and wireless applications.

1. Constant envelope: this allows the operation of Class-C RF power amplifiers to achieve higher system power efficiency.
2. Narrow power spectrum: narrow mainlobe and low spectral tails keep the adjacent channel interference to low levels and achieve higher spectral efficiency.
3. Coherent/non-coherent detection capabilities.
4. Good BER performance.

GMSK modulation can be implemented in two ways. The most straightforward way is to transmit the data stream through a Gaussian low-pass filter and apply the resultant wave form to a voltage controlled oscillator (VCO) as shown in Figure 1. The output of the VCO is then a frequency modulated signal with a Gaussian response. The advantage of this scheme is the simplicity, but it is difficult to keep an exact modulation index of 0.5 with this scheme. Therefore, VCO implemented GMSK is usually used in non-coherent detection systems such as DECT and CT2.

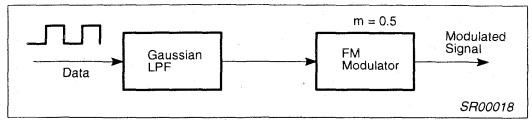


Figure 1. VCO Implemented GMSK Modulator

GMSK signals can also be generated using a quadrature modulation structure. Consider the phase modulated signal given by:

$$s(t) = \cos[\omega_C t + \phi(t)] \quad \text{(EQ. 1)}$$

This can be expanded into its in-phase and quadrature components,

$$s(t) = \cos[\phi(t)]\cos(\omega_C t) - \sin[\phi(t)]\sin(\omega_C t) \quad \text{(EQ. 2)}$$

The quadrature modulator is based on Equation (2). The implementation of such a GMSK modulator is shown in Figure 2. The incoming data is used to address two separate ROMs which contain the sampled versions of all possible phase trajectories within a given interval. After D/A conversion, the output of each ROM is applied to the I/Q modulator. The output is the GMSK modulated signal. This implementation scheme provides an exact modulation index of 0.5, which allows coherent detection.

GFSK (Gaussian Frequency Shift Keying) is also a premodulation Gaussian filtered digital FM scheme, but without the restriction of modulation index to be 0.5. The block diagram of GFSK modulator is the same as shown in Figure 1, but the modulation index can be specified according to the applications.

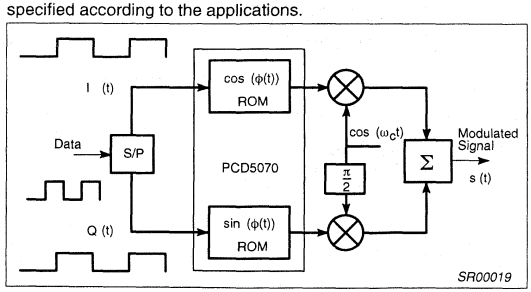


Figure 2. I/Q Implemented GMSK Modulator

GMSK signals can be demodulated in three ways: 1.) FM discriminator detection, 2.) differential detection, and 3.) coherent detection. The coherent detection scheme has the best BER performance, but is only suitable for I/Q structure based GMSK systems (Ref 6.). The differential detection method has BER degradation even with complex implementation (Ref 7.). The limit/frequency discriminator structure is the simplest scheme suitable for both GMSK and GFSK applications. Therefore, the FM discriminator technique is widely used for GMSK/GFSK demodulation in digital cellular/PCS applications. Figure 3 presents the block diagram of an FM discriminator GMSK/GFSK demodulator.

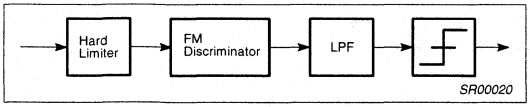


Figure 3. Limit/Frequency Discriminator GMSK/GFSK Demodulator

OVERVIEW OF THE GMSK/GFSK DEMOBOARD

Figure 4 is the block diagram of a VCO/FM discriminator based GMSK/GFSK modem (modulator/demodulator), which also illustrates the structure of the Philips GMSK/GFSK demoboard. The demoboard contains the entire demodulator as well as the Gaussian low-pass filter (LPF) for the modulator. The input data stream is first premodulation filtered by the Gaussian LPF, then the filtered base band wave form is applied to an FM signal generator with specific modulation index. The output is then the GMSK/GFSK modulated signal. After the limit/frequency discriminator detection, a Gaussian LPF is employed to eliminate noise. The output of the threshold detector is the regenerated binary data, which can be sent to a data error analyzer to evaluate the BER performance.

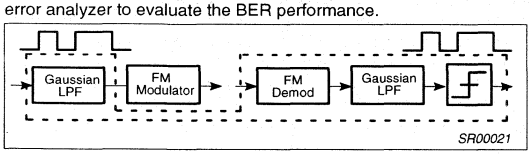


Figure 4. VCO/FM Discriminator GMSK/GFSK Modem (dotted line for the demoboard)

Gaussian LPF

On the demoboard, a 4th-order Gaussian LPF is implemented for both premodulation filtering and post demodulation filtering. The response function of this 4th-order filter can be expressed as (Ref 4.):

$$H(s) = \frac{\omega_1^2}{S^2 + 2\zeta_1\omega_1 S + \omega_1^2} \cdot \frac{\omega_2^2}{S^2 + 2\zeta_2\omega_2 S + \omega_2^2} \quad \text{(EQ. 3)}$$

By looking up the Gaussian LPF poles table[4], with 3dB bandwidth normalized to unity, we have:

$$\omega_1 = 1.9086, \quad \zeta_1 = 0.7441; \quad \omega_2 = 1.6768, \quad \zeta_2 = 0.9720$$

This 4th-order Gaussian LPF is implemented with switched capacitor filters. The reason for using this scheme is that the LPF's 3dB bandwidth can be controlled by an external clock which allows generating GMSK signals with different BTb. To realize a 4th-order LPF, two stages of LMF100 are cascaded and operated at mode-3[5]. Figure 5 shows the circuit diagram for this mode.

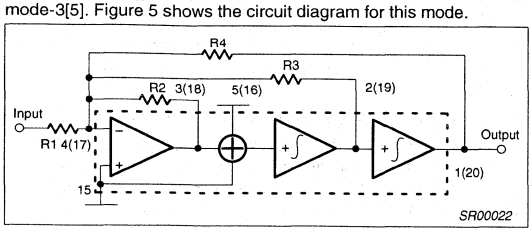


Figure 5. Circuit Diagram of LPF with LMF100 at Mode-3

For mode-3 LPF applications, the following formulas can be used to calculate the resistor values [5]:

$$H_{LP}(s) = \frac{H_{OLP}\omega_0}{S^2 + S\omega_0/Q + \omega_0} \quad \text{(EQ. 4)}$$

where, $H_{OLP} = -\frac{R_4}{R_1}$ (EQ. 5)

$$\omega_0 = \left(\frac{f_{CLK}}{100}\right) \cdot \sqrt{\frac{R_2}{R_4}} \quad \text{(EQ. 6)}$$

$$Q = \left(\frac{R_3}{R_2}\right) \cdot \frac{\sqrt{R_2}}{R_4} \quad \text{(EQ. 7)}$$

Example:

Step 1. Decide the gain and choose R value:
For unity gain, we have
$H_{OLP} = -R_4/R_1 = -1$, i.e. $R_4 = R_1$.
For the first stage, we choose a convenient value for input resistance: $R_{14} = R_{11} = 22k\Omega$

Step 2. Calculate R_{12}:
Compare (3) with (4), we have:

$$\omega_1 = \left(\frac{f_{CLK}}{100}\right) \cdot \sqrt{\frac{R_{12}}{R_{14}}} \quad \text{(EQ. 8)}$$

By choosing f_{clk} = 100 times the 3dB bandwidth, we have

$$\omega_1 = \sqrt{\frac{R_{12}}{R_{14}}} \rightarrow R_{12} = 80.14k\Omega$$

Step 3. Calculate R_{13}:
From the comparison of (3) and (4), we also have,

$$Q_1 = \frac{1}{(2\zeta_1)} = \left(\frac{R_{13}}{R_{12}}\right) \cdot \sqrt{\frac{R_{12}}{R_{14}}} = \frac{1}{(2 \cdot 0.7441)} \quad \text{(EQ. 9)}$$

$R_{13} = 28.22k\Omega$

For the second stage, the resistor values can be calculated by the same procedures. For this example, they are:

$R_{24} = R_{21} = 22k\Omega$
$R_{22} = 61.86k\Omega$
$R_{23} = 18.98k\Omega$

To obtain a good Gaussian LPF, the resistor values have to be adjusted with all input/output circuits connected. Baseband eye-diagrams and modulated power spectrum could be the references for the adjustment. The final values for this example are shown in the circuit diagram.

FM/IF System

The Philips low-voltage high performance monolithic FM/IF system, SA626, is employed for demodulation on the GMSK/GFSK demoboard. SA626 was designed specially for wide bandwidth portable communications applications, incorporating with a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, and audio and RSSI op amps. The RF section is similar to the famous SA605. The audio and RSSI outputs have amplifiers. With power down mode, SA626 will function down to 2.7V. Figure 6 is the block diagram of SA626. Detailed information can be found in the data book and application note [1, 2, 3].

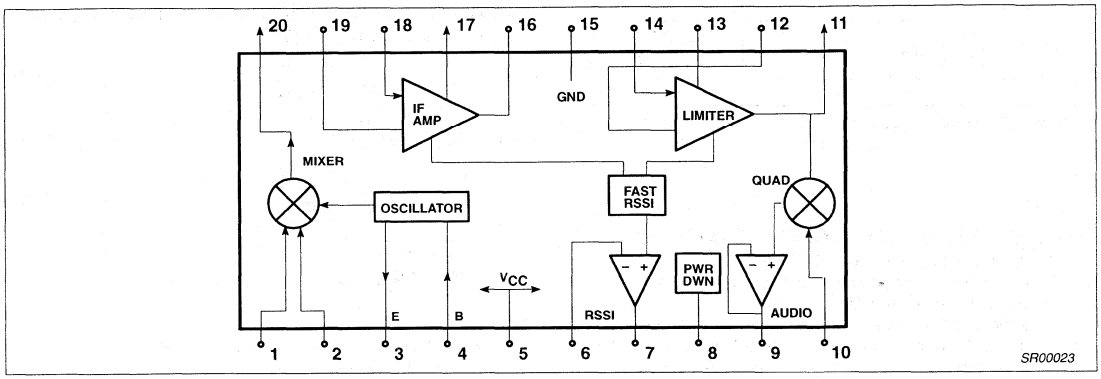


Figure 6. Block Diagram of the FM/IF System SA626

The GMSK/GFSK demoboard is designed for an RF frequency of 45MHz, LO frequency of 55.7 MHz, and intermediate frequency of 10.7MHz. For different RF frequency applications, the step-by-step matching circuits design procedure is presented in Ref. 1.

Although this demoboard is designed with SA626 based on CT-2 specifications, Philips also provides FM/IF solutions for many other GMSK/GFSK systems. SA626 is specially designed for wide bandwidth applications. For lower data rate applications such as CDPD (19.2 kb/s), SA605/625 family is recommended. For DECT and other high data rate applications, SA636 and SA639 are the recommended solutions. Data (audio) output bandwidth is the main limiting factor for high data rate applications. Table 2 presents a summary of the major characteristics of Philips FM/IF systems. The suggested maximum data rate for each part is an approximation based on the baseband eye pattern. Higher data rate could be operated with some modifications or if more BER degradation is allowed.

Table 2. Major Characteristics of the FM/IF Systems

	NE602/604	NE605	NE625	NE626	NE636	NE639*
V_{CC}	4.5 - 8V	4.5 - 8V	4.5 - 8V	2.7 - 5.5V	2.7 - 5.5V	2.7 - 5.5V
I_{CC}	2.4/3.3mA @ 6V	5.7mA @ 6V	5.7mA @ 6V	6.5mA @ 3V	6.5mA @ 3V	8.3mA @ 3V
SINAD	-120dBm/.22µV (RF: 45MHz, IF: 455kHz, 1kHz tone, 8kHz Dev.)	-120dBm/.22µV (RF: 45MHz, IF: 455kHz, 1kHz tone, 8kHz Dev.)	-120dBm/.22µV (RF: 45MHz, IF: 455kHz, 1kHz tone, 8kHz Dev.)	-112dBm/.54µV (RF: 240MHz, IF: 10.7MHz, 1kHz tone, 70kHz Dev.)	-111dBm/.54µV (RF: 240MHz, IF: 10.7MHz, 1kHz tone, 125kHz Dev.)	-111dBm/.54µV (RF: 240MHz, IF: 10.7MHz, 576kHz tone, 288kHz Dev.)
Features	Audio & Data pins IF BW of 25MHz Matching for standard 455kHz IF filters	Audio & Data pins IF BW of 25MHz Matching for 455kHz IF filters	Pin compatible with NE605 Fast RSSI IF BW of 25MHz Matching for 455kHz IF filters	Power down mode Low voltage Fast RSSI IF BW of 25MHz Int. RSSI & Audio op amp Matching for 10.7MHz IF filters	Power down mode Low voltage Fast RSSI IF BW of 25MHz Int. RSSI op amp Wideband data out Matching for 10.7MHz IF filters	Power down mode Low voltage Fast RSSI IF BW of 25MHz Int. RSSI op amp Wideband data out Post detection amp Matching for 10.7MHz IF filters
Data Rate**	100kb/s	100kb/s	100kb/s	300kb/s	1.5Mb/s	2Mb/s
NOTES	* Objective specifications. ** Approximated maximum data rate. With some modifications, higher data rate might be operated.					

Threshold Detector and Data Regeneration

A 2-level threshold detector with sampling time adjustment circuits is implemented for data regeneration as shown in the circuit diagram. The output base band signal (eye-diagrams) from SA626 is first fed into a comparator (LM311) to generate a TTL logic signal which is then sampled with the data clock at the transmitting bit rate. The phase of the data clock can be adjusted manually through a monostable multivibrator (74HC123) to achieve the optimal sampling time. The demoboard is initially adjusted for a bit rate of 72 kb/s. If a different data rate is used, the sampling time has to be re-adjusted.

The symbol timing recovery (STR) circuit is not implemented on this demoboard. The transmitting data clock should be either hard-wire connected from the transmitter, or obtained from a separate STR circuit for operation. The measured performance presented in this paper is conducted with hard-wire connected data clock. However,

BER degradation caused by STR should be no more than 1dB (Ref 8.).

PERFORMANCE MEASUREMENTS

The performance of this GMSK/GFSK demoboard including receiver sensitivity and BER is experimentally evaluated. BER performance is evaluated based on CT-2 specifications. Measurement procedures and the measured results are presented in this section.

Measurement Set-up

Figure 7 illustrates the measurement set-up with the GMSK/GFSK demoboard. A data error analyzer is employed to generate a pseudo random binary sequence (PRBS) with length of 10^9 -1 at a data rate of 72kb/s. This data sequence is sent to the Gaussian LPF on the board for premodulation filtering. The output Gaussian filtered base band signal is then applied to an FM signal generator as the modulating signal. To generate a GMSK modulated signal (modulation index = 0.5) at a bit rate of 72kb/s, frequency deviation of the FM signal generator needs to be set at 18kHz. The output from the generator is then a GMSK modulated signal (at 45MHz). Another signal generator is employed to provide an LO signal at 55.7MHz for the FM/IF system detection.

After FM discriminator detection, the output base band signal is fed into another Gaussian LPF on the board to eliminate noise. The 3dB bandwidth of both Gaussian LPFs is controlled by an external clock. This clock should be a square wave signal with TTL level. By controlling the frequency of this clock, different BTb can be achieved for certain bit rate. To have BTb equal 0.5 with bit rate of 72kb/s, the clock signal is set at 3.6MHz (100 times the required 3dB bandwidth). The output from the LPF is then sent to the threshold detector for data regeneration. The data clock signal is taken directly from the data error analyzer. The sampling time can be controlled by adjusting VR2 in the circuit diagram. The recovered data sequence is fed back to the Data Error Analyzer for BER measurement.

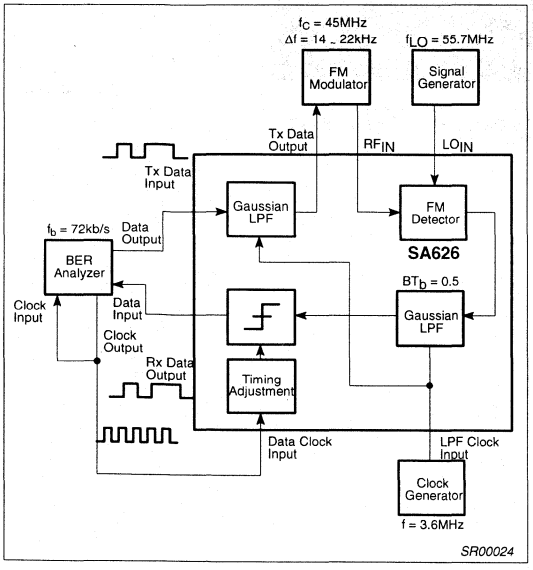


Figure 7. Measurement Set-Up with the GMSK/GFSK Board

Measurement Procedure and Results

1. **Measure SINAD at the audio output of SA626:** use the same set-up as described above, but set RF = 45MHz, fm = 1kHz, Δf = 8kHz; LO = 55.7MHz, -10dBm; the measured typical sensitivity for 12dB SINAD should be about -110dBm. (See Ref 1. for detailed SINAD measurement.)
2. **Check "LPF clock input":** this clock should be a TTL level signal with the frequency of 100 times the desired 3dB bandwidth of the LPF. For the data rate of 72kb/s and BTb = 0.5 LPF, the clock frequency is 3.6MHz (100 × 36kHz).
3. **Check "Tx data input":** 72kb/s baseband NRZ signal.
4. **Measure "Tx data output":** Gaussian low-pass filtered baseband eye-diagram as shown in Figure 8.
5. **Check "data clock input":** 72kHz clock signal.
6. **Adjust sampling position:** by adjusting VR2, set the rising edge of the clock at Pin 11 of Unit 4 (74HC74) to be at the center of the eye-diagram at Pin 2 of Unit 6 (LM311) in the circuit diagram.
7. **Measure BER with high RF level:** set RF input signal level at -80dBm and -90dBm, LO signal level at -10dBm: error free.
8. **Measure BER vs. RF input level curve:** RF level: -94 ~ -104 dBm, LO level: -10dBm, at each point, at least 100 errors have to be measured. Figure 9 presents the measured BER as a reference.

QUESTIONS & ANSWERS

Q. For the SINAD measurement, is it necessary to connect the whole system?

A. Even though only part of the system is used to measure SINAD, it is recommended to connect the whole system because the RF part should be tested under the operating conditions.

Q. Why is the DC current (I_{CC}) very large when I measure the SINAD on SA626?

A. Check the power supplies. Make sure both +5V and -5V are connected all the time even though only +5V is needed for SA626.

Q. Is it possible that SINAD is good, but BER is not good?

A. Yes, because there are other factors affecting BER .

Q. Is it possible that SINAD is bad, but BER is good?

A. No. Good SINAD is a necessary condition to achieve good BER.

Q. What are the main factors affecting BER?

A. They are:

1. Tx LPF
2. FM deviation and RF signal level
3. RF part sensitivity
4. Rx LPF
5. Threshold detector
6. Sampling time

Q. There are two "Rx Data Output" ports. Which one should be used?

A. Two "Rx Data Output" ports are designed to provide convenience for different measurement conditions. Either one can be used if the BER analyzer has the Q/$\overline{Q}$ detection capability.

Q. What needs to be done for higher RF frequency applications?

A. First, RF and LO input matching circuits have to be redesigned at the desired frequency. Second, the layout of RF and LO input circuits might also need to be re-designed. The inputs should be further away from each other and in different directions (not in parallel with each other) to provide better isolation.

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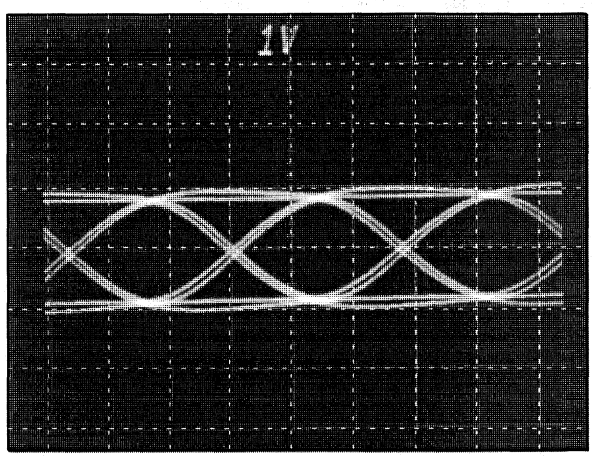


Figure 8. Baseband Eye-Diagram at the Output of Tx Gaussian LPF

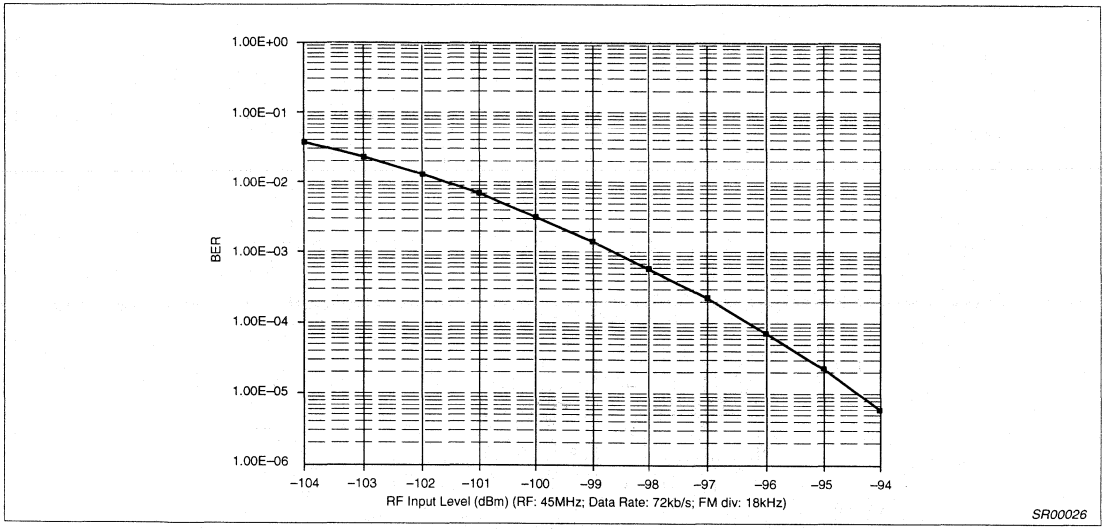


Figure 9. BER of the GMSK/GFSK Demoboard

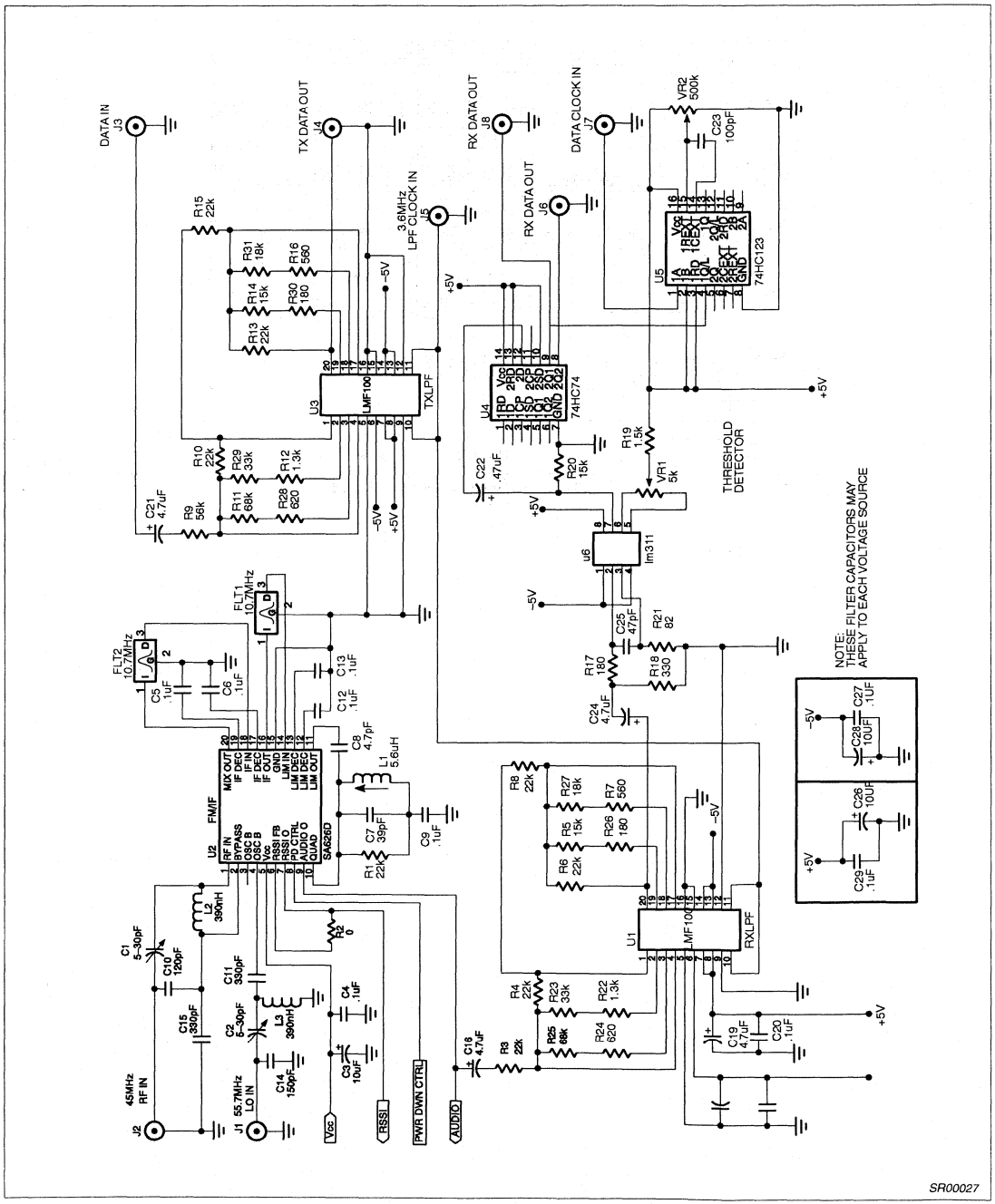


Figure 10. Circuit Diagram of the GMSK/GFSK Demoboard

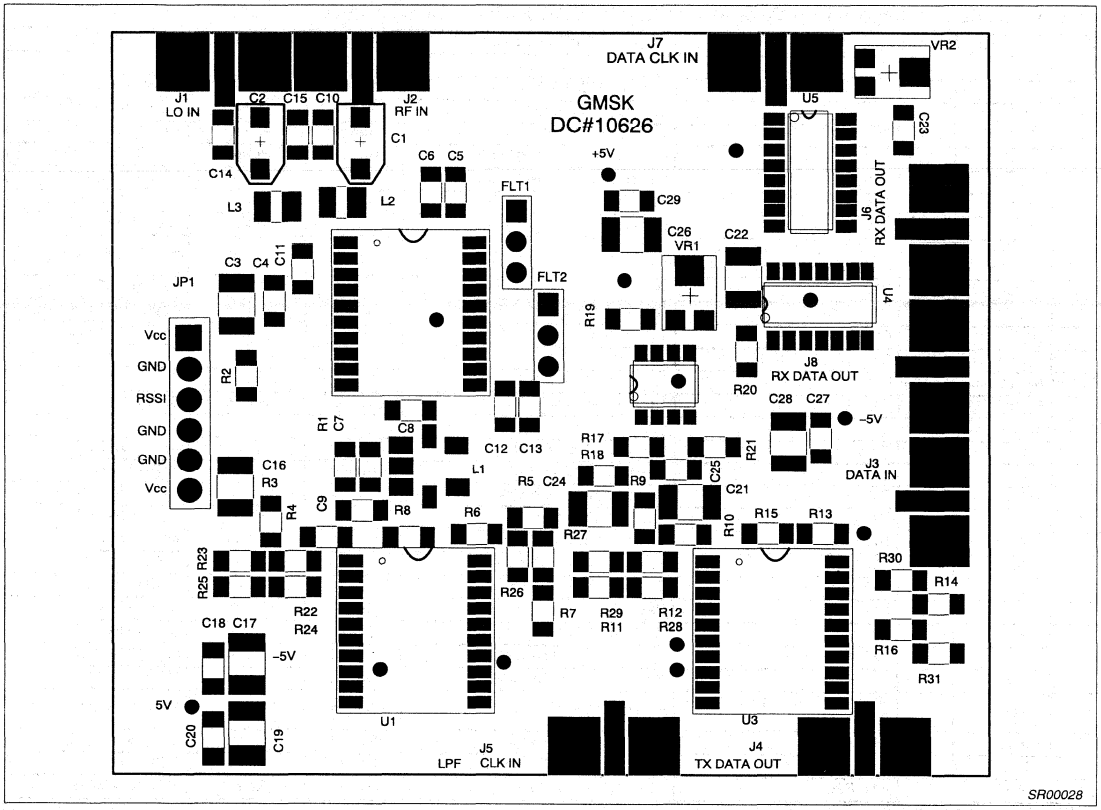


Figure 11. GMSK/GFSK Demoboard Components Layout

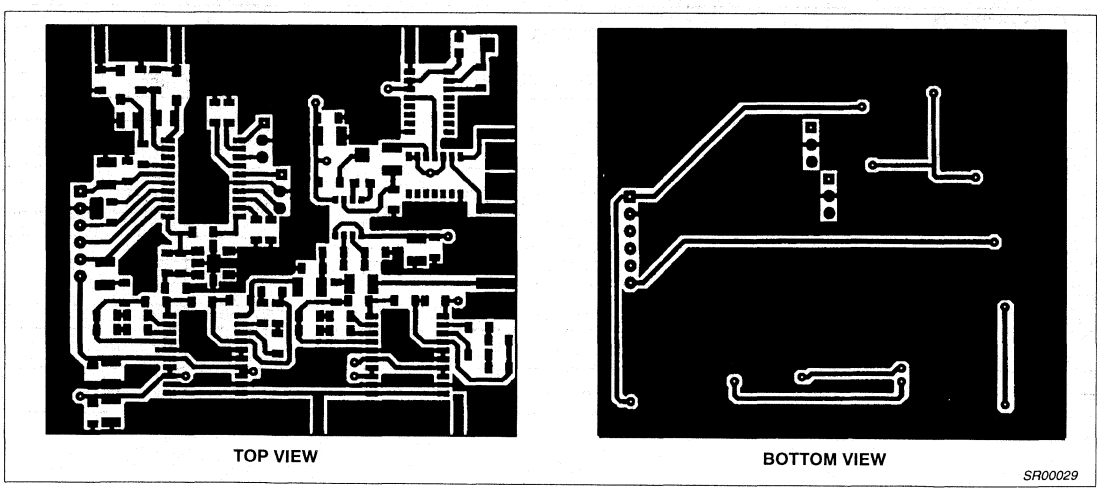


Figure 12. GMSK/GFSK Demoboard Layout

Table 3. Customer Application Component List for GMSK/GFSK Demoboard

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	4.7pF	50V	C8	Cap. cer. 1206 NPO ±0.25pF	Garrett	Rohm	MCH315A4R7CK
1	39pF	50V	C7	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A390JK
1	47pF	50V	C25	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A470JK
1	100pF	50V	C23	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG101J9BB0
1	120pF	50V	C10	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG121J9BB0
1	150pF	50V	C14	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG151J9BB0
2	330pF	50V	C11, C15	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG331J9BB0
8	0.1µF	50V	C4, C5, C6, C9, C12, C13, C18, C20	Cer. chip cap 1206 X7R ±10%	Garrett	Philips	1206R104K9BB0
1	0.47µF	35V	C22	Tant. chip cap B 3528 ±10%	Garrett	Philips	49MC474B035KOAS
3	4.7µF	10V	C16, C21, C24	Tant. chip cap B 3528 ±10%	Garrett	Philips	49MC475B010KOAS
3	10µF	10V	C3, C17, C19	Tant. chip cap B 3528 ±10%	Jaco	AVX	TAJB106K016R
	Option		C26, C27, C28, C29				
Surface Mount Variable Capacitors							
2	5-30pF		C1, C2	Trimmer capacitor	Kent Elect	Kyocera	CTZ3S-30C-W1
Surface Mount Resistors							
1	0Ω		R2	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW000E
1	82Ω		R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW820E
3	180Ω		R17, R26, R30	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW181E
1	330Ω		R18	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW331E
2	560Ω		R7, R16	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW561E
2	620Ω		R24, R28	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW621E
2	1.3kΩ		R12, R22	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW132E
1	1.5kΩ		R19	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW152E
3	15kΩ		R5, R14, R20	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW153E
2	18kΩ		R27, R31	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW183E
1	20kΩ		R1	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW203E
7	22kΩ		R3, R4, R6, R8, R10, R13, R15	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW223E
2	33kΩ		R23, R29	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW333E
1	56kΩ		R9	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW563E
1	68kΩ		R11, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW683E
Surface Mount Variable Resistors							
1	5kΩ		VR1	SM RES TRIM, 1 TRN ±20% J-H	Garrett	Philips	ST-4TA502
1	500kΩ		VR2	SM RES TRIM, 1 TRN ±20% J-H	Garrett	Philips	ST-4TA504
Surface Mount Inductors							
2	0.39µH		L2, L3	Chip Inductors-1800CS series	Coilcraft	Coilcraft	1800CS-391
Surface Mount Variable Inductors							
1	5.6µH		L1	Adjustable SM Inductor 5CCD type	Digikey	TOKO	TKS2251
Filters							
2	10.7MHz		FLT1, FLT2	10.7MHz IF filter 110kHz±30kHz	Murata	Murata	SFE10.7MHY-A
Surface Mount Integrated Circuits							
2			U1, U3	Switched capacitor filter	Hamilton	National	LMF100CIWM
1			U2	Low voltage mixer FM IF high RSSI	Philips	Philips	SA626D
1			U4	Dual D-type flip-flop	Philips	Philips	74HC74
1			U5	Dual re-triggerable monostable	Philips	Philips	74HC123
1			U6	Voltage comparator	Philips	Philips	LM311
Miscellaneous							
8			J1, J2, J3, J4, J5, J6, J7, J8	SMA gold connector	Newark	EF Johnson	142-0701-801
1			JP1	6-pins header straight	Mouser	Molex-Waldem	538-22-05-2061
1				Printed circuit board	Philips	Philips	GMSK/DC#10626
78 Total Parts							

High performance low power mixer FM IF system with high-speed RSSI

NE/SA627

DESCRIPTION

The NE/SA627 has faster RSSI rise and fall times. The NE/SA627 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI) with fast rise and fall time, voltage regulator and frequency check/limiter out (–). The NE/SA627 also has an extra limiter output. This signal is buffered from the output of the limiter and provides a negative (–) limiter output. This can be used to provide a frequency check function. The NE/SA627 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 5.8mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Audio output - mutable
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA627 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

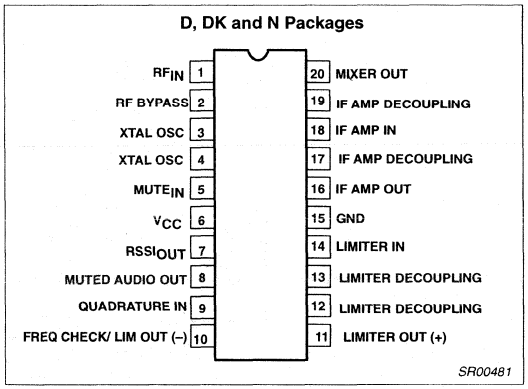


Figure 1. Pin Configuration

APPLICATIONS

- Digital cellular base stations
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification
- Digital cordless telephones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE627N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	0 to +70°C	NE627D	SOT163-1
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE627DK	SOT266-1
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA627N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA627D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA627DK	SOT266-1

BLOCK DIAGRAM

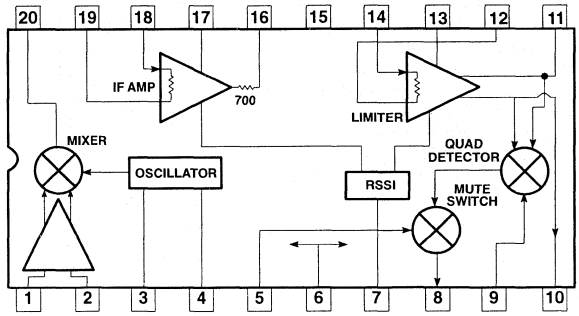


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range NE627		0 to +70	°C
	SA627		-40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W
		DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.8	6.7	4.55	5.8	6.75	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	IF RSSI output rise time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.2			1.2		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.1			1.1		µs
	IF RSSI output fall time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		2.1			2.1		µs
		RF level = -28dBm		7.6			7.6		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		2.0			2.0		µs
		RF level = -28dBm		7.3			7.3		µs
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		1.40	1.6		kΩ
	Limiter output impedance	Pin 10 or 11		300			300		Ω
	Limiter output level	Pin 10 or 11 with no load 3kΩ load (min)		280 250			280 250		mV_{RMS}

AC ELECTRICAL CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
IF section (continued)									
	Muted audio output resistance			58			58		kΩ
RF/IF section (int LO)									
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA627 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA627 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA627 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

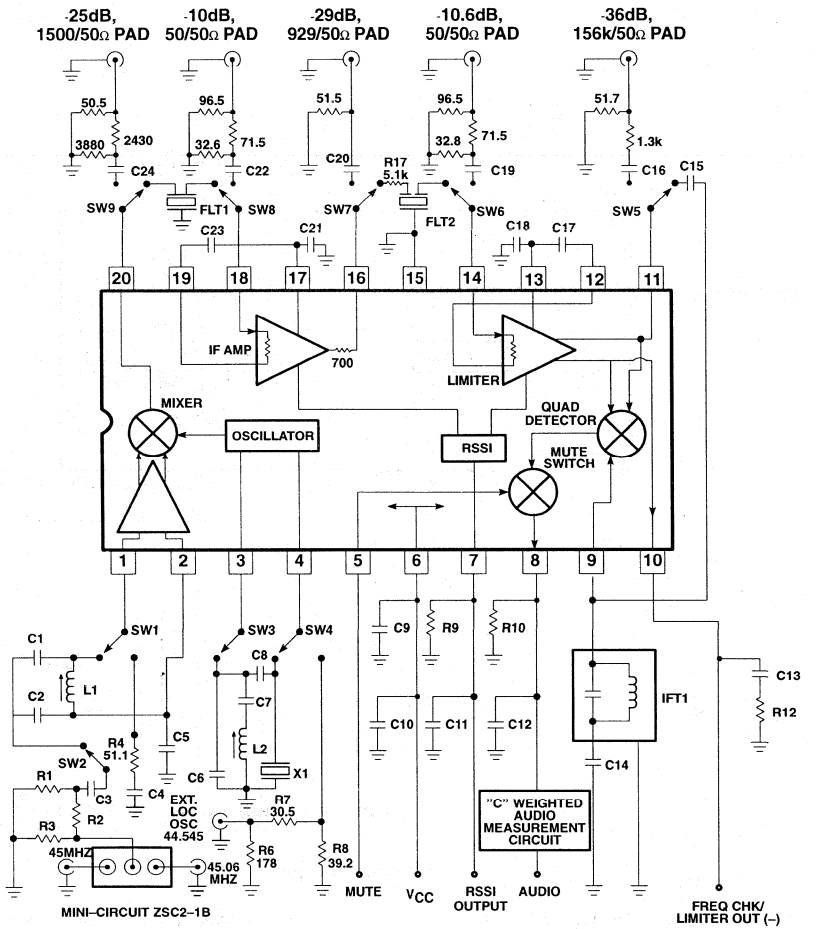
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



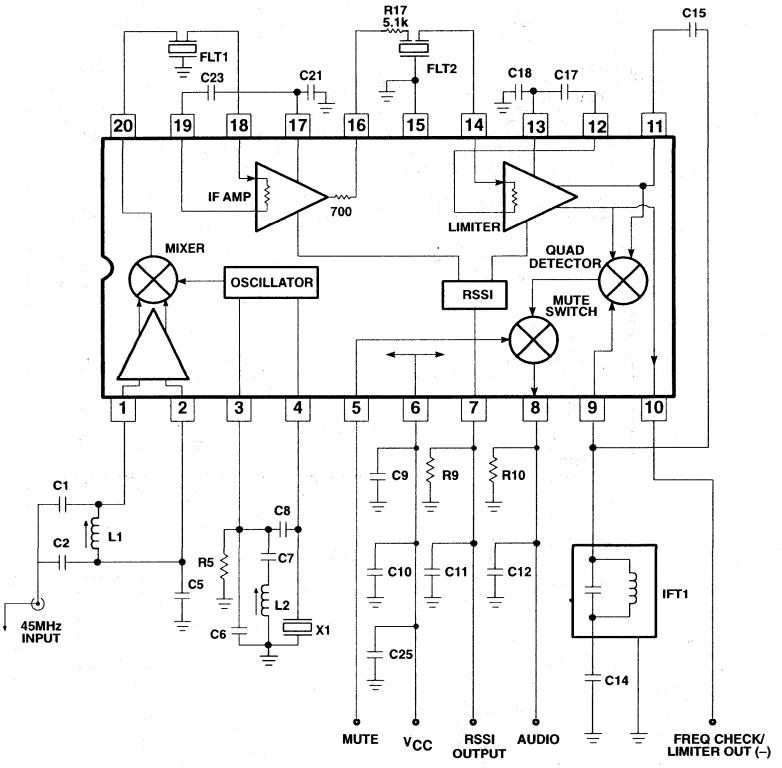
Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C9	100nF ±10% Monolithic Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C10	10μF Tantalum (minimum)	L2	0.8μH nominal Toko 292CNS–T1038Z
C11	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C12	15nF ±10% Ceramic	R9	100k ±1% 1/4W Metal Film
C13	0.1μF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C14	100nF ±10% Monolithic Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C15	10pF NPO Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R12	3kΩ ±5% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

*NOTE: This value can be reduced when a battery is the power source.

SR00483

Figure 3. NE/SA627 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

SR00484

Figure 4. NE/SA627 45MHz Application Circuit

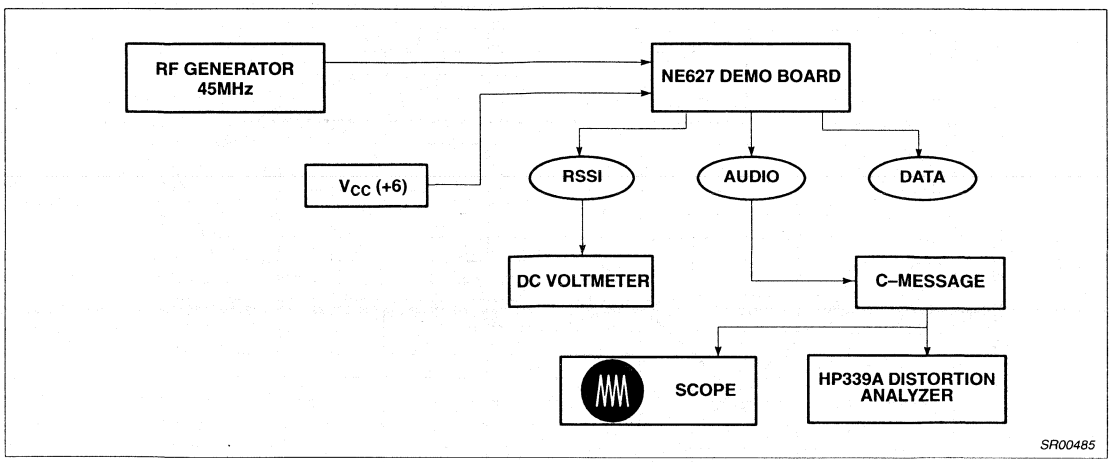


Figure 5. NE/SA627 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

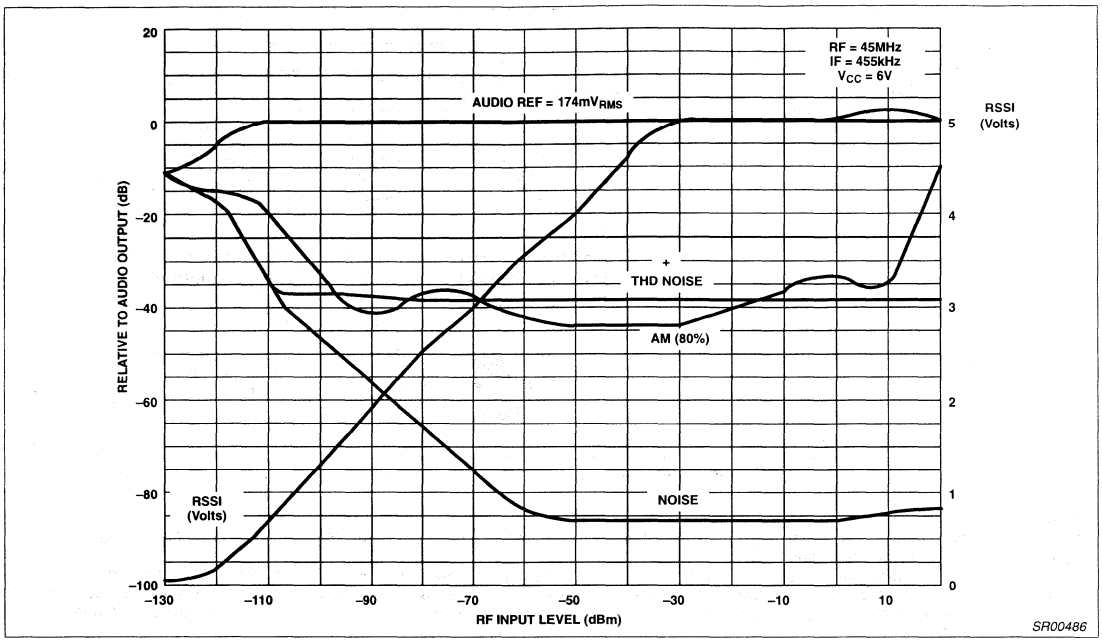


Figure 6. NE627 Application Board at 25°C

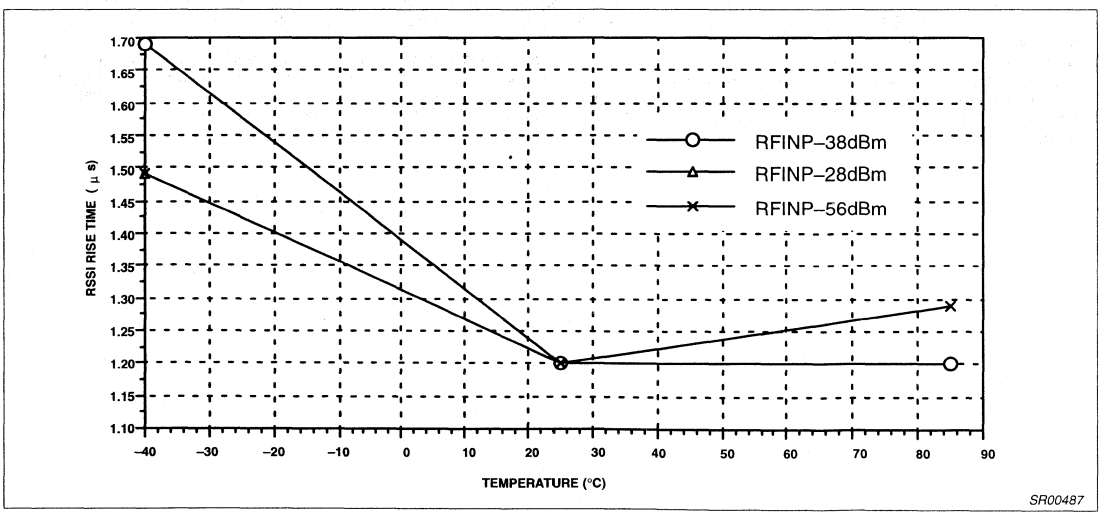


Figure 7. NE/SA627 Rise Time 455kHz IF Frequency

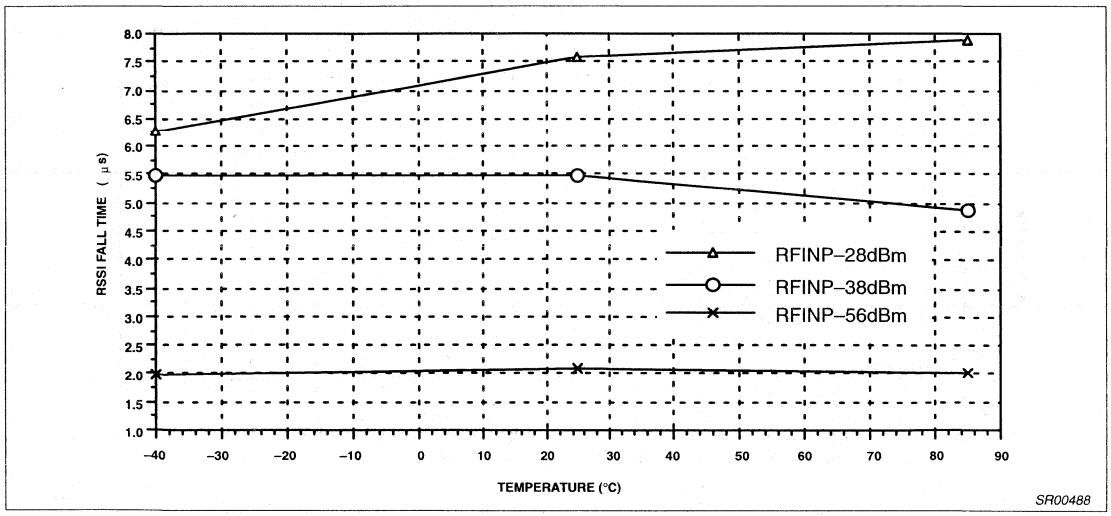


Figure 8. NE/SA627 Fall Time 455kHz IF Frequency

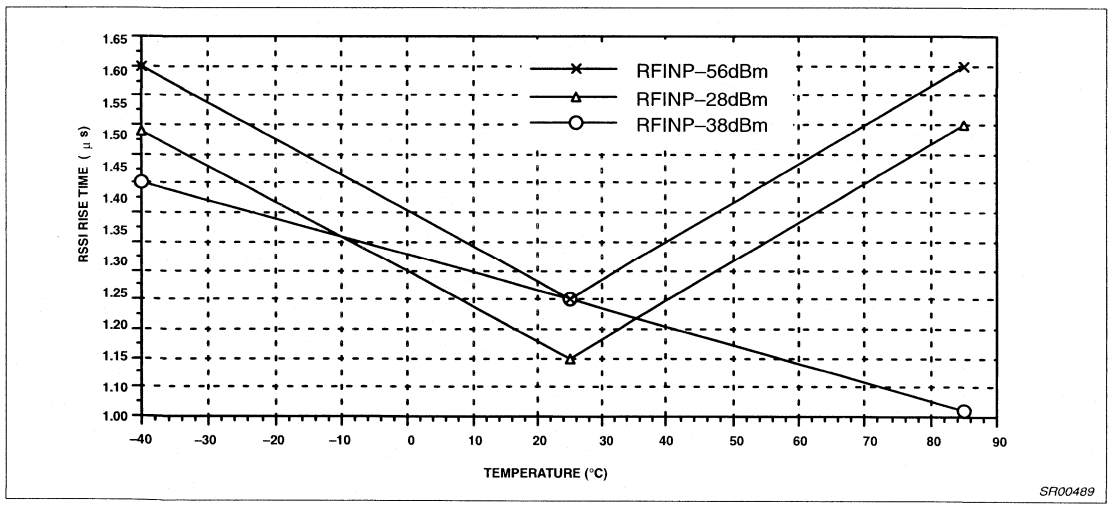


Figure 9. NE/SA627 Rise Time 10.7MHz IF Frequency

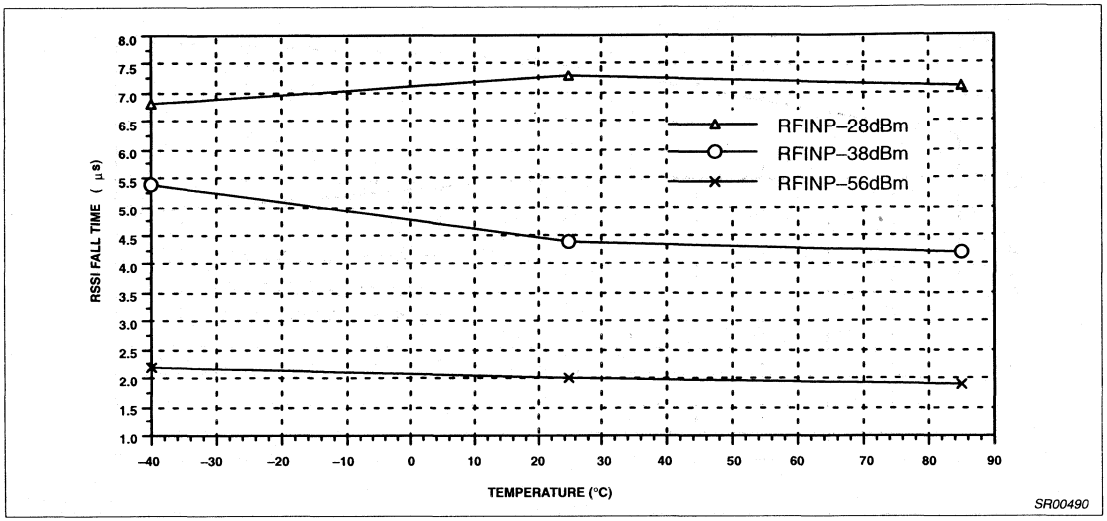


Figure 10. NE/SA627 Fall Time 10.7MHz IF Frequency

Low voltage high performance mixer FM IF system with high-speed RSSI

SA636

DESCRIPTION

The SA636 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator, wideband data output and fast RSSI op amps. The SA636 is available in 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The SA636 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The data output has a minimum bandwidth of 600kHz. This is designed to demodulate wideband data. The RSSI output is amplified. The RSSI output has access to the feedback pin. This enables the designer to adjust the level of the outputs or add filtering.

SA636 incorporates a power down mode which powers down the device when Pin 8 is low. Power down logic levels are CMOS and TTL compatible with high input impedance.

APPLICATIONS

- DECT (Digital European Cordless Telephone)
- Digital cordless telephones
- Digital cellular telephones
- Portable high performance communications receivers
- Single conversion VHF/UHF receivers
- FSK and ASK data receivers
- Wireless LANs

FEATURES

- Wideband data output (600kHz min.)
- Fast RSSI rise and fall times
- Low power consumption: 6.5mA typ at 3V
- Mixer input to >500MHz
- Mixer conversion power gain of 11dB at 240MHz
- Mixer noise figure of 12dB at 240MHz

PIN CONFIGURATION

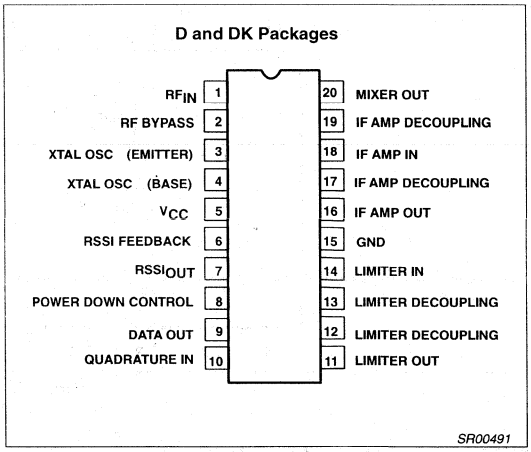


Figure 1. Pin Configuration

- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 92dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.54µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 240MHz and IF at 10.7MHz
- ESD hardened
- 10.7MHz filter matching (330Ω)
- Power down mode (I_{CC} = 200µA)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA636D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA636DK	SOT266-1

Low voltage high performance mixer FM IF system with high-speed RSSI

SA636

BLOCK DIAGRAM

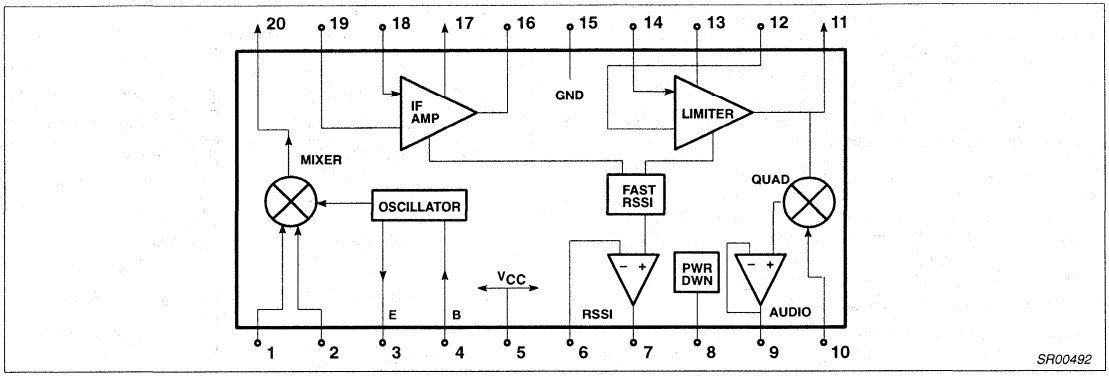


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	0.3 to 7	V
V_{IN}	Voltage applied to any other pin	–0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA636	–40 to +85	°C

NOTE: θ_{JA}, Thermal impedance D package 90°C/W
DK package 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

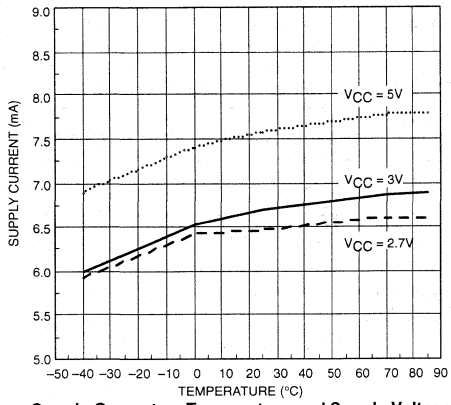
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA636			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7	3.0	5.5	V
I_{CC}	DC current drain	Pin 8 = HIGH	5.5	6.5	7.5	mA
	Input current	Pin 8 LOW	–10		10	µA
		Pin 8 HIGH	–10		10	
	Input level	Pin 8 LOW	0		0.3V_{CC}	V
		Pin 8 HIGH	0.7V_{CC}		V_{CC}	
I_{CC}	Standby	Pin 8 = LOW		0.2	0.5	mA
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

AC ELECTRICAL CHARACTERISTICS

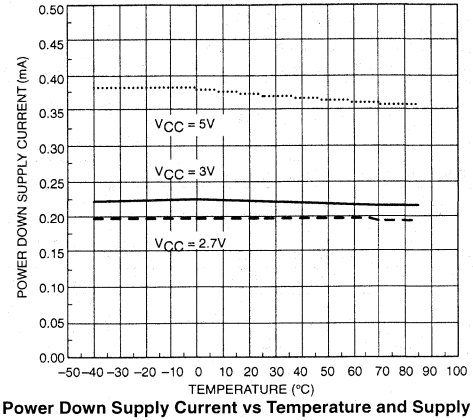
T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 240.05MHz + 14.5dBV RF input step-up; IF frequency = 10.7MHz; RF level = -45dBm; FM modulation = 1kHz with ±125kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA636 MIN	LIMITS SA636 TYP	LIMITS SA636 MAX	UNITS
Mixer/Osc section (ext LO = 160mV$_{RMS}$)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	External oscillator (buffer)			500		MHz
	Noise figure at 240MHz			12		dB
	Third-order input intercept point	Matched f1=240.05; f2=240.35MHz		-16		dBm
	Conversion power gain	Matched 14.5dBV step-up	8	11	14	dB
	RF input resistance	Single-ended input		700		Ω
	RF input capacitance			3.5		pF
	Mixer output resistance	(Pin 20)		330		Ω
IF section						
	IF amp gain	330Ω load		38		dB
	Limiter gain	330Ω load		54		dB
	Input limiting -3dB	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		50		dB
	Data level	R_{LOAD} = 100kΩ	100	130		mV$_{RMS}$
	3dB data bandwidth		600	700		kHz
	SINAD sensitivity	RF level = -111dBm		16		dB
THD	Total harmonic distortion			-43	-38	dB
S/N	Signal-to-noise ratio	No modulation for noise		60		dB
	IF RSSI output with buffer	IF level = -118dBm		0.2	0.5	V
		IF level = -68dBm	0.3	0.6	1.0	V
		IF level = -10dBm	0.9	1.3	1.8	V
	IF RSSI output rise time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		1.2		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		1.1		µs
	IF RSSI output fall time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		2.0		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		7.3		µs
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance			330		Ω
	IF output impedance			330		Ω
	Limiter input impedance			330		Ω
	Limiter output impedance			300		Ω
	Limiter output level with no load			130		mV$_{RMS}$
RF/IF section (int LO)						
	System RSSI output	RF level = -10dBm		1.4		V
	System SINAD	RF level = -106dBm		12		dB

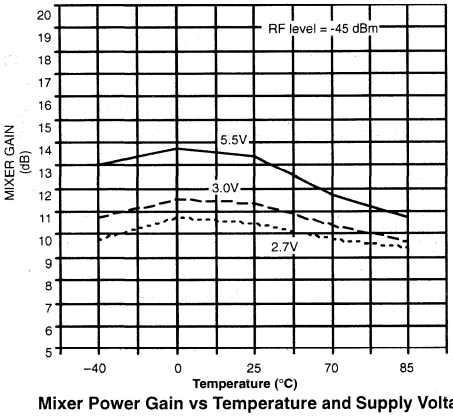
PERFORMANCE CHARACTERISTICS



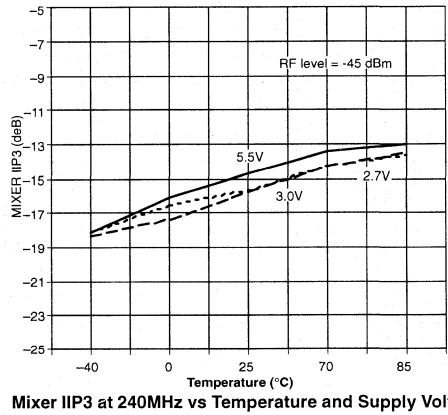
Supply Current vs Temperature and Supply Voltage



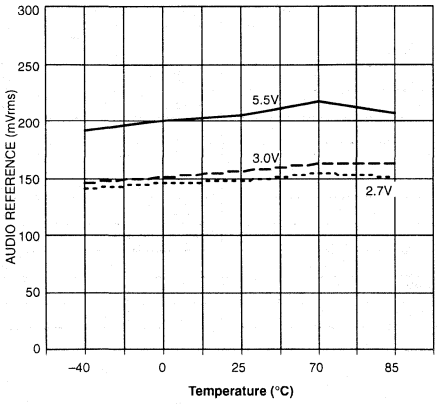
Power Down Supply Current vs Temperature and Supply Voltage



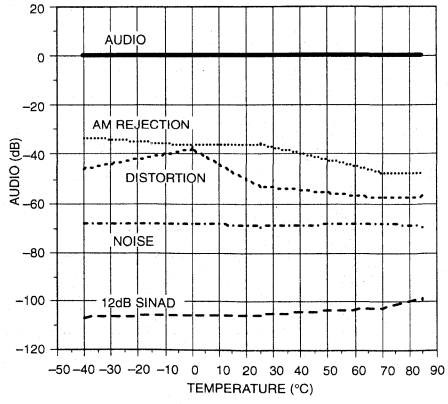
Mixer Power Gain vs Temperature and Supply Voltage



Mixer IIP3 at 240MHz vs Temperature and Supply Voltage



Audio Reference Level vs Temperature and Supply Voltage

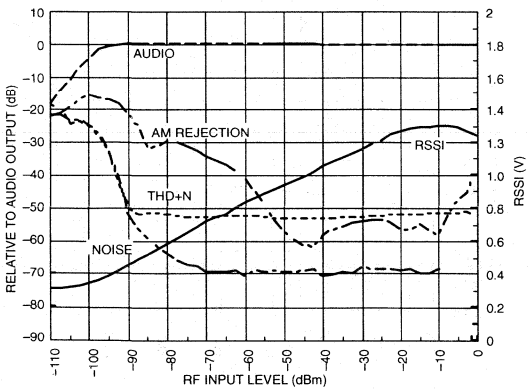


12dB SINAD and Relative Audio, THD, Noise and AM Rejection for VCC = 3V vs Temperature RF = 240MHz, Level = –68dBm, Deviation = 125kHz

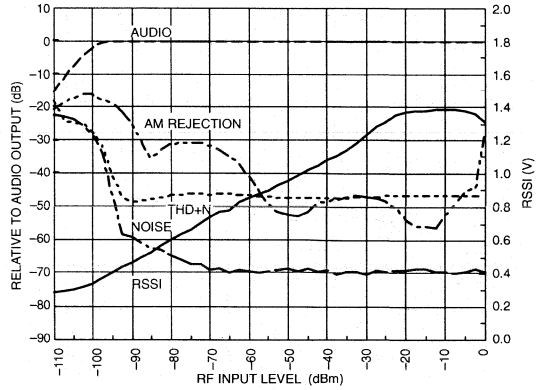
SR00493

Figure 3. Performance Characteristics

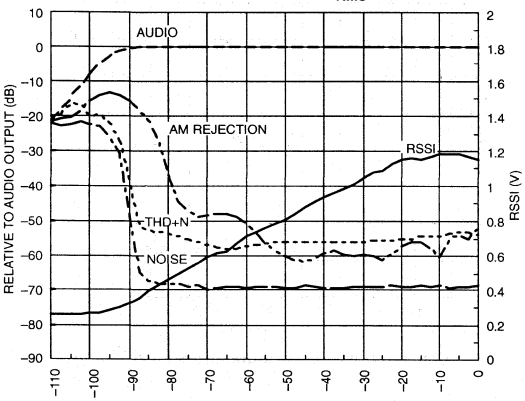
PERFORMANCE CHARACTERISTICS (continued)



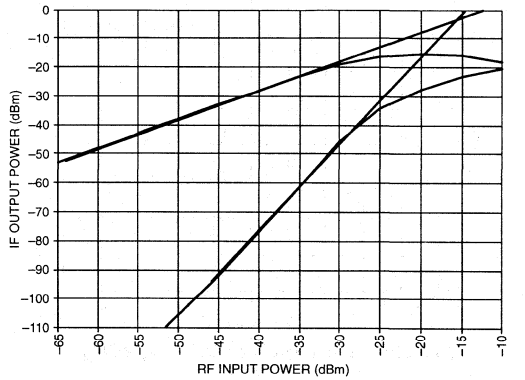
Receiver RF Performance — T = 25°C, Audio Level = 129mV$_{RMS}$



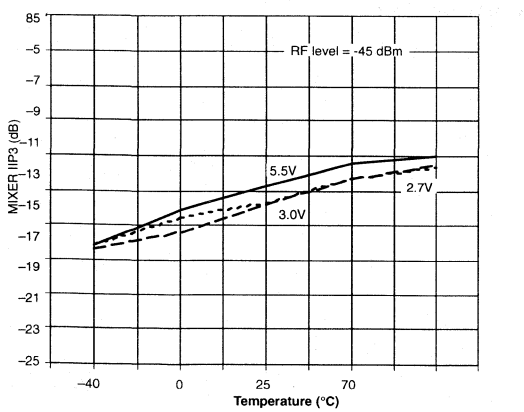
Receiver RF Performance — T = –40°C, Audio Level = 118mV$_{RMS}$



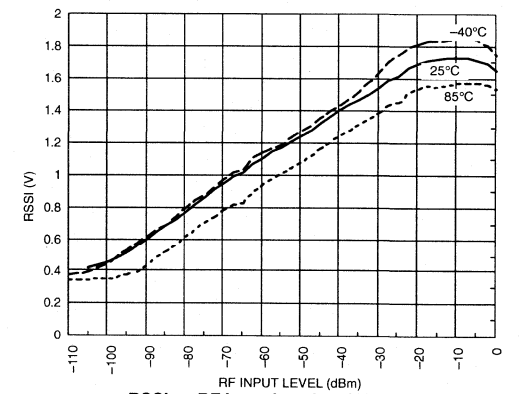
Receiver RF Performance – T = 85°C, Audio Level = 131mV$_{RMS}$



Mixer Third Order Intercept and Compression



Mixer IIP3 at 240MHz vs Temperature and Supply Voltage

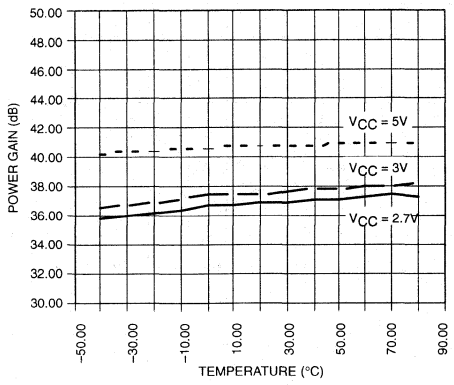


RSSI vs RF Input Level and Temperature

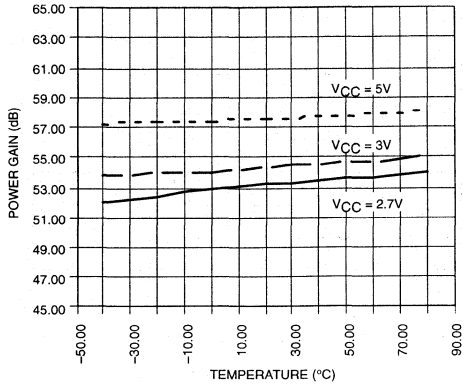
SR00494

Figure 4. Performance Characteristics

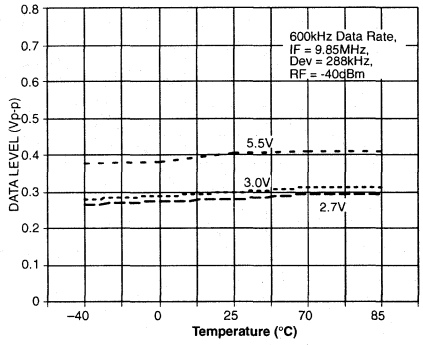
PERFORMANCE CHARACTERISTICS (continued)



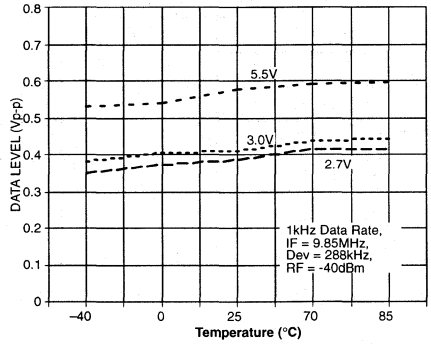
SA626 IF Amplifier Gain vs Temperature vs Supply Voltage



SA626 Limiting Amplifier Gain vs Temperature vs Supply Voltage



Data Level vs Temperature and Supply Voltage

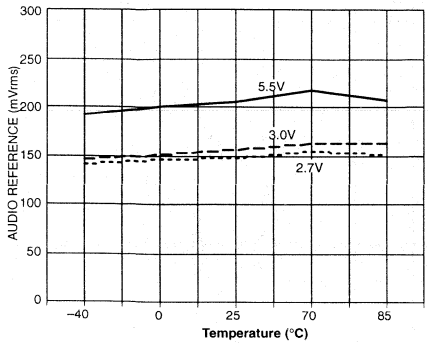


Data Level vs Temperature and Supply Voltage

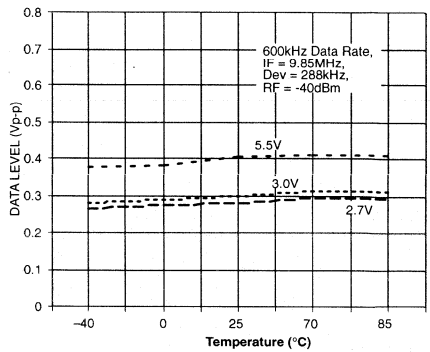
SR00495

Figure 5. Performance Characteristics

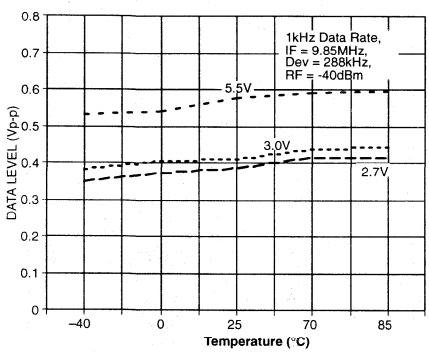
PERFORMANCE CHARACTERISTICS (continued)



Audio Reference Level vs Temperature and Supply Voltage



Data Level vs Temperature and Supply Voltage

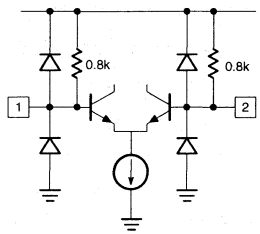
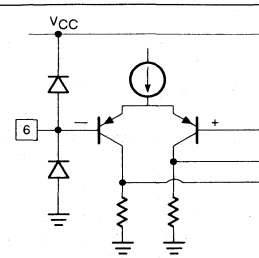
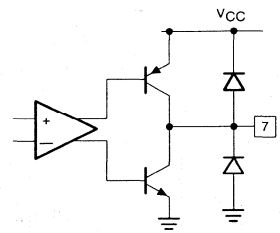
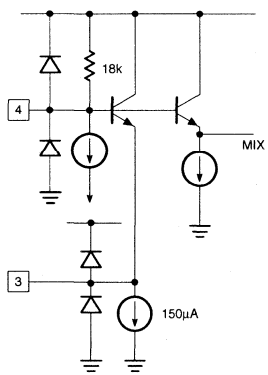
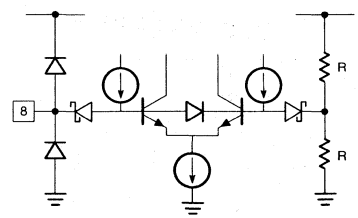
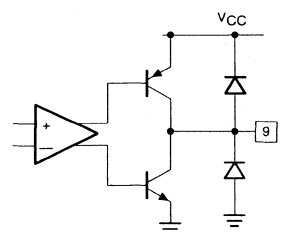
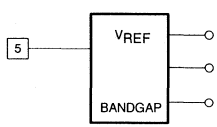
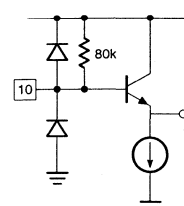


Data Level vs Temperature and Supply Voltage

SR00496

Figure 6. Performance Characteristics

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	+2.75	
4	XTAL OSC	+2.32		9	DATA OUT	+1.09	
5	VCC	+3.00		10	QUAD. IN	+3.00	

SR00497

Figure 7. Pin Functions

PIN FUNCTIONS (continued)

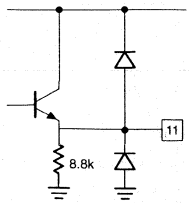
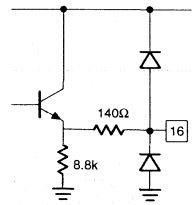
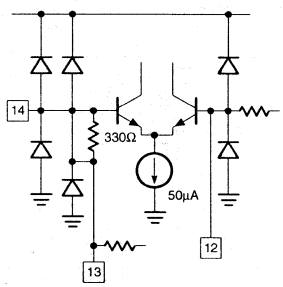
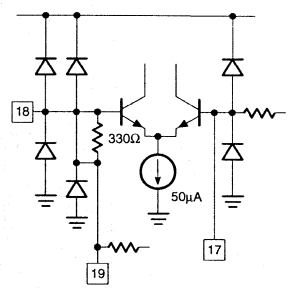
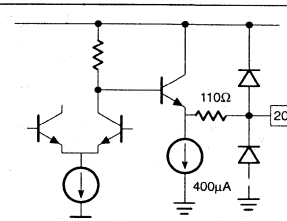
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	LIMITER OUT	+1.35		16	IF AMP OUT	+1.22	
12	LIMITER DECOUP	+1.23		17	IF AMP DECOUP	+1.22	
13	LIMITER COUPLING	+1.23		18	IF AMP IN	+1.22	
14	LIMITER IN	+1.23		19	IF AMP DECOUP	+1.22	
15	GND	0		20	MIXER OUT	+1.03	

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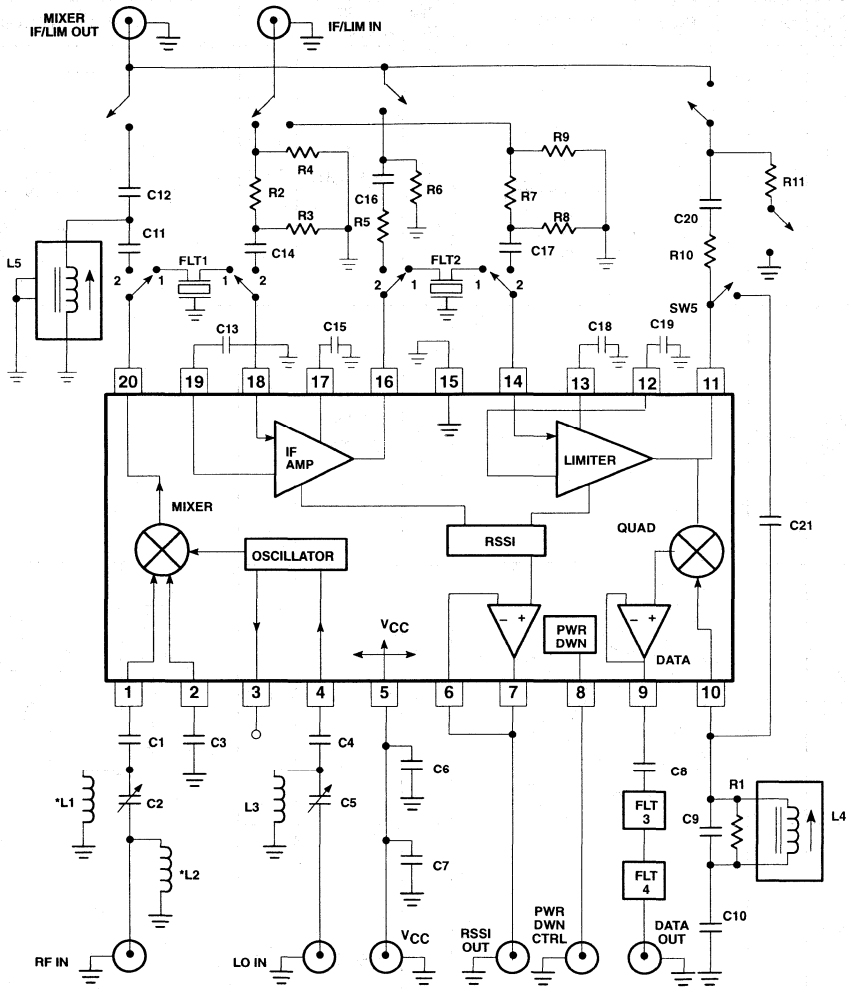
Figure 8. Pin Functions (cont.)



Automatic Test Circuit Component List

R1	8.2kΩ select	C1	0.1µF	C12	160pF select	L1	150nH select for input match
R2	6.42kΩ	C2	1–5pF select for input match	C13	1000pF	L2	22nH select for input match
R3	347.8Ω	C3	0.1µF	C14	0.1µF	L3	47nH select for input match
R4	49.9Ω	C4	0.1µF	C15	1000pF	L4	5.6µH select for input match
R5	1kΩ	C5	1–5pF select for input match	C16	0.1µF	L5	1.27–2.25µH select for mixer output match
R6	49.9Ω	C6	100pF	C17	0.1µF		
R7	6.42kΩ	*C7	6.8µF 10V	C18	1000pF	FLT1	10.7MHz (Murata SFE10.7MA5-A)
R8	347.8Ω	C8	1µF	C19	1000pF	FLT2	10.7MHz (Murata SFE10.7MA5-A)
R9	49.9Ω	C9	39pF select	C20	0.1µF	FLT3	"C" message weighted
R10	1kΩ	C10	0.1µF	C21	1pF	FLT4	Active de-emphasis
R11	49.9Ω	C11	0.1µF				

*NOTE: This value can be reduced when a battery is the power source.

SR00501

Figure 9. SA636 240.05MHz (RF) / 10.7MHz (IF) Test Circuit

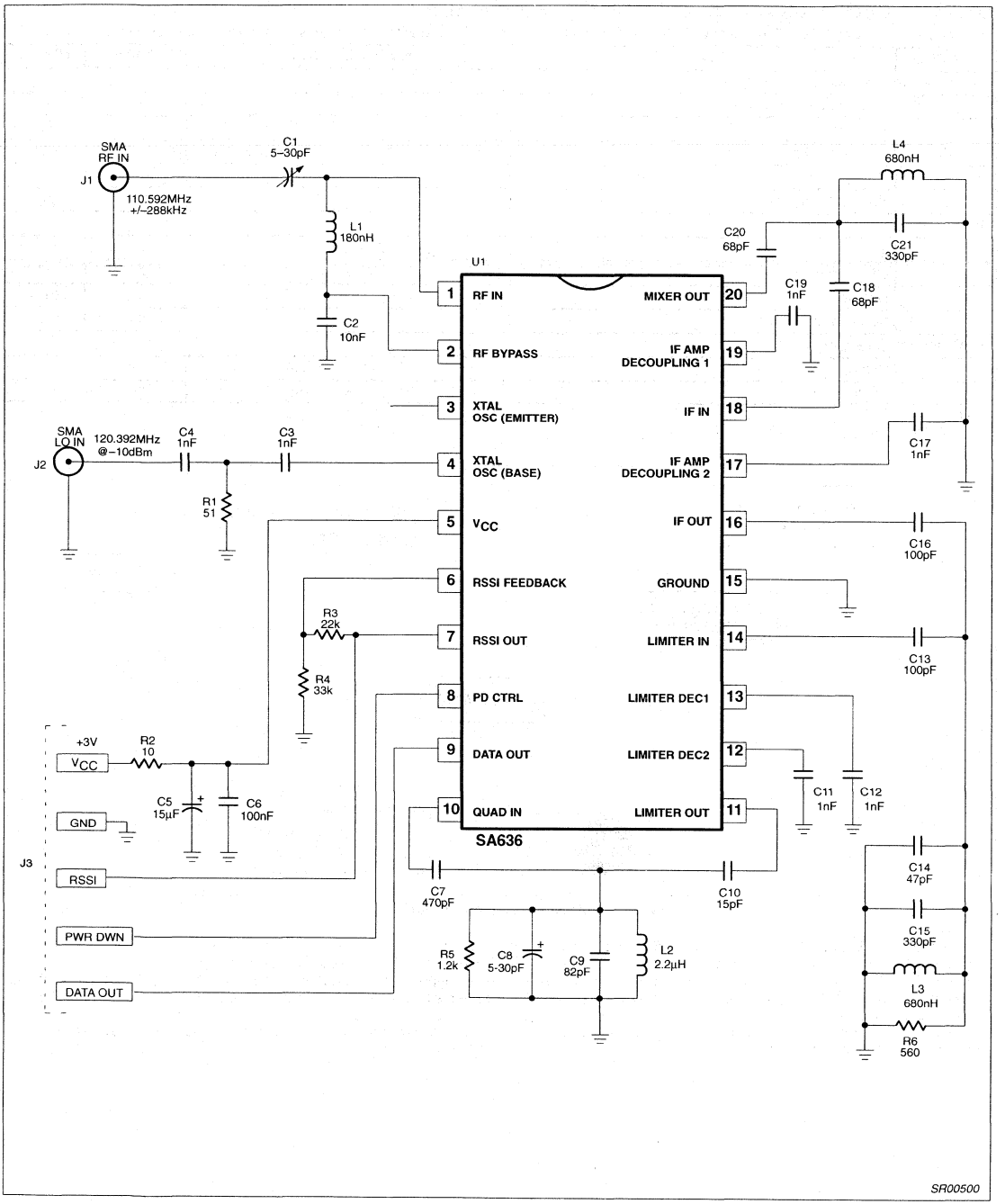


Figure 10. SA636 110.592MHz (RF) / 9.8MHz (IF) DECT Application Circuit

Table 1. DECT Application Circuit Electrical Characteristics

RF frequency = 110.592MHz; IF frequency = 9.8MHz; RF level = -45dBm; FM modulation = 100kHz with ±288kHz peak deviation.

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	UNITS
Mixer/Osc section (ext LO = 160mV$_{RMS}$)				
PG	Conversion power gain		13	dB
NF	Noise Figure at 110MHz		12	dB
IIP3	Third order input intercept	Matched f1 = 110.592; f2 = 110.892MHz	-15	dBm
R_{IN}	RF input resistance		690	Ω
C_{IN}	RF input capacitance		3.6	pF
IF section				
	IF amp gain	330Ω load	38	dB
	Limiter amp gain	330Ω load	54	dB
	Data level	R_{LOAD} = 3kΩ	130	mV$_{RMS}$
	3dB data bandwidth		700	kHz
RF/IF section (internal LO)				
	System RSSI output	RF level = -10dBm	1.4	V
	System S/N[1]	RF level = -83dBm	10	dB

NOTE:
1. 10dB S/N corresponds to BER = 10^{-3}.

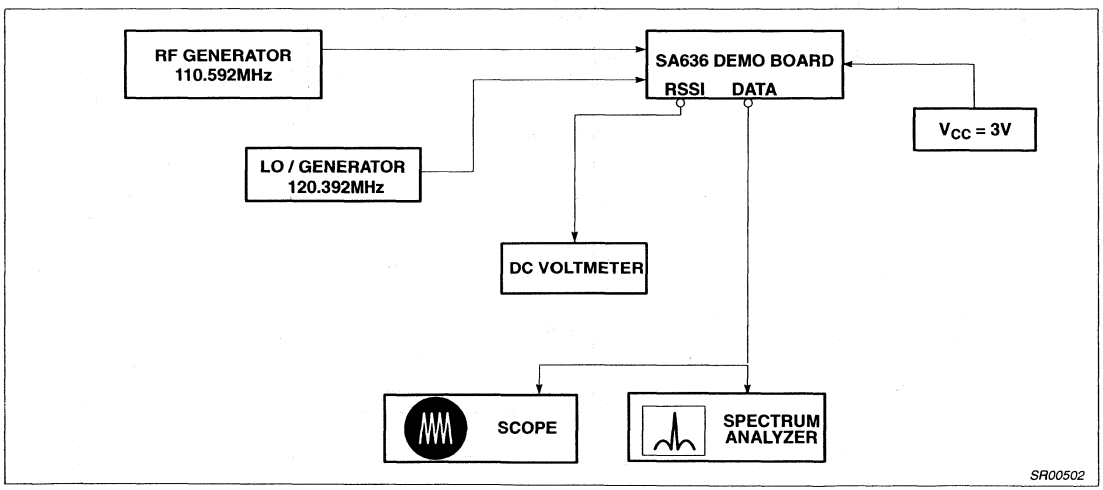
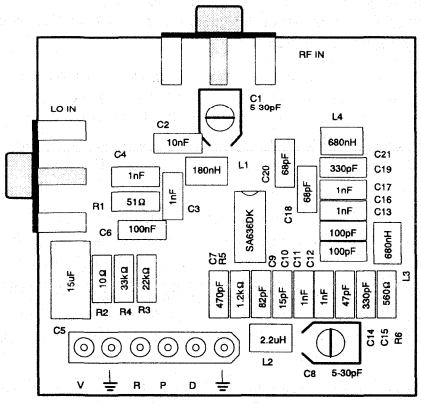
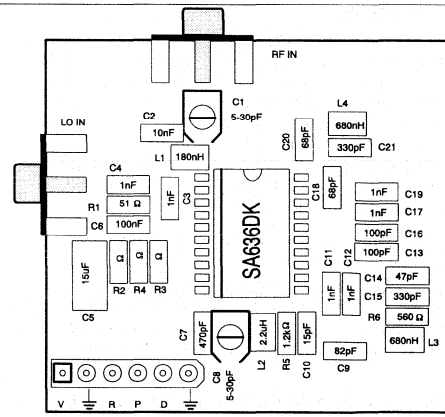


Figure 11. SA636 Application Circuit Test Set Up

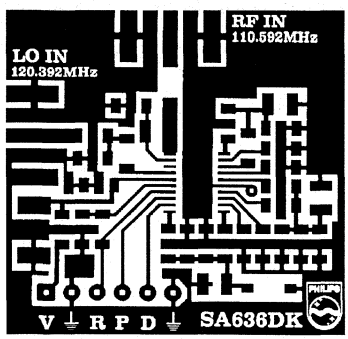
NOTES:
1. RF generator: Set your RF generator at 110.592MHz, use a 100kHz modulation frequency and a ±288kHz deviation.
2. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
3. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
4. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1µF bypass capacitor on the supply pin improves sensitivity.



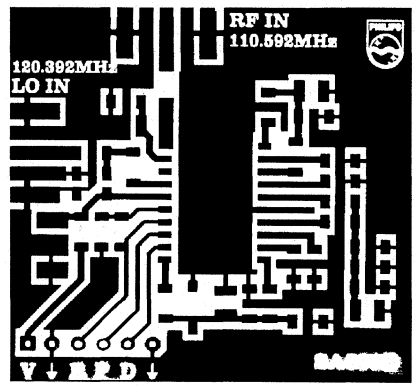
TOP SILK SCREEN (SSOP)



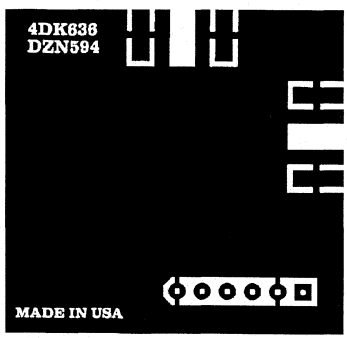
TOP SILK SCREEN (SOL)



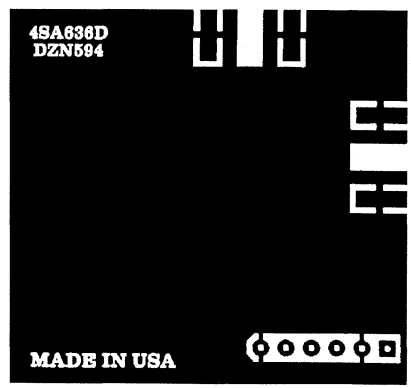
TOP VIEW (SSOP)



TOP VIEW (SOL)



BOTTOM VIEW (SSOP)



BOTTOM VIEW (SOL)

SR00503

Figure 12. SA636 Demoboard Layout (Not Actual Size)

CIRCUIT DESCRIPTION

The SA636 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 38dB of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 54dB of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 10.7MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as cordless and cellular hand-held phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 14dB, conversion gain of 11dB, and input third-order intercept of -16dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 10.7MHz ceramic filter for narrowband applications. The input resistance of the limiting IF amplifiers is also 330Ω. With most 10.7MHz ceramic filters and many crystal filters, no impedance matching network is necessary. For applications requiring wideband IF filtering, such as DECT, external LC filters are used (see Figure 10). To achieve optimum linearity of the log signal strength indicator, there must be a 6dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequency at 10.7MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output (DATA) of the quadrature is a voltage output. This output is designed to handle a minimum bandwidth of 600kHz. This is designed to demodulate wideband data, such as in DECT applications.

A Receive Signal Strength Indicator (RSSI) completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPS or TACS cellular telephone, DECT and RCR-28 cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

Low-voltage digital IF receiver SA637

DESCRIPTION

The SA637 is a low-voltage high performance monolithic digital system with high-speed RSSI incorporating a mixer, oscillator with buffered output, two limiting intermediate frequency amplifiers, fast logarithmic received signal strength indicator (RSSI), voltage regulator, RSSI op amp and power down pin. The SA637 is available in SSOP (shrink small outline package).

The SA637 was designed for portable digital communication applications and will function down to 2.7V. The limiter amplifier has differential outputs with 2MHz small signal bandwidth. The RSSI output has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

FEATURES

- V_{CC} = 2.7 to 5.5V
- Low power receiver (3.8mA @ 3V)
- Power down mode (I_{CC} = 110µA)
- Fast RSSI rise and fall times
- Extended RSSI range with temperature compensation
- RSSI op amp
- 2MHz limiter small signal bandwidth
- 455kHz filter matching (1.5kΩ)
- Differential limiter output

PIN CONFIGURATION

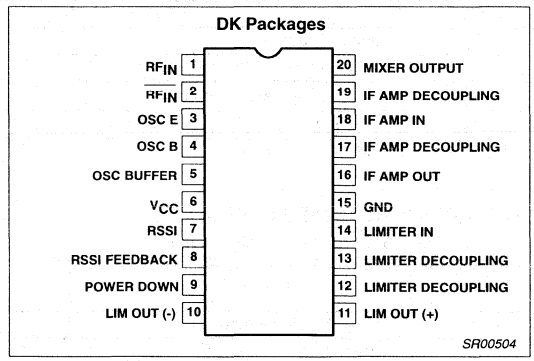


Figure 1. Pin Configuration

- Oscillator buffer
- SSOP-20 package

APPLICATIONS

- ADC (American Digital Cellular)
- Digital receiver systems
- Cellular radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA637DK	SOT266-1

BLOCK DIAGRAM

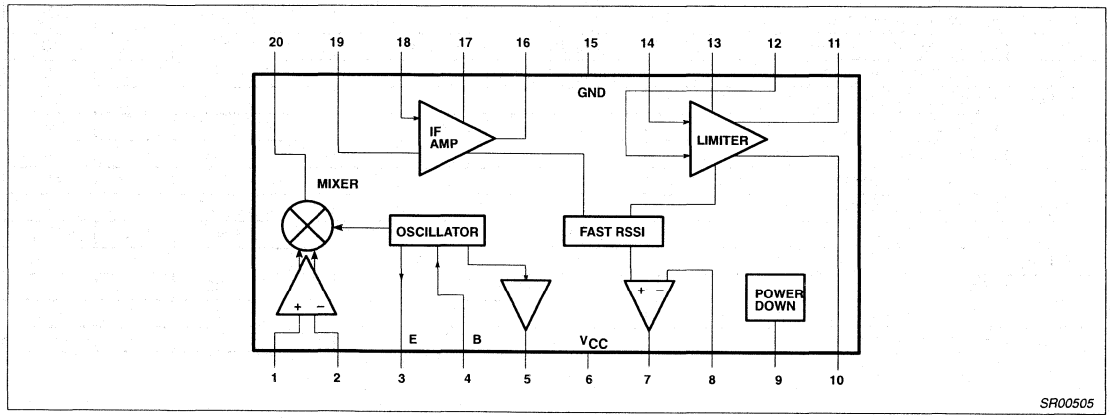


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		5.5	V
I_{CC}	DC current drain	Pin 9 = HIGH or OPEN		3.8	4.5	mA
		V_{CC} = 4.7V		4.4	5.5	mA
	Standby	Pin 9 = LOW		0.11	0.5	mA
	Input current	Pin 9 = LOW	-10		10	µA
		Pin 9 = HIGH	-10		10	
	Input level	Pin 9 = LOW	0		$0.3V_{CC}$	µA
		Pin 9 = HIGH	$0.7V_{CC}$		V_{CC}	
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 90MHz; RF input step-up = +14.5dBV; IF frequency = 455kHz; RF level = -68dBm. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section						
f_{IN}	Input signal frequency			200		MHz
f_{OSC}	Crystal oscillator frequency			200		MHz
NF	Noise figure at 90MHz	Matched input and output		6.2		dB
TOI	Third-order input intercept point	Input matched to 50Ω source		-17		dBm
P1dB	Input 1dB compression point			-27		dBm
	Conversion power gain	Matched 50Ω		7		dB
R_{IN}	Mixer input resistance			2.5		kΩ
C_{IN}	Mixer input capacitance			2.2		pF
R_{OUT}	Mixer output resistance			1.87		kΩ
	Buffered LO output level	LO = 447mV_{P-P}, 1kΩ AC load	100	300	500	mV_{P-P}
IF section						
	IF amp power gain	50Ω source		36		dB
	Limiter power gain	50Ω source		60		dB
IF_{BW}	IF amp bandwidth			2.5		MHz

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
	RF RSSI output	RF level = -118dBm	.01	0.2	.65	V
		RF level = -68dBm	.4	0.9	1.7	V
		RF level = -28dBm	1.0	1.7	2.3	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	RSSI ripple			30		mV_{P-P}
	RSSI speed Rise time	No interstage filter		2.5		µs
		With interstage filter		22		µs
	RSSI speed Fall time	No interstage filter		10		µs
		With interstage filter		50		µs
	IF input impedance			1.5		kΩ
	IF output impedance			1.5		kΩ
	Limiter input impedance			1.5		kΩ
	Limiter output impedance	(Pin 10, Pin 11)		200		Ω
	Limiter output signal level	(Pin 10, Pin 11) 1.5kΩ AC load		280		mV_{P-P}
	Limiter output DC level			1.27		V
	Differential output matching			±6		mV
	Differential output offset			±30		mV

CIRCUIT DESCRIPTION

Mixer

The mixer has a balanced input and is capable of being driven single-ended. The input impedance is 2.5kΩ in parallel with a 2.2pF cap at 90MHz RF. The mixer output can drive a 1500Ω ceramic filter at 455kHz or 600kHz directly without any matching required. The mixer conversion power gain is 7dB when both input and output are matched and optimum LO level is used to drive the internal mixer core.

Oscillator and Buffer

The on-board oscillator supplies the signal for the mixer down-conversion. The internally biased transistor can be configured as a Colpitts or Butler overtone crystal oscillator. The transistor's bias current can be increased if desired by adding a shunt resistor from Pin 3 to ground. The oscillator's buffered output (Pin 5) can be used as a feedback signal to lock the oscillator to an appropriate reference.

IF Amplifier and IF Limiter

The IF strip provides more than 95dB of power gain for the down converted signal. Its overall bandwidth is limited to 2MHz. The input and output impedance of the IF amplifier and the input impedance of the IF limiter are set to 1500Ω (match to 455kHz filter). A second filter is connected between the IF amplifier and the limiter for improved channel selectivity and reduced instability. This ceramic filter provides 3dB interstage insertion loss which results in optimal RSSI linearity. The overall gain can be reduced if desired by adding an external attenuator after the IF amplifier. The differential limiter outputs (Pins 10 and 11) are available for demodulator circuits.

RSSI

The received signal strength indicator provides a linear voltage indication of the received signal strength in dB for a range in excess of 90dB. The response time to a change in input signal is less than a few microseconds and the delay is kept to a minimum because of the use of a minimum phase shift circuit. Because of the speed of the RSSI circuit, the RSSI rise and fall time may, in practice, be dominated by the bandwidth of the external bandpass filter that is placed between the mixer and the IF, and the external filter placed between the IF amplifier and limiter. Since the RSSI function requires the signal to propagate through the whole IF strip, and the rise and fall time of the filters are inversely proportional to their bandwidth, there is a trade-off between channel selectivity and RSSI response. A possible solution is to use a second SA637 with wider band external filters for faster RSSI response.

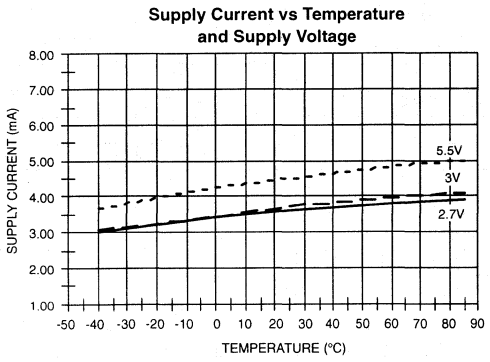
The RSSI curve is temperature compensated and in addition is designed for improved consistency from unit to unit.

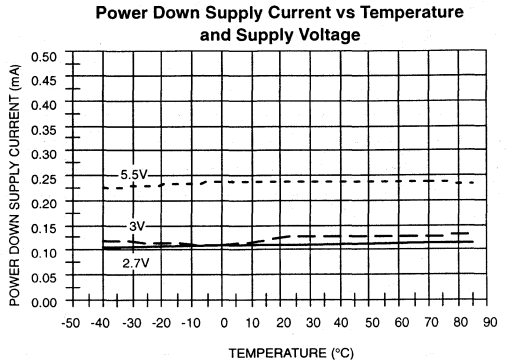
The RSSI circuit drives an on-chip low power op amp with rail-to-rail output which can be connected as a unity gain RSSI buffer or a gain stage or even a comparator.

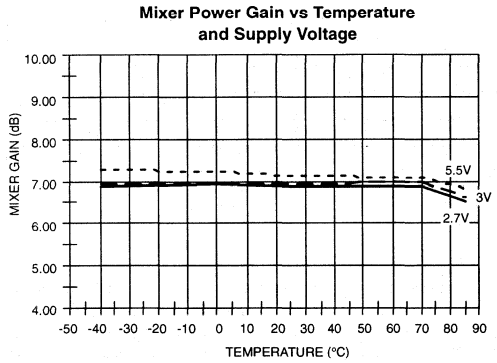
DC Power Supply

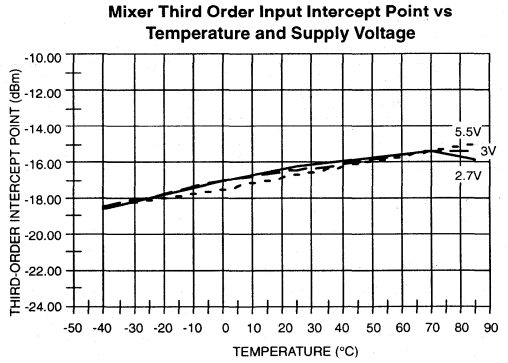
The IC is designed for operation between 2.7 and 5.5V. A power supply dependent biasing scheme is used in the mixers to benefit from the large headroom available at higher V_{CC}s.

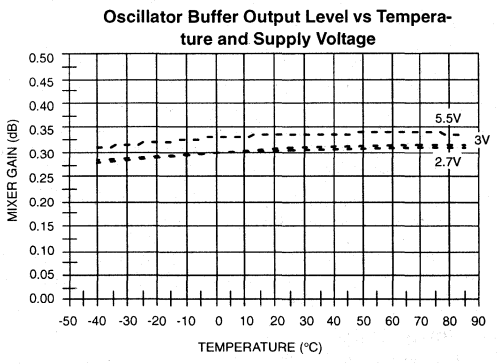
PERFORMANCE CHARACTERISTICS

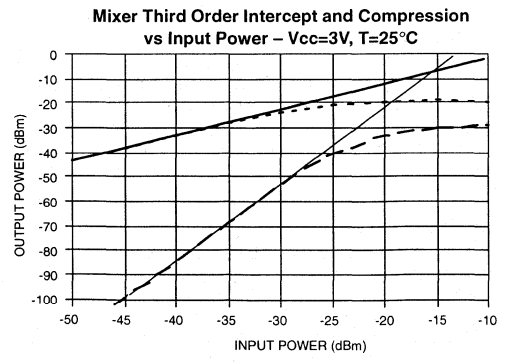












SR00506

Figure 3. Performance Characteristics

PERFORMANCE CHARACTERISTICS (cont.)

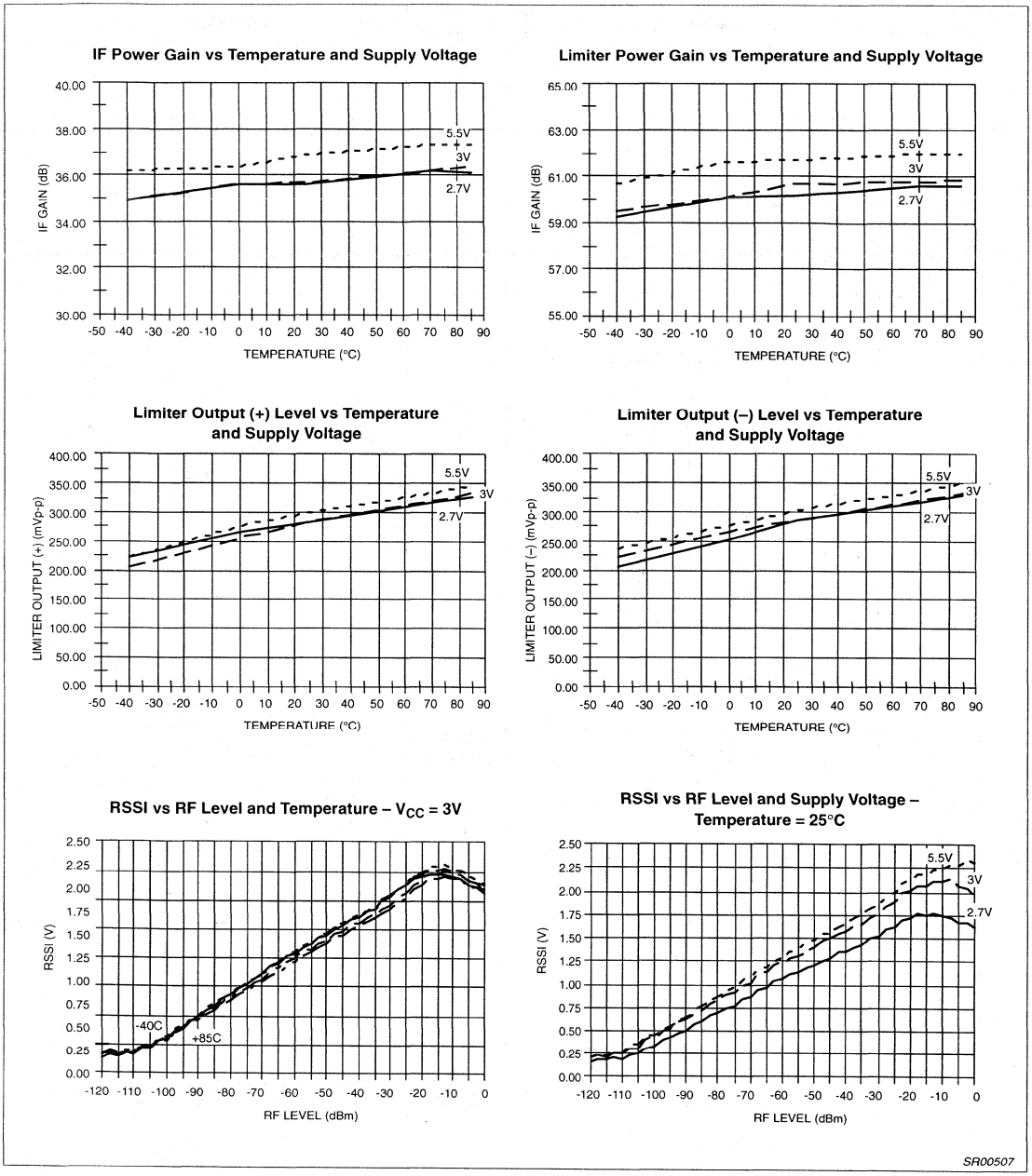
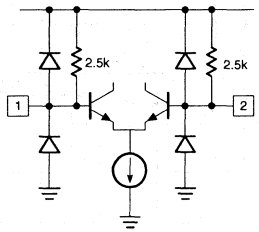
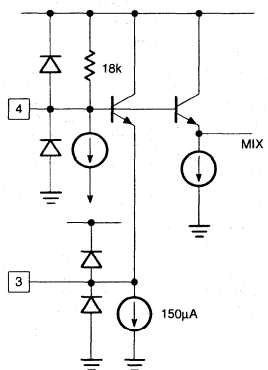
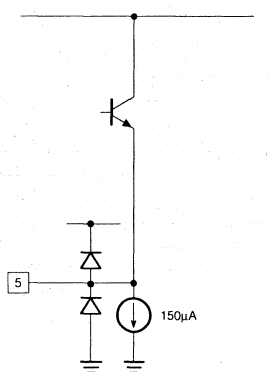
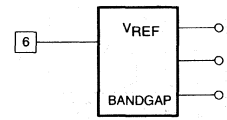
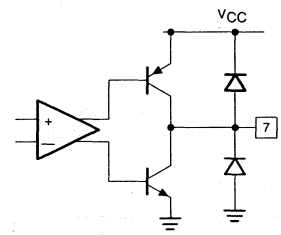
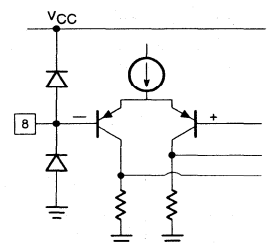
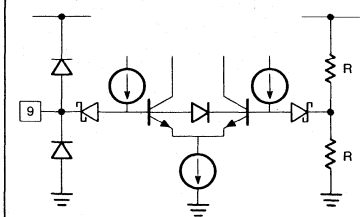


Figure 4. Performance Characteristics

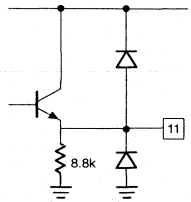
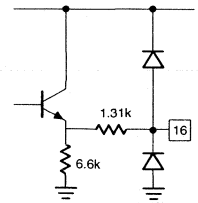
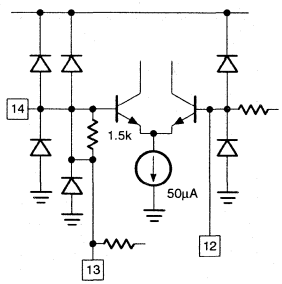
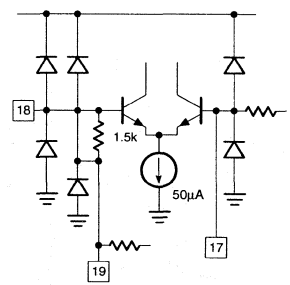
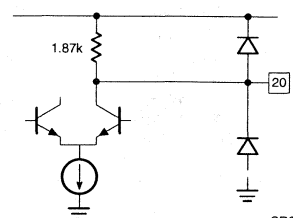
PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.40	
2	RF BYPASS	+1.40	
3	OSC E	+1.79	
4	OSC B	+2.56	
5	OSC BUFFER	+1.79	
6	V_{CC}	+3.00	
7	RSSI OUT	+0.20	
8	RSSI FEEDBACK	+0.20	
9	POWER DOWN	+2.00	

SR00508

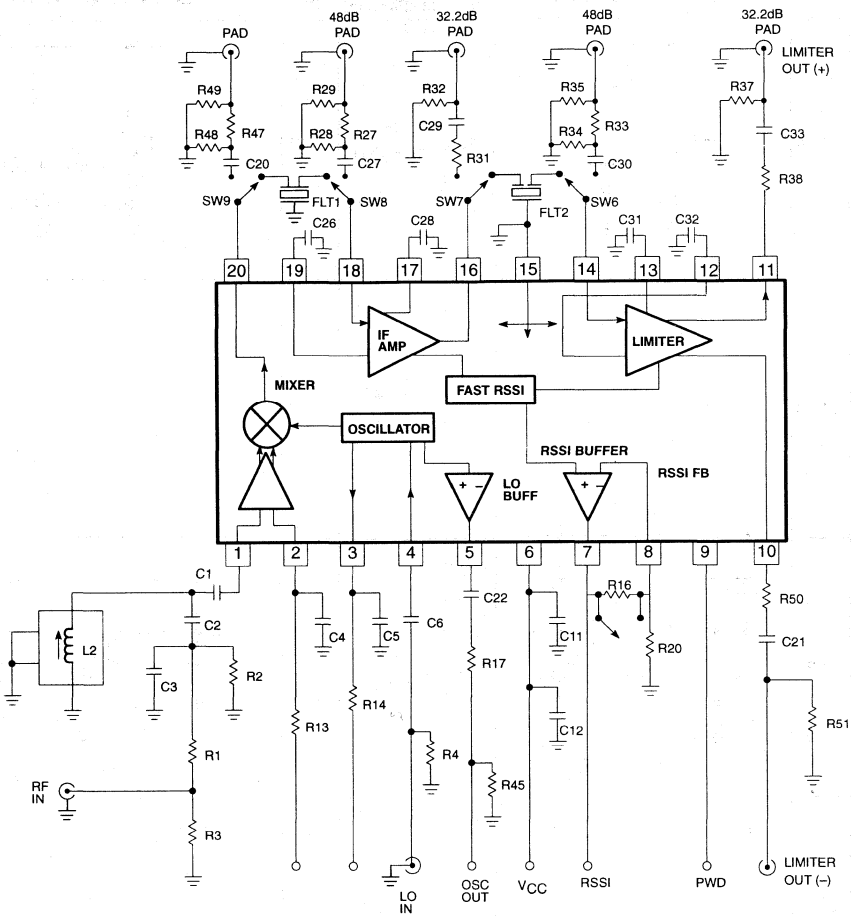
Figure 5. Pin Functions

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
10 11	LIMITER OUT	+1.25		16	IF AMP OUT	+1.28	
12	LIMITER DECOUP	+1.28		17	IF AMP DECOUP	+1.28	
13	LIMITER COUPLING	+1.28		18	IF AMP IN	+1.28	
14	LIMITER IN	+1.28		19	IF AMP DECOUP	+1.28	
15	GND	0		20	MIXER OUT	+2.03	

SR00509

Figure 6. Pin Functions (cont.)

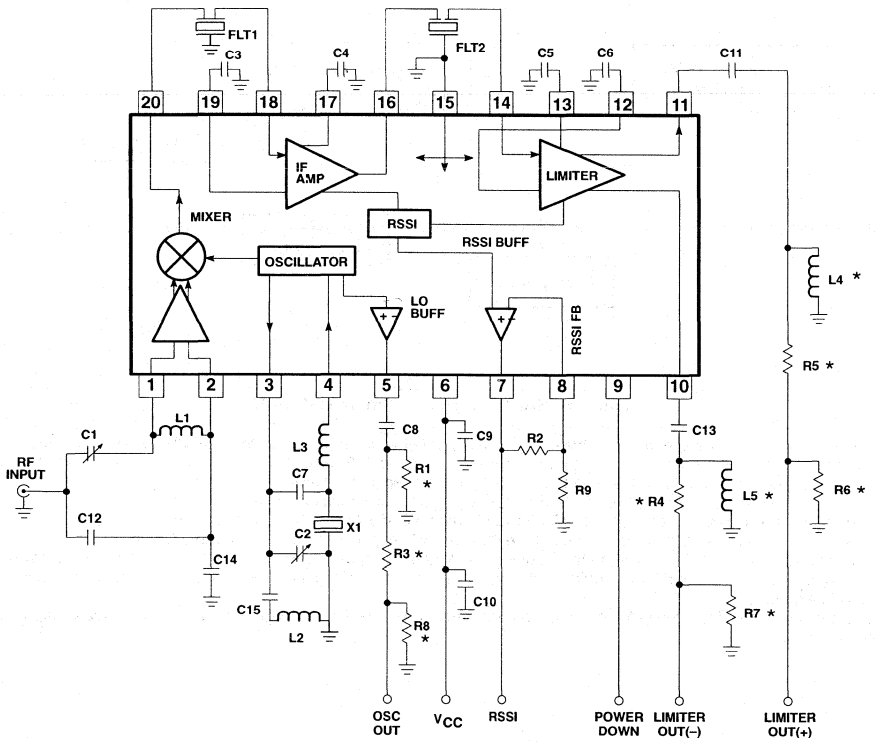


Automatic Test Circuit Component List

C1	10nF	C27	100nF	R4	49.9Ω	R32	49.9Ω	R32	49.9Ω
C2	91pF	C28	100nF	R13	10kΩ	R33	13.7kΩ	R50	1kΩ
C3	620pF	C29	100nF	R14	10kΩ	R34	1.68kΩ	R51	49.9Ω
C4	100nF	C30	100nF	R16	10kΩ	R35	49.9Ω	L2	62nH
C5	100nF	C31	100nF	R17	1kΩ	R38	1kΩ		
C6	10nF	C32	100nF	R20	10kΩ	R39	49.9Ω		
C11	100nF	C33	100nF	R27	13.7kΩ	R45	49.9Ω		
C20	100nF	R1	249Ω	R28	1.68kΩ	R47	2.43kΩ		
C21	100nF	R2	60.4Ω	R29	49.9Ω	R48	39.2kΩ		
C26	100nF	R3	60.4Ω	R31	1kΩ	R49	49.9Ω		

SR00510

Figure 7. SA637 Automatic Test Circuit



Component List

C1	5-30pF	C9	0.1µF	R1	OPEN	L1	0.15µH PM20-R15M
C2	5-30pF	C10	1.0µF	R2	0Ω (short)	L2	0.15µH PM20-R15M
C3	0.1µF	C11	0.1µF	R3	1kΩ	L3	0.47µH PM20-R47M
C4	0.1µF	C12	68pF	R4	1.0kΩ	L4	OPEN
C5	0.1µF	C13	0.1µF	R5	2.0kΩ	L5	OPEN
C6	0.1µF	C14	0.1µF	R6	51Ω	FLT1	455kHz SFGCC 455BX-TC
C7	10pF	C15	1000pF	R7	100Ω	FLT2	455kHz SFGCC 455BX-TC
C8	0.1µF			R8	100Ω	X1	82.705MHz CTS XTAL 020-3249-042
				R9	OPEN		

* NOTE: These components are optional and depend on user matching requirements.
Pads are provided on the demo board.
R2 and R9 set the RSSI buffer gain. For unity gain short R2 (Pin 7 to Pin 8) and leave R9 open.

SR00511

Figure 8. SA637 Application Circuit

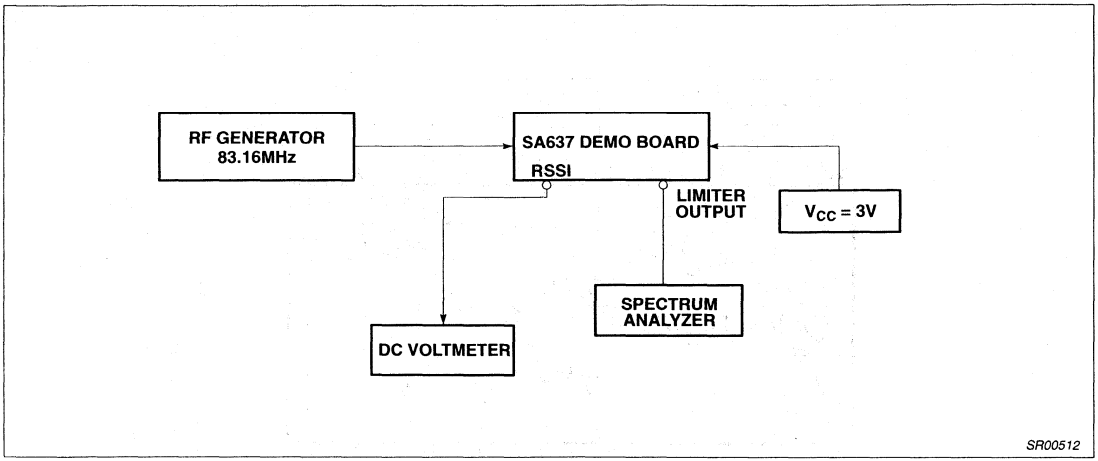


Figure 9. SA637 Application Circuit Test Set Up

NOTES:

1. Carrier-to-Noise (C/N): Connect a spectrum analyzer to Pin 10 or 11; set your RF generator to 83.16MHz or 455kHz above your LO frequency, modulation off; set the spectrum analyzer resolution bandwidth to 300Hz; and adjust your RF input level until the C/N = 26dB. Use video averaging. Assure that LIMOUT(+) and LIMOUT(–) are matched symetrically.
2. Ceramic filters: The ceramic filter can be SFGCC455BX-TC made by Murata which has 30kHz IF bandwidth.
3. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.45µV or -114dBm at the RF input.
4. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
5. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
6. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1µF bypass capacitor on the supply pin improves sensitivity.

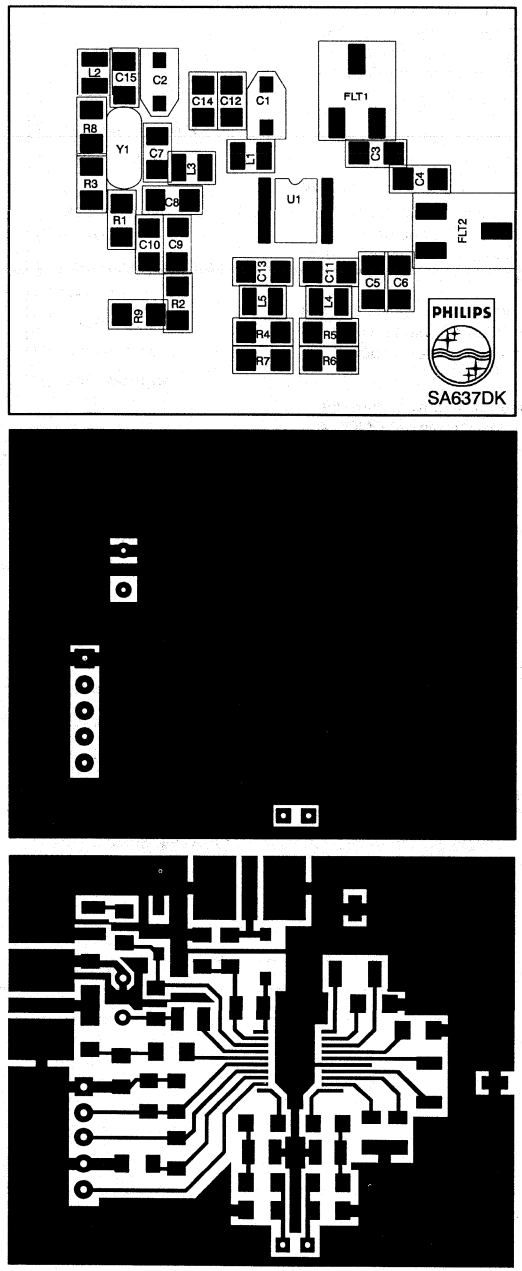


Figure 10. SA637 Board Layout (NOT ACTUAL SIZE)

Low voltage mixer FM IF system with filter amplifier and data switch

SA639

DESCRIPTION

The SA639 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two wideband limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), fast RSSI op amps, voltage regulator, wideband data output, post detection filter amplifier and data switch. The SA639 is available in 24-lead TSSOP (Thin shrink small outline package).

The SA639 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The data output provides a minimum bandwidth of 1MHz to demodulate wideband data. The RSSI output is amplified and has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

The post-detection amplifier may be used to realize a low pass filter function. A programmable data switch routes a portion of the data signal to an external integration circuit that generates a data comparator reference voltage.

SA639 incorporates a power down mode which powers down the device when Pin 8 is high. Power down logic levels are CMOS and TTL compatible with high input impedance.

APPLICATIONS

- DECT (Digital European Cordless Telephone)
- FSK and ASK data receivers

FEATURES

- V_{CC} = 2.7 to 5.5V
- Low power consumption: 8.6mA typ at 3V
- Wideband data output (1MHz min.)
- Fast RSSI rise and fall times
- Mixer input to >500MHz
- Mixer conversion power gain of 9.2dB and noise figure of 11dB at 110MHz

PIN CONFIGURATION

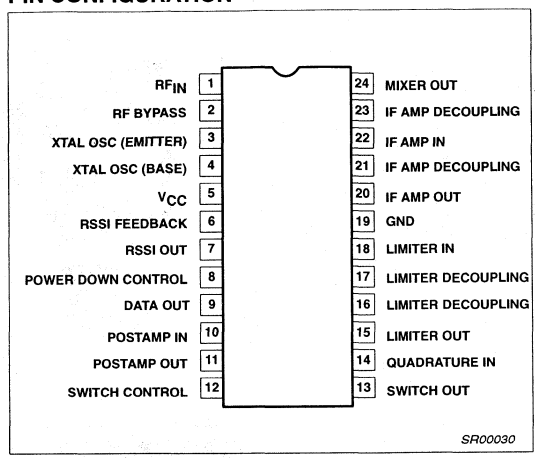


Figure 1. Pin Configuration

- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 92dB of IF Amp/Limiter power gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 80dB
- RSSI output internal op amp
- Post detection amplifier for filtering
- Programmable data switch
- Excellent sensitivity: 2.24μV into 50Ω matching network for 10dB SNR (Signal to Noise Ratio) with RF at 110MHz and IF at 9.8MHz
- ESD hardened
- Power down mode

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic TSSOP (Thin Shrink Small Outline Package)	-40 to +85°C	SA639DH	SOT-355

BLOCK DIAGRAM

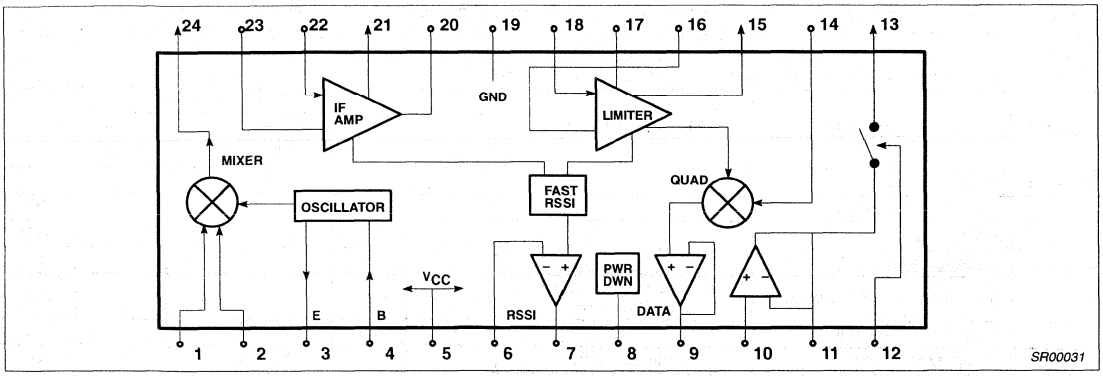


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin[1]	-0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA639[2]	-40 to +85	°C

NOTE:
1. Except logic input pins (Pins 8 and 12) which can have 6V maximum.
2. θ_{JA} Thermal impedance (DH package) 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA639					UNITS
			MIN	-3σ	TYP	+3σ	MAX	
V_{CC}	Power supply voltage range		2.7		3.0		5.5	V
I_{CC}	DC current drain	Pin 8 = LOW, Pin 12 = HIGH		8.33	8.6	8.87	10	mA
I_{CC}	Standby	Pin 8 = HIGH, Pin 12 = HIGH		131.9	140	148.1	500	µA
	Input current	Pin 8 = LOW					10	µA
		Pin 8 = HIGH					4	
	Input level	Pin 8 = LOW	0				$0.3V_{CC}$	V
		Pin 8 = HIGH[NO TAG]	$0.7V_{CC}$				6	
t_{ON}	Power up time	RSSI valid (10% to 90%)			10			µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)			5			µs
	Power up settling time	Data output valid			100		200	µs
	Switch closed	Pin 12 = LOW, PIN 8 = LOW	0				$0.3\ V_{CC}$	V
	Switch open (output tri-state)	Pin 12 = HIGH	$0.7\ V_{CC}$				6	V
	Input current	Pin 12 = LOW					10	µA
		Pin 12 = HIGH					4	
	Switch activation time				0.5		1	µs

NOTE:
1. When the device is forced in power down mode via Pin 8, the Data Switch will output a voltage close to 1.6V and the state of the switch control input will have no effect.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 110.592MHz ;LO frequency = 120.392MHz; IF frequency = 9.8MHz; RF level = -45dBm; FM modulation = 576kHz with ±288kHz peak deviation, discriminator tank circuit Q=4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			SA639					
			MIN	-3σ	TYP	+3σ	MAX	
Mixer/Osc section (ext LO = -14dBm)								
f_{IN}	Input signal frequency				500			MHz
f_{OSC}	External oscillator (buffer)		0.2		500			MHz
	Noise figure at 110MHz			10.4	11	11.6		dB
	Third-order input intercept point	Matched f1=110.592MHz; f2=110.852MHz		-11	-9.5	-8		dBm
	Conversion power gain		6	8.6	9.2	11.1		dB
	RF input resistance	Single-ended input			800			Ω
	RF input capacitance				3.5			pF
	Mixer output resistance	(Pin 24)			330			Ω
IF section								
	IF amp gain			38.86	40	41.14		dB
	Limiter gain			50.44	52	53.56		dB
	Input limiting -3dB	Test at Pin 22			–100			dBm
	IF input impedance				330			Ω
	IF output impedance				330			Ω
	Limiter input impedance				330			Ω
	Limiter output impedance				300			Ω
	Limiter output level with no load				130			mV_{RMS}
RF/IF section (ext LO = -14dBm)								
	Data level	R_L = 10kΩ, C_L = 30pF	260		360			mV_{P-P}
	Data bandwidth			2.1	2.4	2.7		MHz
S/N	Signal-to-noise ratio	No modulation for noise		56.1	60	63.9		dB
	AM rejection	80% AM 1kHz		34.8	36	37.2		dB
	RF RSSI output with buffer	RF level = -90dBm	0	0.232	0.4	0.568	0.75	V
		RF level = -45dBm	0.5	0.732	0.9	1.068	1.3	
		RF level = -10dBm	0.8	1.032	1.2	1.368	1.6	
	RF RSSI output rise time	IF frequency = 9.8MHz						
	(10kHz pulse, w/ 9.8MHz filter)	RF level = -45dBm			0.8			µs
	(no RSSI bypass capacitor)	RF level = -28dBm			0.8			
	RF RSSI output fall time	IF frequency = 9.8MHz						
	(10kHz pulse, w/ 9.8MHz filter)	RF level = -45dBm			2.0			µs
	(no RSSI bypass capacitor)	RF level = -28dBm			1.8			
	RSSI range				80			dB
	RSSI accuracy				±1.5			dB
	SINAD	RF level = -85dBm		9.45	12	14.55		dB
	S/N	RF level = -100dBm		5.8	10	14.2		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA639					UNITS
			MIN	-3σ	TYP	+3σ	MAX	
Post detection filter amplifier								
	Amplifier 3dB bandwidth	AC coupled: R_L = 10kΩ, C_L = 30pF		3.85	4.75	5.65		MHz
	Amplifier gain	AC coupled: R_L = 10kΩ, $V_{OUT\ DC}$ = 1.6V		-0.39	-0.3	-0.21		dB
	Slew rate	AC coupled: R_L = 10kΩ, C_L = 30pF			14.0			V/μs
	Input resistance		300					kΩ
	Input capacitance						3	pF
	Output impedance				250		800	Ω
	Output load resistance	AC coupled	5					kΩ
	Output load capacitance[1]	AC coupled			30			pF
	DC output level[2]		1.5	1.682	1.7	1.718	1.9	V
Data switch								
	DC input voltage range[3]		1.2		1.6		2.0	V
	AC input swing				400			mV_{P-P}
	Input impedance		100					kΩ
	Input capacitance						5	pF
	Output load resistance				500			Ω
Through Mode (Pin 12 = LOW)								
	AC voltage gain[4]				-1.5			dB
	Output drive capability	Sink/source, $V_{OUT\ DC}$ = 1.6V	3					mA
	Slew rate	$V_{OUT\ DC}$ = 1.6V			>14.0			V/μs
	Static offset voltage[5]	$V_{IN\ DC}$ = 1.2 to 2.0V		-0.6	0.30	1.2	±5	mV
	Dynamic offset voltage[2, 6]	$V_{IN\ DC}$ = 1.4 to 2.0V; V_{CC} = 3.0 to 5.0V; RF level = -70 to -40 dBm	-7				+7	mV
		$V_{IN\ DC}$ = 1.4 to 2.0V; V_{CC} = 3.0 to 5.0V; RF level = -40 to -5 dBm	-10				+10	
Tri-State Mode (Pin 12 = HIGH)								
	Output leakage current	$V_{OUT\ DC}$ = 1.2 to 2.0V		9.5	20	30.5	100	nA

NOTES:

1. Includes filter feedback capacitance, comparator input capacitance. PCB stray capacitances and switch input capacitance.
2. Demodulator output DC coupled with Post Detection Filter Amplifier input and the demodulator tank exactly tuned to center frequency.
3. Includes DC offsets due to frequency offsets between Rx and Tx carrier and demodulator tank offset due to mis-tuning.
4. With a 400mV_{P-P} sinusoid at 600kHz driving Pin 10. Output load resistance 500Ω in series with 10nF.
5. With a DC input and capacitor in the RC load fully charged.
6. The switch is closed every 10ms for a duration of 40μs. The DC offset is determined by calculating the difference of 2 DC measurements, which are determined as follows: 1) The first DC value is measured at the integrating capacitor of the switch when the switch is in the closed position immediately before it opens. The value to be measured is in the middle of the peak-to-peak excursion of the superimposed sine-wave. (DClow + (DChigh – DClow)/2). 2) The second DC value (calculated as above) is measured at Pin 11 immediately after the switch opens, and is the DC value which gives the largest DC offset to the first DC measurement within a 400μs DECT burst. Minimum and maximum limits are not tested, however, they are guaranteed by design and characterization using an optimized layout and application circuit.
7. Standard deviations are measured based on application of 60 parts.

CIRCUIT DESCRIPTION

The SA639 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 44dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 58dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 9.8MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as digital cordless phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 11dB, conversion power gain of 9.2dB, and input third-order intercept of -9.5dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 330Ω ceramic filter. The input resistance of the limiting IF amplifiers is also 330Ω. With most 330Ω ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 6dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 20) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequency at 9.8MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output (DATA) of the quadrature is a low impedance voltage output. This output is designed to handle a minimum bandwidth of 1MHz. This is designed to demodulate wideband data, such as in DECT applications.

Post Detection Filter Amplifier

The filter amplifier may be used to realize a group delay optimized low pass filter for post detection. The filter amplifier can be configured for Sallen & Key low pass with Bessel characteristic and a 3dB cut frequency of about 800kHz.

The filter amplifier provides a gain of 0dB. The output impedance is less than 500Ω in order to reduce frequency response changes as a result of amplifier load variations. The filter amplifier has a 3dB bandwidth of at least 4 MHz in order to keep the amplifier's frequency response influence on the filter group delay characteristic at a minimum. At the center of the carrier it is mandatory to provide a filter output DC bias voltage of 1.6V in order to be within the input common mode range of the external data comparator. The filter output DC bias voltage specification holds for an exactly center tuned demodulator tank and for the demodulator output connected to the filter amplifier input.

Data Switch

The SA639 incorporates an active data switch used to derive the data comparator reference voltage by means of an external integration circuit. The data switch is typically closed for 10µs before and during reception of the synchronization word pattern, and is otherwise open. The external integration circuit is formed by an R/C low pass with a time constant of 5 to 10µs.

The active data switch provides excellent tracking behavior over a DC input range of 1.2 to 2.0V. For this range with an RC load (no static current drawn), the DC output voltage will not differ more than ±5mV from the input voltage. Since the active data switch is designed to behave like a non-linear charge pump (to allow fast tracking of the input signal without slew rate limitations under dynamic conditions of a 576kHz input signal with 400mV$_{P-P}$ and the RC load), the output signal will have a 340mV$_{P-P}$ output with a DC average that will not vary from the input DC average by more than ±10mV.

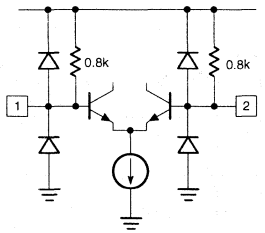
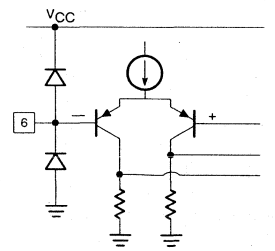
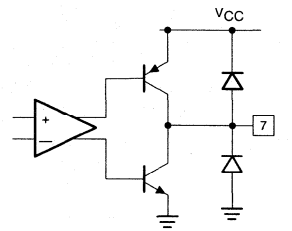
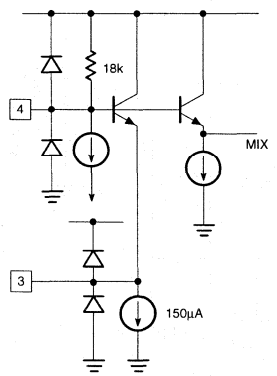
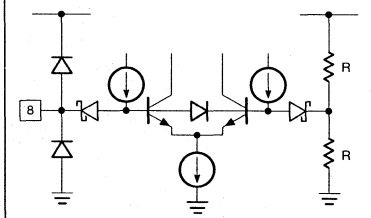
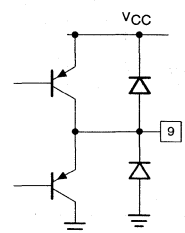
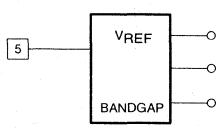
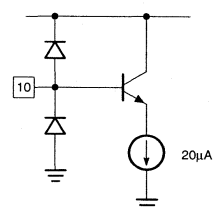
The data switch is able to sink/source 3mA from/to the external integration circuit in order to minimize the settling time after long power-down periods (DECT paging mode). In addition, during power-down conditions a reference voltage of approximately 1.6V will be used as the input to the switch. The switch will be in a low current mode to maintain the voltage on the external RC load. This will further reduce the settling time of the capacitor after power-up. It should be noted that during power-down the switch can only source and sink a trickle current (10µA). Thus, the user should make sure that other circuits (like the data comparator inputs) are not drawing current from the RC circuit.

The data switch provides a slew rate better than 1V/µs in order to track with system DC offset from receive slot to receive slot (DECT idle lock or active mode). When the data switch is opened the output is in a tri-state mode with a leakage current of less than 100nA. This reduces discharge of the external integration circuit. When powered-down, the data switch will output a reference of approximately 1.6V to maintain a charge on the external RC circuit.

A Receive Signal Strength Indicator (RSSI) completes the circuitry. The output range is greater than 80dB and is temperature compensated. This log signal strength indicator exceeds the criteria for DECT cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}

PIN FUNCTIONS All DC voltages measured with Pin 8 = Pin 12 = Pin 19 = 0V, Pin 5 = 3V and Pin 9 connected to Pin 10.

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	0.00	
4	XTAL OSC	+2.32		9	DATA OUT	+1.7	
5	V_{CC}	+3.00		10	POST AMP IN	+1.70	

SR00032

Figure 3. Pin Functions

PIN FUNCTIONS (continued)

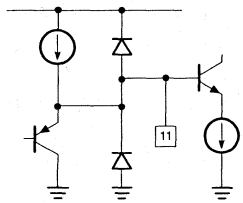
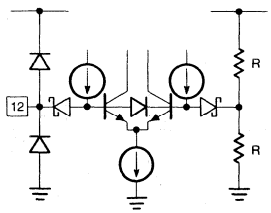
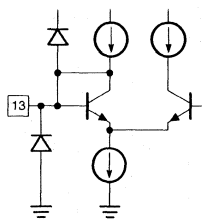
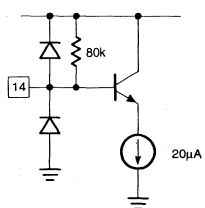
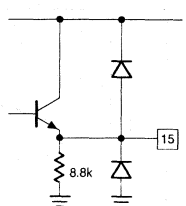
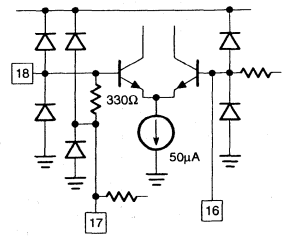
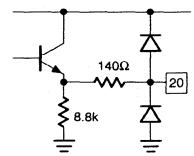
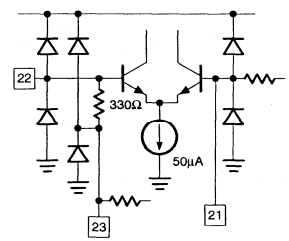
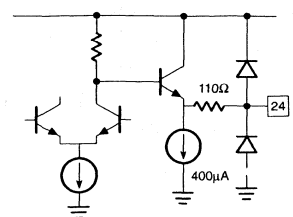
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	POST AMP OUT	+1.70	
12	SWITCH CONTROL	0.00	
13	SWITCH OUT	+1.70	
14	QUAD IN	+3.00	
15	LIMITER OUT	+1.35	
16	LIMITER DECOUP	+1.23	
17	LIMITER COUPLING	+1.23	
18	LIMITER IN	+1.23	
19	GND	0	
20	IF AMP OUT	+1.22	
21	IF AMP DECOUP	+1.22	
22	IF AMP IN	+1.22	
23	IF AMP DECOUP	+1.22	
24	MIXER OUT	+1.03	

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Figure 4. Pin Functions (cont.)

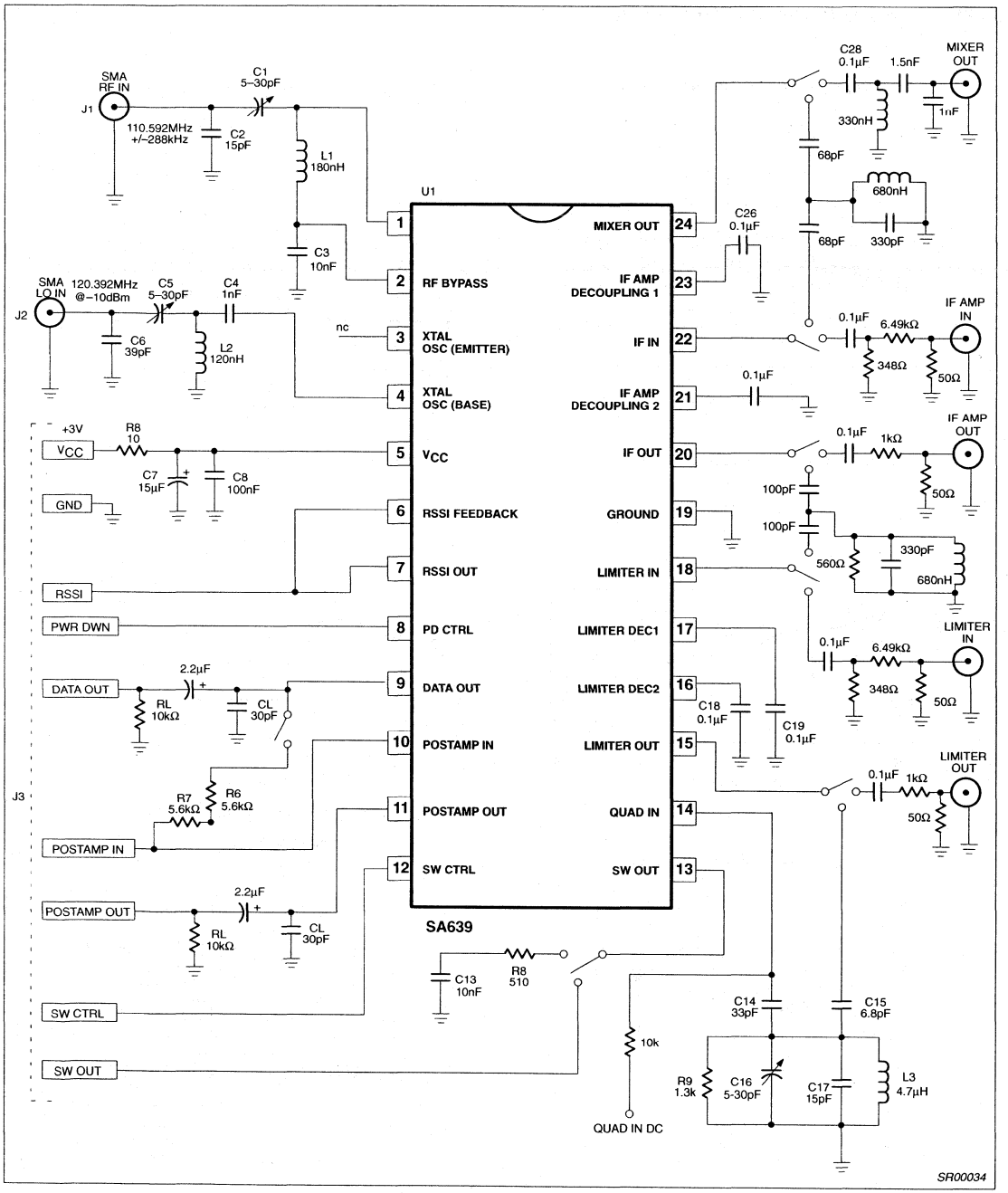
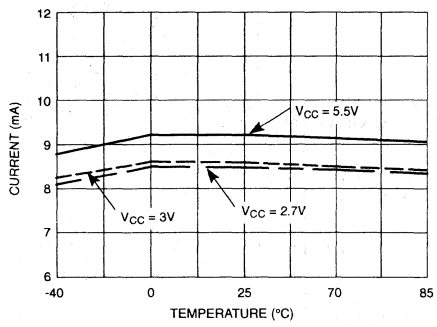


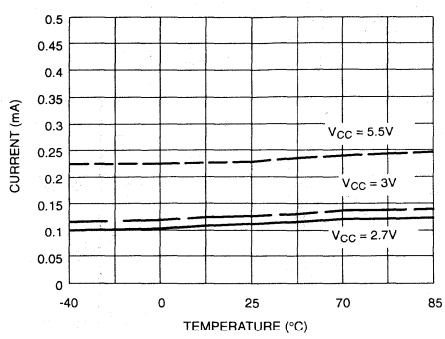
Figure 5. SA639 Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature and V_{CC}

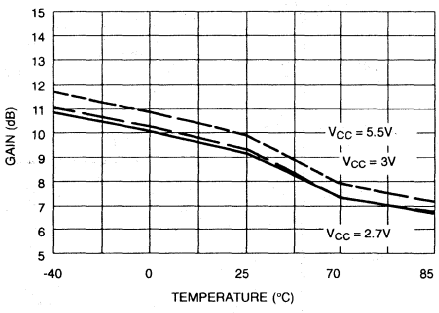


Standby Supply Current vs Temperature and V_{CC}



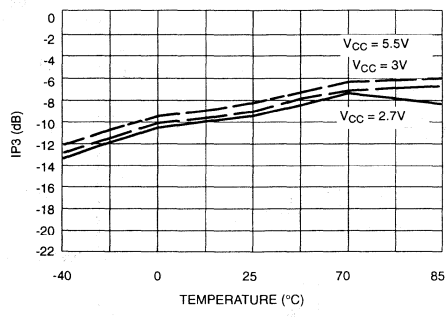
Mixer Power Gain vs Temperature and V_{CC}

RF = -40dBm, 110.392MHz
LO = -10dBm, 120.592MHz



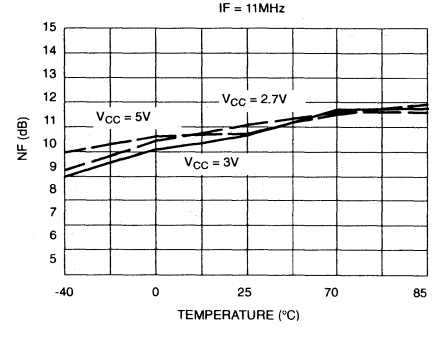
Mixer Input IP3 vs Temperature and V_{CC}

RF = -40dBm, 110.392MHz
LO = -10dBm, 120.592MHz



Mixer NF vs Temperature and V_{CC}

IF = 11MHz



Limiter and IF Gain vs Temperature and V_{CC}

IF Input = -90dBm, 9.8MHz
LIM Input = -100dBm, 9.8MHz

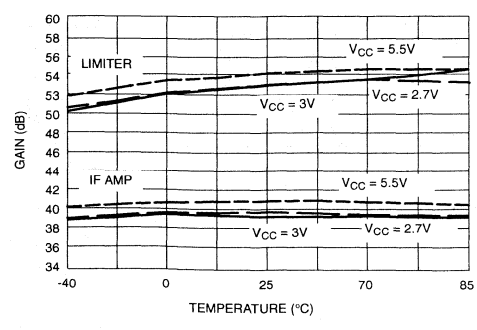


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Figure 6. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

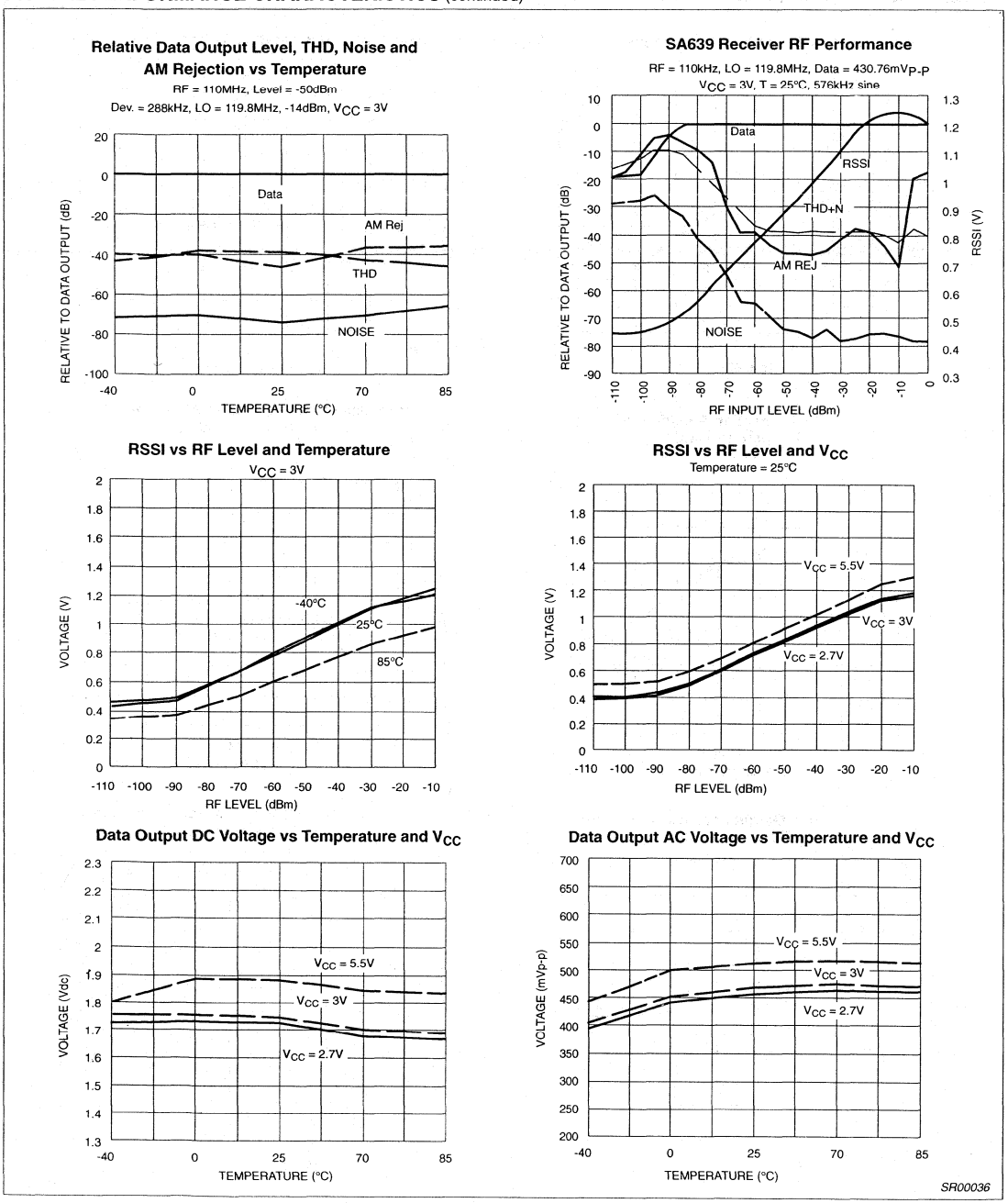

Figure 7. Typical Performance Characteristics (cont.)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

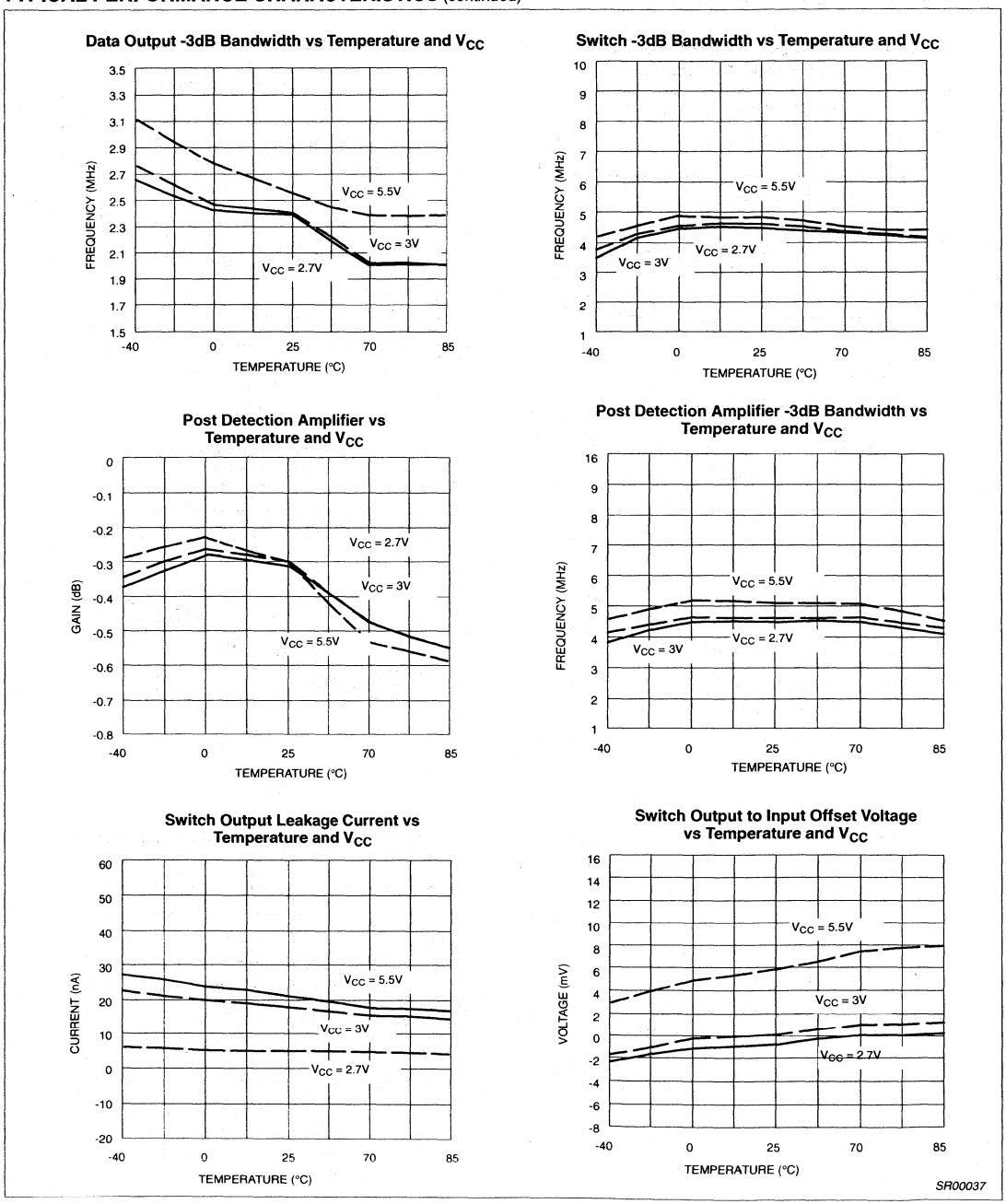

Figure 8. Typical Performance Characteristics (cont.)

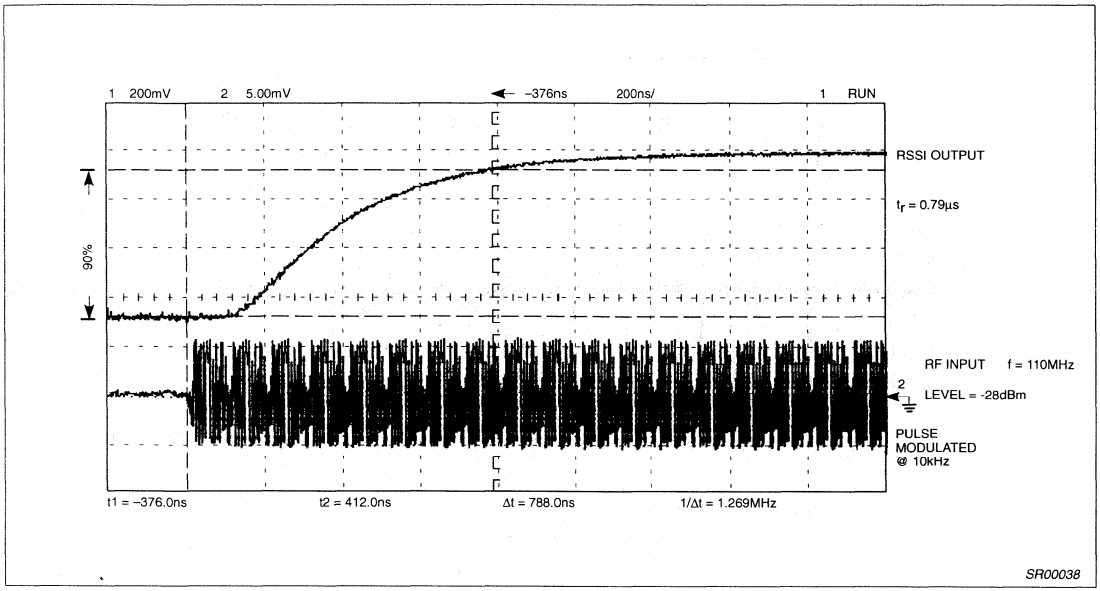

Figure 9. SA639 RSSI Rise Time

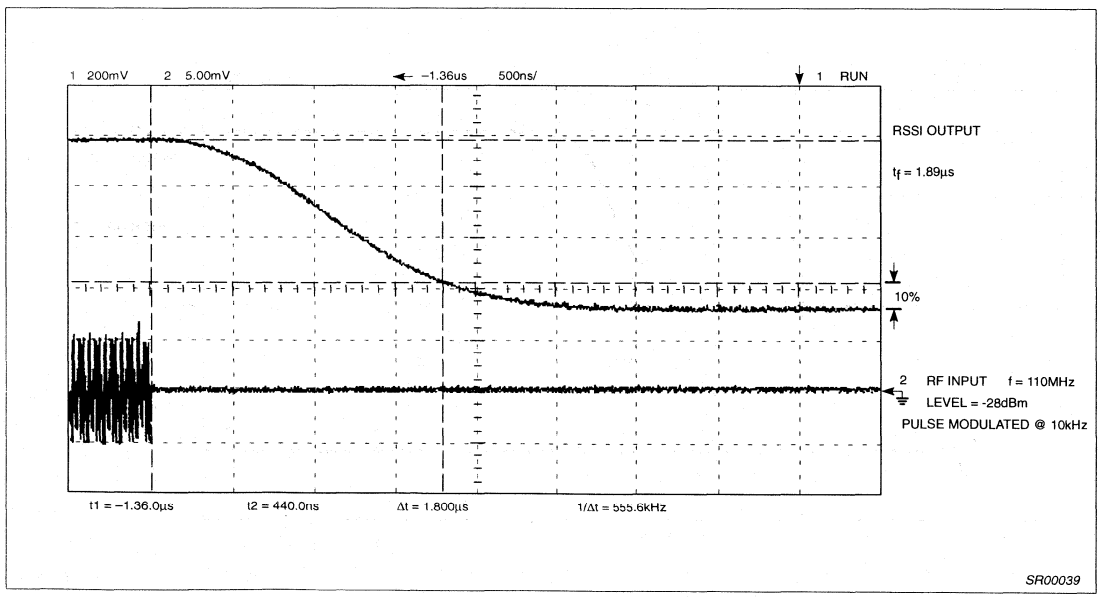

Figure 10. SA639 RSSI Fall Time

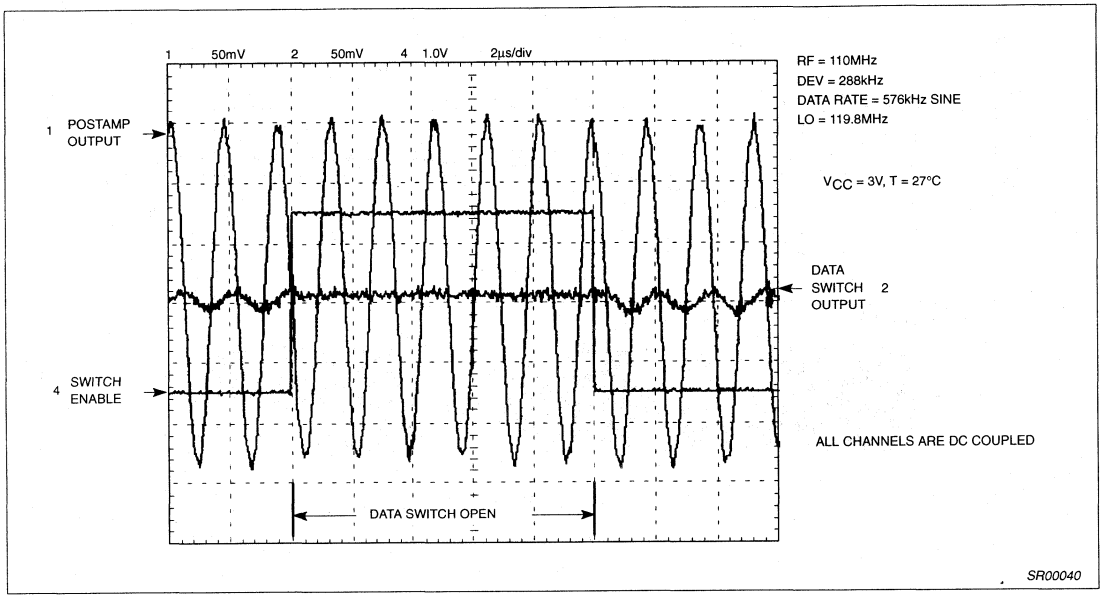

Figure 11. SA639 System Dynamic Response

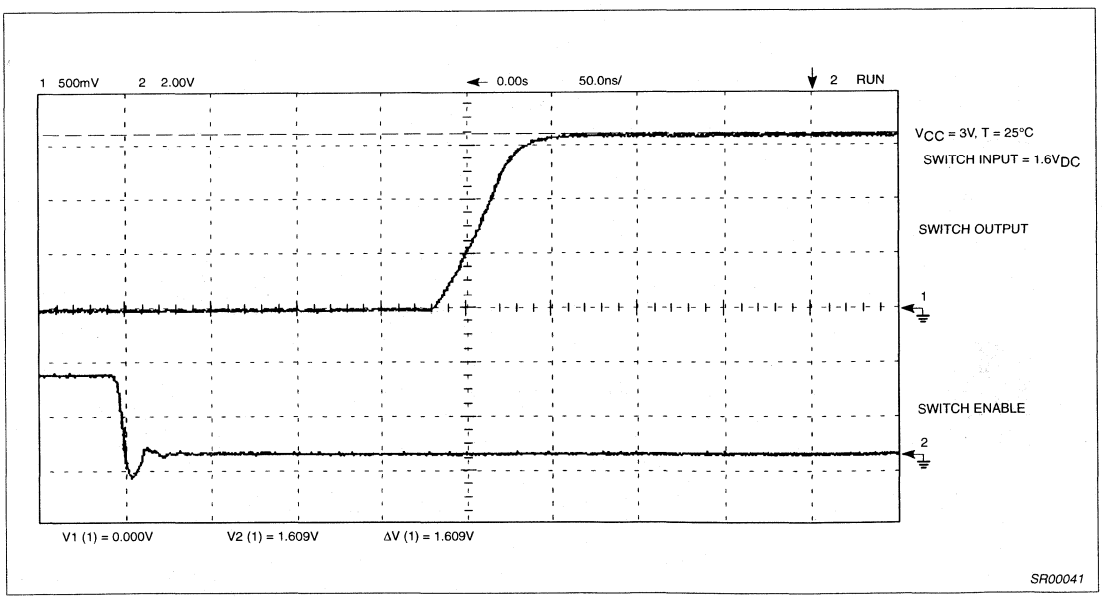

Figure 12. SA639 Data Switch Activation Time

An FM/IF system for DECT and other high speed GFSK applications: SA639

AN1998

Author: Yanpeng Guo

ABSTRACT

A Philips low voltage high performance monolithic FM/IF system, the SA639 is introduced to meet the increasing demand for high speed digital wireless PCS applications. In order to assist the system design, a SA639-based performance evaluation board has been developed according to the Digital European Cordless Telephone (DECT) specifications. This application note presents a detailed description of the SA639 FM/IF system, the evaluation board, and design information including circuit diagram, component list, and the board layout. The experimental performance evaluation procedures, measured bit error rate (BER), sensitivity to frequency off-set, and sensitivity to FM deviation variation of this system are also presented. Results indicate that the low voltage SA639 FM/IF system provides superior performance for high speed digital wireless applications.

I. INTRODUCTION

To achieve the goal of wireless personal communications, allowing users access to the capabilities of the global communications network at any time without regard to location and mobility, cellular and cordless telephony have been taken as two major approaches. Cellular systems are evolving towards smaller cells (microcells) and lower power levels to provide higher overall capacity. Cordless telephones have evolved from home appliances towards wide spread "universal" low power personal communications systems. With the advent of digital cordless telephony, cordless systems with enhanced functionality have been developed that can support higher data rates and more sophisticated applications such as wireless private branch exchanges (WPBX) and public-access Telepoint systems. One of the first digital cordless standards is the Digital European Cordless Telecommunications (DECT) system, a pan-European standard designed to connect all of Europe with a common digital cordless system. DECT is also a flexible standard for providing a wide range of services in small cells.

In this application note, the SA639, a Philips low voltage FM/IF system with several important features such as post filter amplifier and active data switch, is proposed for DECT and other high speed digital wireless applications. A SA639-based DECT receiver evaluation board has been developed. Detailed description of the SA639 FM/IF system, structure of the evaluation board, design information, and experimental evaluation results are presented.

II. REVIEW OF DECT STANDARD

DECT is designed as a flexible interface to provide cost-effective communications services to high user densities in small cells. This standard is intended for the applications such as domestic cordless telephony, Telepoint, cordless PBXs, and Radio Local Loop (RLL). It supports multiple bearer channels for speech and data transmission (which can be set up and release during a call), hand over, location registration, and paging. Functionally, DECT is closer to a cellular system than to a classical cordless telephone. However, the interface to PSTN or ISDN remains the same as for a PBX or corded telephone. Table 1 is a summary of the key specifications of DECT and other digital cordless telephone systems.

DECT is based on Time Division Duplex (TDD) and Time Division Multiple Access (TDMA) with 10 carriers in the 1880 - 1900MHz band. Figure 1 illustrates the DECT TDD/TDMA frame structure. The completed frame is 10ms in duration with 24 time slots. The first 12 slots are allocated for the transmission from base station to handsets, and the other 12 slots are for the transmission from hand sets to base station. Each slot is 417µs long with 480 bits. The first 32 bits is a "1010..." sequence for synchronization. The 32kb/s ADPCM CODEC is used for speech coding in DECT, which provides 320 bits during each 10ms frame. When a call is made, two slots (one is in the first 12 slots, the other is in the last 12 slots) are assigned to the user for transmit and receive.

Gaussian filtered FSK (GFSK) modulation scheme is employed in DECT. GFSK is a premodulation Gaussian filtered digital FM scheme. Figure 2 shows the block diagram of a GFSK modulator. The advantages of GFSK can be summarized as follows.

i) Constant envelope nature: this allows GFSK modulated signal to be operated with class-C power amplifier without introducing spectrum regeneration. Therefore, lower power consumption and higher power efficiency can be achieved.

ii) Narrow power spectrum: narrow mainlobe and low spectral tails keep the adjacent channel interference to low levels and achieve higher spectral efficiency.

iii) Non-coherent detection: GFSK modulated signal can be demodulated by the limiter/discriminator receiver as shown in Figure 3. This simple structure leads to low cost GFSK receivers.

III. THE SA639 FM/IF SYSTEM

The SA639 is a low-voltage high performance monolithic FM/IF system with high speed RSSI incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, fast RSSI op amps, post detection filter amplifier, and a data switch. The block diagram of SA639 is presented in Figure 4. The SA639 was designed specially for high data rate portable communications applications and will function down to 2.7V. The data output provides a minimum bandwidth of 1MHz to demodulate high speed data, such as in DECT applications. Figure 5 presents the quad tank S-curve of SA639, which indicates the linear range to be about 2MHz. The measured RSSI characteristics of SA639 is presented in Figure 6. With more than 75dB dynamic range, the SA639 RSSI rise/fall time is 0.8/2.0ms at -45dBm RF level.

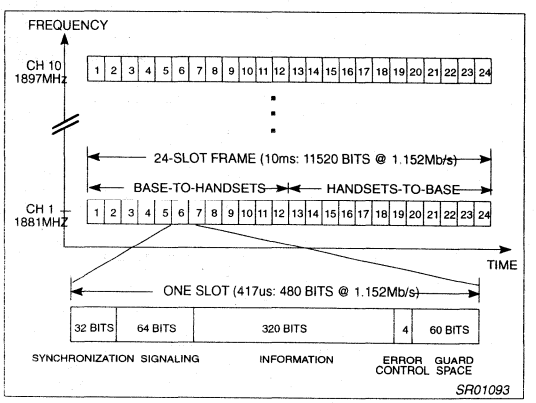

Figure 1. DECT TDD/TDMA Frame Structure

An FM/IF system for DECT and other high speed GFSK applications: SA639

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Table 1. Summary of Digital Cordless Standards

Standard	CT2/CT2+	DECT	PHS	PACS
Region	Europe/Canada	Europe	Japan	USA
Frequency Band (MHz)	CT2: 864–868 CT2+: 944–948	1880–1900	1895–1918	Tx: 1850-1910 Rx: 1930-1990
Duplex	TDD	TDD	TDD	FDD
Multiple Access	TDMA	TDMA	TDMA	TDMA
Number of Channels	40	10	77	16 pairs
Channel Spacing (kHz)	100	1728	300	300
Users/Channel	1	12	4	8/pair
Modulation	GFSK (FM dev. 14-25kHz)	GFSK (FM dev. 288kHz)	π/4-DQPSK	π/4-DQPSK
Bit Rate	72kb/s	1.152Mb/s	384kb/s	384kb/s
Speech Coding	32kb/s ADPCM	32kb/s ADPCM	32kb/s ADPCM	32kb/s ADPCM
Frame Duration	2ms	10ms	5ms	2.5ms
Peak Power	10mW	250mW	80mW	200mW

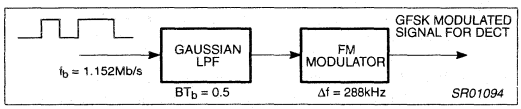

Figure 2. Block Diagram of GFSK Modulator

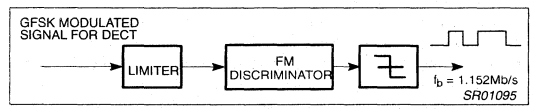

Figure 3. Block Diagram of GFSK Demodulator

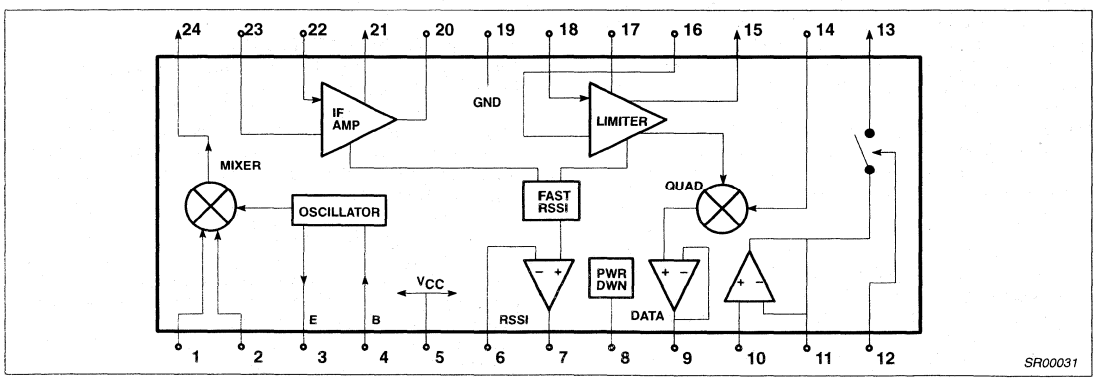

Figure 4. Block Diagram of the SA639 FM/IF System

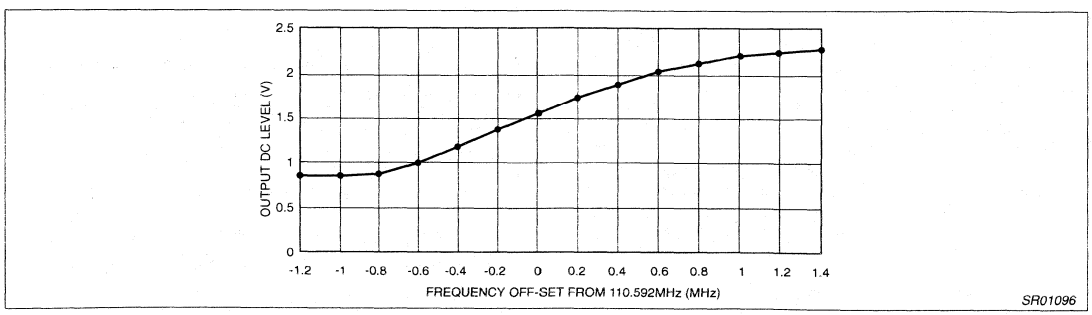

Figure 5. Quad Tank S-Curve of SA639 Board

An FM/IF system for DECT and other high speed GFSK applications: SA639

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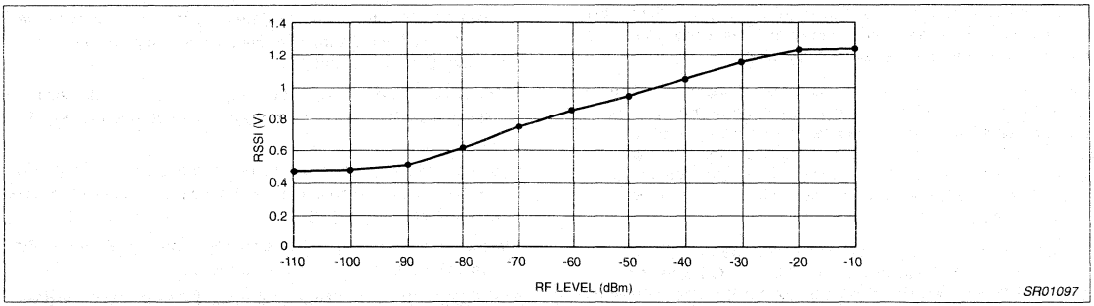

Figure 6. Measured RSSI Characteristics of SA639

The post-detection amplifier may be used to realize a group delay optimized low pass filter. The filter amplifier provides 0dB gain and has a 3dB bandwidth of at least 4MHz in order to keep its frequency response influence on the filter group delay characteristics at a minimum. It can be configured for Sallen & Key low pass with Bessel characteristic and a 3dB cut frequency of about 800kHz.

The SA639 incorporates an active data switch to derive the data comparator reference voltage by means of routing a portion of data signal to an external integration circuit. The data switch is typically closed for 10ms in the course of 32 bit synchronization sequence, and is open otherwise. The time constant of the external integration circuit is about 5 to 10ms. This active switch provides excellent tracking behavior over a DC input range of 1.2 - 2.0V. The slew rate is better than 1V/ms. When the switch is opened, the output is in a tri-state mode with a leakage current of less than 100nA. This reduces the discharge of the external integration circuit. As compared to other similar FM/IF chips, another advantage of SA639 is that during power down mode (between data bursts) the data switch will output a reference of about 1.6V to maintain a charge on the external RC circuit. This idea helps extract the reference voltage for the external capacitor in a shorter time and improves the accuracy of the voltage on the capacitor. The overall system is well suited for battery operated high quality products in digital wireless personal communications. Detailed specifications of SA639 can be found in [3].

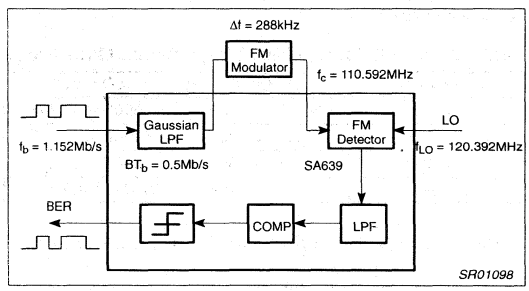

Figure 7. Structure of the SA639 GFSK Evaluation Board

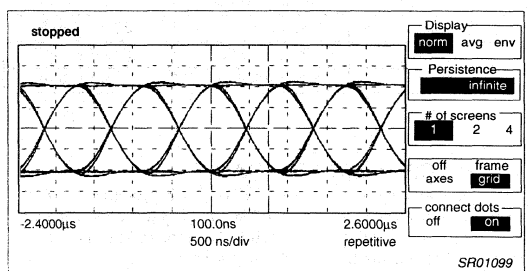

Figure 8. Measured Eye-Diagram at the Output of Tx Gaussian LPF

IV. STRUCTURE OF THE SA639 EVALUATION BOARD

A SA639-based evaluation board has been developed based on DECT specifications. The structure of this board is illustrated in Figure 7 together with a VCO/FM discriminator based GFSK modem (modulator/demodulator). The demo board contains the entire demodulator as well as the Gaussian low-pass filter (LPF) for the modulator. The DECT modulated signal, therefore, can be generated either by a standard DECT signal generator, or by sending a 1.152Mb/s data stream to the on-board Gaussian LPF (BTb = 0.5), then applying the filtered base band wave form to a FM signal generator with a modulation index of 0.5. The output is then the GFSK modulated signal (DECT). The schematic of the Gaussian LPF can be found in Figure 14. Baseband eye-diagram at the output of the Gaussian LPF is presented in Figure 8.

At the output of the limit/frequency discriminator, the post-detection amplifier is configured as a Sallen & Key LPF to eliminate noise. For the convenience of operation, the evaluation board is designed in such a way that the reference voltage for the data comparator can be obtained either from the switch controlled DC extraction circuit, or directly from the power supply. If the DECT Burst Mode Control circuit is available, the active data switch can be used to extract and track DC level during the synchronization sequence. Otherwise the DC reference can be obtained from the power supply and manually adjusted for the comparator operation.

A 2-level threshold detector with sampling time adjustment circuit is implemented on the board for data regeneration. The phase of data clock can be adjusted manually through a monostable multivibrator (74HC123) to achieve the optimal sampling time. The demo board is initially adjusted for a bit rate of 1.152Mb/s. If a different data rate

is used, the sampling time has to be re-adjusted. The output of the threshold detector is the regenerated binary data, which can be sent to a data error analyzer to evaluate the BER performance.

The symbol timing recovery (STR) circuit is not implemented on this evaluation board. Transmit data clock either hard-wire connected from the transmitter or from a separate STR circuit is required for the operation. The performance measurements presented in this application note were conducted with hard-wire connected data clock. However, BER degradation caused by STR should not be more than 1dB [6].

This SA639-based GFSK demo board is designed with DECT specifications at RF frequency of 110.592MHz, LO frequency of 120.392MHz, and intermediate frequency of 9.8MHz. For different frequency plan applications, the step-by-step matching circuit design procedure can be found in [1]. Tables 2 and 3 present the SA639 RF/LO input impedance and Mixer/Limiter output impedance over frequency, respectively.

Table 2. SA639 RF/LO Input Impedance Over Freq.

Frequency	RF Input	LO Input
50MHz	846Ω // 4.52pF	6900Ω // 4.07pF
110MHz	687Ω // 3.84pF	4900Ω // 4.09pF
240MHz	510Ω // 3.69pF	1900Ω // 4.22pF
500MHz	190Ω // 4.21pF	245Ω // 4.98pF

Table 3. SA639 Mixer/Limiter Output Impedance Over Freq.

Frequency	RF Input	LO Input
0.5MHz	395Ω // 20.2pF	438Ω // 14.5pF
10MHz	350Ω // 6.67pF	383Ω // 3.5pF
21MHz	339Ω // 4.58pF	393Ω // 2.04pF
50MHz	326Ω // 3.44pF	391Ω // 1.35pF

V. PERFORMANCE EVALUATION

Performance of this SA639 based DECT GFSK system including BER and sensitivity to frequency off-set and FM deviation variation is experimentally evaluated. Measurement procedures and the measured results are presented in this section.

Figure 9 illustrates the measurement set-up with the SA639 DECT evaluation board. A data error analyzer is employed to generate a pseudo random binary sequence (PRBS) with length of 10^9-1 at a data rate of 1.152Mb/s. This data sequence is sent to a DECT signal generator to generate a standard DECT modulated signal at 110.592MHz. Another signal generator is employed to provide an LO signal at 120.392MHz for the FM/IF system detection. The reference DC voltage for the data comparator is obtained from power supply for this evaluation. Data clock signal is directly from the data error analyzer. The sampling time is manually adjusted at the center of baseband eye diagram. Recovered data sequence is fed back to the Data Error Analyzer for BER measurement.

The BER measurement procedures can be summarized as follows.

- Build the measurement set-up as shown in Figure 9.
- Measure SINAD at the data output of SA639: RF = 110.592MHz, fm = 1kHz, Df = 288kHz; LO = 120.392MHz, -10dBm; the typical sensitivity for 12dB SINAD should be about -97dBm.
- Check SA639 output level: tune the quad tank circuit to have the least distorted eye-diagrams at the post-op. amp. output. The DC level should be about 1.4 - 1.7v.
- Check the DC reference for the comparator: set the reference voltage at the DC level of the op. amp. output by adjusting VR1 in Figure 14.
- Adjust sampling position: set the up edge of the clock at pin 11 of 74HC74 to be at the center of the eye-diagram at pin 2 of LM311B by adjusting VR2 in Figure 14.
- Measure BER with high RF level: set RF input signal level at -60 dBm; LO signal level at -10 dBm: error free.
- Measure BER vs. RF input level curve: RF level: -76 ~ -86 dBm, LO level: -10 dBm, at each point, at least 100 errors have to be measured.

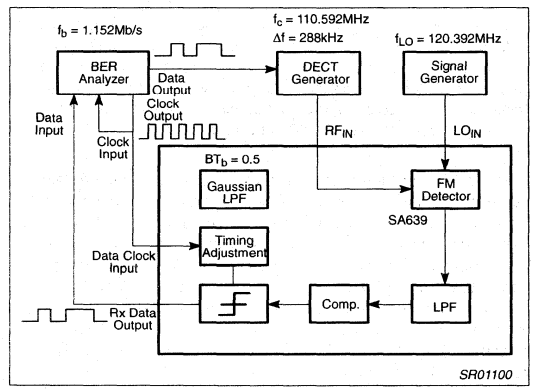

Figure 9. Block Diagram of the BER Evaluation Set-up

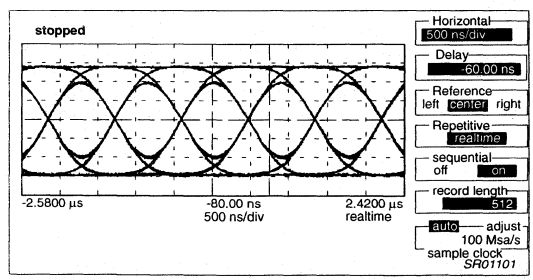

Figure 10. Recovered Eye-Diagram at the Output of SA639

The recovered baseband eye-diagram is shown in Figure 10, and the measured BER vs. RF input level is presented in Figure 11. It can be seen that about -83dBm RF power is needed to achieve the bit error rate of 10^{-3}. Since a typical front-end circuit has a better noise figure than FM/IF system, it is common to achieve more than 5dB signal-to-noise ratio gain by the front-end circuit. Therefore, with the SA639 FM/IF the overall system sensitivity could be better than -88dBm for the BER of 10^{-3}. Based on our measurements, by applying the Philips UAA2077AM 2GHz image rejecting front-end to the SA639 FM/IF system the overall system sensitivity is -91dBm for the BER of 10^{-3}. This performance compares very well to the DECT specifications for public access equipment (-86dBm for 10^{-3} BER).

An FM/IF system for DECT and other high speed GFSK applications: SA639

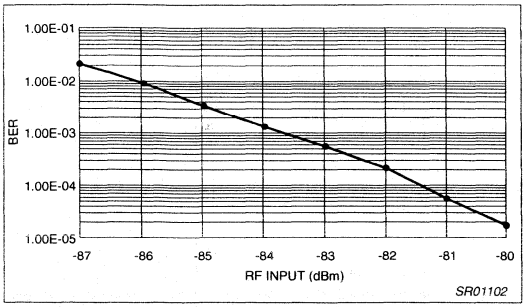

Figure 11. BER of the SA639 DECT Demoboard (RF: 110.592 MHz; LO: 120.392 MHz; fb: 1.152 Mb/s)

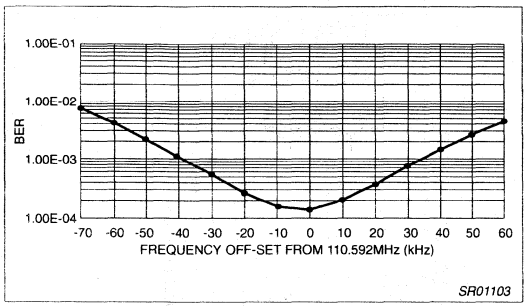

Figure 12. BER Degradation Caused by Frequency Off-Set (RF: -82dBm)

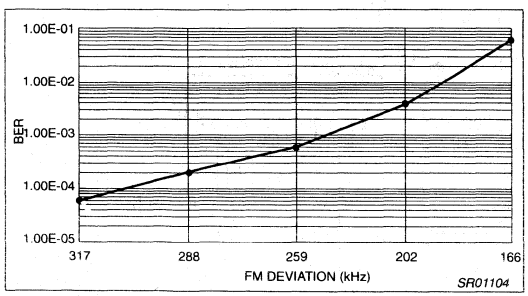

Figure 13. BER vs. FM Deviation (RF: 110.592 MHz, -82 dBm; fb: 1.152 Mb/s)

The performance degradation caused by frequency off-set and the sensitivity to FM deviation variation of this system are also evaluated. Figure 12 presents the measured BER vs. frequency off-set. Even with 50 kHz off-set, only minor degradation can be observed, and -82dBm RF level is enough for 10^{-3} BER. The sensitivity of this system to FM deviation variation is illustrated in Figure 13. Even with 10% deviation reduction (259kHz), less than -82dBm RF signal is needed to achieve the BER of 10^{-3}. These results indicate that the Philips SA639 FM/IF system provides superior performance for DECT and other high data rate GFSK applications.

An FM/IF system for DECT and other high speed GFSK applications: SA639

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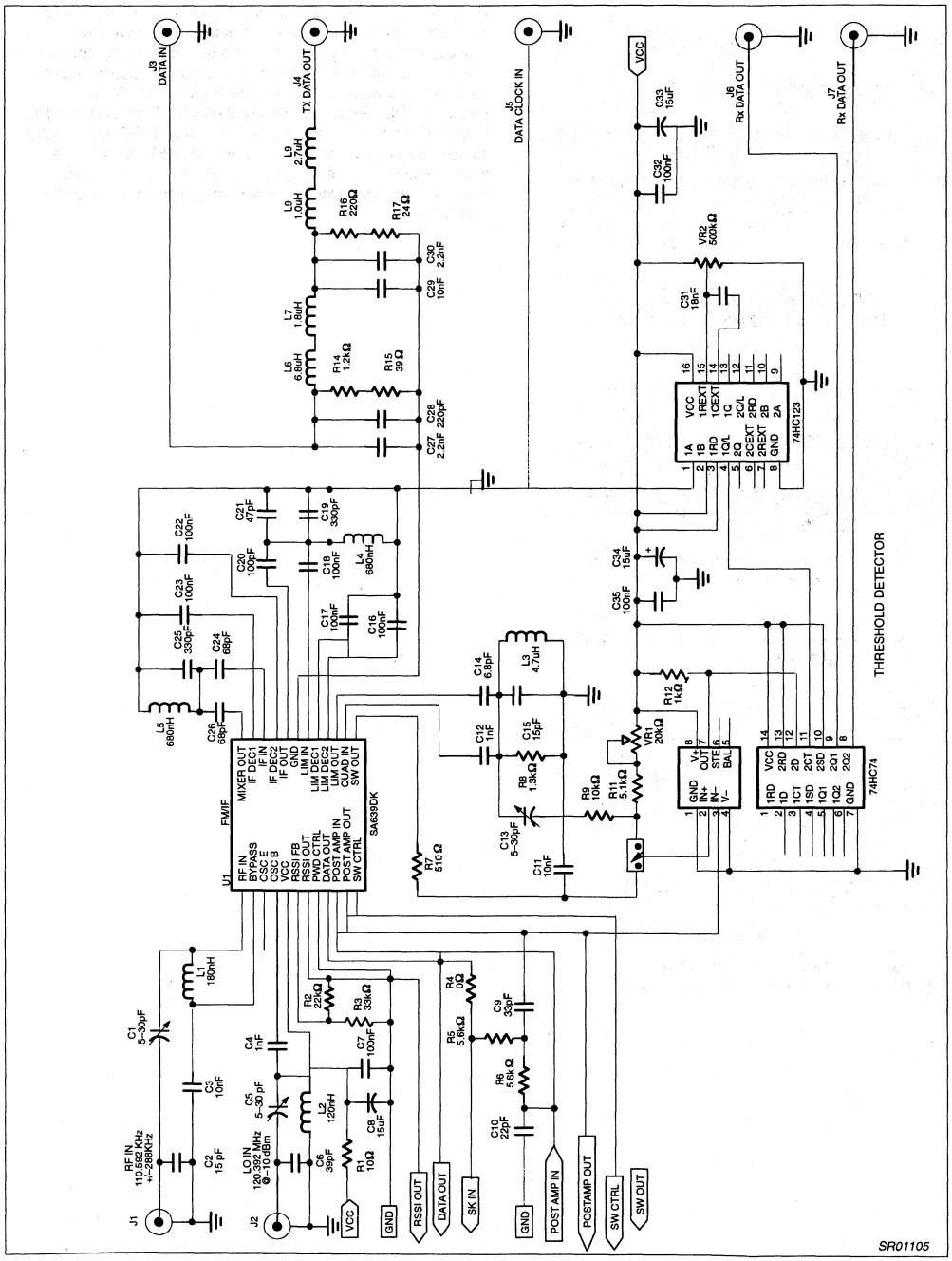

Figure 14. Schematic

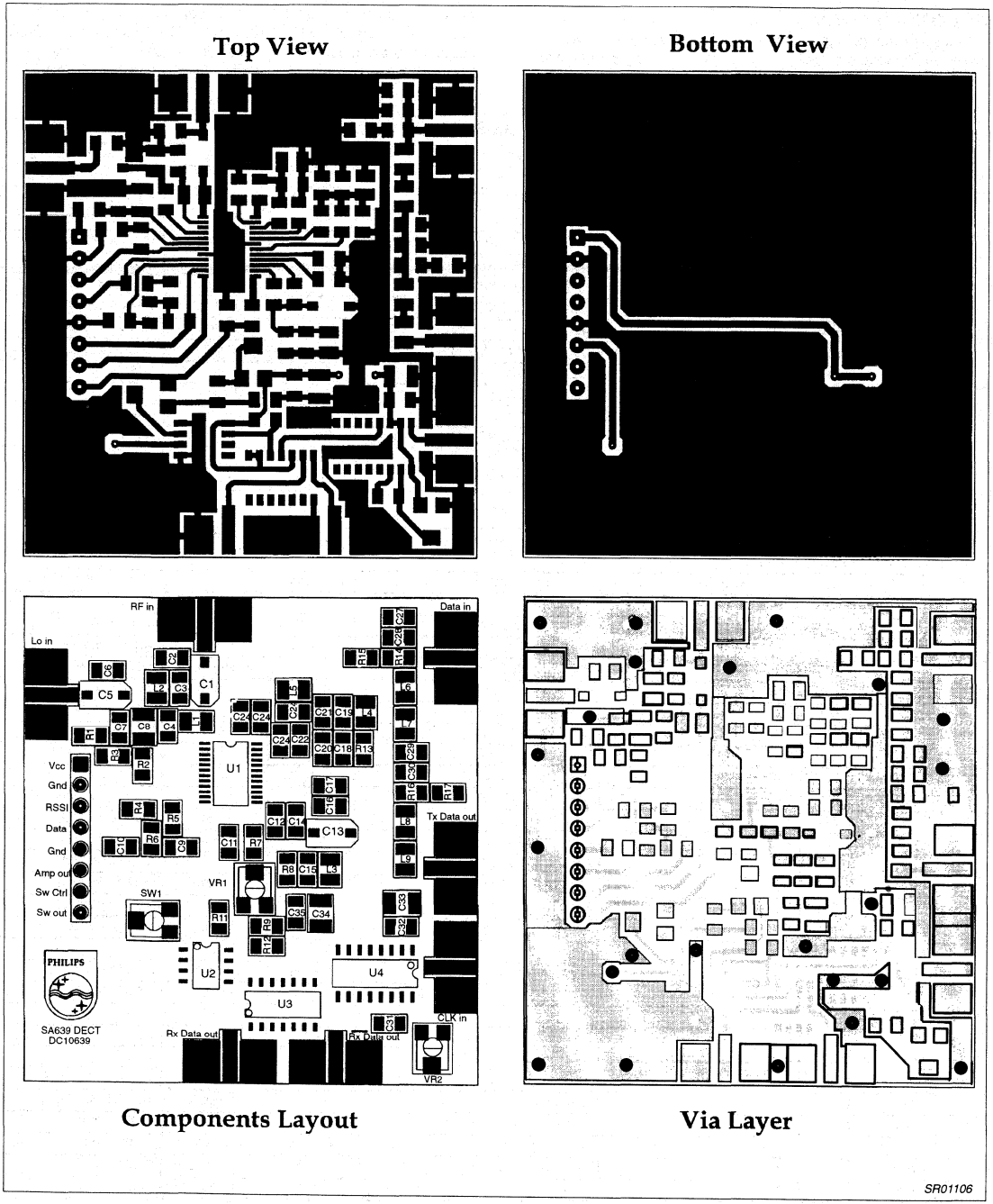

Figure 15. Board Layout

An FM/IF system for DECT and other high speed GFSK applications: SA639

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VI. CONCLUSIONS

A Philips low voltage high performance FM/IF system (SA639) based GFSK modem evaluation board is presented. Experimental performance evaluation including bit error rate (BER), sensitivity to frequency off-set, and sensitivity to FM deviation variation of this system has been conducted based on DECT specifications. Results indicate that a superior performance can be achieved with the Philips FM/IF systems for high speed digital wireless applications.

Table 4. Customer Application Component List for GMSK/GFSK Demoboard

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	6.8pF	50V	C14	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG689C9BB2
1	15pF	50V	C2, C15	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG150J9BB2
1	18pF	50V	C31	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG180J9BB2
1	22pF	50V	C10	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG220J9BB2
1	33pF	50V	C9	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG330J9BB2
1	39pF	50V	C6	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG390J9BB2
1	47pF	50V	C21	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG470J9BB2
2	68pF	50V	C24, C26	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG680J9BB2
2	100pF	50V	C18, C20	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG101J9BB2
1	220pF	50V	C28	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG221J9BB2
1	330pF	50V	C19, C25	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG331J9BB2
3	1000pF	50V	C4, C12	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG102J9BB2
2	2200pF	50V	C27, C30	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG222J9BB2
3	0.01µF	50V	C3, C11, C29	Cer Cap 1206 X7R ±10%	Garrett	Philips	12062R103K9BB2
7	0.1µF	50V	C7, C16, C17, C22, C23, C32, C35	Cer Cap 1206 X7R ±10%	Garrett	Philips	12062R104K9BB2
3	15µF	10V	C8, C33, C34	Tantalum Capacitor Chips	Garrett	Philips	49MC106C006KOAS
Surface Mount Variable Capacitors							
3	5-30pF		C1, C5, C13	Trimmer capacitor	Kent Elect	Kyocera	CTZ3S-30C-W1
Surface Mount Resistors							
1	0Ω	50V	R4	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW000E
1	10Ω	50V	R1	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW100E
1	24Ω	50V	R17	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW240E
1	39Ω	50V	R15	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW390
1	220Ω	50V	R16	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW221E
1	510Ω	50V	R7	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW511E
1	560Ω	50V	R13	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW561E
1	1kΩ	50V	R12	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW102E
1	1.2kΩ	50V	R14	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW122E
1	1.3kΩ	50V	R8	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW132E
1	5.1kΩ	50V	R11	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW512E
2	5.6kΩ	50V	R5, R6	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW562E
1	10kΩ *	50V	R9	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW223E
1	22kΩ	50V	R2	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW223E
3	33kΩ	50V	R3	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW333E
Surface Mount Variable Resistors							
1	20kΩ	50V	VR1	Trimmer Resistor .25W ±20%	Garrett	Philips	ST-4TA203
1	500kΩ	50V	VR2	Trimmer Resistor .25W ±20%	Garrett	Philips	ST-4TA504
Surface Mount Switch							
1	SPDT		SW1	4mm Selector Switch	Garrett	Philips	CS-412YTA
Surface Mount Inductors							
1	120nH		L2	Chip Inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-331XKBB
1	180nH		L1	Chip Inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-331XKBB
2	680nH		L4, L5	Chip Inductor 1008 ±10%	Digikey	TOKO	380NB-R68M
1	1.8µH		L7	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-1R8K
1	2.7µH		L9	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-2R7K
1	4.7µH		L3	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-4R7K
1	6.8µH		L6	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-6R8K
1	10µH		L8	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-100K

Table 4. Continued

Surface Mount Integrated Circuits							
1		5V	U1	FM IF with filter switch	Philips	Philips	SA639
1		5V	U2	Voltage comparator	Philips	Philips	LM311B
1		5V	U3	Dual D-type flip-flop	Philips	Philips	74HC74
1		5V	U4	Dual re-triggerable multivibrator	Philips	Philips	74HC123
Miscellaneous							
7			J1, J2, J3, J4, J5, J6, J7	SMA gold connector	Newark	EF Johnson	142-0701-801
1			JP1	8-pins header straight	Mouser	Molex	538-22-03-2081
1				Printed circuit board	Excel	Philips	DC10639
78 Total Parts							

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6. K. Feher, *Digital Communications, Satellite/Earth Station Engineering,* Prentice Hall, 1983.

IF quadrature transceiver SA1630

DESCRIPTION

The SA1630 is a 70–400 MHz I/Q transceiver for wireless LAN using direct controlled IF amplifier, a pair of quadrature down conversion mixers and a pair of baseband amplifiers. The transmit path contains a pair of quadrature up conversion mixers that transposes a quadrature baseband input signal up to IF frequency. An external VCO signal is divided internally and provides quadrature local oscillator signals for the mixers. Another divider chain, reference divider and phase detector are provided to avoid the need for an external synthesizer. To keep power consumption to a minimum the transmit, receive and local oscillator functions can be powered down under digital control.

FEATURES

- Low supply voltage operation of 2.7V for main chip and 2.9V for charge pump.
- Low current consumption: 33.5 mA in RX, 26.5 mA in TX, typical at 3V.
- Flexible power up/down options.
- Optional 2.5V regulated reference voltage available during transmit.
- Input/output IF frequency from 70–400 MHz.
- Internal IF PLL for synthesizing the local IF oscillator signal.
- Bandwidth of baseband Tx inputs is 20 MHz and that of baseband Rx outputs is 10 MHz.
- Designed for IEEE 802.11 wireless LAN using Direct Sequence Spread Spectrum modulation.
- Control registers power up in a default state.
- Optional quadrature phase trim capability.
- Only standard reference input frequency required, choice of 8, 11, 22 or 44 MHz.
- Digital IF gain control of 70 dB in steps of 2 dB.
- Package: LQFP–48

APPLICATIONS

- IF circuitry for IEEE 802.11 DSSS wireless LAN.
- Applications for high speed wireless data.

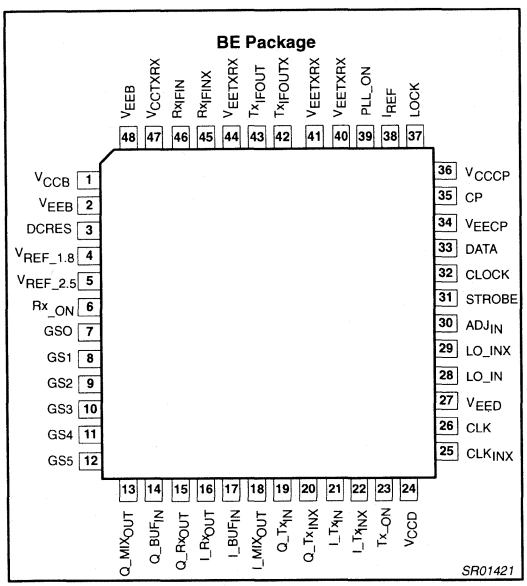


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48–Pin Plastic Low Profile Quad Flat package	–40 to +85°C	SA1630BE	SOT313–2

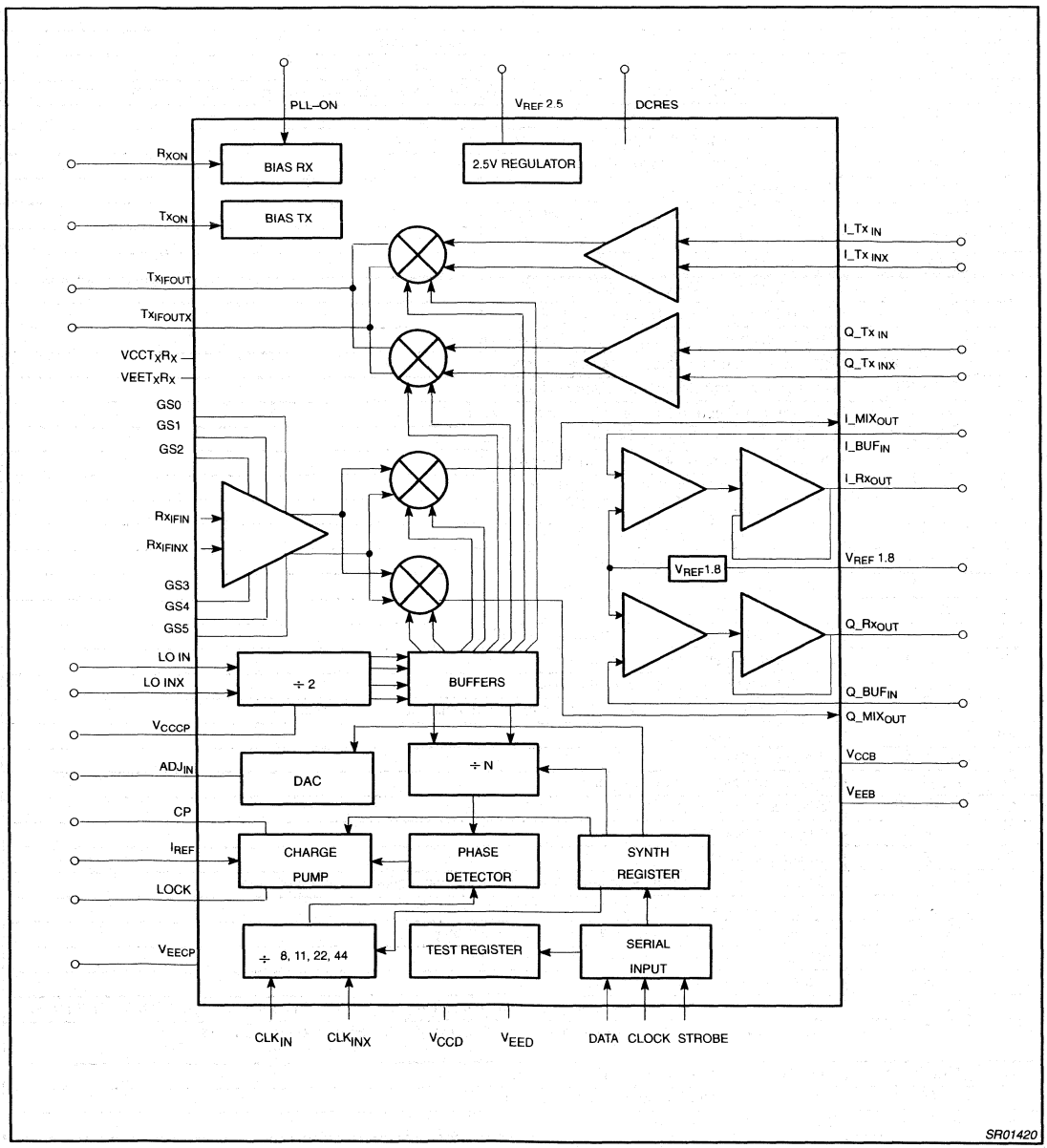


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VCCB	Supply Pin for Baseband and Bias circuits of R_x, bypassed suitably externally
2, 48	VEEB	Ground pins for Baseband and Bias Circuits of R_x. Needs low inductance separate path to system ground.
3	DCRES	Not used currently.
4	Vref_1.8	Reference Voltage Output (used for test only, do not connect)
5	Vref_2.5	Reference Voltage output in Tx mode for external use.
6	RX_ON	Rx enable CMOS signal input.
7	GS0	Control bit 0 for IF VGA Gain control, CMOS input
8	GS1	Control bit 1 for IF VGA Gain control, CMOS input
9	GS2	Control bit 2 for IF VGA Gain control, CMOS input
10	GS3	Control bit 3 for IF VGA Gain control, CMOS input
11	GS4	Control bit 4 for IF VGA Gain control, CMOS input
12	GS5	Control bit 5 for IF VGA Gain control, CMOS input
13	Q_MIXOUT	RX Q Mixer current output for external filtering
14	Q_BUFIN	Rx Q Buffer current input after external filtering
15	Q_RXOUT	Quadrature baseband voltage output, single–ended
16	I_RXOUT	In–phase baseband voltage output, single–ended
17	I_BUFIN	Rx I Buffer current input after external filtering
18	I_MIXOUT	Rx I Mixer current output for external filtering
19	Q_TXIN	Quadrature differential Tx baseband input
20	Q_TXINX	Quadrature differential Tx baseband input
21	I_TX IN	In–phase differential Tx baseband input
22	I_TX INX	In–phase differential Tx baseband input
23	TX_ON	Tx Enable CMOS input.
24	$V_{CC}D$	Digital circuit supply, bypassed suitably, externally.
25	CLKINX	Differential reference input for synthesizer
26	CLKIN	Differential reference input for synthesizer
27	VEED	Digital Ground, needs separate low inductance connection to system ground.
28	LO_IN	Differential LO input
29	LO_INX	Differential LO input
30	ADJIN	Used for test only. Do not connect
31	STROBE	Serial bus strobe input
32	CLOCK	Serial bus clock input
33	DATA	Serial bus data input
34	VEECP	Charge pump ground, needs separate low inductance connection to system ground.
35	CP	Charge pump output, connected to PLL loop filter.
36	VCCCP	Charge pump circuit supply, bypassed suitably externally
37	LOCK	Test control output and synthesizer lock indicator
38	IREF	Reference current for charge pump
39	PLL_ON	Power–on input (CMOS) for synthesizer circuits (active high). When LOW the entire chip goes into SLEEP mode.
40, 41, 44	VEETXRX	Ground pins for Tx and Rx. Needs separate low inductance connection to system ground.
42	TXIFOUTX	Differential transmitter IF output (open collector)
43	TXIFOUT	Differential transmitter IF output (open collector)
45	RXIFINX	Differential receiver IF input
46	RXIFIN	Differential receiver IF input
47	VCCTXRX	Supply for Tx and Rx. Bypass suitably externally

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to V_{CCXX}+0.3	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	300	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXXXX}	Supply voltages:	2.7 to 3.6	V
$V_{CC}CP$	Charge pump supply voltage	2.9 to 3.6	V
T_A	Operating ambient temperature range	-40 to +85	°C

POWER CONTROL

NO:	PLL_ON	RX_ON	TX_ON	STATE DESCRIPTION	MODE
1	0	0	0	SLEEP mode	SLEEP
2	1	0	0	Synthesizer ON, Rx STDBY, Tx OFF	WAIT
3	1	0	1	Synthesizer ON, Rx STDBY, Tx ON	TRANSMIT
4	1	1	0	Synthesizer ON, Rx ON, Tx OFF	RECEIVE
5	1	1	1	Synthesizer ON, Rx OFF, Tx ON	TRANSMIT

1. Sleep mode (PLL OFF, Rx OFF, Tx OFF)

In this mode everything is switched off except the 3–wire digital bus. As long as the digital supply is still on, the programmed values are active and the 3–wire bus will continue to be programmable.

2. Wait Mode (Tx Off, Rx Standby)

PLL is on. Receiver is in the reduced current standby mode and the transmitter is completely switched off. This mode maybe useful if the PLL is to be kept on and is waiting for a quick turn–on to either transmit or receive modes.

3. Transmit mode (Rx standby)

The PLL and transmitter are on. The receive section is in a reduced current mode wherein most of the Rx circuitry is powered down except for the bias and baseband circuits needed to hold the baseband output voltages in the active state. This mode is useful if the Rx baseband outputs are AC coupled via a large capacitor and the application demands quick turn–on for the Rx.

4. Receive Mode (Tx Off)

The Transmitter is completely shut–off. The PLL and receiver sections are operating.

5. Transmit Mode (Rx OFF)

PLL and Transmit sections are on. However, the Receiver is completely shut–down. This mode is useful if the Rx baseband outputs are DC coupled to the external world.

DC ELECTRICAL CHARACTERISTICS

V_{CC}XXX=+3V; V_{EE}XXX = 0V; TA=25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC-4}	Supply Current, Receive mode	PLL_ON=Rx_ON=Hi Tx_ON = Low		33.5	tbd	mA
I_{CC-2}	Supply Current, Wait mode	Wait mode (2) PLL_ON = Hi Tx_ON = Rx_ON = Low		17	tbd	mA
I_{CC-3}	Supply Current, Transmit mode	PLL_ON = TX_ON = Hi RX_ON = Low		26.5	tbd	mA
I_{CC-1}	Supply Current, Sleep mode	PLL_ON = Low RX_ON = Low TX_ON = Low		.068	tbd	mA
CMOS LOGIC INPUTS (DATA, CLOCK, STROBE)						
V_{IH}	Input logic 1 level		2.0		V_{CCD}	V
V_{IL}	Input logic 0 level		0		0.8	V
I_I	Input logic current				1	µA
C_I	Input logic capacitance				4	pF
CMOS Logic output (LOCK)						
V_{OH}	Output logic 1 level	I_O = –2mA	V_{CCD}–0.4			V
V_{OL}	Output logic 0 level	I_O = 2mA			0.4	V
CMOS Logic Inputs (PLL_ON, RX_ON, TX_ON)						
V_{IH}	Input logic 1 level		2.0		V_{CCTXRX}	V
V_{IL}	Input logic 0 level		0		0.8	V
I_I	Input logic current				1	µA

AC ELECTRICAL CHARACTERISTICS IF TRANSMIT MODULATOR

$V_{CC}XXX$ = TX_ON = PLL_ON = +3V; $V_{EE}XXX$ = RX_ON = 0V; LO_in = 100 mV peak at 704 MHz, CLKin = 100mV peak at 22 MHz, Ta = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX	
BW[4,5]	Input modulation bandwidth	500 ohms source impedance	22			MHz
V_{IN}	Input signal amplitude, Differential[1]	Vcm range		1		Vpp
THD	Total harmonic distortion[1]	Input signal amplitude[1] = 1 V_{PP}, 11 MHz		–50		dBc
R_{INTx}	Input resistance	Between pins I_T_XIN, I_T_XINX Q_T_XIN, Q_T_XINX		98		kΩ
C_{INTx}	Input Capacitance	Between pins I_T_XIN, I_T_XINX Q_T_XIN, Q_T_XINX			2	pF
	Output saturation limit	ITxIn = ITxinX = QTxin = QTxinX = $V_{CC}/2$	V_{CC}–0.3			V
	Mean output current	At T_XIF_{OUT} and T_XIF_{OUTX}		2		mA
	Output current DC offset	Mismatch at T_XIF_{OUT} and T_XIF_{OUTX}			20	µA
	Output Current[1,2]	At T_XIF_{OUT} and T_XIF_{OUTX}		0.475		mA rms
	Output differential voltaage[1,2]	400 Ω tuned load[2]		190		mV rms
f_{LO-IF}	LO feedthrough[1,3]	Differential output		–43	–30	dBc
	SSB Suppression [1,3]	f_{OUT} = 352 MHz	35	50		dBc
	Spot Noise[4] (Output Spectrum)	offset F1 (tbd) offset (tbd)		tbd tbd		dBc/Hz
ΔG[4]	Gain stability				2.0	dB
t_{ON}[4]	Turn–on time	T_X_ON, R_X_ON transition to transmit signal at 90% level		3		µs
T_{OFF}[4]	Turn–off time	T_X_ON, R_X_ON transition to transmit signal at 10% level		2		µs

NOTES:
1. I_TXIN = 0.25 Sin wmt, I_TXINX = 0.25 Sin wmt, Q_TXIN = 0.25 Sin (wmt–90), Q_TXINX = 0.25 Sin (wmt–90). The output spectrum will be a SSB one. The tone is at a frequency of 11 MHz.
2. The output current in each arm is the same but 180 degrees out of phase with each other. Also the tuned load of 400 ohms differential, is assumed. The power delivered to 400 ohms will be –10.4 dBm (typ.). The output current measurement is indirect based on output power measurement.
3. This is measured with respect to the SSB output.
4. Guaranteed by design and or characterization but not final tested.
5. The input bandwidth will be tested by measuring the output THD and signal level using a DSB spectrum where I = Q and the signal is a tone at 22 MHz.

AC ELECTRICAL CHARACTERISTICS IF RECEIVER DEMODULATOR

V_{CC}XXX = RX_ON = PLL_ON = +3V TO +5V, V_{EE}XXX = Tx_ON 0V; LO IN = 100 mV_{peak} at 704 MHz, CLKIN = 100mV_{peak}, at 22 MHz, Ta = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX	
RInRx	Differential input impedance	f_{IN} = 400 MHz		tbd		kΩ
VG	Voltage gain	AGC at maximum gain	tbd	83		dB
NF[1]	Input noise figure[6]	VGA at maximum gain		7.5		dB
	AGC range			70		dB
	AGC step size			2		dB
	AGC differential error				1	dB
	AGC settling time	any AGC step			200	nS
	Channel matching gain phase			0.2 1.0		dB deg
	Output voltage swing	V_{CC} = 3V, into Load[8]	1			Vpp
THD[9]	Total Harmonic Distortion	Max. Gain, rated output at 1 MHz		3		%
t_{ON}[4]	Turn–on time	R_X_ON, T_X_ON transition to baseband signal out			2	µs
t_{OFF}[4]	Turn–off time	R_X_ON, T_X_ON transition to no baseband signal out			2	µs

NOTES:

6. The Receive input is to be differential (using a balun or a differential source such as a differential SAW filter) and matched to external generator's impedance (ex: 50 ohms). The balun may or may not provide any impedance transformation depending on availability. An external L–C matching circuit can provide the rest of the impedance transformation as well absorb the input capacitance of the receiver input. Such a differential input scheme is mandatory to avoid pickup, and keep the noise figure low. A shunt resistor across the input (value TBD) will be used to set the input impedance as a compromise between the matching ease in production versus the noise figure of the receiver.
7. The system board layout has to keep the isolation between the receive inputs and the LO signal as high as possible. Otherwise the LO leakage will overload the receiver.
8. The load is 1000 ohms in parallel with 15pF of capacitor.
9. THD is total harmonic distortion. Since 3rd harmonic will dominate we will just measure this one.

AC ELECTRICAL CHARACTERISTICS IF SYNTHESIZER

$V_{CC}XXX$ = RX_ON = TX_ON = PLL_ON = +3V TO +5V, $V_{EE}XXX$ = 0V; LO_IN = 100 mV_{peak} at 704 MHz, CLKIN = 100mV_{peak} at 22 MHz, Ta = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX.	
f_{LO}	Local oscillator input frequency range		140		800	MHz
Z_{LOIN}	Differential input impedance	Between LO_IN and LO_INX		276 0.6		Ω pF
	LO input sensitivity	Single ended Referred to 50Ω	tbd		tbd	mVpp
	Programmable divider: division range step size		64	 1	511	
f_{CLK}	Reference clock frequency			8, 11, 22 or 44		MHz
Z_{CLKIN}	Differential input impedance	Between Clk_{IN} and Clk_{INX}		10 1.0		kΩ pF
	CLK input sensitivity	Referred to 50Ω	50	200	400	mVpk
f_C	Phase detector comparison frequency			1		MHz
I_{REF}	Charge pump reference current			31.25		µA
$\|I_{CP}\|$	Charge pump output current: C0...C2 = 000 C0...C2 = 111 step size	I_{REF} = 31.25 µA $V_{CP} = V_{CC}CP/2$		0.200 0.400 0.029		mA mA mA
$\frac{\Delta I_{CP}}{I_{CP}}$	Relative output current variation	I_{REF} = 31.25 µA		1.3	±10	%
ΔI_{CP_M}	Output current matching	I_{REF} = 31.25 µA $V_{CP} = V_{CC}CP/2$			±12	%
	Output current tolerance with programmed step with temperature with output voltage	CP between 0.8 V and V_{CC} CP = 0.8V		±10 ±10 ±5		%

APPLICATION DESCRIPTION

General

The 1630 performs the IF modulator and demodulator functionality for high–speed wireless data transceivers. The design is optimized for IEEE 802.11 wireless LAN using 11 chips/symbol Direct Sequence Spread Spectrum.

Transmitter

The IF quadrature transmitter baseband modulator input is driven from single–ended D/A converters in the DSP chip *using a minimum number of external components*. The baseband signals are DC coupled for fast turn–on and turn–off and for constant carrier testing. A constant output carrier is generated if ITXIN is high and QTXIN is low or vice versa, while this does not offset the ITXINX and QTXINX lines. This requires a good common–mode rejection of the baseband inputs (>20 dB). The typical common–mode input voltage is VCC/2.

The open collector outputs of the mixers are biased by two choke coils, which are part of an LC tank. The LC tank matches the output impedance of the mixers to the input impedance of the upconverter chip (or any filter in between) and suppresses IF harmonics.

Receiver

The receiver part of the SA1638 consists of an IF AGC amplifier, a quadrature demodulator and a pair of baseband amplifiers. The IF AGC amplifier has its gain controlled by the DSP chip. This ensures linear operation of the receiver chain over a wide dynamic range of input signals. Linear operation is essential for resolving echo's due to multipath reception.

The digital controlled AGC is meant for fast level training for the receiver. During message reception the digital AGC should not change state.

The high gain receiver, which is distributed between the IF and baseband part facilitates interfacing with the RF front–end chip, which normally have moderate gains (up to 20 dB), and SAW IF filters, which mostly have considerable loss (up to 8 dB) without external amplifiers.

The baseband amplifiers have a high drive capability (1 Vpp into 1kΩ, 15 pF for VCC = 3V) that facilitates direct interfacing to the A/D converter without active external elements.

Power control

The DSP chip contains power management logic that support at least three modes of operation: SLEEP (all off), Transmit (PLL on, Tx on, Rx standby) and Receive (PLL on, Rx on, Tx off) and supplies the corresponding logic control lines to the IF chip. The data transmission protocol requires fast transmit/receive turnaround times (2µs). The maximum power–up time from standby mode is 0.25 ms, which is determined by the PLL and VCO characteristics.

Local oscillator

The SA1630 has an integrated synthesizer that uses an external VCO operating on twice the IF frequency. It is internally divided by 2 for obtaining quadrature signals. The divided VCO signal is not

externally available. This minimizes the LO feedthrough to the IF input port and hence minimizes output dc glitches when the IF gain is switched.

The PLL reference clock is derived from the 22 MHz DSP clock. The available divider ratios facilitate both 1 and 2 MHz phase comparison frequency from a 22 MHz and an optional 44 MHz clock respectively. In essence the reference divider will have programmable dividers ratios of 8, 11, 22 and 44.

The VCO is fed from a stabilized supply. Such a stabilized supply is necessary in order to prevent oscillator jitters due to Rx/Tx switching. The effect of oscillator jitters is further minimized when using a high PLL loop bandwidth, which on its turn requires a high phase comparison frequency (1 MHz, preferably 2 MHz).

Low voltage IF I/Q transceiver SA1638

DESCRIPTION

The SA1638 is a combined Rx and Tx IF I/Q circuit. The receive path contains an IF amplifier, a pair of quadrature down-mixers, and a pair of baseband filters and amplifiers. A second pair of mixers in the transmit path transposes a quadrature baseband input up to the IF frequency. An external VCO signal is divided down internally and buffered to provide quadrature local oscillator signals for the mixers. A further divider chain, reference divider and phase detector are provided to avoid the need for an external IF synthesizer. Rx or Tx path or the entire circuit may be powered down by logic inputs. On-board voltage regulators are provided to allow direct connection to a battery supply.

FEATURES

- Direct supply: 3.3V to 7.5V
- Two DC regulators giving 3.0V output
- Low current consumption: 18mA for Rx or 22mA for Tx
- Input/output IF frequency from 70-400 MHz
- Internal IF PLL for synthesizing the local oscillator signal
- High performance on-board integrated receive filters with bandwidth tunable between 50-850 kHz
- Switchable alternative bandwidth setting available to allow channel bandwidth flexibility in operation
- Designed for a widely used I and Q baseband GSM interface
- Control registers power up in a default state
- Optional DC offset trim capability to <200mV
- Only a standard reference input frequency required, choice of 13, 26, 39 or 52MHz
- Fully compatible with SA1620 GSM RF front-end (see Figure 9)

APPLICATIONS

- IF circuitry for GSM 900MHz hand-held units
- IF circuitry for PCN (DCS1800) hand-held units
- Quadrature up and down mixer stage

PIN CONFIGURATION

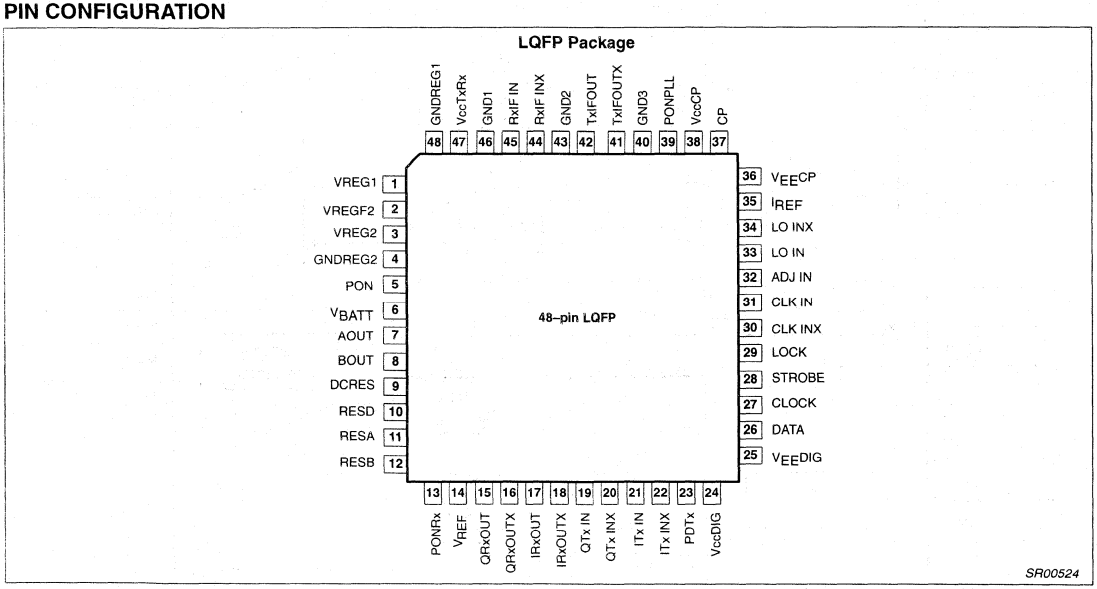


Figure 1. SA1638 Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (LQFP)	-40 to +85°C	SA1638BE	SOT313-2

BLOCK DIAGRAM

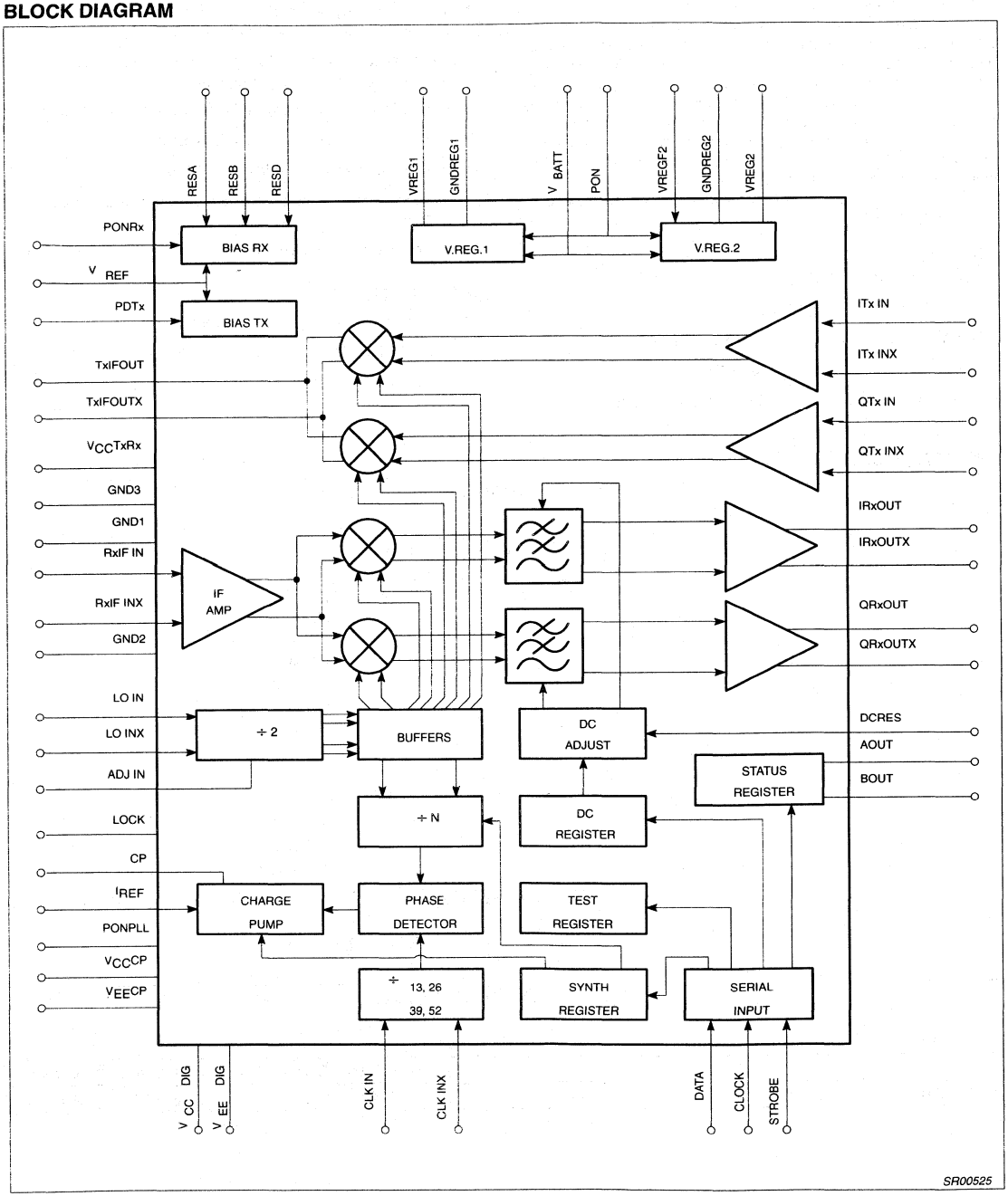


Figure 2. SA1638 Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VREG1	Output voltage of regulator 1
2	VREGF2	Feedback of regulator 2
3	VREG2	Output voltage of regulator 2
4	GNDREG2	Ground of regulator 2
5	PON	Power-on input for voltage regulators 1 and 2 (active high)
6	V_{BATT}	Input voltage for regulators 1 and 2
7	AOUT	Programmable logic output (see Figure 9)
8	BOUT	Programmable logic output (see Figure 9)
9	DCRES	Reference current setting resistor for DC offset circuit
10	RESD	Additional external current defining resistor for filters
11	RESA	Principal external current defining resistor for filters
12	RESB	Principal external current defining resistor for filters
13	PONRx	Power-on input for Rx (active high)
14	V_{REF}	Reference voltage
15	QRxOUT	Differential receive baseband output
16	QRxOUTX	Differential receive baseband output
17	IRxOUT	Differential receive baseband output
18	IRxOUTX	Differential receive baseband output
19	QTx IN	Differential transmit baseband input
20	QTx INX	Differential transmit baseband input
21	ITx IN	Differential transmit baseband input
22	ITx INX	Differential transmit baseband input
23	PDTx	Power-on for transmitter (active low)
24	V_{CC}DIG	Digital circuit supply
25	V_{EE}DIG	Digital ground
26	DATA	Serial bus data input
27	CLOCK	Serial bus clock input
28	STROBE	Serial bus strobe input
29	LOCK	Test control/synthesizer lock indicator
30	CLK INX	Differential reference divider input
31	CLK IN	Differential reference divider input
32	ADJ IN	Used for test only. Do not connect
33	LO IN	Differential LO input
34	LO INX	Differential LO input
35	I_{REF}	Reference current setting for charge pump
36	V_{EE}CP	Charge pump ground
37	CP	Charge pump output
38	V_{CC}CP	Charge pump circuit supply
39	POnPLL	Power-on input for synthesizer circuits (active high)
40	GND3	Ground (internal connection to GND1 and GND2)
41	TxIFOUTX	Differential transmit IFoutput (open collector)
42	TxIFOUT	Differential transmit IFoutput (open collector)
43	GND2	Ground (internal connection to GND1 and GND3)
44	RxIF INX	Differential receive IF input
45	RxIF IN	Differential receive IF input
46	GND1	Ground (internal connection to GND2 and GND3)
47	V_{CC}TxRx	Transmit and receive circuits supply voltage (also feedback of Regulator 1)
48	GNDREG1	Ground of regulator 1

NOTE: There are no ESD protection diodes at Pins 41 and 42. Thus, open collector outputs may have increased DC voltage or higher AC peak voltage.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC}XXX$	Supply voltages: $V_{CC}TxRx$, $V_{CC}DIG$, $V_{CC}CP$	-0.3 to +6.0	V
V_{BATT}	Battery voltage	-0.3 to +8.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CCXXX}+0.3)	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	300	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}. 48-pin LQFP: θ_{JA} = 67°C/W.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC}XXX$	Supply voltages: $V_{CC}TxRx$, $V_{CC}DIG$	2.7 to 5.5	V
$V_{CC}CP$	Charge pump supply voltage	2.9 to 5.5	V
V_{BATT}	Battery voltage	3.3 to 7.5	V
T_A	Operating ambient temperature range	-40 to +85	°C

Voltage Regulators

T_A = 25°C, P_{ON} = 3V, $P_{ON}RX$ = 0V, PDTX = 3V, $P_{ON}PLL$ = 0V, V_{BATT} = 3.3V, $I_{OUT}1$ = $I_{OUT}2$ = 15mA, $V_{REG}1$ connected to $V_{CC}TxRx$, $V_{REG}2$ connected to $V_{REG}F2$; $V_{CC}DIG$ = $V_{CC}CP$ = 3V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			Min	–3σ	Typ	+3σ	Max	
$V_{REG}1$, $V_{REG}2$	Nominal V_{OUT}		2.85	2.93	3.00	3.07	3.15	V
V_{BATT}			3.3				7.5	V
$I_{OUT}1$, $I_{OUT}2$	Maximum output current for each regulator[1]						30	mA
I_{BATT}	Supply current for both regulators	I_{LOAD} = 0mA		4.3	5	5.7	7	mA
$I_{BATT\ PD}$	Power-down supply current	P_{ON} = 0V, I_{LOAD} = 0mA		7.7	9	10.3	15	µA
$C_{REG}1$[2]	$V_{REG}1$ cap load		0.1				1000	µF
$C_{REG}2$[2]	$V_{REG}2$ cap load		0.1				500	µF
LINEREG	Line regulation	DC, V_{BATT} = 3.3V to 7.5V	–0.4	–0.2	0.001	0.2	0.4	%
LOADREG	Load regulation	I_{LOAD} = 15mA to 30mA	–5	–0.37	-0.17	0.03	5	%
BW	Bandwidth		100					kHz
F_{PON}	Feedthrough attenuation from P_{ON} to each regulator				≤ -40			dB
F_{REG}	Feedthrough attenuation from V_{BATT} to each regulator	f ≤ 100kHz f = 10MHz f = 100MHz f = 400MHz			≤ -61 ≤ -32 ≤ -37 ≤ -48			dB
t_{ON}	Turn ON time				10			µs

NOTES:
1. At $T_j \geq$ 150°C a thermal switch reduces the output current to avoid damage.
2. Recommended load capacitors: In every case $C_{REG}1$ = $C_{REG}2$ = 100nF to ground with series resistance ≤0.1Ω. Additional capacitor optional ≤1000µF with series resistance ≤5Ω. The low series resistance is very important to ensure regulator stability.
3. Standard deviations are based on the characterization results of 90 ICs.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}TxRx=V_{CC}DIG=V_{CC}CP=PONRx=PONPLL=$ +3V; $V_{EE}DIG = V_{EE}CP=GND1=GND2=GND3=PDTx$ = 0V; T_A = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	−3σ	TYP	+3σ	MAX	
I_{CC}	Supply current							mA
	Rx and IF synthesizer active	PONRx = PONPLL = PDTx = Hi		14.4	16	17.6	20	
	Tx and IF synthesizer active	PONRx = PDTx = Low; PONPLL = Hi		17.4	19.5	21.6	24	
	Power-down mode	PONRx = PONPLL = Low; PDTx = Hi			0.068			
V_{REF}	Reference voltage	Generated internally		1.39	1.57	1.75		V
IV_{REF}	V_{REF} I_{SINK} I_{SOURCE}				5 5			µA
I_{OUT}	DC output current	At pins TxIFOUT and TxIFOUTX	1.5	1.86	2.0	2.14	2.7	mA
Digital inputs (P_{ON})								
V_{IH}	High level input voltage range		2.0				V_{BATT}	V
V_{IL}	Low level input voltage range		0				0.8	V
Digital inputs (PDTx, P_{ON}Rx, P_{ON}PLL, P_{ON})								
V_{IH}	High level input voltage range		2.0				$V_{CC}TxRx$	V
V_{IL}	Low level input voltage range		0				0.8	V
Digital inputs (Clock, Data, Strobe)								
V_{IH}	High level input voltage range		2.0				$V_{CC}Dig$	V
V_{IL}	Low level input voltage range		0				0.8	V
Digital outputs (LOCK, AOUT, BOUT)								
V_{OH}	Output voltage HIGH	I_O = -2mA	$V_{CC}DIG-0.4$					V
V_{OL}	Output voltage LOW	I_O = 2mA					0.4	V

AC ELECTRICAL CHARACTERISTICS

$V_{CC}TxRx=V_{CC}DIG=V_{CC}CP=PONRx=PONPLL=$ +3V; $V_{EE}DIG = V_{EE}CP=GND1=GND2=GND3=PDTx$ = 0V; LO_{IN} = 100mV$_{PEAK}$, 800MHz; CLK_{IN} = 100mV$_{PEAK}$, 52MHz; serial registers programmed with default values; T_A = 25°C unless otherwise stated. Test Circuit Figure 8.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	−3σ	TYP	+3σ	MAX	
IF Transmit Modulator								
BW	Input modulation bandwidth	200Ω source impedance		0.82	0.94	1.06		MHz
V_{COM}	Common mode range for baseband inputs	DC at pins ITxIN, ITxINx, QTxIN, QTxINx	1		1.5		2	V
V_{IN}	Peak input signal amplitude	Centered on V_{COM}			0.75			V
	Third harmonic distortion[1]	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75V$_{PEAK}$; fin = 20kHz		-61	-57	-53	-40	dB
R_{INTx}	Input resistance	Between pins: ITxIn and ITxInX or QTxIn and QTxInX	112					kΩ
C_{INTx}	Input capacitance	At ITxIn, ITxInX, QTxIn, QTxInX					10	pF
	Output saturation limit						$V_{CC}TxRx$-0.3	V
I_{OUT}	RMS output current	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75V$_{PEAK}$	0.6	0.73	0.82	0.91	1.08	mA
S_{LO}	LO suppression[1]	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75V$_{PEAK}$; fin = 20k	+30		+43			dB
SSB	Sideband suppression[1]	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75V$_{PEAK}$; fin = 20k	+35		+50			dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	−3σ	TYP	+3σ	MAX	
IF Transmit Modulator (continued)								
	Noise density at 600kHz	|ITxInI = |ITxInXI = |QTxInI = |QTxInXI = 0.75V_{PEAK}		-130	-129	-128		dBc/Hz
	Noise density at 10MHz			-133	-131	-129		
t_{ON}	Turn ON time	PdTx = LO, transmit signal to 90%			5			µs
t_{OFF}	Turn OFF time	PdTx = HI, transmit signal to 10%			5			µs
IF Receiver (R = 36kΩ between pins RESA and RESB)								
RInRx	Differential input impedance	f_{IN} = 400MHz			5 || 0.6			kΩ || pF
ROutRx	Output impedance				1			kΩ
	Output common mode voltage				V_{REF}			V
f3dB	Low pass filter -3dB bandwidth		70		83		90	kHz
	Low pass filter attenuation: 200kHz 400kHz 600kHz 6.5MHz 13.0MHz		 6.5 30	 8.9 38.1	 10.7 45 70 >80 >80	 12.5 51.9		dB
VG	Voltage gain	Differential output PD into GSM baseband relative to 1200Ω source EMF	43	49.4	51	52.7	58	dB
NF	Noise figure[8]	1200Ω source and external matching resistor and inductor		5.7	7.0	8.3		dB
	Channel matching: Gain Phase	f_{IN} = 400.005MHz	-1.5		 -0.26 0.0		1.5	 dB degrees
	Output DC offset[2]	Differential, DCRES=100kΩ	-200		-25		200	mV
I_{OUT}	Output drive current at each pin	Source (Sink)			10 (700)			µA
V_{OUT}	Minimum differential output swing				2.0			V
P_{-1dB}	Input 1dB compression point: In band 200kHz 400kHz 600kHz	1200Ω source EMF	 -59 -54	 -55.3 -49.3	 -53 -47 -47 -47	 -50.7 -44.8	 -47 -40	dBV
t_{ON}	Turn ON time[3]	POnRx = HI, to baseband signal out			2			µs
t_{OFF}	Turn OFF time	POnRx = LO, to no baseband signal out			2			µs
IF Synthesizer								
f_{LO}	Local oscillator input frequency range[9]		140				800	MHz
Z_{LOIN}	Differential input impedance	Between pins LO_{IN} and $LO_{IN}X$, f_{IN} = 800MHz			276 || 0.6			Ω || pF
V_{LOIN}	LO peak input voltage range	Single-ended Referred to 50Ω	50				100	mV
	Programmable divider: Division range Step size		64		 1		511	
f_{CLKIN}	Reference clock input frequency	V_{CLKIN} = 100mV$_{PEAK}$					52	MHz
Z_{CLKIN}	Differential input impedance	Between pins ClkIn and ClkInX			10 || 1.0			kΩ || pF
V_{CLKIN}	CLK_{IN} peak input voltage range	Single-ended, referred to 50Ω	50				400	mV
I_{REF}	Charge pump input reference current				31.2			µA
$\|I_{CP}\|$	Charge pump output current: c0...c2 = 000 c0...c2 = 111 Step size	I_{REF} =31.2µA, V_{CP} = V_{CC}CP/2	0.425 0.85 0.045	0.487 0.979 0.062	0.5 1.0 0.071	0.513 1.021 0.08	0.575 1.15 0.105	mA

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
IF Synthesizer (cont.)								
$\frac{\Delta I_{CP}}{I_{CP}}$	Relative output current variation[4]	I_{REF} =31.2µA		0.1	1.3	2.5	±10	%
ΔI_{CP_M}	Output current matching[5]	I_{REF} =31.2µA, $V_{CP} = V_{CC}CP/2$					±12	%
$\lvert I_{CP\_L} \rvert$	Output leakage current	V_{CP} = 0.3V to V_{CC}CP-0.3V		-0.02	0.1	0.22	±15	nA
t_{ON}	Turn ON time	POnPLL = HI, to full charge pump current			15			µs
t_{OFF}	Turn OFF time[6]	POnPLL = LO, to I_{CC}CP, I_{CC}DIG <5% of operational supply current			15			µs
Serial Interface[7]								
f_{CLOCK}	Clock frequency						10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30					ns
t_H	Hold time: CLOCK to DATA		30					ns
t_W	Pulse width: CLOCK		30					ns
	Pulse width: STROBE		30					

NOTES:

1. Parameter measured relative to modulation sideband amplitude.
2. After programming the DC offset register for minimum offset. DCRES = 100kΩ.
3. The turn on time relates only to the power up time of the circuit. The settling time of the integrated baseband filters has to be added (for GSM–mode = 8µs with filter bandwidth setting resistor = 36kΩ).
4. The relative output current variation is defined thus: $\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{\lvert(I_2 + I_1)\rvert}$; with V_1 = 0.3V, $V_2 = V_{CC}CP - 0.3V$ (see Figure 3).
5. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on.
6. As soon as P_{ON}PLL is set to LO, the phase detector is reset and no charge pumps pulses are generated.
7. Guaranteed by design.
8. $NF = \left[20 \log \left(\frac{E_{no}}{\sqrt{4kTR}} \right) \right] - VG$ where, E_{no} is the output noise voltage measured in a 1Hz bandwidth, R = 1200Ω, VG = gain in dB.
9. Minimum frequency is guaranteed by design.

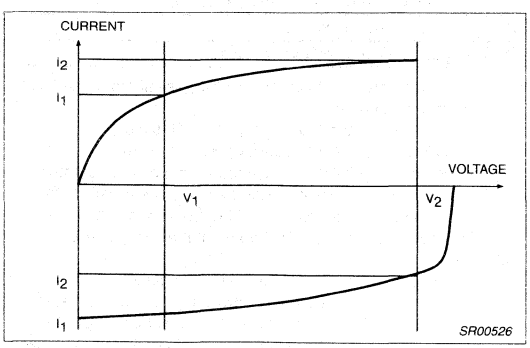


Figure 3. Relative Output Current Variation

FUNCTIONAL DESCRIPTION

Serial Programming Input

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program the counter ratios, charge pump current, status- and DC-offset register, mode select and test register. The programming data is structured into two 21-bit words; each word includes 4 chip address bits and 1 subaddress bit. Figure 2 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the value of the subaddress bit the data is latched into different working registers. Table 3 shows the contents of each word.

Default States

Upon power up (V_{CC}DIG is applied) a reset signal is generated, which sets all registers to a default state. The logic level at the STROBE pin should be low during power up to guarantee a proper reset. These default states are shown in Table 3.

Reference Divider

The reference divider can be programmed to four different division ratios (:13, :26, :39, :52), see registers r0, r1; default setting: divide by 13.

Main Divider

The external VCO signal, applied to the LO_{IN} and $LO_{IN}X$ inputs, is divided by two and then fed to the main divider (:N). The main divider is a programmable 9 bit divider, the minimum division ratio is

divide by 64. The division ratio is binary coded and set in the registers n0 to n8. The default setting is a divide by 400.

At the completion of a main divider cycle, a main divider output is generated which will drive the phase detector.

Phase Detector

The phase detector is a D-type flip-flop phase and frequency detector shown in Figure 5. The flip-flops are set by the negative edges of the output signals of the dividers. The rising edge of the signal L will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump acts to increase the VCO frequency; a sink current acts to decrease the VCO frequency.

Current Setting

The charge pump current is defined by the current set between the pin I_{REF} and $V_{EE}CP$. The current value to be set there is 31.2µA. This current can be set by an external resistor to be connected between the pin I_{REF} and $V_{EE}CP$. The typical value R_{EXT} (current setting resistor) can be calculated with the formula

$$R_{EXT} = \frac{V_{CC}CP - 1.4V}{31.2\mu A}$$

The current can be set to zero by connecting the pin I_{REF} to $V_{CC}CP$.

Charge Pumps

The charge pumps at pin CP are driven by the phase dectector and the current value is determined by the binary value of the charge pumps register CN = c2, c1, c0, default 1mA. The active charge pump current is typically:

$$|I_{CP}| = (c0 + 2c1 + 4c2) \cdot 71\mu A + 500\mu A$$

Lock Detect

The output LOCK is H when the phase detector indicates a lock condition. This condition is defined as a phase difference of less than ±1 cycle on the reference input CLK_{IN}, $CLK_{IN}X$.

Test Modes (Synthesizer, Transmit Mixer)

The LOCK output is selectable as a test output. Bits x0, x1 control the selection, the default setting is normal lock output as described in the Lock detect section. The selection of a Bit x0, x1 combination has a twofold effect: First it routes a divider output signal to the LOCK pin, second it disables mixer stages in the transmit path. Setting x0,1 = 11 disables both transmit path mixers. This mode can be used to prevent the transmitter from producing an IF output signal even if the transmit part is powered on (PDTx = 0V). This can be used to simplify the control timing while commanding the transmit and receive simultaneously without the transmit part causing interference.

Table 1. Test Modes

x0	x1	Synthesizer Signal at LOCK Pin	Transmit Mixer	
			Q-mixer	I-mixer
0	0	normal lock detect	on	on
1	0	CLK_{IN} divided by reference divider ratio	off	on
0	1	$LO_{IN} \div 2$ * (main divider ratio)	on	off
1	1	main divider output, that goes to the phase detector	off	off

Status Register

The s0 and s1 status bits determine the values of the logic output pins A_{OUT} and B_{OUT}. These outputs can be connected to the AGC control inputs A and B of the SA1620. (See Figure 9)

DC Offset Register

Registers i0 to i3 and q0 to q3 control a correction to the output DC offset of the I and Q channels of the receiver. The polarity of the DC offset correction in the I and Q channels are determined by i0 and q0, respectively. The other bits set the magnitude of the offset correction. The step size of the two offset correction DACs is fixed by an external resistor between the DCRES pin and ground. A value of 120kΩ will give a step size of 200mV.

Mode Select Register

t0: switches the RX IF gain.
- t0 = 0 no attenuation
- t0 = 1 10dB attenuation

The attenuation switch is included between the IF amplifier and the I and Q mixers, thereby influencing the noise figure negligibly. The purpose of this switch is to provide another AGC step which does not influence the receiver noise figure. Please note that this gain change will influence the DC offset of the I and Q mixers.

t1 = 0 test mode only, always to be set to 0.

t2, t3 sets the mode of the level locked loop (LLL)

The LLL is a circuit which processes the LO input signal in order to provide an LO signal with a perfect 50% duty cycle, which determines the precision of the 90° shift of the I and Q mixing signals generated by the ÷2 divider. For an external tuning of the 90° phase shift of the I and Q mixing signals, a trimming resistor may be connected (but is not required) between the ADJ_{IN} pin and ground, and the LLL has to be put in one of the following modes:

Table 2. Mode Select Register

t2	t3	LLL Status
0	0	LLL on (no external tune, monitor performance, default)
0	1	LLL on (with medium external tune)
1	0	LLL off (tune externally)
1	1	LLL on (with fine external tune)

t4 selects the bandwidth of the RC low pass filters at the I, Q Rx mixer outputs
- t4 = 0 cutt-off frequency (-3dB) 110kHz
- t4 = 1 cutt-off frequency (-3dB) 792kHz

t5 selects the bandwidth of the integrated 5th-order gyrator filters. The filters are tuneable over a range of 50kHz to 1MHz with external resistors. The -3dB bandwidth is inversely proportional to the value of the external resistor.

With t5, two external resistor values are selectable.
- t5 = 0 the resistance between the pins RESA and RESB determines the cutoff frequency. For GSM a nominal bandwidth of 80kHz is chosen when the external resistor is 36kΩ.
- t5 = 1 a second resistor between the pins RESB and RESD is connected in parallel to the first external resistor, thus increasing the filter bandwidth. The relative amplification is decreased in this mode.

The overall filter response in the receive section is the sum of the filter responses of the passive RC low-pass filter and the active gyrator filter.

Power Down Modes

There are 4 power-on pins in the SA1638: P_{ON}, P_{ON}Rx, PDTx, P_{ON}PLL.

P_{ON} = H powers up both voltage regulators $V_{REG}1$ and $V_{REG}2$. P_{ON} should be set to L, if these internal voltage regulators are not to be used.

P_{ON}Rx = H powers up the receiver part.

PDTx = L powers up the transmitter part.

P_{ON}PLL = H powers up the synthesizer part. As it also powers up the first divide by 2 stage for generating the 0/90 degree phase shifted signals for the transmit and receive mixers, it also has to be set H if either the transmit part or the receive part is used. P_{ON}PLL = L powers down the dividers, resets the phase detector and disconnects the current setting pin I_{REF}. In P_{ON}PLL = L mode, the values in the serial input registers are still kept and the part still can be reprogrammed as long as V_{CC}DIG is present.

Table 3. Definition of SA1638 Serial Registers

First data word: (shown with default values)

Address SA1638				Sub Adr	N-Divider									Ref ÷ Reg		Charge-Pump			Reg Test	
MSB																				LSB
a0	a1	a2	a3	sa	n0	n1	n2	n3	n4	n5	n6	n7	n8	r0	r1	c0	c1	c2	x0	x1
1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	1	1	1	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 0 for first data word
N-Divider:	9 bits, n0...n8, values 64 (00100 0000) to 511 (111111111) allowed for IF-choice, default 400
Reference Divider Register:	2 bits, r0...r1, 00 = ÷13, 01 = ÷26, 10 = ÷39, 11 = ÷52. Default: 00
Charge-Pump Register:	3 bits, c0...c2, Binary current setting factor for charge pumps, values 000 = minimum current to 111 = maximum current, default maximum charge pump current
Test Register:	2 bits, x0...x1, default 00, see Functional Description

Second data word: (shown with default values)

Address SA1638				Sub Adr	Status Reg	DC Offset Register								Mode Select Register					
						Q-Channel				I-Channel									
MSB																			LSB
a0	a1	a2	a3	sa	s0	s1	q0	q1	q2	q3	i0	i1	i2	i3	t0	t1	t2	t3	t4	t5
1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 1 for second data word
Status Register:	2 bits, s0 sets pin A_{OUT}, s1 sets pin B_{OUT}, see Functional Description
DC Offset Register:	4 bits per channel, i0...i3 and q0...q3, no correction as default i0 and q0 switches offset polarity, 0 to lower voltage, 1 to higher voltage il...i3 and q1...q3, 000 no correction to 111 max. correction enabled
Mode Select Register:	6 bits, t0...t5, 000000 = normal GSM-Operation as default, see Functional Description

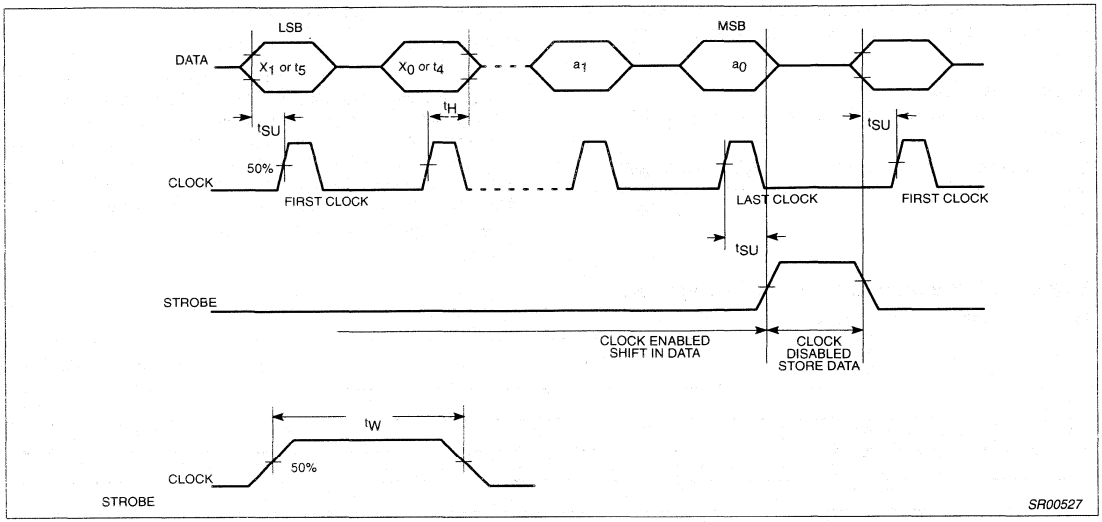


Figure 4. Serial Input Timing Sequence

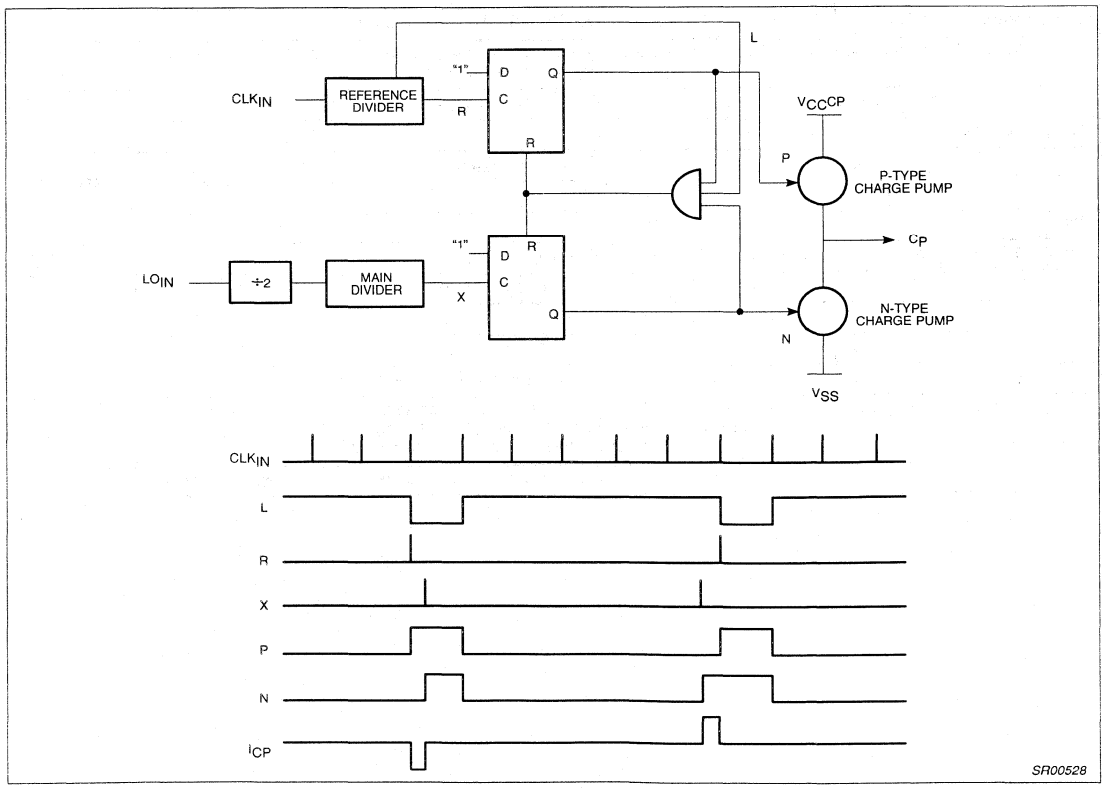
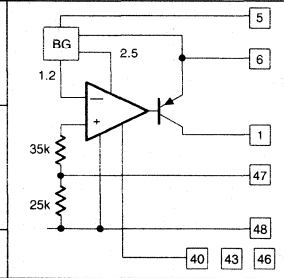
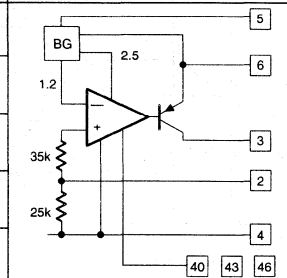
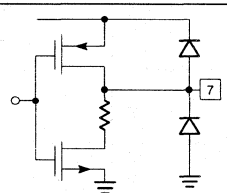
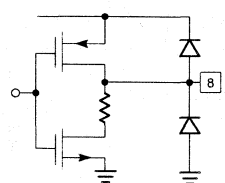
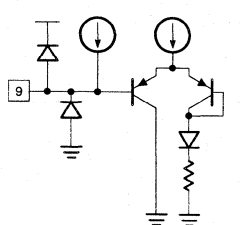


Figure 5. Phase Detector Structure with Timing

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
47	$V_{CC}TxRx$	3.0	
48	$GND_{REG}1$	0.0	
1	$V_{REG}1$	3.0	
2	$V_{REG}F2$	3.0	
3	$V_{REG}2$	3.0	
4	$GND_{REG}2$	0.0	
5	P_{ON}	3.3	
6	V_{BATT}	3.3	
7	A_{OUT}	3.0	
8	B_{OUT}	3.0	
9	DC_{RES}	1.6	

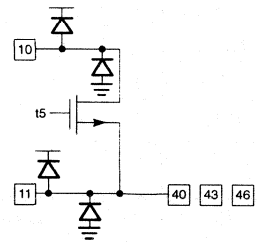
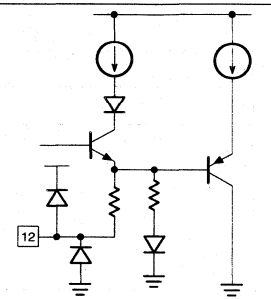
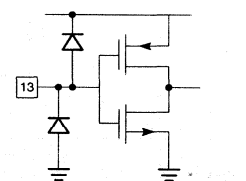
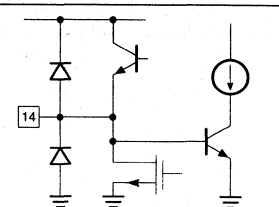
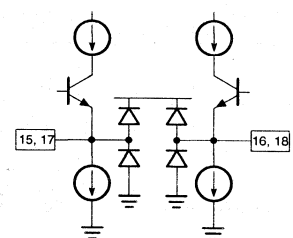
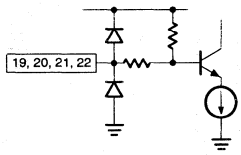
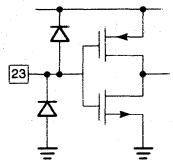
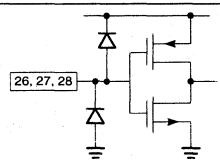
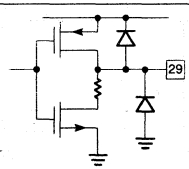
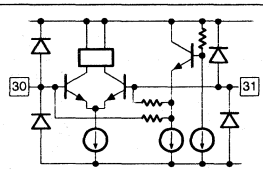
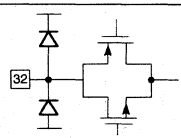
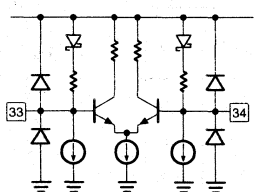
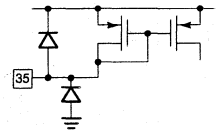
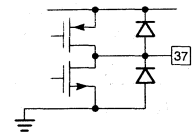
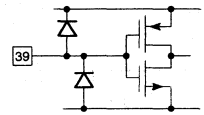
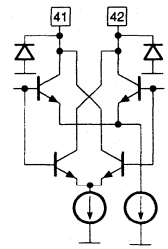
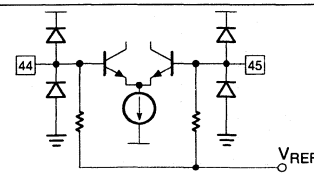
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
10	RES_D	0.05	
11	RES_A	0.00	
12	RES_B	0.05	
13	$P_{ON}Rx$	3.0	
14	V_{REF}	1.5	
15	QRX_{OUT}	1.5	
16	$QRX_{OUT}X$	1.5	
17	IRX_{OUT}	1.5	
18	$IRX_{OUT}X$	1.5	

Figure 6. Pin Functions

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
19	QTX_{IN}	1.5	
20	$QTX_{IN}X$	1.5	
21	ITX_{IN}	1.5	
22	$ITX_{IN}X$	1.5	
23	PdTx	0.0	
24	$V_{CC}DIG$	3.0	
25	$V_{EE}DIG$	3.0	
26	DATA		
27	CLOCK		
28	STROBE		
29	LOCK		
30	CLK_{IN}	2.0	
31	$CLK_{IN}X$	2.0	
32	ADJ_{IN}	2.0	
33	LO_{IN}	2.0	
34	$LO_{IN}X$	2.0	

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
35	I_{REF}	1.6	
36	$V_{EE}CP$	0.0	
37	CP		
38	$V_{CC}CP$	3.0	
39	$P_{ON}PLL$	3.0	
40	GND3	0.0	
41	$TXIF_{OUT}X$	OPEN COLLECTOR	
42	$TXIF_{OUT}X$	OPEN COLLECTOR	
43	GND2	0.0	
44	$RxIF_{IN}X$	1.5	
45	$RxIF_{IN}$	1.5	
46	GND1	0.0	
47	$V_{CC}TxRx$	3.0	
48	$GND_{REG}1$	0.0	

SR00530

Figure 7. Pin Functions (cont.)

Overview of Dual GSM/PCN Architecture

The SA1620 RF front-end and SA1638 IF transceivers form a dual conversion architecture which uses a common IF and standard I/Q baseband interface for both transmit and receive paths. The time division multiplex nature of the GSM system permits integration of the transmit and receive functions together on the one RF and one IF chips. This simplifies the distribution of local oscillator signals, maximizes circuitry commonality, and reduces power consumption.

The SA1620 and SA1638 allow considerable flexibility to optimize the transceiver design for particular price/size/performance requirements, through choice of appropriate RF and IF filters. The IF may be chosen freely in the range 70–400 MHz. The same IF can be used in the transmit and receive directions. Alternately, different IFs can be used if the SA1638 synthesizer frequency is switched between transmit and receive timeslots. The comparison frequency of the SA1638 PLL is high in order to provide fast switching time.

With suitable choice of the IF, an identical SA1638 IF receiver design can be used for both 900MHz GSM and 1800MHz PCN (DCS1800) equipment.

General Benefits/Advantages

- 2.7V operation. Compatible with 3V digital technology and portable applications. (Higher voltage operation also possible, if desired.)
- Excellent dynamic range. The availability of two LNAs in the SA1620 allows flexibility in receiver dynamic design for portable and mobile GSM spec. applications with appropriate filters. If for a particular application a GaAs or discrete front-end is desired, one of the LNAs can be left unpowered. Placing the AGC gain switches at the front results in some attenuation most of the time, further increasing typical dynamic performance beyond that specified by GSM.
- High power transmit output driver, delivering +7.5dBm output. This is sufficient to drive a filter and power amplifier input, without a driver amplifier. To avoid unnecessary current consumption, the output power can be reduced to an appropriate level by choice of an external resistor.
- DC offsets generated in the receive channel are independent of the LNA AGC setting, and correctable by software to prevent erosion of signal handling dynamic range by DC offsets.
- Minimal high-quality filter requirements. As a result of the integration in the SA1638 of high quality channel selectivity filters, only sufficient filtering is needed in the receive path to provide blocking protection for the second mixers. This reduces receiver cost and size.
- Operation at a high IF allows RF image reject filter requirements to be relaxed. For example, at a 400MHz IF, the natural gain roll-off in the SA1620 LNAs and mixer suppresses the image signal in the 1800MHz band by typically 28dB below the desired 900MHz band signal.

DC Offset Correction

DC offset correction is provided by two DACs each feeding into one of the two Rx channels. The step size of both DACs is set by the value of the external resistor between DCRES and ground. Thus any original offset less than 1.5V magnitude in either channel can be reduced to the specified level by selecting the appropriate DAC setting via the serial interface.

Integrated Receive Filters

The low-pass characteristics of the Rx channel are determined by two low-pass responses. The first of these is a passive filter at the output of the quadrature mixers and the second is the low-pass filters which follow the post-mixer amplifiers. These specifications refer only to the response of the default state, but this may be switched by the control register to an alternative setting with a nominal 3dB point of 792kHz.

The corner frequency of the low pass filters can be adjusted over a wide range by varying the value of the external resistor between RESA and RESB. The range of feasible corner frequencies extends at least between 50kHz and 500kHz.

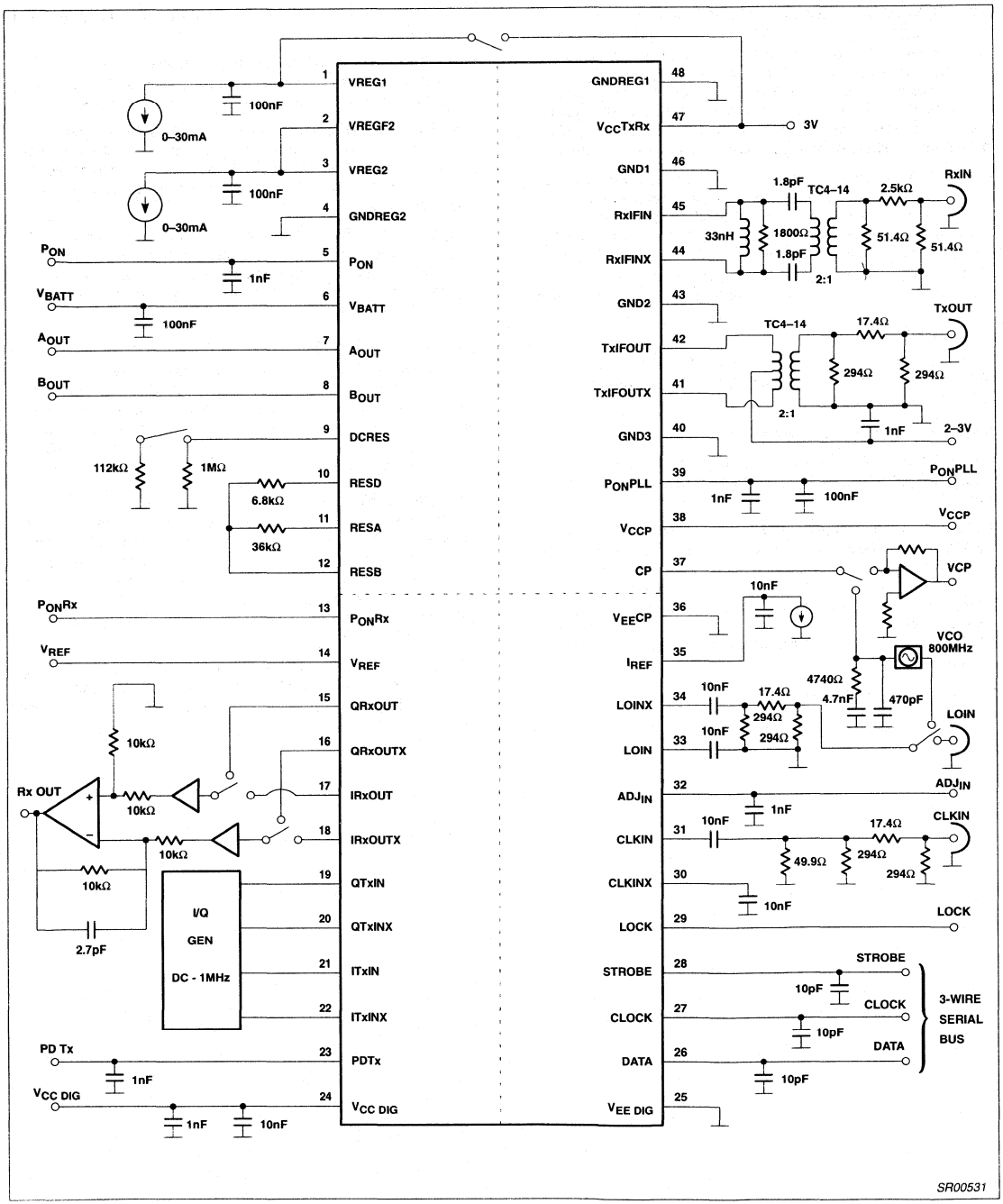


Figure 8. SA1638 Test Circuit

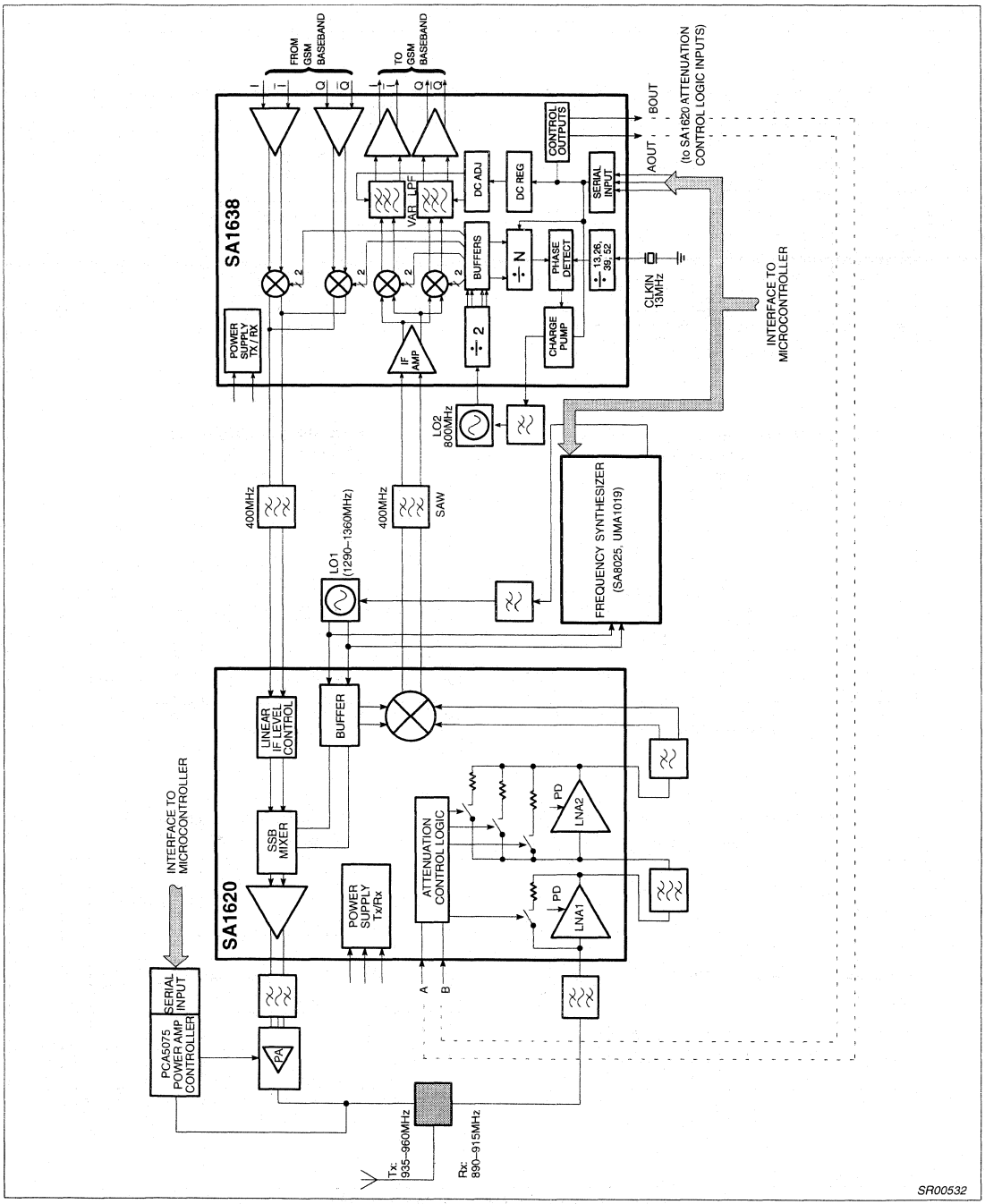
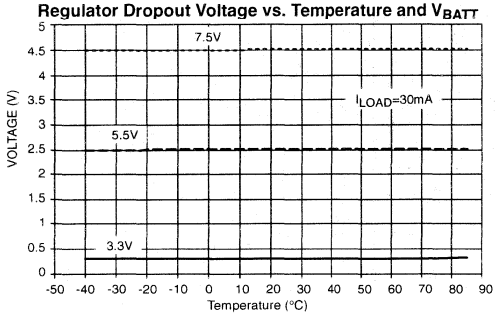


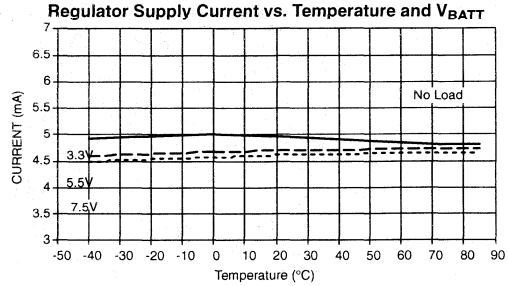
Figure 9. SA1620 / SA1638 System Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

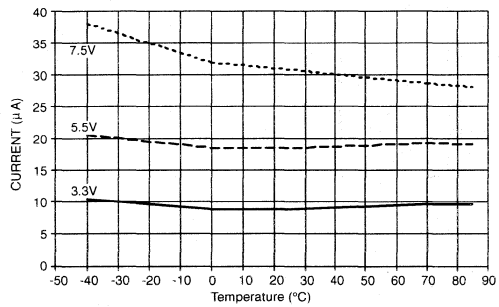
Regulator Dropout Voltage vs. Temperature and V_{BATT}



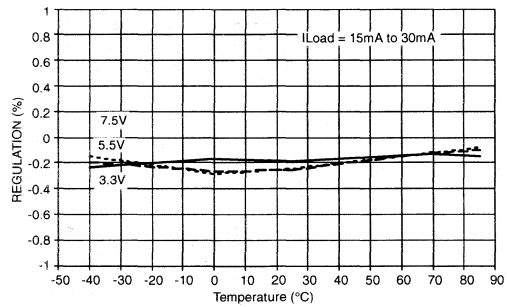
Regulator Supply Current vs. Temperature and V_{BATT}



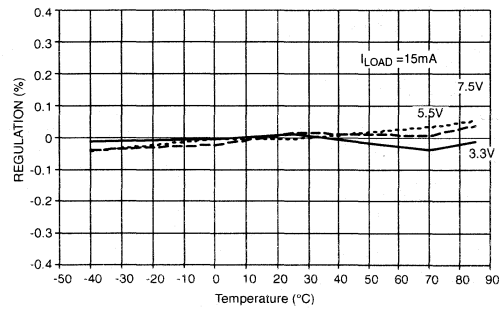
Regulator Powerdown Supply Current vs. Temperature and V_{BATT}



Regulator Load Regulation vs. Temperature and V_{BATT}



Regulator Line Regulation vs. Temperature and V_{BATT}



Regulator Output Voltage vs. Temperature and V_{BATT}

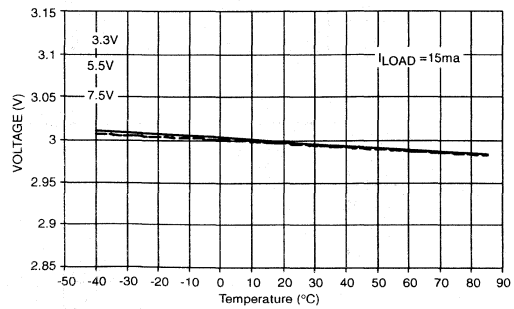
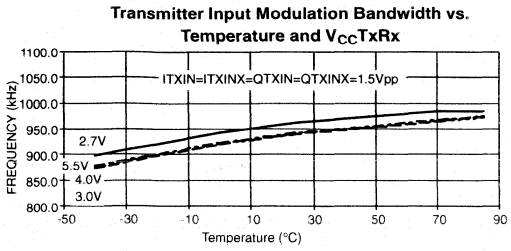
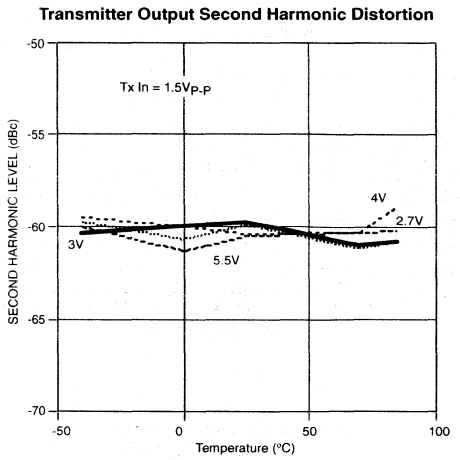
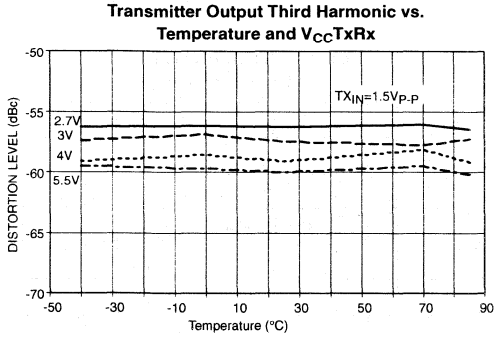


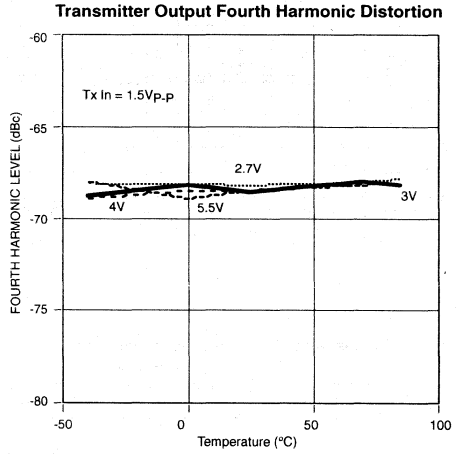
Figure 10. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)









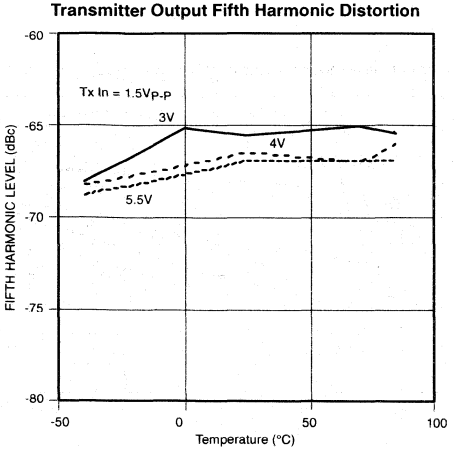
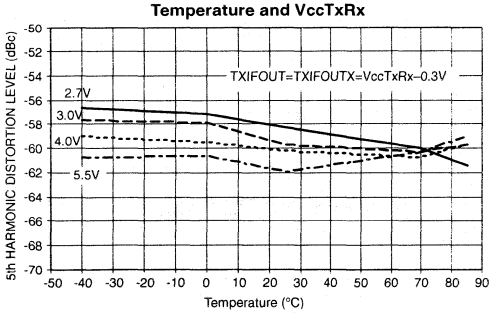


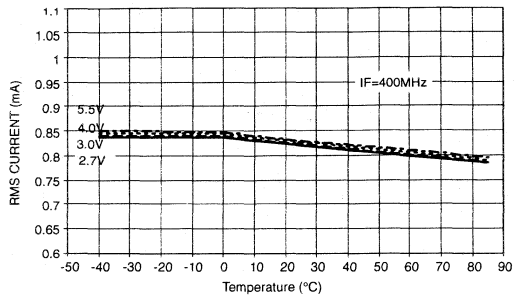
Figure 11. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

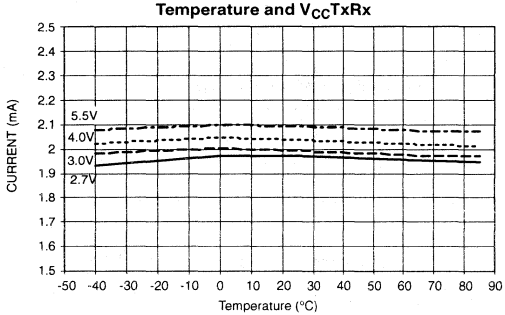
Transmitter Output Saturation vs. Temperature and VccTxRx



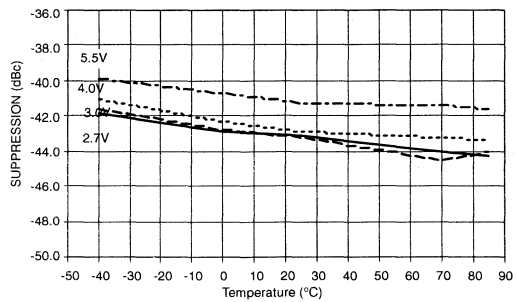
Transmitter RMS Output Current vs. Temperature and V_{CC}TxRx



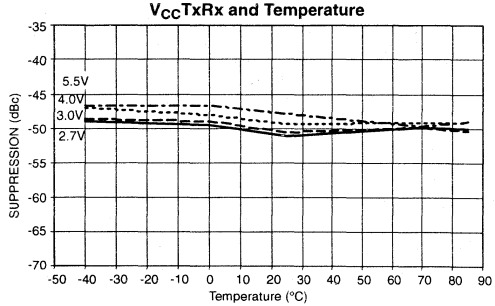
Transmitter DC Output Current vs. Temperature and V_{CC}TxRx



Transmitter LO Suppression vs. Temperature and VccTxRx



Transmitter Side Band Suppresion vs. V_{CC}TxRx and Temperature



Transmit Noise Floor vs Temperature and Supply Voltage

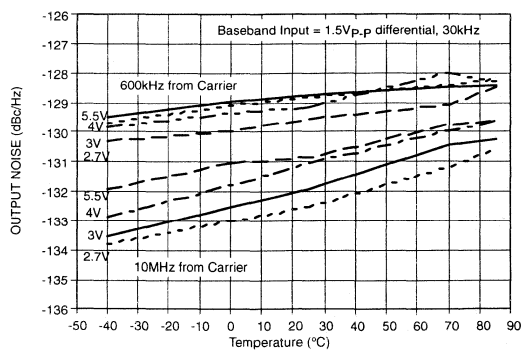
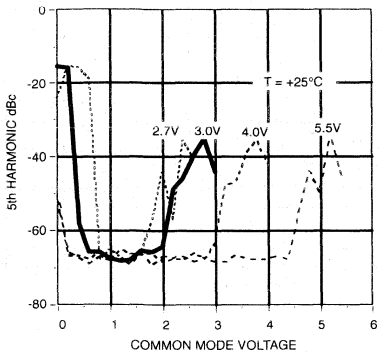


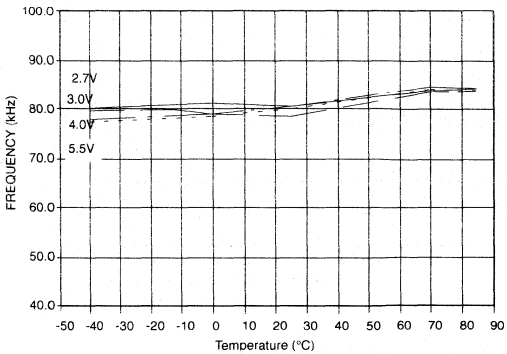
Figure 12. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

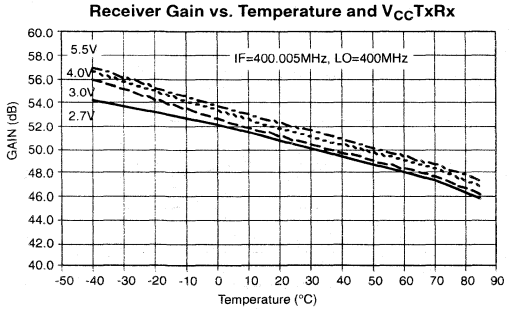
Transmitter Input Common Mode Range Vs. Supply Voltage



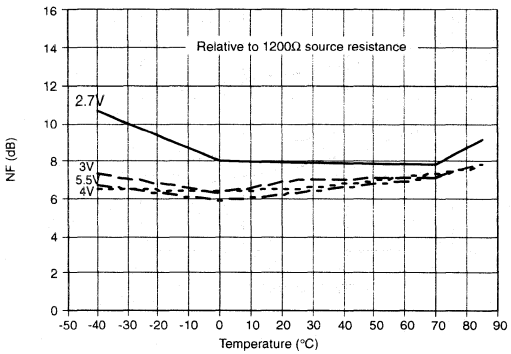
Receiver 3dB Bandwidth vs. Temperature and V_{CC}TxRx



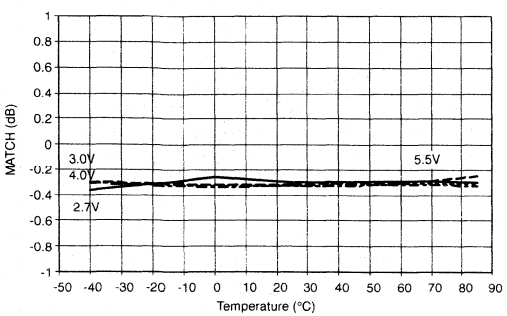
Receiver Gain vs. Temperature and V_{CC}TxRx



Receiver NF vs Temperature and Supply Voltage



Receiver Gain match vs V_{CC}TxRx and Temperature



Receiver Channel Matching Phase Error vs. Temperature and V_{CC}TxRx

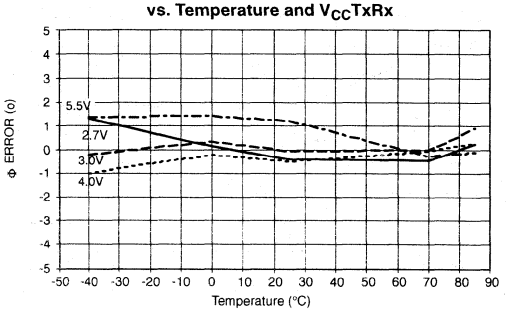


Figure 13. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

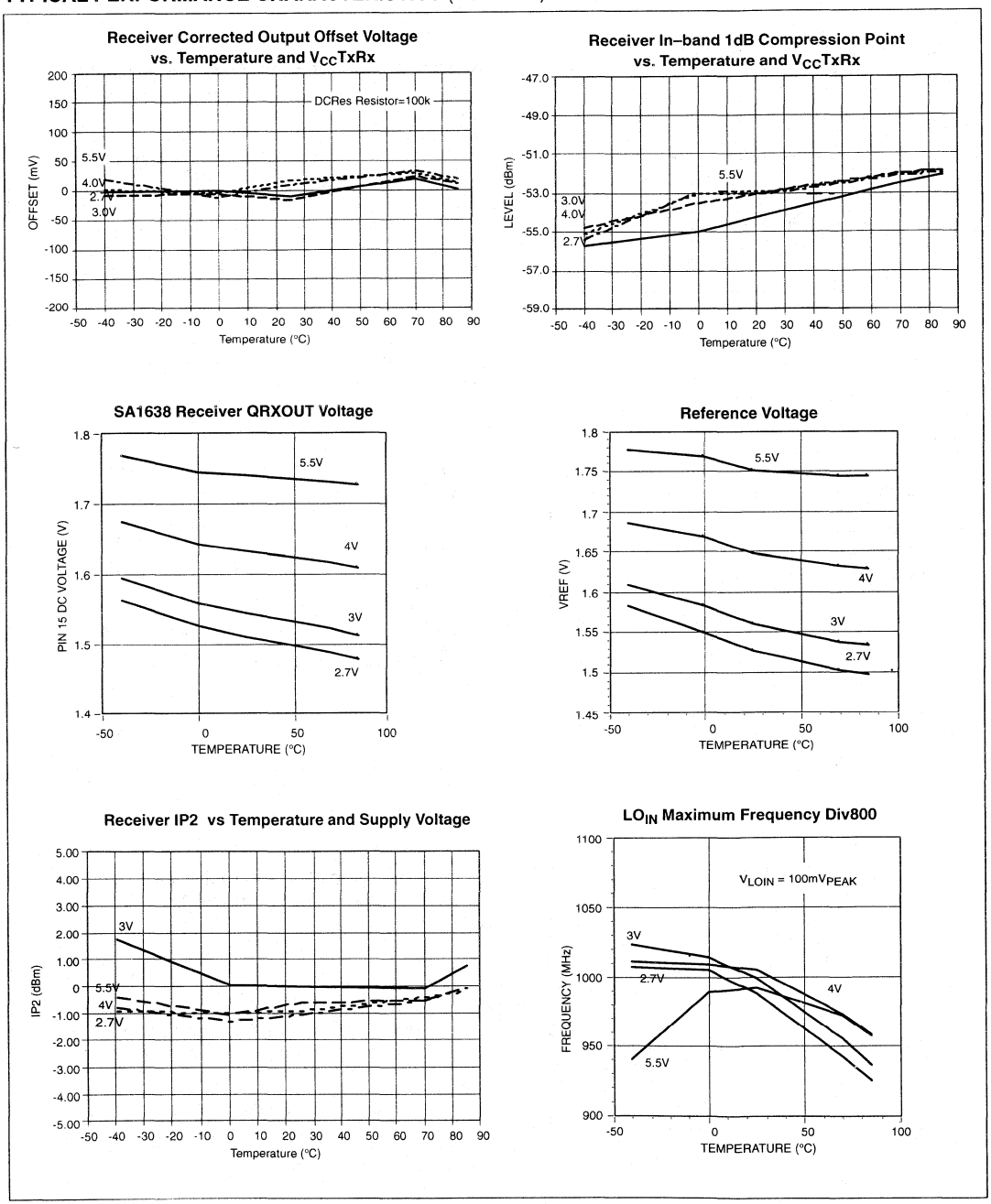


Figure 14. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

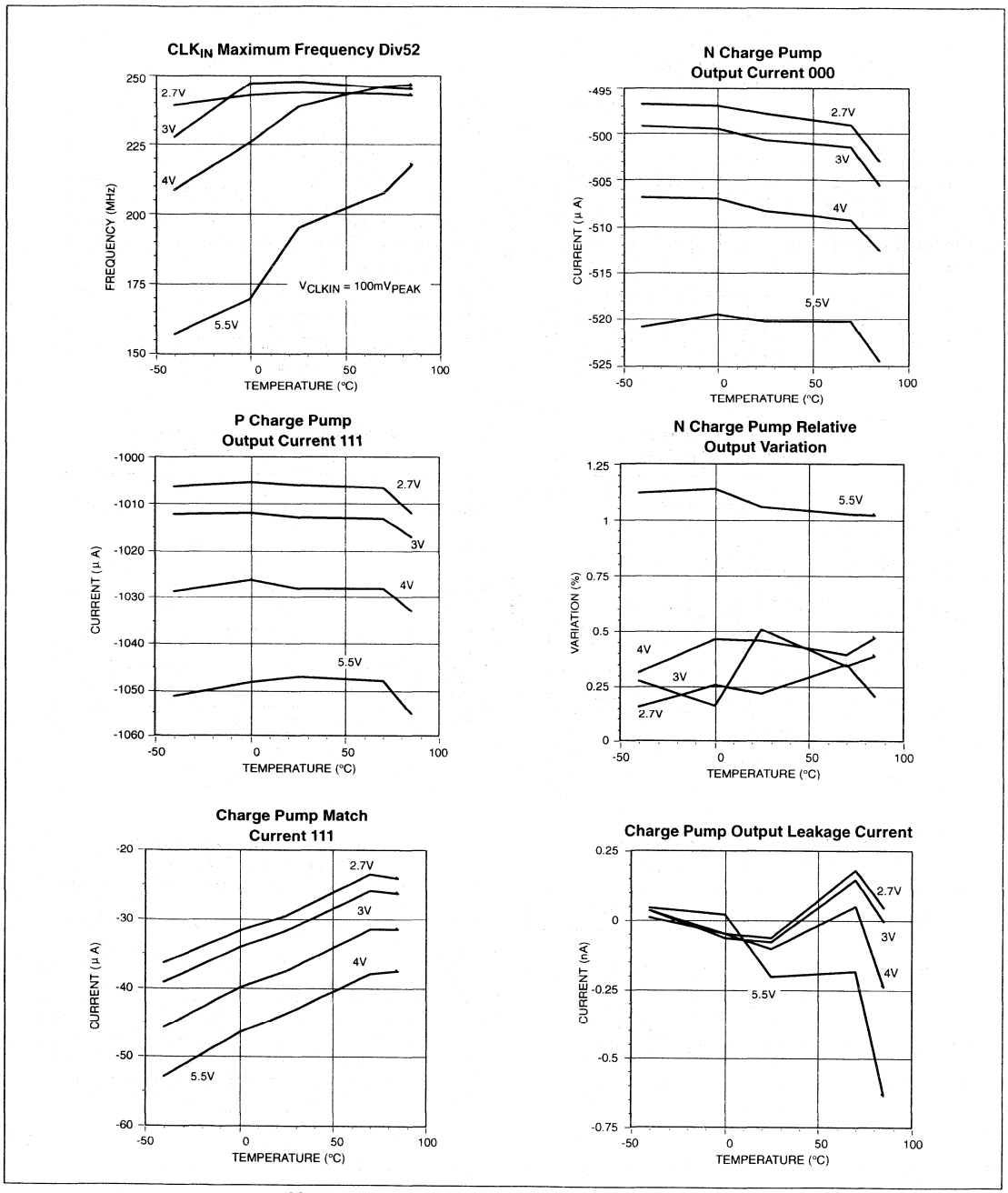


Figure 15. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

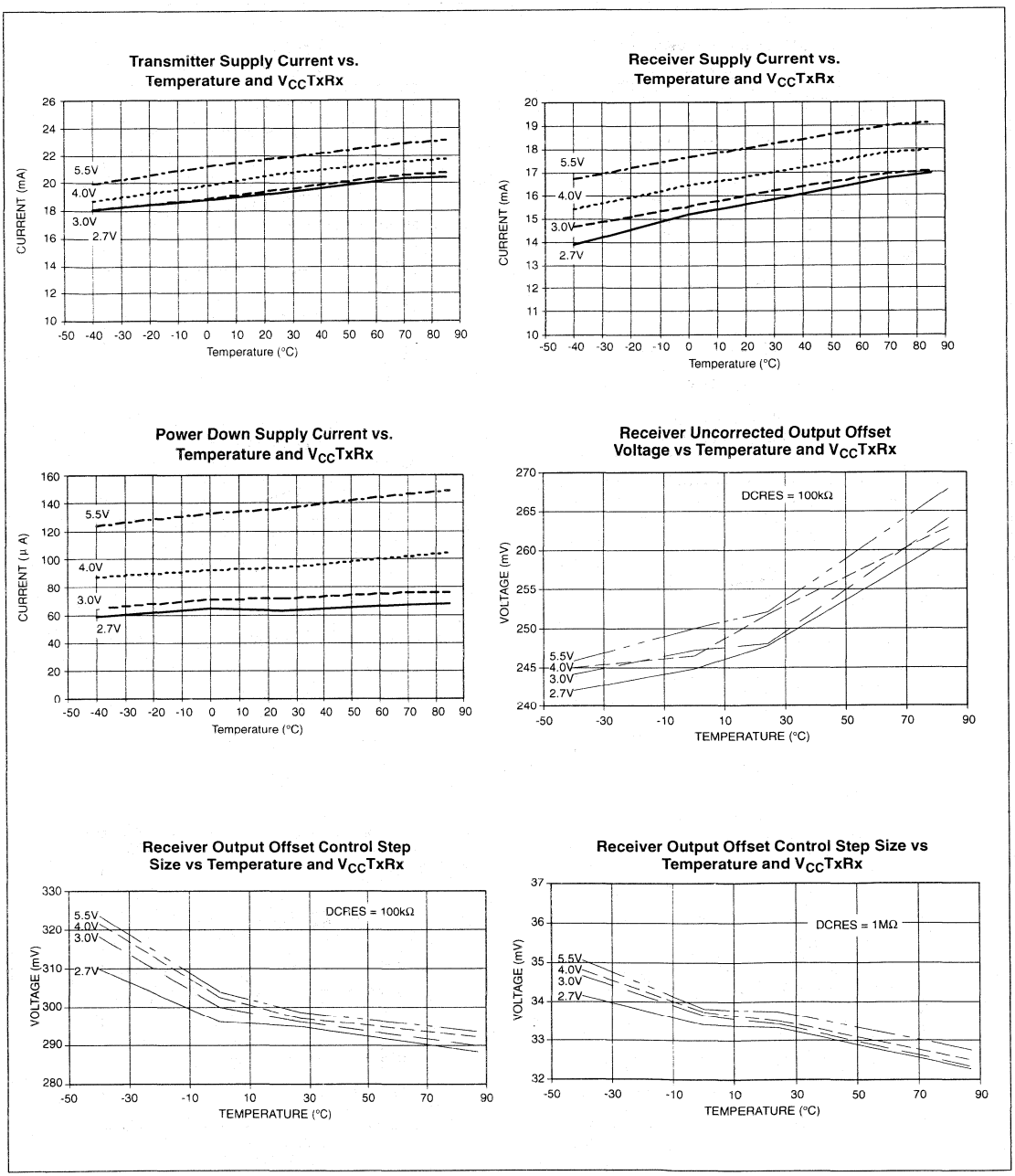


Figure 16. Typical Performance Characteristics (continued)

Section 7
Frequency Synthesizers and Prescalers

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UMA1022M	Low cost dual frequency synthesizer for radio telephones	7–283

The Philips Family of High Performance Frequency Synthesizers

	V_{CC}	I_{CC}	Pins	Pkg	Max RF/Input Frequency	Channel Spacing	Fractional–N Divider	Auxiliary Synthesizer	Applications
Fractional–N Frequency Syntesizer									
SA7025DK	2.7 to 5.5V	7.5mA@3V	20	SSOP20	1.0GHz (main) 150MHz (aux) 40MHz(aux)	10–5000kHz (main) 40–20,000kHz (aux) 10–5000kHz (aux)	✓	✓	IS–54/–136, IS–95, PDC, GSM digital cellular
SA8025ADK	2.7 to 5.5V	11 mA@3V	20	SSOP20	1.8GHz (main) 150MHz (aux) 40MHz(aux)	10–5000kHz (main) 40–20,000kHz (aux) 10–5000kHz (aux)	✓	✓	PHS digital cordless, U.S. PCS, PDC digital cellular
UMA1005T	2.9 to 5.5V	5mA@3V	20	SSOP20	30GHz (main) 90MHz (aux) 30MHz(aux)	10–20,000kHz (aux) 40–20,000kHz (aux) 10–5000kHz (aux)	✓	✓	IS–54/–136, IS–95, PDC, GSM digital cellular
Frequency Synthesizers									
UMA1014T	4.5 to 5.5V	13mA@5V	16	SO16	1.1GHz	5–100kHz			AMPS/TACS cellular, cordless
UMA1015M	2.7 to 5.5V	9.6mA@3V	20	SSOP20	1.1GHz 1.1GHz	8.5–375kHz		✓ (dual)	CT1/CT1+ cordless AMPS/TACS, NMT cellular
UMA1017M	2.7 to 5.5V	6.5mA@3V	20	SSOP20	1200MHz	10–200kHz			GSM digital cellular, spread spectrum
UMA1018M	2.7 to 5.5V	8.5mA@3V	20	SSOP20	1200MHz (main) 300MHz (aux)	10–2000kHz (main) 10–1000kHz (aux)		✓	GSM digital cellular
UMA1019M	2.7 to 5.5V	9.5mA@3V	20	SSOP20	2200MHz	10–2000kHz			DECT digital cordless DCS 1800
UMA1020M	2.7 to 5.5V	12mA@3V	20	SSOP20	2200MHz (main) 300MHz (aux)	10–2000kHz (main) 10–2000kHz (aux)		✓	DECT digital cordless, dcs1800, phs
UMA1021M	2.7 to 5.5V	9mA@3V	20	SSOP20	2200MHz	10–2000kHz			WLAN DECT digital cordless DCS 1800, PHS
UMA1022M	2.7 to 5.5V	13mA@3V	20	SSOP20	2200MHz (main) 500MHz (aux)	10–2000kHz		✓	WLAN DECT digital cordless DCS 1800, PHS

	V_{CC}	I_{CC}	Pins	Pkg	Max Input Frequency	Max Compare Frequency	Input Sensitivity	Divide Ratio
Prescalers								
SA701N,D	2.7 TO 6V	4.5mA@3V	8	DIP, S08	1.1GHz	65kHz/270kHz	–35 dBm	128/129,64/65
SA702N,D	2.7 TO 6V	4.5mA@3V	8	DIP, S08	1.1GHz	1000kHz	–35 dBm	64/66/72
SA703N,D	2.7 TO 6V	4.5mA@3V	8	DIP, S08	1.1GHz	335kHz	–35 dBm	128/129/144

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

SA701

DESCRIPTION

The SA701 is an advanced dual modulus (Divide By 128/129 or 64/65) low power ECL prescaler. The minimum supply voltage is 2.7V and is compatible with the CMOS UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package, and is pin compatible with Fujitsu MB501, Plessey SP8704 and Motorola MC12022.

PIN CONFIGURATION

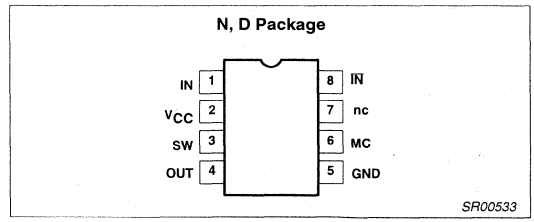


Figure 1. Pin Configuration

FEATURES

- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA701N	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA701D	SOT96-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

BLOCK DIAGRAM

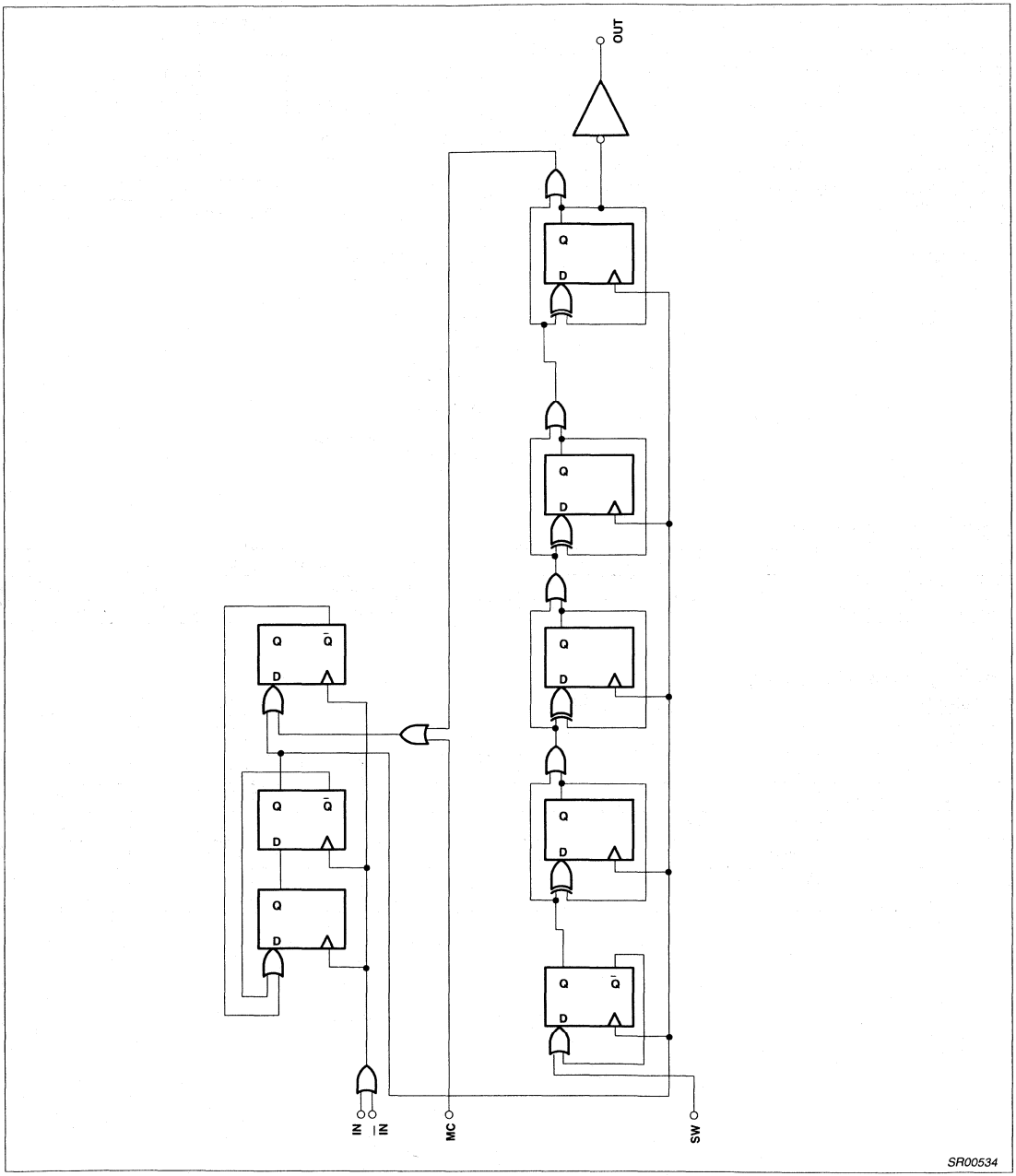


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25°C$ and $V_{CC} = 3.0V$; unless otherwise stated. Test circuit Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC input high threshold		2.0		V_{CC}	V
V_{IL}	MC input low threshold		–0.3		0.8	V
V_{IH}	SW input high threshold		2.0		V_{CC}	V
V_{IL}	SW input low threshold		–0.3		0.8	V
I_{IH}	MC input high current	$V_{MC} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC input low current	$V_{MC} = 0V$, $V_{CC} = 6V$	–100	–30		µA
I_{IH}	SW input high current	$V_{SW} = V_{CC} = 6V$		35	100	µA
I_{IL}	SW input low current	$V_{SW} = 0V$, $V_{CC} = 6V$	–50	–0.1		µA

AC ELECTRICAL CHARACTERISTICS

The following AC specifications are valid for $V_{CC} = 3.0V$, f_{IN} = 1GHz, input level = 0dBm, $T_A = 25°C$; unless otherwise stated. Test circuit Fig. 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	V_{CC} = 5.0V		1.6		V_{P-P}
		V_{CC} = 3.0V		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA701 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for SW (Modulus Set Switch) input to be set low and MC (Modulus Control) input to be set high in which case the circuit comprises a divide by 128. For divide by 129 the MC signal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. Similarly, for divide by 64 and 65 the SA701 will generate those respective moduli with the SW signal forced high, in which the fourth stage of the synchronous divider is bypassed. A truth table for the modulus values is given below:

For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 for modulus 128/129 or count 32 for modulus 64/65 with delay t_{PD}. The SW input is not designed for synchronous switching.

The MC and SW inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed. The SW input has an internal pull-down simplifying modulus group selection. With SW open the divide by 128/129 mode is selected and with SW connected to V_{CC} divide by 64/65 is selected.

The prescaler input is differential and ECL compatible. The output is single-ended ECL compatible.

Table 1.

Modulus	MC	SW
128	1	0
129	0	0
64	1	1
65	0	1

AC TIMING CHARACTERISTICS

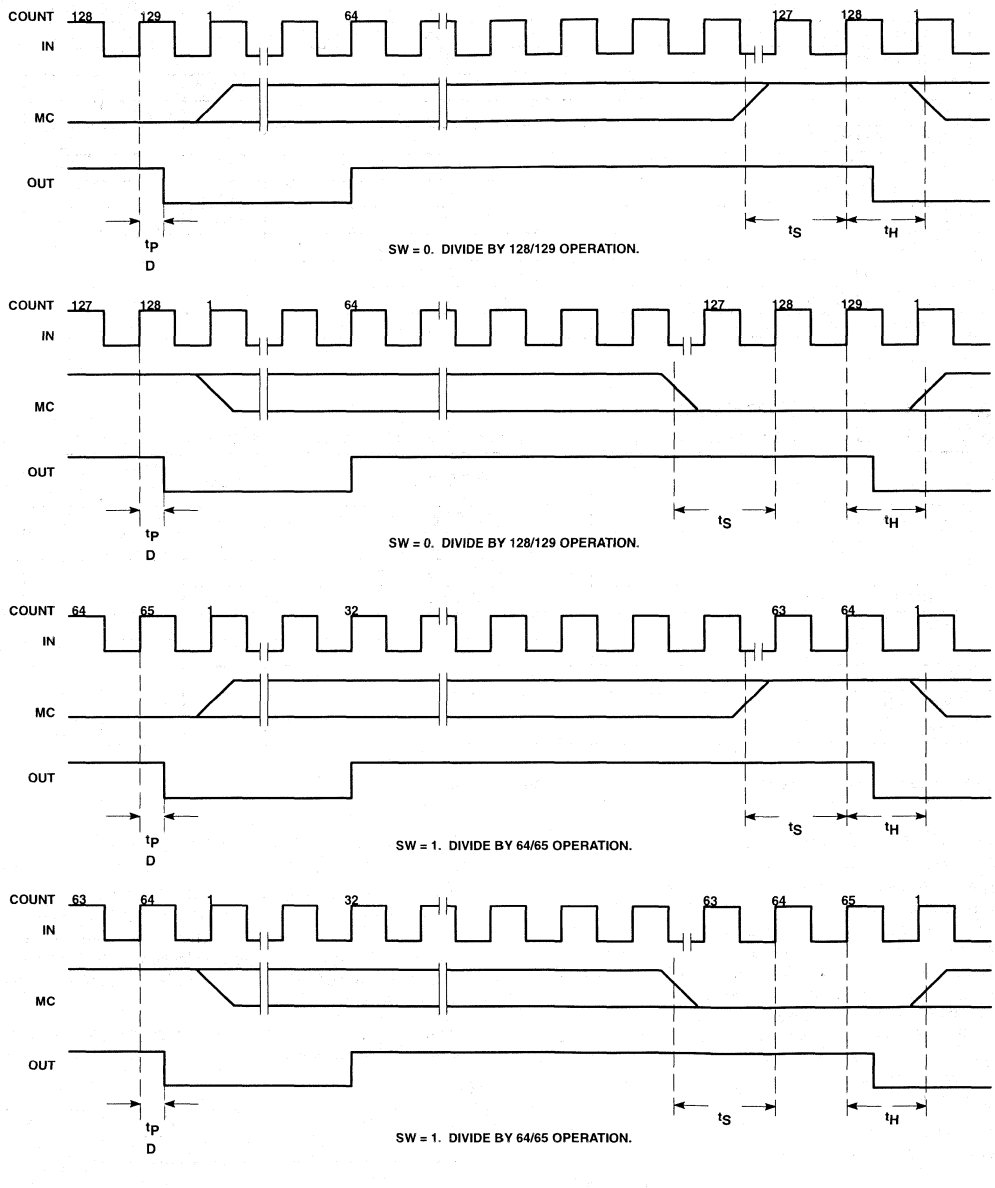


Figure 3. AC Timing Characteristics

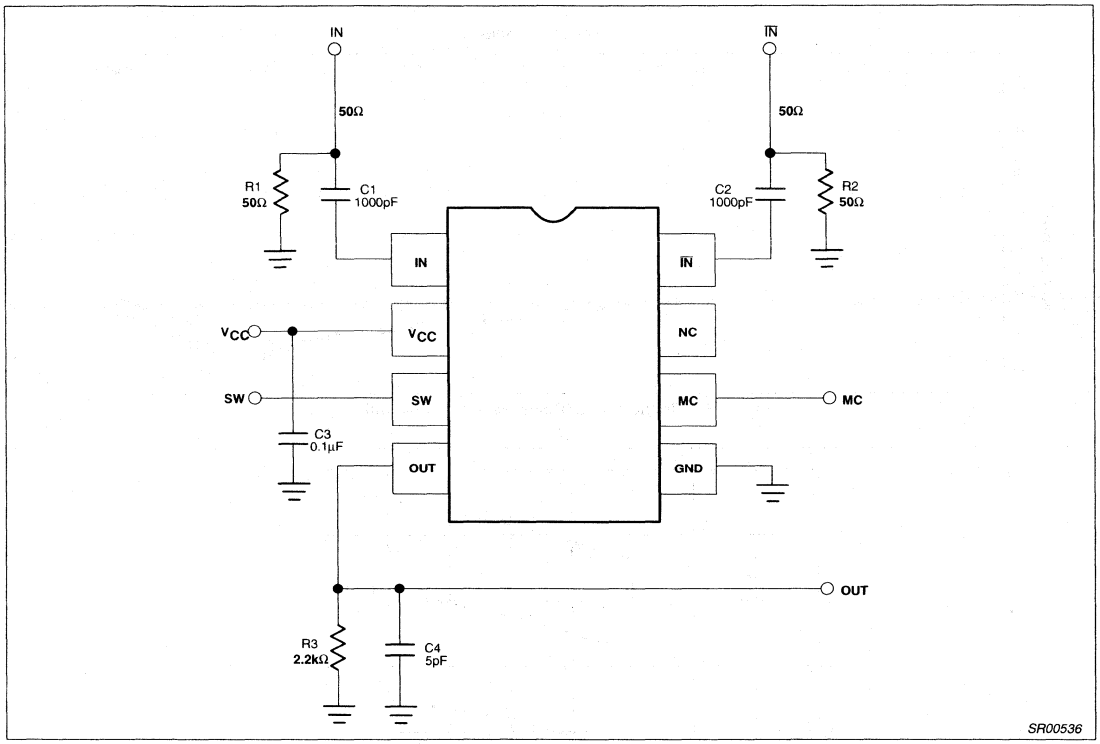


Figure 4. SA701 Test Circuit

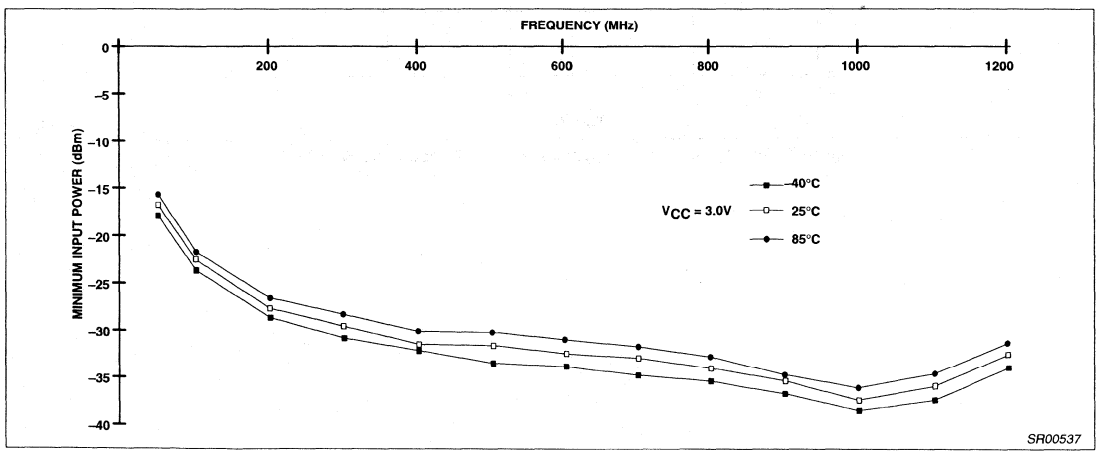


Figure 5. Minimum Input Power vs Frequency and Temperature

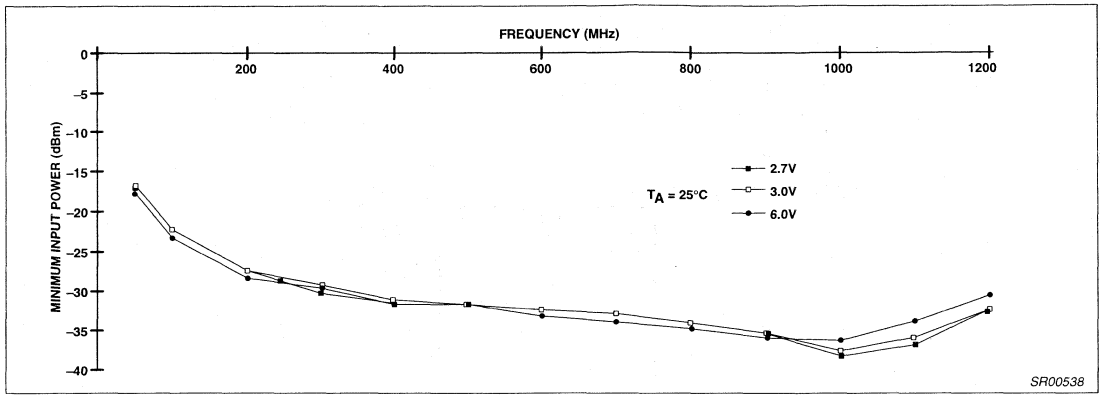


Figure 6. Minimum Input Power vs Frequency and V_{CC}

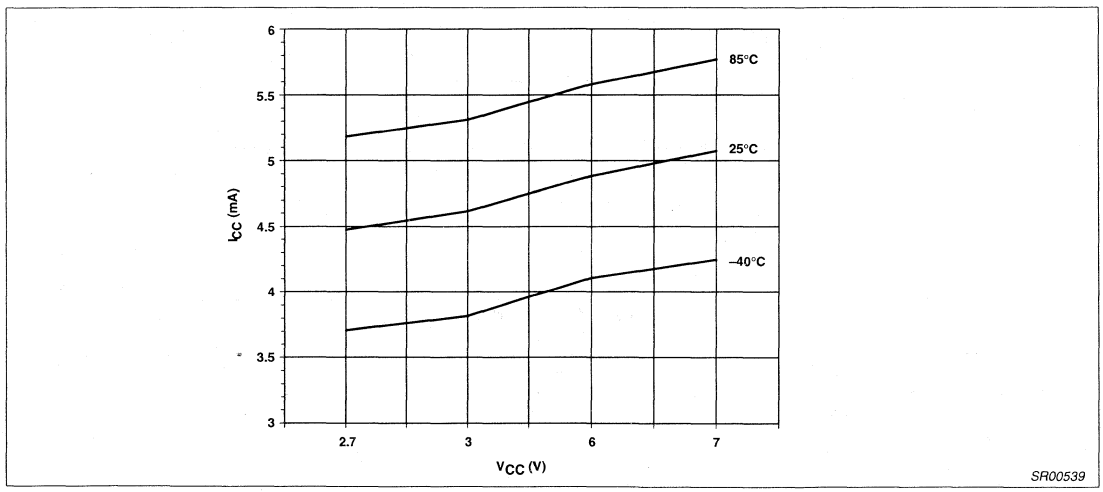


Figure 7. Supply Current vs Supply Voltage and Temperature With No Load

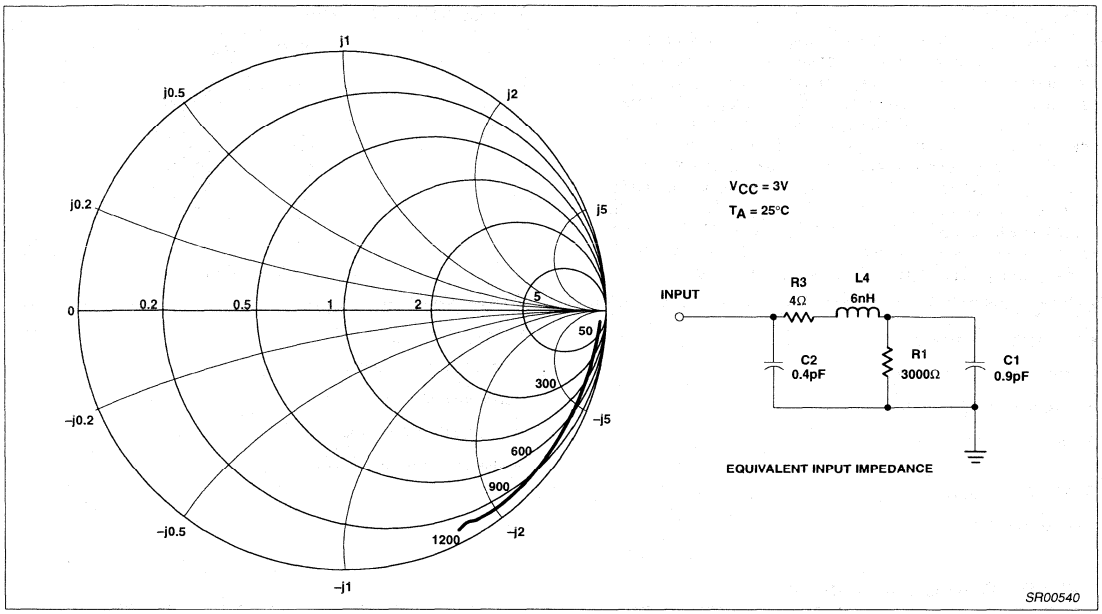


Figure 8. Typical N Package Input Impedance

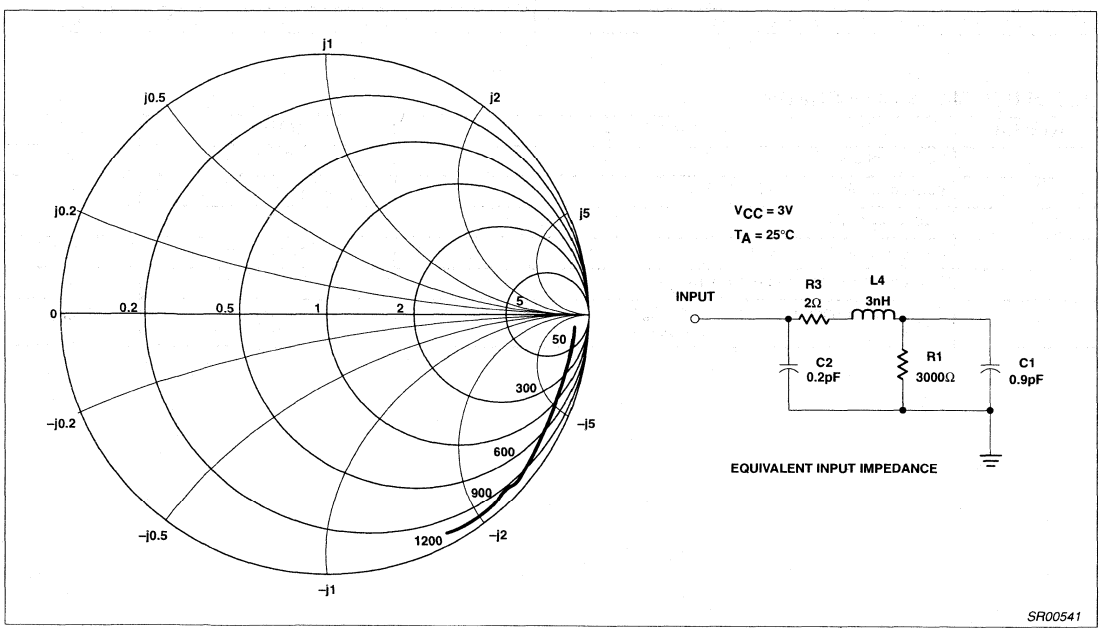


Figure 9. Typical D Package Input Impedance

Divide by: 64/65/72 triple modulus low power ECL prescaler

SA702

DESCRIPTION

The SA702 triple modulus (Divide By 64/65/72) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.7V and is compatible with the CMOS UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package.

FEATURES

- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

APPLICATIONS

- Cellular phones

PIN CONFIGURATION

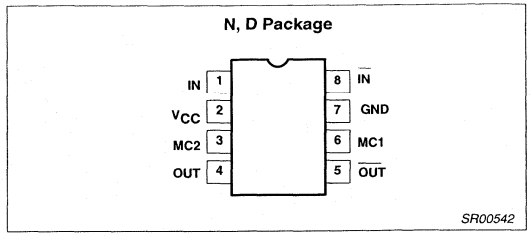


Figure 1. Pin Configuration

- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA702N	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA702D	SOT96-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

BLOCK DIAGRAM

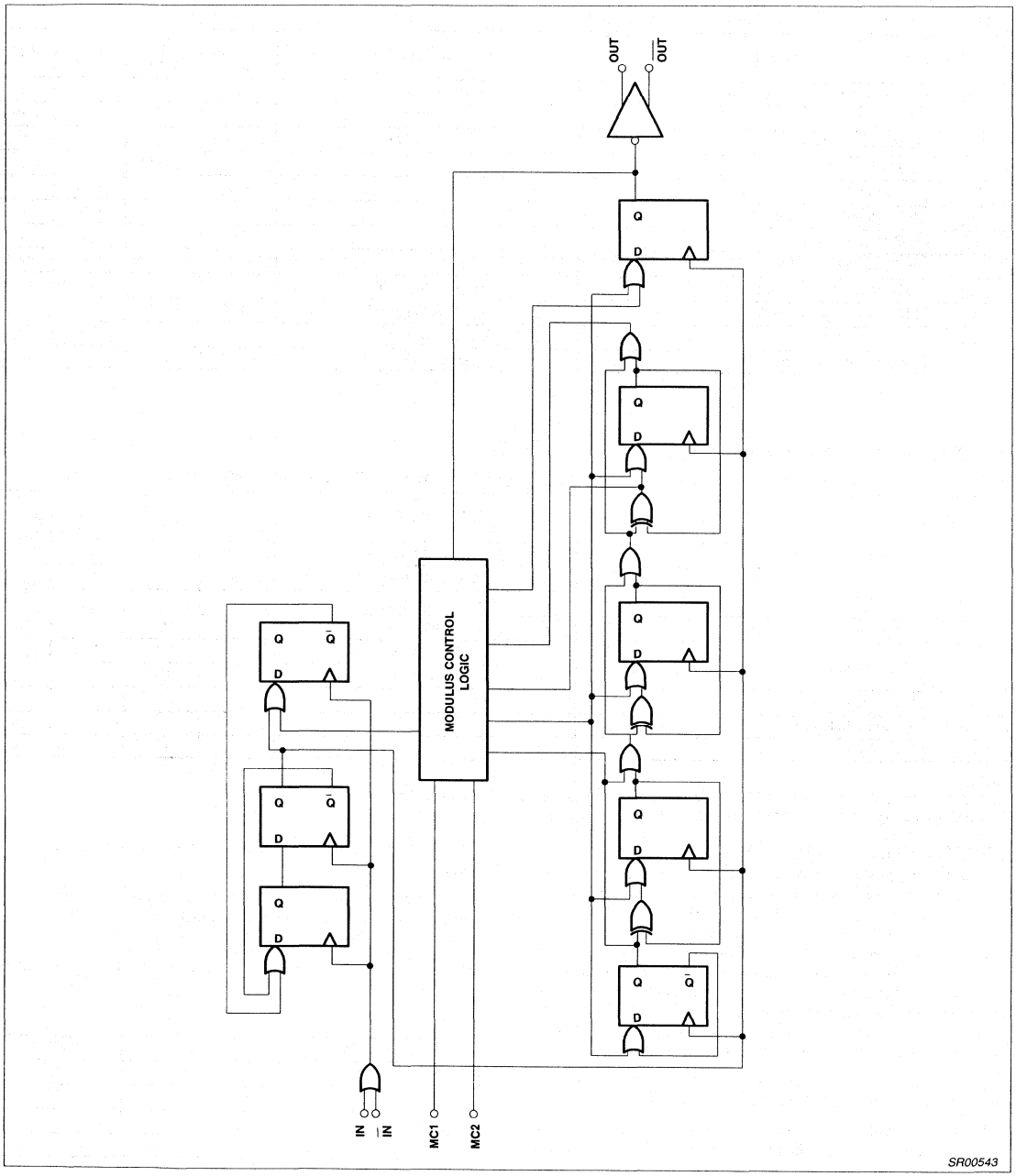


Figure 2. Block Diagram

Divide by: 64/65/72 triple modulus low power ECL prescaler

SA702

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25°C$ and $V_{CC} = 3.0V$; unless otherwise stated. Test circuit Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC1 input high threshold		2.0		V_{CC}	V
V_{IL}	MC1 input low threshold		–0.3		0.8	V
V_{IH}	MC2 input high threshold		2.0		V_{CC}	V
V_{IL}	MC2 input low threshold		–0.3		0.8	V
I_{IH}	MC1 input high current	$V_{MC1} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC1 input low current	$V_{MC1} = 0V$, $V_{CC} = 6V$	–100	–30		µA
I_{IH}	MC2 input high current	$V_{MC2} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC2 input low current	$V_{MC2} = 0V$, $V_{CC} = 6V$	–100	–30		µA

AC ELECTRICAL CHARACTERISTICS

These AC specifications are valid for f_{IN} = 1GHz, input level = 0dBm, $V_{CC} = 3.0V$ and $T_A = 25°C$; unless otherwise stated. Test circuit Fig. 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	V_{CC} = 5.0V		1.6		V_{P-P}
		V_{CC} = 3.0V		1.2		
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA702 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 64. For divide by 65 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. For divide by 72, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 18. A truth table for the modulus values is given below:

For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 32 with delay t_{PD}.

The MC1 and MC2 inputs are TTL compatible threshoid inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

Table 1.

Modulus	MC1	MC2
64	1	0
65	0	0
72	0	1
72	1	1

AC TIMING CHARACTERISTICS

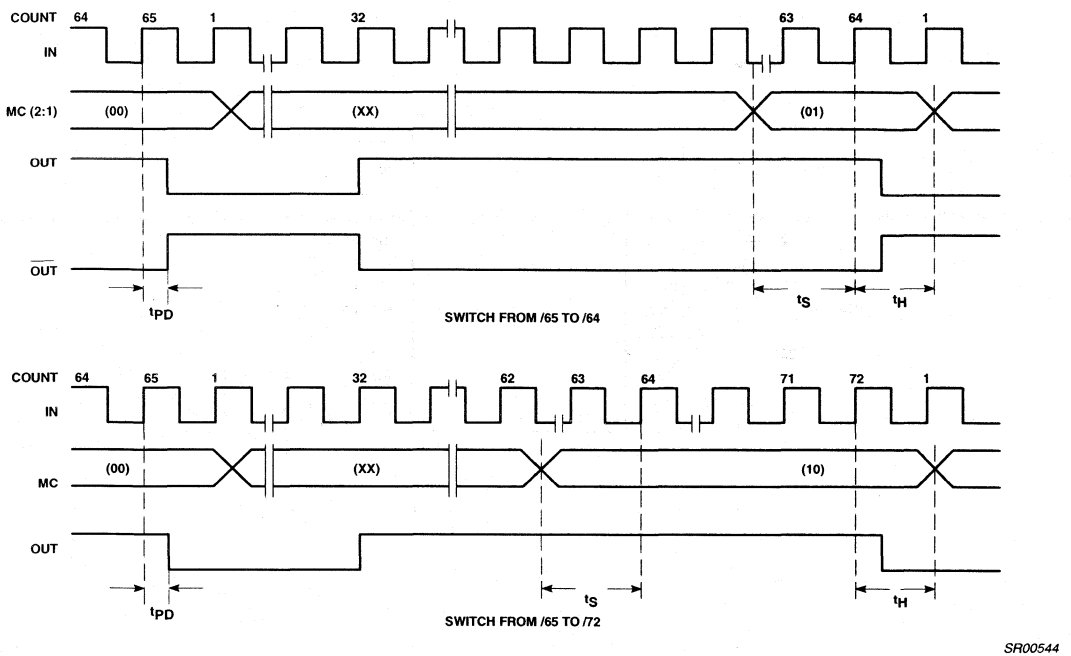


Figure 3. AC Timing Characteristics

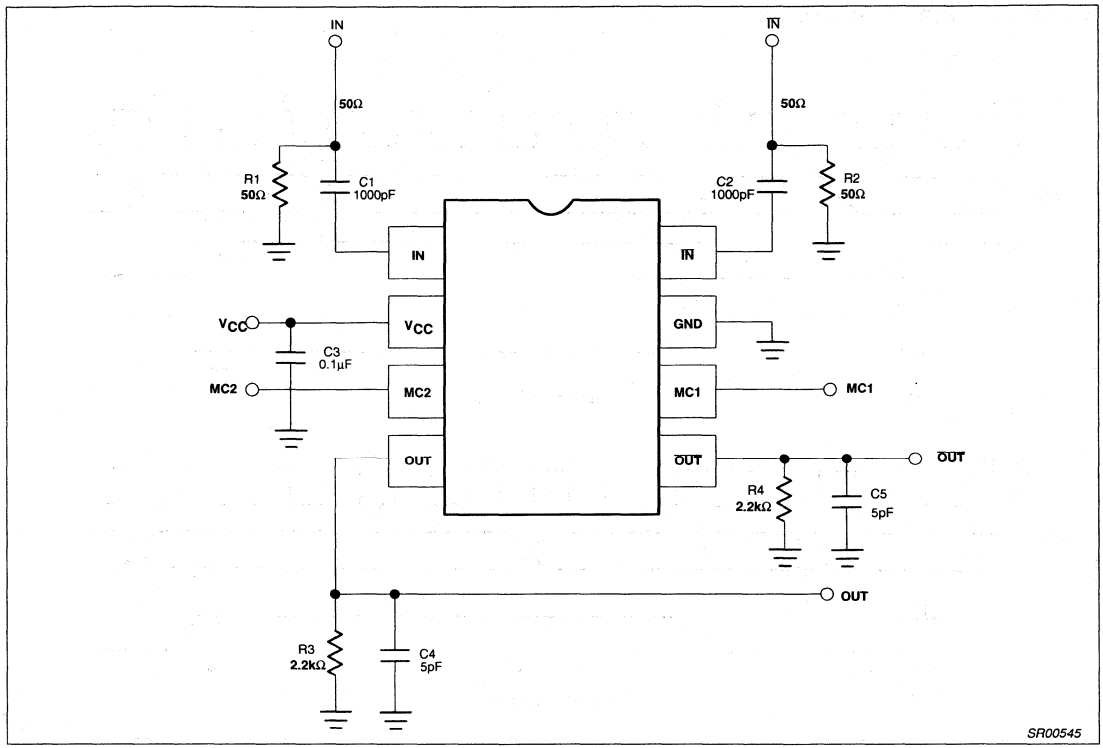


Figure 4. SA702 Test Circuit

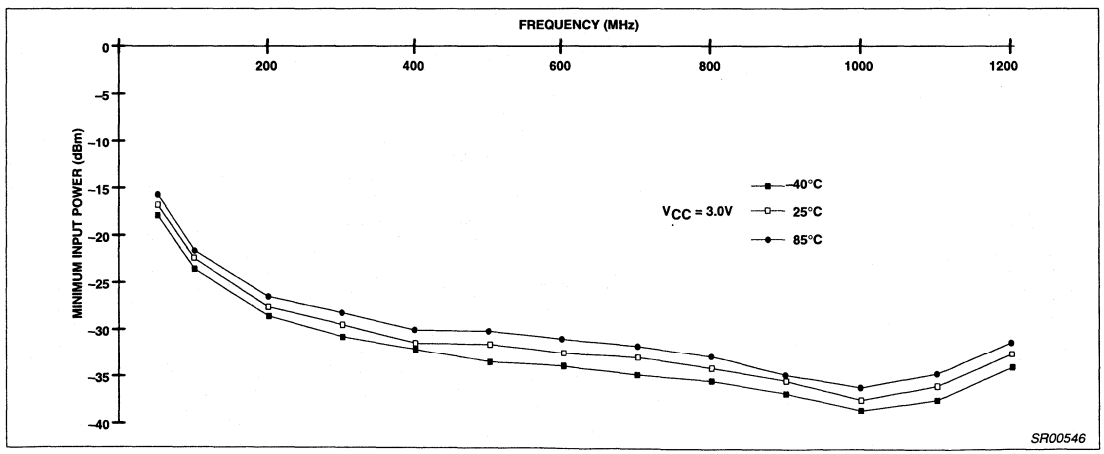


Figure 5. Minimum Input Power vs Frequency and Temperature

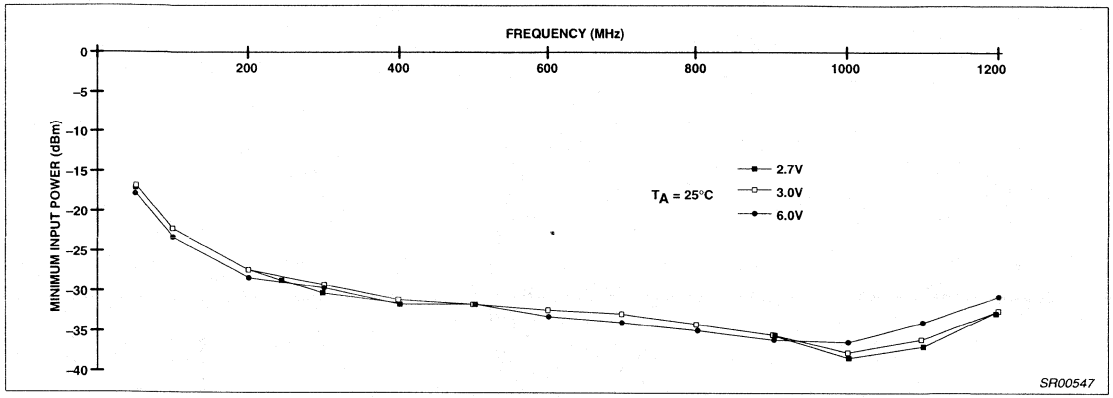


Figure 6. Minimum Input Power vs Frequency and V_{CC}

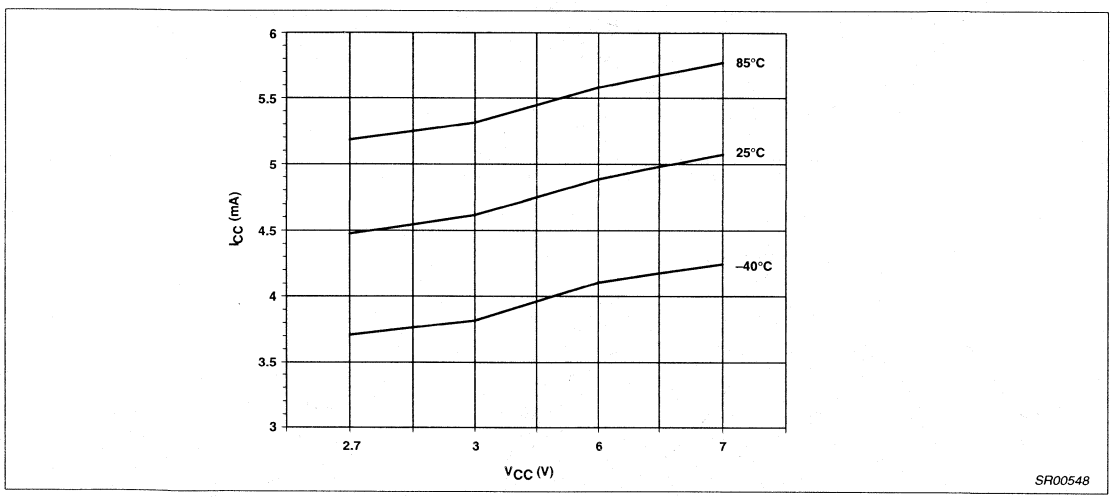


Figure 7. Supply Current vs Supply Voltage and Temperature With No Load

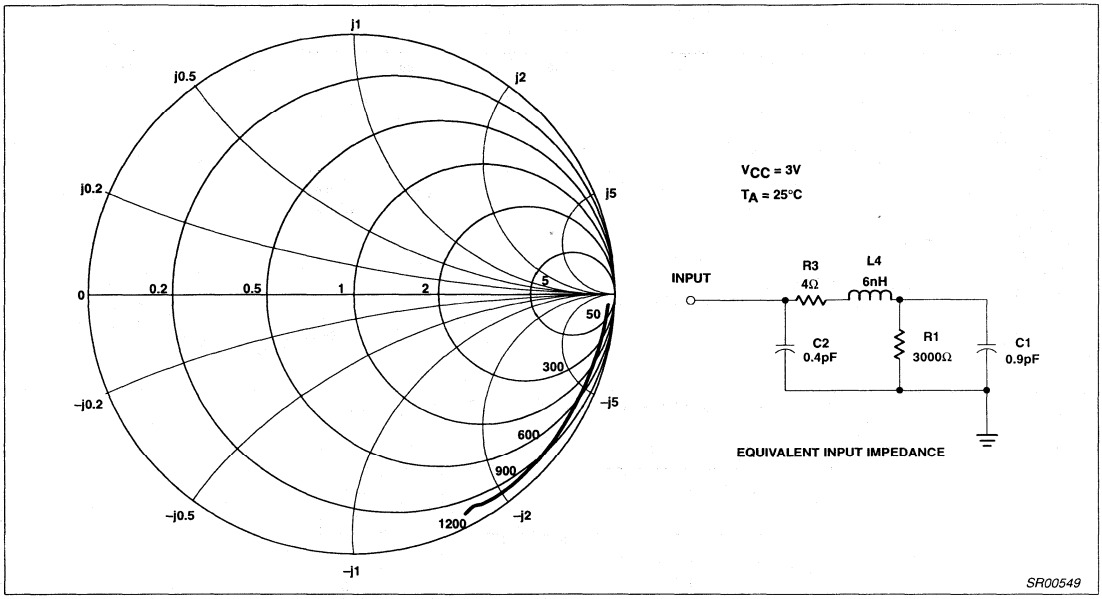


Figure 8. Typical N Package Input Impedance

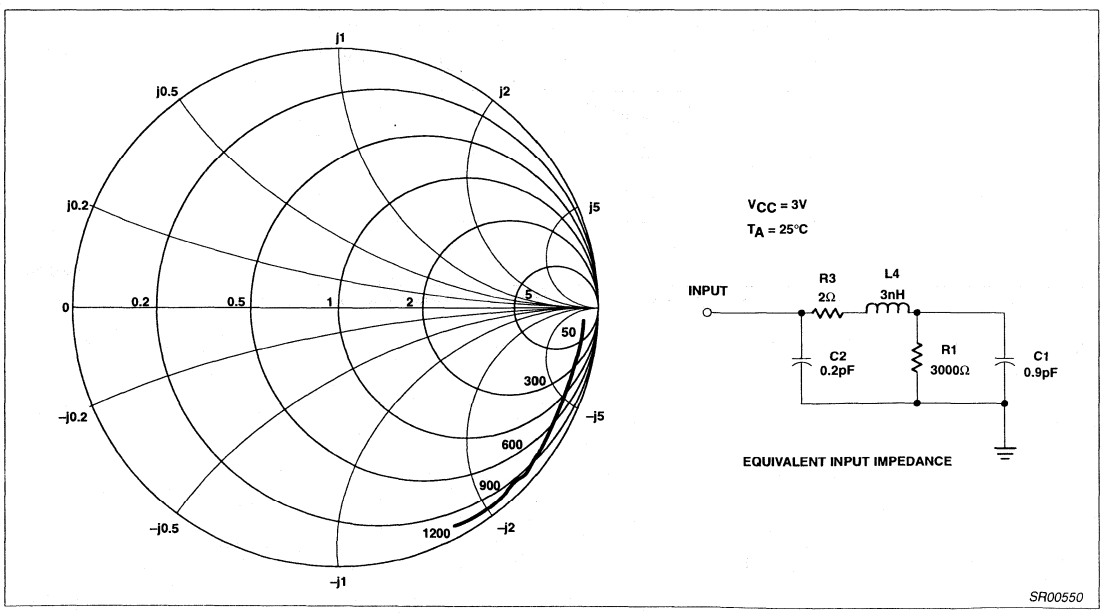


Figure 9. Typical D Package Input Impedance

Divide by: 128/129/144 triple modulus low power ECL prescaler

SA703

DESCRIPTION

The SA703 triple modulus (Divide By 128/129/144) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.7V and is compatible with the UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package.

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

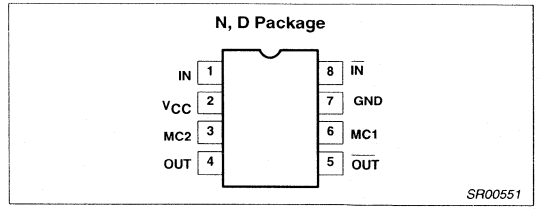


Figure 1. Pin Configuration

FEATURES

- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA703N	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA703D	SOT96-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

BLOCK DIAGRAM

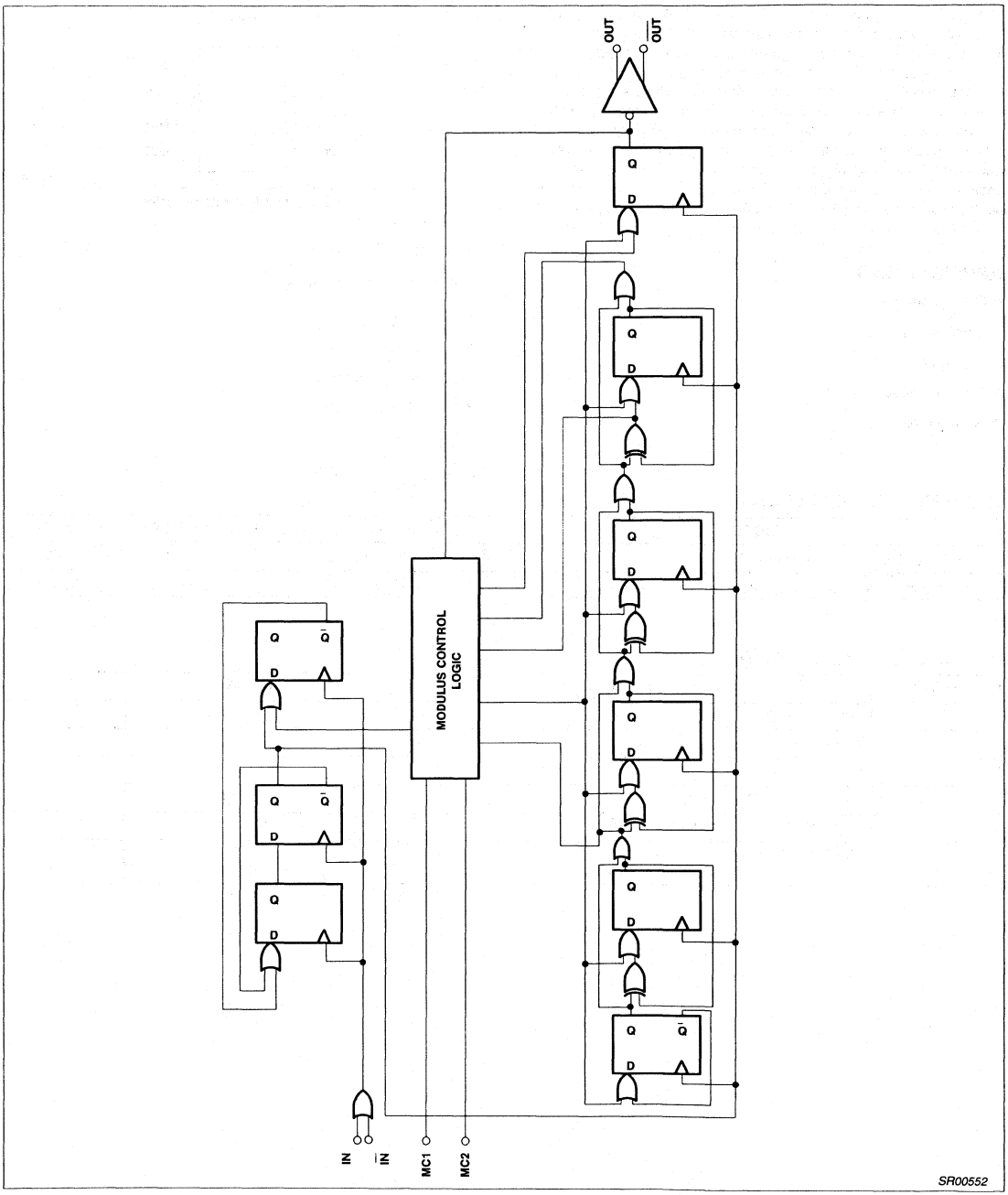


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25^\circ C$ and $V_{CC} = 3.0V$; unless otherwise stated. Test circuit Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC1 input high threshold		2.0		V_{CC}	V
V_{IL}	MC1 input low threshold		–0.3		0.8	V
V_{IH}	MC2 input high threshold		2.0		V_{CC}	V
V_{IL}	MC2 input low threshold		–0.3		0.8	V
I_{IH}	MC1 input high current	$V_{MC1} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC1 input low current	$V_{MC1} = 0V$, $V_{CC} = 6V$	–100	–30		µA
I_{IH}	MC2 input high current	$V_{MC2} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC2 input low current	$V_{MC2} = 0V$, $V_{CC} = 6V$	–100	–30		µA

AC ELECTRICAL CHARACTERISTICS

These AC specifications are valid for $V_{CC} = 3.0V$, f_{IN} = 1GHz, input level = 0dBm, $T_A = 25^\circ C$; unless otherwise stated. Test circuit Fig. 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	V_{CC} = 5.0V		1.6		V_{P-P}
		V_{CC} = 3.0V		1.2		
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA703 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 128. For divide by 129 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. For divide by 144, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 36. A truth table for the modulus values is given in Table 1.

For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 with delay t_{PD}.

The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

Table 1.

Modulus	MC1	MC2
128	1	0
129	0	0
144	0	1
144	1	1

AC TIMING CHARACTERISTICS

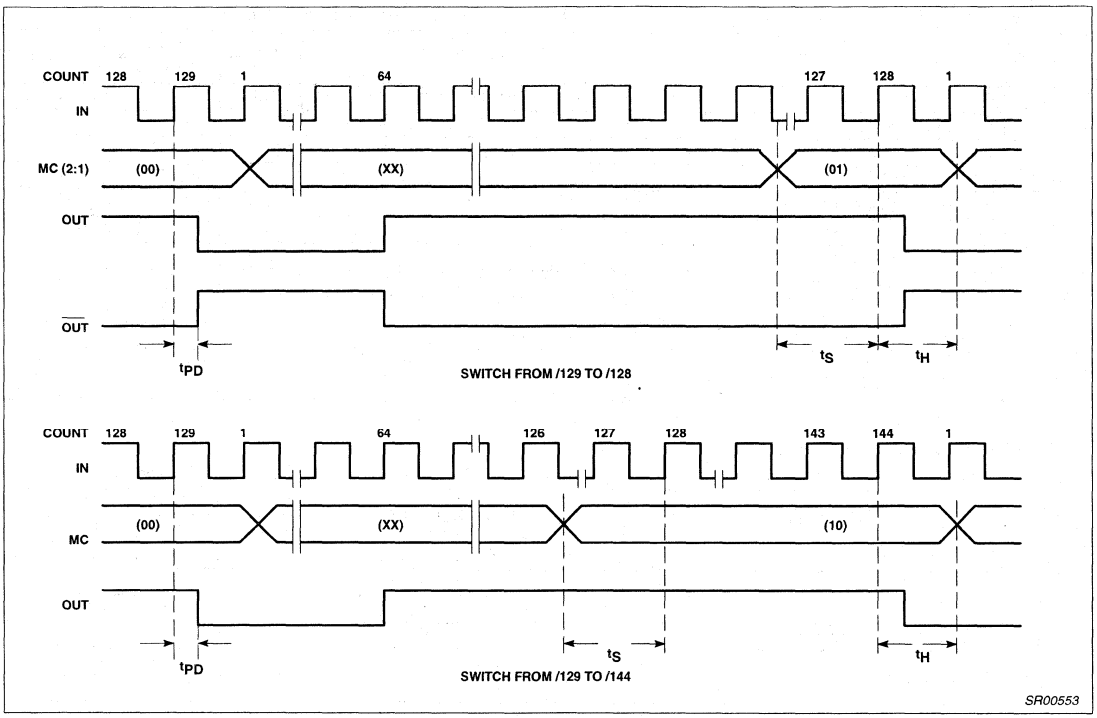


Figure 3. AC Timing Characteristics

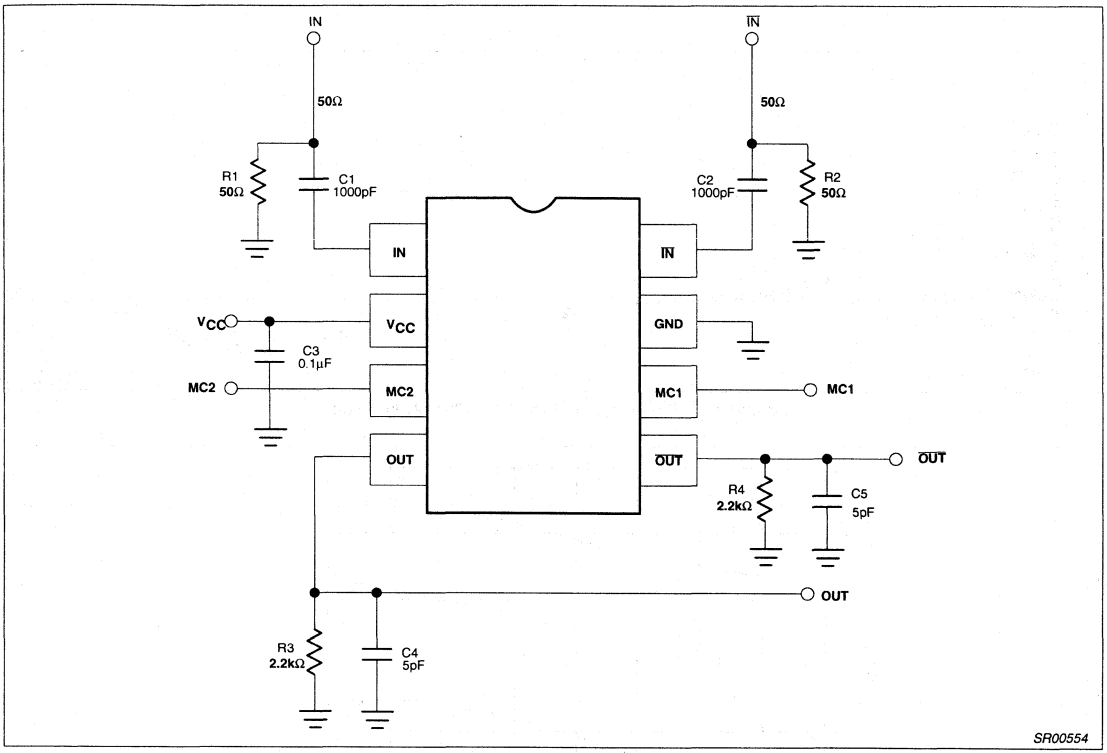


Figure 4. SA703 Test Circuit

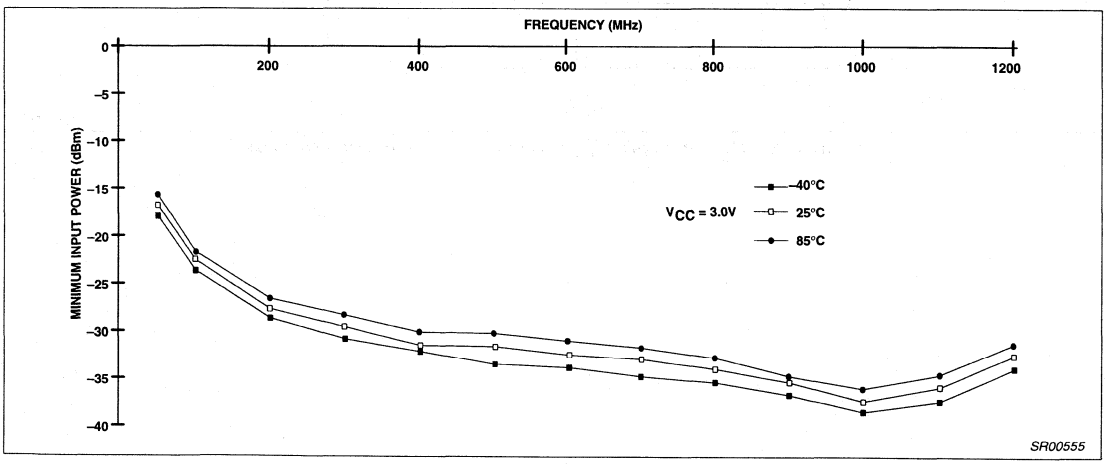


Figure 5. Minimum Input Power vs Frequency and Temperature

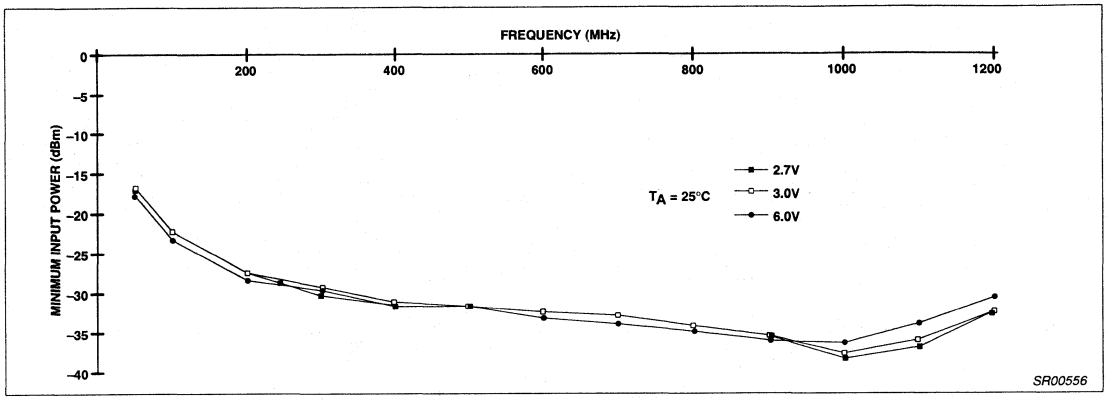


Figure 6. Minimum Input Power vs Frequency and V_{CC}

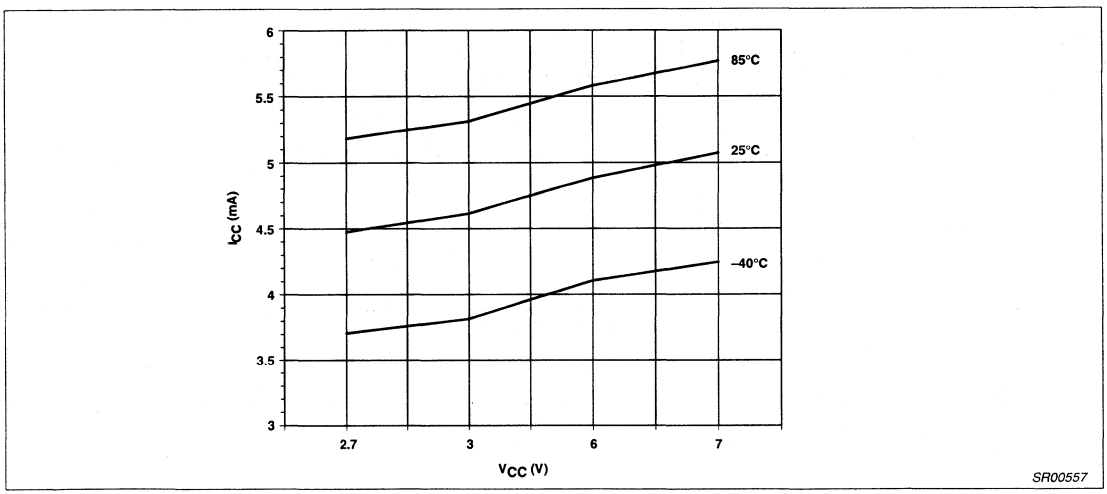


Figure 7. Supply Current vs Supply Voltage and Temperature With No Load

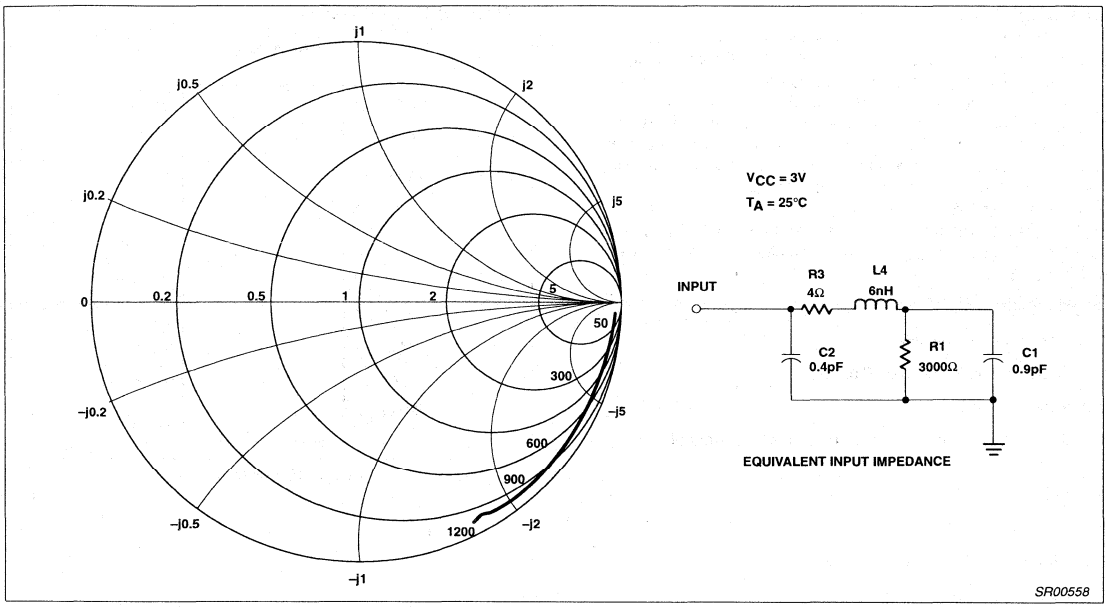


Figure 8. Typical N Package Input Impedance

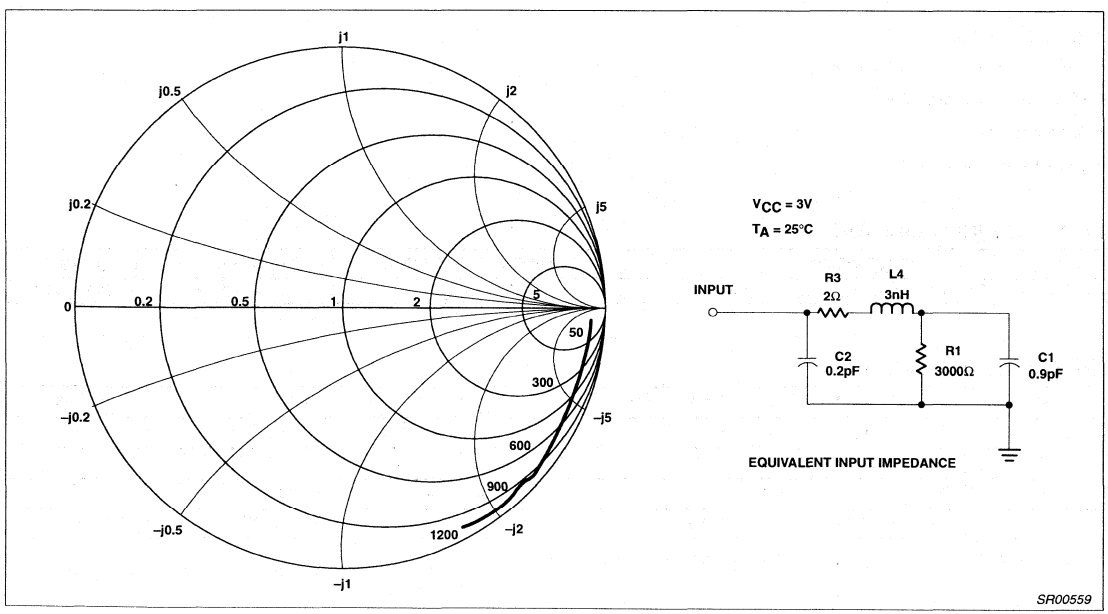


Figure 9. Typical D Package Input Impedance

1GHz low-voltage Fractional-N synthesizer SA7025

DESCRIPTION

The SA7025 is a monolithic low power, high performance dual frequency synthesizer fabricated in QUBiC BiCMOS technology. Featuring Fractional-N division with selectable modulo 5 or 8 implemented in the Main synthesizer to allow the phase detector comparison frequency to be five or eight times the channel spacing. This feature reduces the overall division ratio yielding a lower noise floor and faster channel switching. The phase detectors and charge pumps are designed to achieve phase detector comparison frequencies up to 5MHz. A triple modulus prescaler (divide by 64/65/72) is integrated on chip with a maximum input frequency of 1.04GHz. Programming and channel selection are realized by a high speed 3-wire serial interface.

FEATURES

- Operation up to 1.04GHz
- Fast locking by "Fractional-N" divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High speed serial input
- Low power consumption
- Programmable charge pump currents
- Supply voltage range 2.7 to 5.5V
- Excellent input sensitivity: V_{RF_IN} = –20dBm

APPLICATIONS

- NADC (North American Digital Cellular)
- PDC (Personal Digital Cellular)
- Cellular radio
- Spread-spectrum receivers

PIN CONFIGURATION

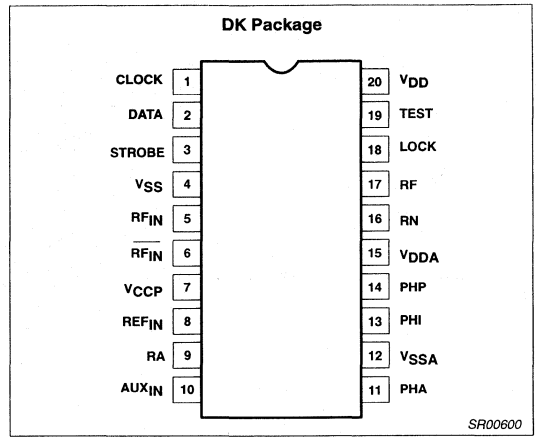


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA7025DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V	Supply voltage, V_{DD}, V_{DDA}, V_{CCP}	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{DD} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W. This device is ESD sensitive.

PIN DESCRIPTIONS

Symbol	Pin	Description
CLOCK	1	Serial clock input
DATA	2	Serial data input
STROBE	3	Serial strobe input
V_{SS}	4	Digital ground
RF_{IN}	5	Prescaler positive input
$\overline{RF_{IN}}$	6	Prescaler negative input
V_{CCP}	7	Prescaler positive supply voltage. This pin supplies power to the prescaler and RF input buffer
REF_{IN}	8	Reference divider input
RA	9	Auxiliary current setting; resistor to V_{SSA}
AUX_{IN}	10	Auxiliary divider input
PHA	11	Auxiliary phase detector output
V_{SSA}	12	Analog ground
PHI	13	Integral phase detector output
PHP	14	Proportional phase detector output
V_{DDA}	15	Analog supply voltage. This pin supplies power to the charge pumps, Auxiliary prescaler, Auxiliary and Reference buffers.
RN	16	Main current setting; resistor to V_{SSA}
RF	17	Fractional compensation current setting; resistor to V_{SSA}
LOCK	18	Lock detector output
TEST	19	Test pin; connect to V_{DD}
V_{DD}	20	Digital supply voltage. This pin supplies power to the CMOS digital part of the device

BLOCK DIAGRAM

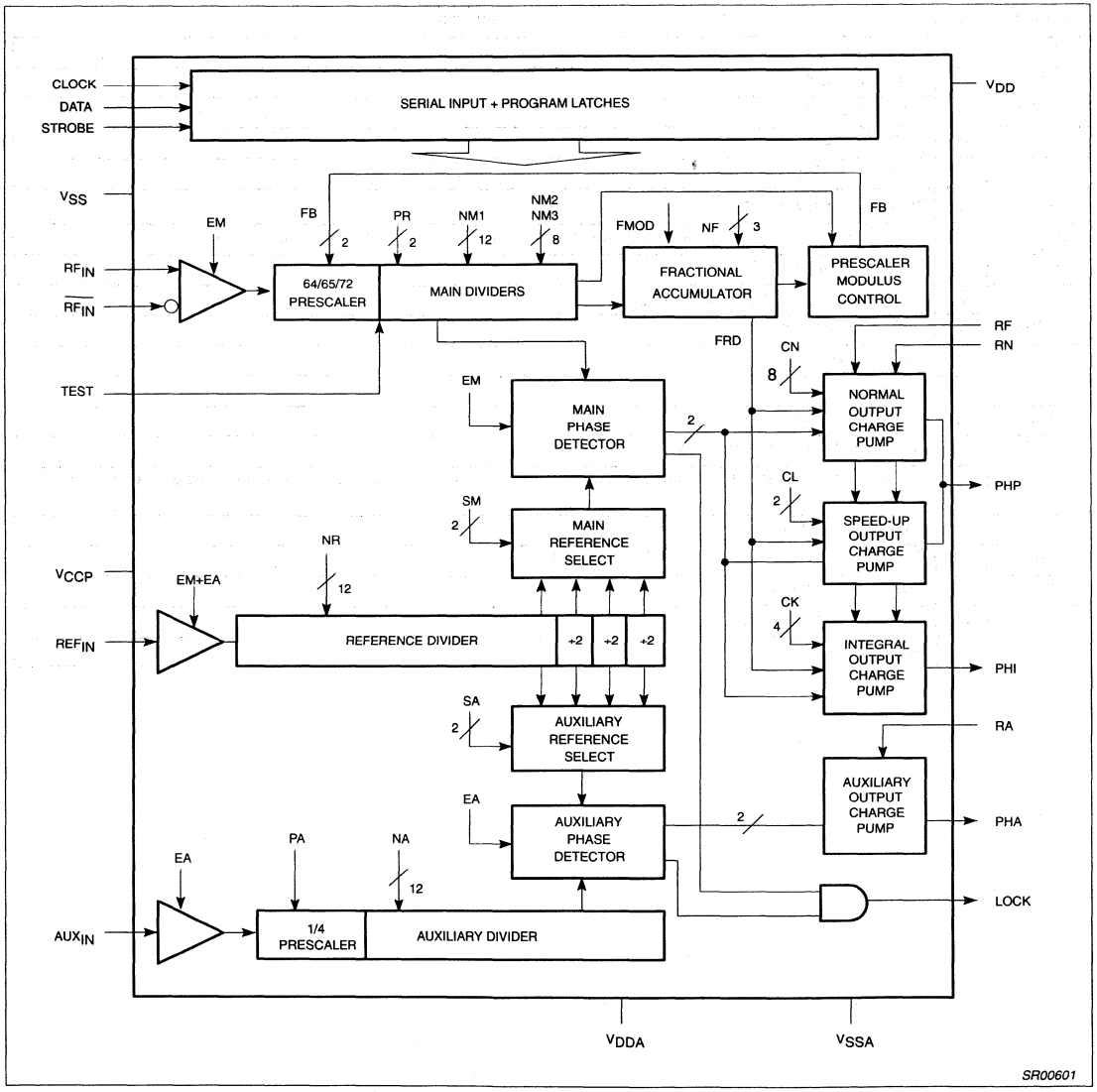


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{SUPPLY}	Recommended operating conditions	$V_{CCP} = V_{DD}$, $V_{DDA} \geq V_{DD}$	2.7		5.5	V
$I_{STANDBY}$	Total standby supply currents	EM = EA = 0, $I_{RN} = I_{RF} = I_{RA} = 0$		50	500	µA
Operational supply currents: $I = I_{DD} + I_{CCP} + I_{DDA}$; $I_{RN} = 25\mu A$, $I_{RA} = 25\mu A$, (see Note 5)						
I_{AUX}	Operational supply currents	EM = 0, EA = 1		3.5		mA
I_{MAIN}	Operational supply currents	EM = 1, EA = 0		5.5		mA
I_{TOTAL}	Operational supply currents	EM = EA = 1		7.5		mA
Digital inputs CLK, DATA, STROBE						
V_{IH}	High level input voltage range		$0.7xV_{DD}$		V_{DD}	V
V_{IL}	Low level input voltage range		0		$0.3xV_{DD}$	V
Digital outputs LOCK						
V_{OL}	Output voltage LOW	$I_O = 2mA$			0.4	V
V_{OH}	Output voltage HIGH	$I_O = -2mA$	$V_{DD}-0.4$			V
Charge pumps: $V_{DDA} = 3V$ / $I_{RX} = 25\mu A$ or $V_{DDA} = 5V$ / $I_{RX} = 62.5\mu A$, V_{PHX} in range, unless otherwise specified. (See Note 16)						
$\|I_{RX}\|$	Setting current range for any setting resistor	$2.7V < V_{DDA} < 5.5V$		25		µA
		$4.5V < V_{DDA} < 5.5V$		62.5		
V_{PHOUT}	Output voltage range		0.7		$V_{DDA}-0.8$	V
Charge pump PHA						
$\|I_{PHA}\|$	Output current PHA	$I_{RA} = -62.5\mu A$; $V_{PHA} = V_{DDA}/2$ [13]	400	500	600	µA
		$I_{RA} = -25\mu A$; $V_{PHA} = V_{DDA}/2$	160	200	240	
$\frac{\Delta\|I_{PHP\_A}\|}{\|I_{PHP\_A}\|}$	Relative output current variation PHA	$I_{RA} = -62.5\mu A$ [2, 13]		2	6	%
ΔI_{PHA_M}	Output current matching PHA pump	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±50	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±65	
Charge pump PHP, normal mode [1, 4, 6] $V_{RF} = V_{DDA}$						
$\|I_{PHP\_N}\|$	Output current PHP	$I_{RN} = -62.5\mu A$; $V_{PHP} = V_{DDA}/2$ [13]	440	550	660	µA
		$I_{RN} = -25\mu A$; $V_{PHP} = V_{DDA}/2$	175	220	265	
$\frac{\Delta I_{PHP\_N}}{I_{PHP\_N}}$	Relative output current variation PHP	$I_{RN} = -62.5\mu A$ [2, 13]		2	6	%
$\Delta I_{PHP\_N\_M}$	Output current matching PHP normal mode	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±50	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±65	
Charge pump PHP, speed-up mode [1, 4, 7] $V_{RF} = V_{DDA}$						
$\|I_{PHP\_S}\|$	Output current PHP	$I_{RN} = -62.5\mu A$; $V_{PHP} = V_{DDA}/2$ [13]	2.20	2.75	3.30	mA
		$I_{RN} = -25\mu A$; $V_{PHP} = V_{DDA}/2$	0.85	1.1	1.35	
$\frac{\Delta I_{PHP\_S}}{I_{PHP\_S}}$	Relative output current variation PHP	$I_{RN} = -62.5\mu A$ [2, 13]		2	6	%
$\Delta I_{PHP\_S\_M}$	Output current matching PHP speed-up mode	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±250	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±300	
Charge pump PHI, speed-up mode [1, 4, 8] $V_{RF} = V_{DDA}$						
$\|I_{PHI}\|$	Output current PHI	$I_{RN} = -62.5\mu A$; $V_{PHI} = V_{DDA}/2$ [13]	4.4	5.5	6.6	mA
		$I_{RN} = -25\mu A$; $V_{PHI} = V_{DDA}/2$	1.75	2.2	2.65	
$\frac{\Delta I_{PHI}}{I_{PHI}}$	Relative output current variation PHI	$I_{RN} = -62.5\mu A$ [2, 13]		2	8	%
ΔI_{PHI_M}	Output current matching PHI pump	$V_{DDA} = 3V$, $I_{RA} = 25\mu A$			±500	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5\mu A$			±600	
Fractional compensation PHP, normal mode [1, 9] $V_{RN} = V_{DDA}$, $V_{PHP} = V_{DDA}/2$						
$I_{PHP\_F\_N}$	Fractional compensation output current PHP vs F_{RD} [3]	$I_{RF} = -62.5\mu A$; $F_{RD} = 1$ to 7 [13]	–625	–400	–250	nA
		$I_{RF} = -25\mu A$; $F_{RD} = 1$ to 7	–250	–180	–100	

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Fractional compensation PHP, speed up mode [1, 10] $V_{PHP} = V_{DDA}$, $V_{RN} = V_{DDA}$						
$I_{PHP\_F\_S}$	Fractional compensation output current PHP vs F_{RD}[3]	I_{RF} = –62.5µA;F_{RD} = 1 to 7[13]	–3.35	–2.0	–1.1	µA
		I_{RF} = –25µA;F_{RD} = 1 to 7	–1.35	–1.0	–0.5	
	Pump leakage		–20		20	nA
Fractional compensation PHI, speed up mode [1, 11] $V_{PHP} = V_{DDA}/2$, $V_{RN} = V_{DDA}$						
I_{PHI_F}	Fractional compensation output current PHI vs F_{RD}[3]	I_{RF} = –62.5µA;F_{RD} = 1 to 7[13]	–5.4	–4.0	–2.6	µA
		I_{RF} = –25µA;F_{RD} = 1 to 7	–2.15	–1.6	–1.05	
Charge pump leakage currents, charge pump not active						
I_{PHP_L}	Output leakage current PHP; normal mode[1]	V_{PHP} = 0.7 to V_{DDA} – 0.8		0.1	10	nA
I_{PHI_L}	Output leakage current PHI; normal mode[1]	V_{PHI} = 0.7 to V_{DDA} – 0.8		0.1	10	nA
I_{PHA_L}	Output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} – 0.8		0.1	10	nA

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP}$ = 3V; T_A = 25°C; f_{RF_IN} = 1GHz, input level = –20dBm; unless otherwise specified. Test Circuit, Figure 4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Main divider						
f_{RF_IN}	Input signal frequency	Direct coupled input[14]			1.04	GHz
		1000pF input coupling			1.04	
V_{RF_IN}	Input sensitivity	1040MHz	–20		0	dBm
Reference divider ($V_{DD} = V_{DDA}$ = 3V or V_{DD} = 3V / V_{DDA} = 5V)						
f_{REF_IN}	Input signal frequency	2.7 < V_{DD} and V_{DDA} < 5.5V			25	MHz
		2.7 < V_{DD} and V_{DDA} < 4.5V			30	
V_{REF_IN}	Input signal range, AC coupled	2.7 < V_{DD} and V_{DDA} < 5.5V	500			mV_{P-P}
		2.7 < V_{DD} and V_{DDA} < 4.5V	300			
Z_{REF_IN}	Reference divider input impedance[15]			100		kΩ
				3		pF
Auxiliary divider						
f_{AUX_IN}	Input signal frequency PA="0", prescaler enabled		0		50	MHz
		4.5V ≤ V_{DDA} ≤ 5.5V	0		150	
		4.0V ≤ V_{DDA} ≤ 5.5V; Pin ≥ –12dBm	0		180	
	Input signal frequency PA="1", prescaler enabled		0		30	
		4.5V ≤ V_{DDA} ≤ 5.5V	0		40	
V_{AUX_IN}	Input signal range, AC coupled		200			mV_{P-P}
Z_{AUX_IN}	Auxiliary divider input impedance			100		kΩ
				3		pF
Serial interface[15]						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time; CLOCK to DATA		30			ns
t_W	Pulse width; CLOCK		30			ns
	Pulse width; STROBE	B, C, D, E words	30			
In-Loop Performance[17] V_{DDA} = 5V, V_{DD} = 2.7V						
R_{MM}	Main loop residual FM	FVCO = 1030MHz		300	600	Hz

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
t_{SW}	Pulse width; STROBE	A word, PR = '01'	$\frac{1}{f_{VCO}} \cdot (NM2 \cdot 65) + t_W$			ns
		A word, PR = '10'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM3 + 1) \cdot 72] + t_W$			

NOTES:

1. When a serial input "A" word is programmed, the main charge pumps on PHP and PHI are in the "speed up mode" as long as STROBE = H. When this is not the case, the main charge pumps are in the "normal mode".
2. The relative output current variation is defined thus:
$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|}$$; with $V_1 = 0.7V$, $V_2 = V_{DDA} - 0.8V$ (see Figure 3).
3. F_{RD} is the value of the 3 bit fractional accumulator.
4. Monotonicity is guaranteed with C_N = 0 to 255.
5. Power supply current measured with $V_{DD} = V_{CCP} = 3V$, $V_{DDA} = 5V$, $f_{RF\ IN} = 915.99MHz$, XTAL at 21.36MHz, AUX at 85.92MHz (PA = '0'), Main comp frequency = 240kHz, Auxiliary comp frequency = 120kHz, CN = 160, CL = 0, CK = 0. Internal registers NM1 = 52, NM2 = 0, NM3 = 4, PR = '10', SM = '00', SA = '01', NA = 179, NF = 5, FMOD = 8, NR = 89, PA = 0, IRN = IRA = IRF = 25µA, lock condition, normal mode. Operational supply current = $I_{DDA} + I_{DD} + I_{CCP}$.
6. Specification condition: CN = 255
7. Specification conditions:
   1) CN = 255; CL = 1, or
   2) CN = 75; CL = 3
8. Typical output current $|I_{PHI}| = -I_{RN} \times CN \times 2^{(CL+1)} \times CK/32$:
   1) CN = 160; CL = 3; CK = 1, or
   2) CN = 160; CL = 2; CK = 2, or
   3) CN = 160; CL = 1; CK = 4, or
   4) CN = 160; CL = 0; CK = 8
9. Any RFD, CL = 1 for speed-up pump. The integral pump is intended for switching only and the fractional compensation is not guaranteed.
10. Specification conditions: F_{RD} = 1 to 7; CL = 1.
11. Specification conditions:
   1) F_{RD} = 1 to 7; CL = 1; CK = 2, or
   2) F_{RD} = 1 to 7; CL = 2; CK = 1.
12. The matching is defined by the sum of the P and the N pump for a given output voltage.
13. Limited analog supply voltage range 4.5 to 5.5V.
14. For f_{IN} < 50MHz, low frequency operation requires DC-coupling and a minimum input slew rate of 32V/µs.
15. Guaranteed by design.
16. Close in noise for the charge pumps is tested on a sample basis in a typical application in order to eliminate parts outside the normal distribution.
17. F_{XTAL} = 14.4MHz, V_{XTAL} = 500mV_{P-P}, comparison frequency = 200kHz, Loop bandwidth = 5kHz, Audio filter = 300Hz to 15kHz.

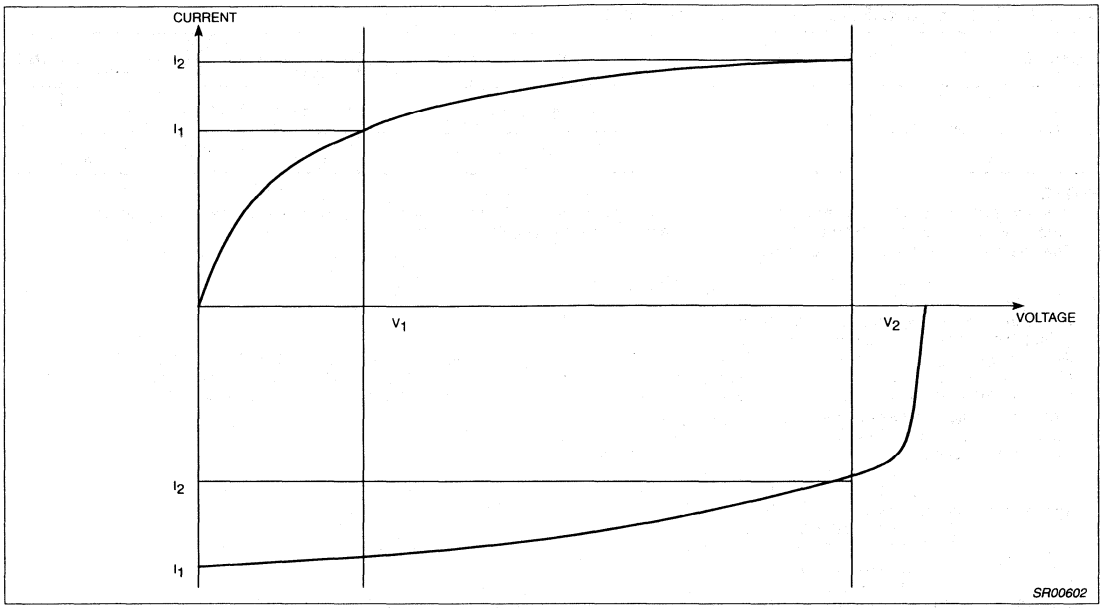


Figure 3. Relative Output Current Variation

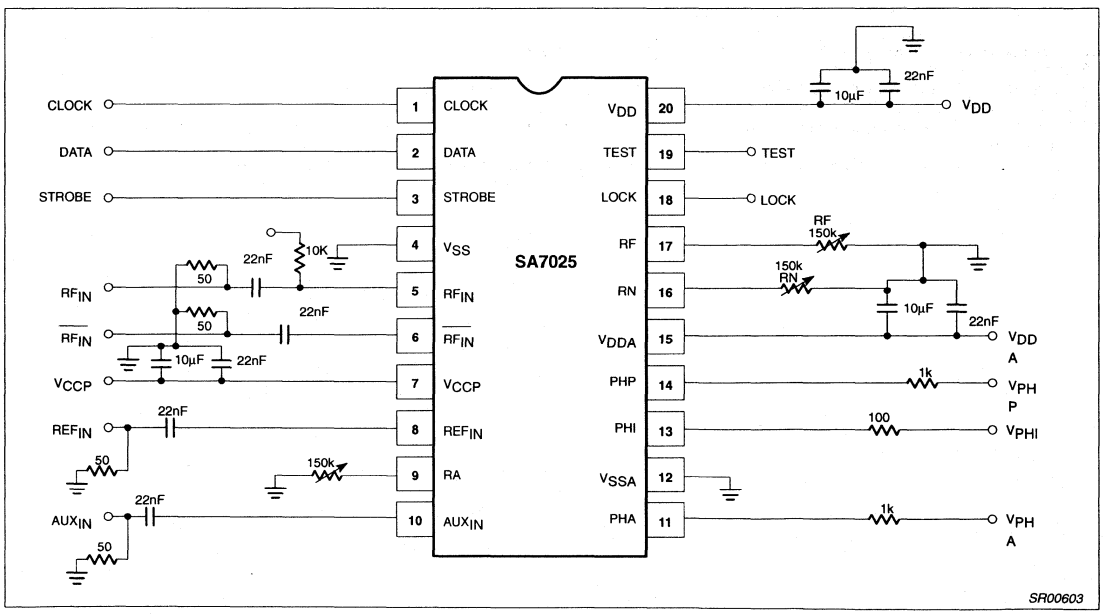


Figure 4. Test Circuit

AC TIMING CHARACTERISTICS

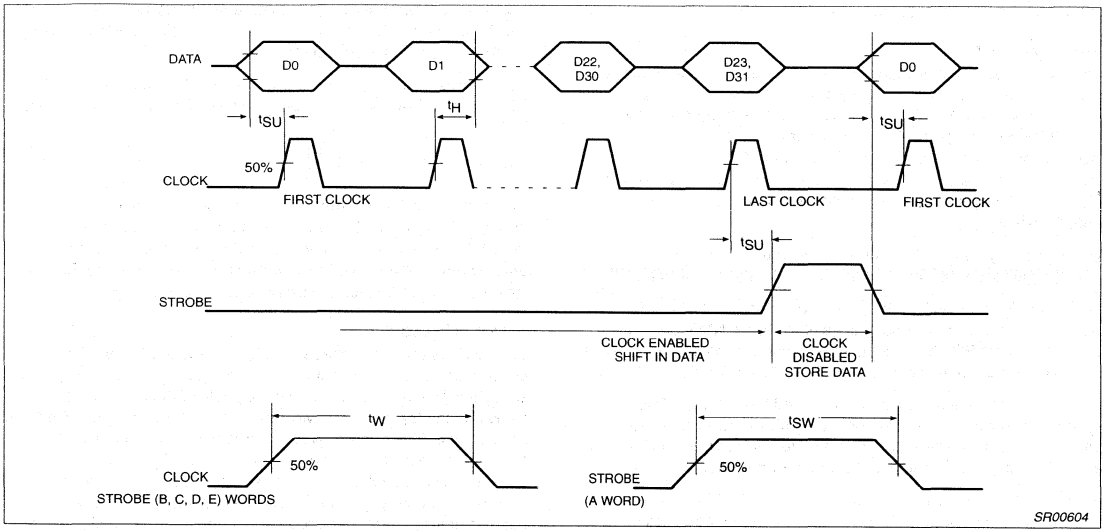


Figure 5. Serial Input Timing Sequence

FUNCTIONAL DESCRIPTION

Serial Input Programming

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32 bit words; each word includes 1 or 4 address bits. Figure 5 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent: D, C, B and A. Figure 6 and Table 1 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for CN and PR is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24 bit A0 word is used. CN will be directly loaded by programming a long 32 bit A1 word. The flag LONG in the D word determines whether A0 (LONG = "0") or A1 (LONG = "1") format is applicable. The A word contains new data for the main divider.

Main Divider Synchronization

The A word is loaded only when a main divider synchronization signal is also active in order to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. The signal is active while the NM1 divider is counting down from the programmed value. The new A word will be loaded after the NM1 divider has reached its terminal count; also, at this time a main divider output pulse will be sent to the main phase detector. The loading of the A word is disabled while the NM2 or NM3 dividers are counting up to their programmed values. Therefore, the new A word will be correctly loaded provided that the STROBE signal has been at an active high value for at least a minimum number of VCO input cycles at RF_{IN} or $\overline{RF_{IN}}$.

$$t\_strobe\_min = \frac{1}{f_{VCO}}(NM_2 \cdot 65) + t_W \text{ for PR} = \text{'01'}$$

$$t\_strobe\_min = \frac{1}{f_{VCO}}[NM_2 \cdot 65 + (NM_3 + 1) \cdot 72] + t_W \text{ for PR} = \text{'10'}$$

Programming the A word means also that the main charge pumps on output PHP and PHI are set into the speed-up mode as long as the STROBE is H.

Auxiliary Divider

The input signal on AUX_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled if the serial control bit EA = "1". Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = "0". This divider has been optimized to accept a high frequency input signal. If PA = "1", this divider is disabled and the input signal is fed directly to the second stage, which is a 12-bit programmable divider with standard input frequency (40MHz). The division ratio can be expressed as:

if PA = "0": N = 4 x NA

if PA = "1": N = NA; with NA = 4 to 4095

Reference Divider

The input signal on REF_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 4095) followed by a three bit binary counter. The 2 bit SM register (see Figure 7) determines which of the 4 output pulses is selected as the main

phase detector input. The 2 bit SA register determines the selection of the auxiliary phase detector signal.

Main Divider

The differential inputs are amplified (to internal ECL logic levels) and provide excellent sensitivity (–20dBm at 1GHz) making the prescaler ideally suited to directly interface to a VCO as integrated on the SA620 RF gain stage, VCO and mixer device. The internal triple modulus prescaler feedback loop FB controls the selection of the divide by ratios 64/65/72, and reduces the minimum system division ratio below the typical value required by standard dual modulus (64/65) devices.

This input stage is enabled when serial control bit EM = "1". Disabling means that all currents in the prescaler are switched off.

The main divider is built up by a 12 bit counter plus a sign bit. Depending on the serial input values NM1, NM2, NM3, and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles according to Table 2 and Table 3.

The loading of the work registers NM1, NM2, NM3 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as explained in the Serial Input Programming section.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = "1". Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider will then be

$$NQ = N + \frac{NF}{Q}$$

Programming a fraction means the prescaler with main divider will divide by N or N + 1. The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

Phase Detectors

The auxiliary and main phase detectors are a two D-type flip-flop phase and frequency detector shown in Figure 8. The flip-flops are set by the negative edges of output signals of the dividers. The rising edge of the signal, L, will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

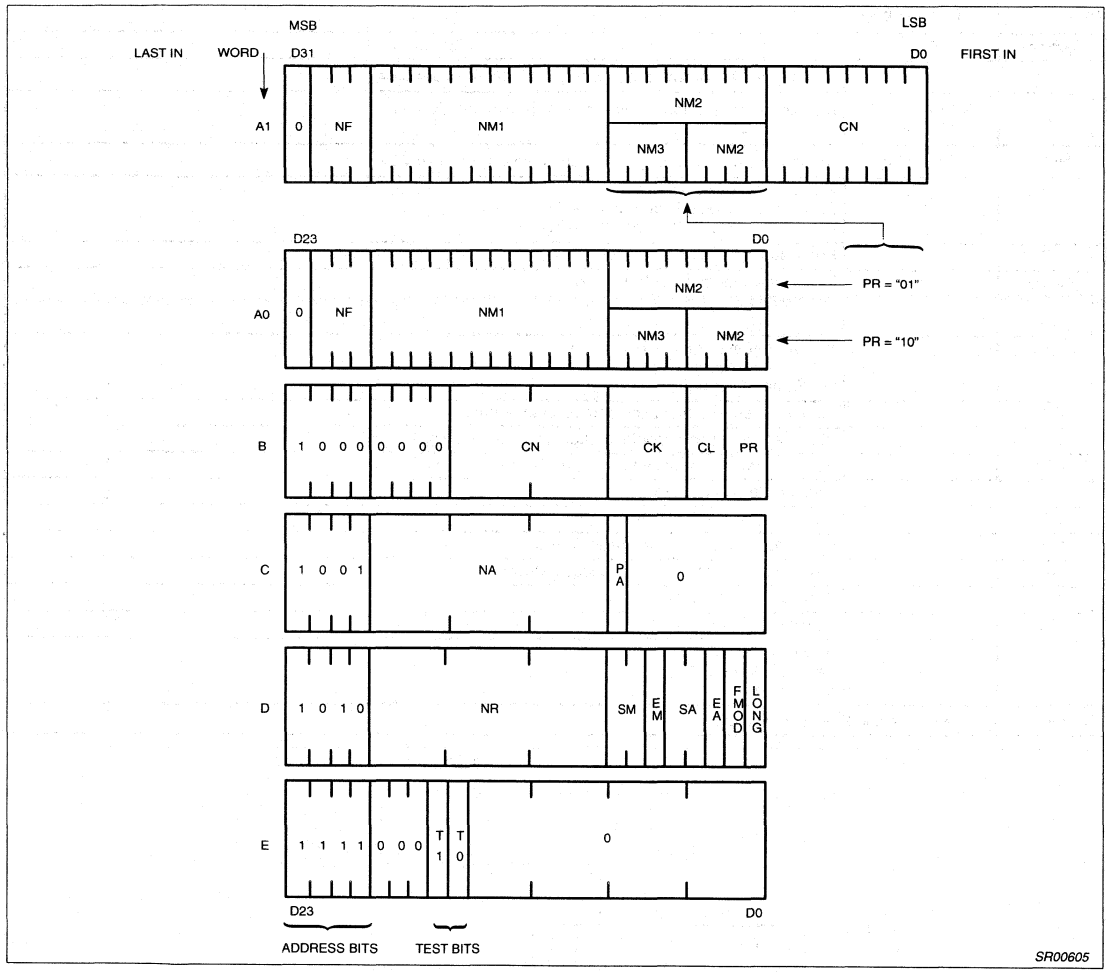


Figure 6. Serial Input Word Format

Current Settings

The SA7025 has 3 current setting pins: RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current connected between the current setting pin and V_{SS}. The typical value R (current setting resistor) can be calculated with the formula:

$$R = \frac{V_{DDA} - 0.9 - 150\sqrt{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary Output Charge Pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor RA at pin RA. The active charge pump current is typically:

$$|I_{PHA}| = 8 \cdot I_{RA}$$

Main Output Charge Pumps and Fractional Compensation Currents

The main charge pumps on pin PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 9 shows the waveforms for a typical case.

Table 1. Function Table

Symbol	Bits	Function
NM1	12	Number of main divider cycles when prescaler modulus = 64*
NM2	8 if PR = "01" 4 if PR = "10"	Number of main divider cycles when prescaler modulus = 65*
NM3	4 if PR = "10"	Number of main divider cycles when prescaler modulus = 72*
PR	2	Prescaler type in use PR = "01": modulus 2 prescaler (64/65) PR = "10": modulus 3 prescaler (64/65/72)
NF	3	Fractional-N increment
FMOD	1	Fractional-N modulus selection flag "1": modulo 8 "0": modulo 5
LONG	1	A word format selection flag "0": 24 bit A0 format "1": 32 bit A1 format
CN	8	Binary current setting factor for main charge pumps
CL	2	Binary acceleration factor for proportional charge pump current
CK	4	Binary acceleration factor for integral charge pump current
EM	1	Main divider enable flag
EA	1	Auxiliary divider enable flag
SM	2	Reference select for main phase detector
SA	2	Reference select for auxiliary phase detector
NR	12	Reference divider ratio
NA	12	Auxiliary divider ratio
PA	1	Auxiliary prescaler mode: PA = "0": divide by 4 PA = "1": divide by 1

*Not including reset cycles and Fractional-N effects.

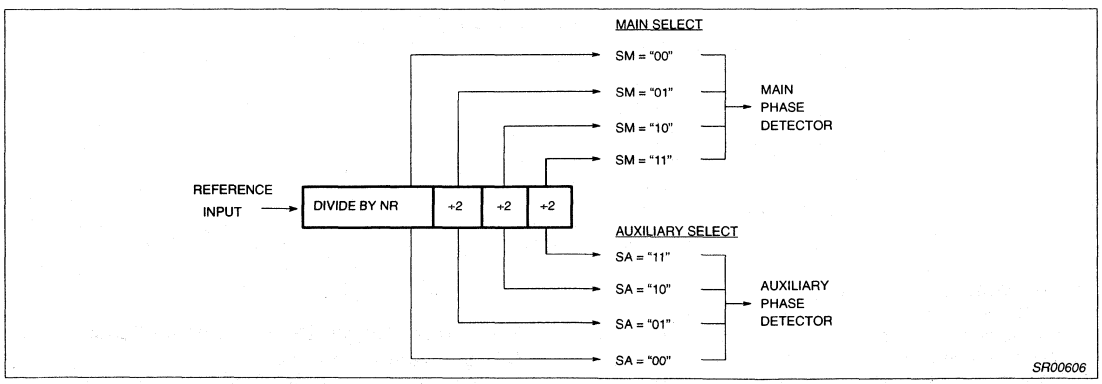


Figure 7. Reference Divider

Table 2. Prescaler Ratio

The total division ratio from prescaler to the phase detector may be expressed as:	
if PR = "01"	N = (NM1 + 2) x 64 + NM2 x 65
	N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 (*)
if PR = "10"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 72
	N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 72 (*)
(*) When the fractional accumulator overflows the prescaler ratio = 65 (64 + 1) and the total division ratio N' = N + 1	

Table 3. PR Modulus

PR	Modulus Prescaler	Bit Capacity		
		NM1	NM2	NM3
01	2	12	8	–
10	3	12	4	4

When the serial input A word is loaded, the output circuits are in the "speed-up mode" as long as the STROBE is H, else the "normal mode" is active. In the "normal mode" the current output PHP is:

$$I_{PHP\_N} = I_{PHP} + I_{PHP\_comp}$$

where:

$$|I_{PHP}| = \frac{CN \cdot I_{RN}}{32} \quad \text{:charge pump current}$$

$$|I_{PHP\_comp}| = FRD \cdot \frac{I_{RF}}{128} \quad \text{:fractional comp. current}$$

The current in PHI is zero in "normal mode".

In "speed-up mode" the current in output PHP is:

$$I_{PHP\_S} = I_{PHP} + I_{PHP\_comp}$$

$$|I_{PHP}| = \left(\frac{CN \cdot I_{RN}}{32}\right)(2^{CL+1} + 1)$$

$$|I_{PHP\_comp}| = \left(\frac{FRD \cdot I_{RF}}{128}\right)(2^{CL+1} + 1)$$

In "speed-up mode" the current in output PHI is:

$$I_{PHI\_S} = I_{PHI} + I_{PHI\_comp}$$

where:

$$|I_{PHI}| = \left(\frac{I_{RN}CN}{32}\right)(2^{CL+1})\ CK$$

$$|I_{PHI\_comp}| = \left(\frac{I_{RF}\ FRD}{128}\right)(2^{CL+1})\ CK$$

Figure 9 shows that for proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output. This means that the current setting on the input RN, RF is approximately:

$$\frac{I_{RN}}{I_{RF}} = \frac{(Q \cdot f_{VCO})}{(3 \cdot CN \cdot F_{INR})}$$

where:

Q	=	fractional-N modulus
$f_{VCO} = f_{INM} \times N$,		input frequency of the prescaler
F_{INR} =		input frequency of the reference divider

PHI pump is meant for switching only. Current and compensation are not as accurate as PHP.

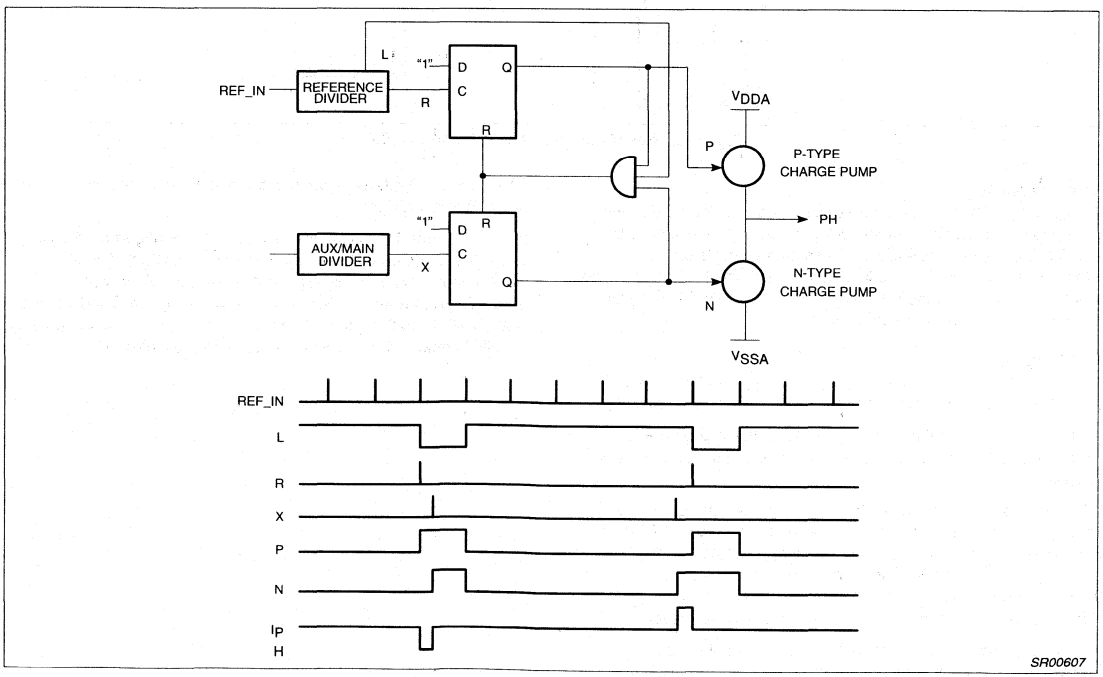


Figure 8. Phase Detector Structure with Timing

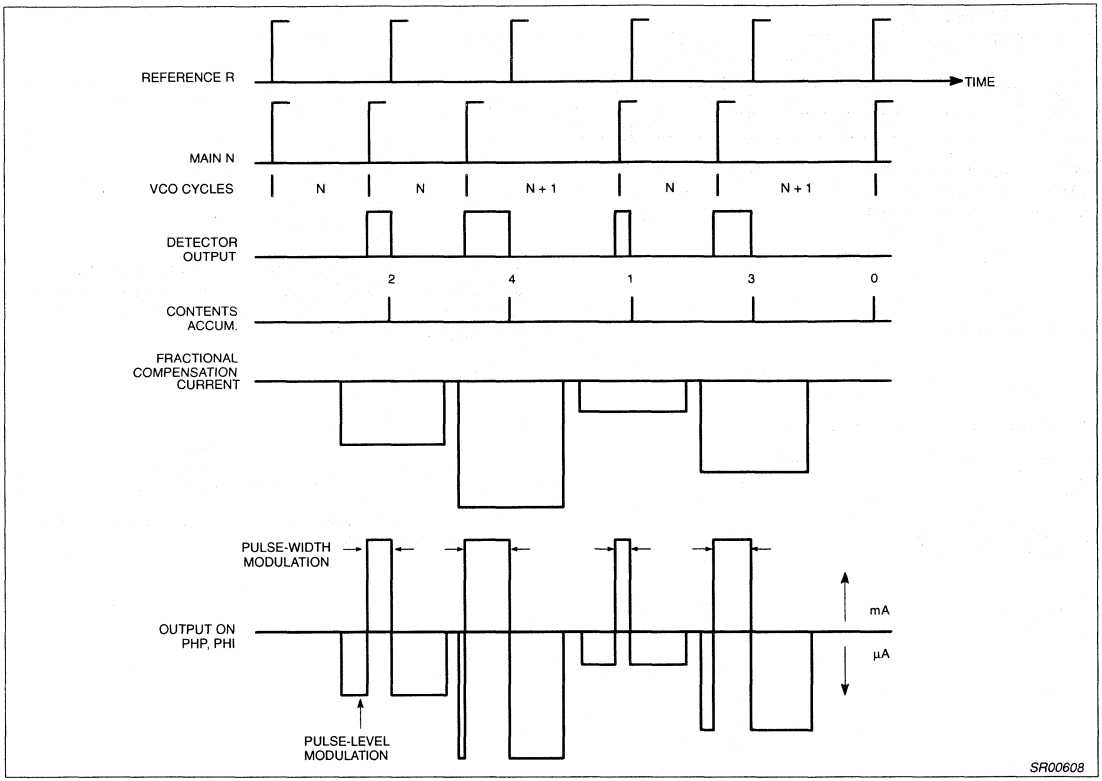


Figure 9. Waveforms for NF = 2, Fraction = 0.4

Lock Detect

The output LOCK is H when the auxiliary phase detector AND the main phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than +1 cycle on the reference input REF_IN. The lock condition is also fulfilled when the relative counter is disabled (EM = "0" or respectively EA = "0") for the main, respectively auxiliary counter.

Test Modes

The lock output is selectable as f_{REF}, f_{AUX}, f_{MAIN} and lock. Bits T1 and T0 of the E word control the selection (see Figures 6 and 10).

If T1 = T0 = Low, or if the E-word is not sent, the lock output is configured as the normal lock output described in the Lock Detect section.

If T1 = Low and T0 = High, the lock output is configured as f_{REF}. The signal is the buffered output of the reference divider NR and the 3-bit binary counter SM. The f_{REF} signal appears as normally low and pulses high whenever the divider reaches terminal count from the value programmed into the NR and SM registers. The f_{REF} signal can be used to verify the divide ratio of the Reference divider.

If T1 = High and T0 = Low, the lock output is configured as f_{AUX}. The signal is normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NA and PA registers. The f_{AUX} signal can be used to verify the divide ratio of the Auxiliary divider.

If T1 = High and T0 = High, the lock output is configured as f_{MAIN}. The signal is the buffered output of the MAIN divider. The f_{MAIN} signal appears as normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NM1, NM2 or NM3 registers. The f_{MAIN} signal can be used to verify the divide ratio of the MAIN divider and the prescaler.

Test Pin

The Test pin, Pin 19, is a buffered logic input which is exclusively ORed with the output of the prescaler. The output of the XOR gate is the input to the MAIN divider. The Test pin must be connected to V_{DD} during normal operation as a synthesizer. This pin can be used as an input for verifying the divide ratio of the MAIN divider; while in this condition the input to the prescaler, RF_{IN}, may be connected to V_{CCP} through a 10kΩ resistor in order to place prescaler output into a known state.

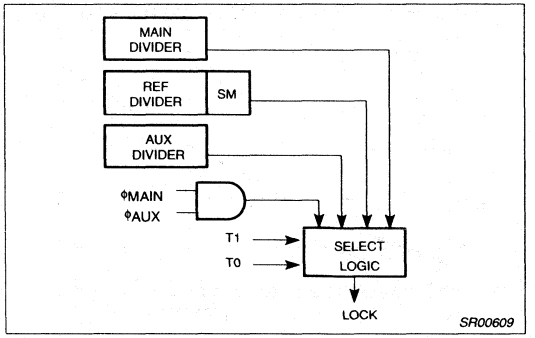


Figure 10. Test Mode Diagram

PIN FUNCTIONS

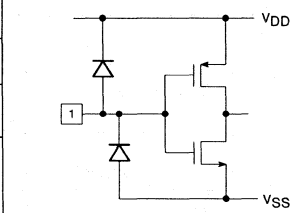
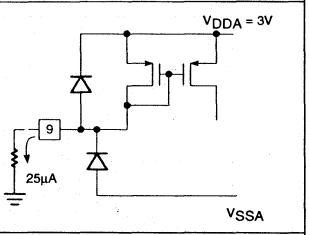
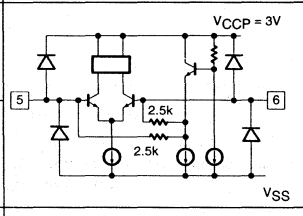
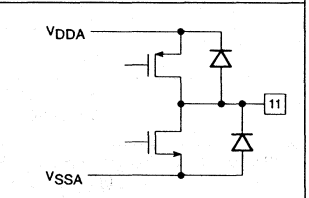
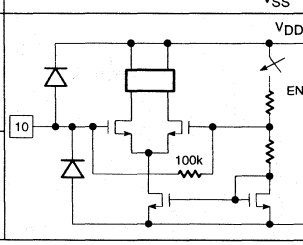
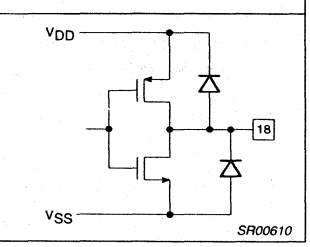
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	CLOCK	—		9	RA	1.35	
2	DATA	—		16	RN	1.35	
3	STROBE	—					
19	TEST	—		17	RF	1.35	
5	RF_{IN}	2.1		11	PHA	—	
6	$\overline{RF_{IN}}$	2.1		13	PHI	—	
				14	PHP	—	
8	REF_{IN}	1.8		18	LOCK	—	
10	AUX_{IN}	1.8					

Figure 11. Pin Functions

TYPICAL PERFORMANCE CHARACTERISTICS

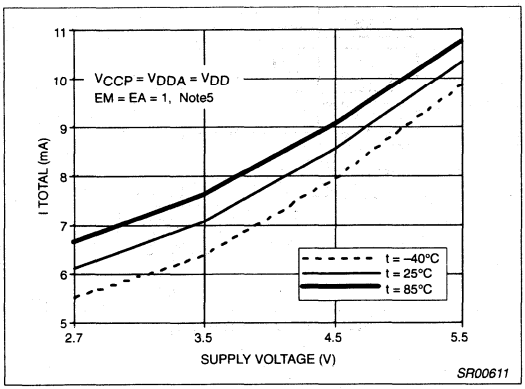


Figure 12. Operational Supply Current vs Supply Voltage and Temperature

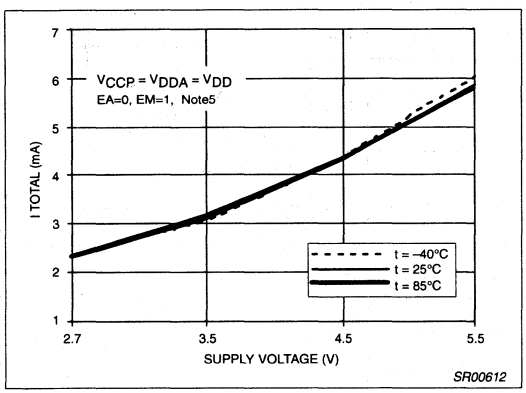


Figure 13. Auxiliary Operational Supply Current vs Supply Voltage and Temperature

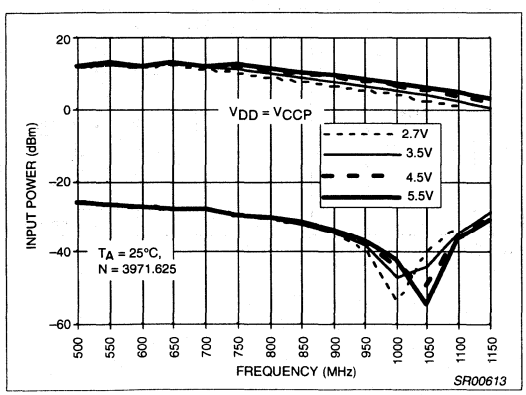


Figure 14. Main Divider Input Power vs frequency and Supply

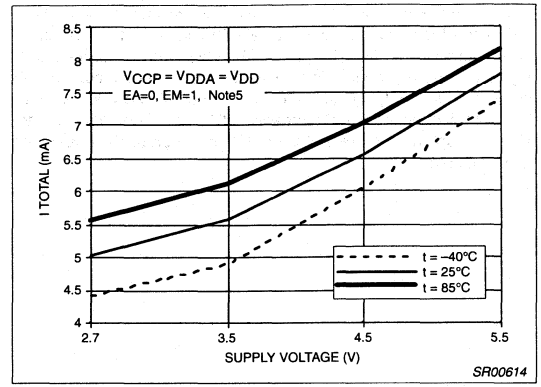


Figure 15. Main Operational Supply Current vs Supply Voltage and Temperature

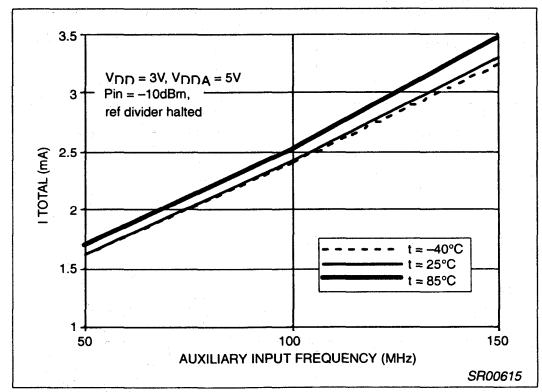


Figure 16. Auxiliary Operational Supply Current vs Frequency and Temperature

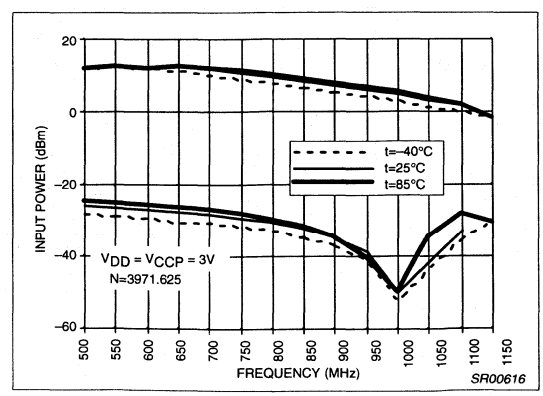


Figure 17. Main Divider Input Power vs Frequency and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

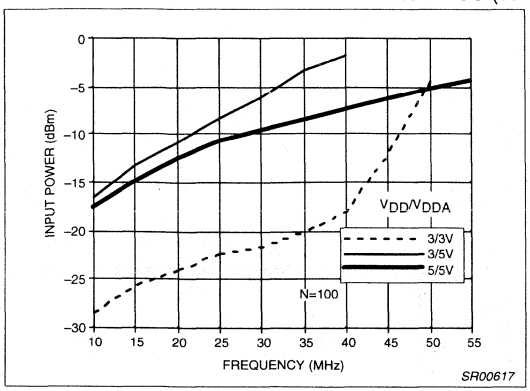


Figure 18. Reference Divider Minimum Input Power vs frequency and Supply

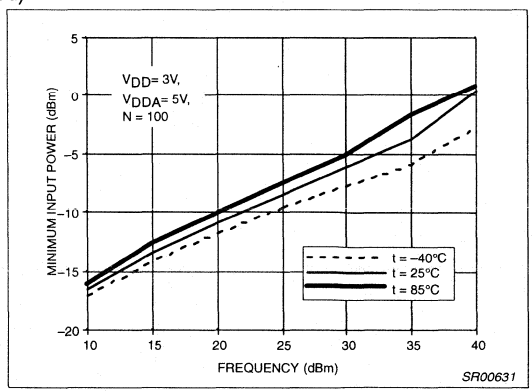


Figure 21. Reference Divider Minimum Input Power vs Frequency and Temperature

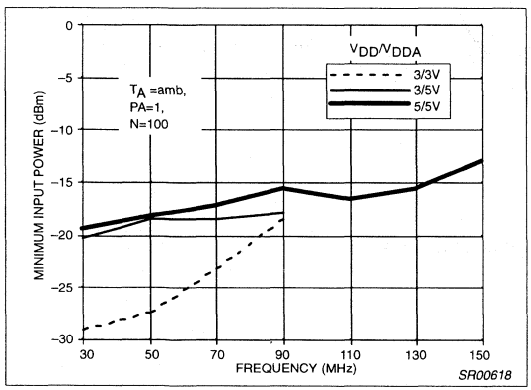


Figure 19. Auxiliary Divider Minimum Input Power vs Frequency and Supply

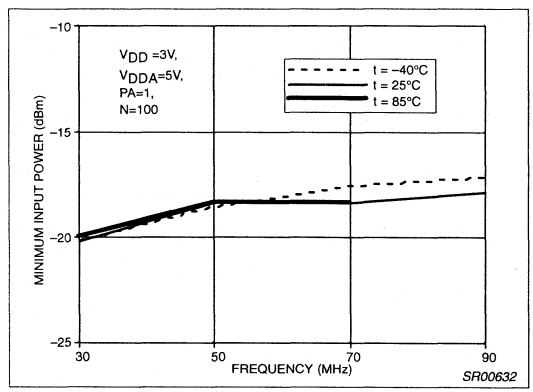


Figure 22. Auxiliary Divider Minimum Input Power vs Frequency and Temperature

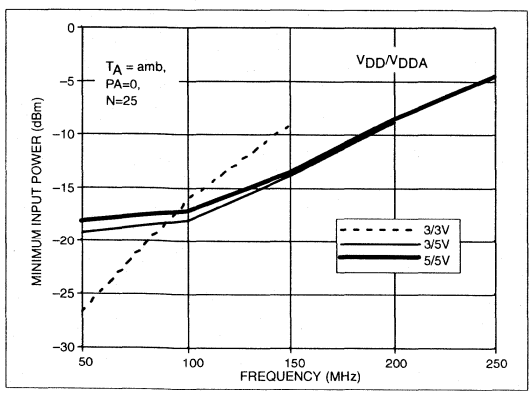


Figure 20. Auxiliary Divider Minimum Input Power vs Frequency and Supply

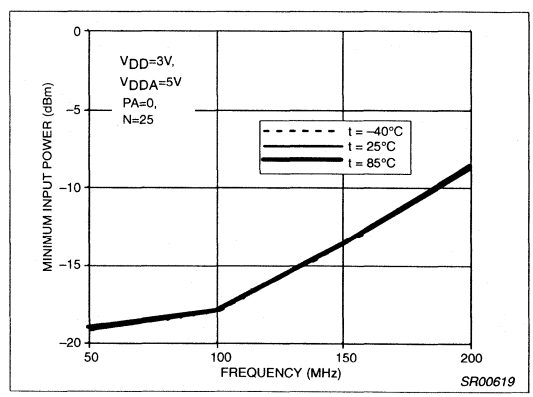


Figure 23. Auxiliary Divider Minumum Input Power vs Frequency and Temperature

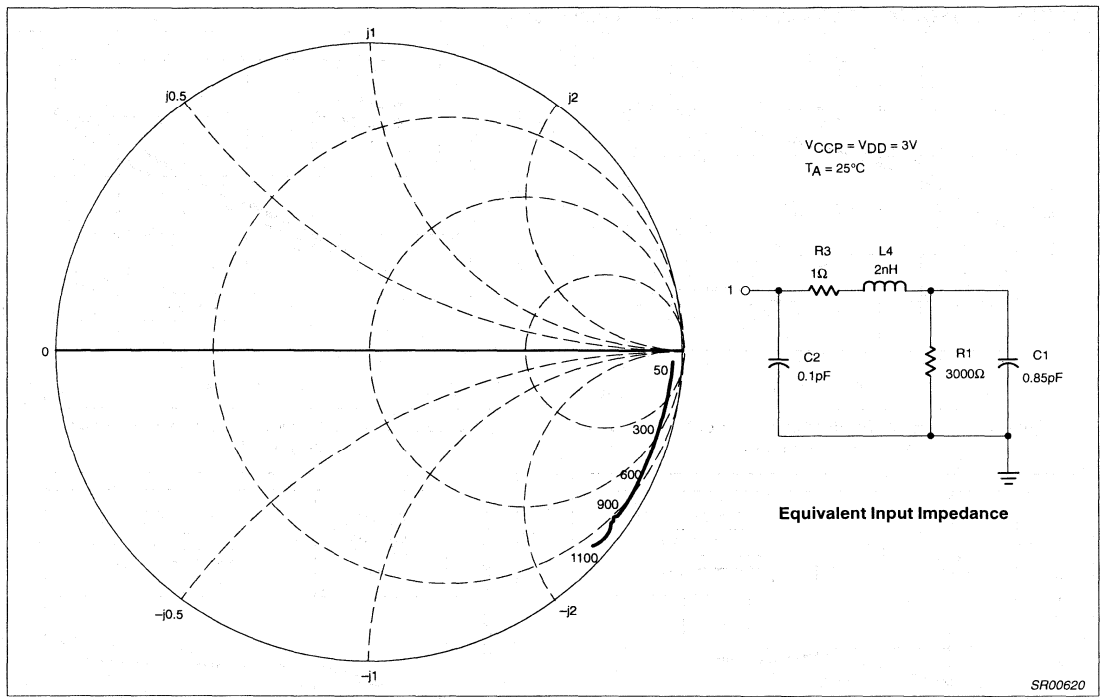
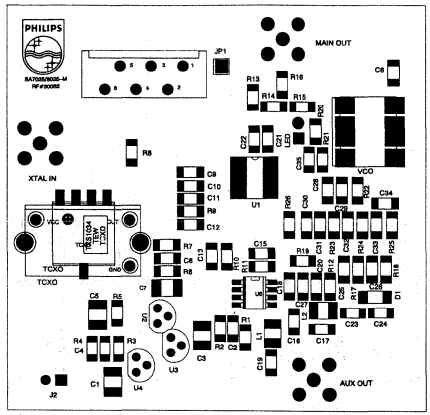
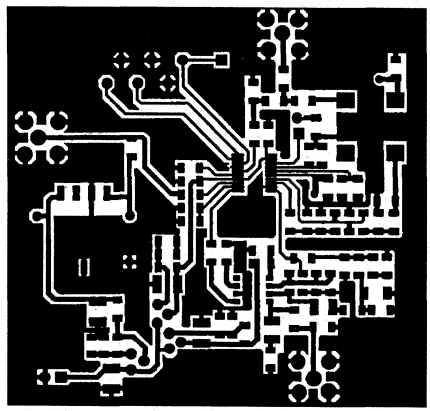


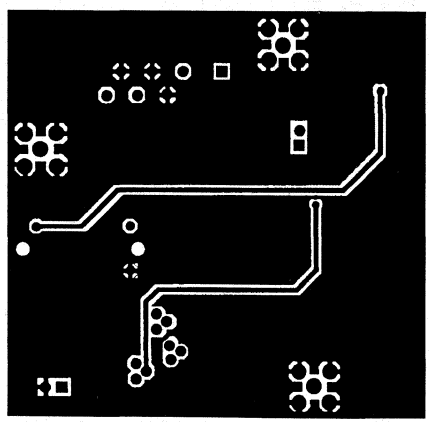
Figure 24. Typical RF_{IN} Input Impedance



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

SR00621

Figure 25. SA7025DK Demoboard Layout (NOT ACTUAL SIZE)

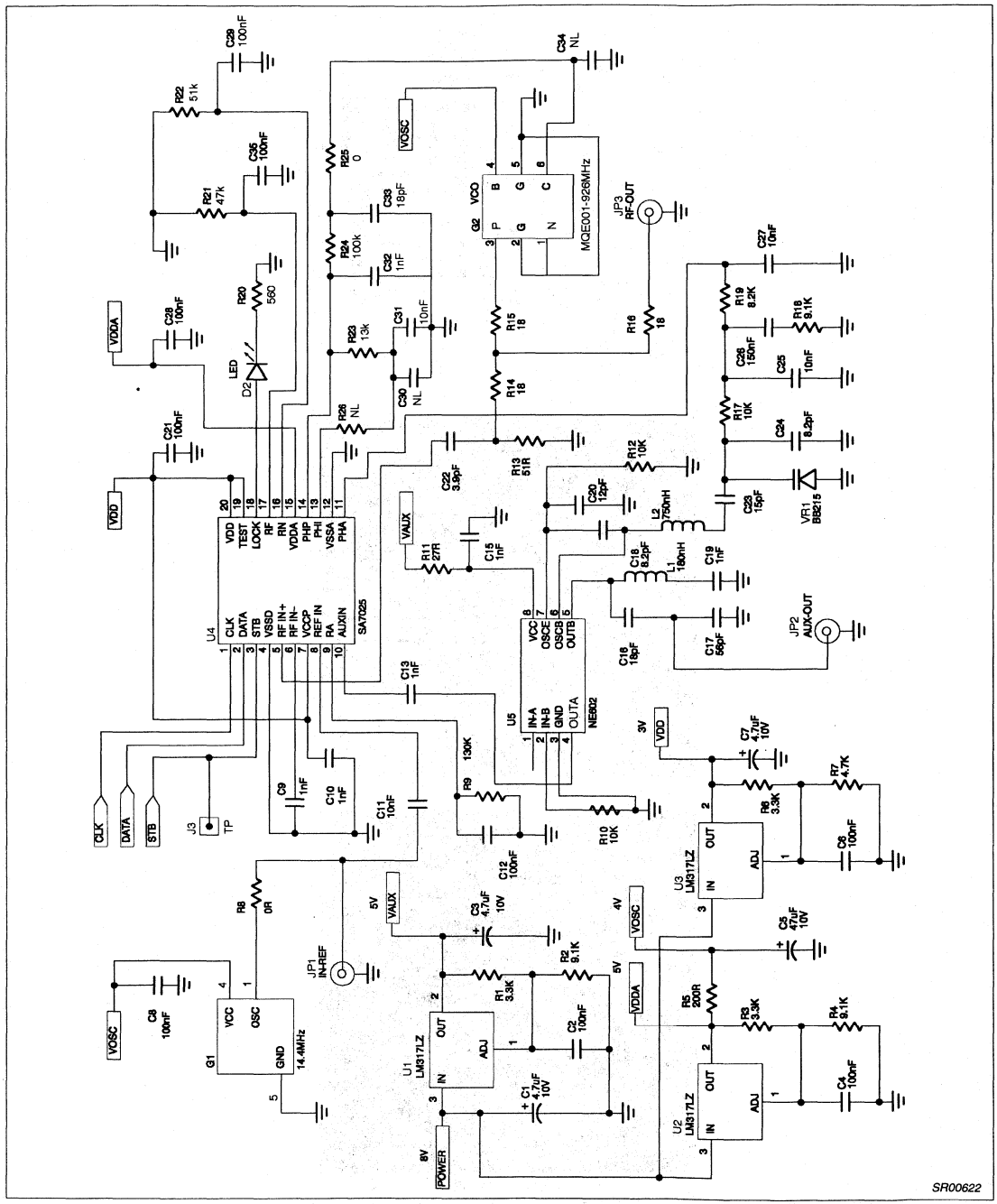
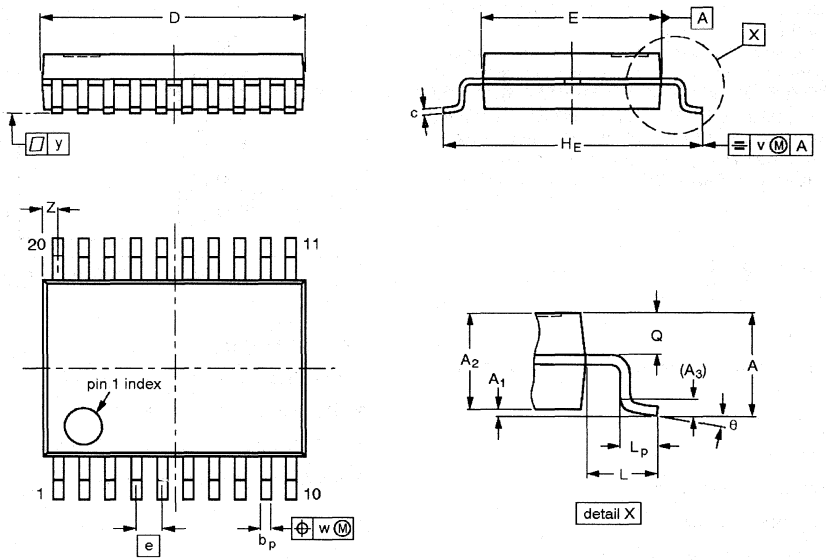
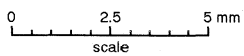


Figure 26. SA7025DK Application Circuit

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm SOT266-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

1.8GHz low-voltage Fractional-N synthesizer SA8025A

DESCRIPTION

The SA8025A is a monolithic low power, high performance dual frequency synthesizer fabricated in QUBiC BiCMOS technology. The SA8025A is an improved version of the SA8025, suitable for narrow band systems like the Japan Personal Digital Cellular (PDC) system. The new design improves the performance of the fractional spur compensation circuitry. The new version is pin-for-pin compatible with the previous version. Featuring Fractional-N division with selectable modulo 5 or 8 implemented in the Main synthesizer to allow the phase detector comparison frequency to be five or eight times the channel spacing. This feature reduces the overall division ratio yielding a lower noise floor and faster channel switching. The phase detectors and charge pumps are designed to achieve phase detector comparison frequencies up to 5MHz. A four modulus prescaler (divide by 64/65/68/73) is integrated on chip with a maximum input frequency of 1.8GHz at 3V. Programming and channel selection are realized by a high speed 3-wire serial interface. A 1GHz version (SA7025DK) is also available with the same pinout.

FEATURES

- Operation up to 1.8GHz at 3V
- Fast locking by "Fractional-N" divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High speed serial input
- Low power consumption
- Programmable charge pump currents
- Supply voltage range 2.7 to 5.5V
- Excellent input sensitivity: V_{RF_IN} = –20dBm

PIN CONFIGURATION

DK Package

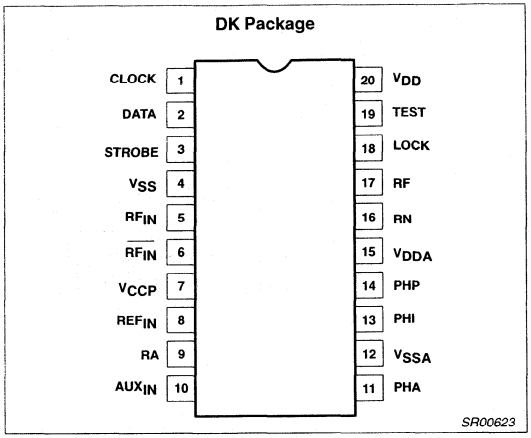


Figure 1. Pin Configuration

APPLICATIONS

- PHS (Personal Handy-phone System)
- PDC (Personal Digital Cellular)
- PCS (Personal Communication Service)
- Portable communication systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA8025ADK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V	Supply voltage, V_{DD}, V_{DDA}, V_{CCP}	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{DD} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W. This device is ESD sensitive.

PIN DESCRIPTIONS

Symbol	Pin	Description
CLOCK	1	Serial clock input
DATA	2	Serial data input
STROBE	3	Serial strobe input
V_{SS}	4	Digital ground
RF_{IN}	5	Prescaler positive input
$\overline{RF_{IN}}$	6	Prescaler negative input
V_{CCP}	7	Prescaler positive supply voltage. This pin supplies power to the prescaler and RF input buffer
REF_{IN}	8	Reference divider input
RA	9	Auxiliary current setting; resistor to V_{SSA}
AUX_{IN}	10	Auxiliary divider input
PHA	11	Auxiliary phase detector output
V_{SSA}	12	Analog ground
PHI	13	Integral phase detector output
PHP	14	Proportional phase detector output
V_{DDA}	15	Analog supply voltage. This pin supplies power to the charge pumps, Auxiliary prescaler, Auxiliary and Reference buffers.
RN	16	Main current setting; resistor to V_{SSA}
RF	17	Fractional compensation current setting; resistor to V_{SSA}
LOCK	18	Lock detector output
TEST	19	Test pin; connect to V_{DD}
V_{DD}	20	Digital supply voltage. This pin supplies power to the CMOS digital part of the device

BLOCK DIAGRAM

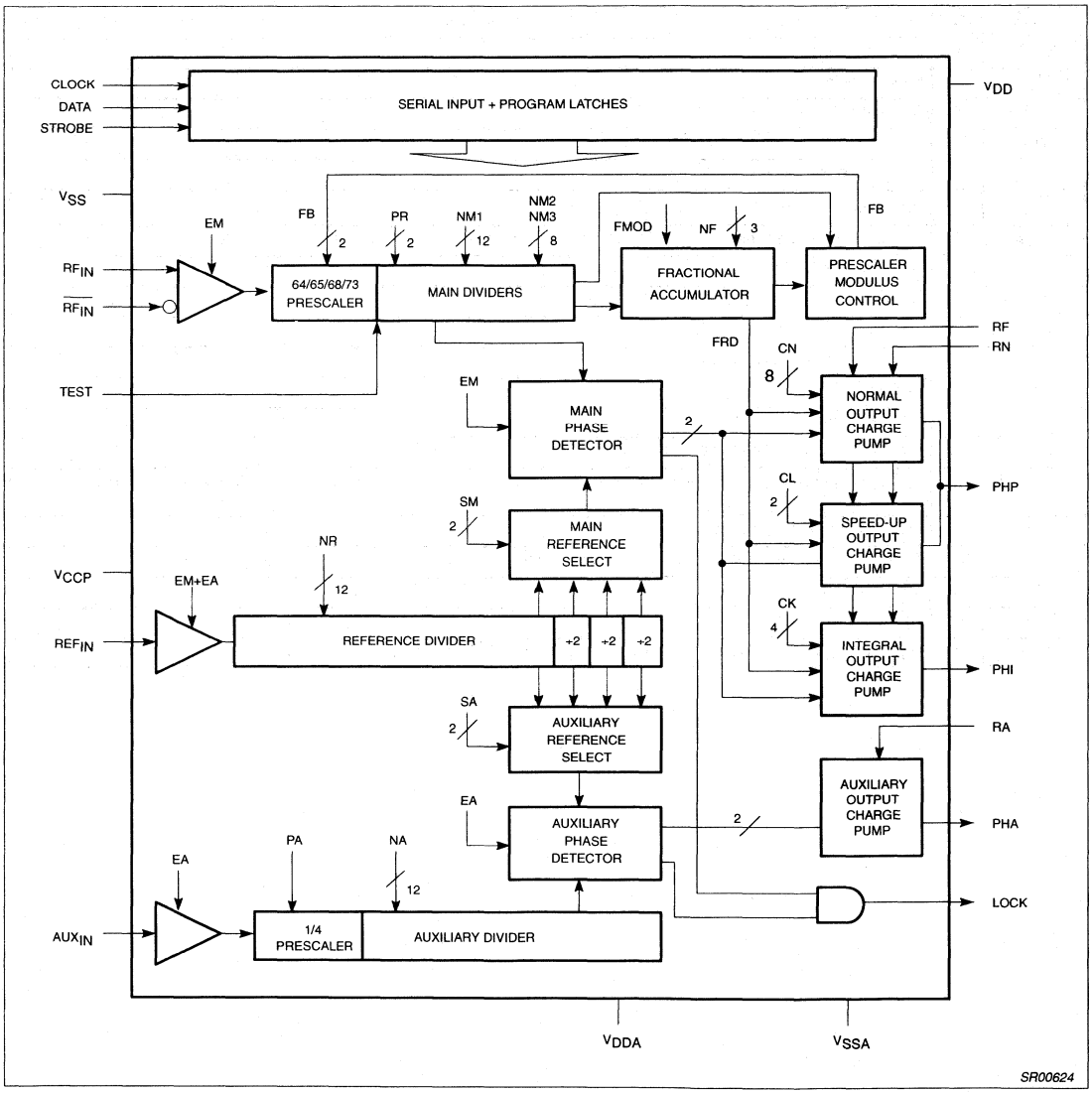


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{SUPPLY}	Recommended operating conditions	$V_{CCP} = V_{DD}$, $V_{DDA} \geq V_{DD}$	2.7		5.5	V
$I_{STANDBY}$	Total standby supply currents	EM = EA = 0, $I_{RN} = I_{RF} = I_{RA} = 0$		50	500	µA
Operational supply currents: $I = I_{DD} + I_{CCP} + I_{DDA}$; $I_{RN} = 25µA$, $I_{RA} = 25µA$, (see Note 5)						
I_{AUX}	Operational supply currents	EM = 0, EA = 1		3.5		mA
I_{MAIN}	Operational supply currents	EM = 1, EA = 0		11.0		mA
I_{TOTAL}	Operational supply currents	EM = EA = 1		13.5		mA
Digital inputs CLK, DATA, STROBE						
V_{IH}	High level input voltage range		$0.7xV_{DD}$		V_{DD}	V
V_{IL}	Low level input voltage range		0		$0.3xV_{DD}$	V
Digital outputs LOCK						
V_{OL}	Output voltage LOW	$I_O = 2mA$			0.4	V
V_{OH}	Output voltage HIGH	$I_O = -2mA$	$V_{DD}-0.4$			V
Charge pumps: $V_{DDA} = 3V$ / $I_{RX} = 25µA$ or $V_{DDA} = 5V$ / $I_{RX} = 62.5µA$, V_{PHX} in range, unless otherwise specified.						
$\|I_{RX}\|$	Setting current range for any setting resistor	$2.7V < V_{DDA} < 5.5V$		25		µA
		$4.5V < V_{DDA} < 5.5V$		62.5		
V_{PHOUT}	Output voltage range		0.7		$V_{DDA}-0.8$	V
Charge pump PHA						
$\|I_{PHA}\|$	Output current PHA	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2$ [13]	400	500	600	µA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	160	200	240	
$\frac{\Delta\|I_{PHP\_A}\|}{\|I_{PHP\_A}\|}$	Relative output current variation PHA	$I_{RA} = -62.5µA$ [2, 13]		2	6	%
ΔI_{PHA_M}	Output current matching PHA pump	$V_{DDA} = 3V$, $I_{RA} = 25µA$			±50	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5µA$			±65	
Charge pump PHP, normal mode [NO TAG, 4, 6] $V_{RF} = V_{DDA}$						
$\|I_{PHP\_N}\|$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2$ [13]	440	550	660	µA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	175	220	265	
$\frac{\Delta I_{PHP\_N}}{I_{PHP\_N}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$ [2, 13]		2	6	%
$\Delta I_{PHP\_N\_M}$	Output current matching PHP normal mode	$V_{DDA} = 3V$, $I_{RA} = 25µA$			±50	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5µA$			±65	
Charge pump PHP, speed-up mode [NO TAG, 4, 7] $V_{RF} = V_{DDA}$						
$\|I_{PHP\_S}\|$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2$ [13]	2.20	2.75	3.30	mA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	0.85	1.1	1.35	
$\frac{\Delta I_{PHP\_S}}{I_{PHP\_S}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$ [2, 13]		2	6	%
$\Delta I_{PHP\_S\_M}$	Output current matching PHP speed-up mode	$V_{DDA} = 3V$, $I_{RA} = 25µA$			±250	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5µA$			±300	
Charge pump PHI, speed-up mode [NO TAG, 4, 8] $V_{RF} = V_{DDA}$						
$\|I_{PHI}\|$	Output current PHI	$I_{RN} = -62.5µA$; $V_{PHI} = V_{DDA}/2$ [13]	4.4	5.5	6.6	mA
		$I_{RN} = -25µA$; $V_{PHI} = V_{DDA}/2$	1.75	2.2	2.65	
$\frac{\Delta I_{PHI}}{I_{PHI}}$	Relative output current variation PHI	$I_{RN} = -62.5µA$ [2, 13]		2	8	%
ΔI_{PHI_M}	Output current matching PHI pump	$V_{DDA} = 3V$, $I_{RA} = 25µA$			±500	µA
		$V_{DDA} = 5V$, $I_{RA} = 62.5µA$			±600	
Fractional compensation PHP, normal mode [NO TAG, 9] $V_{RN} = V_{DDA}$, $V_{PHP} = V_{DDA}/2$						
$I_{PHP\_F\_N}$	Fractional compensation output current PHP vs F_{RD} [3]	$I_{RF} = -62.5µA$; $F_{RD} = 1$ to 7 [13]	–625	–400	–250	nA
		$I_{RF} = -25µA$; $F_{RD} = 1$ to 7	–300	–180	–50	

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Fractional compensation PHP, speed up mode [NO TAG, 10] **$V_{PHP} = V_{DDA}$, $V_{RN} = V_{DDA}$**						
$I_{PHP\_F\_S}$	Fractional compensation output current PHP vs F_{RD}[3]	I_{RF} = –62.5µA;F_{RD} = 1 to 7[13]	–3.35	–2	–1.1	µA
		I_{RF} = –25µA;F_{RD} = 1 to 7	–1.35	–1.0	–0.5	
	Pump leakage		–20		20	nA
Charge pump leakage currents, charge pump not active						
I_{PHP_L}	Output leakage current PHP; normal mode[NO TAG]	V_{PHP} = 0.7 to V_{DDA} – 0.8		0.1	20	nA
I_{PHI_L}	Output leakage current PHI; normal mode[NO TAG]	V_{PHI} = 0.7 to V_{DDA} – 0.8		0.1	20	nA
I_{PHA_L}	Output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} – 0.8		0.1	20	nA

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP}$ = 3V; T_A = 25°C; unless otherwise specified. Test Circuit, Figure 4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Main divider guaranteed and tested on an automatic tester. Some performance parameters may be improved by using optimized layout.						
f_{RF_IN}	Input signal frequency	Pin = -20dBm, Direct coupled input[14]	0		1.8	GHz
		Pin = -20dBm, 1000pF input coupling			1.8	
V_{RF_IN}	Input sensitivity	f_{IN} = 1800MHz	–20		0	dBm
Reference divider ($V_{DD} = V_{DDA}$ = 3V or V_{DD} = 3V / V_{DDA} = 5V)						
f_{REF_IN}	Input signal frequency	2.7 < V_{DD} and V_{DDA} < 5.5V			25	MHz
		2.7 < V_{DD} and V_{DDA} < 4.5V			30	
V_{REF_IN}	Input signal range, AC coupled	2.7 < V_{DD} and V_{DDA} < 5.5V	500			mV_{P-P}
		2.7 < V_{DD} and V_{DDA} < 4.5V	300			
Z_{REF_IN}	Reference divider input impedance[15]			100		kΩ
				3		pF
Auxiliary divider						
f_{AUX_IN}	Input signal frequency PA="0", prescaler enabled		0		50	MHz
		4.5V ≤ V_{DDA} ≤ 5.5V	0		150	
		4.0V ≤ V_{DDA} ≤ 5.5V; Pin ≥ –12dBm	0		180	
	Input signal frequency PA="1", prescaler enabled		0		30	
		4.5V ≤ V_{DDA} ≤ 5.5V	0		40	
V_{AUX_IN}	Input signal range, AC coupled		200			mV_{P-P}
Z_{AUX_IN}	Auxiliary divider input impedance[15]			100		kΩ
				3		pF
Serial interface[15]						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time; CLOCK to DATA		30			ns
t_W	Pulse width; CLOCK		30			ns
	Pulse width; STROBE	B, C, D, E words	30			
In-Loop Performance[16] **V_{DDA} = 5V, V_{DD} = 2.7V**						
RF_{MM}	Main loop residual FM	F_{VCO} = 1780MHz		600	900	Hz

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
t_{SW}	Pulse width; STROBE	A word, PR = '01'	$\frac{1}{f_{VCO}} \cdot (NM2 \cdot 65) + t_W$			ns
		A word, PR = '10'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM3 + 1) \cdot 68] + t_W$			
		A word, PR = '11'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65 + (NM3 + 1) \cdot 68 + (NM4 + 1) \cdot 73)] + t_W$			
		A word, PR = '00'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM4 + 1) \cdot 73] + t_W$			

NOTES:

1. When a serial input "A" word is programmed, the main charge pumps on PHP and PHI are in the "speed up mode" as long as STROBE = H. When this is not the case, the main charge pumps are in the "normal mode".
2. The relative output current variation is defined thus:
$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|} \text{ with } V_1 = 0.7V, V_2 = V_{DDA} - 0.8V \text{ (see Figure 3).}$$
3. F_{RD} is the value of the 3 bit fractional accumulator.
4. Monotonicity is guaranteed with C_N = 0 to 255.
5. Power supply current measured with f_{RF_IN} = 1667.4MHz, NM1 = 0, NM2 = 1, NM3 = 1, NM4 = 4, FMOD = 8, N = 694 6/8, main phase detector frequency = 2.4MHz, $f_{REF\ IN}$ = 19.2MHz, NR = 8, SM = 1, f_{AUX_IN} = 150MHz, NA = 125, SA = 1, PA = 0, auxiliary phase detector frequency = 300kHz, IRN = IRA = IRF = 25µA, CN = 160, CL = 0, CK = 0, lock condition, normal mode, $V_{CCP} = V_{DD} = V_{DDA}$ = 3V. Operational supply current = $I_{DDA} + I_{DD} + I_{CCP}$.
6. Specification condition: CN = 255
7. Specification conditions:
   1) CN = 255; CL = 1, or
   2) CN = 75; CL = 3
8. Typical output current $|I_{PHI}| = -I_{RN} \times CN \times 2^{(CL+1)} \times CK/32$:
   1) CN = 160; CL = 3; CK = 1, or
   2) CN = 160; CL = 2; CK = 2, or
   3) CN = 160; CL = 1; CK = 4, or
   4) CN = 160; CL = 0; CK = 8
9. Any RFD, CL = 1 for speed-up pump. The integral pump is intended for switching only and the fractional compensation is not guaranteed.
10. Specification conditions: F_{RD} = 1 to 7; CL = 1.
11. Specification conditions:
    1) F_{RD} = 1 to 7; CL = 1; CK = 2, or
    2) F_{RD} = 1 to 7; CL = 2; CK = 1.
12. The matching is defined by the sum of the P and the N pump for a given output voltage.
13. Limited analog supply voltage range 4.5 to 5.5V.
14. For f_{IN} < 50MHz, low frequency operation requires DC-coupling and a minimum input slew rate of 32V/µs.
15. Guaranteed by design.
16. F_{XTAL} = 14.4MHz, V_{XTAL} = 500mV_{P-P}, comparison Freq. = 200kHz, Loop bandwidth = 5kHz, Audio filter = 300Hz to 15kHz.

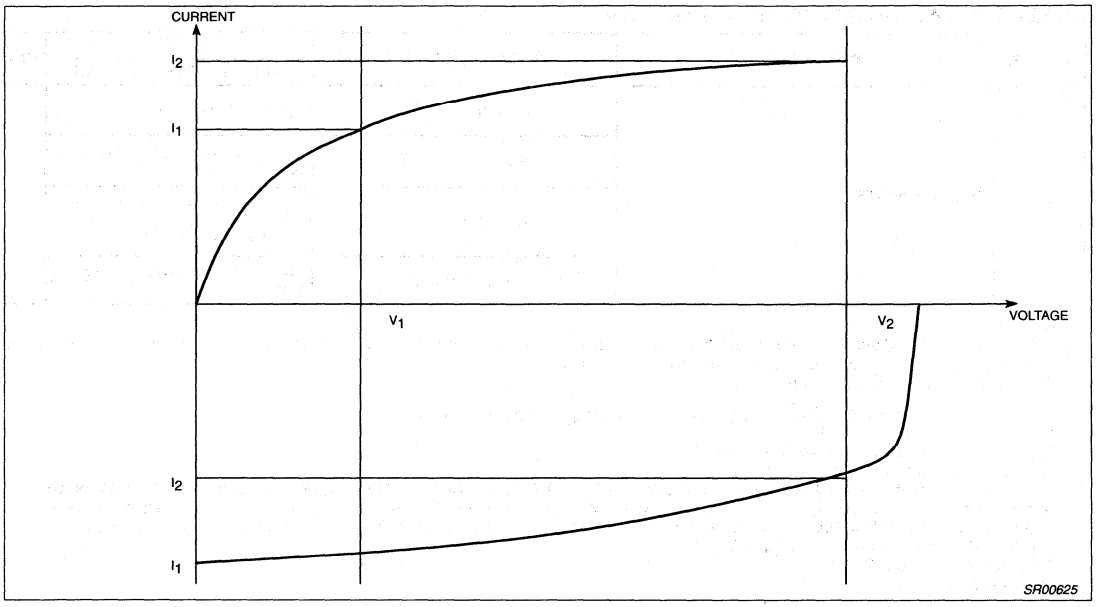


Figure 3. Relative Output Current Variation

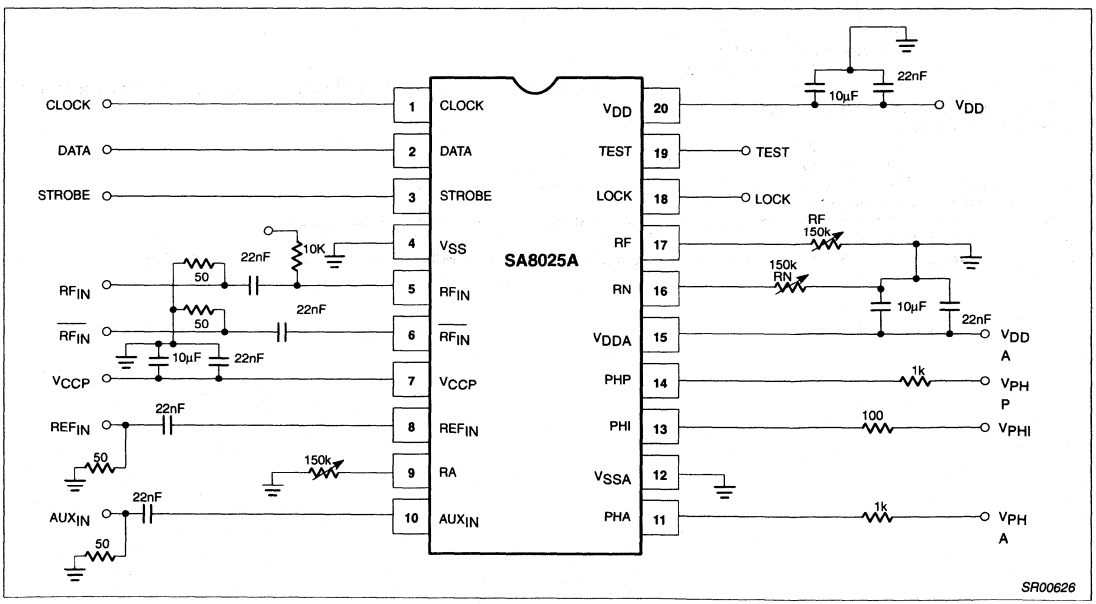


Figure 4. Test Circuit

AC TIMING CHARACTERISTICS

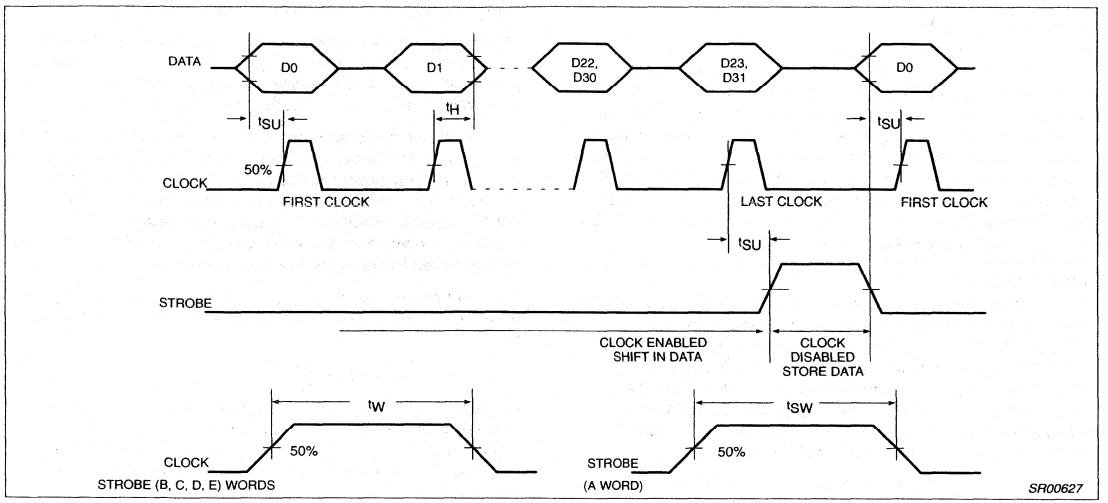


Figure 5. Serial Input Timing Sequence

FUNCTIONAL DESCRIPTION

Serial Input Programming

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32 bit words; each word includes 1 or 4 address bits. Figure 5 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent: D, C, B and A. Figure 6 and Table 1 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for CN and PR is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24 bit A0 word is used. CN will be directly loaded by programming a long 32 bit A1 word. The flag LONG in the D word determines whether A0 (LONG = "0") or A1 (LONG = "1") format is applicable. The A word contains new data for the main divider.

Main Divider Synchronization

The A word is loaded only when a main divider synchronization signal is also active in order to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. The signal is active while the NM1 divider is counting down from the programmed value. The new A word will be loaded after the NM1 divider has reached its terminal count; also, at this time a main divider output pulse will be sent to the main phase detector. The loading of the A word is disabled while the other dividers are counting up to their programmed values.

Therefore, the new A word will be correctly loaded provided that the STROBE signal has been at an active high value for at least a minimum number of VCO input cycles at RF_{IN} or $\overline{RF_{IN}}$.

For PR = '01'

$$t\_strobe\_min = \frac{1}{f_{VCO}}(NM2 \cdot 65) + t_W$$

For PR = '10'

$$t\_strobe\_min = \frac{1}{f_{VCO}}[NM2 \cdot 65 + (NM3 + 1) \cdot 68] + t_W$$

For PR = '11'

$$t\_strobe\_min = \frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65 + (NM3 + 1) \; 68 + (NM4 + 1) \cdot 73)] + t_W$$

For PR = '00'

$$t\_strobe\_min = \frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM4 + 1) \cdot 73] + t_W$$

Programming the A word means also that the main charge pumps on output PHP and PHI are set into the speed-up mode as long as the STROBE is H.

Auxiliary Divider

The input signal on AUX_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled if the serial control bit EA = "1". Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = "0". This divider has been optimized to accept a high frequency input signal. If PA = "1", this divider is disabled and the input signal is fed directly to the second stage, which is a 12-bit programmable divider with standard input frequency (40MHz). The division ratio can be expressed as:

if PA = "0": N = 4 x NA

if PA = "1": N = NA; with NA = 4 to 4095

Reference Divider

The input signal on REF_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 4095) followed by a three bit binary counter. The 2 bit SM register (see Figure 7) determines which of the 4 output pulses is selected as the main phase detector input. The 2 bit SA register determines the selection of the auxiliary phase detector signal.

Main Divider

The differential inputs are amplified (to internal ECL logic levels) and provide excellent sensitivity (–20dBm at 1.7GHz) making the prescaler ideally suited to directly interface to a VCO as integrated on the Philips front-end devices including RF gain stage, VCO and mixer. The internal four modulus prescaler feedback loop FB controls the selection of the divide by ratios 64/65/68/73, and reduces the minimum system division ratio below the typical value required by standard dual modulus (64/65) devices.

This input stage is enabled when serial control bit EM = "1". Disabling means that all currents in the prescaler are switched off.

The main divider is built up by a 12 bit counter plus a sign bit. Depending on the serial input values NM1, NM2, NM3, NM4 and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles according to Table 2 and Table 3.

The loading of the work registers NM1, NM2, NM3, NM4 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as explained in the Serial Input Programming section.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = "1". Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider will then be

$$NQ = N + \frac{NF}{Q}$$

Programming a fraction means the prescaler with main divider will divide by N or N + 1. The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

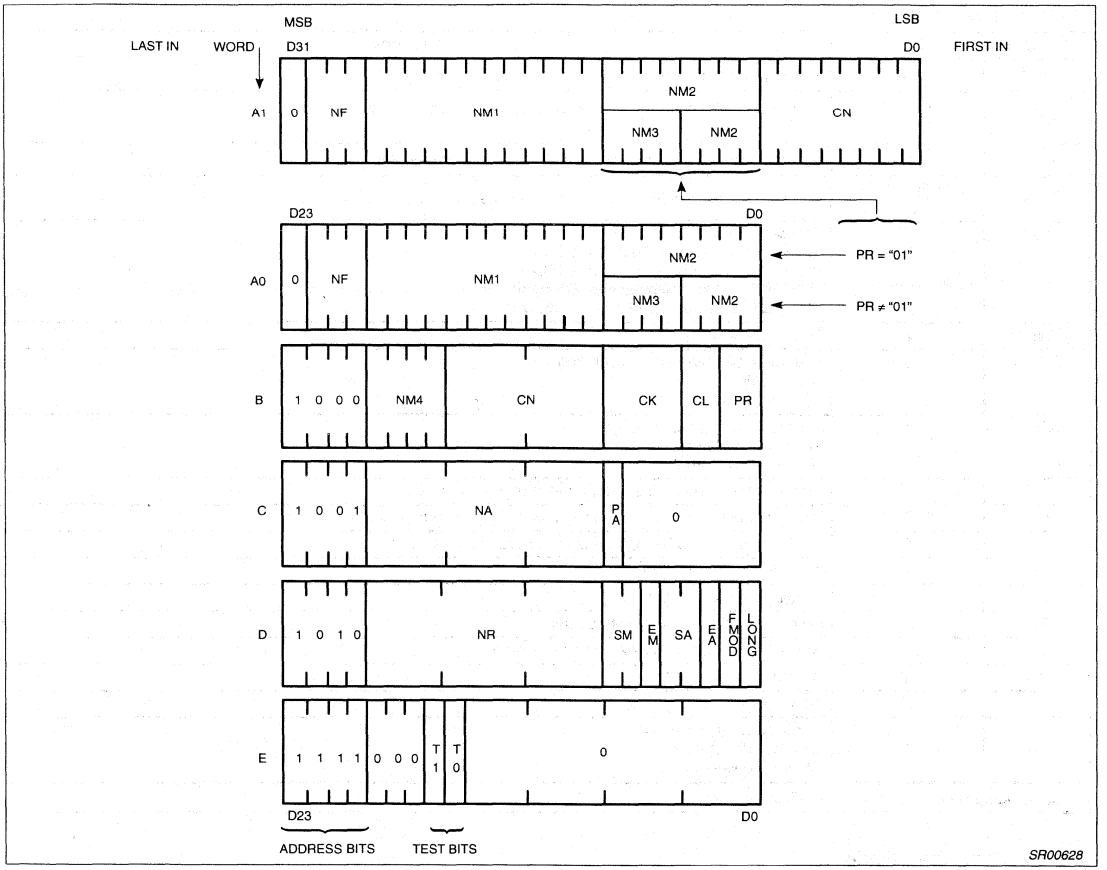


Figure 6. Serial Input Word Format

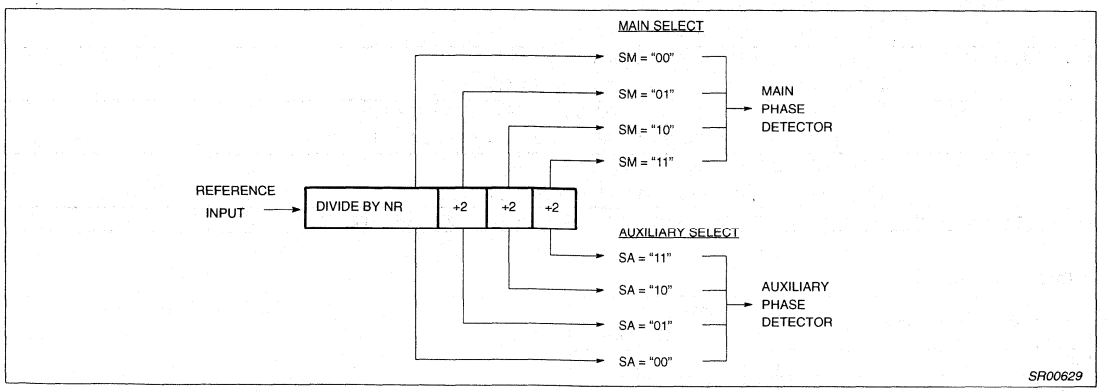


Figure 7. Reference Divider

Table 1. Function Table

Symbol	Bits	Function
NM1	12	Number of main divider cycles when prescaler modulus = 64*
NM2	8 if PR = "01" 4 if PR = "10"	Number of main divider cycles when prescaler modulus = 65*
NM3	4 if PR = "10"	Number of main divider cycles when prescaler modulus = 68*
NM4	4 if PR = "11" or "00"	Number of main divider cycles when prescaler modulus = 73*
PR	2	Prescaler type in use PR = "01": modulus 2 prescaler (64/65) PR = "10": modulus 3 prescaler (64/65/68) PR = "11": modulus 4 prescaler (64/65/68/73) PR = "00": modulus 3 prescaler (64/65/73)
NF	3	Fractional-N increment
FMOD	1	Fractional-N modulus selection flag "1": modulo 8 "0": modulo 5
LONG	1	A word format selection flag "0": 24 bit A0 format "1": 32 bit A1 format
CN	8	Binary current setting factor for main charge pumps
CL	2	Binary acceleration factor for proportional charge pump current
CK	4	Binary acceleration factor for integral charge pump current
EM	1	Main divider enable flag
EA	1	Auxiliary divider enable flag
SM	2	Reference select for main phase detector
SA	2	Reference select for auxiliary phase detector
NR	12	Reference divider ratio
NA	12	Auxiliary divider ratio
PA	1	Auxiliary prescaler mode: PA = "0": divide by 4 PA = "1": divide by 1
*Not including reset cycles and Fractional-N effects.		

Table 2. Prescaler Ratio

The total division ratio from prescaler to the phase detector may be expressed as:	
if PR = "01"	N = (NM1 + 2) x 64 + NM2 x 65
	N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 (*)
if PR = "10"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 68
	N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 68 (*)
if PR = "11"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 68 + (NM4 + 1) x 73
	N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 68 + (NM4 + 1) x 73 (*)
if PR = "00"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM4 + 1) x 73
	N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM4 + 1) x 73 (*)
(*) When the fractional accumulator overflows the prescaler ratio = 65 (64 + 1) and the total division ratio N' = N + 1	

Table 3. PR Modulus

PR	Modulus Prescaler	Bit Capacity			
		NM1	NM2	NM3	NM4
01	2	12	8	–	–
10	3	12	4	4	–
11	4	12	4	4	4
00	3	12	8	–	4

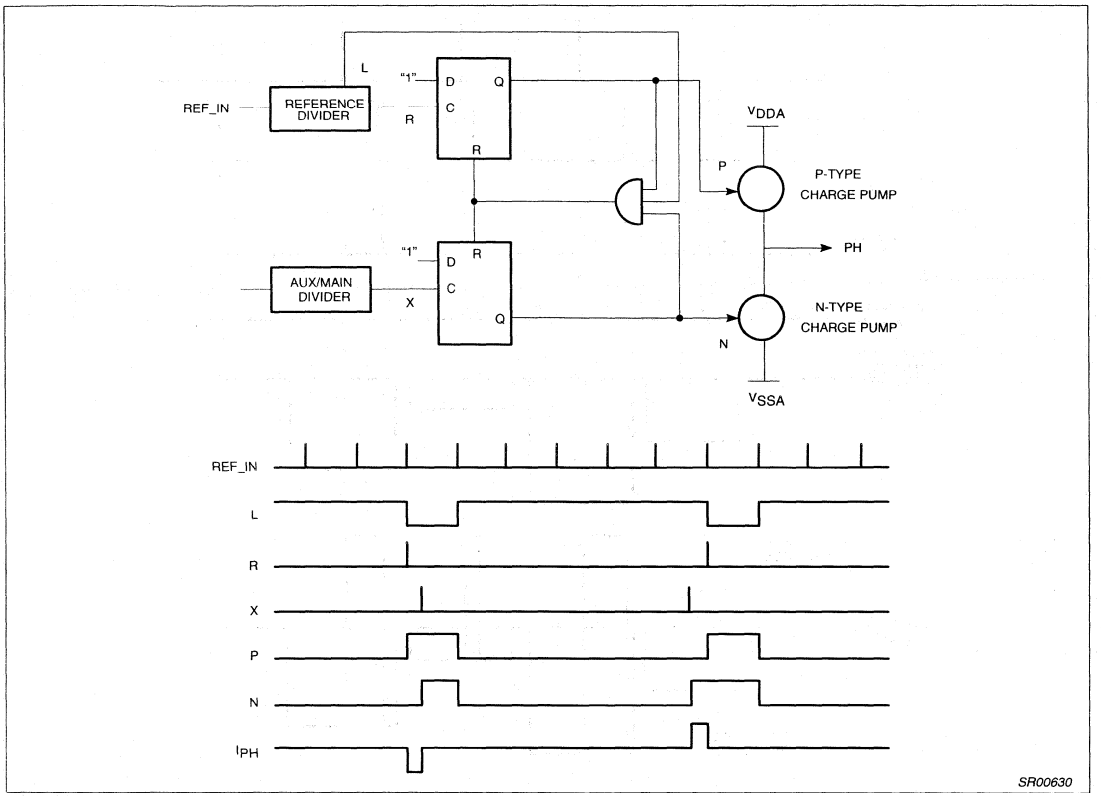


Figure 8. Phase Detector Structure with Timing

Phase Detectors

The auxiliary and main phase detectors are a two D-type flip-flop phase and frequency detector shown in Figure 8. The flip-flops are set by the negative edges of output signals of the dividers. The rising edge of the signal, L, will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

Current Settings

The SA8025A has 3 current setting pins: RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current connected between the current setting pin and V_{SS}. The typical value R (current setting resistor) can be calculated with the formula:

$$R = \frac{V_{DDA} - 0.9 - 150\sqrt{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary Output Charge Pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor RA at pin RA. The active charge pump current is typically:

$$|I_{PHA}| = 8 \cdot I_{RA}$$

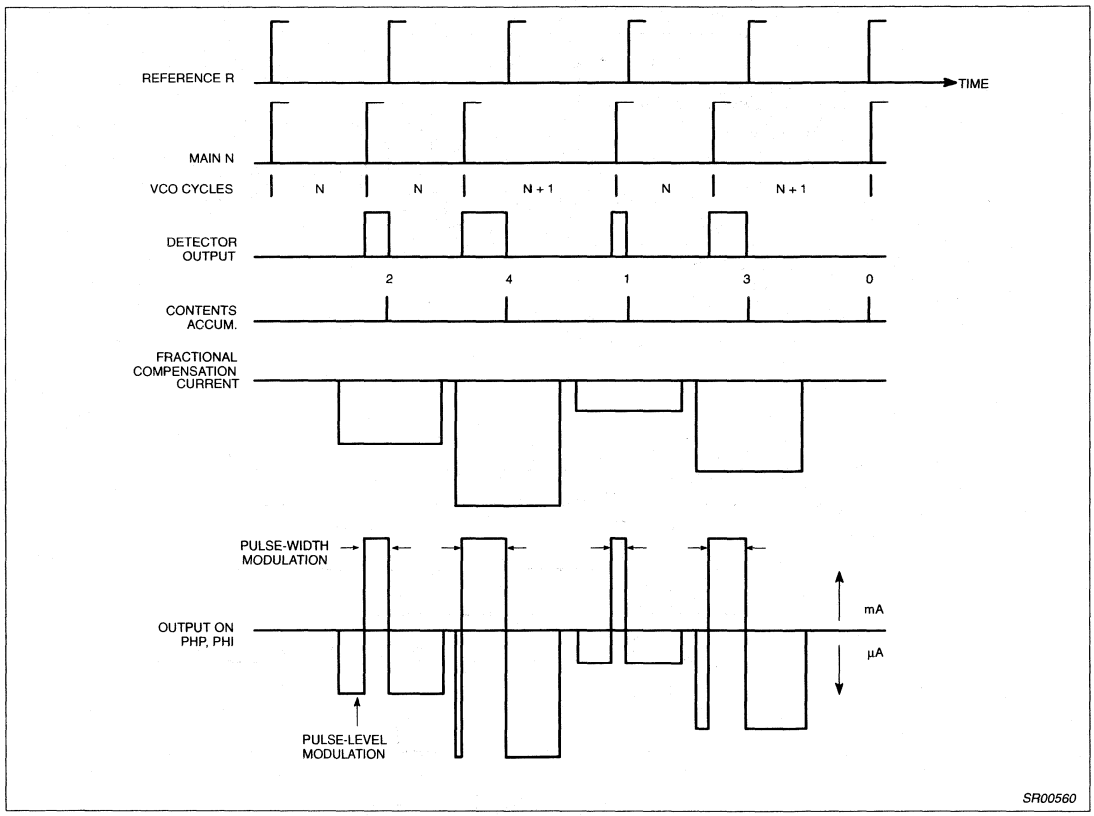


Figure 9. Waveforms for NF = 2, Fraction = 0.4

Main Output Charge Pumps and Fractional Compensation Currents

The main charge pumps on pin PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 9 shows the waveforms for a typical case.

When the serial input A word is loaded, the output circuits are in the "speed-up mode" as long as the STROBE is H, else the "normal mode" is active. In the "normal mode" the current output PHP is:

$$I_{PHP\_N} = I_{PHP} + I_{PHP\_comp}$$

where:

$$|I_{PHP}| = \frac{CN \cdot I_{RN}}{32} \quad \text{:charge pump current}$$

$$|I_{PHP\_comp}| = FRD \cdot \frac{I_{RF}}{128} \quad \text{:fractional comp. current}$$

The current in PHI is zero in "normal mode".

In "speed-up mode" the current in output PHP is:

$$I_{PHP\_S} = I_{PHP} + I_{PHP\_comp}$$

$$|I_{PHP}| = \left(\frac{CN \cdot I_{RN}}{32}\right)(2^{CL+1} + 1)$$

$$|I_{PHP\_comp}| = \left(\frac{FRD \cdot I_{RF}}{128}\right)(2^{CL+1} + 1)$$

In "speed-up mode" the current in output PHI is:

$$I_{PHI\_S} = I_{PHI} + I_{PHI\_comp}$$

where:

$$|I_{PHI}| = \left(\frac{CN \cdot I_{RN}}{32}\right)(2^{CL+1})\ CK$$

$$|I_{PHI\_comp}| = \left(\frac{FRD \cdot I_{RN}}{128}\right)(2^{CL+1})\ CK$$

Figure 9 shows that for proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output. This means that the current setting on the input RN, RF is approximately:

$$\frac{I_{RN}}{I_{RF}} \approx \frac{(Q \cdot f_{VCO})}{(3 \cdot CN \cdot F_{INR})}$$

where:

Q = fractional-N modulus
$f_{VCO} = f_{INM} \times N$, input frequency of the prescaler
F_{INR} = input frequency of the reference divider

PHI pump is meant for switching only. Current and compensation are not as accurate as PHP.

Lock Detect

The output LOCK is H when the auxiliary phase detector AND the main phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than +1 cycle on the reference input REF_IN. The lock condition is also fulfilled when the relative counter is disabled (EM = "0" or respectively EA = "0") for the main, respectively auxiliary counter.

Test Modes

The lock output is selectable as f_{REF}, f_{AUX}, f_{MAIN} and lock. Bits T1 and T0 of the E word control the selection (see Figures 6 and 10).

If T1 = T0 = Low, or if the E-word is not sent, the lock output is configured as the normal lock output described in the Lock Detect section.

If T1 = Low and T0 = High, the lock output is configured as f_{REF}. The signal is the buffered output of the reference divider NR and the 3-bit binary counter SM. The f_{REF} signal appears as normally low and pulses high whenever the divider reaches terminal count from the value programmed into the NR and SM registers. The f_{REF} signal can be used to verify the divide ratio of the Reference divider.

If T1 = High and T0 = Low, the lock output is configured as f_{AUX}. The signal is normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NA and PA registers. The f_{AUX} signal can be used to verify the divide ratio of the Auxiliary divider.

If T1 = High and T0 = High, the lock output is configured as f_{MAIN}. The signal is the buffered output of the MAIN divider. The f_{MAIN} signal appears as normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NM1, NM2, NM3 or NM4 registers. The f_{MAIN} signal can be used to verify the divide ratio of the MAIN divider and the prescaler.

Test Pin

The Test pin, Pin 19, is a buffered logic input which is exclusively ORed with the output of the prescaler. The output of the XOR gate is the input to the MAIN divider. The Test pin must be connected to V_{DD} during normal operation as a synthesizer. This pin can be used as an input for verifying the divide ratio of the MAIN divider; while in this condition the input to the prescaler, RF_{IN}, may be connected to V_{CCP} through a 10kΩ resistor in order to place prescaler output into a known state.

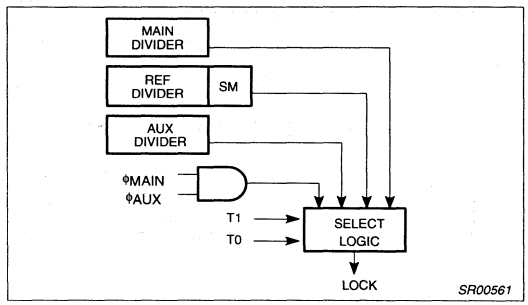
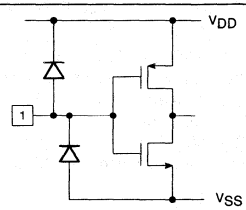
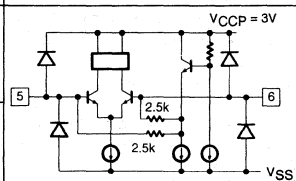
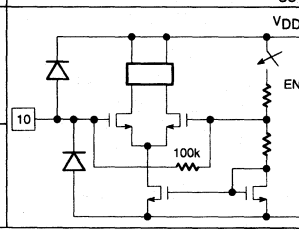


Figure 10. Test Mode Diagram

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	CLOCK	—	
2	DATA	—	
3	STROBE	—	
19	TEST	—	
5	RF_{IN}	2.1	
6	$\overline{RF_{IN}}$	2.1	
8	REF_{IN}	1.8	
10	AUX_{IN}	1.8	

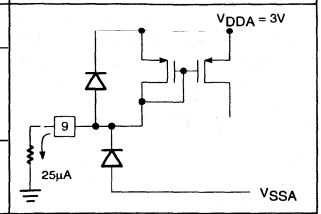
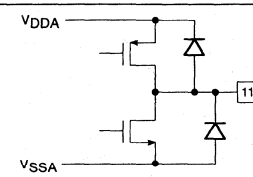
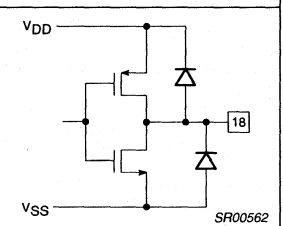
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
9	RA	1.35	
16	RN	1.35	
17	RF	1.35	
11	PHA	—	
13	PHI	—	
14	PHP	—	
18	LOCK	—	

Figure 11. Pin Functions

TYPICAL PERFORMANCE CHARACTERISTICS

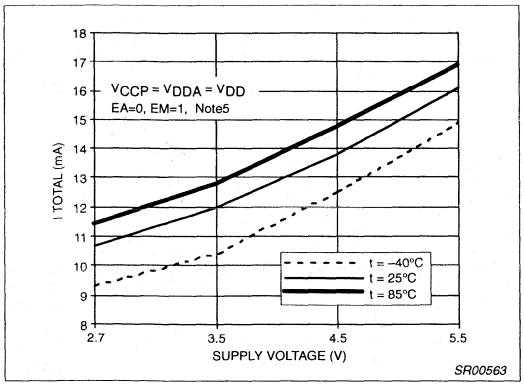


Figure 12. Operational Supply Current vs Supply Voltage and Temperature

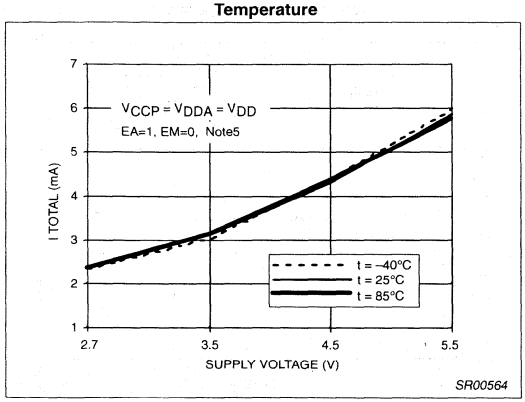


Figure 13. Auxiliary Operational Supply Current vs Supply Voltage and Temperature

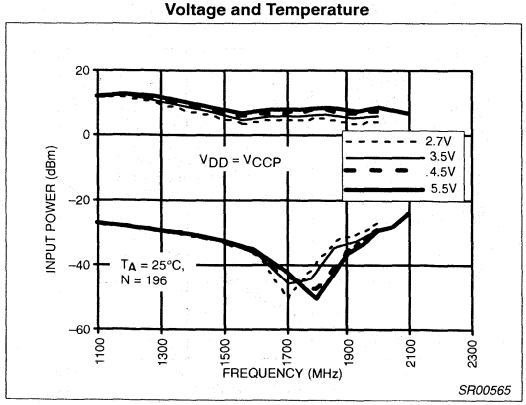


Figure 14. Main Divider Input Power vs Frequency and Supply

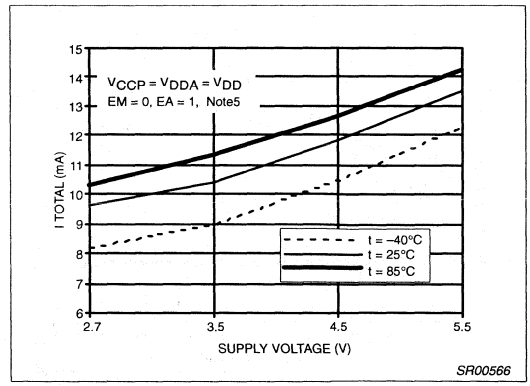


Figure 15. Main Operational Supply Current vs Supply Voltage and Temperature

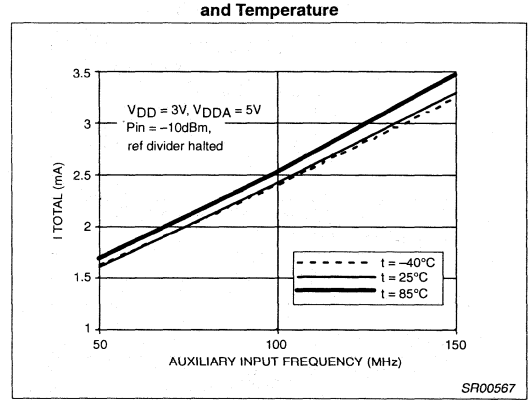


Figure 16. Auxiliary Operational Supply Current vs Frequency and Temperature

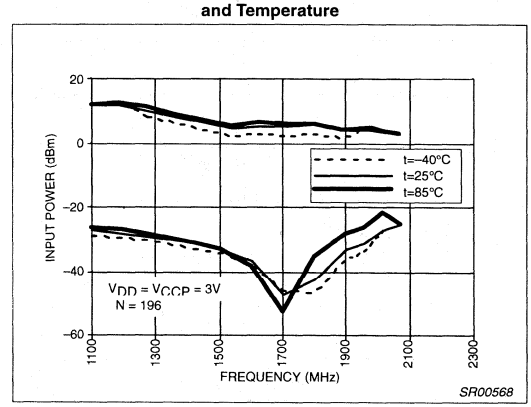


Figure 17. Main Divider Input Power vs Frequency and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

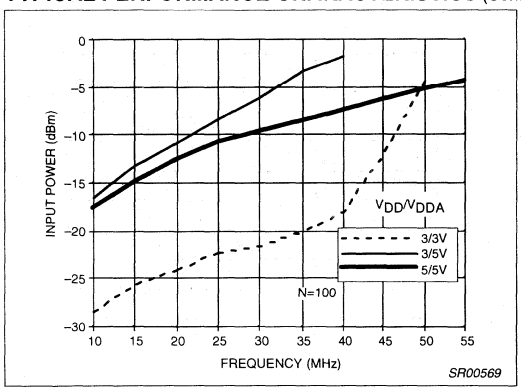


Figure 18. Reference Divider Minimum Input Power vs Frequency and Supply

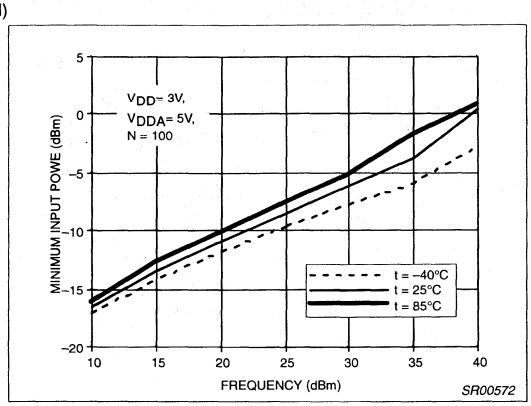


Figure 21. Reference Divider Minimum Input Power vs Frequency and Temperature

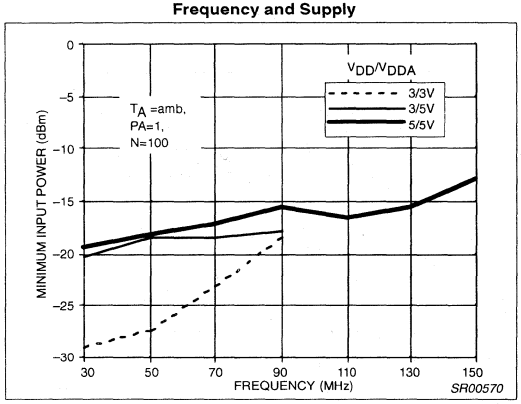


Figure 19. Auxiliary Divider Minimum Input Power vs Frequency and Supply

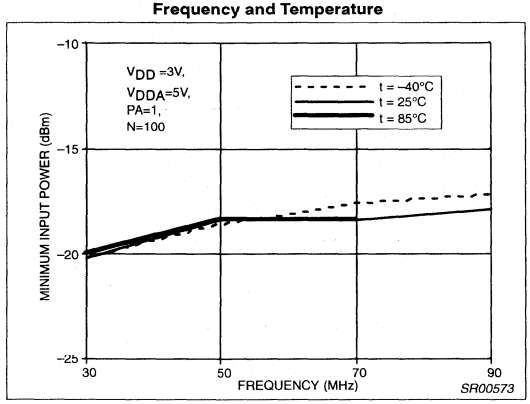


Figure 22. Auxiliary Divider Minimum Input Power vs Frequency and Temperature

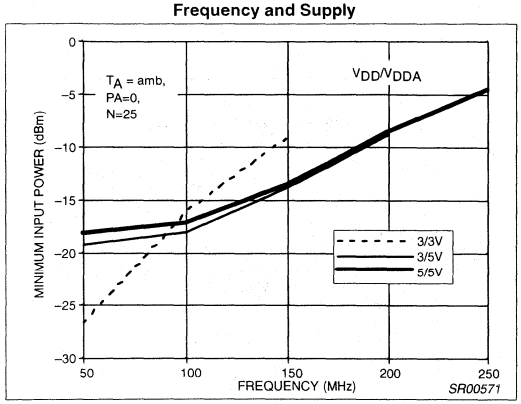


Figure 20. Auxiliary Divider Minimum Input Power vs Frequency and Supply

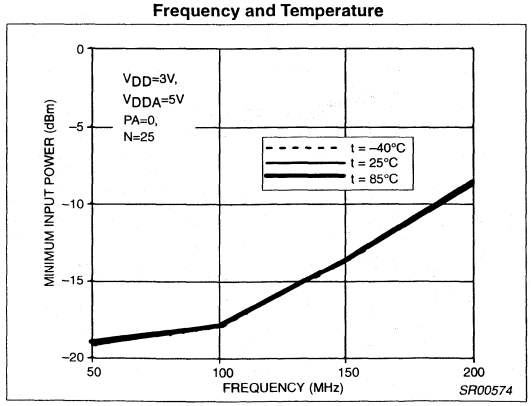


Figure 23. Auxiliary Divider Minumum Input Power vs Frequency and Temperature

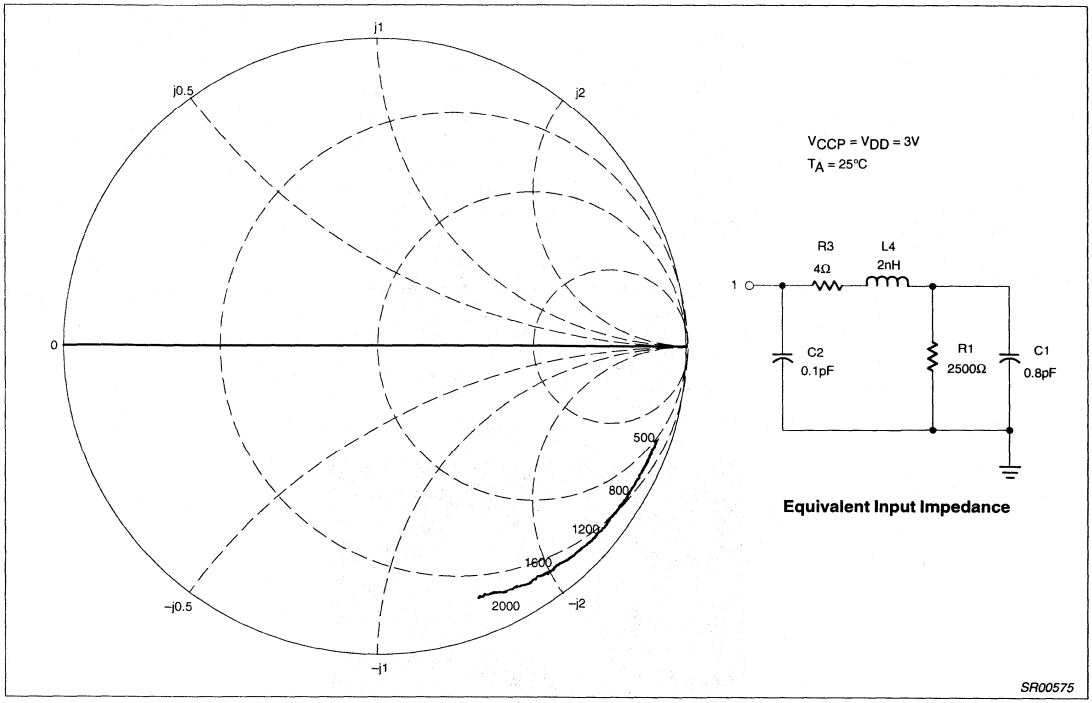
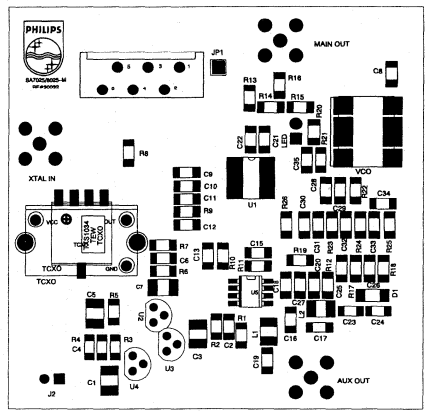
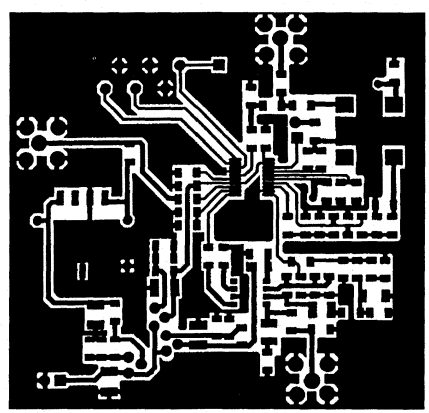


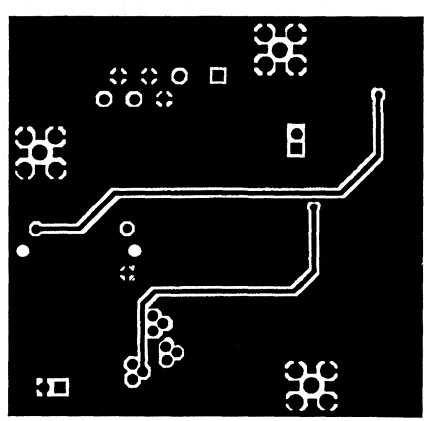
Figure 24. Typical RF_{IN} Input Impedance



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

SR00576

Figure 25. SA8025ADK Demoboard Layout (NOT ACTUAL SIZE)

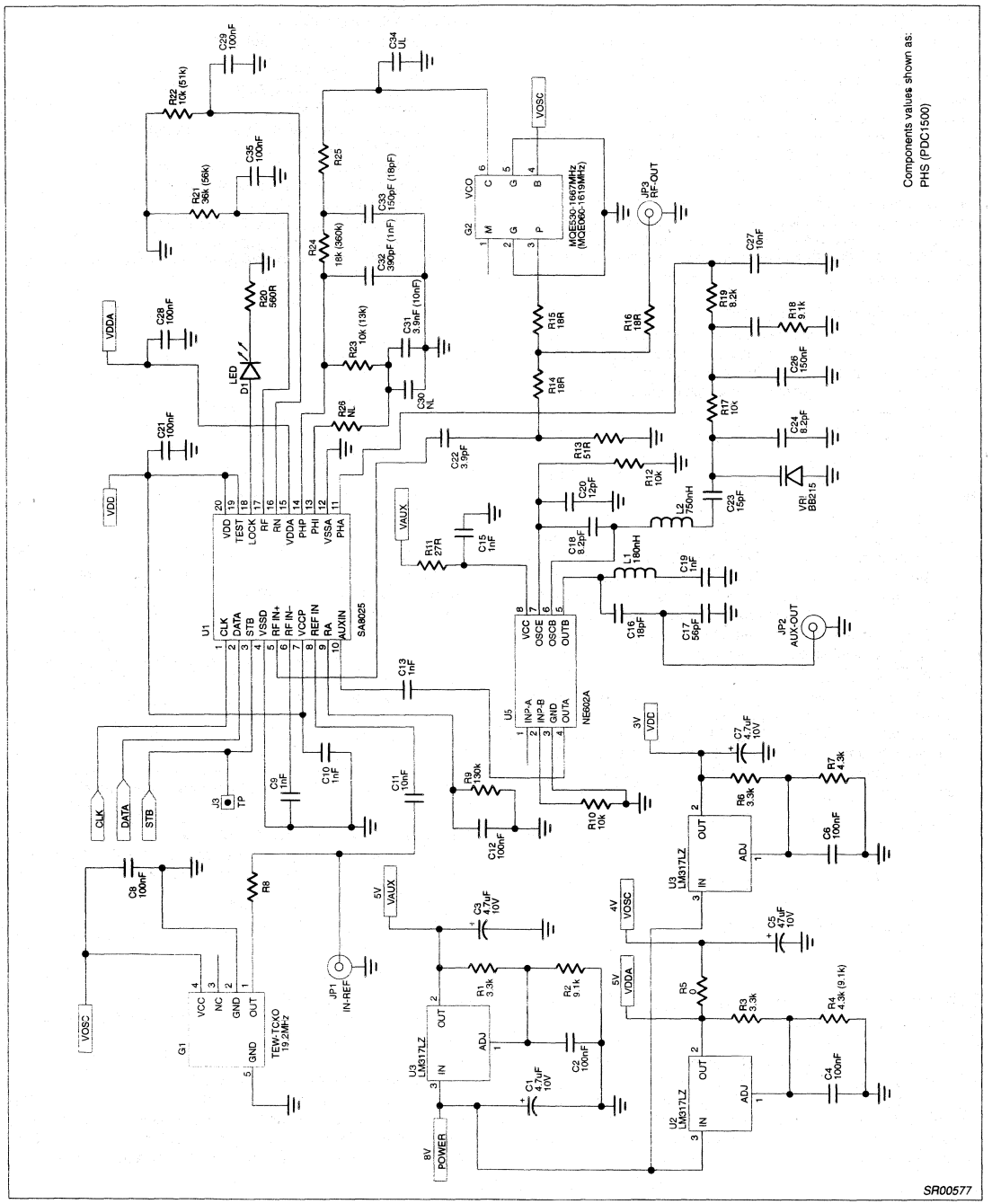


Figure 26. SA8025ADK Application Circuit

Using the SA7025(RevA) and SA8025A for narrow band systems AN1890

Author: Wing S. Djen

INTRODUCTION

The SA7025 (RevA) and SA8025A are improved versions of the SA7025 and SA8025 suitable for narrow band systems like the America Digital Cellular System (IS-54) and Japan Personal Digital Cellular System (PDC). The new design improves the performance of the fractional spurs compensation, which is a by-product of the fractional-N divider. Complete design procedure and performance measurements on both the SA7025 (RevA) and SA8025A are included in this document.

The basics of the fractional-N PLL frequency synthesizers can be found in Philips Semiconductors application note AN1891, "SA8025 Fractional-N synthesizer for 2GHz band applications". AN1891 can be used in conjunction with this document for designing-in the SA7025, SA8025, SA7025 (RevA), and SA8025A.

Fractional Spurs Compensation

The fractional-N divide ratio is achieved by changing the divide ratio between N and N+1. In lock condition, this technique will introduce an instantaneous phase error in the phase detector. This causes the VCO to generate unwanted spurs at the offset of the fractions of the comparison frequency.

On the new SA7025 (RevA) and SA8025A, the fractional compensation circuitry was re-designed to achieve better performance. Three improvements can be found on the SA7025 (RevA) and SA8025A due to this modification:

1. The CN range is much tighter. The CN values are the binary current setting factor for the charge pumps. These values may be varied across the desired frequency band (e.g. 25MHz) for fractional spurs compensation. For the SA7025/SA8025, the CN range is greater than 50 for narrow band systems (e.g. channel spacing, f_{CH}=30kHz). For the new SA7025 (RevA)/SA8025A, this range is much tighter and a **fixed** CN value is usually good enough for all synthesized frequencies on the SA7025 (RevA)/SA8025A.
2. A more accurate calculation of the resistor RF, which determines the amount of fractional compensation current. Eq. 1 gives an approximate value of I_{RF}. RF can be calculated using Eq. 2, which is the same as the one for calculating resistor RN. To obtain an optimum performance, the CN value can be adjusted accordingly.

$$I_{RF} = \frac{3 \cdot I_{RN} \cdot CN \cdot f_{XTAL}}{Q \cdot f_{VCO}} \quad (1)$$

$$RF = \frac{V_{DDA} - 0.9 - 150 \cdot \sqrt{I_{RF}}}{I_{RF}} \quad (2)$$

3. Better performance over temperature. The variation of fractional spurs was minimized over the rated temperature range (-40 to +80°C).

Compatibility Between the SA7025/SA8025 and SA7025 (RevA)/SA8025A

The SA7025/SA8025 and SA7025 (RevA)/SA8025A are pin-to-pin compatible and have exactly the same performance except for the fractional compensation section. When replacing the SA7025/SA8025 with SA7025 (RevA)/SA8025A, new values for CN and resistor RF may have to be used. Users should calculate resistor RF using Eq. 1 and 2 and experiment with it on the bench with the new RF value.

PLL Design Equations

δ : final frequency resolution after settling.

$$\delta = \frac{\text{frequency error after settling}}{\text{switching step}} \quad (3)$$

t_{SW} : switching time (sec)
f_N : natural frequency of the 2nd order system(Hz) , $\omega_N = 2\pi f_N$ (rad/s)
N : total divide ratio
ξ: : damping factor of the 2nd order system. Typical value is 0.707.
K_{VCO}: VCO gain (Hz/V) or 2π * VCO gain (rad/V)
K_ϕ : phase detector gain = $I_{CP}/2\pi$ (A/rad)

$$\omega_N = \frac{-\ln(\delta \cdot \sqrt{1 - \xi^2})}{\xi \cdot t_{SW}} \quad (4)$$

$$C_1 = \frac{K_\phi \cdot K_{VCO}}{N\omega_N^2} \quad (5)$$

$$R_1 = 2 \cdot \xi \left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C_1}\right)^{0.5} \quad (6)$$

$$C_2 \le \frac{C_1}{10} \quad (7)$$

$$\omega = \frac{1}{C_3 \cdot R_2} \quad \omega \text{ should be at least 10 times larger than } \omega_N \quad (8)$$

Note: The unit of the factor $K_\phi \cdot K_{VCO}$ is unity when all the variables are expressed in radians. Therefore, designers can simply multiply the charge pump output current (I_{CP}) with the VCO gain in Hz/V to obtain this factor.

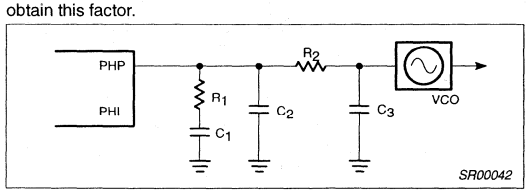


Figure 1. 3-Poles RC Lowpass Loop Filter

SA7025 (RevA) Design Example

This section shows a design example using the SA7025 (RevA) for the IS-54. The system parameters are as follows:

VCO frequency (f_{VCO}) = 913 to 938MHz
Channel spacing (f_{CH}) = 30kHz
Comparison frequency (f_{COMP}) = 8 * 30 kHz = 240kHz
Switching time (t_{SW}) = 1.5ms
Switching step = 25MHz
Frequency error = within 1 kHz
VCO gain (K_{VCO}) = 12MHz/V (measured), Murata MQE001-926
Reference Crystal (f_{REF}) = 14.4MHz

1. Determine total divide ratio N

To synthesize channels from 913 to 938MHz with f_{COMP}=240kHz, N should be between 3804 and 3908. For the same loop components, a larger value of N yields lower natural frequency (f_N). So, jumping from high-end to low-end (larger N) is slower than from low-end to

high-end (smaller N). To ensure the same switching time from both directions, we use N=3908 for the worst case.

2. Determine ω_N

Using Eq. 3 $$\delta = \frac{1000}{25e6} = 0.04e\text{-}3$$

Pick $\xi = 0.707$ and use $t_{SW} = 1.5$ms.

Using Eq. 4 $$\omega_N = \frac{-\ln(0.04e\text{-}3 \cdot 0.707)}{0.707 \cdot 1500e\text{-}6} = 9830$$

3. Determine RN and I_{CP}

Pick RN = 51 kΩ and CN = 200. I_{RN} becomes 58μA when V_{DDA}=5V.

Using the PHP charge pump current equation

$$I_{CP} = 200\left(\frac{58e\text{-}6}{32}\right) = 363\mu A$$

4. Determine R_1, C_1, and C_2

Using Eq. 5 with the 2π's from K_{VCO} (rad/V) and K_ϕ (A/rad) cancel out

$$C_1 = 12e6\left(\frac{363e\text{-}6}{3908 \cdot 9830^2}\right) = 11.5nF$$

Using Eq. 6

$$R_1 = 2 \cdot 0.707 \cdot \left(\frac{3908}{12e6 \cdot 363e\text{-}6 \cdot 11.5e\text{-}9}\right)^{0.5} = 13k\Omega$$

Using Eq. 7 $$C_2 = \frac{11.5e\text{-}9}{10} = 1.15nF$$

5. Determine R_2 and C_3

R_2 and C_3 can help attenuate the comparison spurs at 240kHz offset.

Using Eq. 8 $$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_N$$

6. Determine RF

Crystal frequency (f_{XTAL}) = 14.4MHz
Mid VCO frequency (f_{VCO}) = 926MHz
Q (fractional modulus) = 8
Using Eq. 1 and Eq. 2

$$I_{RF} = \frac{3 \cdot 58e\text{-}6 \cdot 200 \cdot 14.4e6}{8 \cdot 926e6} = 67.65\mu A$$

$$RF = \frac{5 - 0.9 - 150 \cdot \sqrt{67.65e\text{-}6}}{8 \cdot 926e6} = 43k\Omega$$

A minor adjustment of CN maybe required if optimum fractional spurs suppression is needed across the 25MHz band. The experimental results yielded the best spurious suppression at a value of RF=47kΩ.

Component values used on the SA7025(Rev A) demo board:
C31 = 10 nF
R23 = 13 kΩ
C32 = 1 nF
R24 = 100 kΩ
C33 = 18 pF
R21 = 47 kΩ (RF)
R22 = 51 kΩ (RN)
CN = 200
Strobe width = 260μs

Measurement Results of the SA7025 (RevA)

Figure 2 shows the measured close-in noise at 940.05MHz. The phase noise at 1kHz carrier offset is -49.4 - 10 * log (100) = -69.4 dBc/Hz. Fractional spurs performance is shown in Figures 3 to 6. The worst case spurs occur when NF=1 and NF=7 are less than -60dBc. Spurs at the alternate channel, the 60kHz carrier offset required by the IS-54, are totally suppressed. Figures 7 and 8 show the measured switching times. These results show that the PLL can jump a 25MHz step in less than 1.5ms from both directions.

Table 2 shows the difference in performance between the SA7025 and SA7025 (RevA) using the same demoboard. Unless otherwise mentioned, CN=200, RN=51kΩ, RF=47kΩ.

Speed-up Design for Achieving Better Close-in Noise

Better close-in noise can be achieved at the expense of operational current. The PHP charge pumps on the SA7025 (RevA) and SA8025A are both capable of delivering more than 1.5mA in the speed-up mode. To stay in this mode, the STROBE signal has to be kept high after the programming word 'A' is sent. The CL register sets the amount of charge pump current which is either 3 times (CL=0), 5 times (CL=1), or 9 times (CL=2) higher than the current in normal mode. Assume that we want to modify the previous design and use speed-up with CL=1. This implies that the charge pump output current becomes 5*363μA = 1.8mA. In order to maintain the same natural frequency, the value of C31 and C32 is increased by a factor of 5 and R23 is decreased by the same factor of 5. Therefore, the new values used on the demo board are:

C31 = 100nF in parallel with 100nF
C32 = 4.7nF
R23 = 2.4kΩ

Figure 9 compares the close-in phase noise of the two designs with the same natural frequency. The bottom trace has a 4dB improvement in the close-in noise when speed-up mode (higher current) is used. Since the phase noise beyond the loop bandwidth is solely determined by the VCO phase noise, two traces start to merge together at about 5kHz offset.

SA8025A Design Example

This section shows a design example using the SA8025A for the Personal Digital System (PDC1500), a narrow band system. The design procedure is the same as the previous section. The system parameters are as follows:

VCO frequency (f_{VCO}) = 1607 to 1631 MHz
Channel spacing (f_{CH}) = 25kHz
Comparison frequency (f_{COMP}) = 8 * 25kHz = 200kHz
Switching time (t_{SW}) = 1.5ms
Switching step = 24MHz
Frequency error = within 1kHz
VCO gain (K_{VCO}) = 24 MHz/V (measured), Murata MQE060-1619
Reference Crystal (f_{REF}) = 19.2MHz

Table 2. Performance Comparison: SA7025 to SA7025 (Rev A)

	SA7025	SA7025 (Rev A)	Figure
Fractional spurs (dBc) @30kHz, VCO=912.99MHz	-57.6 (CN=200, RF=2MΩ)	-63.6	3
Fractional spurs (dBc) @60kHz, VCO=912.99MHz	not present (CN=200, RF=2MΩ)	not present	3
Fractional spurs (dBc) @30kHz, VCO=939.87MHz	-63.5 (CN=100, RF=2MΩ)	-63.9	5
Fractional spurs (dBc) @60kHz, VCO=939.87MHz	not present (CN=100, RF=2MΩ)	not present	5
Close-in noise (dBc/Hz) @1kHz, VCO=1631.025MHz	-69	-69	2
I_{TOTAL} (mA) for the demo board	21.2	21.2	
Switching time (ms)	<1.5	<1.5	7, 8

1. Determine total divide ratio N

$$N = \frac{1631MHz}{200kHz} = 8155$$

2. Determine ω_N

Using Eq. 3 $$\delta = \frac{1000}{24e6} = 0.042e\text{-}3$$

Pick $\xi = 0.707$ and use $t_{SW} = 1.5ms$.

Using Eq. 4 $$\omega_N = \frac{-\ln(0.042e\text{-}3 \cdot 0.707)}{0.707 \cdot 1500e\text{-}6} = 9830$$

3. Determine R_N and I_{CP}

Pick RN = 51kΩ and CN = 200. I_{RN} becomes 58μA when V_{DDA}=5V.

Using the PHP charge pump current equation

$$I_{CP} = 200\left(\frac{58e\text{-}6}{32}\right) = 363\mu A$$

4. Determine R_1, C_1, and C_2

Using Eq. 5

$$C_1 = 24e6\left(\frac{363e\text{-}6}{8155 \cdot 9830^2}\right) = 11.1nF$$

Using Eq. 6

$$R_1 = 2 \cdot 0.707 \cdot \sqrt{\left(\frac{8155}{24e6 \cdot 363e\text{-}6 \cdot 11.1e\text{-}9}\right)} = 13k\Omega$$

Using Eq. 7 $$C_2 = \frac{11.1e\text{-}9}{10} = 1.1nF$$

5. Determine R_2 and C_3

R_2 and C_3 can help attenuate the comparison spurs at 200kHz offset.

Using Eq. 8 $$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_N$$

Pick R_2 = 360kΩ, then C_3 = 18pF.

6. Determine RF

Crystal frequency (f_{XTAL}) = 19.2MHz
Mid VCO frequency (f_{VCO}) = 1619MHz
Q (fractional modulus) = 8
Using Eq. 1 and Eq. 2

$$I_{RF} = \frac{3 \cdot 58e\text{-}6 \cdot 200 \cdot 14.4e6}{8 \cdot 926e6} = 67.65\mu A$$

$$RF = \frac{5 - 0.9 - 150 \cdot \sqrt{67.65e\text{-}6}}{8 \cdot 926e6} = 43k\Omega$$

Minor adjustment of CN is required if optimum fractional spurs suppression is needed.

Component values used on the demo board:
C31 = 10nF
R23 = 13kΩ
C32 = 1nF
R24 = 360kΩ
C33 = 18pF
R21 = 56kΩ (RF)
R22 = 51kΩ (RN)
CN = 200
Strobe width = 260μs

Measurement Results of the SA8025A

Close-in phase noise spectrum is shown in the Figure 10. At 1kHz carrier offset, the phase noise is -45.3 - 10*log (100) = -65.3 dBc/Hz. The 3dB loop bandwidth is 3kHz, which is about twice as much as the loop natural frequency (f_N). Fractional spurs performance is shown in Figure 11 to 14. Worst case spurs when NF=1 and NF=7 for the low and high bands are all less than -59dBc. Spurs at 50kHz carrier offset, the alternate channel for PDC1500, were totally suppressed. Switching time measurements are shown in Figure 15 and 16. The PLL can reach the desired frequency for a 24MHz jump in less than 1.5ms from both directions.

Table 3 shows the difference in performance between the SA8025 and SA8025A using the same demoboard. Unless otherwise mentioned, CN=200, RN=51kΩ, RF=56kΩ.

Table 3. Performance Comparison: SA8025 to SA8025A

	SA8025	SA8025A	Figure
Fractional spurs (dBc) @25kHz, VCO=1606.625MHz	-41.5 (CN=250, RF=560kΩ)	-60.6	11
Fractional spurs (dBc) @50kHz, VCO=1606.625MHz	not present (CN=250, RF=560kΩ)	not present	11
Fractional spurs (dBc) @25kHz, VCO=1631.025MHz	-59.0 (CN=200, RF=560kΩ)	-59.5	13
Fractional spurs (dBc) @50kHz, VCO=1631.025MHz	not present (CN=200, RF=560kΩ)	not present	13
Close-in noise (dBc/Hz) @1kHz, VCO=1631.025MHz	-65	-65	10
I_{TOTAL} (mA) for the demo board	28.3	28.3	
Switching time (ms)	<1.5	<1.5	15, 16

SA8025A for the PHS System

Philips Semiconductors applications note AN1891, "Using the SA8025 in 2GHz band applications", shows a design for the PHS system based on the SA8025. If the SA8025A is used in the same design, only RF needs to be changed.

Crystal frequency (f_{XTAL}) = 19.2MHz
Mid VCO frequency (f_{VCO}) = 1665MHz
Q (fractional modulus) = 8
I_{RN} = 80μA
CN = 100
Using Eq. 1 and Eq. 2

$$I_{RF} = \frac{3 \cdot 80e\text{-}6 \cdot 100 \cdot 19.2e6}{8 \cdot 1865e6} = 34.6\mu A$$

$$RF = \frac{3 - 0.9 - 150 \cdot \sqrt{34.6e\text{-}6}}{34.6e\text{-}6} = 35.2k\Omega$$

On the demo board, RF=36kΩ was used. The measured fractional spurs when NF=1 and NF=7 are both better than -70dBc.

Table 4 summarizes the components change for the SA7025/SA8025 and the SA7025 (RevA)/SA8025A demo boards.

Table 4. Summary of Component Changes

Component	SA7025	SA7025 (Rev A)	SA8025	SA8025A
R21	560kΩ	47kΩ	560kΩ	36kΩ
R22	33kΩ	51kΩ	10kΩ	10kΩ
R23	24kΩ	13kΩ	10kΩ	10kΩ
R24	22kΩ	100kΩ	18kΩ	18kΩ
R25	22kΩ	0Ω	0Ω	0Ω
C30	330pF	NL	NL	NL
C31	3.3nF	10nF	3.9nF	3.9nF
C32	220pF	1nF	390pF	390pF
C33	220pF	18pF	150pF	150pF
C34	100pF	NL	NL	NL
NL = Not Loaded				

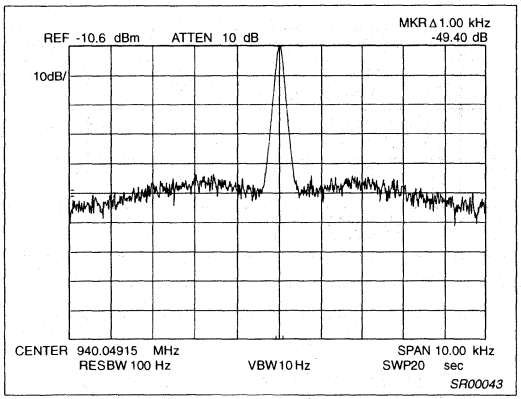


Figure 2. Close-In Noise at 940.05MHz

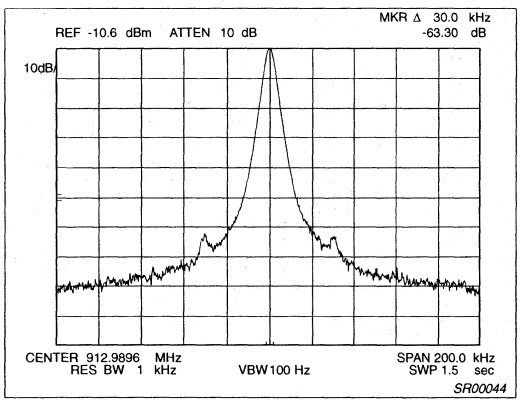


Figure 3. Fractional Spurs, (f_{VCO} = 912.99MHz; NF = 1)

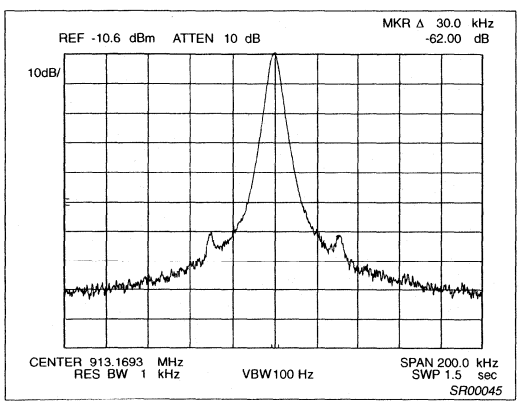


Figure 4. Fractional Spurs, (f_{VCO} = 913.17MHz; NF = 7)

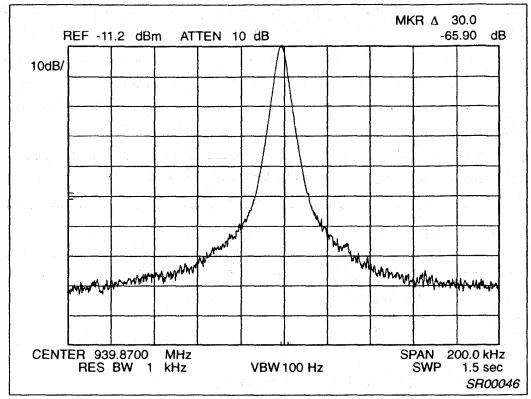


Figure 5. Fractional Spurs, (f_{VCO} = 939.87MHz; NF = 1)

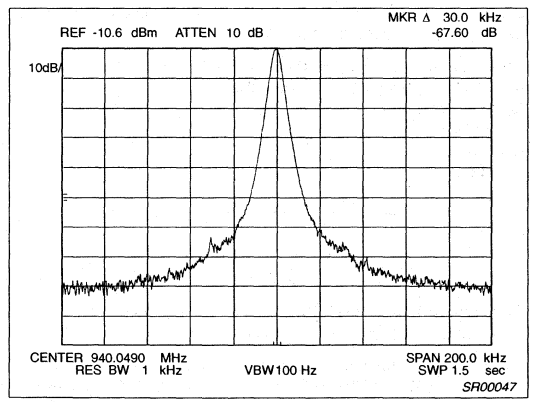


Figure 6. Fractional Spurs, (f_{VCO} = 940.05MHz; NF = 7)

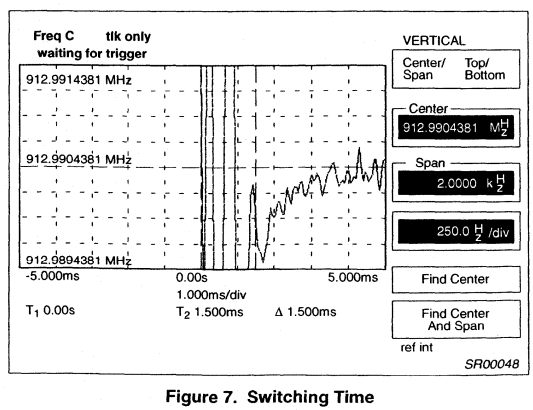


Figure 7. Switching Time (939.87 to 912.99MHz Step to Within 1kHz)

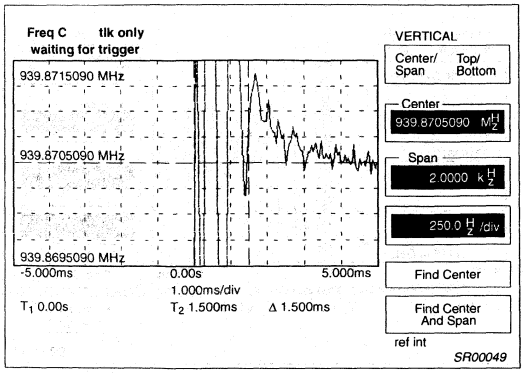


Figure 8. Switching Time (912.99 to 939.87MHz Step to Within 1kHz)

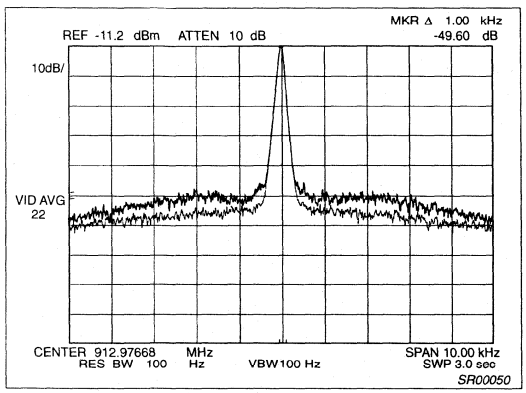


Figure 9. Close-In Phase Noise When CL = 1

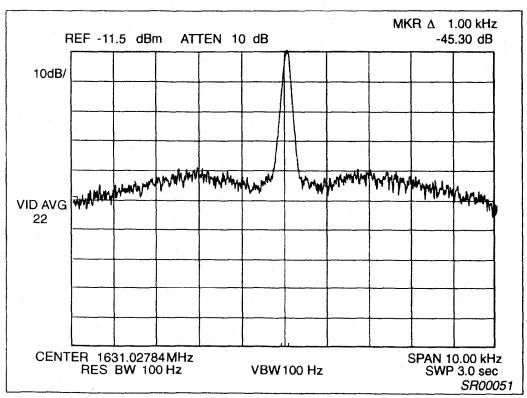


Figure 10. Close-In Phase Noise at 1631.025MHz

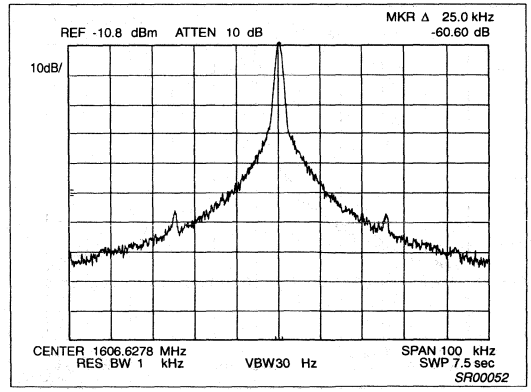


Figure 11. Fractional Spurs, (f_{VCO} = 1606.625MHz; NF = 1)

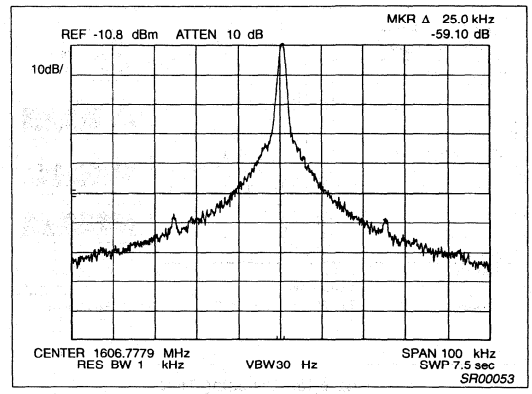


Figure 12. Fractional Spurs, (f_{VCO} = 1606.775MHz; NF = 7)

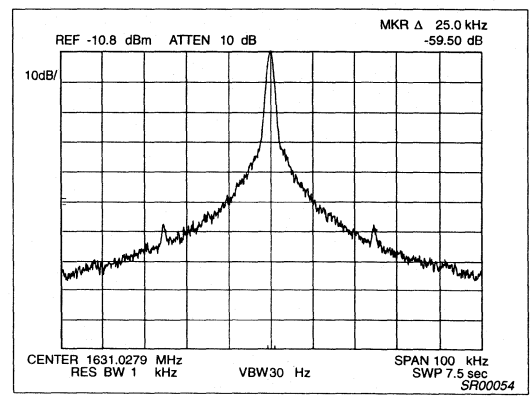


Figure 13. Fractional Spurs, (f_{VCO} = 1606.775MHz; NF = 7)

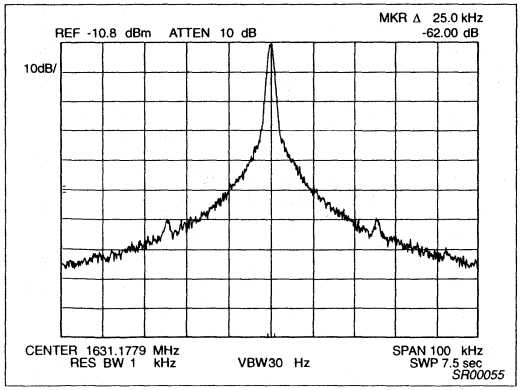


Figure 14. Fractional Spurs, (f_{VCO} = 1631.175MHz; NF = 7)

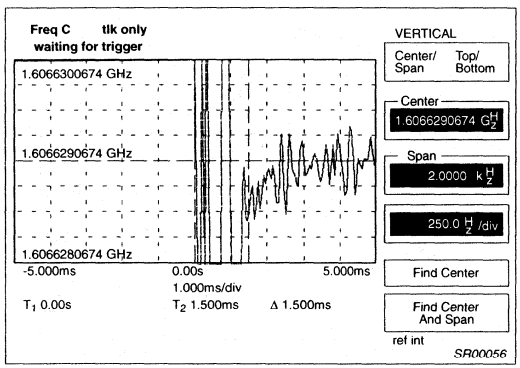


Figure 15. Switching Time (1631.025 to 1606.625MHz Step to Within 1kHz)

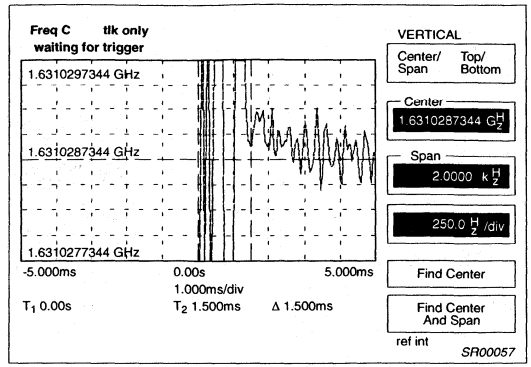


Figure 16. Switching Time (1606.625 to 1631.025MHz Step to Within 1kHz)

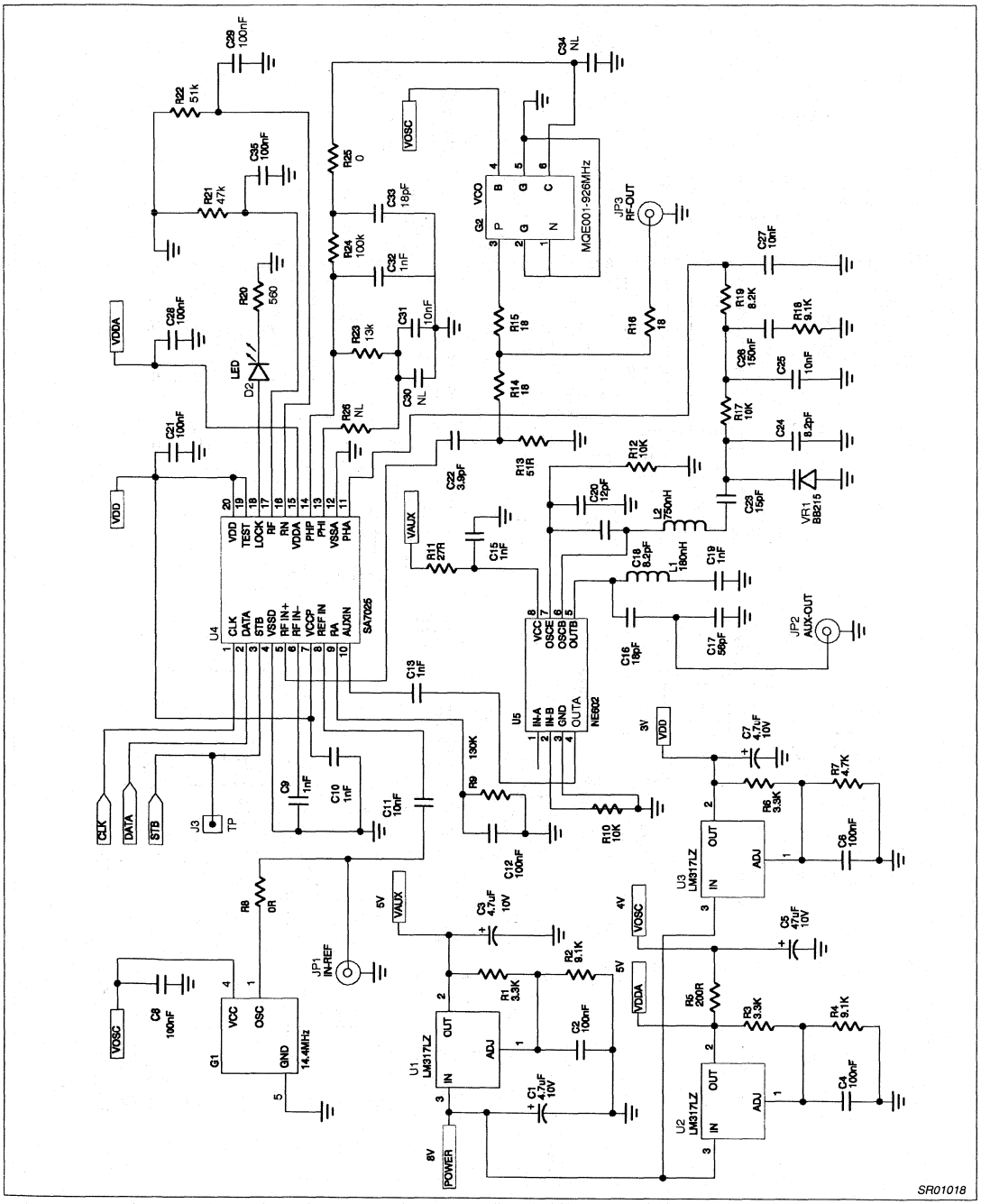


Figure 17. SA7025DK Application Circuit

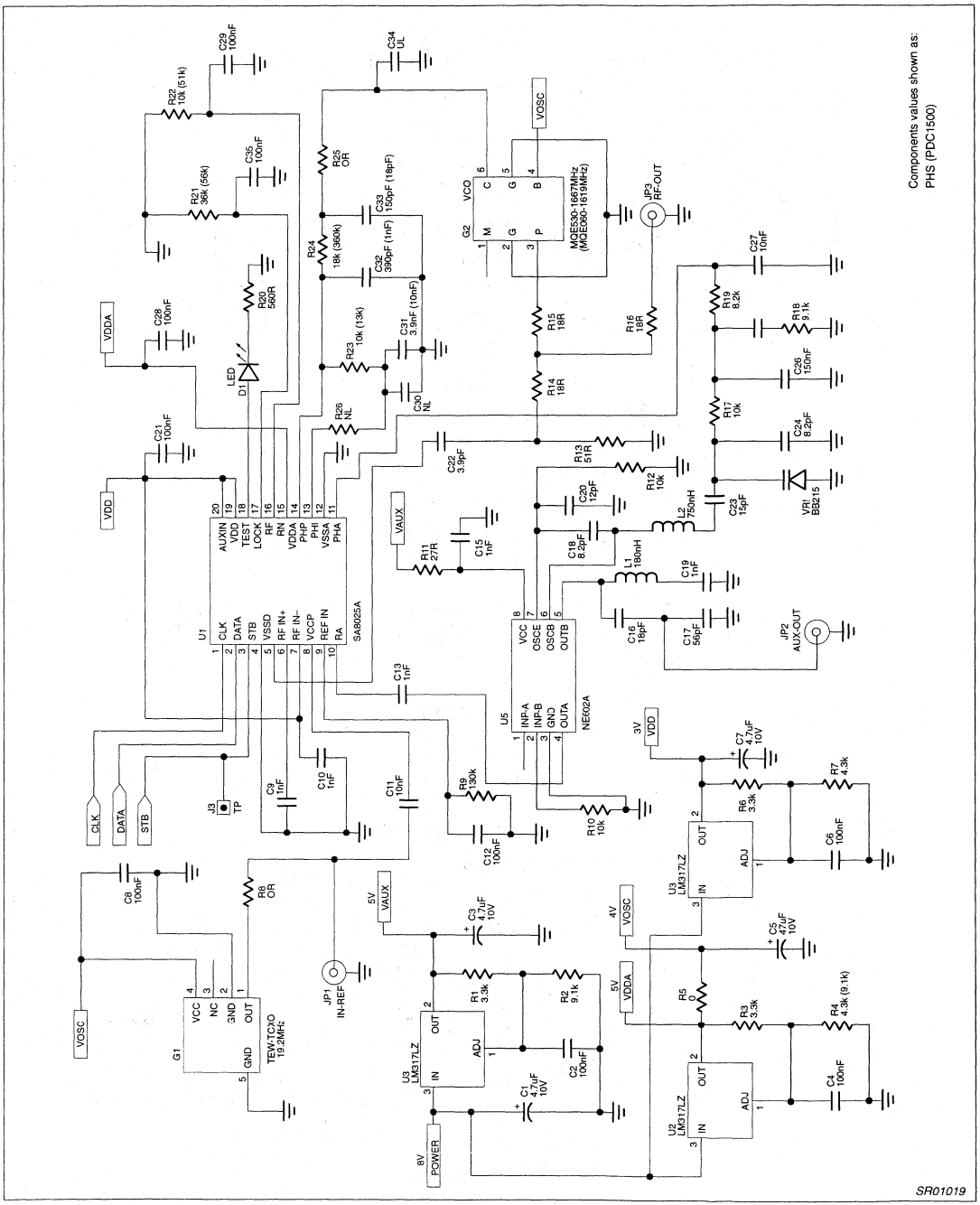
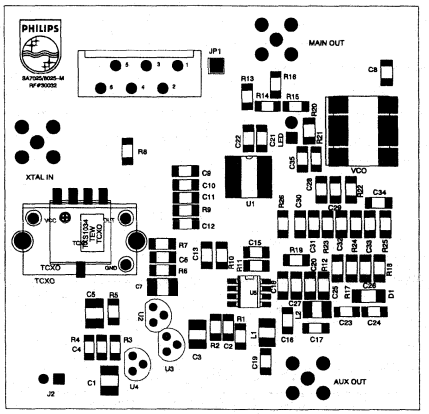
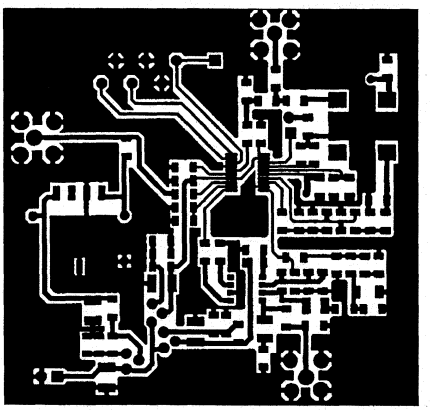


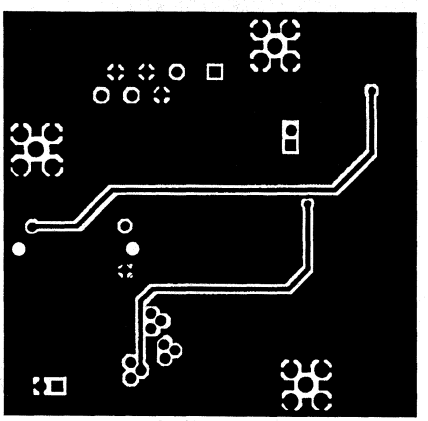
Figure 18. SA8025ADK Application Circuit



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

SR01020

Figure 19. SA8025ADK Demoboard Layout (NOT ACTUAL SIZE)

Table 5. Customer Application Component List for SA7025DK

Qty.	Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	3.9pF	50V	C22	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A3R9CK
2	8.2pF	50V	C24, C18	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A8R2CK
1	12pF	50V	C20	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A120JK
1	15pF	50V	C23	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A150JK
2	18pF	50V	C16, C33	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A180JK
1	56pF	50V	C17	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A560JK
6	1000pF	50V	C9, C10, C13, C15, C19, C32	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315A102JP
4	0.01µF	50V	C11, C25, C27, C31	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C103KK
9	0.1µF	50V	C2, C4, C6, C8, C12, C21, C28, C29, C35	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C104KP
1	0.15µF	16V	C26	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C154KP
4	4.7µF	10V	C1, C3, C5, C7	Tant. chip cap. A 3216 ±10%	Garrett	Philips	49MC475B010KOAS
Surface Mount Resistors							
2	0Ω	50V	R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW000E
3	18Ω	50V	R14, R15, R16	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW180E
1	27Ω	50V	R11	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW270E
1	51Ω	50V	R13	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW510E
1	100Ω	50V	R5	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW101E
1	560Ω	50V	R20	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW561E
3	3.3kΩ	50V	R1, R3, R6	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW332E
1	4.7kΩ	50V	R7	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW472E
1	8.2kΩ	50V	R19	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW822E
3	9.1kΩ	50V	R2, R18, R4	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW912E
3	10kΩ	50V	R10, R12, R17	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW103E
1	13kΩ	50V	R23	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW133E
1	47kΩ	50V	R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW473E
1	51kΩ	50V	R22	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW513E
1	100kΩ	50V	R24	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW104E
1	130kΩ	50V	R9	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW134E
1	560kΩ	50V	R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW564E
Surface Mount Diodes							
1			VR1 (Varactor)	Variable capacitance SMD diode	Digikey	Philips	BB215
1			D1	SM Led	Digikey		
Surface Mount Inductors							
1	0.18µH		L1	Chip inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-181XKBB
1	0.75µH		L2	Chip inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-751XKBB
Voltage Regulators							
3	100mA		U1, U2, U3	Voltage regulator	Digikey	National	LM317LZ
TCXO							
1	14.4MHz		G1	Temp. controlled crystal osc.	TEW	TEW	TXS0924M-14.4MHz
VCO							
1	926MHz		G2	Voltage controlled osc.	Murata	Murata Erie	MQE001-926
Surface Mount Integrated Circuits							
1			U4	1GHz Fractional-N Synthesizer	Philips	Philips	SA7025DK
1			U5	Double Balanced Mixer Oscillator	Philips	Philips	NE/SA602A
Miscellaneous							
3			JP1, JP2, JP3	SMA right angle jack receptacle	Newark	EF Johnson	142-0701-301
1			J1	Male 6-pins connector	STOCKO	STOCKO	MKS1956-6-0-606
1			J2	Male 2-pins connector	STOCKO	STOCKO	MKS1851-6-0-202
1			J3	Test point	Digikey	3M	929647-36
1				Printed circuit board	Philips	Philips	SA7025/8025-M
75 Total Parts							

Table 6. Customer Application Component List for SA8025ADK

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	3.9pF	50V	C22	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A3R9CK
2	8.2pF	50V	C24, C18	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A8R2CK
1	12pF	50V	C20	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A120JK
1	15pF	50V	C23	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A150JK
1	18pF	50V	C16	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A180JK
1	56pF	50V	C17	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A560JK
1	150pF	50V	C33	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A151JK
1	390pF	50V	C32	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A391JK
5	1000pF	50V	C9, C10, C13, C15, C19	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315A102JP
1	3900pF	50V	C31	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C392KK
3	0.01µF	50V	C11, C25, C27	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C103KK
9	0.1µF	50V	C2, C4, C6, C8, C12, C21, C28, C29, C35	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C104KP
1	0.15µF	16V	C26	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C154KP
4	4.7µF	10V	C1, C3, C5, C7	Tant. chip cap. A 3216 ±10%	Garrett	Philips	49MC475B010KOAS
Surface Mount Resistors							
3	0Ω	50V	R5, R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW000E
3	18Ω	50V	R14, R15, R16	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW180E
1	27Ω	50V	R11	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW270E
1	51Ω	50V	R13	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW510E
1	560Ω	50V	R20	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW561E
3	3.3kΩ	50V	R1, R3, R6	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW332E
2	4.3kΩ	50V	R4, R7	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW432E
1	8.2kΩ	50V	R19	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW822E
2	9.1kΩ	50V	R2, R18	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW912E
5	10kΩ	50V	R10, R12, R17, R22, R23	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW103E
1	18kΩ	50V	R24	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW183E
1	36kΩ	50V	R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW364E
1	130kΩ	50V	R9	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW134E
Surface Mount Diodes							
1			VR1 (Varactor)	Variable capacitance SMD diode	Digikey	Philips	BB215
1			D1	SM Led	Digikey		
Surface Mount Inductors							
1	0.18µH		L1	Chip inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-181XKBB
1	0.75µH		L2	Chip inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-751XKBB
Voltage Regulators							
3	100mA		U1, U2, U3	Voltage regulator	Digikey	National	LM317LZ
TCXO							
1	19.2MHz		G1	Temp. controlled crystal osc.	TEW	TEW	TXS1034N-19.2MHz
VCO							
1	1667MHz		G2	Voltage controlled osc.	Murata	Murata Erie	MQE530-1667
Surface Mount Integrated Circuits							
1			U4	2GHz Fractional-N Synthesizer	Philips	Philips	SA8025ADK
1			U5	Double Balanced Mixer Oscillator	Philips	Philips	NE/SA602A
Miscellaneous							
3			JP1, JP2, JP3	SMA right angle jack receptacle	Newark	EF Johnson	142-0701-301
1			J1	Male 6-pins connector	STOCKO	STOCKO	MKS1956-6-0-606
1			J2	Male 2-pins connector	STOCKO	STOCKO	MKS1851-6-0-202
1			T3	Test point	Digikey	3M	929647-36
1				Printed circuit board	Philips	Philips	SA7025/8025-M
75 Total Parts							

SA8025 Fractional-N synthesizer for 2GHz band applications AN1891

Author: Wing S. Djen

INTRODUCTION

The SA8025 is a 3V, 1.8GHz, SSOP 20-pin packaged fractional-N phase locked-loop (PLL) frequency synthesizer. It is targeted for systems like the Japan Personal Handy Phone System (PHS, formerly PHP) which demands fast switching time and good noise performance. Built on the QUBiC BiCMOS process, it has phase detectors with maximum frequency of 5MHz and an auxiliary synthesizer that can operate up to 150MHz. This design was based on the UMA1005 (all CMOS), an earlier version fractional-N synthesizer which requires an external prescaler for 1 and 2GHz applications. There is also a 1GHz version fractional-N PLL frequency synthesizer, the SA7025, available for systems operating under 1GHz. One should expect the performance of the SA8025 and SA7025 to be comparable to the UMA1005 with an extra prescaler. This application note will serve as a supplement to the application note for the UMA1005 (Report No: SCO/AN92002) or as a stand-alone document specifically for the SA8025.

OVERVIEW OF THE FRACTIONAL-N FREQUENCY SYNTHESIZER

Figure 1 shows the basic building blocks of a PLL frequency synthesizer. It consists of a programmable reference divider, phase detector and programmable RF divider (prescaler and main divider). The low-pass filter and voltage-controlled oscillator (VCO) are external to provide design flexibility. The loop has a self-correction mechanism which forces comparison frequency $f_{COMP} = f_{COMP'}$. Since $f_{COMP} = f_{REF}/M$ and $f_{COMP'} = f_{VCO}/N$, the desired frequency becomes $f_{VCO} = (f_{REF}/M)N$. M (reference divider) is fixed for generating f_{COMP}. By incrementing or decrementing the value of N, different frequencies can be synthesized.

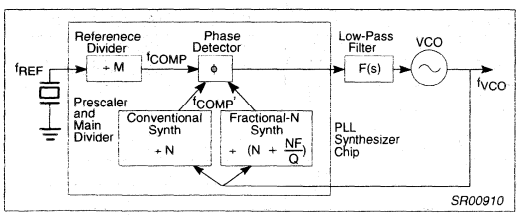


Figure 1. PLL Synthesizer

For conventional synthesizers, the phase detector comparison frequency must be equal to the channel spacing (frequency resolution) because the main divider (N) can only increment and decrement in integer steps. However, the main divider of the fractional-N synthesizer is capable of generating steps to be a fraction of the comparison frequency. Now the total divider ratio consists of an integer part (N) and a fractional part (NF/Q). The numerator (NF) and the denominator (Q, either 5 or 8) of a fraction are controlled through software programming.

Referring to Figure 2, to synthesize channels 1680MHz, 1680.3MHz and 1680.6MHz with channel spacing of 300kHz, the values have to be 5600MHz, 5601MHz and 5602MHz, respectively. The channel spacing of a fractional-N synthesizer is a fraction of the comparison frequency. When using the SA8025, the comparison frequency is increased to either 1.5MHz (mod 5) or 2.4MHz (mod 8), yielding a smaller N value of 1120 (mod 5) or 700 (mod 8) to synthesize 1680MHz.

The advantage of fractional-N synthesizers is two-fold. Since the close-in noise floor is directly related to total divide ratio (N), reducing N five or eight times theoretically implies a close-in noise floor improvement of 14dB (20log(5)) or 18dB (20log(8)), respectively. At the same time, the comparison breakthrough will be 5 or 8 times further away than it would be if a conventional synthesizer were used. This allows a wider loop filter to be used, thus achieving a faster switching time. Faster switching is also achieved due to the higher number of comparison cycles.

To synthesize 1680, 1680.3, 1680.6MHz with channel spacing = 300kHz

Conventional syn. $f_{VCO} = f_{COMP}$ (N)	SA8025 (mod 5) $f_{VCO} = f_{COMP}$ (N + NF/5)	SA8025 (mod 8) $f_{VCO} = f_{COMP}$ (N + NF/8)
1680 = 0.3 (5600)	1680 = 1.5 (1120 + 0/5)	1680 = 2.4 (700 + 0/8)
1680.3 = 0.3 (5601)	1680.3 = 1.5 (1120 + 1/5)	1680.3 = 2.4 (700 + 1/8)
1680.6 = 0.3 (5602)	1680.6 = 1.5 (1120 + 2/5)	1680.6 = 2.4 (700 + 2/8)
f_{COMP} = f_{CH} = 0.3MHz	f_{COMP} = 5 x f_{CH} = 1.5MHz	f_{COMP} = 8 x f_{CH} = 2.4MHz

SR00911

Figure 2. What Is Fractional-N?

DESIGNING WITH THE SA8025

Reference Signal and Divider

Since the synthesized signal is derived from the reference signal, using a clean crystal with an appropriate level is crucial. The reference signal should be AC coupled and deliver between 300 and 600mV_{P-P} to Pin 8 for the input buffer to convert it into a CMOS compatible level. The maximum crystal frequency the part can handle is determined by both analog and digital supplies because the input buffer and the reference divider are powered by V_{DDA} and V_{DD}, respectively. For a $V_{DD} = V_{DDA} = 3V$ configuration, the maximum crystal frequency allowed is 20MHz. When $V_{DD} = 3V$ and $V_{DDA} = 5V$, this frequency becomes 30MHz.

Phase Detector and Charge Pumps

The main and auxiliary phase detectors (see Figure 3) detect both the phase and frequency difference between the divided-down VCO and reference signals. If the main/aux leads the reference, there will be a pulse coming out of the phase detector which turns on the N-type charge pump and sinks current from the low-pass filter. On the other hand, if the main/aux lags the reference, the P-type charge pump will be activated and more current will be delivered to the low-pass filter.

Due to the internal delays of CMOS devices, the phase comparator needs a minimum phase difference, backlash time, to generate an output pulse. This backlash time will introduce a dead-zone around zero phase difference where a small phase error cannot be detected. The way the SA8025 eliminates this problem is by having a minimum on-time of $1/f_{REF}$ for the P pump (sourcing) and N pump (sinking) when the loop is in lock condition, which is shown in Figure 4. Since the charge pump on-time is determined by the crystal reference frequency (f_{REF}), the higher the frequency, the better will be the close-in noise performance. Typically, there will be 3dB close-in noise improvement for a 50% increase in reference frequency (e.g., from 9.6 to 14.4MHz).

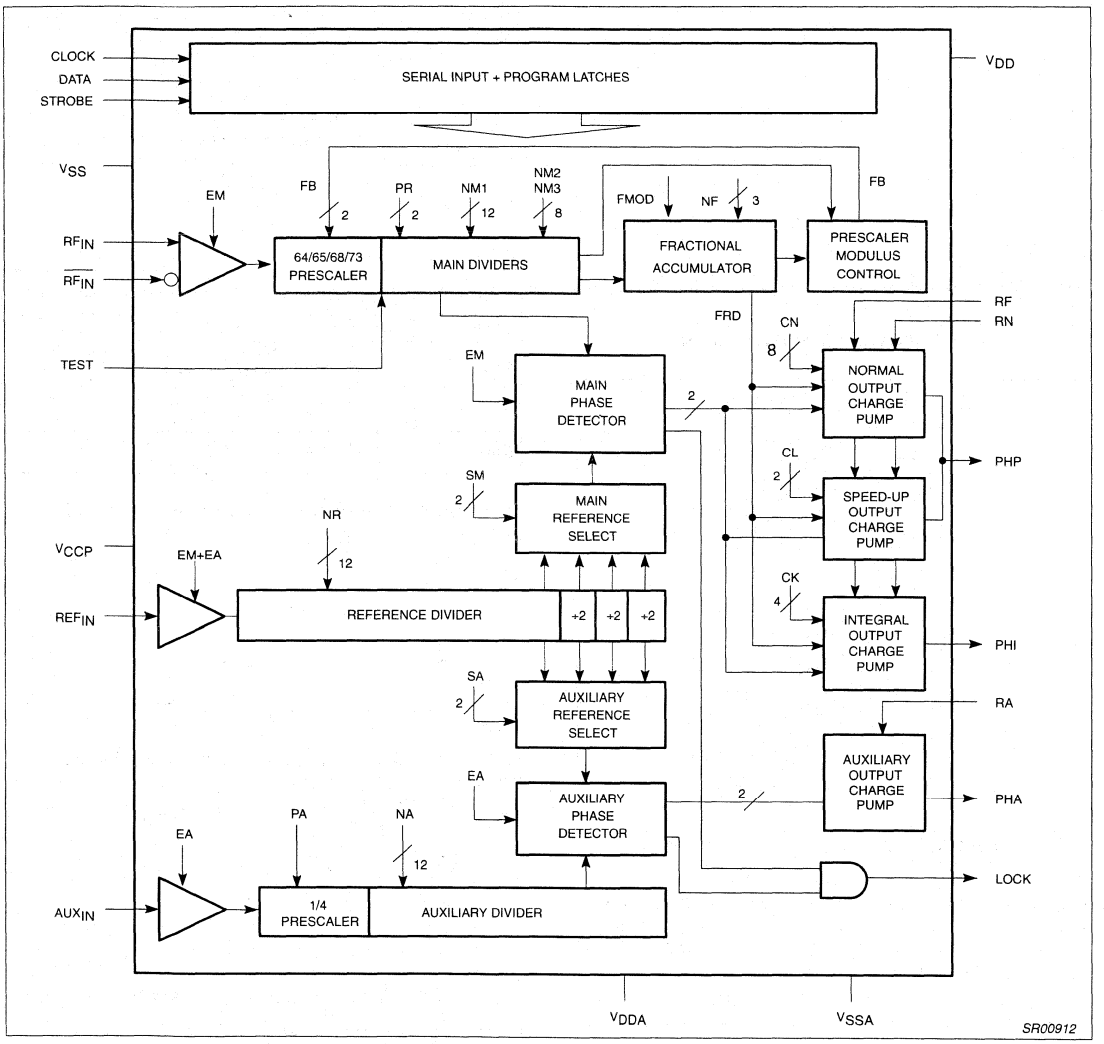


Figure 3. Block Diagram of the SA8025

Since the phase detector detects phase from -2π to 2π, its gain (K_ϕ) equals the charge pump output current (I_{CP}) divided by 2π with units of A/rad.

The charge pump output current, I_{CP} (A), is determined by the external resistor RN and the internal registers CN, CK and CL values. The I_{CP} for normal mode operation (PHP pump only) is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32} \qquad \text{(EQ. 1)}$$

where

$$RN = \frac{V_{DDA} - 0.9 - 150(I_{RN})^{0.5}}{I_{RN}} \qquad \text{(EQ. 2)}$$

Figure 5 shows a graphical representation of Eq. 2. The curves are valid for both main and aux synthesizers. Notice that in normal mode, currents due to the CK and CL values are negligible and only the PHP pump is activated. When the part is in speed-up, both charge pumps are on and the I_{CP} for PHP is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32} (2^{CL+1} + 1) \qquad \text{(EQ. 3)}$$

I_{CP} for PHI is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32} (2^{CL+1})\ CK \qquad \text{(EQ. 4)}$$

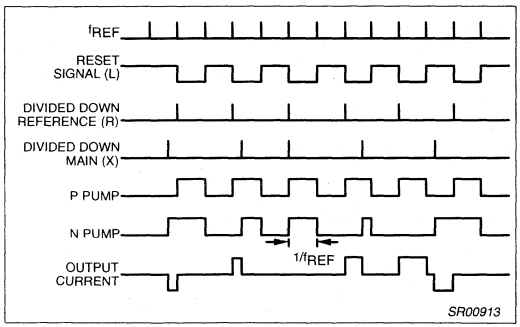


Figure 4. Phase Detector Timing Diagram

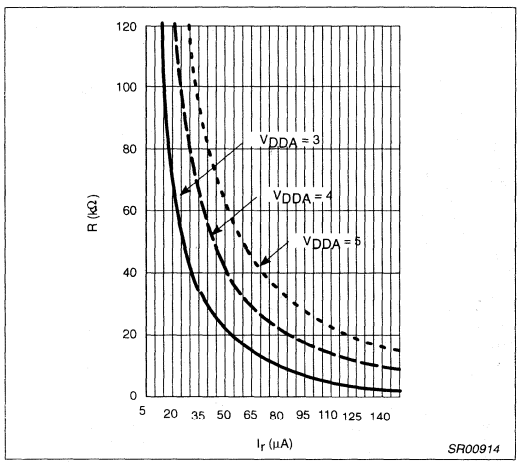


Figure 5. RN(RA) vs. $I_{RN}(I_{RA})$ for Different V_{DDA}

From Eq. 3 notice that in speed-up mode, the PHP output current will be at least 3 times higher than the normal mode current even though CL=0. Speed-up mode stays active as long as the STROBE signal is high after an A word is sent.

Bypass capacitors (100nF) should be used for RN, RF and RA pins to prevent high frequency noise being coupled into the pins causing modulation of the VCO.

Main Divider

The total divide ratio, N, is determined by the combination of the main divider ratio (NM1, NM2, NM3, NM4) and the prescaler values. The part is internally controlled to produce division ratios of N or N+1 when a fractional function is used. The minimum divide ratio, N', which guarantees that all the channels above this ratio can be synthesized consecutively (no blind channels) is different for each prescaler ratio. Since the fractional-N synthesizer increases the comparison frequency, lower N values can be used. To accomplish this, the SA8025 uses a 4 modulus (64/65/68/73) prescaler that lowers the minimum divide ratio to 933.

When programming a total divide ratio (N) which has no components of NM3 or NM4, simply treat them as "don't cares".

Using divide ratios below the minimum divide ratio (N') to synthesize channels is possible, but it requires trial and error. For instance, in the Japan Personal Handy Phone System (PHS), the VCO is running at 1646.7 to 1670.1MHz (248.45MHz first IF). Using a modulus 8 fraction with 300kHz channel spacing, the required N value is between 686 and 695, which is less than the N' of the 4 modulus prescaler. Calculation showed that only N = 695 is not obtainable using the 4 modulus prescaler, but it can be obtained using the 64/65/73 prescaler. The B word must be sent to change the prescaler ratio.

Table 1.

Prescaler Ratio	PR Bits	N'	Total Divide Ratio, N
64/65	01	4032	N = (NM1 + 2) × 64 + NM2 × 65
64/65/68	10	1348	N = (NM1 + 2) × 64 + NM2 × 65 + (NM3 + 1) × 68
64/65/68/73	11	933	N = (NM1 + 2) × 64 + NM2 × 65 + (NM3 + 1) × 68 + (NM4 + 1) × 73
64/65/73	00	1096	N = (NM1 + 2) × 64 + NM2 × 65 + (NM4 + 1) × 73

Determining the Programming Values for NM1, NM2, NM3 and NM4

For the 2-modulus prescaler (64/65), NM1 and NM2 can be determined by:

$$NM2 = 64 \cdot FRAC\left(\frac{N}{64}\right) \quad \text{(EQ. 5)}$$

$$NM1 = INT\left(\frac{N}{64}\right) - NM2 - 2 \quad \text{(EQ. 6)}$$

where FRAC (...) and INT (...) takes the fractional integer part of the argument.

For the 3-modulus prescaler, NM1, NM2 and NM3 (NM4 when PR = 00) can be determined by:

$$K1 = INT\left(\frac{N-R}{64}\right) - 3, \quad K2 = FRAC\left(\frac{N-R}{64}\right) \cdot 64 \quad \text{(EQ. 7)}$$

$$NM3 = INT\left(\frac{K2}{R}\right) \quad \text{(EQ. 8)}$$

$$NM2 = FRAC\left(\frac{K2}{R}\right) \cdot R \quad \text{(EQ. 9)}$$

$$NM1 = K1 - NM2 - NM3 \quad \text{(EQ. 10)}$$

where R = 4 for 64/65/68 prescaler, R = 9 for 64/65/73 prescaler.

For the 4-modulus prescaler (64/65/68/73), we first arbitrarily choose NM4 (smaller values are preferable) and then use the following formulas to calculate NM1, NM2 and NM3:

$$K1 = INT\left(\frac{N-13}{64}\right) - 4, \quad K2 = FRAC\left(\frac{N-13}{64}\right) \cdot 64 \quad \text{(EQ. 11)}$$

$$NM3 = INT\left(\frac{K2 - 9 \cdot NM4}{4}\right) \quad \text{(EQ. 12)}$$

$$NM2 = FRAC\left(\frac{K2 - 9 \cdot NM4}{4}\right) \cdot 4 \quad \text{(EQ. 13)}$$

$$NM1 = K1 - NM2 - NM3 - NM4 \quad \text{(EQ. 14)}$$

Notice that the formulas shown above will give only one set of NM1, NM2, NM3 and NM4 that generates the desired N value. Generating continuous N below 933 (4 modulus) is still possible if all

four modulus options are used. It was found that the part can generate N continuously from 702. The program "8025NMIN.EXE", provided with the "UMAWINE.EXE" for controlling the SA8025 demoboard, calculates all the N values that the part can generate. Users should run the program to find out the right NM1, NM2, NM3 and NM4 if N value of less than 702 is needed. This program will give only one possible combination of NM1 to NM4 for each N.

```
program sa8025
Philips Semiconductors, Sunnyvale, CA
Author: Wing S. Djen
Date: 5/9/94
Purpose: To find the minimum divide ratio on the SA8025

integer i, n1, n2, n3, n4, mod2, mod3a, mod3b, mod4,
+        delta1, delta2, delta3, delta4,
+        temp2, temp3a, temp3b, temp4
+        lown, highn

write(*,*) 'Enter the lowest N value→'
read(*,*) lown
write(*,*) 'Enter the highest N value→'
read(*,*) highn
do 10 i=lown, highn
do 10 n1=0,10
do 10 n2=0,10
do 10 n3=0,10
do 10 n4=0,10
   mod2 = (n1+2)*64 + n2*65
   mod3a = (n1+2)*64 + n2*65 + (n3+1)*68
   mod3b = (n1+2)*64 + n2*65 + (n4+1)*73
   mod4 = (n1+2)*64 + n2*65 + (n3 + 1)*68 + (n4+1)*73
   delta1 = i-mod2
   delta2 = i-mod3a
   delta3 = i-mod3b
   delta4 = i-mod4
   if (delta1.eq.0) then
     if (temp2.eq.mod2) goto 1
     write(*,5) mod2, n1, n2
5    format(' PR="01" N=',i5,3x,'NM1',i2,3x,
+            'NM2=',i2)
     temp2=mod2
     endif
1    if (delta2.eq.0) then
     if (temp3a.eq.mod3a) goto 2
     write(*,6) mod3a, n1, n2, n3
6    format(' PR="10" N=',i5,3x,'NM1',i2,3x,
+            'NM2=',i2,3x,'NM3=',i2)
     temp3a=mod3a
     endif
2    if (delta3.eq.0) then
     if (temp3b.eq.mod3b) goto 3
     write(*,7) mod3b, n1, n2, n4
7    format(' PR="00" N=',i5,3x,'NM1',i2,3x,
+            'NM2=',i2,3x,'NM4=',i2)
     temp3b=mod3b
     endif
3    if (delta4.eq.0) then
     if (temp4.eq.mod4) goto 10
     write(*,8) mod4, n1, n2, n3, n4
8    format(' PR="11" N=',i5,3x,'NM1',i2,3x,
+            'NM2=',i2,3x,'NM3=',i2,3x,'NM4=',i2)
     temp4=mod4
     endif
10   continue
     end
```

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The following is a sample output of the "8025NMIN.EXE" program. It shows the divide ratios that cover the PHS band.

PR="01"	N=128	NM1=0	NM2=0		
PR="01"	N=192	NM1=1	NM2=0		
PR="01"	N=193	NM1=0	NM2=1		
⋮	⋮	⋮	⋮		
PR="11"	N=679	NM1=0	NM2=1	NM3=4	NM4=1
PR="00"	N=679	NM1=1	NM2=3	NM4=3	
PR="00"	N=680	NM1=0	NM2=4	NM4=3	
PR="11"	N=680	NM1=1	NM2=1	NM3=2	NM4=2
PR="11"	N=681	NM1=0	NM2=2	NM3=2	NM4=2
PR="11"	N=682	NM1=0	NM2=0	NM3=5	NM4=1
PR="11"	N=683	NM1=0	NM2=3	NM3=0	NM4=3
PR="11"	N=684	NM1=0	NM2=1	NM3=3	NM4=2
PR="11"	N=685	NM1=1	NM2=1	NM3=1	NM4=3
PR="00"	N=685	NM1=3	NM2=0	NM4=4	
PR="11"	N=686	NM1=0	NM2=2	NM3=1	NM4=3
PR="00"	N=686	NM1=2	NM2=1	NM4=4	
PR="11"	N=687	NM1=0	NM2=0	NM3=4	NM4=2
PR="00"	N=687	NM1=1	NM2=2	NM4=4	
PR="00"	N=688	NM1=0	NM2=3	NM4=4	
PR="11"	N=688	NM1=1	NM2=0	NM3=2	NM4=3
PR="11"	N=689	NM1=0	NM2=1	NM3=2	NM4=3
PR="11"	N=690	NM1=1	NM2=1	NM3=0	NM4=4
PR="11"	N=691	NM1=0	NM2=2	NM3=0	NM4=4
PR="11"	N=692	NM1=0	NM2=0	NM3=3	NM4=3
PR="11"	N=693	NM1=1	NM2=0	NM3=1	NM4=4
PR="11"	N=694	NM1=0	NM2=1	NM3=1	NM4=4
PR="00"	N=694	NM1=2	NM2=0	NM4=5	
PR="00"	N=695	NM1=1	NM2=1	NM4=5	
PR="00"	N=696	NM1=0	NM2=2	NM4=5	
PR="11"	N=697	NM1=0	NM2=0	NM3=2	NM4=4
PR="11"	N=698	NM1=1	NM2=0	NM3=0	NM4=5
PR="11"	N=699	NM1=0	NM2=1	NM3=0	NM4=5
PR="11"	N=702	NM1=0	NM2=0	NM3=1	NM4=5

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RF Inputs

The RF inputs were designed to be used differentially for better noise rejection. However, the part can also be driven single-endedly with $RF_{IN}+$ or $RF_{IN}-$ pin terminated by a 1nF capacitor. The matching network between VCO and RF input was intended for matching both the VCO and the Main Out on the demoboard to 50Ω (see Figure 6).

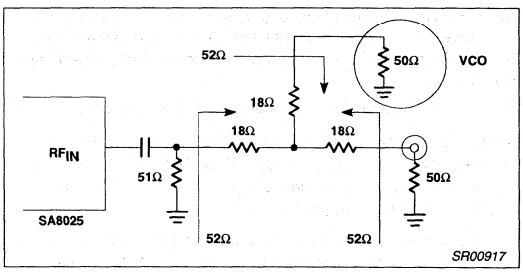

Figure 6. Matching Network for the RF_{IN} Pin

Lock Detect

The LOCK pin is selectable by software to be either the lock detect indicator, output of the main divider, output of the reference divider, or output of the auxiliary divider. Programming details can be found in the data sheet. The pin voltage will go to V_{DD} once the lock condition has been satisfied. Upon power up, the part is in an unknown state and the LOCK pin may go high. It will be functional only after the part is programmed.

Auxiliary Synthesizer

The auxiliary synthesizer does not have fractional-N capability. Therefore, its close-in phase noise and comparison breakthrough performance is comparable to that of a conventional synthesizer. However, this type of performance is not necessary for creating an offset frequency for a Frequency Division Duplex (FDD) system or the 2nd LO in a dual-conversion receiver. Also, an FM signal (e.g., GFSK or analog FM) can be obtained by directly frequency modulating the auxiliary VCO in a PLL structure. The auxiliary phase detector has the same bandwidth (5MHz) as the main phase detector. Current setting for the charge pump (I_{RA}) can be calculated using Eq. 2 and Figure 5. The charge pump output current (I_{CP}) becomes

$$I_{CP} = 8 \cdot I_{RA} \quad \text{(EQ. 15)}$$

Fractional Spurs and Compensation

The total divide ratio of the SA8025 is constantly changing between N and N + 1 to achieve fractional-N capability. This effect introduces an instantaneous phase error at the output of the phase detector in lock condition, which will cause the VCO to generate unwanted spurs at the fractions ($f_{VCO} \pm NF/Q$) of the comparison frequency (f_{COMP}). The SA8025 has internal circuitry which generates appropriate amounts of current to compensate for the phase error for different NF.

Due to the difference in processing technology, fractional compensation current on the SA8025 will not follow the UMA1005. Experimental results show that the resistor RF has to be between 200 and 600 kΩ for optimum fractional spur suppression. It is recommended to adjust the CN value for the high, the middle and the low channel to minimize the fractional spurs. Then linear interpolation technique can be applied to calculate all the CN values for the rest of the channels. A long "A" word (A1) needs to be sent to change the channel and set the CN value at the same time.

PCB Layout

Since careful PCB layout has a great impact on the performance of the synthesizer, users should pay special attention to the rules in building RF circuits. Here are some tips for the synthesizer board layout:

- Follow the layout in this document or on the demoboard.
- It is important that VCO ground is large in size and coupled immediately to the grounded side of the PCB. Make sure that there is a clean path for the VCO ground to get to the system ground (power supply ground).
- To avoid interference, the lead between the VCO output and the RF input should be kept as short as possible. A 50Ω termination resistor should be placed close to the RF input.
- Digital ground (V_{SS}) and analog ground (V_{SSA}) must be separated on the component side of the board. They have to be large in size on the PCB and coupled immediately to the grounded side of the PCB. Designers should refer to the latter part of this application note for the recommended PCB layout.
- Power supply bypass capacitors (100nF) for all devices should be located close to the devices with short leads.
- V_{SSA} should be separated from the ground of other devices such as VCO and mixer chip (NE602).

LOOP FILTER DESIGN

This section presents the procedure for designing the loop filter. Due to the sampling nature of the phase detector and the delay introduced in frequency dividers, complicated mathematical analysis is required for deriving the loop design formulas. However, to give designers a convenient tool for quick design, a simple design procedure based on linear control theory is given below. The detailed derivation is included in the Appendix.

Figure 7a shows a simple 1 pole + 1 zero passive low-pass filter which is commonly used with the PLL synthesizer whose phase detector output is current. This filter has a pole at 0Hz and a zero at $(1/2\pi\ R_1\ C_1)$Hz. Together with the pole introduced by the VCO, this filter will give a 2nd order type 2 (2 poles at 0Hz) PLL loop, which our design procedure is based upon. The inclusion of C_2, R_2 and C_3 (see Figure 7b) effectively introduces two more poles located far away from the zero. This will provide more attenuation, if necessary, on the spurious sidebands without affecting the 2nd order nature of the loop.

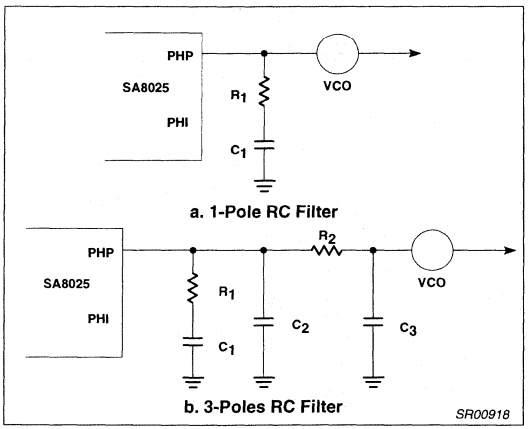

Figure 7. RC Filter Configurations

Definition of the PLL parameters:

δ: final frequency resolution after settling

$$\delta = \frac{\text{frequency error after settling}}{\text{switching step}} \quad \text{(EQ. 16)}$$

t_{SW}: switching time (sec)

f_N: natural frequency of the 2nd order system (Hz), $\omega_N = 2\pi f_N$ (rad/s)

N: total divide ratio

ξ: damping factor of the second order system. Typ. value is 0.707

K_{VCO}: VCO gain (Hz/V) or $2\pi \times$ VCO gain (rad/V)

K_ϕ: phase detector gain = $I_{CP}/2\pi$ (A/rad)

Normal Mode Design

The set of formulas (see Appendix) presented here is valid for normal mode operation in which only charge pump PHP is connected to the low-pass filter. This assumes the STROBE length

is short enough so that speed-up due to STROBE high is minimum in the switching process. Designers should use the normal mode design approach as a starting point and go on to the adaptive mode design if desired PLL performance cannot be met using this configuration.

$$\omega_N = \frac{-\ln(\delta \cdot \xi)}{\xi \cdot t_{SW}} \quad \text{(EQ. 17)}$$

$$C_1 = \frac{K_\phi \cdot K_{VCO}}{N\,\omega_N^{\,2}} \quad \text{(EQ. 18)}$$

$$R_1 = 2 \cdot \xi \left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C_1}\right)^{0.5} \quad \text{(EQ. 19)}$$

$$C_2 \le \frac{C_1}{10} \quad \text{(EQ. 20)}$$

$$\omega = \frac{1}{C_3 \cdot R_2} \quad \omega \text{ should be at least 10 times larger than } \omega_n \quad \text{(EQ. 21)}$$

NOTE: The unit of the factor $K_\phi \times K_{VCO}$ is unity when all the variables are expressed in radians. Therefore, designers can simply multiply the charge pump output current (I_{CP}) with the VCO gain in Hz/V to obtain this factor.

Adaptive Mode Design

The adaptive mode allows designers to take advantage of having one filter with two different loop filter responses. When the synthesizer is switching from channel to channel, a wider filter bandwidth (speed-up) is desired. Once the loop is locked at the correct frequency, a narrower filter is required to achieve lower noise. This mode can be realized by connecting the PHI charge pump to the integrating capacitor C1 (see Figure 8), controlling the width of the STROBE (amount of time for speed-up), and programming the CK and CL registers. Due to this configuration, the zero of the filter gets multiplied by $[2^{CL+1}\,(CK + 1) + 1] / [1 + 2^{CL+1}]$ times, which makes the loop more stable in speed-up mode. One drawback of this design is that switching from speed-up to normal current will cause a difference in the final phase error due to different current gain, which results in frequency instability or a "glitch" in the frequency domain. Because of this effect, the actual switching time will be longer than what the speed-up loop is designed for, since the loop has to re-settle again due to the glitch. Experimental trial of the width of the STROBE can help alleviate this problem.

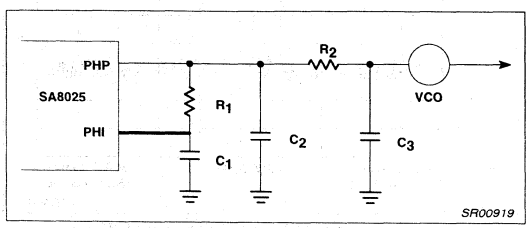

Figure 8. Adaptive Filter

Definition:

ξ_S: speed-up mode damping ratio

ξ_N: normal mode damping ratio

ω_{NS}: speed-up mode natural frequency

ω_{NN}: normal mode natural frequency

Design Steps:

1. Calculate ω_{NS} to meet the system switching time requirement using Eq. 17.
2. Decide how many times ω_{NN} is smaller than ω_{NS}. 5 times will be a good number.
3. Calculate filter component values using Eq. 17 to Eq. 20.
4. Calculate CL and CK values according to

$$CL = 3.32 \log_{10}\left(\frac{\xi_S \cdot \omega_{NS}}{\xi_N \cdot \omega_{NN}} - 1\right) - 1 \quad \text{(EQ. 22)}$$

$$CK = \left[\frac{\left(\frac{\omega_{NS}}{\omega_{NN}}\right)^2 - 1}{\left(\frac{\xi_S \cdot \omega_{NS}}{\xi_N \cdot \omega_{NN}} - 1\right)}\right] - 1 \quad \text{(EQ. 23)}$$

The above procedure ensures the loop bandwidth in speed-up mode is 5 times greater than that in normal mode while maintaining the required stability of the loop.

DESIGN EXAMPLE

This section shows a design example using the SA8025 for the Personal Handy Phone System (PHS), where the device is used in the normal mode (only PHP charge pump is active). The system parameters are as follows:

VCO frequency (f_{VCO}) = 1646.7 to 1670.1MHz

Channel spacing (f_{CH}) = 300kHz

Comparison frequency (f_{COMP}) = 8 × 300kHz = 2.4MHz

Switching time (t_{SW}) = 500µs

Switching step = 25MHz

Frequency error = within 1kHz

VCO gain (K_{VCO}) = 15MHz/V

Reference Crystal (f_{REF}) = 19.2MHz

Determine total divide ratio N

To synthesize channels from 1646 to 1670MHz with f_{COMP} = 2.4MHz, N should be between 686 and 695. For the same loop components, larger N yields smaller natural frequency (f_N). So, jumping from high-end to low-end (larger N) is slower than from low-end to high-end (smaller N). To ensure the same switching time from either direction, we use N = 695 for the worst case.

Determine ω_N

Using Eq. 16

$$\delta = \frac{1000}{25e6} = 0.04e\text{-}3$$

Pick ξ = 0.707 and use t_{SW} = 400µs for safety.
Using Eq. 17

$$\omega_N = \frac{-\ln(0.04e\text{-}3 \cdot 0.707)}{0.707 \cdot 400e\text{-}6} = 37{,}035$$

Determine R_N and I_{CP}

Pick RN = 10kΩ and CN = 100. Referring to Figure 5, I_{RN} becomes 80µA when V_{DDA} = 3V.
Using Eq. 1

$$I_{CP} = 100\left(\frac{80e\text{-}6}{32}\right) = 250\mu A$$

Determine R_1, C_1 and C_2

Using Eq. 18 with 2π's from K_{VCO} (rad/V) and K_ϕ (A/rad) cancel out

$$C_1 = 15e6 \left(\frac{250e\text{-}6}{695 \cdot 37,035^2}\right) = 3.93nF$$

Using Eq. 19

$$R_1 = 2 \cdot 0.707 \cdot \left(\frac{695}{15e6 \cdot 250e\text{-}6 \cdot 3.9e\text{-}9}\right)^{0.5} = 9.7k\Omega$$

Using Eq. 20

$$C_2 = \frac{3.93e\text{-}9}{10} = 390pF$$

Determine R_2 and C_3

R_2 and C_3 can help attenuate the unwanted fractional spurs at 300kHz offset.

Using Eq. 21

$$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_N$$

Pick R_2 = 18kΩ, then C_3 = 150pF.

Fractional spurs compensation, if necessary

With f_{COMP} = 300kHz, there would be some spurs located at 300kHz or multiples of 300kHz when NF not equal to 0. For this particular design, we are able to use a fixed CN value (100) to achieve spurs suppression of at least -64dBc for spurs located at 300kHz carrier offset. Spurs located at other frequencies are not present.

Design results

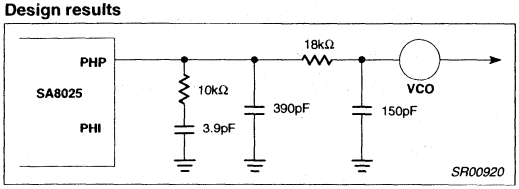

Figure 9. Main Loop Filter

Component values used on the demoboard:
C31 = 3.9pF
R23 = 10kΩ
C32 = 390pF
R24 = 18kΩ
C33 = 150pF
R21 = 560kΩ (RF)
R22 = 10kΩ (RN)

Software setting:
CN = 100
STROBE = 190µs

MEASUREMENT RESULTS

The major performance parameters for a PLL synthesizer are close-in phase noise, spurious sidebands and switching time. This section presents the measurement results obtained from the design made in the section on LOOP FILTER DESIGN.

Close-In Phase Noise

The close-in phase noise level directly correlates with the residual FM and integrated jitter performance, two integrated noise parameters. It is measured within the loop bandwidth (the peak of the "hump" around the carrier) at a specified carrier frequency offset, e.g., 1kHz, and it is expressed in -dBc/Hz. Figure 10 displays the result of such a measurement. The carrier is located at 1668.3MHz (NF = 1) and the span is 10kHz. The resolution bandwidth (measurement bandwidth) is 100Hz. Therefore, the close-in phase noise at 1kHz offset is:

= -58.2dBc – 10 log (100)

= -78.2dBc/Hz

Spurious Performance

Figures 11 and 14 show the spurious performance of the highest and the lowest bands of interest with NF = 1 and 7, which are the worst case for fractional spurs. Other spurs within the band are totally compensated.

Switching Time

The switching time (see Figures 15 and 16) was measured using the HP 53310A Modulation Domain Analyzer (MDA) with option 031. Under the TRIGGER Menu of the MDA, "Triggered", "Ext Edge" and "Arm Only" were selected. The instrument was setup to accept an external trigger, which was the STROBE signal used for programming the synthesizer. This signal was connected to the Ext Arm input while the VCO signal was fed into the Channel C. The MDA would display the frequency versus time variation of the VCO signal upon the arrival of the STROBE signal. This design achieved a switching time of 400µs to within 1kHz of the final frequency for a 21.6MHz jump between 1646.7 and 1668.3MHz in either direction. The STROBE width used in this experiment was 190µs.

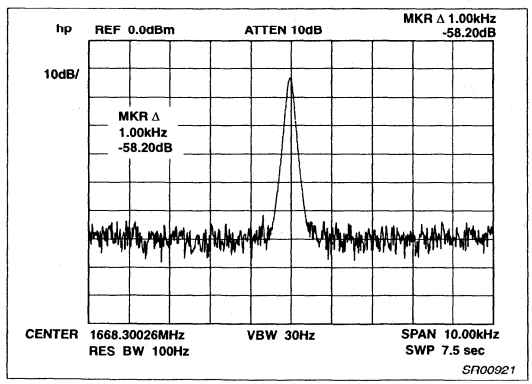

Figure 10. Close-In Phase Noise at 1668.3MHz

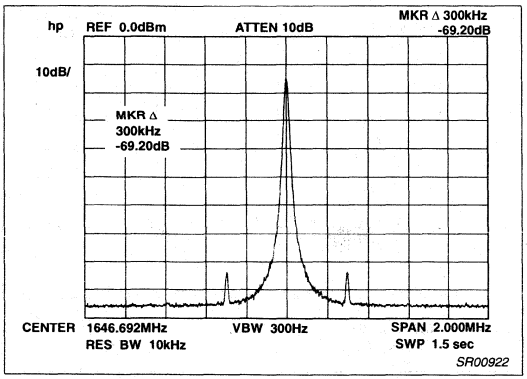

Figure 11. Fractional Spurs (f_{VCO} = 1646.7MHz, NF = 1)

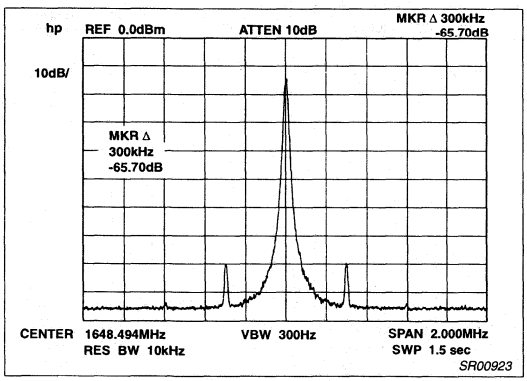

Figure 12. Fractional Spurs (f_{VCO} = 1648.5MHz, NF = 7)

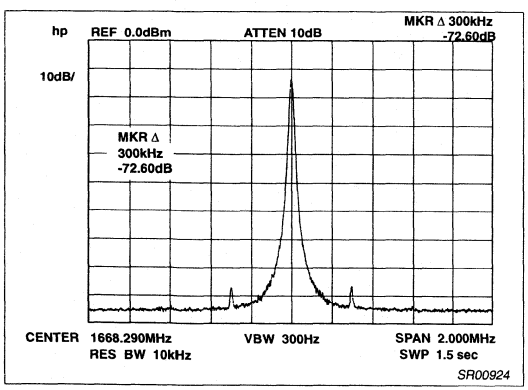

Figure 13. Fractional Spurs (f_{VCO} = 1668.3MHz, NF = 1)

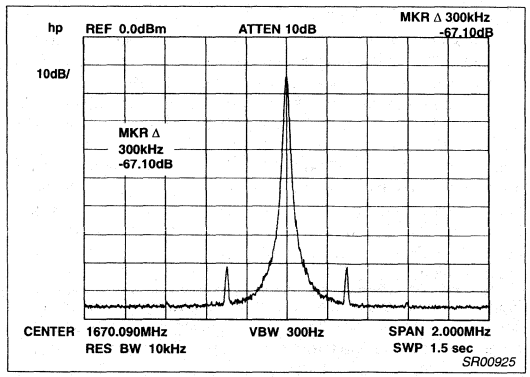

Figure 14. Fractional Spurs (f_{VCO} = 1670.1MHz, NF = 7)

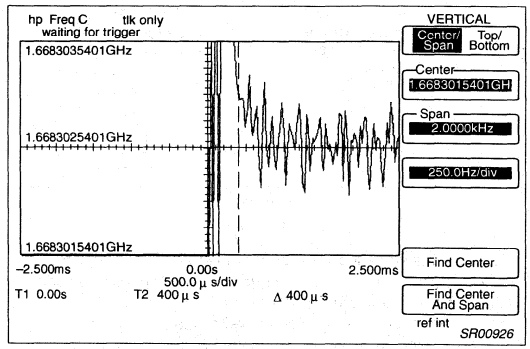

Figure 15. Switching Time (1668.3 to 1646.7MHz Step to Within 1kHz)

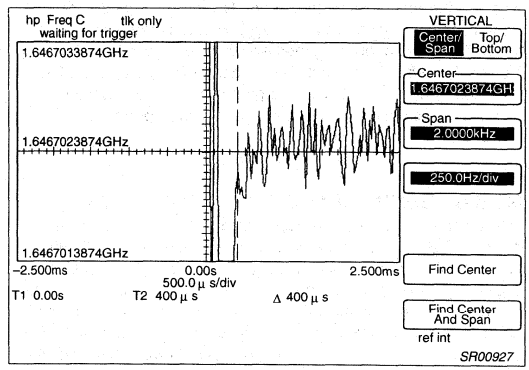

Figure 16. Switching Time (1646.7 to 1668.3MHz Step to Within 1kHz)

MODULO 4 DESIGN

Previous sections showed a design using a 4 modulus prescaler (64/65/68/73) to synthesize total divide ratios (N) from 686 to 694. This requires sending both B and A words since NM4 is stored in B word. In some designs, users may prefer to send only one word for channel switching due to hardware limitation. We could have used modulo 5 (FMOD = 5) to make N five times higher and used a triple modulus prescaler (64/65/68 or 64/65/73). In some situations this is impossible since the comparison frequency has to be an integer factor of the crystal reference. For instance, if f_{REF} is 19.2MHz and f_{CH} is 300kHz, f_{COMP} becomes 1.5MHz, which is not an integer factor of 19.2MHz. To get around this problem, a modulo 4 design must be used.

Figure 17 shows the concept of a modulo 4 design. In the mod 4 case, f_{COMP} is four times the channel spacing, f_{CH}. Instead of programming NF to one through seven, even numbers are used.

To synthesize 1656.3, 1656.6, 1656.9, 1657.2MHz with channel spacing = 300kHz using mod 8 and mod 4.

SA8025 (mod 8)	SA8025 (mod 4)
$f_{VCO} = f_{COMP}$ (N+NF/8)	$f_{VCO} = f_{COMP}$ (N+NF/8)
1656.3 = 2.4 (690 + 1/8)	1656.3 = 1.2 (1380 + 2/8)
1656.6 = 2.4 (690 + 2/8)	1656.6 = 1.2 (1380 + 4/8)
1656.9 = 2.4 (690 + 3/8)	1656.9 = 1.2 (1380 + 6/8)
1657.2 = 2.4 (690 + 4/8)	1657.2 = 1.2 (1381 + 0/8)
f_{COMP} = 8 x f_{CH} = 2.4MHz	f_{COMP} = 4 x f_{CH} = 1.2MHz

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Figure 17.

To achieve the same loop response with the mod 8 design, the same loop filter with twice the charge pump current can be used. This can be derived from Eq. 18. When N is doubled, K_ϕ (two times more current) has to be doubled as well to maintain the same natural frequency which determines the switching time and residual FM. In this case, we use CN = 200 for the mod 4 design.

The only penalty of this method is that theoretical close-in phase noise performance is affected. Since N is twice as much, the close-in noise floor should be 20log(2) = 6dB higher. However, minor degradation for using mod 4 was measured in the laboratory. This could be due to the fact that the comparison cycles are fewer with mod 4, which makes the charge pump ON time less, thus producing less noise. In addition, higher charge pump current improves the phase noise.

MOD 4 DESIGN MEASUREMENT RESULTS

Figures 18 to 22 show the measurement results for the mod 4 design. The close-in phase noise level is shown to be -77.1dBc/Hz at 1kHz carrier offset with a measurement bandwidth of 100Hz. Spurious sidebands (see Figures 19 and 20), which are caused by fractional jitter, are -67dB down from carrier for the high band and -68dB down for the low band. Switching time (see Figures 21 and 22) is exactly the same as the mod 8 design (400µs) because the loop natural frequency is the same for both cases.

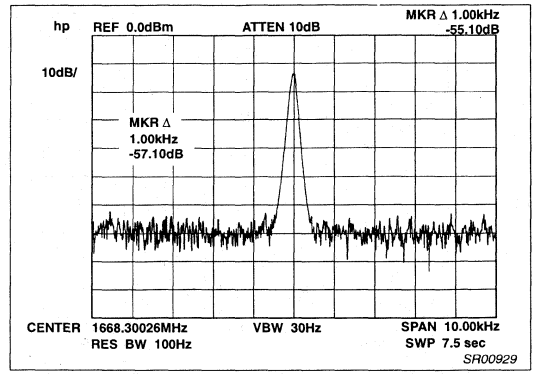


Figure 18. Close-In Phase Noise at 1668.3MHz

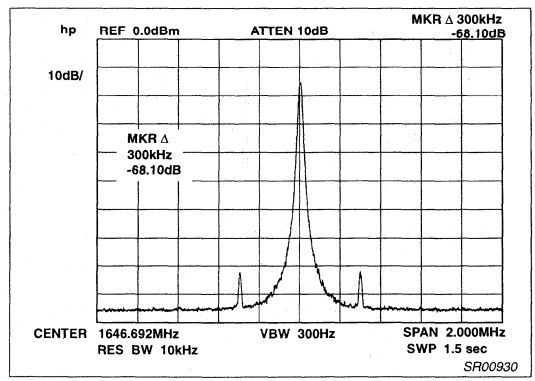


Figure 19. Fractional Spurs (f_{VCO} = 1646.7MHz, NF = 2)

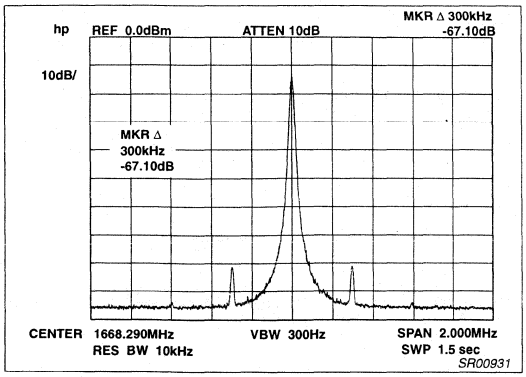


Figure 20. Fractional Spurs (f_{VCO} = 1668.3MHz, NF = 2)

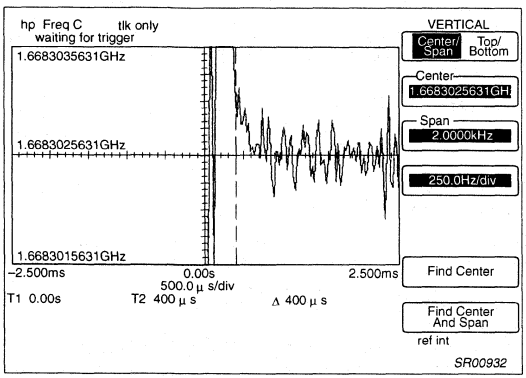


Figure 21. Switching Time (1668.3 to 1646.7MHz Step to Within 1kHz)

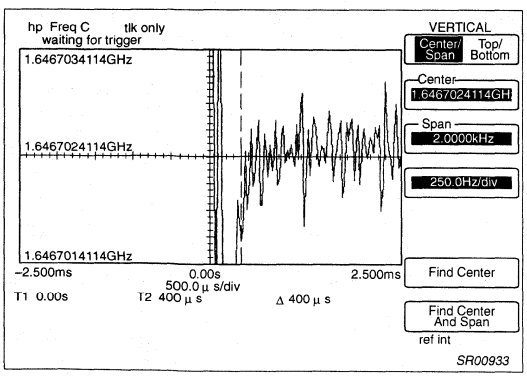


Figure 22. Switching Time (1646.7 to 1668.3MHz Step to Within 1kHz)

FREQUENTLY ASKED QUESTIONS

Q. The part is powered-up and programmed. The VCO is still free-running. What's wrong?

A. Three things to check for if the PLL does not lock:

1. Make sure the correct data have been transmitted to the CLK, DATA and STROBE pins
2. Make sure a reference signal with correct frequency and amplitude are present at the REF_{IN} pin.
3. Make sure that the prescaler value is chosen correctly. The SA8025 has two 3 modulus prescalers and uses different programming bits.
4. Be aware of cold solder joints. Pay special attention to the loop filter section and the connection from the VCO to the RF_{IN} pin.

Q. The synthesizer locks up, but it locks at a wrong frequency. Why?

A. Check the NM1, NM2, NM3 and NM4 bits. Make sure they are correctly programmed.

Q. I see spurs sitting at the comparison frequency offset and they don't change with the filter bandwidth. How can I get rid of them?

A. These spurs may be caused by improper grounding of the VCO and the filter section. Make sure they all have short and clean paths going back to the supply ground. Also, clean the filter section to avoid leakage.

Q. I see some spurs which are neither fractional nor comparison spurs. What are they?

A. Since the VCO is a very sensitive device, it can be influenced by many noise sources. Common ones are:

1. Computer monitor. The sweeping frequency of the screen will modulate the VCO and create spurious sidebands at 30 to 40kHz carrier offset.
2. Free-running auxiliary VCO. Even though the EA bit is disabled, if the auxiliary VCO is still ON, it will modulate the main VCO and cause spurs.
3. Fluorescent lamp.

Q. How can the residual FM be improved?

A. Three things can be done to improve residual FM:

1. Use a narrower loop filter.
2. Use a higher crystal reference frequency. This will reduce the charge pumps ON time and make the charge pumps generate less noise.
3. Use higher charge pump output current. This will increase the signal to noise ratio at the charge pump, which makes the circuit less noisy.

Q. When I FM modulate the AUX synthesizer, I see modulation on the MAIN carrier as well. Is that normal?

A. Yes, that is normal. The amount of interference between the AUX and the MAIN has to be verified experimentally.

Q. If I double the phase detector gain (twice the current), what should be done to keep the switching time the same?

A. Referring to Eq. 18 and Eq. 19, the value of C_1 should be doubled and R_1 should be halved if you want to maintain the same natural frequency of the loop when the detector gain (K_ϕ) is twice what it was before.

Q. When I use the 3 modulus prescaler (PR = 10), what should the values for NM4 be?
A. Simply treat them as "don't cares".

Q. What is the phase detector gain? Is it charge pump output current divided by 2π or just the charge pump output current, itself?
A. The phase detector gain (K_ϕ) is equal to the charge pump output current (I_{CP}) divided by 2π since the phase detector covers 2π range. However, when we use the design formulas shown in the "Loop Filter Design" section, K_ϕ can be replaced directly by I_{CP} because the 2π factor will be cancelled out by the 2π from the VCO gain, K_{VCO}.

Q. What should I do with the RA and PHA pins when the auxiliary synthesizer is not used?
A. When the auxiliary synthesizer is not used, leave PHA open, connect AUX_{IN} to ground, connect RA to V_{DDA} or leave it open and program EA bit to zero.

Q. Variations on the RF pins input impedance for different prescaler value can cause VCO pulling. Does that happen to the SA8025?
A. The RF input to the prescaler is well buffered, and the input impedance should always stay the same.

Q. Can the clock signal be disconnected after the A word is sent?
A. Yes, the clock signal can be disabled after the A word is sent and enabled again for sending new words to the part.

Q. Can I drive the part with a +5dBm RF signal even though the spec is 0dBm max?
A. Users should refer to the graphs put in the latter part of the data sheet for minimum and maximum input power. The device should be able to handle +5dBm at 1800MHz, but this is not guaranteed in the data sheet.

Q. I am doing open-loop modulation on the main synthesizer. How do I put the charge pump to high impedance state to allow modulation?
A. Program CN register to zero. This will set the charge pump to a high output impedance state so that FM modulation can be done.

Q. Is the demoboard layout good for any applications? If not, what should I do?
A. The demoboard layout included in this document was optimized only for this particular design. Designers should consult the PCB layout hints in the "PCB Layout" section of this application note when laying out circuit boards for other applications.

Q. I am using the S8025 for PHS system and seeing different amplitudes on the fractional spurs from part to part. However, this variation does not appear to affect my RX/TX performance. Is this a safe assumption?
A. Yes, because the SA8025 is targeted for the PHS system and any spurs that only fall in the adjacent channels (at 300kHz carrier offset) are acceptable for the PHS.

REFERENCES

"Digital PLL Frequency Synthesizers", Ulrich L. Rohde, Prentice Hall, 1983.

"Designer Guide to Frequency Synthesis Using the UMA1005", Application Note, Report No: SCO/AN92002.

"Modem Control Systems", Richard C. Dorf, Addison Wesley, 1989.

APPENDIX

Derivation of the 2nd order PLL design formula:

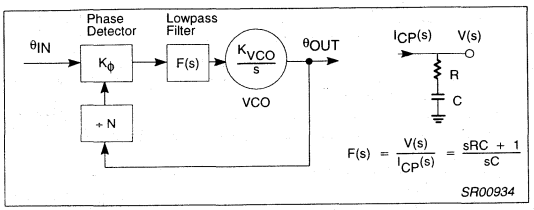


Figure 23. PLL Block Diagram

The transfer function of the loop low-pass filter is represented by:

$$F(s) = \frac{sRC + 1}{sC} \quad \text{(EQ. 24)}$$

The low-pass filter has a pole at 0Hz (set denominator to zero) and a zero at $1/2\pi RC$ Hz (set numerator to 0).

Referring to Figure 23, the open-loop response of the system (multiplication of the Forward Gain and Feedback Gain) becomes:

$$G(s)H(s) = \frac{K_\phi \cdot K_{VCO}}{Ns}\left(\frac{sRC + 1}{sC}\right) \quad \text{(EQ. 25)}$$

Phase Margin (ϕ_{PM}) is defined as the difference between -180° and the phase at the point where the open-loop response has unity gain. A stable system must have a ϕ_{PM} greater than 0°. Eq. 25 shows that there are two poles sitting at 0Hz, one from the filter and one from the VCO, which causes -180° phase shift. In order to have a stable system, a zero has to be added to the filter so that ϕ_{PM} will be greater than zero. ϕ_{PM} is related to the damping factor, ξ, with $\xi = 0.01 \times \phi_{PM}$.

To find the characteristic equation (CE) of the system, we equate 1 + G(s)H(s) to zero. Therefore,

$$1 + \frac{K_\phi \cdot K_{VCO}\,(sRC + 1)}{s^2 NC} = 0 \quad \text{(EQ. 26)}$$

The CE becomes

$$s^2 + \frac{K_\phi \cdot K_{VCO} \cdot R}{N}s + \frac{K_\phi \cdot K_{VCO}}{NC} \quad \text{(EQ. 27)}$$

Compare Eq. 27 with the standard 2nd order CE ($s^2 + 2\zeta\omega_N s + \omega_N^2$), we have

$$\omega_N^2 = \frac{K_\phi \cdot K_{VCO}}{NC} \Rightarrow C = \frac{K_\phi \cdot K_{VCO}}{N\,\omega_N^2} \quad \text{(EQ. 28)}$$

$$2\xi\omega_N^2 = \frac{K_\phi \cdot K_{VCO} \cdot R}{N} \Rightarrow R = 2 \cdot \xi \left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C}\right)^{0.5} \quad \text{(EQ. 29}$$

which are the design used in "Loop Filter Design" section.

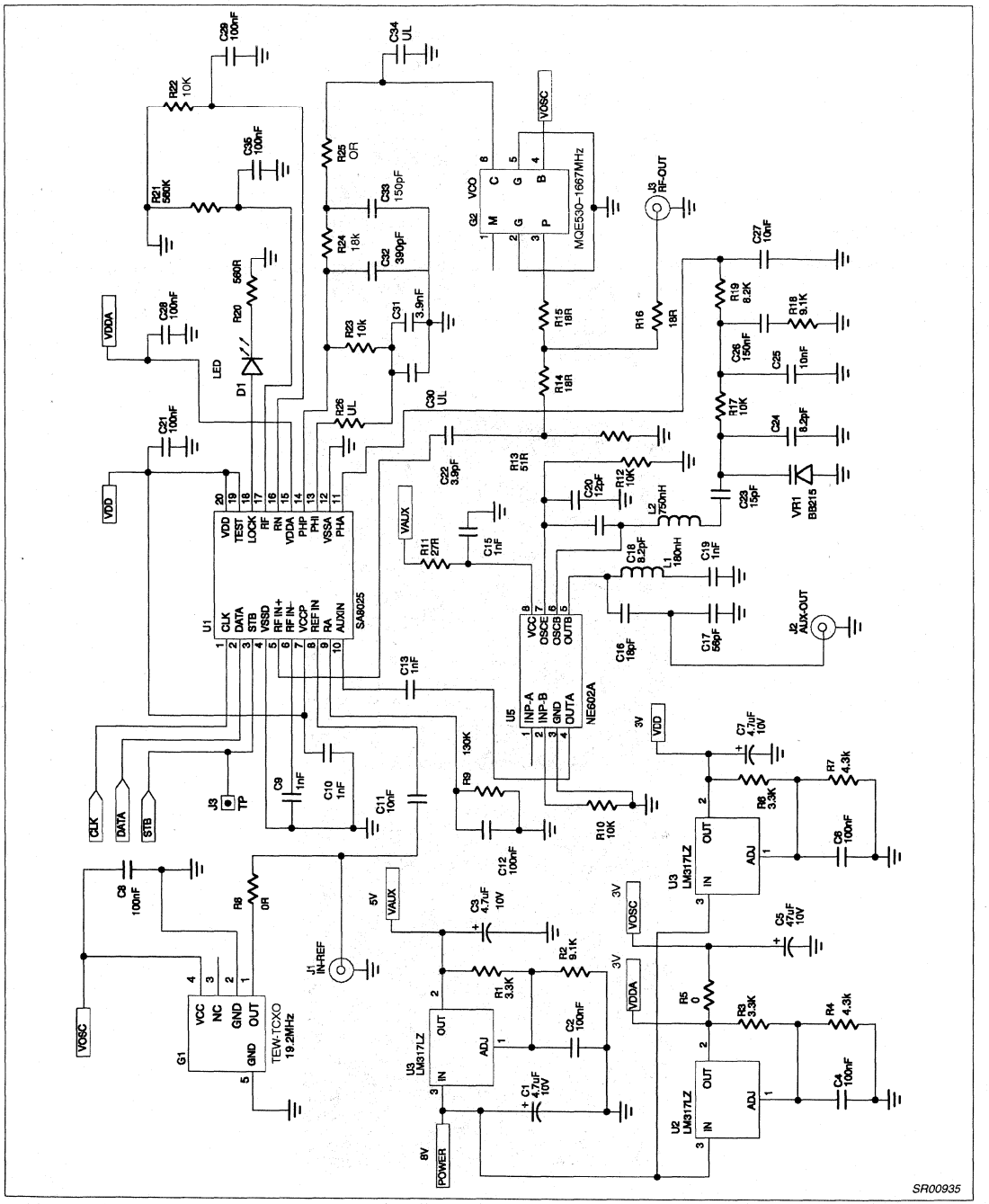
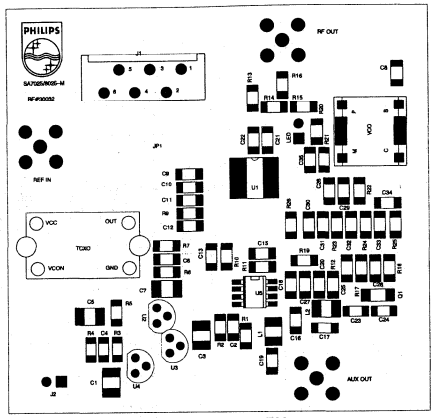
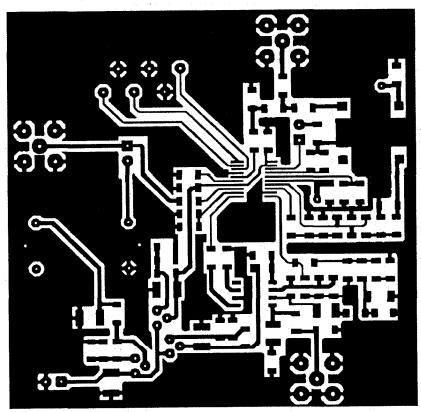


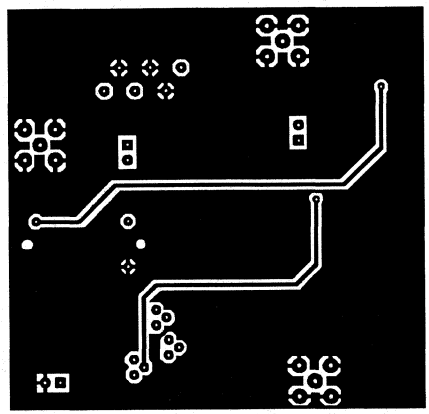
Figure 24. SA8025DK Application Circuit



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

SR00936

Figure 25. SA8025DK Demoboard Layout (NOT ACTUAL SIZE)

Table 2. Customer Application Component List for SA8025DK

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	3.9pF	50V	C22	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A3R9CK
2	8.2pF	50V	C24, C18	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A8R2CK
1	12pF	50V	C20	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A120JK
1	15pF	50V	C23	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A150JK
1	18pF	50V	C16	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A180JK
1	56pF	50V	C17	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A560JK
1	150pF	50V	C33	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A151JK
1	390pF	50V	C32	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A391JK
5	1000pF	50V	C9, C10, C13, C15, C19	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315A102JP
1	3900pF	50V	C31	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C392KK
3	0.01µF	50V	C11, C25, C27	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C103KK
9	0.1µF	50V	C2, C4, C6, C8, C12, C21, C28, C29, C35	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C104KP
1	0.15µF	16V	C26	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C154KP
4	4.7µF	10V	C1, C3, C5, C7	Tant. chip cap. A 3216 ±10%	Garrett	Philips	49MC475B010KOAS
Surface Mount Resistors							
3	0Ω		R5, R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW000E
3	18Ω		R14, R15, R16	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW180E
1	27Ω		R11	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW270E
1	51Ω		R13	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW510E
1	560Ω		R20	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW561E
3	3.3kΩ		R1, R3, R6	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW332E
2	4.3kΩ		R5, R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW432E
1	8.2kΩ		R19	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW822E
2	9.1kΩ		R2, R18	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW912E
5	10kΩ		R10, R12, R17, R22, R23	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW103E
1	18kΩ		R24	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW183E
1	130kΩ		R9	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW134E
1	560kΩ		R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW564E
Surface Mount Diodes							
1			VR1 (Varactor)	Variable capacitance SMD diode	Digikey	Philips	BB215
1			D1	SM Led	Digikey		
Surface Mount Inductors							
1	0.18µH		L1	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R18M
1	0.75µH		L2	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R68M
Voltage Regulators							
3			U1, U2, U3	Voltage regulator	Digikey		LM317LZ
TCXO							
1	19.2MHz		G1	Temp. controlled crystal osc.	TEW	TEW	TXS1034N-19.2MHz
VCO							
1	1667MHz		G2	Voltage controlled osc.	Murata	Murata Erie	MQE530-1667
Surface Mount Integrated Circuits							
1			U4	1MHz Fractional-N Synthesizer	Philips	Philips	SA8025DK
1			U5	Double Balanced Mixer Oscillator	Philips	Philips	NE/SA602A
Miscellaneous							
3			SMA1, SMA2, SMA3	SMA right angle jack receptacle	Newark	EF Johnson	142-0701-301
1			J1	Male 6-pins connector	STOCKO	STOCKO	MKS1956-6-0-606
1			J2	Male 2-pins connector	STOCKO	STOCKO	MKS1851-6-0-202
1			JP1	Test point	Digikey	3M	929647-36
1				Printed circuit board	Philips	Philips	SA7025/8025-M
75 Total Parts							

Dual low-power frequency synthesizer UMA1005T

FEATURES

- Fast locking by 'Fractional-N' divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High-speed serial input
- Low-power consumption
- Programmable charge pump currents
- Supply voltage range 2.9 to 5.5 V.

APPLICATIONS

- Mobile telephony
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1005T is a low-power, high-performance dual frequency synthesizer fabricated in CMOS technology. Fractional-N division with selectable modulo 5 or 8 is implemented in the main synthesizer.

The detectors and charge pumps are designated to achieve 10 to 5000 kHz channel spacing using fractional-N decreases the channel spacing by a factor 5 or 8. Together with an external standard 2, 3 or 4 ratio prescaler the main synthesizer can operate in the GHz frequency range.

Channel selection and programming is realized by a high-speed 3-wire serial interface.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1005T	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

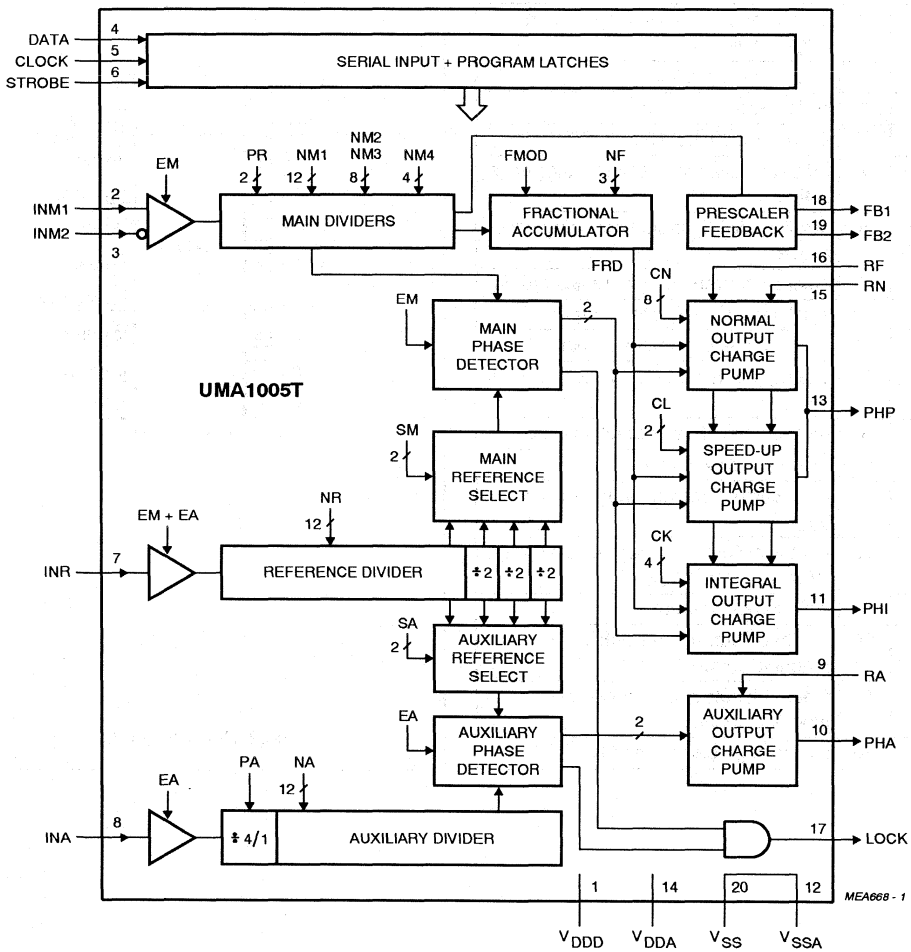


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDD}	1	digital supply voltage
INM1	2	main divider positive input; rising edge active
INM2	3	main divider negative input; falling edge active
DATA	4	serial data input line
CLOCK	5	serial clock input line
STROBE	6	serial strobe input line
INR	7	reference divider input line; rising edge active
INA	8	auxiliary divider input line; rising edge active
RA	9	auxiliary current setting; resistor to V_{SS}
PHA	10	auxiliary phase detector output
PHI	11	integral phase detector output
V_{SSA}	12	analog ground; internally connected to V_{SS}
PHP	13	proportional phase detector output
V_{DDA}	14	analog supply voltage
RN	15	main current setting input; resistor to V_{SS}
RF	16	fractional compensation current setting input; resistor to V_{SS}
LOCK	17	lock detector output
FB1	18	feedback output 1 for prescaler modulus control
FB2	19	feedback output 2 for prescaler modulus control
V_{SS}	20	common ground connection

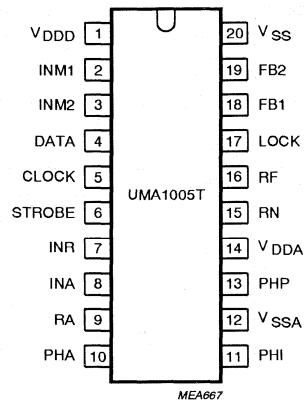


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Serial programming input

The serial input is a 3-wire input (CLOCK, STROBE and DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32-bit words. Each word includes 1 or 4 address bits. Figure 3 shows the timing diagram of the serial input. When the STROBE = LOW, the clock driver is enabled and on the positive edges of the CLOCK the signal on the DATA input is clocked into a shift register. When the STROBE = HIGH, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent:

1. D word.
2. C word.
3. B word.
4. A word.

Figure 4 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for NM4, CN and PR is stored by the B word temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24-bit A0 word is used. CN will be directly loaded by programming a long 32-bit A1 word. The flag LONG in the D word determines whether A0 (LONG = 0) or A1 (LONG = 1) format is applicable.

The A word contains new data for the main divider. The A word is loaded only when a main divider synchronization signal is also active, to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. It disables the loading of the A word each main divider cycle during maximum 300 main divider input cycles. To make sure that the A word will be correctly loaded the STROBE signal must be HIGH for at least 300 main divider input cycles. Programming the A word also means that the main charge pumps on outputs PHP and PHI are set into the speed-up mode as long as the STROBE remains HIGH.

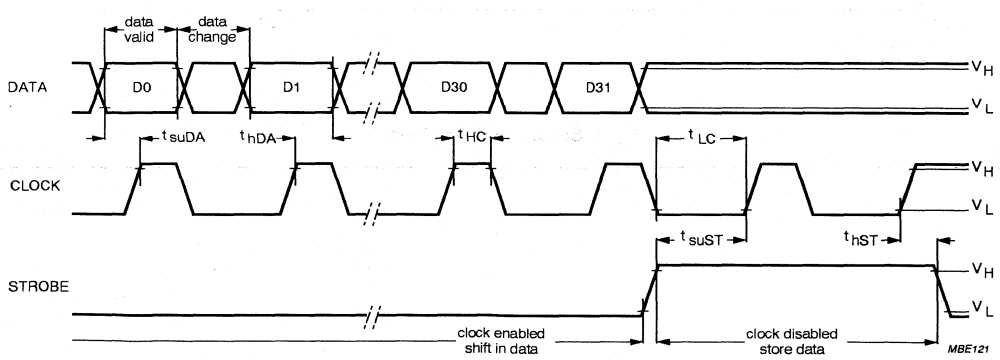


Fig.3 Serial input timing sequence.

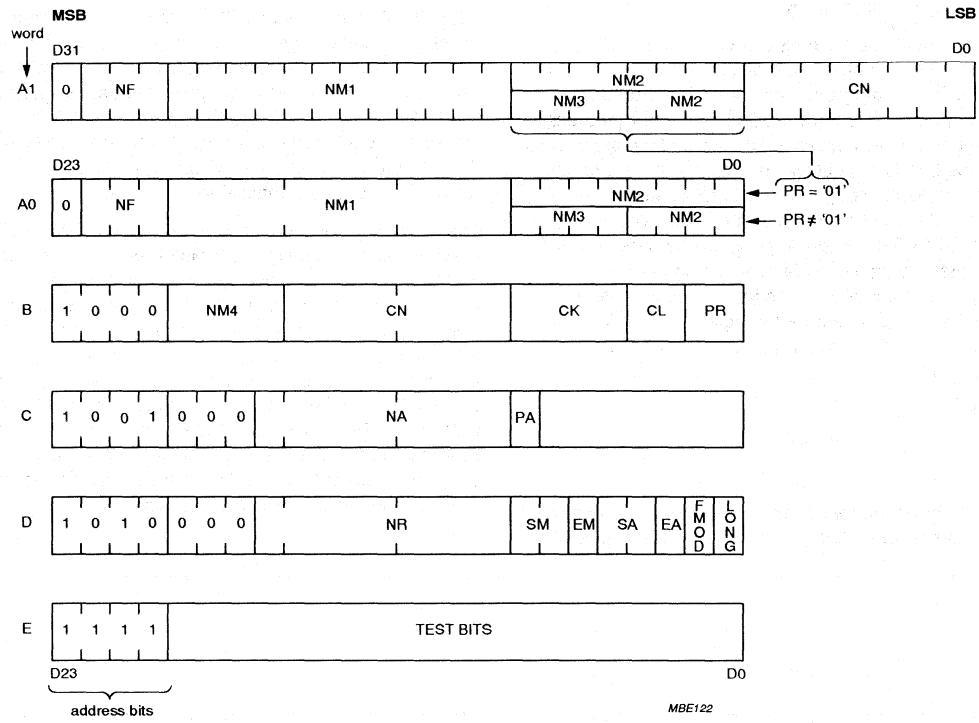


Fig.4 Serial input word format.

Table 1 Description of symbols used in Fig.4

SYMBOL	BITS[1]	FUNCTION
NM1	12	number of main divider cycles when prescaler is programmed in ratio R1 (FB1 = 1; FB2 = 0); note 2
NM2	8 if PR = 01 4 if PR ≠ 01	number of main divider cycles when prescaler is programmed in ratio R2 (FB1 = 0; FB2 = 0); note 2
NM3	4 if PR = 1X	number of main divider cycles when prescaler is programmed in ratio R3 (FB1 = 0; FB2 = 1); note 2
NM4	4 if PR = 11 or 00	number of main divider cycles when prescaler is programmed in ratio R4 (FB1 = 1; FB2 = 1); note 2
PR	2	prescaler type in use: PR = 01; modulus 2 prescaler PR = 10; modulus 3 prescaler PR = 11; modulus 4 prescaler PR = 00; modulus 4 prescaler (inhibit ratio 3)
NF	3	fractional-N increment
FMOD	1	fraction-N modulus selection flag: 1 = modulo 8 0 = modulo 5
LONG	1	A word format selection flag: 0 = 24-bit A0 format 1 = 32-bit A1 format
CN	8	binary current setting factor for main charge pumps
CL	2	binary acceleration factor for proportional charge pump current
CK	4	binary acceleration factor for integral charge pump current
EM	1	main divider enable flag
EA	1	auxiliary divider enable flag
SM	2	reference select for main phase detector
SA	2	reference select for auxiliary phase detector
NR	9	reference divider ratio
NA	9	auxiliary divider ratio
PA	1	auxiliary prescaler mode: PA = 0; divide-by-4 PA = 1; divide-by-1

Notes

1. X = don't care.
2. Not including reset cycles and fractional-N effects.

Auxiliary variable divider

The input signal on INA is amplified to a logic level by a single ended input buffer, which accepts LOW level AC coupled input signals. This input stage is enabled if the serial control bit EA = 1. Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = 0. This divider has been optimized to accept a high-frequency (90 MHz at a supply voltage range of 4.75 to 5.5 V) input signal. If PA = 1 this divider is disabled and the input signal is fed directly to the second

stage, which is a 9-bit programmable divider with standard input frequency (30 MHz). The division ratio can be expressed as:

If PA = 0; N = 4 × NA.

If PA = 1; N = NA; with NA = 4 to 511.

Reference variable divider (Fig.5)

The input signal on INR is amplified to a logic level by a single ended input buffer, which accepts LOW level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 511) followed by a 3-bit binary counter. The 2-bit SM determines which of the 4 output pulses is selected as main phase detector input. The 2-bit SA determines the selection of the auxiliary phase detector signal. To obtain the best time spacing for the main and auxiliary reference signals, the opposite output will be used for the auxiliary phase detector, reducing the possibility of unwanted interactions. For this reason the programmable divider produces a symmetric output pulse for even ratios and a 1 input cycle asymmetric pulse for odd ratios.

Main variable divider

The input signals on INM1 and INM2 are amplified to a logic level by a balanced input comparator giving a common mode rejection. This input stage is enabled when serial control bit EM = 1. Disabling means that all currents in the comparator are switched off. The main divider is built-up by a 12-bit counter plus a sign bit. Depending on the serial input values of NM1, NM2, NM3, NM4 and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles in accordance with the information in Table 2.

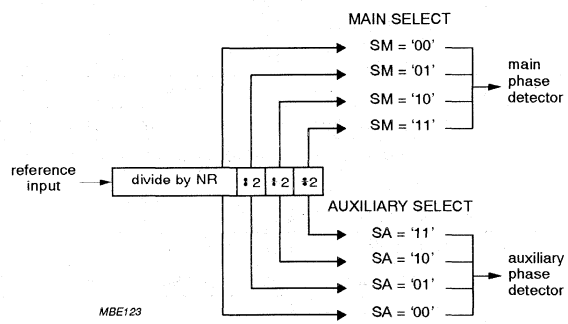


Fig.5 Reference variable divider.

Table 2 Selection of prescaler ratio

COUNTER STATUS	FB1	FB2	PRESCALER RATIO[1]
(–NM1 – 1) to 0	1	0	R1
(–NM1 – 1) to –1	1	0	R1[2]
1 to NM2	0	0	R2
0 to NM2	0	0	R2[2]
0 to NM3	0	1	R3; if PR = 1X
0 to NM4	1	1	R4; if PR = 11 or 00

Notes

1. X = don't care.
2. When the fractional accumulator overflows.

The total division ratio from prescaler to the phase detector expressions are given in Table 3.

The loading of the work registers NM1, NM2, NM3, NM4 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as is explained in Section "Serial programming input".

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = 1. Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider cycles will then be: $NQ = N + \frac{NF}{Q}$

Programming a fraction means the prescaler with main divider will divide by N or N + 1.

The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

Phase detectors (Fig.6)

The auxiliary and main phase detectors are a 2 D-type flip-flop phase and frequency detector. The flip-flops are set by the negative edges of output signals of the dividers. The reset inputs are activated when both flip-flops have been set and when the reset enable signal is active (LOW). Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or dead band around zero phase error. The flip-flops drive on-chip charge pumps. A pull-up current from the charge pump indicates that the VCO frequency shall be increased while a pull-down pulse indicates that the VCO frequency shall be decreased.

Current settings

The UMA1005T has 3 current setting pins RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current in the current setting pins. This current I_R can be set by an external resistor to be connected between the current setting pin (pin 9) and V_{SS}. The typical value for R (current setting resistor) can be calculated with the equation:

$$R = \frac{(V_{DDA} - 0.5) - 237\sqrt{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary output charge pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor (R_{ext}) at pin RA. The active charge pump current is typically: $|I_{PHA}| = 8 \times I_{RA}$.

Main output charge pumps and fractional compensation currents

The main charge pumps on pins PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 7 shows the waveforms for a typical case.

When the serial input A word is loaded, the output circuits are in the 'speed-up mode' as long as the STROBE is HIGH, else the 'normal mode' is active.

NORMAL MODE

In the 'normal mode' the current output at PHP is: $I_{PHP(N)} = I_{pump10} + I_{comp10}$.

Where:

$$|I_{pump10}| = \frac{CN \times I_{RN}}{29}$$; charge pump current.

$$I_{comp10} = \frac{FRD \times I_{RF}}{128}$$; fractional compensation current.

In 'normal mode' the current at output PHI is zero.

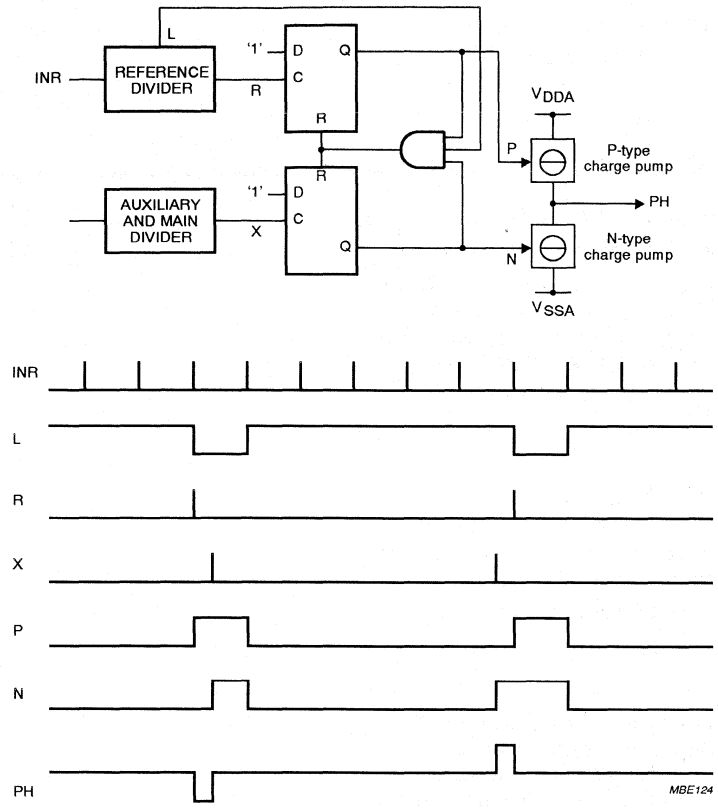


Fig.6 Phase detector structure with timing.

SPEED-UP MODE

In 'speed-up mode' the current in output PHP is:
$I_{PHP(S)} = I_{PHP(N)} + I_{pump11} + I_{comp11}$.

Where:

$I_{pump11} = I_{pump10} \times 2^{(CL+1)}$; charge pump current.

$I_{comp11} = I_{comp10} \times 2^{(CL+1)}$; fractional compensation current.

In 'speed-up mode' the current in output PHI is:
$I_{PHI(S)} = I_{pump21} + I_{comp21}$.

Where:

$I_{pump21} = I_{pump11} \times CK$; charge pump current.

$I_{comp21} = I_{comp11} \times CK$; fractional compensation current.

Figure 7 shows that for a proper fractional compensation the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output. This means that the current setting on the inputs RN and RF must have following ratio: $\frac{I_{RN}}{I_{RF}} = \frac{29 \times Q \times f_{VCO}}{64 \times CN \times f_{i(max)2}}$.

Where:

Q = fractional-N modulus.

$f_{VCO} = f_{i(max)1} \times N$; input frequency of the prescaler.

$f_{i(max)1}$ = maximum input frequency of the main divider (pins INM1 and INM2).

$f_{i(max)2}$ = maximum input frequency of the reference divider (pin INR).

Lock detect

The output LOCK is HIGH when the auxiliary phase detector and the main phase detector indicate a lock condition. The lock condition is defined as a phase difference of less than ±1 cycle on the reference input INR. The lock condition is also fulfilled when the relative counter is disabled (EM = 0 or EA = 0 respectively) for the main or auxiliary counter respectively.

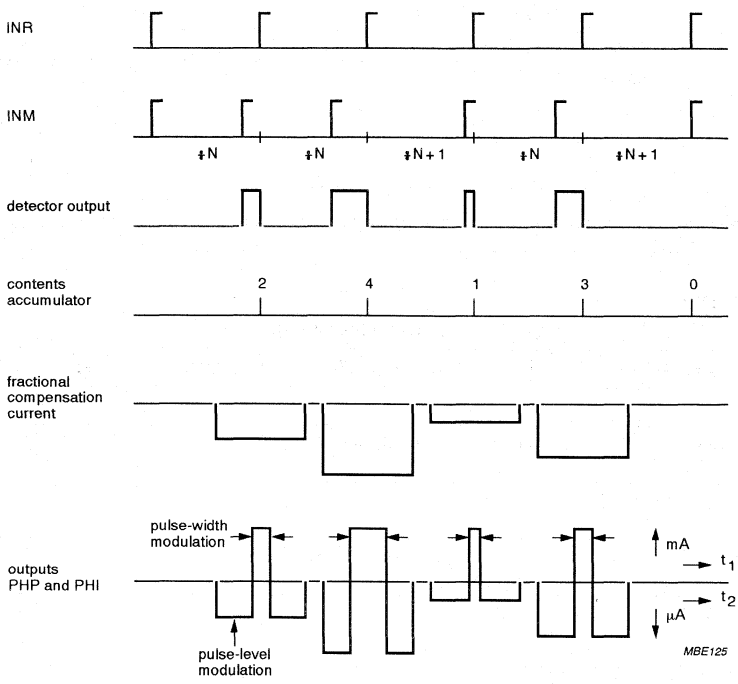


Fig.7 Waveforms for NF = 2 and fraction = 0.4.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	−0.5	6.5	V
V_{DDA}	analog supply voltage	−0.5	6.5	V
V_I	voltage on any input	−0.5	V_{DD} + 0.5	V
I_n	DC current into any input or output	−10	+10	mA
P_{tot}	total power dissipation	−	25	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+70	°C

DC CHARACTERISTICS

$V_{DDD} = V_{DDA}$ = 2.9 to 5.5 V; T_{amb} = −40 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$I_{DDD(stb)}$	digital standby supply current	EM = EA = 0; inputs on V_{DD} or 0	−	−	5	μA
I_{DDD}	operating digital supply current	note 1	−	−	5	mA
$I_{DDA(stb)}$	analog standby supply current	$V_{RA} = V_{DDA}$; $V_{RF} = V_{DDA}$; $V_{RN} = V_{DDA}$	−	−	10	μA
I_{DDA}	operating analog supply current	note 1	−	−	0.6	mA
Digital inputs CLK, DATA and STROBE						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
Digital outputs FB1, FB2 and LOCK						
V_{OL}	LOW level output voltage	I_O = 2 mA; note 2	−	−	0.4	V
V_{OH}	HIGH level output voltage	I_O = −2 mA; note 2	V_{DD} − 0.4	−	−	V
Charge pump PHA						
$\lvert I_{PHA} \rvert$	output current	I_{RA} = −62.5 μA; $V_{PHA} = \frac{1}{2}V_{DD}$; note 2	400	500	600	μA
		I_{RA} = −25 μA; $V_{PHA} = \frac{1}{2}V_{DD}$	160	200	240	μA
$\frac{\Delta I_{PHA}}{\lvert I_{PHA} \rvert}$	relative output current variation	I_{RA} = −62.5 μA; notes 2 and 3	−	2	6	%
$\Delta I_{PHA\,M}$	output current matching	I_{RA} = −62.5 μA; $V_{PHA} = \frac{1}{2}V_{DD}$; notes 2 and 4	−	−	±50	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump PHP; normal mode (notes 5, 6 and 7); $V_{RF} = V_{DD}$						
$\lvert I_{PHP(N)} \rvert$	output current	I_{RN} = −62.5 μA; $V_{PHP} = \frac{1}{2}V_{DD}$; note 2	440	550	660	μA
		I_{RN} = −25 μA; $V_{PHP} = \frac{1}{2}V_{DD}$	175	220	265	μA
$\Delta I_{PHP(N)}$	relative output current variation	I_{RN} = −62.5 μA; note 3	–	2	6	%
$\Delta I_{PHP(N\ M)}$	output current matching	I_{RN} = −62.5 μA; $V_{PHP} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±50	μA
Charge pump PHP; speed-up mode (notes 5, 6 and 8); $V_{RF} = V_{DD}$						
$\lvert I_{PHP(S)} \rvert$	output current	I_{RN} = −62.5 μA; $V_{PHP} = \frac{1}{2}V_{DD}$; note 2	2.20	2.75	3.30	mA
		I_{RN} = −25 μA; $V_{PHP} = \frac{1}{2}V_{DD}$	0.85	1.1	1.35	mA
$\Delta I_{PHP(S)}$	relative output current variation	I_{RN} = −62.5 μA; notes 2 and 3	–	2	6	%
$\Delta I_{PHP(S\ M)}$	output current matching	I_{RN} = −62.5 μA; $V_{PHP} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±250	μA
Charge pump PHI; speed-up mode (notes 5, 6 and 9); $V_{RF} = V_{DD}$						
$\lvert I_{PHI(S)} \rvert$	output current	I_{RN} = −62.5 μA; $V_{PHI} = \frac{1}{2}V_{DD}$; note 2	4.4	5.5	6.6	mA
		I_{RN} = −25 μA; $V_{PHI} = \frac{1}{2}V_{DD}$	1.75	2.2	2.65	mA
$\Delta I_{PHI(S)}$	relative output current variation	I_{RN} = −62.5 μA; notes 2 and 3	–	2	8	%
$\Delta I_{PHI(S\ M)}$	output current matching	I_{RN} = −62.5 μA; $V_{PHI} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±500	μA
Fractional compensation PHP; normal mode (notes 5, 10 and 11); $V_{RN} = V_{DD}$; $V_{PHP} = \frac{1}{2}V_{DD}$						
$I_{PHP(F\ N)}$	fractional compensation output current PHP as a function of FRD	I_{RF} = −62.5 μA; FRD = 1 to 7; notes 2 and 12	−675	−500	−325	nA
		I_{RF} = −25 μA; FRD = 1 to 7; note 12	−270	−200	−130	nA
Fractional compensation PHP; speed-up mode (notes 5, 11 and 13); $V_{RN} = V_{DD}$; $V_{PHP} = \frac{1}{2}V_{DD}$						
$I_{PHP(F\ S)}$	fractional compensation output current PHP as a function of FRD	I_{RN} = −62.5 μA; FRD = 1 to 7; notes 2 and 12	−3.35	−2.50	−1.65	μA
		I_{RN} = −25 μA; FRD = 1 to 7; note 12	−1.35	−1.00	−0.65	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fractional compensation PHI; speed-up mode (notes 5, 11 and 14); $V_{RN} = V_{DD}$; $V_{PHP} = \frac{1}{2}V_{DD}$						
$I_{PHI(F)}$	fractional compensation output current PHI as a function of FRD	I_{RN} = −62.5 μA; FRD = 1 to 7; notes 2 and 12	−5.4	−4.0	−2.6	μA
		I_{RN} = −25 μA; FRD = 1 to 7; note 12	−2.15	−1.60	−1.05	μA
Charge pump leakage currents; charge pump not active						
$I_{PHP(LO)}$	output leakage current PHP	normal mode; V_{PHP} = 0.7 to V_{DDA} − 0.8 V note 5	−	10	750	nA
$I_{PHI(LO)}$	output leakage current PHI	normal mode; V_{PHI} = 0.7 to V_{DDA} − 0.8 V note 5	−	10	100	nA
$I_{PHA(LO)}$	output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} − 0.8 V	−	10	750	nA

Notes

1. Operational conditions:
   a) Main and auxiliary divider enabled (EM = EA = 1).
   b) NA = 125.
   c) NR = 125.
   d) NM1 = 60.
   e) NM2 = 63.
   f) $f_{i(max)1} = f_{i(max)2}$ = 15 MHz.
   g) $f_{i(max)3}$ = 60 MHz.
   h) Lock condition.
   i) Normal mode; note 5
   j) $I_{RN} = I_{RF} = I_{RA}$ = 25 μA.
   k) CN = 255.
   l) PA = 0.
2. Limited supply voltage range 4.5 to 5.5 V.
3. The relative output current variation is defined as:
   $\frac{\Delta I_O}{I_O} = 2 \times \frac{I_2 - I_1}{|I_2 + I_1|}$; with V_1 = 0.7 V; $V_2 = V_{DD}$ − 0.8 V (see Fig.8).
4. The output current matching is measured when both (positive and negative current) sections of the output charge pumps are on.
5. When a serial 'A' word is programmed, the main charge pumps on PHP and PHI are in the 'speed-up mode' as long as STROBE = HIGH, otherwise the main charge pumps are in the 'normal mode'.
6. Monotonicity is guaranteed with CN = 0 to 255.
7. Typical output current: $|I_{PHP(N)}| = -I_{RN} \times \frac{CN}{29}$; specification condition: CN = 255.

8. Typical output current: $|I_{PHP(S)}| = -I_{RN} \times CN \times \frac{2^{(CL+1)}+1}{29}$; specification conditions:
   a) CN = 255; CL = 1 or,
   b) CN = 75; CL = 3.
9. Typical output current: $|I_{PHI}| = -I_{RN} \times CN \times 2^{(CL+1)} \times \frac{CK}{29}$; specification conditions:
   a) CN = 160; CL = 3; CK = 1 or,
   b) CN = 160; CL = 2; CK = 2 or,
   c) CN = 160; CL = 1; CK = 4 or,
   d) CN = 160; CL = 0; CK = 8.
10. Typical fractional compensation output current: $I_{PHP(FN)} = I_{RF} \times \frac{FRD}{128}$; specification condition: FRD = 1 to 7.
11. The compensation current specified does not include the leakage current of this output.
12. FRD is the value of the 3-bit fractional accumulator.
13. Typical fractional compensation output current: $I_{PHP(FS)} = I_{RF} \times FRD \times \frac{2^{(CL+1)}+1}{128}$; specification conditions: FRD = 1 to 7; CL = 1.
14. Typical fractional compensation output current: $I_{PHI(F)} = I_{RF} \times FRD \times 2^{(CL+1)} \times \frac{CK}{128}$; specification conditions:
   a) FRD = 1 to 7; CL = 1; CK = 2 or,
   b) FRD = 1 to 7; CL = 2; CK = 1.

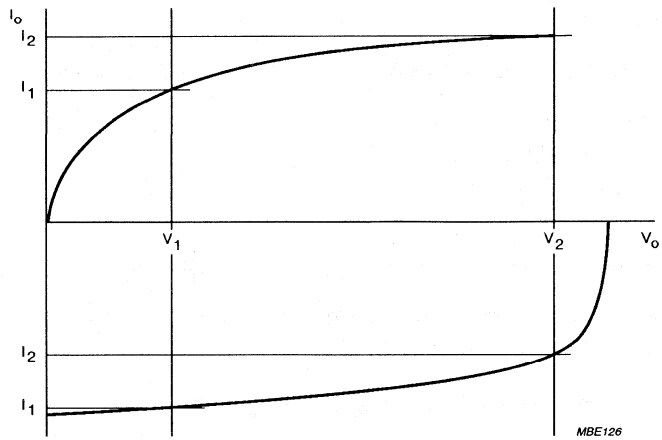


Fig.8 Relative output current variation.

AC CHARACTERISTICS

$V_{DDD} = V_{DDA} = 2.9$ to 5.5 V; $T_{amb} = -40$ to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main divider (inputs INM1 and INM2)						
$f_{i(max)1}$	maximum input frequency		10	–	–	MHz
		note 1	30	–	–	MHz
$\Delta V_{INM(p-p)}$	differential input signal amplitude $V_{INM1} - V_{INM2}$ (peak-to-peak value)		600	–	–	mV
V_{CM}	common mode range for V_{INM1} and V_{INM2}		1	–	$V_{DD} - 1$	V
t_{pd}	propagation delay time from I_{NM1} and I_{NM2} to FB1 and FB2		–	–	60	ns
		note 1	–	18	30	ns
msr	mark-to-space ratio for differential input signals		35 : 65	–	65 : 35	
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference divider (input INR)						
$f_{i(max)2}$	maximum input frequency		15	–	–	MHz
		note 1	30	–	–	MHz
$V_{i(p-p)}$	input signal amplitude AC coupled (peak-to-peak value)		300	–	–	mV
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF
Auxiliary divider (input INA)						
$f_{i(max)3}$	maximum input frequency	prescaler enabled; PA = 0	35	–	–	MHz
		prescaler enabled; PA = 0; note 1	90	–	–	MHz
		prescaler disabled; PA = 1	15	–	–	MHz
		prescaler disabled; PA = 1; note 1	30	–	–	MHz
$V_{i(p-p)}$	input signal amplitude AC coupled (peak-to-peak value)		300	–	–	mV
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF
Serial interface (inputs DATA, CLOCK and STROBE); see Fig.3						
f_{clk}	clock frequency		–	–	10	MHz
t_{HC}	clock HIGH time		30	–	–	ns
t_{LC}	clock LOW time		30	–	–	ns
t_{suDA}	DATA set-up time		30	–	–	ns
t_{hDA}	DATA hold time		30	–	–	ns
t_{suST}	STROBE set-up time		30	–	–	ns
t_{hST}	STROBE hold time		30	–	–	ns

Notes

1. Limited supply voltage range 4.5 to 5.5 V.
2. Periodically sampled; not 100% tested.

Low-power frequency synthesizer for mobile radio communications

UMA1014

FEATURES

- Single chip synthesizer; compatible with Philips cellular radio chipset
- Fully programmable RF divider
- I^2C interface for two-line serial bus
- On-chip crystal oscillator/TCXO buffer from 3 to 16 MHz
- 16 reference division ratios allowing 5 to 100 kHz channel spacing
- 1/8 crystal frequency output
- On-chip out-of-lock indication
- Two extra VCO control outputs
- Latched synthesizer alarm output
- Status register including out-of-lock indication and power failure
- Power-down mode.

APPLICATIONS

- Cellular mobile radio (NMT, AMPS, TACS)
- Private mobile radio (PMR)
- Cordless telephones.

GENERAL DESCRIPTION

The UMA1014 is a low-power universal synthesizer which has been designed for use in channelized radio communication. The IC is manufactured in bipolar technology and is designed to operate at 5 to 100 kHz channel spacing with an RF input from 50 to 1100 MHz. The channel is programmed via a standard I^2C-bus. A low-power sensitive RF divider is incorporated together with a dead-zone eliminated, 3-state phase comparator. The low-noise charge pump delivers 1 mA or 1/2 mA output current to enable a better compromise between fast switching and loop bandwidth. A power-down circuit enables the synthesizer to be set to idle mode.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{CP}	supply voltage range	4.5	5.0	5.5	V
$I_{CC} + I_{CP}$	supply current	–	13	–	mA
I_{CCpd}	I_{CC} in power-down	–	2.5	–	mA
f_{ref}	phase comparator reference frequency	5	–	100	kHz
f_{RF}	RF input frequency	50	–	1100	MHz
T_{amb}	operating ambient temperature range	−40	–	85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1014T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

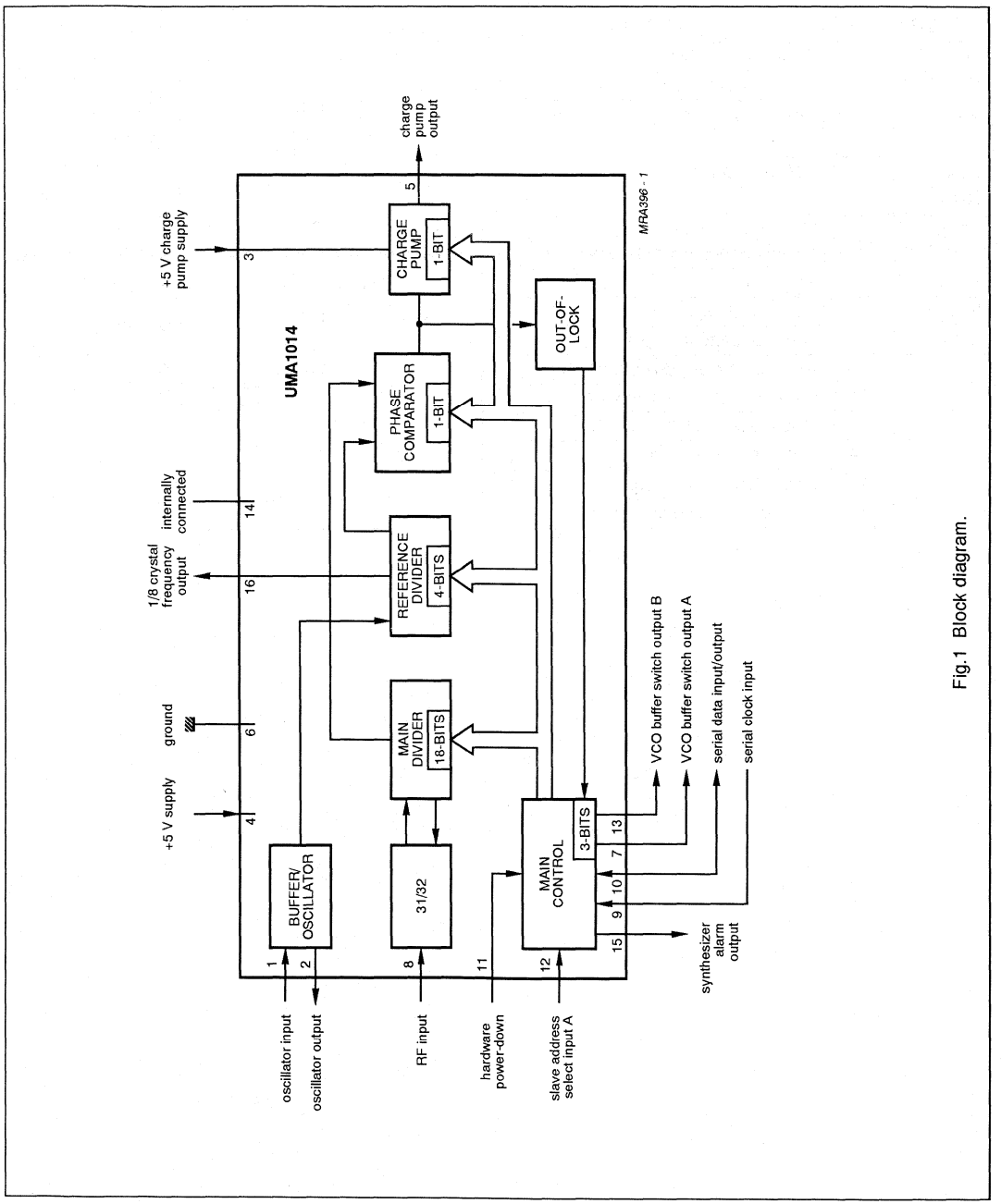


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCIN	1	oscillator or TCXO input
OSCOUT	2	oscillator output
V_{CP}	3	5 V charge pump supply
V_{CC}	4	5 V supply
PCD	5	charge pump output
GND	6	ground
VCOA	7	VCO buffer switch output A (including out-of-lock)
RF	8	RF input
SCL	9	serial clock input
SDA	10	serial data input/output
$\overline{HPD}$	11	hardware power-down (active LOW)
SAA	12	slave address select input A
VCOB	13	VCO buffer switch output B
i.c.	14	internally connected
SYA	15	synthesizer alarm output
FX8	16	1/8 crystal frequency output

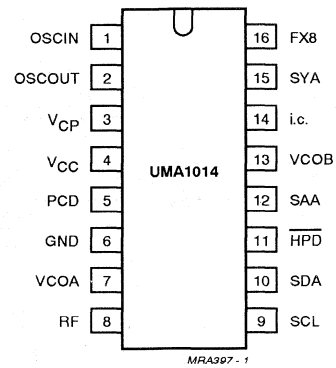


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The UMA1014 is a low-power frequency synthesizer for radio communication which operates in the 50 to 1100 MHz range. The device includes an oscillator/buffer circuit, a reference divider, an RF divider, a 3-state phase comparator, a charge pump and a main control circuit to transfer the serial data into the four internal 8-bit registers. The V_{CC} supply feeds the logic part, the V_{CP} supply feeds the charge-pump only. Both supplies are +5 V (±10%). The power-down facility puts the synthesizer in the idle mode (all current supplies are switched off except in the control part). This allows any I²C transfer and all information in the registers is retained thus enabling fast power-up.

Main divider

The main divider is a pulse swallow type counter which is fully programmable. After a sensitive input amplifier (50 mV, –13 dBm), the RF signal is applied to a 31/32 duo-modulus counter. The output is then used as the clock for the 5-bit swallow counter R = (MD4 to MD0) and the 13-bit main counter N = (MD17 to MD5). The ratio is transferred via the I²C-bus to the registers B, C and D, and then buffered in an 18-bit latch. The ratio in the divider chain is updated with the new information when the least significant bit is received (i.e. D0). This update is synchronized to the output of the divider in order to limit the phase error during small jumps of the synthesized frequency.

The main divider can be programmed to any value between 2048 and 262143 (i.e. 2^{18} –1). If ratio X, below 2048, is sent to the divider, the ratio (X + 2048) will be programmed. When it is required to switch between adjacent channels it is possible to program register D only, thus allowing shorter I²C programming time.

Oscillator

The oscillator is a common collector Colpitts type with external capacitive feedback. The oscillator has very small temperature drift and high voltage supply rejection. A TCXO or other type of clock can be used to drive the oscillator by connecting the source (preferably AC-coupled) to pin 1 and leaving pin 2 open-circuit. The oscillator acts as a buffer in this mode and requires no additional external components. The signal from the clock source should have a minimum space width of 31 ns.

Reference divider

The reference divider is semi-programmable with 16 division ratios which can be selected via the I²C-bus. The programming uses four bits of the register A (A3 to A0) as listed in Table 2. These ratios allow the use of a large number of crystal frequencies from 3 MHz up to 16 MHz. All main channel spacings can be obtained with a single crystal/TXCO frequency of 9.6 MHz.

Phase comparator

A diagram of the phase comparator and charge pump is illustrated in Fig.3.

The phase comparator is both a phase and frequency detector. The detector comprises dual flip-flops together with logic circuitry to eliminate the dead-zone. When a phase error is detected the UP or DOWN signal goes HIGH. This switches on the corresponding current generator which produces a source or sink current for the loop filter. When no phase error is detected PCD goes high impedance. The final tuning voltage for the VCO is provided by the loop filter. The charge pump current is programmable via the I²C-bus. When IPCD (bit 5) is set to logic 1 the charge pump delivers 1 mA; when IPCD is set to logic 0 the charge pump delivers 0.5 mA.

The phase comparator has a phase inverter logic input (PHI). This allows the use of inverted or non-inverted loop filter configurations. It is thus possible to use a passive loop filter which offers higher performances without an operational amplifier. The function of the phase comparator is given in Table 3 and a typical transfer curve is illustrated in Fig.4.

Out-of-lock detector

An out-of-lock detector using the UP and DOWN signals from the phase comparator is included on-chip. The pin VCOA is an open collector output which is forced LOW during an out-of-lock condition. The same information is also available via the I²C-bus in the status register (bit OOL). When the phase error (measured at the phase comparator) is greater than approximately 200 ns, an out-of-lock condition is immediately flagged. The flag is only released after 6 reference cycles when the phase error is less than 200 ns.

Table 1 Division ratio in the main divider

MAIN COUNTER: N								SWALLOW COUNTER: R		
MD17	MD16	MD15	...	MD8	MD7	...	MD5	MD4	...	MD0
B1	B0	C7	...	C0	D7	...	D5	D4	...	D0
MSB										LSB

Table 2 Reference divider programming

A3(RD3)	A2(RD2)	A1(RD1)	A0(RD0)	REFERENCE DIVISION RATIO	CHANNEL SPACING FOR 9.6 MHz AT OSCIN
0	0	0	0	128	75 kHz
0	0	0	1	160	60 kHz
0	0	1	0	192	50 kHz
0	0	1	1	240	40 kHz
0	1	0	0	256	37.5 kHz
0	1	0	1	320	30 kHz
0	1	1	0	384	25 kHz
0	1	1	1	480	20 kHz
1	0	0	0	512	18.75 kHz
1	0	0	1	640	15 kHz
1	0	1	0	768	12.5 kHz
1	0	1	1	960	10 kHz
1	1	0	0	1024	9.375 kHz
1	1	0	1	1280	7.5 kHz
1	1	1	0	1536	6.25 kHz
1	1	1	1	1920	5 kHz

Table 3 Operation of the phase comparator

	PHI = 0 (PASSIVE LOOP FILTER)			PHI = 1 (ACTIVE LOOP FILTER)		
	$f_{ref} < f_{var}$	$f_{ref} > f_{var}$	$f_{ref} = f_{var}$	$f_{ref} < f_{var}$	$f_{ref} > f_{var}$	$f_{ref} = f_{var}$
UP	0	1	0	1	0	0
DOWN	1	0	0	0	1	0
I_{pcd}	−1 mA	1 mA	< ±5 nA	1 mA	−1 mA	< ±5 nA

MAIN CONTROL

The control part consists mainly of the I²C-bus control interface and a set of four registers A, B, C and D. The serial input data (SDA) is converted into 8-bit parallel words and stored in the appropriate registers. The data transmission to the synthesizer is executed in the burst mode with the following format:

//slave addr./subaddr./data1/data2/.../datan//; n up to 4

Data byte 1 is written in the register indicated by the subaddress. An auto-increment circuit, if enabled (AVI = 1), then provides the correct addressing for the ensuing data bytes. Since the length of the data burst is not fixed, it is possible to program only one register or the whole set. The registers are structured in such a way so that the burst, for normal operation, is kept as short as possible. The bits that are only programmed during the set-up (reference division ratio, power-down, phase inversion and current on PCD) are stored in registers A and B.

In the slave address six bits are fixed, the remaining two bits depend on the application.

Table 4 Slave address

1	1	0	0	0	1	$\overline{SAA}$	R/$\overline{W}$

SAA is the slave address. When SAA goes HIGH then $\overline{SAA}$ = 0, when SAA goes LOW then $\overline{SAA}$ = 1. This allows the use of two UMA1014s on the same bus but using a different address. R/$\overline{W}$ should be set to logic 0 when writing to the synthesizer or set to logic 1 when reading the status register.

The subaddress includes the register pointer, and sets the two flags related to the auto-increment (AVI) and the alarm disable (DI).

Table 5 Subaddress

X	X	X	DI	AVI	X	SB1	SB0

Where:

X = not used

DI (Disable Interrupt):
DI = 1 disables the alarm on SYA
DI = 0 enables the alarm.

AVI (Auto Value Increment):
AVI = 1 enables the automatic increment
AVI = 0 disables the auto-increment.

SB1/SB0 are the pointers of the register where DATA1 will be written (see Table 6).

When the auto-increment is disabled (AVI = 0), the subaddress pointer will maintain the same value during the I²C-bus transfer. All the data bytes will then be written consecutively in the register pointed by the subaddress.

Table 6 Pointer of the registers

SB1	SB0	REGISTER POINTED
0	0	A
0	1	B
1	0	C
1	1	D

Status register and synthesizer alarm

When an out-of-lock condition or a power dip occurs, SYA, which is an open collector output, is forced LOW and latched. The pin SYA will be released after the status register is read via the I²C-bus.

The status register contains the following information:

Table 7 Status register

0	0	0	OOL	0	LOOL	LPD	DI

Where:

OOL = momentary out-of-lock
LOOL = latched out-of-lock
LPD = latched power dip
DI = disable interrupt (of the last write cycle).

The I²C-bus protocol to read this internal register is a single byte without subaddressing:

//slave address (R/$\overline{W}$ = 1)/status register (read)//

Table 8 Bit allocation

REGISTER	POINTER	BIT ALLOCATION								PRESET
		7	6	5	4	3	2	1	0	
A	00	PD	X	IPCD	X	RD3	RD2	RD1	RD0	00001110
B	01	1	0	1	PHI	VCOB	VCOA	MD17	MD16	10100101
C	10	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	00111000
D	11	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	10000000

Where X = not used

Table 9 Register allocation

REGISTER NAME	BIT NAME	FUNCTION		PRESET VALUE
A	PD	power down	PD = 0 normal operation	0
	IPCD	programmable charge pump current	IPCD = 1 = 1 mA; IPCD = 0 = 0.5 mA	0
	RD3...RD0	reference ratio	see Table 2	1110; r = 1536
B	PHI	phase inverter	PHI = 0 passive loop filter	0
	VCOA	VCO switch A	set pin 7	1
	VCOB	VCO switch B	set pin 13	0
	MD17, MD16	bits 17 and 16	MSB of main divider ratio	01
C	MD15 to MD8	bits 15 to 8	main divider ratio	00111000
D	MD7 to MD0	bits 7 to 0	main divider ratio	10000000; r = 80000

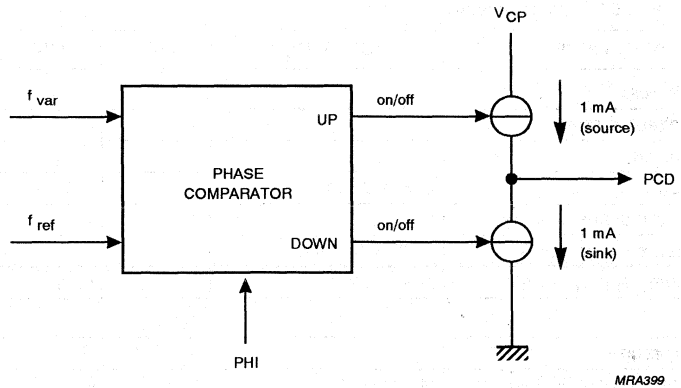


Fig.3 Phase comparator block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage range	−0.3	7.0	V
V_i	voltage range to ground (all pins)	0	V_{CC}	V
T_{stg}	IC storage temperature range	−55	+125	°C
T_{amb}	operating ambient temperature range	−40	+85	°C

HANDLING

Every pin referenced to ground withstands ESD (HMB) tests in accordance with MIL-STD-883C method 3015 class 2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling Integrated Circuits.

CHARACTERISTICS

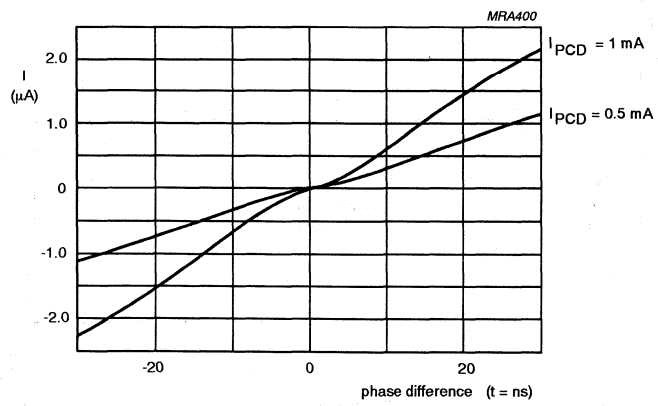
T_{amb} = 25 °C; V_{CC} = 4.5 to 5.5 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{CC} and V_{CP})						
V_{CC}	supply voltage range		4.5	–	5.5	V
I_{CC}	supply current		–	11.5	13.5	mA
I_{CCpd}	supply current	power-down	–	2.5	3.3	mA
V_{CP}	charge pump supply voltage		4.5	–	5.5	V
I_{CP}	charge pump supply current	IPCD = 0.5 mA	–	1.4	1.8	mA
I_{CPpd}	charge pump supply current	power-down	–	0.01	–	mA
RF dividers (pin RF)						
f_{RF}	frequency range		50	–	1100	MHz
$V_{RF(rms)}$	input voltage level (RMS value)	50 to 100 MHz	150	–	200	mV
		100 to 1100 MHz	50	–	150	mV
R_I	input resistance	at 1 GHz	–	200	–	Ω
		at 100 MHz	–	600	–	Ω
C_I	input capacitance	note 1	–	2.0	–	pF
R_{RF}	division ratios		2048	–	262143	–
Oscillator and reference divider (pins OSCIN and OSCOUT)						
f_{OSC}	oscillator frequency range		3	–	16	MHz
$V_{OSC(RMS)}$	input level sine wave (RMS value)		0.15	–	$V_{CC}/2.8$	V
$V_{OSC(p-p)}$	input level square wave (peak-to-peak value)		0.45	–	V_{CC}	V
t_{OSC_mk}	input mark width	see Fig.8	10	–	–	ns
t_{OSC_sp}	input space width		31	–	–	ns
Z_{OSC}	output impedance at pin OSCOUT		–	–	2	kΩ
R_{ref}	reference division ratio	see Table 1	128	–	1920	
1/8 crystal frequency (open collector output) (pin FX8)						
I_{OL}	LOW level output current	$V_{OL} \geq 0.6$ V	1.0	–	–	mA
Phase comparator (pin PCD)						
f_{PCD}	frequency range		5	–	100	kHz
I_{PCD}	output current	V_{PCD} = 2.5 V				
		bit IPCD = 1	0.9	1.2	1.4	mA
		bit IPCD = 0	0.45	0.6	0.75	mA
I_{PCDL}	output leakage current		–5	±1	+5	nA
V_{PCD}	output voltage		0.4	–	V_{CP}–0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock and serial data input (pins SCL and SDA)						
f_{CLK}	clock frequency		0	–	100	kHz
V_{IH}	HIGH level input voltage		3	–	–	V
V_{IL}	LOW level input voltage		–	–	1.5	V
I_{IH}	HIGH level input current		–	3	10	μA
I_{IL}	LOW level input current		−10	−5	–	μA
C_I	input capacitance		–	–	10	pF
I_{sink}	SDA sink current	V_{OL} = 0.4 V	3	–	–	mA
Slave address select input (pin SAA) and Hardware power-down input (pin HPDN)						
V_{IH}	HIGH level input voltage		3	–	–	V
V_{IL}	LOW level input voltage		–	–	0.4	V
I_{IH}	HIGH level input current		–	–	0.1	μA
I_{IL}	LOW level input current		−10	–	–	μA
VCO output switches (pins VCOA and VCOB) and synthesizer alarm (pin SYA); note2						
I_{OL}	LOW level sink current	$V_{OL} \geq 0.4$ V	400	–	–	μA

Notes

1. C_I is in parallel with R_I.
2. Pin VCOA is forced to logic 0 during out-of-lock condition.



The current I_{PCD} is averaged over a reference period of 24 μs.

Fig.4 Gain of phase detector and charge pump.

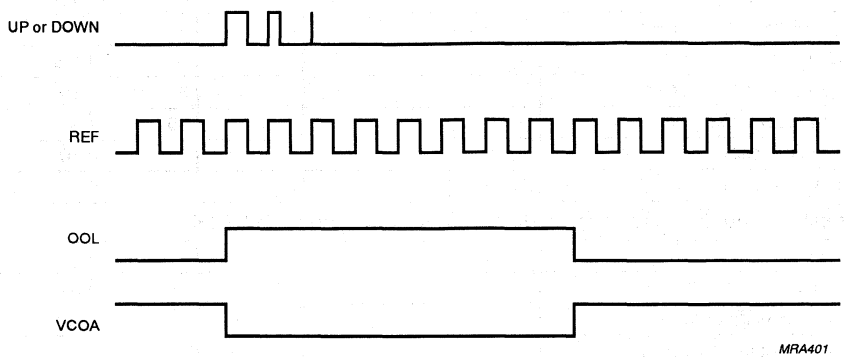


Fig.5 Out-of-lock function.

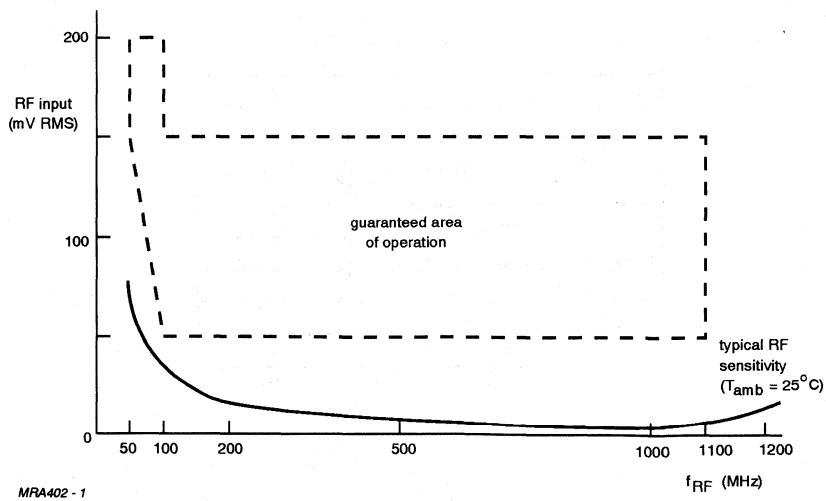


Fig.6 RF input high frequency sensitivity.

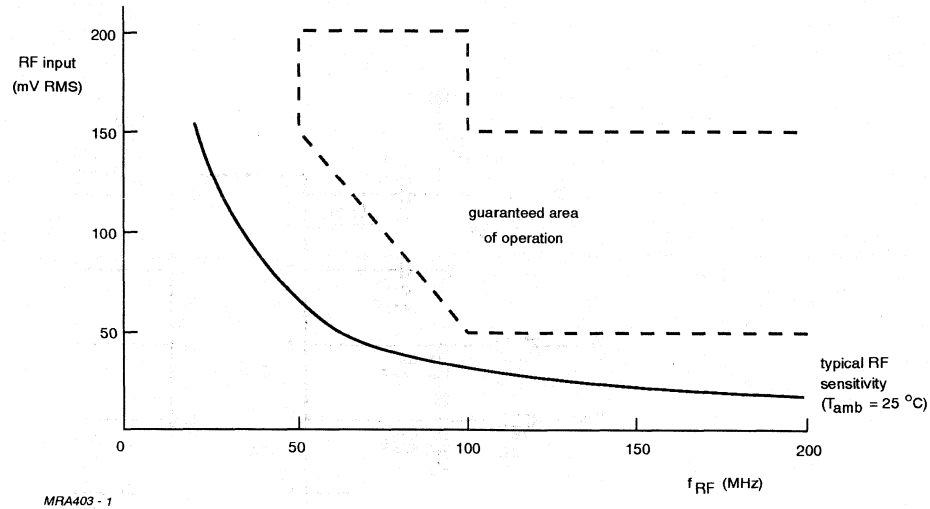


Fig.7 RF input low frequency sensitivity.

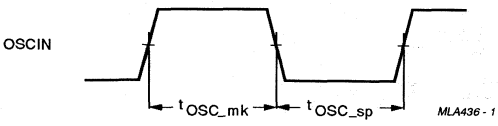
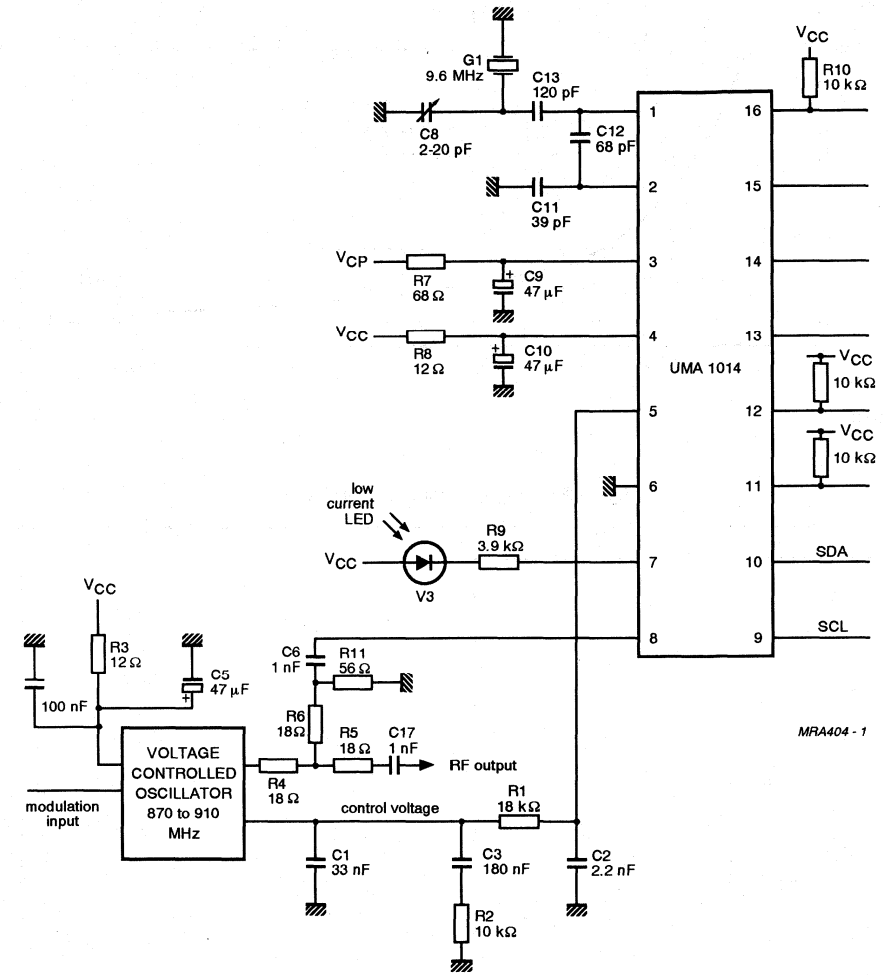


Fig.8 Oscillator input timing.

APPLICATION INFORMATION



ETACS application for:
V_{CO} sensitivity = 11 MHz/V.
Channel spacing = 12.5 kHz.

Fig.9 Typical cellular mobile radio application.

Application report for the UMA1014T frequency synthesizer

SCO/AN91004

1. INTRODUCTION

This application note is intended as a guide to designing a phase locked loop based on the Philips UMA1014T frequency synthesizer integrated circuit. The UMA1014T is a low power single chip solution to frequency synthesis in the range 100 MHz to 1100 MHz and is primarily intended for use in analogue cellular radio applications.

The device comprises of the following functional blocks:

- RF dual-modulus prescaler.
- RF programmable divider.
- Reference oscillator.
- Reference programmable divider.
- Digital phase comparator.
- In-lock detection circuitry.
- I^2C serial programming interface.

In addition, the device features a power down mode for battery conservation and a XTAL/4 output for use with the Philips cellular radio chipset. The only major external component required is a voltage controlled oscillator (VCO).

This application report presents a design for a frequency synthesizer based on the UMA1014T suitable for the local oscillator for analogue cellular radio applications in the 900 MHz band. A PCB layout is suggested. For detailed device specifications of the UMA1014T refer to the data sheet (Reference 1).

2. FUNCTIONAL DESCRIPTION OF THE UMA1014T

The main functions are illustrated in a Phase Lock Loop (PLL) block diagram (Fig 1). A temperature controlled crystal oscillator (TCXO) provides a reference frequency to the PLL. A phase comparator uses a charge pump to send correction current pulses to a low pass filter. The filter integrates the pulses giving a voltage which controls a VCO. VCO and TCXO o/ps are divided down to a common comparison frequency to control the phase comparator. When the VCO o/p is on frequency, the current pulses need only be large enough to cancel leakage currents, thus maintaining the required voltage on the VCO.

2.1 Main Divider Chain

The UMA1014T contains a fully programmable main divider chain with an on-chip RF prescaler. The range of the main divider is from 2,048 to 262,143, thus permitting all useful phase detector comparison frequencies over the full range of input frequencies.

2.2 Reference Divider Chain

Since current analogue systems have only a few different channel spacings, and in any system there is a restricted choice of reference crystal frequencies, the UMA1014T implements a reference divider with limited programmability. A total of 16 different division ratios can be selected which enables all the required phase detector comparison frequencies to be generated. These ratios are 128, 160, 192, 240, 256, 320, 384, 480, 512, 640, 768, 960, 1024, 1280, 1536 and 1920.

In addition, there is one eighth of the crystal frequency available on an output for use with the Philips cellular radio chipset. This chipset uses a 1.2 MHz clock for the analogue and digital baseband circuits which is provided by the frequency synthesizer; the synthesizer thus requires the use of a 9.6 MHz crystal in this application.

2.3 Phase Detector

There are three requirements for the phase detector; firstly it should cover the full 360 degree phase range, secondly it should have good noise performance, and thirdly it should have good comparison frequency suppression. In order to meet these requirements, the use of a high gain digital phase comparator is beneficial. The comparator covers the complete phase range while introducing little noise owing to the high proportion of time that is spent in a high impedance state. Good reference rejection is achieved due to low leakage currents.

2.3.1 Digital Phase Comparator

The Digital Phase Comparator (PCD) has three states, sinking current, sourcing current and a high impedance tristate. The design is based on D type flip-flops and responds to the full 360 degree range of phase inputs. The D type flip-flops control two current sources arranged in a push pull configuration. PCD delivers a constant current while the main and reference dividers are out of phase, either sinking or sourcing (Fig 2). The current IPCD is programmed via the I^2C interface to be either 1 mA or 0.5 mA. The phase comparator gain is hence:

$$\text{PCD gain} = \frac{\text{IPCD}}{2 \times \pi} \text{ A / rad} \qquad (1.)$$

The phase comparator circuit incorporates a delay which eliminates a dead band that would otherwise be present in digital phase comparators. Dead bands are due to the finite time the current sources take to switch on. The design of the UMA1014T takes this into account by introducing the delay into the D type reset line. This gives the current sources enough time to respond. Both current sources are switched on for the duration of the delay thus cancelling each other at PCD.

3. INTERFACING TO THE UMA1014T

The UMA1014T provides two way communication to a controller, power down facility, programmable o/p ports, oscillator circuitry and PLL control. The UMA1014T is designed to have the minimum of external components to enable low cost, compact and reliable circuits.

3.1 Programming the UMA1014T

The UMA1014T is programmed via the Philips Standard I^2C bus. To program information into the device registers, it is necessary to transmit first the device address, then the sub-address, and finally the data bytes for the register(s) (Reference 2). To read the status register, it is only necessary to transmit the address before reading back the value of the status register. When writing to the UMA1014T, the sub-address allows writing to any single register, or a burst mode where all registers can be written in one I^2C transfer. The formats are thus:

Write to one register:

START - address - sub-address - data - STOP

- contains register number to be accessed
- R/WN (read/write not) bit set to 0 (write)

Write to several registers:

START - address - sub-address - data 1 - ... - data n - STOP

- contains first register number to be accessed in the sequence and auto-increment enabled
- R/WN bit set to 0 (write)

Read from status register:

START - address - status - STOP

- R/WN bit set to 1 (read)

The address byte, in addition to containing the R/WN bit as shown above, has one bit that reflects the inverse of the SAA pin logic level. This allows the addressing of up to two synthesizer circuits on the same I²C bus.

The format for the address bus is as follows:

1 1 0 0 0 1 SAA R/WN

- R/WN: 0 (write, 1 (read)
- SAA: opposite logic level to that of SAA pin
- 1 1 0 0 0 1: MSB of device address, transmitted first after START condition

The sub-address has the following format: (X means not used)

X X X DI AVI X SB1 SB0

- SB1 SB0: register pointer
- AVI: auto-increment – 0 (disable), 1 (enable)
- DI: SYA interrupt – 1(disable), 0 (enable)

Data is formatted as a series of registers as follows:

Reg	SB 1/0	Bit Allocation 7	6	5	4	3	2	1	0	Preset
A	00	PD	0	IPCD	X	RD3	RD2	RD1	RD0	00001110
B	01	1	0	1	PHI	VCOB	VCOA	MD17	MD16	10101001
C	10	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	00111000
D	11	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	10000000

Register map bit polarities:

	0	1
PD	Normal operation	Power down
IPCD	Current in PCD = 0.5mA	PCD = 1mA
RD3..0	Reference divider ratio MSB = RD3	
PHI	Passive loop (no inversion)	Active loop (Phase inversion)
VCOA	Set Pin 7 low	Set Pin 7 high
VCOB	Set Pin 13 low	Set Pin 13 high
MD17..0	Main divider ratio MSB = MD17	

RD3..RD0 reference divider programming:

RD3	RD2	RD1	RD0	Reference Division Ratio
0	0	0	0	128
0	0	0	1	160
0	0	1	0	192
0	0	1	1	240
0	1	0	0	256
0	1	0	1	320
0	1	1	0	384
0	1	1	1	480
1	0	0	0	512
1	0	0	1	640
1	0	1	0	768
1	0	1	1	960
1	1	0	0	1024
1	1	0	1	1280
1	1	1	0	1536
1	1	1	1	1920

MD17..MD0 main divider value 2048 to 262,143 (hex $800 to $3ffff).

3.2 Hardware Control Inputs and Outputs

There are a number of status and control signals generated by the UMA1014T and also a hardware control input.

3.2.1 HPD Input

This input is used to disable the divider chains in order to save power when the synthesizer is not required to be operational. The power down state can be activated either by taking this pin low or by setting the power down bit in the I²C register to a '1'. The input has an internal pull-up resistor so that normal operation will be obtained if the pin is left open circuit.

The power down state does not have any effect on the I²C circuitry, so that the device may still be addressed, and new information programmed into the registers even in the power down mode.

3.2.2 FX8 Output

This is an open collector output of one eighth of the crystal or TCXO input frequency. It is required for use with the Philips cellular radio chipset for AMPS and TACS systems; in this application the synthesizer should be used with a 9.6 MHz TCXO. The recommended pull-up load is 27 kΩ.

3.2.3 SYA (Synthesizer Alarm) Output

This is an open collector output which is normally held high by an external 27 kΩ load. Under error conditions, the synthesizer latches SYA low. The error conditions that set SYA low are a power dip or an out-of-lock condition. A power dip occurs when V_{CC} supply falls below about 3.5 V. SYA is reset again by reading the status register, which contains the relevant alarm information. The SYA output can also be enabled and disabled via I²C as required.

The typical use of SYA would be to interrupt a microcontroller to warn of the error condition. As the output is open collector, it is possible to connect more than one device together directly; in this case the microcontroller would poll the relevant devices to locate the source of the error condition.

3.2.4 VCO0 and VCO1 Outputs

These are open collector outputs and are intended for enabling the power supply to VCOs or buffer stages so that these parts of the set can be powered down when not required to be operational. The outputs are controlled via I^2C. In addition, the VCO0 output is forced low during an out-of-lock condition; this output could, therefore, be used to disable the transmitter when this condition occurs to prevent causing interference. In this case, there may well be other parts of the circuitry also controlling the transmitter in the same way; as the VCO0 and VCO1 lines are open collector, they may be directly connected to other such controlling signals.

The VCO1 output is not affected by the hardware power down input or power down via I^2C. The VCO0 output will of course be forced low due to the out-of-lock condition resulting from a power down.

3.3 Crystal Oscillator

For analogue cellular radio applications, the UMA1014T will almost certainly be used with an external oscillator in order to provide the stability necessary to ensure operation within the specification. However, in case some other applications do not require such accuracy, provision has been made to form a crystal oscillator using the OSC_{IN} and OSC_{OUT} inputs (Pins 1 and 2, respectively). The oscillator circuit should be of the Colpitts type and requires the addition of four capacitors to function. This is shown in Fig 3, with capacitor values suitable for operation at 9.6 MHz.

The internal biasing provides possible operation over the range 3 MHz to 16 MHz with the addition of a suitable crystal. It may be necessary to adjust the values of the capacitors slightly to guarantee oscillation under all conditions for frequencies significantly different at 9.6 MHz.

The crystal used in this circuit is parallel resonant, fundamental mode, with a load capacitance of 30 pF which is approximately the series combination of the three fixed capacitors in parallel with the trimmer capacitor.

3.4 External Oscillator

When using an external oscillator such as a TCXO module, the output from the oscillator should be connected directly to the OSC_{IN} pin (Pin 1). The OSC_{OUT} pin (Pin 2) should either be left open circuit, or could be used as a buffered version of the signal applied to OSC_{IN}.

3.5 RF Connection to Main Divider

The output from the VCO needs to be split between the synthesizer RF o/p and the UMA1014T main divider input. A matched splitter is used as shown in Fig 4. Ideally, the splitter should provide maximum isolation to the VCO to prevent pulling or modulation due to changes in the load impedance at the RF o/p and main divider input. The amount of isolation is limited by the required RF output power and the main divider input sensitivity. Emphasis is placed on the importance of providing sufficient isolation between the VCO and the main divider to keep spurious modulations at a minimum level.

3.6 Loop Filter Design

The correct design of the loop filter is of considerable importance to the optimum performance of the synthesizer. The filter should be designed so as to achieve the required compromise between noise performance and switching time. The actual circuit will, therefore, depend on the particular application. A procedure has been established to ensure quick and simple loop filter design. The method, based on first-order approximations, provides a working solution without a need for computer simulation and modelling.

Design Procedure

For typical applications a passive loop is used, thus removing the need for an operational amplifier. The following design is based on a second-order low-pass filter (Reference 3). Then, for applications requiring further reference breakthrough rejection, a third-order is incorporated. The third-order loop filter is used for circuits and measurements in this report.

Loop parameters are first chosen, these are:

- Radio frequency RF
- Comparison frequency CF
- Switching time St
- Minimum modulating frequency MF
- VCO gain rad/Volt Ko
- Phase comparator gain Amps/rad Kd
- Phase margin Φ

Determine the loop bandwidth Fn from

$$\frac{3}{\text{switching time}} = fn \qquad (2.)$$

Determine main divider ratio from

$$N = \frac{RF}{CF} \qquad (3.)$$

Determine angular velocity wn rads / s from $wn = 2 \times \pi \times Fn$

The loop filter circuit (Fig 5) has three time constants, these are:

$$T1 = C3 \cdot R2 \qquad (4.)$$

$$T2 = R2 \cdot C1 \cdot C3 \,/\, (C3 + C4) \qquad (5.)$$

$$T3 = C2 \cdot R1 \qquad (6.)$$

The second-order loop is designed by omitting R1 and C2 (T3) and uses the equations below:

$$T2 = \frac{\frac{1}{\Phi} - \text{Tan}\ \Phi}{wn} \qquad (7.)$$

$$T1 = \frac{1}{wn^2 \cdot T2} \qquad (8.)$$

$$C3 + C1 = K\sqrt{\frac{1 + (wn \cdot T1)^2}{1 + (wn \cdot T2)^2}} \qquad (9.)$$

where,

$$K = \frac{Kd \cdot Ko}{N \cdot wn^2} \qquad (10.)$$

$$C1 = \frac{T2 \cdot (C3 + C1)}{T1} \qquad (11.)$$

$$C3 = (C3 + C1) - C1 \qquad (12.)$$

$$R2 = \frac{T1}{C3} \qquad (13.)$$

Measuring the reference spurs and comparing with a particular specification establishes if a third-order is necessary.

If a further 'A' dB of breakthrough suppression is needed to meet specification, then T3 is included to make a third-order filter. Note 'A' should not be so large that T3 x 10 > T1. A good starting value for 'A' is 20 dB.

$$T3 = \sqrt{\left(\frac{10^{(A/20)} - 1}{(2 \cdot \pi \cdot Fc)^2}\right)} \quad (14.)$$

T2 determines the loop stability and remains the same as for 2nd-order loop.

A calculated value of closed loop bandwidth wnc is used. This is usually slightly less than wn so the switching time will be slightly longer than originally specified.

$$wnc = \frac{(T2 + T3)}{T2^2} \cdot \tan \Phi \cdot \sqrt{1 + \frac{4 \cdot T2^2}{(2 \cdot \tan\Phi \cdot (T2 + T3))^2}} - 1 \quad (15.)$$

$$T1 = \frac{1}{wnc^2 \cdot (T2 + T3)} \quad (16.)$$

$$C3 + C1 = K \sqrt{\frac{1 + (wnc \cdot T1)^2}{(1 - wnc^2 \cdot T2 \cdot T3)^2 + \frac{T3 + T2}{T1}}} \quad (17.)$$

where,

$$K = \frac{Ko \cdot Kd}{N \cdot wnc^2} \quad (18.)$$

$$C1 = \frac{(C3 + C1) \cdot T2}{T1} \quad (19.)$$

$$C2 = C(C3 + C1) - C1 \quad (20.)$$

$$C2 = \frac{C1}{16} \quad (21.)$$

$$R2 = \frac{T1}{C3} \quad (22.)$$

$$R1 = \frac{T3}{C2} \quad (23.)$$

For a successful filter it is important that C3 > > C1 and C1 > > C2.

3.6.1 Worked Example

As an example the design of the third-order loop filter for the UMA1014T under the following conditions is shown below. This design on the PCAL1143-I board suitable for ETACS transmit application. Switching time is set slightly shorter than expected to compensate for the reduction in the final loop bandwidth Fnc.

VCO frequency		=	888MHz
VCO gain	Ko	=	13MHz/V
Channel spacing		=	25kHz (with half channel offset)
Reference oscillator		=	9.6MHz
Switching time		=	12ms (for a requirement < 14ms)
Min mod frequency		=	300Hz
Phase margin (degrees)		=	45
Additional reference Rejection	A	=	20dB

In this example the phase comparator gain Kd chosen is 1 mA / cycle as opposed to 0.5 mA / cycle. In open environment a loop based on this is less susceptible to interference as capacitor values are higher. A comparison frequency of 12.5 kHz is chosen to allow for the half channel offset specified in ETACS.

The first-order loop bandwidth Fn:

$$\frac{3}{12 \cdot 10^3} = 250Hz \quad wn = 2 \cdot \pi \cdot Fn = 1570rads/s \quad \text{Use (2.)}$$

The main divider ratio N:

$$\frac{888 \cdot 10^6}{12.5 \cdot 10^3} = 71,040 \quad \text{Use (3.)}$$

$$T2 = \frac{\frac{1}{\cos 45} - \tan 45}{1570} = 2.64 \cdot 10^{-4} \quad \text{Use (7.)}$$

$$T3 = \sqrt{\frac{10^{(20/20)} - 1}{(2 \cdot \pi \cdot 12,500)^2}} = 3.82 \cdot 10^{-5} \quad \text{Use (14.)}$$

$$wnc = \frac{4 \cdot (2.64 \cdot 10^{-4})^2}{(2.64 \cdot 10^{-4})^2} x \quad \text{Use (15.)}$$

$$\left(\sqrt{\frac{4 \cdot (2.64 \cdot 10^{-4})^2}{(2 \cdot \tan 45 \cdot (2.64 \cdot 10^{-4} + 3.82 \cdot 10^{-5}))^2}} - 1\right) = 1421$$

$$T1 \cdot \frac{1}{1421^2 \cdot (2.64 \cdot 10^{-4} + 3.82 \cdot 10^{-5})} = 1.64 \cdot 10^{-3} \quad \text{Use (16.)}$$

$$K = \frac{13 \cdot 10^6 \cdot 10^{-3}}{71,040 \cdot 1421^2} = 9.04 \cdot 10^{-8} \quad \text{Use (18.)}$$

$$C1 + C3 = \quad \text{Use (17.)}$$

$$k \sqrt{\frac{1 + (1421 \cdot 1.64 \cdot 10^{-3})^2}{(1 - 1421^2 \cdot 2.64 \cdot 10^{-4} \cdot 3.82^{-5})^2 + \frac{3.82 \cdot 10^{-5} + 2.64^{-4}}{1.64 \cdot 10^{-3}}}}$$

$$= 2.14 \cdot 10^{-7}$$

$$C1 = \frac{2.14 \cdot {}^{-7} \cdot 2.64 \cdot 10^{-4}}{1.64 \cdot 10^{-3}} = 3.45 \cdot 10^{-8} \quad \text{Use (19.)}$$

$$C3 = 2.14 \cdot 10^{-7} - 3.45 \cdot 10^{-8} = 1.8 \cdot 10^{-7} \quad \text{Use (20.)}$$

$$C2 = \frac{3.45 \cdot 10^{-8}}{16} = 2.15 \cdot 10^{-9} \quad \text{Use (21.)}$$

$$R2 = \frac{1.64 \cdot 10^{-3}}{1.8 \cdot 10^{-7}} = 9111 \quad \text{Use (22.)}$$

$$R1 = \frac{3.82 \cdot 10^{-5}}{2.15 \cdot 10^{-9}} = 17,767 \quad \text{Use (23.)}$$

Values chosen for filter components are:

C1 = 33nF R1 = 18kΩ
C2 = 2.2nF R2 = 10kΩ
C3 = 180nF

3.7 PCB Layout Considerations

The circuit of the UMA1014T demonstration board (PCAL1143-1) is shown in Fig 6, with the layout shown in Fig 7. This PCB has a solid ground plane on one side (apart from isolated pads for non-grounded connections to leaded components). In addition, there are areas of ground plane on the surface mount side of the board to ensure satisfactory grounding of important components. There are a good number of plated-through holes connecting the

two layers of ground plane. Normal RF design practices should of course be taken into account when laying out the circuit.

There are a number of particular points that should be borne in mind when considering the circuit and layout.

- The non-surface mount side of the board (if a 2 sided board is used) should be virtually solid ground plane to give good RF performance.
- The 5 V digital supply (V_{CC}) should be well decoupled as close to the pin as possible, preferably with a large value capacitor (e.g., 47 µF) and in series with a small value resistor (e.g., 12 Ω) from the 5 V line.
- The 5 V charge pump supply (V_{CP}) should be decoupled separately from V_{CC} but in a similar manner. Routing the 5 V supply under the IC is to be avoided.
- Incorporating a ground plane on the surface mount side of the PCB underneath the synthesizer helps isolate digital noise from the charge pump parts. This ground plane should be well connected with vias to the full ground plane.

4. TYPICAL PERFORMANCE

This section describes the typical performance obtainable with the UMA1014T with the circuit shown in Fig 6 and parameters listed in 3.6.1. The relevant performance criteria for a synthesizer are usually:

Close-in phase noise (i.e., noise within the loop bandwidth).
Noise floor at an offset from the carrier.
Comparison breakthrough components.
Switching time.

It should be noted of course that these criteria can be traded off against each other to some extent to tailor the overall performance, and that the performance described here is only one compromise between the various criteria. In general, the choice of a low loop bandwidth will improve the comparison frequency breakthrough and will filter out more of the close-in phase noise, but will result in a longer switching time. The use of a higher order filter can improve comparison frequency breakthrough with little effect on the noise or switching time. The noise floor at offsets significantly higher than the loop bandwidth are determined completely by the VCO itself.

Plots of the close-in spectrum (span of 2 kHz) and also a span of 50 kHz are shown in Figs 8 and 9, respectively, for a carrier frequency of 888 MHz and a comparison frequency of 12.5 kHz. From Fig 8 we can see from the noise plateau that the loop bandwidth is around 270 Hz, and Fig 9 shows the spectrum analyzer noise floor at offsets greater than about 15 kHz from the carrier with the first and second comparison frequency breakthrough component being visible at 12.5 kHz and 25 kHz from the carrier, respectively.

Figure 10 shows switching waveforms for a frequency jump of 10 MHz. The top trace (labelled CH1) is the I^2C transfer to the UMA1014T; the second (CH2) is the VCO control line. The third trace (CH3) is the VCOA output showing the out-of-lock condition. The fourth trace (CH4) is the RF output of the VCO mixed down to 0 Hz with a signal generator at the destination frequency. The VCO output is coupled to the mixer via an amplifier with 17 dB gain followed by a 10 dB attenuator. This is to provide isolation to the VCO from the mixer.

The mixer output trace shows that the switching time is 13 ms, which is a little longer than the VCO control line trace appears to show. This is because observation of the VCO control line is not accurate due to the very high VCO gain (13 MHz / V).

From Fig 10, we can see that the VCO control line has a single overshoot during switching; this shows that the loop is properly damped, so the phase margin is correct.

To summarize the performance of the circuit in Fig 6:

loop bandwidth	270 Hz
close-in noise	- 55 dBc / Hz at 200 Hz from carrier
VCO noise floor	- 113 dBc / Hz at 25 kHz from carrier
residual fm	< 18 Hz rms, CCITT weighted
comparison frequency breakthrough	- 65 dBc at 12.5 kHz - 82 dBc at 25 kHz
typical switching time	< 13 ms for 10 MHz jump to within 1 kHz of the destination frequency

5. CONCLUSIONS

Information regarding the use of the UMA1014T in a frequency synthesizer application has been presented. A methodology for determining the loop filter components has been described since the switching and noise performance of the complete circuit depends on a good filter design. The layout of the PCAL1143-1 demonstration board has been shown as an example PCB layout.

6. REFERENCES

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2. N. M. W. Oatley; Application Information for the UMA1010T/UMA1012T, Philips Components Application Report MC090001.
3. Ulriche, L. Rhode; Digital PLL Frequency Synthesizers Theory and Design. 28/3/91.

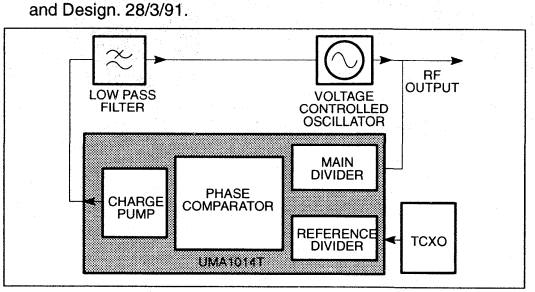

Figure 1. PLL Circuit Block Diagram

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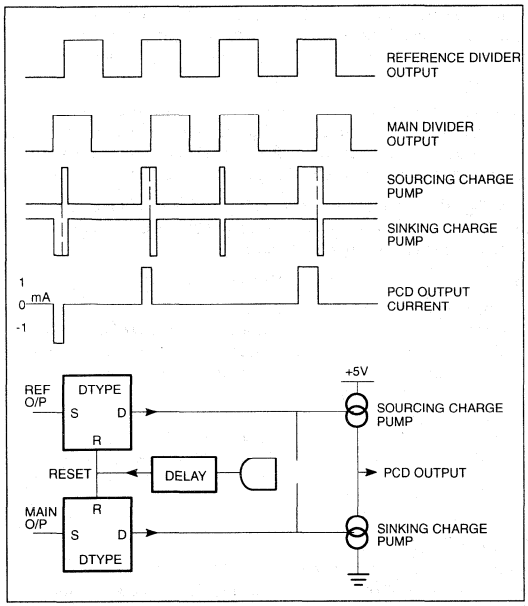


Figure 2. Digital Phase Comparator Operation

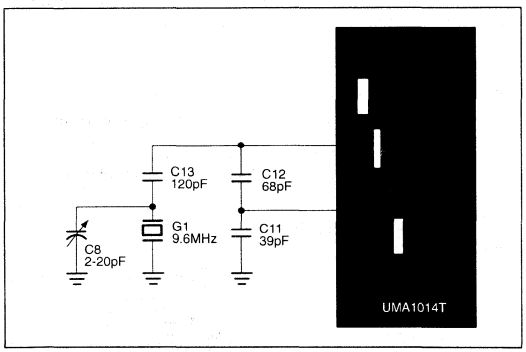


Figure 3. Crystal Oscillator Circuit Diagram

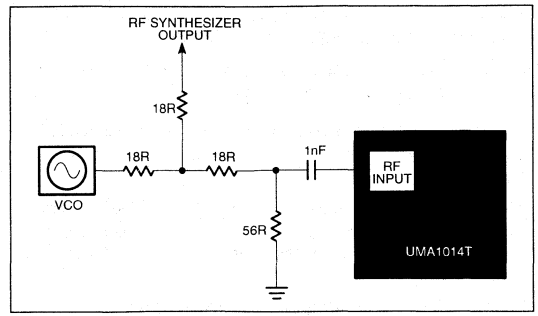


Figure 4. RF Power Splitter Circuit Diagram

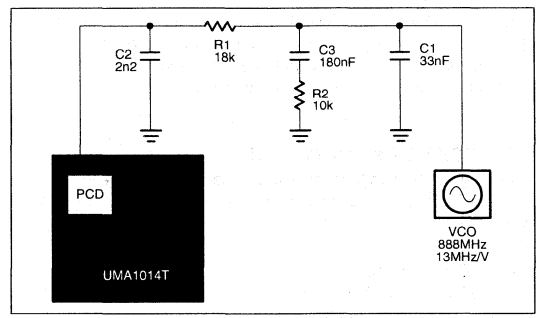


Figure 5. Loop Filter Circuit Diagram

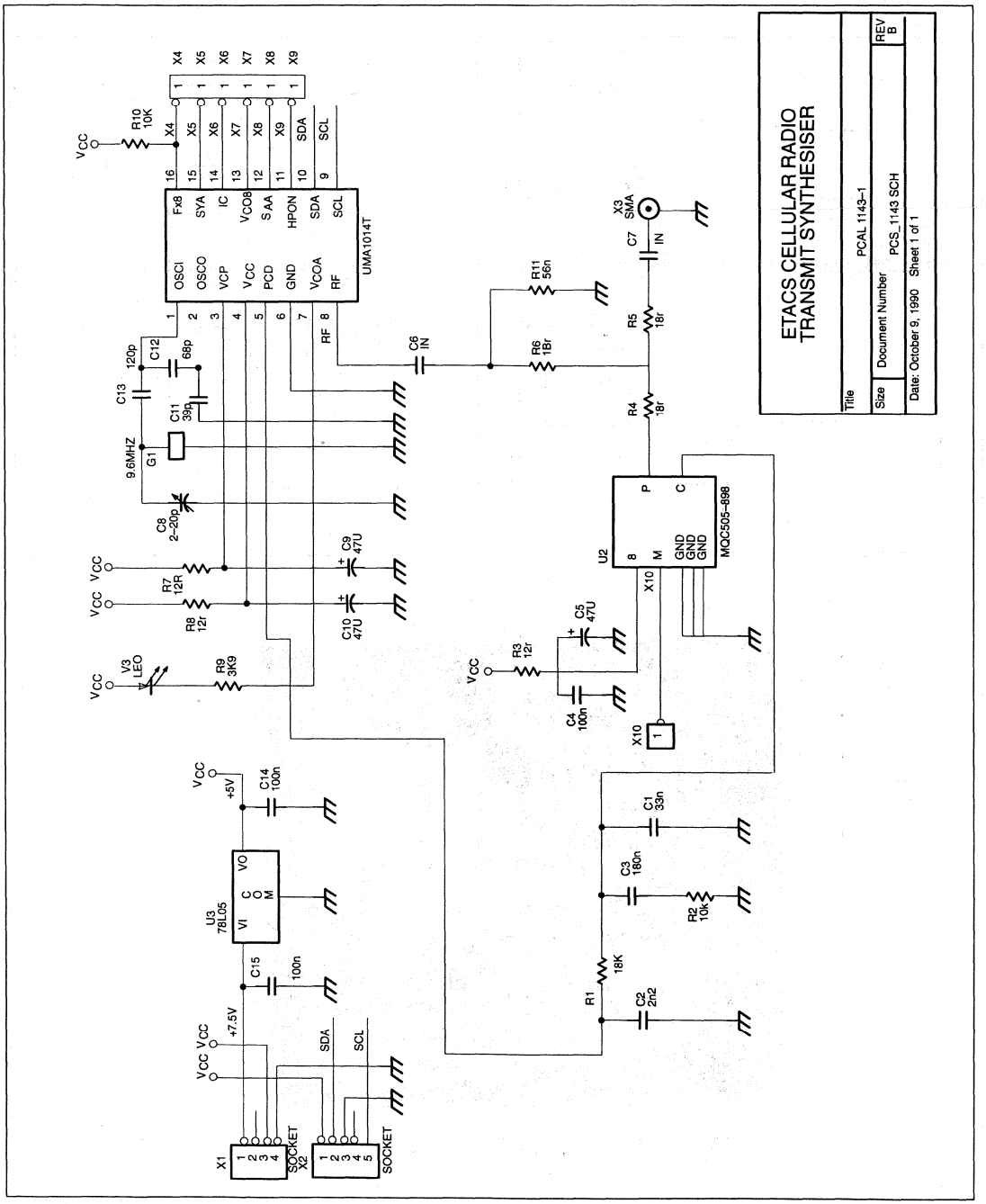


Figure 6. Frequency Synthesizer Circuit Using the UMA1014T

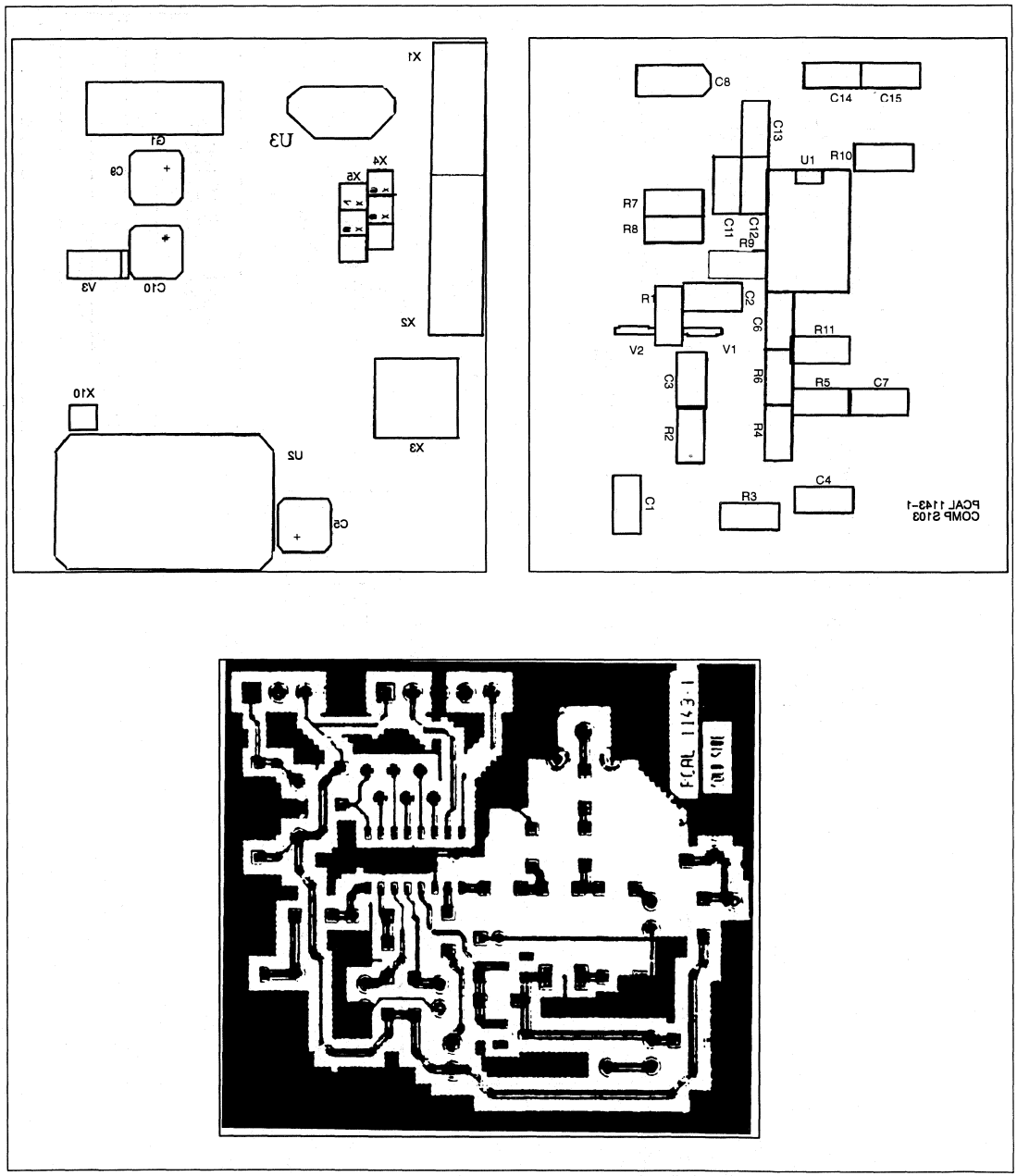


Figure 7. Board Layout for UMA1014T Frequency Synthesizer

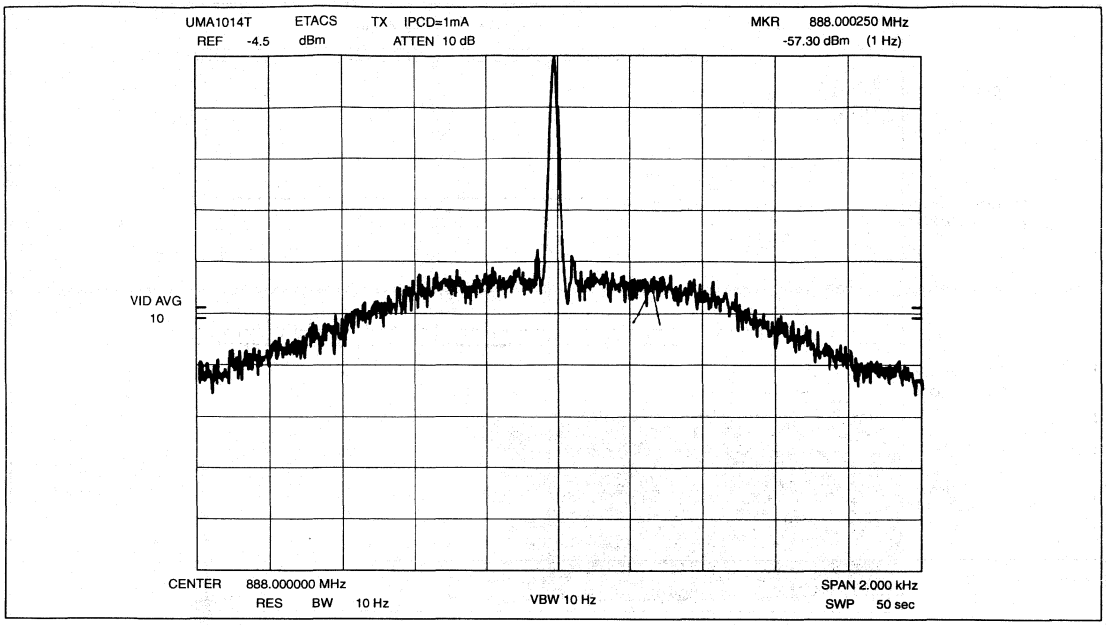


Figure 8. Typical Carrier Spectrum – 2kHz Span

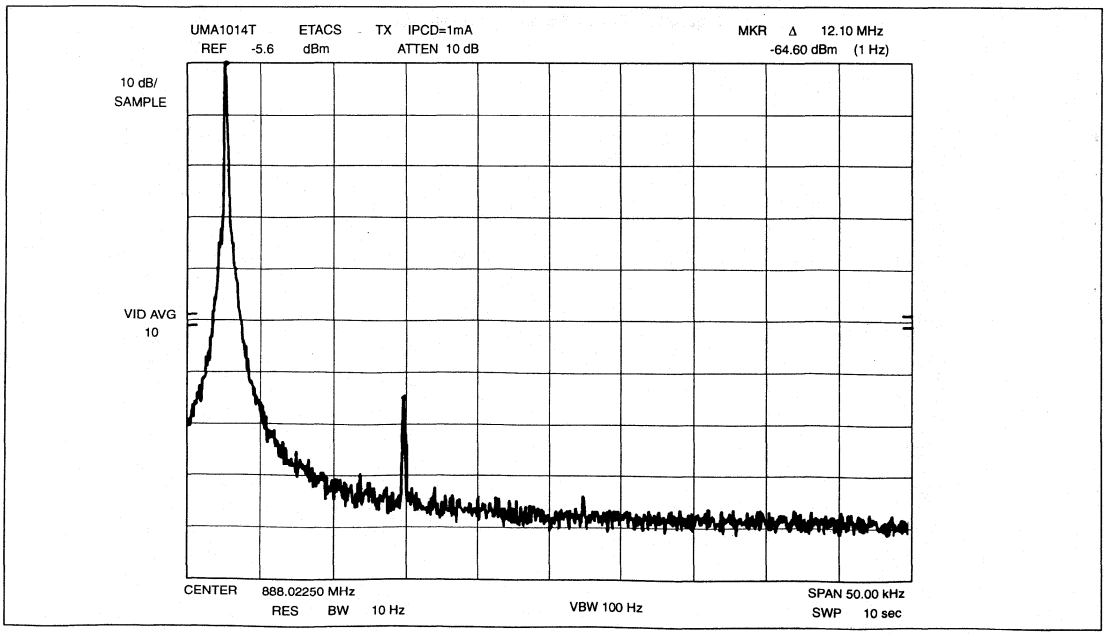


Figure 9. Typical Carrier Spectrum – 50kHz Span

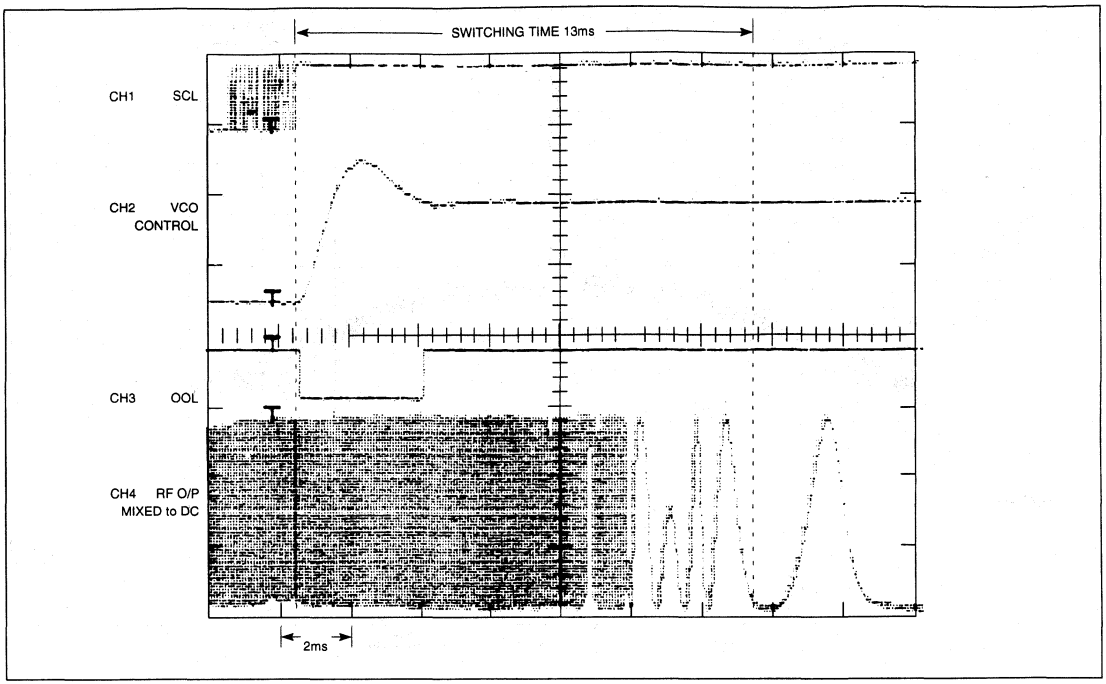


Figure 10. Typical Switching Waveforms

Low-power dual frequency synthesizer for radio communications

UMA1015AM

FEATURES

- Two fully programmable RF dividers up to 1.1 GHz
- Fully programmable reference divider up to 35 MHz
- 2 : 1 or 1 : 1 ratio of selectable reference frequencies
- Fast three-line serial bus interface
- Adjustable phase comparator gain
- Programmable out-of-lock indication for both loops
- On-chip voltage doubler
- Low current consumption from 3 V supply
- Separate power-down mode for each synthesizer
- Up to 4 open-drain output ports
- Crystal input frequency signal inverted and buffered output on separate pin.

APPLICATIONS

- Cordless telephone
- Hand-held mobile radio.

GENERAL DESCRIPTION

The UMA1015AM is a low-power dual frequency synthesizer for radio communications which operates in the 50 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz.

The device is programmed via a 3-wire serial bus which operates up to 10 MHz. The charge pump currents (gains) are fixed by an external resistance at pin 20 (I_{SET}). The BiCMOS device is designed to operate from 2.7 V (3 NiCd cells) to 5.5 V at low current. Digital supplies V_{DD1} and V_{DD2} must be at the same potential. The charge pump supply (V_{CC}) can be provided by an external source or on-chip voltage doubler. V_{CC} must be equal to or higher than V_{DD1}.

Each synthesizer can be powered-down independently via the serial bus to save current. It is also possible to power-down the device via the HPD input (pin 5).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	charge pump supply voltage	external supply; doubler disabled; $V_{CC} \geq V_{DD}$	2.7	–	6.0	V
V_{CCvd}	charge pump supply from voltage doubler	doubler enabled	–	$2V_{DD1} - 0.6$	6.0	V
$I_{DDO1} + I_{DDO2} + I_{CCO}$	operating supply current	both synthesizers ON; doubler disabled; $V_{DD1} = V_{DD2} = 3$ V	–	8.5	–	mA
$I_{DD1pd} + I_{DD2pd} + I_{CCpd}$	current in power-down mode per supply	doubler disabled; $V_{DD1} = V_{DD2} = 3$ V	–	3	–	µA
I_{DD1pd}	current in power-down mode from supply V_{DD}	doubler enabled; $V_{DD1} = V_{DD2} = 3$ V	–	0.15	–	mA
f_{RFA}, f_{RFB}	RF input frequency for each synthesizer		50	–	1100	MHz
f_{XTALIN}	crystal input frequency		3	–	35	MHz
$f_{pc(min)}$	minimum phase comparator frequency	f_{RF} = 50 to 1100 MHz; f_{XTALIN} = 3 to 35 MHz	–	10	–	kHz
$f_{pc(max)}$	maximum phase comparator frequency	f_{RF} = 50 to 1100 MHz; f_{XTALIN} = 3 to 35 MHz	–	750	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

Low-power dual frequency synthesizer for radio communications

UMA1015AM

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1015AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

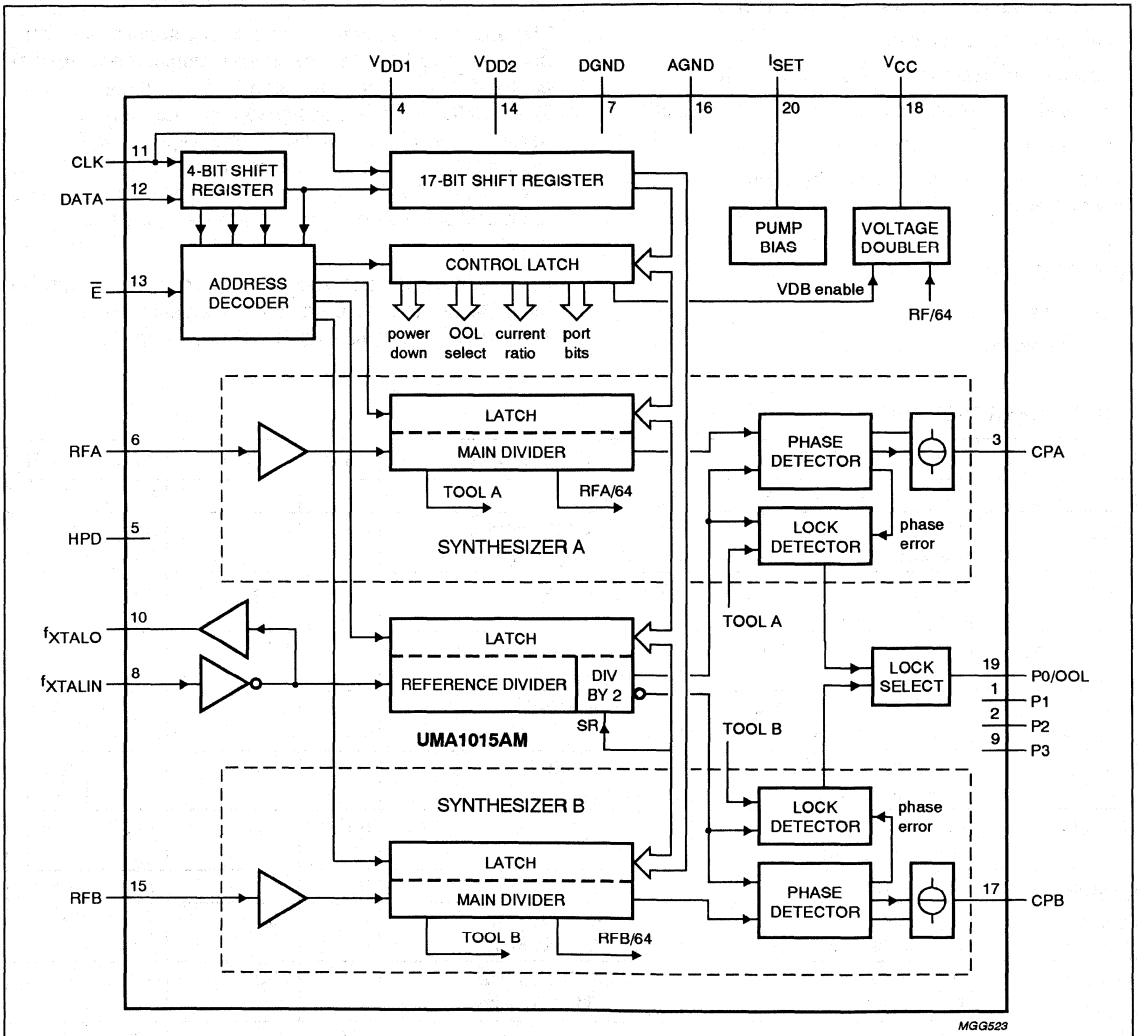


Fig.1 Block diagram.

Low-power dual frequency synthesizer for radio communications

UMA1015AM

PINNING

SYMBOL	PIN	DESCRIPTION
P1	1	output Port 1
P2	2	output Port 2
CPA	3	charge-pump output synthesizer A
V_{DD1}	4	digital supply voltage 1
HPD	5	hardware power-down (input LOW = power-down)
RFA	6	RF input synthesizer A
DGND	7	digital ground
f_{XTALIN}	8	common crystal frequency input from TCXO
P3	9	output Port 3
f_{XTALO}	10	open-drain output of f_{XTAL} signal
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
V_{DD2}	14	digital supply voltage 2
RFB	15	RF input synthesizer B
AGND	16	analog ground to charge pumps
CPB	17	charge pump output synthesizer B
V_{CC}	18	analog supply to charge pump; external or voltage doubler output
P0/OOL	19	Port output 0/out-of-lock output
I_{SET}	20	regulator pin to set charge-pump currents

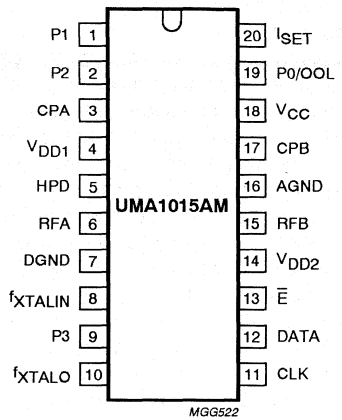


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main dividers

Each synthesizer has a fully programmable 17-bit main divider. The RF input drives a pre-amplifier to provide the clock to the first divider bit. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from below 50 mV (RMS) up to 250 mV (RMS), and at frequencies up to 1.1 GHz. The high frequency sections of the divider are implemented using bipolar transistors, while the slower section uses CMOS technology. The range of division ratios is 512 to 131071.

Reference divider

There is a common fully programmable 12-bit reference divider for the two synthesizers. The input f_{XTALIN} drives a pre-amplifier to provide the clock input for the reference divider. This clock signal is also inverted and output on pin f_{XTALO} (open drain). A crystal connected between f_{XTALIN} and f_{XTALO} with suitable feedback components can be used to make an oscillator. An extra divide-by-2 block allows a reference comparison frequency for synthesizer B to be half that of synthesizer A. This feature is selectable using the program bit SR. If the programmed reference divider ratio is R then the ratio for each synthesizer is as given in Table 1.

The range for the division ratio R is 8 to 4095.
Opposite edges of the divider output are used to drive the phase detectors to ensure that active edges arrive at the phase detectors of each synthesizer at different times. This minimizes the potential for interference between the charge pumps of each loop. The reference divider consists of CMOS devices operating beyond 35 MHz.

Table 1 Synthesizer ratio of reference divider

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Phase comparators

For each synthesizer, the outputs of the main and reference dividers drive a phase comparator where a charge pump produces phase error current pulses for integration in an external loop filter. The charge pump current is set by an external resistance R_{SET} at pin I_{SET}, where a temperature-independent voltage of 1.2 V is generated. R_{SET} should be between 12 kΩ and 60 kΩ (to give an I_{SET} of 100 μA and 20 μA respectively). The charge-pump current, I_{CP}, can be programmed to be either ($12 \times I_{SET}$) or ($24 \times I_{SET}$) with the maximum being 2.4 mA. The dead zone, caused by finite switching of current pulses, is cancelled by an internal delay in the phase detector thus giving improved linearity. The charge pump has a separate supply, V_{CC}, which helps to reduce the interference on the charge pump output from other parts of the circuit. Also, V_{CC} can be higher than V_{DD1} if a wider range on the VCO input is required. V_{CC} must not be less than V_{DD1}.

Voltage doubler

If required, there is a voltage doubler on-chip to supply the charge pumps at a higher level than the nominal available supply. The doubler operates from the digital supply V_{DD1}, and is internally limited to a maximum output of 6 V. An external capacitor is required on pin V_{CC} for smoothing, the capacitor required to develop the extra voltage is integrated on-chip. To minimize the noise being introduced to the charge pump output from the voltage doubler, the doubler clock is suppressed (provided both loops are in-lock) for the short time that the charge pumps are active. The doubler clock (RF/64) is derived from whichever main divider is operating (synthesizer A has priority). While both synthesizers are powered down (and the doubler is enabled), the doubler clock is supplied by a low-current internal oscillator. The doubler can be disabled by programming the bit VDON to logic 0, in order to allow an external charge pump supply to be used.

Out-of-lock indication/output ports

There is a common lock detector on-chip for the synthesizers. The lock condition of each, or both loops, is output via an open-drain transistor which drives the pin P0/OOL (when out-of-lock, the transistor is turned on and therefore the output is forced LOW). The lock condition output is software selectable (see Table 4). An out-of-lock condition is flagged when the phase error is greater than T_{OOL}, the value of which is approximately equal to 80 cycles of the relevant RF input. The out-of-lock flag is only released after the first reference cycle where the phase error is less than T_{OOL}. The out-of-lock function can be disabled, via the serial bus, and the pin P0/OOL can be used as an output port. Three other port outputs P1, P2 and P3 (open-drain transistors) are also available.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. This is allowed when CLK is in either state without causing any consequences to the register data. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down of both synthesizers.

However when either synthesizer A or synthesizer B or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTALIN}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To ensure that data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The data format and register bit allocations are shown in Table 2.

Table 2 Bit allocation

FIRST	REGISTER BIT ALLOCATION																			LAST
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
X	X	VDON	PO	OLA	OLB	CRA	CRB	X	X	sPDA	sPDB	P3	P2	P1	X	X	0	0	0	1
MA16	SYNTHESIZER A MAIN DIVIDER COEFFICIENT															MA0	0	1	0	0
0	0	0	0	SR	R11	REFERENCE DIVIDER COEFFICIENT										R0	0	1	0	1
MB16	SYNTHESIZER B MAIN DIVIDER COEFFICIENT															MB0	0	1	1	0
RESERVED FOR TEST[1]																	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	sPBF	0	0	1	0	0	0

Note

1. The test register should not be programmed with any other values except all zeros for normal operation.

Table 3 Bit allocation description

SYMBOL	DESCRIPTION
sPDA, sPDB	software power-down for synthesizers A and B (0 = power-down)
sPBF	software power-on for f_{xtal} buffer (1 = buffer on)
P3, P2, P1 and P0	bits output to pins 1, 2, 9 and 19 (1 = high impedance)
VDON	voltage doubler enable (1 = doubler enabled)
OLA, OLB	out-of-lock select; selects signal output to pin 19 (see Table 4)
CRA, CRB	charge pump A/B current to I_{SET} ratio select (see Table 5)
SR	reference frequency ratio select (see Table 6)

Table 4 Out-of-lock select

OLA	OLB	OUTPUT AT PIN 19
0	0	P0
0	1	lock status of loop B; OOLB
1	0	lock status of loop A; OOLA
1	1	logic OR function of loops A and B

Table 5 Charge pump current ratio

CRA/CRB	CURRENT AT PUMP
0	$I_{CP} = 12 \times I_{SET}$
1	$I_{CP} = 24 \times I_{SET}$

Table 6 Reference division ratio

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Power-down modes

The device can be powered down either via pin HPD (active LOW = power-down) or via the serial bus (bits sPDA and sPDB, logic 0 = power-down).
The synthesizers are powered up when both hardware and software Power-down signals are at logic 1.
When only one synthesizer is powered down, the functions common to both will be maintained (independent of the state of sPBF). When both synthesizers are powered down, the f_{xtal} buffer can be maintained in an active state by setting sPBF to logic 1.

This will allow any system clock derived from the FXTALO buffered output to remain on in power down. Note that sPBF is independent of the state of HPD. When both synthesizers are switched off, the voltage doubler (if enabled) will remain active drawing a reduced current. An internal oscillator will drive the doubler in this situation. If both synthesizers have been in a power-down condition, then when one or both synthesizers are reactivated, the reference and main dividers restart in such a way as to avoid large random phase errors at the phase comparator.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}, V_{DD2}	DC range of digital power supply voltage with respect to DGND	−0.3	+6.0	V
V_{CC}	DC charge pump supply voltage with respect to AGND	−0.3	+6.0	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD1}, V_{DD2}	−0.3	+6.0	V
V_n	DC voltage at pins 1, 2, 5, 6, 8 to 15, 19 and 20 with respect to DGND	−0.3	V_{DD1} + 0.3	V
$V_{3, 17}$	DC voltage at pins 3 and 17 with respect to AGND	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 6.0 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; (V_{DD1}, V_{DD2} and V_{CC}) voltage doubler disabled, external supply on V_{CC}						
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
$I_{DD1} + I_{DD2}$	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2}$ = 3 V	–	8.5	–	mA
		f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2}$ = 5.5 V	–	–	12.5	mA
I_{DDpda}, I_{DDpdb}	total digital supply current from V_{DD1} and V_{DD2} with one synthesizer in power-down mode	f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2}$ = 3 V	–	5.5	–	mA
		f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2}$ = 5.5 V	–	–	7.5	mA
I_{DDpd}	digital supply current in power-down mode	both synthesizers powered down; V_{HPD} = 0 V; sPBF = 0	–	–	60	μA
V_{CC}	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	6.0	V
I_{CC}	charge pump supply current	both synthesizers on and in lock; f_{ref} = 12.5 kHz	–	–	25	μA
I_{CCpd}	charge pump supply current in power-down mode	both synthesizers powered down	–	–	25	μA
Voltage doubler enabled						
I_{DD}	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on and in lock; V_{DD1} = 3 V; $f_{doubler}$ = 16 MHz	–	8.5	12	mA
I_{DDpd}	total digital supply current in power-down mode from V_{DD1} and V_{DD2}	both synthesizers powered down; V_{DD1} = 3 V; V_{HPD} = 0 V; sPBF = 0	–	0.25	0.4	mA
V_{CCvd}	charge pump supply voltage	DC current drawn from V_{CC} = 50 μA	$2V_{DD1} - 1.2$	$2V_{DD1} - 0.6$	6.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF main divider input; RFA and RFB						
f_{RF}	RF input frequency		50	–	1100	MHz
$V_{RF(rms)}$	RF input signal voltage (RMS value; AC coupled)	R_s = 50 Ω; f_{RF} = 400 to 1100 MHz	50	–	250	mV
		R_s = 50 Ω; f_{RF} = 50 to 400 MHz	150	–	400	mV
Z_I	input impedance (real part)	f_{RF} = 1 GHz; indicative, not tested	–	300	–	Ω
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{pm}	principle main divider ratio		512	–	131071	
Reference divider input; f_{XTALIN}						
f_{XTALIN}	reference input frequency from crystal		3	–	35	MHz
$V_{XTALIN(rms)}$	sinusoidal input voltage (RMS value)		100	–	500	mV
Z_I	input impedance (real part)	f_{XTALIN} = 12.8 MHz; indicative, not tested	–	10	–	kΩ
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{rd}	reference divider ratio		8	–	4095	
Charge pump current setting resistor input; I_{SET}						
V_{SET}	voltage output on I_{SET}	R_{SET} = 12 to 60 kΩ	–	1.2	–	V
Charge pump outputs; CPA and CPB						
I_{CP}	charge pump sink or source current	R_{SET} = 15 kΩ; CRA/CRB = logic 1; $I_{cp} = I_{SET} \times 24$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	1.4	1.9	2.4	mA
		R_{SET} = 15 kΩ; CRA/CRB = logic 0; $I_{cp} = I_{SET} \times 12$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	0.7	0.96	1.2	mA
I_{LI}	charge pump off leakage current	V_{cp} = 0.4 V to V_{CC} – 0.5 V	–5	±1	+5	nA
Logic input signal levels; DATA, CLK, $\overline{E}$ and HPD						
V_{IH}	HIGH level input voltage	at logic 1	$0.7V_{DD1}$	–	V_{DD1} + 0.3	V
V_{IL}	LOW level input voltage	at logic 0	–0.3	–	$0.3V_{DD1}$	V
I_{bias}	input bias currents	at logic 1 or logic 0	–5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	1	–	pF
Port outputs/Out-of-lock; P0/OOL, P1, P2, P3 and f_{XTALO} - open drain outputs						
V_{OL}	LOW level output voltage	I_{sink} < 0.4 mA	–	–	0.4	V

SERIAL TIMING CHARACTERISTICS

V_{DD1} = 3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r, t_f	input rise and fall times	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	−20	–	–	ns
t_W	minimum inactive pulse width	4000	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

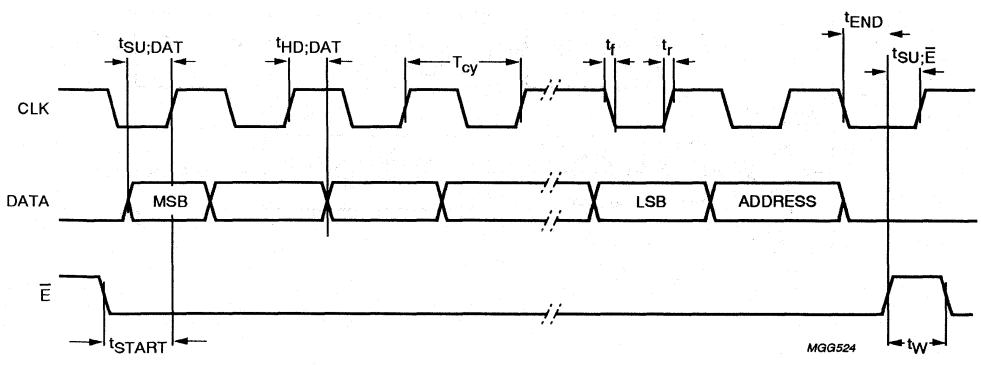


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

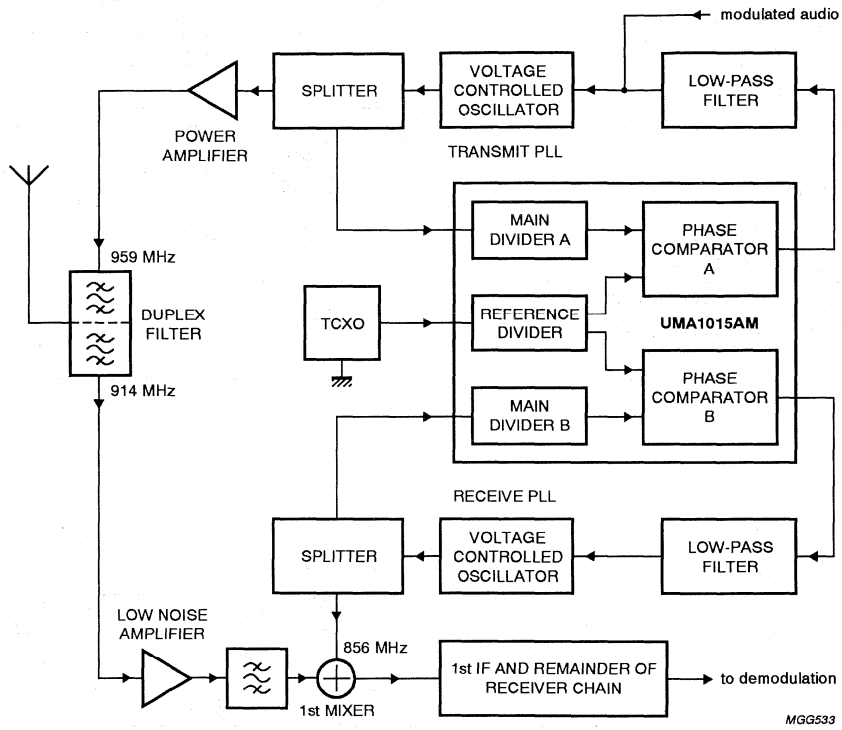


Fig.4 Typical application block diagram.

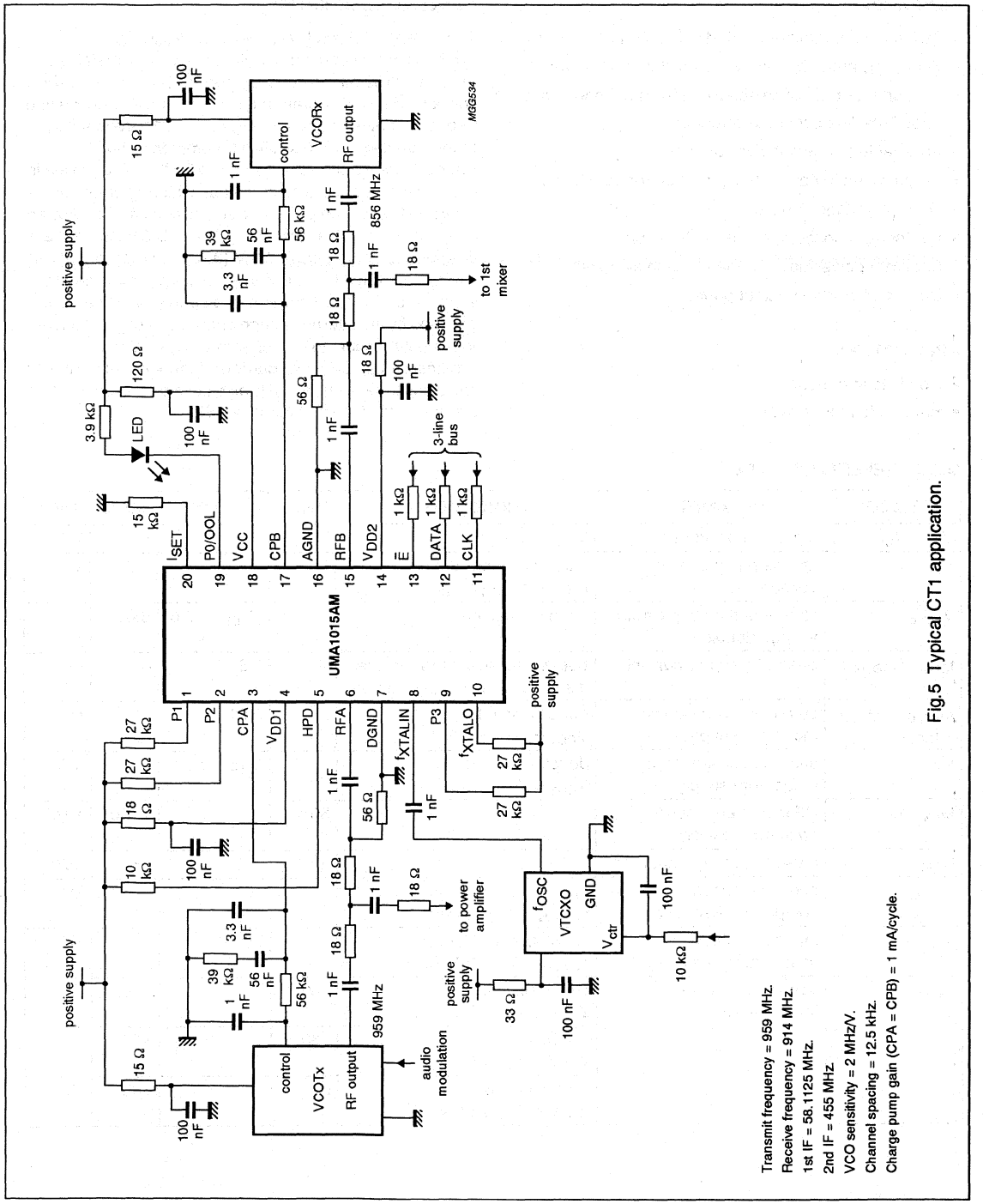


Fig.5 Typical CT1 application.

Low-power dual frequency synthesizer for radio communications

UMA1015M

FEATURES

- Two fully programmable RF dividers up to 1.1 GHz
- Fully programmable reference divider up to 35 MHz
- 2 : 1 or 1 : 1 ratio of selectable reference frequencies
- Fast three-line serial bus interface
- Adjustable phase comparator gain
- Programmable out-of-lock indication for both loops
- On-chip voltage doubler
- Low current consumption from 3 V supply
- Separate power-down mode for each synthesizer
- Up to 4 open-drain output ports.

APPLICATIONS

- Cordless telephone
- Hand-held mobile radio.

GENERAL DESCRIPTION

The UMA1015M is a low-power dual frequency synthesizer for radio communications which operates in the 50 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz. The device is programmed via a 3-wire serial bus which operates up to 10 MHz. The charge pump currents (gains) are fixed by an external resistance at pin 20 (I_{SET}). The BiCMOS device is designed to operate from 2.6 V (3 Ni-Cd cells) to 5.5 V at low current. Digital supplies V_{DD1} and V_{DD2} must be at the same potential. The charge pump supply (V_{CC}) can be provided by an external source or on-chip voltage doubler. V_{CC} must be equal to or higher than V_{DD1}. Each synthesizer can be powered-down independently via the serial bus to save current. It is also possible to power-down the device via the HPD input (pin 5).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.6	–	5.5	V
V_{CC}	charge pump supply voltage	external supply; doubler disabled; $V_{CC} \geq V_{DD}$	2.6	–	6.0	V
V_{CCvd}	charge pump supply from voltage doubler	doubler enabled	–	$2V_{DD1} - 0.6$	6.0	V
$I_{DDO1} + I_{DDO2} + I_{CCO}$	operating supply current	both synthesizers ON; doubler disabled; $V_{DD1} = V_{DD2} = 5.5$ V	–	9.6	–	mA
$I_{DD1pd} + I_{DD2pd} + I_{CCpd}$	current in power-down mode per supply	doubler disabled; $V_{DD1} = V_{DD2} = 5.5$ V	–	0.01	–	mA
I_{DD1pd}	current in power-down mode from supply V_{DD}	doubler enabled; $V_{DD1} = V_{DD2} = 3$ V	–	0.15	–	mA
f_{RFA}, f_{RFB}	RF input frequency for each synthesizer		50	–	1100	MHz
f_{XTALIN}	crystal input frequency		3	–	35	MHz
$f_{pc(min)}$	minimum phase comparator frequency	f_{RF} = 50 to 1100 MHz; f_{XTALIN} = 3 to 35 MHz	–	10	–	kHz
$f_{pc(max)}$	maximum phase comparator frequency	f_{RF} = 50 to 1100 MHz; f_{XTALIN} = 3 to 35 MHz	–	750	–	kHz
T_{amb}	operating ambient temperature	synthesizer A $2.6 \text{ V} \leq V_{DD} \leq 5.5$ V	−30	–	+85	°C
		synthesizer B $2.6 \text{ V} \leq V_{DD} \leq 4.5$ V	−30	–	+85	°C
		synthesizer B $2.6 \text{ V} \leq V_{DD} \leq 5.0$ V	0	–	+85	°C

Low-power dual frequency synthesizer for radio communications

UMA1015M

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1015M/C2	20	SSOP20	plastic	SOT266-1

BLOCK DIAGRAM

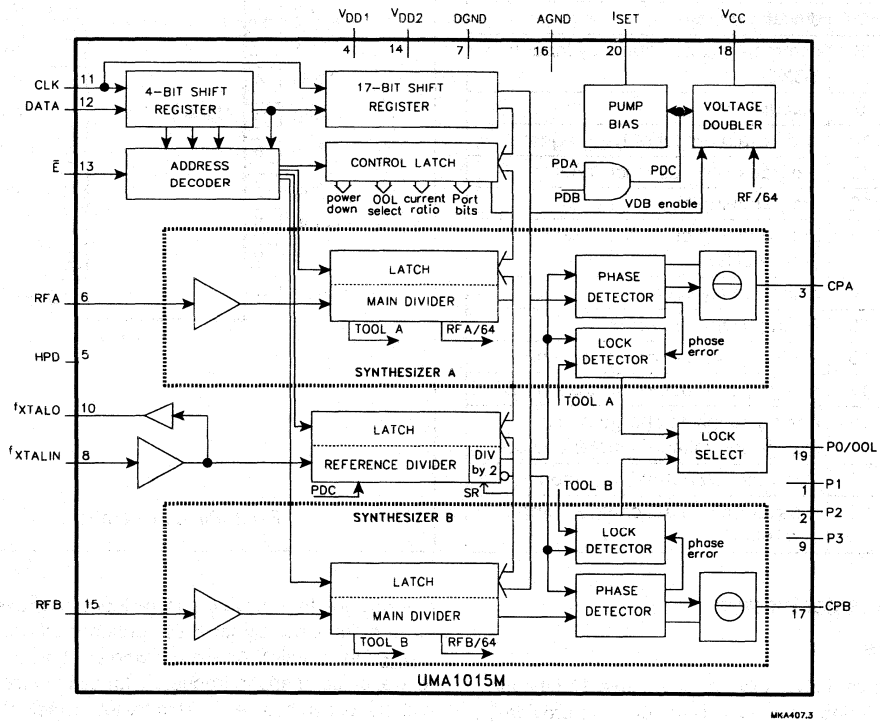


Fig.1 Block diagram.

Low-power dual frequency synthesizer for radio communications

UMA1015M

PINNING

SYMBOL	PIN	DESCRIPTION
P1	1	output Port 1
P2	2	output Port 2
CPA	3	charge-pump output synthesizer A
V_{DD1}	4	digital supply voltage 1
HPD	5	hardware power-down (input LOW = power-down)
RFA	6	RF input synthesizer A
DGND	7	digital ground
f_{XTALIN}	8	common crystal frequency input from TCXO
P3	9	output Port 3
f_{XTALO}	10	open-drain output of f_{XTAL} signal
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
V_{DD2}	14	digital supply voltage 2
RFB	15	RF input synthesizer B
AGND	16	analog ground to charge pumps
CPB	17	charge pump output synthesizer B
V_{CC}	18	analog supply to charge pump; external or voltage doubler output
P0/OOL	19	Port output 0/out-of-lock output
I_{SET}	20	regulator pin to set charge-pump currents

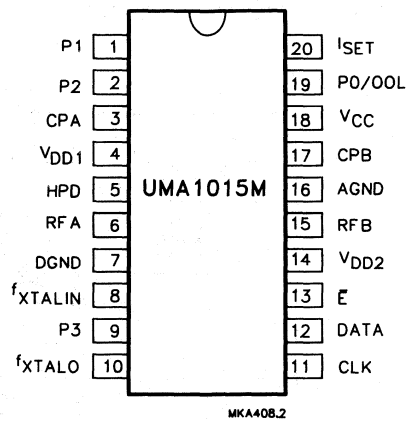


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main dividers

Each synthesizer has a fully programmable 17-bit main divider. The RF input drives a pre-amplifier to provide the clock to the first divider bit. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from below 50 mV (RMS) up to 250 mV (RMS), and at frequencies up to 1.1 GHz. The high frequency sections of the divider are implemented using bipolar transistors, while the slower section uses CMOS technology. The range of division ratios is 512 to 131071.

Reference divider

There is a common fully programmable 12-bit reference divider for the two synthesizers. The input f_{XTALIN} drives a pre-amplifier to provide the clock input for the reference divider. This clock signal is also buffered and output on pin f_{XTALO} (open drain). An extra divide-by-2 block allows a reference comparison frequency for synthesizer B to be half that of synthesizer A. This feature is selectable using the program bit SR. If the programmed reference divider ratio is R then the ratio for each synthesizer is as given in Table 1.

The range for the division ratio R is 8 to 4095. Opposite edges of the divider output are used to drive the phase detectors to ensure that active edges arrive at the phase detectors of each synthesizer at different times. This minimizes the potential for interference between the charge pumps of each loop. The reference divider consists of CMOS devices operating beyond 35 MHz.

Table 1 Synthesizer ratio of reference divider

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Phase comparators

For each synthesizer, the outputs of the main and reference dividers drive a phase comparator where a charge pump produces phase error current pulses for integration in an external loop filter. The charge pump current is set by an external resistance R_{SET} at pin I_{SET}, where a temperature-independent voltage of 1.2 V is generated. R_{SET} should be between 12 kΩ and 60 kΩ (to give an I_{SET} of 100 μA and 20 μA respectively).
The charge-pump current, I_{CP}, can be programmed to be either ($12 \times I_{SET}$) or ($24 \times I_{SET}$) with the maximum being 2.4 mA. The dead zone, caused by finite switching of current pulses, is cancelled by an internal delay in the phase detector thus giving improved linearity. The charge pump has a separate supply, V_{CC}, which helps to reduce the interference on the charge pump output from other parts of the circuit. Also, V_{CC} can be higher than V_{DD1} if a wider range on the VCO input is required. V_{CC} must not be less than V_{DD1}.

Voltage doubler

If required, there is a voltage doubler on-chip to supply the charge pumps at a higher level than the nominal available supply. The doubler operates from the digital supply V_{DD1}, and is internally limited to a maximum output of 6 V.
An external capacitor is required on pin V_{CC} for smoothing, the capacitor required to develop the extra voltage is integrated on-chip. To minimize the noise being introduced to the charge pump output from the voltage doubler, the doubler clock is suppressed (provided both loops are in-lock) for the short time that the charge pumps are active. The doubler clock (RF/64) is derived from whichever main divider is operating (synthesizer A has priority). While both synthesizers are powered down (and the doubler is enabled), the doubler clock is supplied by a low-current internal oscillator. The doubler can be disabled by programming the bit VDON to logic 0, in order to allow an external charge pump supply to be used.

Out-of-lock indication/output ports

There is a lock detector on-chip for each synthesizer. The lock condition of each, or both loops, is output via an open-drain transistor which drives the pin P0/OOL (when out-of-lock, the transistor is turned on and therefore the output is forced LOW). The lock condition output is software selectable (see Table 4). An out-of-lock condition is flagged when the phase error is greater than T_{00L}, the value of which is approximately equal to 80 cycles of the relevant RF input. The out-of-lock flag is only released after 8 consecutive reference cycles where the phase error is less than T_{00L}. The out-of-lock function can be disabled, via the serial bus, and the pin P0/OOL can be used as an output port. Three other port outputs P1, P2 and P3 (open-drain transistors) are also available.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. This is allowed when CLK is in either state without causing any consequences to the register data. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down of both synthesizers.

However when either synthesizer A or synthesizer B or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTALIN}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To ensure that data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The data format and register bit allocations are shown in Table 2.

Table 2 Bit allocation

FIRST	REGISTER BIT ALLOCATION																			LAST
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
X	X	VDON	PO	OLA	OLB	CRA	CRB	X	X	sPDA	sPDB	P3	P2	P1	X	X	0	0	0	1
MA16	SYNTHESIZER A MAIN DIVIDER COEFFICIENT															MA0	0	1	0	0
0	0	0	0	SR	R11	REFERENCE DIVIDER COEFFICIENT										R0	0	1	0	1
MB16	SYNTHESIZER B MAIN DIVIDER COEFFICIENT															MB0	0	1	1	0
RESERVED FOR TEST(1)																	0	0	0	0

Note

1. The test register should not be programmed with any other values except all zeros for normal operation.

Table 3 Bit allocation description

SYMBOL	DESCRIPTION
sPDA, sPDB	software power-down for synthesizers A and B (0 = power-down)
P3, P2, P1 and P0	bits output to pins 1, 2, 9 and 19 (1 = high impedance)
VDON	voltage doubler enable (1 = doubler enabled)
OLA, OLB	out-of-lock select; selects signal output to pin 19 (see Table 4)
CRA, CRB	charge pump A/B current to I_{SET} ratio select (see Table 5)
SR	reference frequency ratio select (see Table 6)

Table 4 Out-of-lock select

OLA	OLB	OUTPUT AT PIN 19
0	0	P0
0	1	lock status of loop B; OOLB
1	0	lock status of loop A; OOLA
1	1	logic OR function of loops A and B

Table 5 Charge pump current ratio

CRA/CRB	CURRENT AT PUMP
0	$I_{CP} = 12 \times I_{SET}$
1	$I_{CP} = 24 \times I_{SET}$

Table 6 Reference division ratio

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Power-down modes

The device can be powered down either via pin HPD (active LOW = power-down) or via the serial bus (bits SPDA and SPDB, logic 0 = power-down). The synthesizers are powered up when both hardware and software Power-down signals are at logic 1. When only one synthesizer is powered down, the functions common to both will be maintained. When both synthesizers are switched off, only the voltage doubler (if enabled) will remain active drawing a reduced current. An internal oscillator will drive the doubler in this situation. If both synthesizers have been in a power-down condition, then when one or both synthesizers are reactivated, the reference and main dividers restart in such a way as to avoid large random phase errors at the phase comparator.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}, V_{DD2}	DC range of digital power supply voltage with respect to DGND	−0.3	+6.0	V
V_{CC}	DC charge pump supply voltage with respect to AGND	−0.3	+6.0	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD1}, V_{DD2}	−0.3	+6.0	V
V_n	DC voltage at pins 1, 2, 5, 6, 8 to 15, 19 and 20 with respect to DGND	−0.3	V_{DD1} + 0.3	V
$V_{3, 17}$	DC voltage at pins 3 and 17 with respect to AGND	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.6$ to 5.5 V; $V_{CC} = 2.6$ to 6.0 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; (V_{DD1}, V_{DD2} and V_{CC}) voltage doubler disabled, external supply on V_{CC}						
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.6	–	5.5	V
$I_{DD1} + I_{DD2}$	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2}$ = 3 V	–	8.5	–	mA
		f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2}$ = 5.5 V	–	–	12.5	mA
I_{DDpda}, I_{DDpdb}	total digital supply current from V_{DD1} and V_{DD2} with one synthesizer in power-down mode	f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2}$ = 3 V	–	5.5	–	mA
		f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2}$ = 5.5 V	–	–	7.5	mA
I_{DDpd}	digital supply current in power-down mode	both synthesizers powered down; V_{HPD} = 0 V	–	–	60	µA
V_{CC}	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.6	–	6.0	V
I_{CC}	charge pump supply current	both synthesizers on and in lock; f_{ref} = 12.5 kHz	–	–	25	µA
I_{CCpd}	charge pump supply current in power-down mode	both synthesizers powered down	–	–	25	µA
Voltage doubler enabled						
I_{DD}	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on and in lock; V_{DD1} = 3 V; $f_{doubler}$ = 16 MHz	–	8.5	12	mA
I_{DDpd}	total digital supply current in power-down mode from V_{DD1} and V_{DD2}	both synthesizers powered down; V_{DD1} = 3 V; V_{HPD} = 0 V	–	0.25	0.4	mA
V_{CCvd}	charge pump supply voltage	DC current drawn from V_{CC} = 50 µA	$2V_{DD1} - 1.2$	$2V_{DD1} - 0.6$	6.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF main divider input; RFA and RFB						
f_{RF}	RF input frequency		50	–	1100	MHz
$V_{RF(rms)}$	RF input signal voltage (RMS value; AC coupled)	R_s = 50 Ω; $V_{DD1} = V_{DD2}$ = 2.6 to 3.5 V; f_{RF} = 400 to 1100 MHz	50	–	250	mV
		R_s = 50 Ω; $V_{DD1} = V_{DD2}$ = 3.5 to 5.5 V; f_{RF} = 400 to 1100 MHz	100	–	250	mV
		R_s = 50 Ω; $V_{DD1} = V_{DD2}$ = 2.6 to 5.5 V; f_{RF} = 50 to 400 MHz	150	–	400	mV
Z_I	input impedance (real part)	f_{RF} = 1 GHz; indicative, not tested	–	300	–	Ω
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{pm}	principle main divider ratio		512	–	131071	
Reference divider input; f_{XTALIN}						
f_{XTALIN}	reference input frequency from crystal		3	–	35	MHz
$V_{XTALIN(rms)}$	sinusoidal input voltage (RMS value)		100	–	500	mV
Z_I	input impedance (real part)	f_{XTALIN} = 12.8 MHz; indicative, not tested	–	10	–	kΩ
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{rd}	reference divider ratio		8	–	4095	
Charge pump current setting resistor input; I_{SET}						
V_{SET}	voltage output on I_{SET}	R_{SET} = 12 to 60 kΩ	–	1.2	–	V
Charge pump outputs; CPA and CPB						
I_{CP}	charge pump sink or source current	R_{SET} = 15 kΩ; CRA/CRB = logic 1; $I_{cp} = I_{SET} \times 24$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	1.4	1.9	2.4	mA
		R_{SET} = 15 kΩ; CRA/CRB = logic 0; $I_{cp} = I_{SET} \times 12$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	0.7	0.96	1.2	mA
I_{LI}	charge pump off leakage current	$V_{cp} = 0.5V_{CC}$	–5	–	+5	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic input signal levels; DATA, CLK, $\overline{E}$ and HPD						
V_{IH}	HIGH level input voltage	at logic 1	$0.7V_{DD1}$	–	$V_{DD1} + 0.3$	V
V_{IL}	LOW level input voltage	at logic 0	−0.3	–	$0.3V_{DD1}$	V
I_{bias}	input bias currents	at logic 1 or logic 0	−5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	1	–	pF
Port outputs/Out-of-lock; P0/OOL, P1, P2, P3 and f_{XTALO} - open drain outputs						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

SERIAL TIMING CHARACTERISTICS

V_{DD1} = 3 V; T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r, t_f	input rise and fall times	–	10	40	ns
t_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	−20	–	–	ns
t_W	minimum inactive pulse width	4000	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

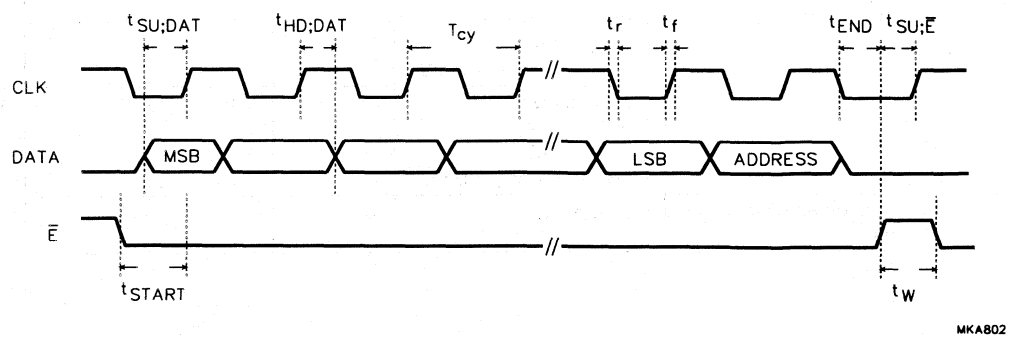
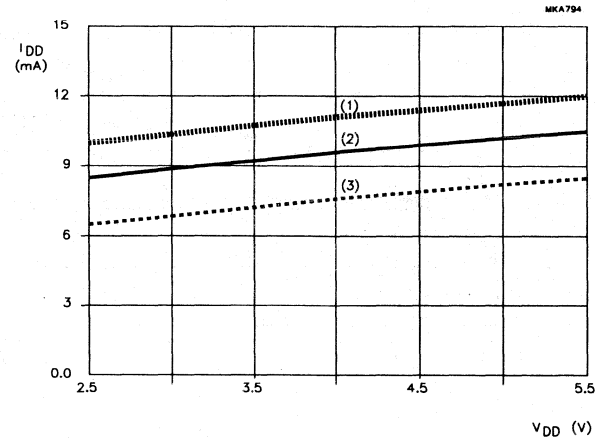


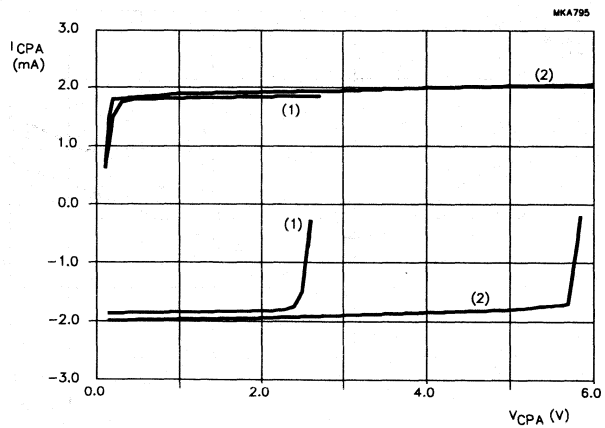
Fig.3 Serial bus timing diagram.

TYPICAL PERFORMANCE CHARACTERISTICS



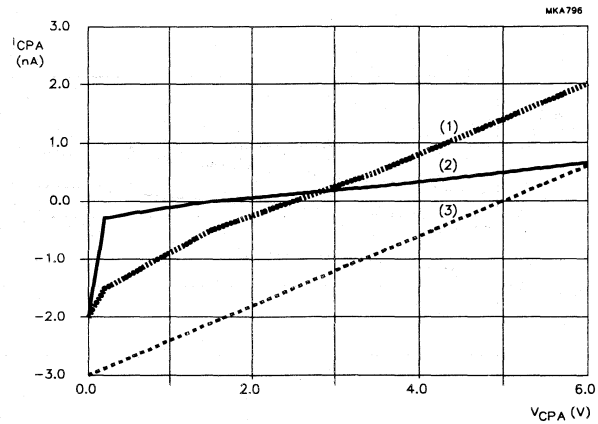
(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −30 °C.

Fig.4 I_{DD} as a function of V_{DD} with both synthesizers on and voltage doubler disabled.



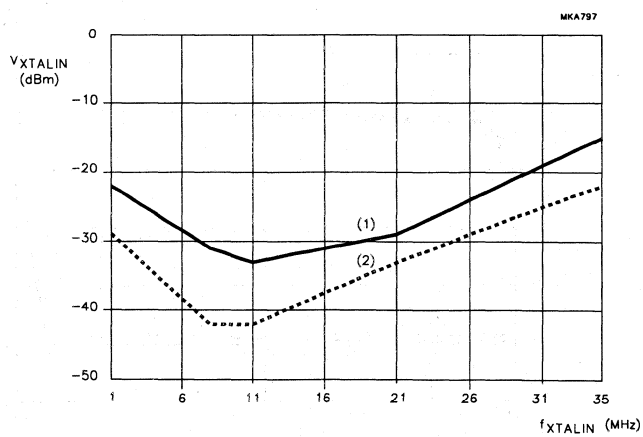
R_{SET} = 15 kΩ; CRA = 1.
(1) V_{CC} = 2.7 V.
(2) V_{CC} = 6.0 V.

Fig.5 Charge pump current as a function of CPA voltage.



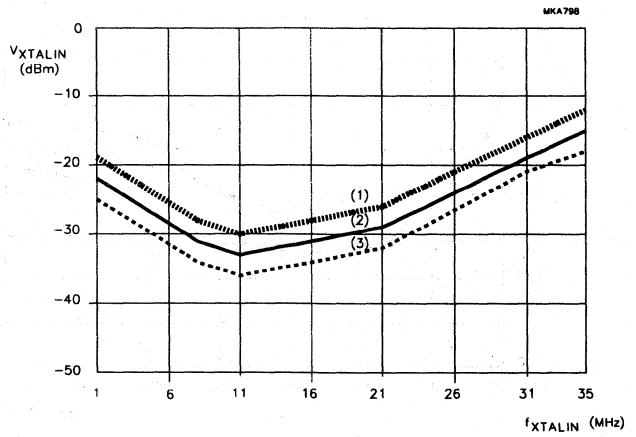
R_{SET} = 15 kΩ; CRA = 1.
(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −30 °C.

Fig.6 Charge pump 3-state current as a function of CPA voltage.



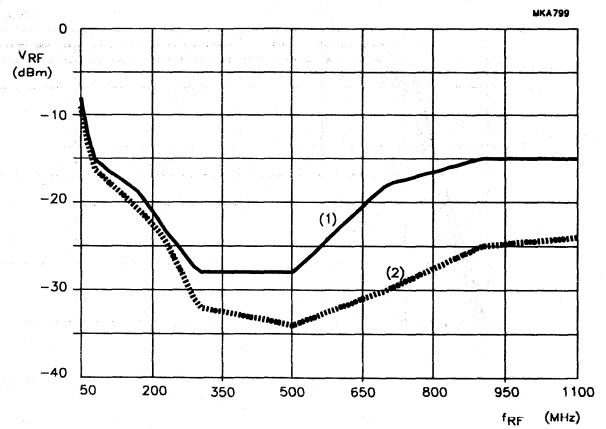
f_{XTALIN} externally terminated by 50 Ω load; AC-coupled.
(1) V_{DD} = 5.5 V.
(2) V_{DD} = 2.7 V.

Fig.7 Crystal input sensitivity as a function of input frequency.



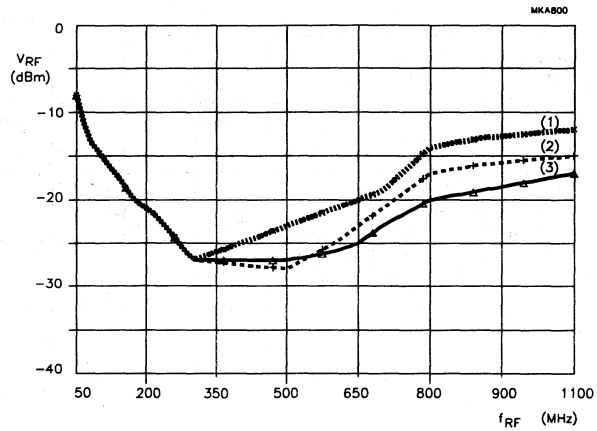
f_{XTALIN} externally terminated by 50 Ω load; AC-coupled.
(1) T_{amb} = −30 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.8 Crystal input sensitivity as a function of input frequency with V_{DD} = 5.5 V.



RF input externally terminated by 50 Ω load; AC-coupled.
(1) V_{DD} = 5.5 V.
(2) V_{DD} = 2.7 V.

Fig.9 RF input sensitivity as a function of input frequency.



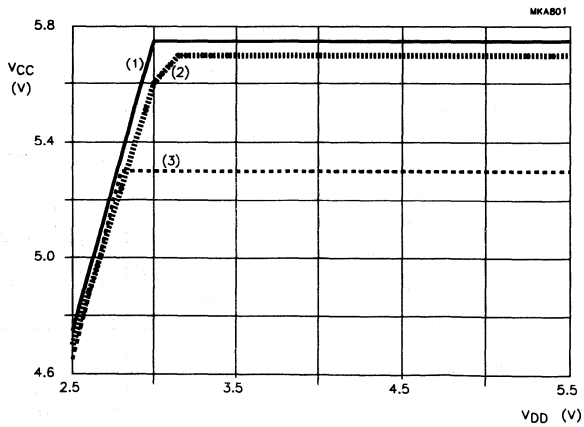
RF input externally terminated by 50 Ω load; AC-coupled.

(1) T_{amb} = −30 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = +85 °C.

Fig.10 RF input sensitivity as a function of input frequency with V_{DD} = 5.5 V.

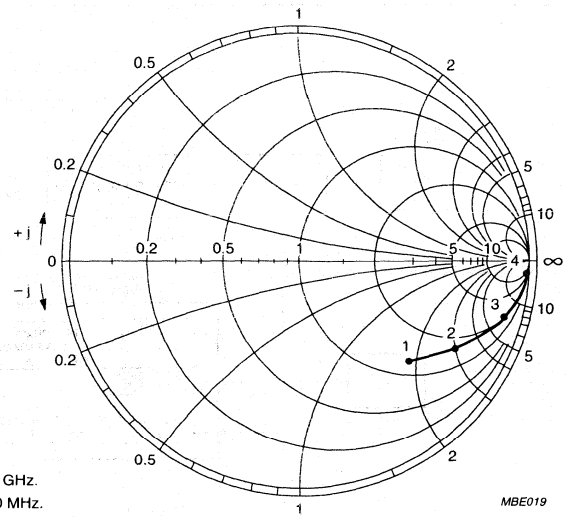


(1) T_{amb} = −30 °C.

(2) T_{amb} = +25 °C.

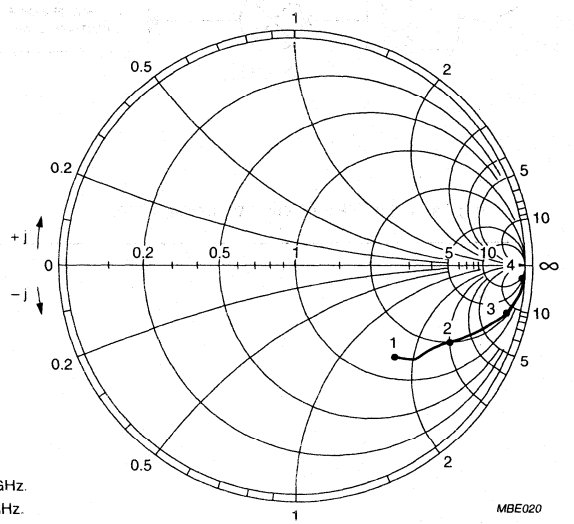
(3) T_{amb} = +85 °C.

Fig.11 Typical charge pump supply voltage as a function of V_{DD} voltage with voltage doubler enabled.



(1) 68.316 Ω, −92.457 Ω at 1.1 GHz.
(2) 85.914 Ω, −152.08 Ω at 800 MHz.
(3) 102.83 Ω, −354.66 Ω at 400 MHz.
(4) 853.75 Ω, −2.7735 kΩ at 50 MHz.

Fig.12 Input impedance as a function of input frequency; synthesizer A.



(1) 69.293 Ω, −78.027 Ω at 1.1 GHz.
(2) 100.2 Ω, −148.37 Ω at 800 MHz.
(3) 128.22 Ω, −378.81 Ω at 400 MHz.
(4) 674.25 Ω, −3.06 kΩ at 50 MHz.

Fig.13 Input impedance as a function of input frequency; synthesizer B.

APPLICATION INFORMATION

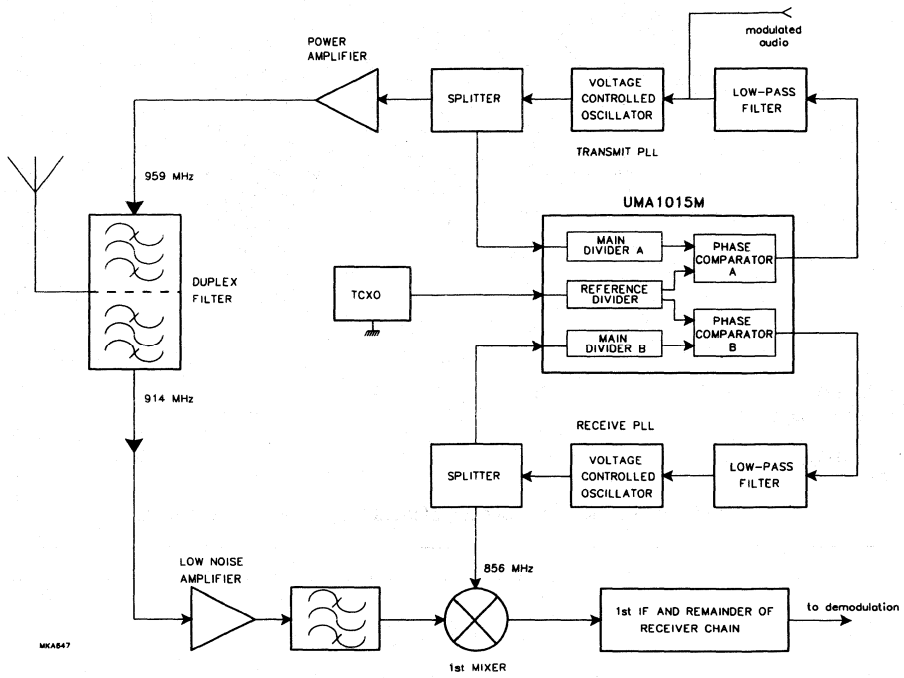


Fig.14 Typical application block diagram.

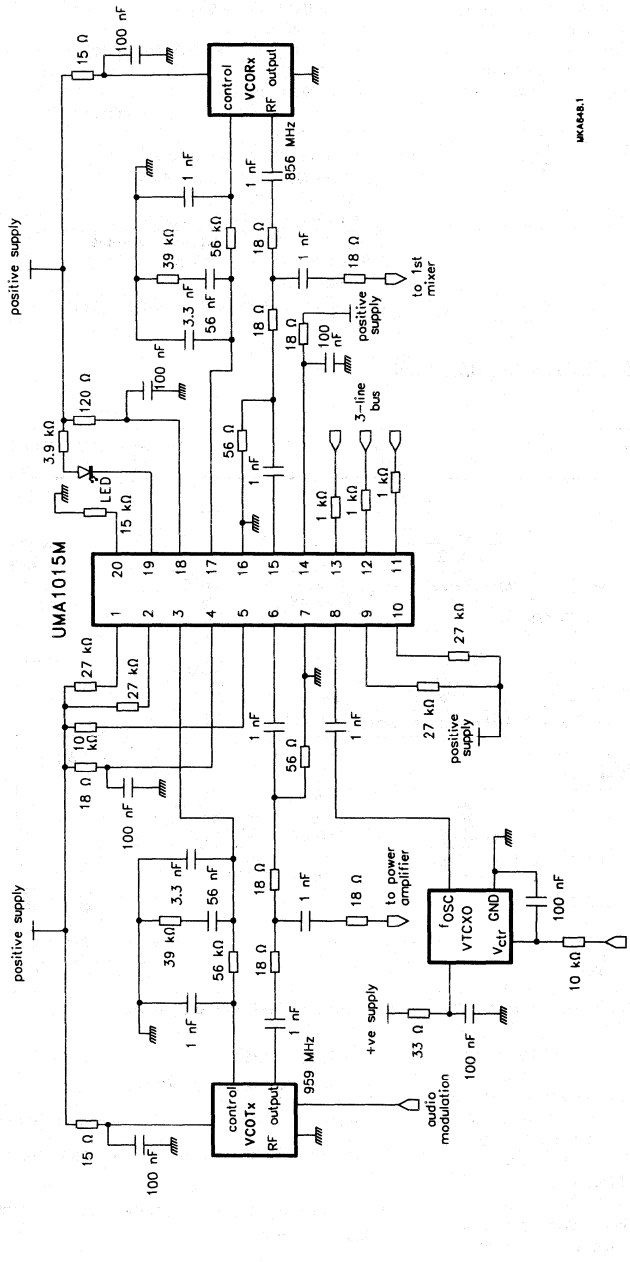


Fig.15 Typical CT1 application.

Transmit frequency = 959 MHz.
Receive frequency = 914 MHz.
1st IF = 58.1125 MHz.
2nd IF = 455 MHz.
VCO sensitivity = 2 MHz/V.
Channel spacing = 12.5 kHz.
Charge pump gain (CPA = CPB) = 1 mA/cycle.

UMA1015M low power dual 1GHz frequency synthesizer

AN93016

Author: Ir. J. J. Jacobs

SUMMARY

This application note is a guide for designing a phase locked loop based on the Philips UMA1015M dual frequency synthesizer. The UMA1015M is a low power single chip solution to dual frequency synthesis in the range 50 MHz to 1100 MHz and is primarily intended for use in analog wireless communications equipment, such as 900 MHz cordless telephone, CT1, CT1+ and cellular radio telephone AMPS, TACS and NMT.

A basic loop filter design method is discussed. Following this procedure a dual synthesizer at 900 MHz is designed and measurement results are presented.

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1 INTRODUCTION TO UMA1015M DUAL SYNTHESIZER

1.1 General Description

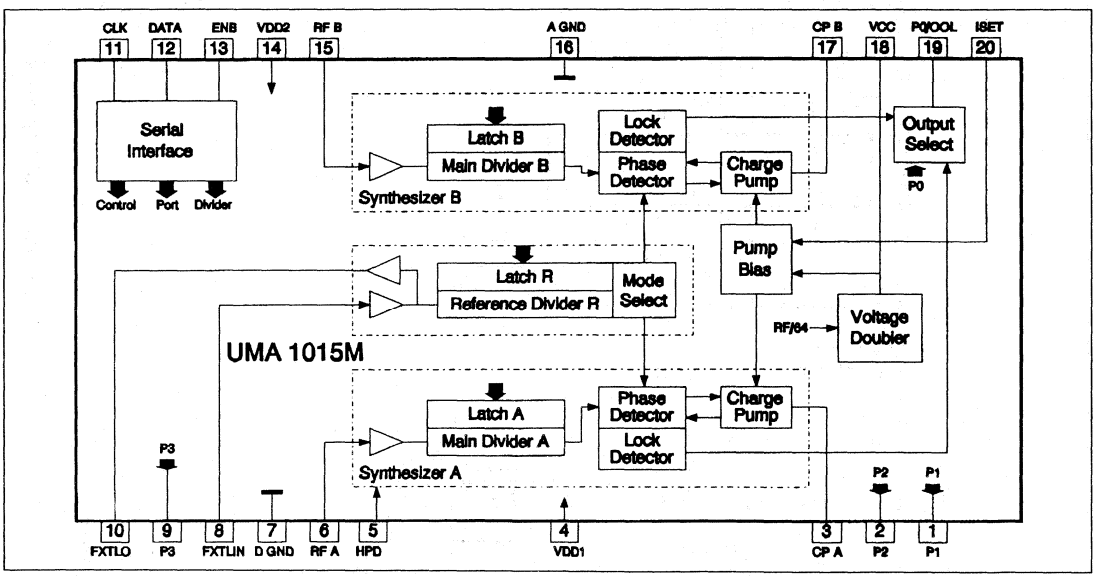


Figure 1. UMA1015M Dual Synthesizer for Mobile Radio Communications

The UMA1015M [1] is a low power dual frequency synthesizer for radio communications which operates in the 50 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz. The IC is programmed via a 3-wire serial bus which works up to 10 MHz. The programmable charge pump currents are fixed by an external resistance at pin I_{SET}. The BiCMOS device is designed to operate from 2.6 (3 Ni-Cd cells) to 5.5V. Each synthesizer can be powered down independently via the bus to save current. It is also possible to power down the chip via the pin HPD.

1.2 FEATURES

- Two synthesizers in one package
- Integrated prescalers for each synthesizer, 50 MHz to 1.1 GHz
- Reference divider common for both synthesizers, 3 MHz to 35 MHz
- Serial bus (3-line bus: data, clock, enable) for fast programming (f_{max} = 10 MHz)

UMA1015M low power dual 1GHz frequency synthesizer

AN93016

- Wide, continuous and independent ranges of division ratios:
  - 17 bits for each main divider (integer ratios between 512 and 131071)
  - 12 bits common reference divider (integer ratios between 8 and 4095)
  - In addition to the reference divider an extra divide by 2 block is selectable to set the reference frequency ratio between both synthesizers (1:1 or 1:2).
- Simple passive loop filter for typical applications
- Charge pump output current under bus control, set by external resistor, 0.1 .. 2.4 mA
- Operating voltage range 2.6 to 5.5 V for battery powered operation
- Low current consumption, 8.5 mA typically at 3 V.
- Independent power down modes for both synthesizers
- 4 multifunction output ports
  - (bus controlled, open drain, also active in power down mode)
- Programmable Out Of Lock detector/Output port (open drain)
  - (OOL synth. A, OOL synth. B, OOL synth. A or B, logic '1', logic '0')
- SSOP20 Package
- Buffered output of reference signal (open drain)
- Integrated voltage doubler for high phase detector output voltage

1.3 Typical Application Architecture

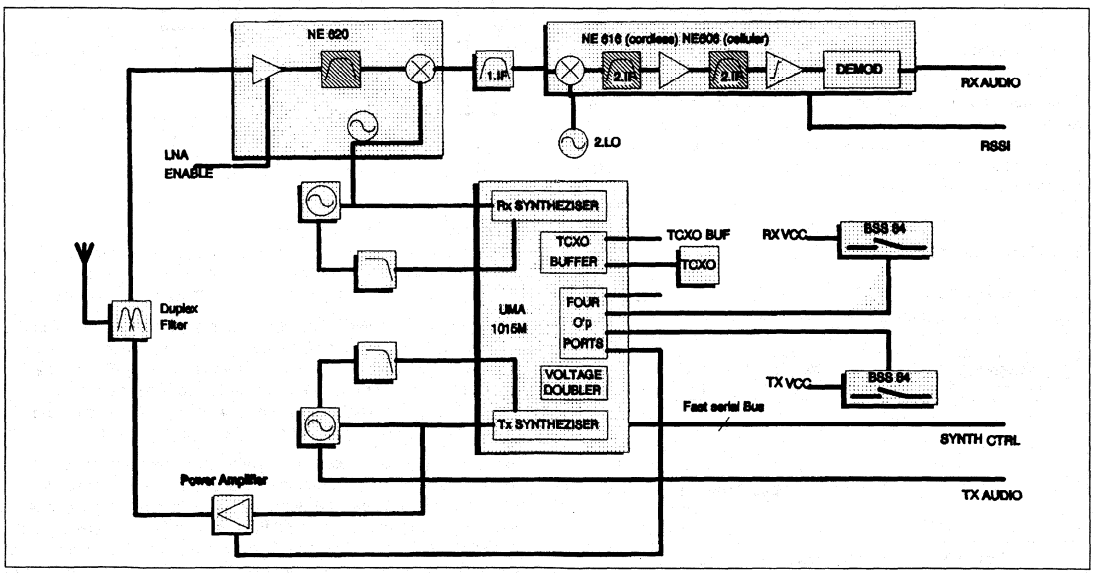


Figure 2. UMA1015M Dual Synthesizer in Typical Analog Transceiver Architecture

The UMA1015M dual synthesizer is processor controlled and notable for its flexibility in many different applications, e.g., CT1, CT1+, AMPS, TACS, NMT.

Figure 2 demonstrates the UMA1015M in an architecture commonly used in analog battery powered telecommunication equipment. The first local oscillator (LO) in the receive path and the carrier oscillator in the transmitter use PLL frequency synthesizers.

Four output ports allow processor control on miscellaneous functions in the transceiver, e.g. disable the transmit VCO or power amplifier.

The independent power down modes allow the transmit synthesizer to stand by while only the receiver periodically 'wakes up' to scan for incoming calls. When both synthesizers are in power down mode, the programmed data is retained in the synthesizer and current consumption is reduced to only 60 µA (maximum value).

For typical applications (900 MHz radio communications) a passive loop filter is sufficient, thus removing the need for operational amplifiers in the loop filter. The gain inside the loop is under bus control by switch-selecting the charge pump output current to either 12 or 24 times a value set by an external resistor at pin I_{SET}.

Programming the comparison frequency ratio select to 2:1 (as opposed to 1:1) allows optimized designs even for applications with half channel offset, such as CT1 and TACS. The comparison frequency may equal channel spacing in the receive synthesizer and half channel spacing in the transmit synthesizer.

In typical applications a temperature compensated reference oscillator will be used to provide the specified frequency stability. The reference input signal (pin 8, FXTLIN) is internally buffered and output to pin 10 (FXTLO). The buffered signal may be used as a

stable system clock or (after conversion) as the second local oscillator.

If a 9.6 MHz TCXO is used as a reference, a 1/8 divider is enough to generate a 1.2 MHz stable system clock for use in the Philips Cellular Chip Set [2].

The UMA1015M synthesizer features an on board voltage doubler. The primary use of the voltage doubler is in low voltage applications to generate VCO control voltages above the synthesizer supply voltage. The voltage doubler is enabled and disabled by programming the VDON bit via the bus. Programming the synthesizer into power down mode does not disable the voltage doubler. An external capacitor is required on pin VCC (pin 18) for smoothing. When the voltage doubler is enabled, thorough decoupling between synthesizer and VCO supply lines is necessary.

The P0/OOL signal can be used to switch the power amplifier enable line under control of the lock detect circuitry during normal 'conversation' mode to avoid false transmission if lock is unexpectedly lost. In other situations (for example when terminating a call) the processor can directly control the output of this pin by programming it to logic '1' or '0'.

Since the P0/OOL port is of open drain type, a wired-or configuration can be implemented to allow control of the transmitter to different devices, such as a micro controller. In a wired-or configuration, control of the transmitter is provided by a single line with controlling devices 'pulling low' to disable.

2 FUNDAMENTALS

2.1 Phase Lock Loop

Figure 3 depicts a generalized PLL block diagram.

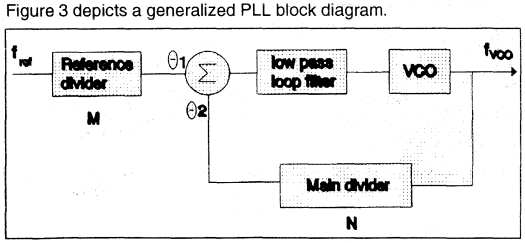


Figure 3. Main Components in Common PLL

The main parts in a common PLL are a phase detector, loop filter, voltage controlled oscillator, main divider and reference divider. In an in-lock situation the output frequency of the system is:

$$f_{VCO} = \frac{N}{M} \cdot f_{REF} \qquad (1.)$$

where f_{ref} = reference input frequency
f_{VCO} = VCO output frequency
M = reference divider division ratio
N = main divider division ratio

The inputs θ_2 and θ_1 to the phase detector are the comparison frequencies. The output of the phase detector is an error signal proportional to the difference in phase between the two input signals.

The keys for controlling the phase lock loop response are the time constants in the loop filter [3][4][5]. Frequency synthesis always involves PLL performance compromise: keeping loop bandwidth as wide as possible to reduce acquisition time and VCO noise, and at the same time suppressing reference frequency sidebands that can pass through wide bandwidths. But stability, being an absolute necessity, gets priority. The other two requirements, unfortunately, are inversely dependent and must be traded off against each other.

2.2 Phase comparator & charge pump

The two phase comparators in the UMA1015M dual synthesizer are sensitive to both phase and frequency. They react to small frequency differences between the inputs and have a highly linear response characteristic. The design responds to the full 360° range of phase inputs and control the charge pumps.

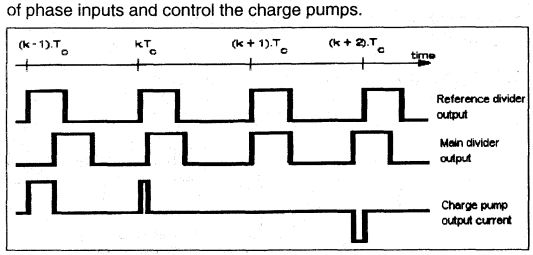


Figure 4. Timing Diagram

The phase comparator outputs are configured as charge pumps (current sources) so that the loop filters (integrators) can be designed with simple, passive components. The charge pumps drive the synthesizer loop filter to generate the VCO control voltages.

The operation principle of the phase detectors is depicted in figure 4. The comparison frequency f_c at the inputs of the phase comparator is typically the same as the system channel spacing. The phase comparison is performed once in each period of the reference signal. The duration between the comparisons is T_c, which is the reciprocal of f_c. Lower case letter k is an arbitrary index.

The charge pump outputs of the synthesizers are tri-state outputs. When in lock, i.e. when the phase error at the inputs of the phase comparator is zero, the charge pump output is in high impedance state. When the loop is unlocked the charge pump sources current pulses when the output of the reference divider is leading and sinks current pulses when lagging the main divider output. The duration of the pulses is proportional to the phase error. The sinking and sourcing pulses charge or discharge the capacitors in the loop filter.

To prevent cross talk between both synthesizers, the design of the chip assures that both charge pumps are never active simultaneously during normal operation.

The charge pump current (the 'height' of the positive or negative pulses in figure 4) is switch-selectable by software (bits CRA and CRB) and continuously adjustable via an external resistor.

The charge pump current is set by an external resistance R_{SET} at pin I_{SET}, where a temperature independent voltage of 1.2 volt is generated. R_{SET} should be between 12 kΩ and 60 kΩ to give an I_{SET} of 100 µA and 20 µA respectively. The charge pump current, I_{CP}, can be programmed for each synthesizer to be either (12 x I_{SET}) or (24 x I_{SET}) with the maximum being 2.4 mA.

Larger currents are used for fast switching. Smaller currents allow use of smaller capacitors but may make the system more susceptible to interferences and noise.

3 LOOP FILTER DESIGN

This chapter presents a loop filter design procedure in two parts:

- A basic design procedure yields approximate values for the main components.
- A PC based simulation program is used for analysis and optimization.

3.1 Basic Design Procedure

The basic design procedure yield approximate values for the components in the loop filter depicted in figure 5.

The procedure resorts to second-order loop approximations and describes the loop behavior in terms of its natural frequency f_n and damping ratio ζ. The natural frequency of the loop refers to the resonant frequency of the loop. The damping refers to the damping of this resonant frequency [3][4][5].

a: select basic loop and synthesizer parameters:

- output signal frequency, f_{VCO}, [Hz]
- VCO gain, K_{VCO}, [Hz/V]
- switching time, t_{sw}, [s]
- comparison frequency, f_{comp}, [Hz] (equals channel spacing or half channel spacing)
- loop damping factor, ζ , unitless (select ζ =0.707 for fastest switching, ζ =1 for low overshoot)
- charge pump output current, I_{CP}, [A]

b: calculate main division ratio and approximate natural frequency of loop from switching time requirement:

- main division ratio, $N = \frac{f_{VCO}}{f_{comp}}$ (2.)
- natural frequency, $f_n = \frac{2}{t_{SW}}$ (3.)

c: calculate resistor R_{SET} for setting charge pump output current

- resistor at I_{SET} pin, $R_{SET} = \frac{1.2 \cdot CRx}{I_{CP}}\ \Omega$ (4.)

where CRx = 24 if CRA/CRB bit is programmed to 1
CRx = 12 if CRA/CRB bit is programmed to 0

d: calculate approximate loop component values:

- main capacitor, $C_1 \approx K_{VCO} \cdot \frac{I_{CP}}{N \cdot (2\pi f_n)^2}$ (5.)
- damping resistor, $R_1 \approx 2 \cdot \zeta \sqrt{\frac{N}{K_{VCO} \cdot I_{CP} \cdot C1}}$ (6.)
- filter capacitor, $C_2 \approx \frac{C_1}{10}$ (7.)

The loop filter components calculated above are approximations and can be used as starting values for further analysis and optimization.

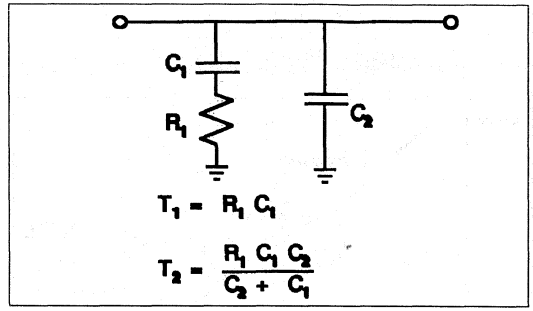


Figure 5. Second-Order Loop Filter

3.2 Analysis and Optimization

For analysis, optimization and worst case design of more complex filters, key loop parameters can be entered into a software analysis program to verify loop stability and switching time, for example SIMPATA [6]. Simpata is an interactive menu driven Phase Lock Loop design tool that runs on a personal computer and comes with a user manual. Among others the program can generate Bode Plots.

Figure 6 depicts a third order filter. The filter results from adding a low pass RC filter stage to the second order filter from the previous paragraph. The extra filter stage can reduce comparison frequency breakthrough spurs without slowing down the response of the loop.

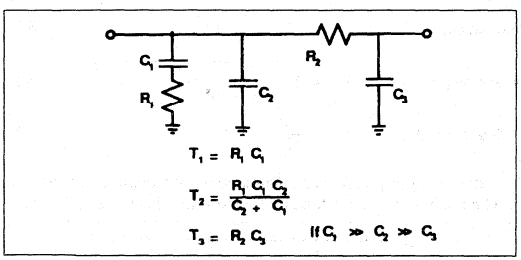


Figure 6. Third-Order Loop Filter

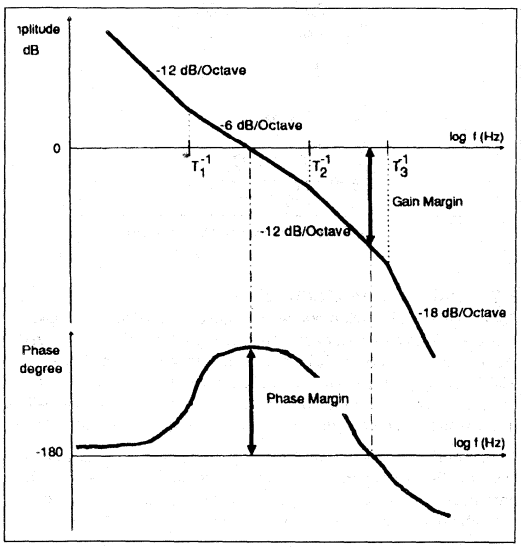


Figure 7. Bode Plot 4th-Order Open Loop Transfer Function Magnitude and Phase

A damping factor to control stability as in simpler second-order loops can not be readily defined in a higher-order loop. Instead, the phase margin becomes important.

The phase margin is easily evaluated and determined from the Bode plot. A Bode plot is a pair of graphs which displays the open loop transfer function magnitude and phase. In figure 7 shows Bode plot of a fourth order loop with third order filter and a pole in the origin due to the VCO.

The phase margin is defined as the difference between 180 and the phase of the open loop transfer function at the frequency where the logarithmic gain is 0 dB (gain cross over). The critical point for stability is a phase margin of 0 . The factor by which the system gain would have to be increased for the phase margin to reach the critical value of 0 is called the gain margin.

The time constants in the loop filter are the keys for controlling the loop performance and phase margin. The effects of different time constants can be evaluated from a Bode diagram. The reciprocal of the time constants of the loop filter in figure 6 are the breakpoints of the magnitude function in figure 7.

When increasing the time constant $T_3 = C_3.R_2$, the breakpoint T_3.[1] will move left and the magnitude curve will start to roll off at a lower frequency. Therefore, the greater the time constant T_3, the better the comparison frequency breakthrough is suppressed. But increasing T_3 will force the point of inflection of the phase margin curve to move to the left as well, thus decreasing the phase margin and eventually making the system unstable.

Iteratively inspecting the Bode plot, adjusting the loop components and measuring performance, will yield a compromise between switching time and stability. Simulation programs may give reasonable approximations of PLL behavior, but their accuracy is always limited due to the fact that many practical imperfections and non linearities are not taken into account.

The phase margin should be between 30 and 70 for most applications. The larger the phase margin, the more stable the loop, and the slower the response.

A loop with a low phase margin is still stable but may exhibit other problems aside from outright oscillation. A low phase margin makes the transient response more oscillatory and requires very tight tolerances on all loop components, i.e. the phase margin must be positive over all variations in loop components.

A phase margin of 45° is often a good compromise between desired stability and the other generally undesired effects.

4 APPLICATION EXAMPLE

This chapter discusses the design and performance of the UMA1015M demo board.

The UMA1015M demo board demonstrates the UMA1015M dual synthesizer at frequencies in the AMPS (Advanced Mobile Phone System) cellular radio band. The circuit consists of two PLLs with 6 main parts: one temperature compensated crystal oscillator, one UMA1015M comprising two synthesizers, two loop filters and two VCOs.

Auxiliary functions are also demonstrated such as the output ports which can be programmed to power up/down the oscillators.

Circuit diagram and PCB layout are included in the appendix.

4.1 Loop filter design example

To accommodate for a fast receive synthesizer and a slower transmit synthesizer, the charge pump current I_{CP} to I_{SET} ratio is programmed to 12 for the transmitter and 24 for the receiver. On the demoboard the charge pumps currents are I_{CP} = 0.9 mA for the receiver (synthesizer A) and I_{CP} = 0.45 mA for the transmitter (synthesizer B).

Basic design procedure for AMPS receive synthesizer:

- VCO frequency, F_{VCO} = 920 MHz
- VCO gain, K_{VCO} = 11 MHz/V (from VCO specifications)
- Comparison frequency, F_{comp} = Channel spacing = 30 kHz (AMPS specification)
- Reference frequency, $F_{reference}$ = 9.6 MHz (arbitrarily, can have system advantage)

- switching time, t_s , 9 ms (indicative, for 10 MHz jump to within 1 kHz)
- I_{cp} , 0.9 mA, with CRA bit set to 1

Following the basic design procedure from paragraph 3.1 yields:

- main division ratio, $N = \frac{f_{VCO}}{f_{comp}} = \frac{918MHz}{30kHz} = 30,600$ (8.)
- natural frequency, $f_n = \frac{2}{t_{SW}}$

$$= \frac{2}{9 \cdot 10^{-3}} \approx 220Hz \quad (9.)$$

- resistor at pin I_{SET}: $\frac{1.2 \cdot CRx}{I_{CP}}$

$$= \frac{1.2 \cdot 24}{0.9 \cdot 10^{-3}} \approx 33k\Omega \quad (10.$$

The main components in the loop filter are:

- main capacitor, $C_1 \approx K_{VCO} \cdot \frac{I_{CP}}{N \cdot (2\pi f_n)^2}$

$$= 11 \cdot 10^6 \cdot \frac{0.9 \cdot 10^{-3}}{30,600 \cdot (2\pi \cdot 220)^2} \approx 180nF \quad (11.$$

- damping resistor, $R_1 \approx 2\zeta \sqrt{\frac{N}{K_{VCO} \cdot I_{CP} \cdot C_1}}$

$$= 2 \cdot 0.707 \sqrt{\frac{30,600}{11 \cdot 10^6 \cdot 0.9 \cdot 10^{-3} \cdot 180 \cdot 10^{-9}}}$$

$$= 5.8k\Omega \quad (12.$$

- filter capacitor, $C_2 \approx \frac{C_1}{10} \approx 18nF$ (13.

The above values for the main components in the receive synthesizer are only approximations as they are based on second order assumptions. For further optimization both a computer simulation program as well as practical experiments are used.

For trying out different component values in the loop filter, adjustable components can be used. The PLL performance can then be evaluated for various component values in the loop filter to find an optimum compromise of loop filter components with respect to the required performances.

Capacitors with leakage currents, such as electrolytic capacitors and capacitors with piezo or delay effects are not preferred because of higher reference breakthrough spurious responses.

For designing the demo board the main performance criteria for optimization were: fast switching, low residual FM and low comparison frequency breakthrough as measured with respectively a time domain analyzer, a frequency modulation analyzer and a spectrum analyzer.

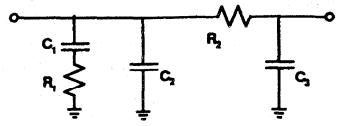
During the optimization process, the software simulation program SIMPATA was used to verify the stability of the design. Figure 9 depicts the Bode plot of synthesizer A on the demo board. The loop gains falls at 6 dB/Octave at the gain cross over point. The requirement for basic loop stability is fulfilled since the phase margin is 52°.

The design procedure of the transmit synthesizer is similar to the above procedure for the receive synthesizer. The main difference is that in typical applications restrictions are imposed on the bandwidth of the loop filter of the transmit synthesizer. To allow audio modulation of the VCO, the loop filter bandwidth must be well below the lowest audio frequency, i.e. well below 300 Hz.

The loop filter components on the UMA1015M demoboard are summarized in Table 1.

Table 1. Design Parameters and Simulation Results UMA1015M Dual Synthesizer Demoboard

Parameter		Slow Transmit Synthesizer B	Fast Receive Synthesizer A
Loop filter components (reference Figure 8 below)		C_1 = 200nF	C_1 = 200nF
		C_2 = 33nF	C_2 = 15nF
		C_3 = 6.8nF	C_3 = 2.2nF
		R_1 = 10kΩ	R_1 = 6.8kΩ
		R_2 = 6.8kΩ	R_2 = 22kΩ
VCO	Gain, K_{VCO}	11MHz/V	11MHz/V
	VCO center frequency, F_{VCO}	836MHz	926MHz
	VCO frequency range	25MHz	25MHz
Comparison frequency ratio synthesizer A : B		ratio 1 : 1	
Comparison frequency, f_{comp}		30kHz	30kHz
Charge pump	Current I_{CP}	0.45mA	0.9mA
	R_{SET}	33kΩ	
	I_{SET} ratio, bits CRA, CRB	12	24
Reference	Frequency (TCXO)	9.6MHz	
	Division ratio	320	
Unity gain phase margin (simulated)		42°	52°
Gain margin at 180° phase margin (simulated)		24dB	23dB
Unity gain phase margin (simulated)		225Hz	330Hz



$$T_1 = R_1 C_1$$

$$T_2 = \frac{R_1 C_1 C_2}{C_2 + C_1}$$

$$T_3 = R_2 C_3 \qquad \text{If } C_1 \gg C_2 \gg C_3$$

Figure 8. Loop Filter Components

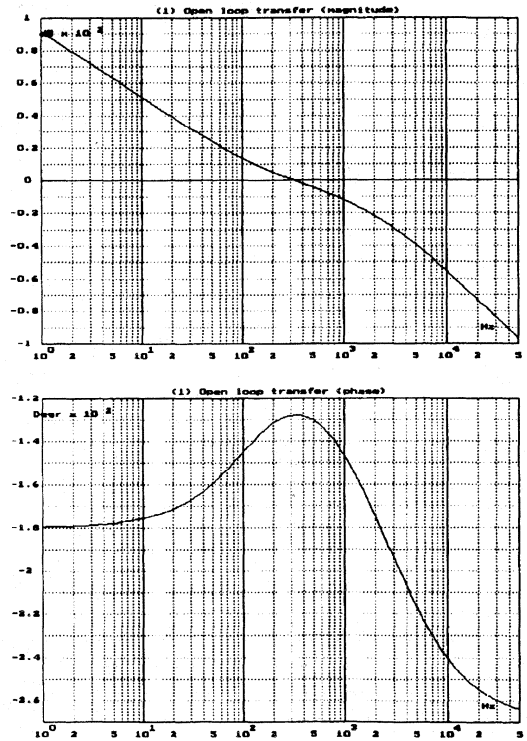


Figure 9. Simulated Bode Plot of 4th-Order Open Loop Transfer Function of Synthesizer A on UMA1015M Demoboard, Magnitude (above) and Phase (below) vs. Frequency

4.2 Performance of Design Example

This section describes the performance measured of the UMA1015M dual synthesizer demo board UMA1015M, designed in the previous paragraphs.

Important performance criteria for a frequency synthesizer are usually:

Close-in phase noise (i.e., noise level within the loop bandwidth relative to carrier)

Noise level at a specified distance from the carrier

Comparison breakthrough components

Switching time for specified frequency jump to within specified distance from target

Residual FM

Power consumption

It should be noted that these criteria can be traded off against each other to some extent to tailor overall performance, and that the performance described here is only one compromise between the various criteria. In general, the choice of a low loop bandwidth will improve the comparison frequency breakthrough and will filter out more of the close-in noise, but will result in a longer switching time. The use of a higher order filter can improve comparison frequency breakthrough with little effect on the noise or switching time. The noise floor at offsets significantly higher than the loop bandwidth is dominated by the VCO characteristics.

Table 2 summarizes the measurement results. Figures 10 to 12 show some measurement graphs from which the numbers in table 2 are read. During the recording of the measurement results, both synthesizers were enabled and locked.

Table 2. Results UMA1015M Dual Synthesizer Demoboard

Measurement results UMA1015M dual synthesizer demo board. Data are extracted from a limited number of engineering samples and do not indicate typical values. VCO supply voltage: 4.2V, both synthesizers enabled; UMA1015M supply voltage: 4.2V, room temperature.

Parameter		Fast Receive Synthesizer A	Slow Transmit Synthesizer B
VCO frequency range		914–939 MHz	824–849 MHz
Residual FM (CCITT weighted, RMS)		13.5 Hz RMS	8.5 Hz RMS
Comparison frequency breakthrough	at 30kHz	71 dBc	90 dBc
Switching time for frequency jump around center frequency to within 2.5kHz off the target frequency	30kHz (single channel)	2.6 ms	2.9 ms
	10MHz	6.2 ms	9.5 ms
	25MHz (maximum jump)	7.5 ms	10 ms
VCO noise level relative to carrier, at specified distance from carrier, normalized	120Hz (close-in)	–57 dBc/Hz	–57 dBc/Hz
	45kHz (adjacent channel)	–116 dBc/Hz	–116 dBc/Hz
Current consumption UMA1015M (Voltage doubler disabled)	Both synthesizers enabled	9.1 mA	
	Transmitter disabled; Receiver enabled	5.2 mA	
	Both synthesizers disabled	approx. 0.007 mA	

Figure 10 shows the transient response of synthesizer A for a 10 MHz frequency jump to within 2,5 kHz of the target to be 6.2 ms.

Figures 11 and 12 demonstrate the noise spectrum of synthesizer B with narrow (2 kHz) and wide (50 kHz) frequency span respectively. The markers in Figure 10 indicate the close-in noise to be 57 dB/Hz below carrier power level. Also from figure 10 the width of the noise plateau indicates that the loop band width is around 230 Hz, which is in accordance with design targets.

Figure 12 reveals an outstanding low comparison frequency (at 30 kHz) breakthrough of more then 90 dB below the carrier power level (below noise level). The low comparison frequency breakthrough allows a trade off of the comparison breakthrough against faster switching.

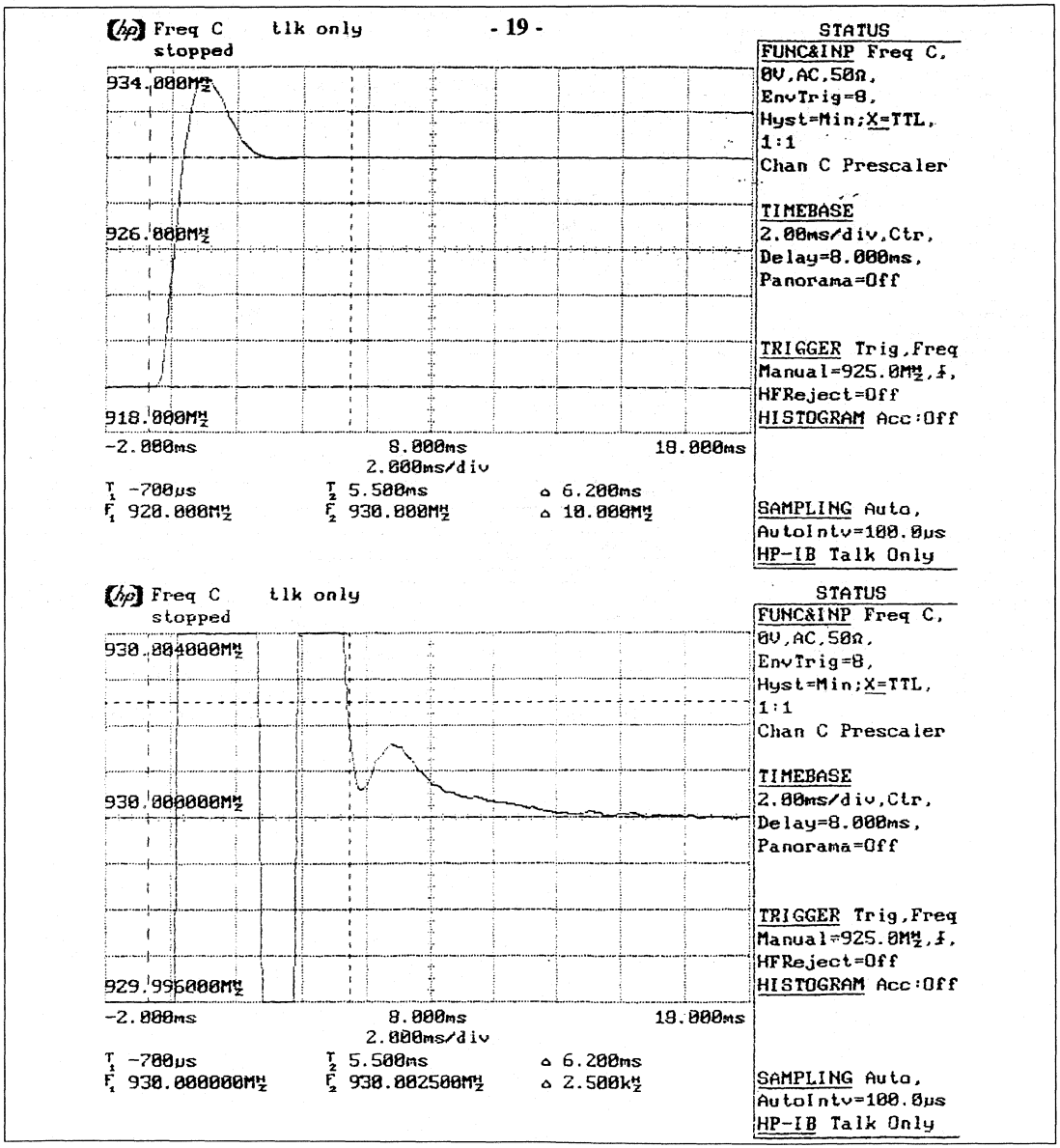


Figure 10. UMA1015M Demoboard, Transient Response Synthesizer A. 6.2ms for 10MHz Jump to Within 2.5kHz Off Target Frequency.

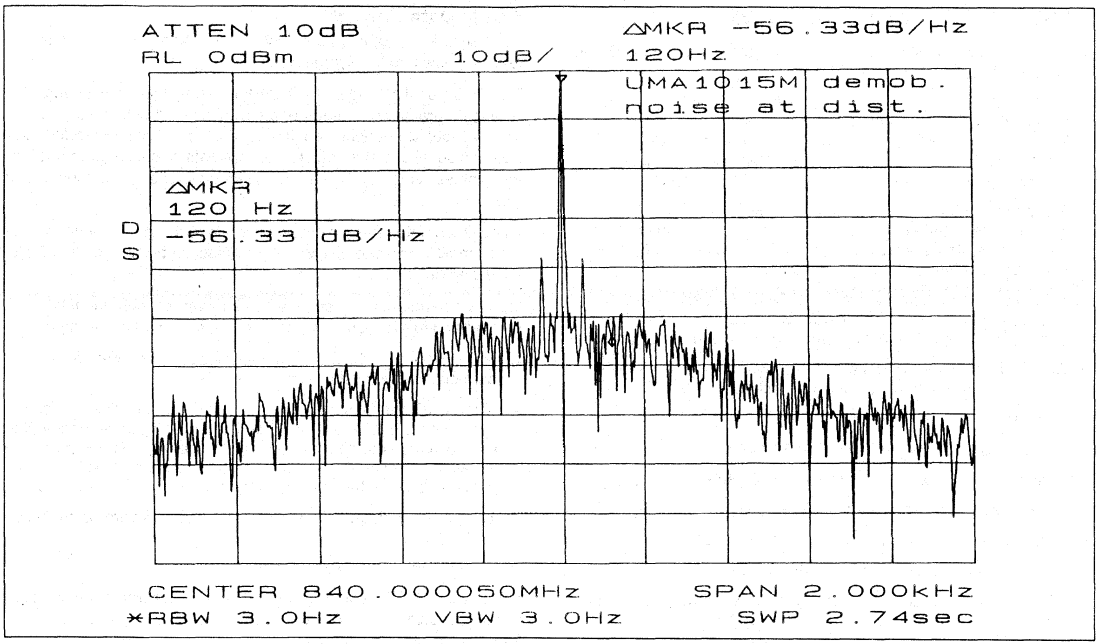
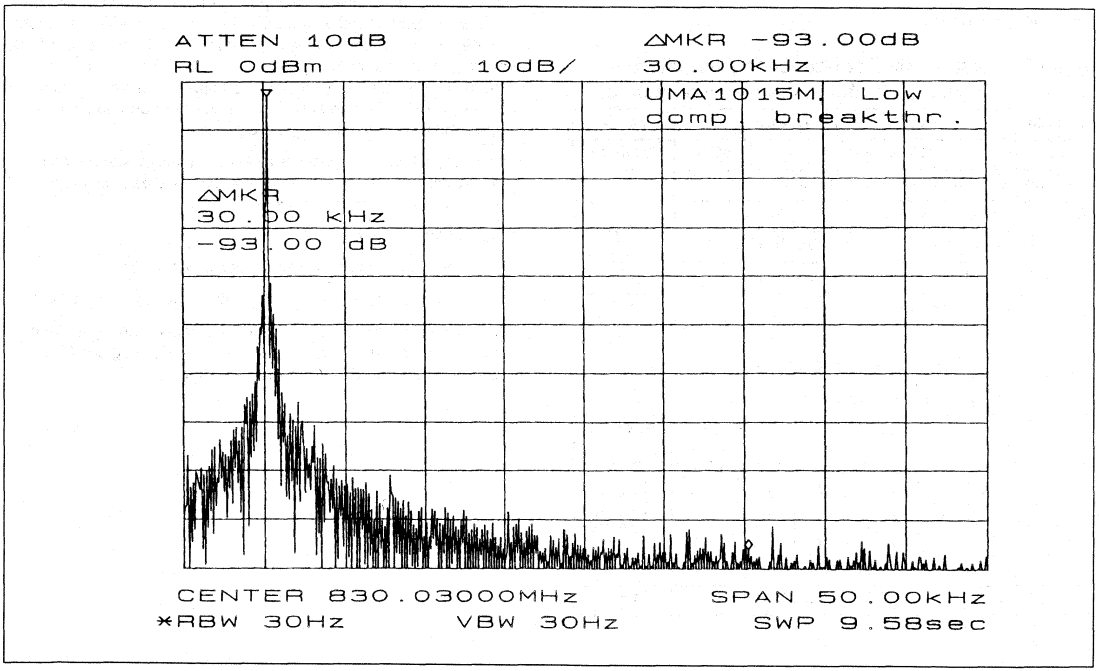


Figure 11. UMA1015M Demoboard, Frequency Spectrum Synthesizer B, 2kHz Span. Close-in Noise: 56dB/Hz Below Carrier.



5 FREQUENTLY ASKED QUESTIONS

Q. How to use the synthesizer with V_{DD} < 4.5V whereas pins DATA, CLK and ENB are at 5V logic?

A. A. Because of protection against electrostatic discharges, the input voltage for these logic pins can not be greater than V_{DD}+0.3V. An interface between the microcontroller and the synthesizer is then needed to reduce voltage at bus pins. A voltage divider is a simple and cheap solution to implement.

The design of this voltage divider (see below) involves performance compromise between the current consumption and the programming speed, which depend on R1, R2 and Cpar, a parasitic capacitance from the demo board.

A Technical Marketing Report (n° CTT94008) describes some measurements results : for different values of V_{DD} <4.5V, the current consumption and the programming speed are given.

Q. The example below shows a typical programming example of the UMA1015M with the following conditions :

– fxtal input frequency : 9.6 MHz

– Synthesizer A input frequency : 926.01 MHz

– Synthesizer A comparison frequency : 30 kHz

– Synthesizer B input frequency : 836.01 MHz

– Synthesizer B comparison frequency : 30 kHz

– Both synthesizers ON (sPDA = sPDB = 1)

– Out of lock indication from both synthesizer loops (OLA = OLB = 1)

– Charge pumps currents : $I_{CPA} = 24*I_{SET}$ (CRA = 1)

$I_{CPB} = 12*I_{SET}$ (CRB = 0)

– Voltage doubler disabled (VDON = 0)

Table 3. UMA1015M Register Data Allocations Expressed in Decimal and Hexadecimal

First In	Register Bit Allocation		Last In
dtl6	Data Field	dt10	Address
Test register (must be 0 if programmed)			0h
Control register = 0 0001 1100 0110 0000			1h
Synth A main divider coefficient = 30867d = 7893h			4h
Reference divider coefficient = 320 d = 140h			5h
Synth B main divider coefficient = 27867d = 6CDBh			6h

Table 4. UMA1015M Register Data Allocations Expressed in Binary

First In (MSB)								Data Field								Last In (LSB)	Address		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	1
0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	1	1	0	1	0	0
0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	1
0	0	1	1	0	1	1	0	0	1	1	0	1	1	0	1	1	0	1	1	0

About Data Format

Special care has to be taken for correct programming when first applying power to the synthesizer.

The ENB signal should be held LOW and only taken HIGH after having programmed an appropriate register on first powering up. If this condition is not achieved, it may result in loading of random data from the serial bus shift register (programming register) into one of the synthesizers data registers/ addressed latches including the test register.

It should be noted that the test register does not normally need to be programmed. However, if it is programmed, all bits in the Data Field should be set to 0.

In case of random data being loaded into the test register, it is recommended to program a frame of zeros, on first powering up.

Q. How to use the TCXO output buffer stage to generate an harmonic of the crystal frequency?

A. The TCXO output is an open drain MOS output. The aim is to generate a signal at a multiple of the crystal input frequency. The most common method is to use a non-linear circuit, for instance a biased amplifier stage and to use a LC output circuit tuned to some multiple of the input frequency.

The following diagram is a proposal to obtain a third harmonic on pin fxtalo.

Q. About PCB layout considerations

Since careful PCB layout has a great impact on performances of RF circuitry, special attention should be paid when designing the frequency synthesizer layout.

To avoid crosstalk between synthesizers (A and B), the printed circuit board should have a solid ground plane on the non surface mount side (apart from isolated pads for non-grounded connections to leaded components). On the surface mount side of the board, the ground plane should be designed round each synthesizer, and underneath the integrated circuit so as to provide maximum isolation between two PLLs. A good number of plated-through holes must connect the two layers of the ground plane.

Power supply bypass capacitors (100 nF) in series with a small value resistor (12 Ω) should be located as close as possible to the device with short leads for pins 4 and 14.

Q. Out-of-lock indication

The Out-of-Lock functions works in such a way that :

– when $_e > T_{OOL}$ with $T_{OOL} = 80/ f_{RF}$, the OOL signal goes LOW

– for coming back into lock, $_e$ has to be smaller than T_{OOL} during 8 reference cycles. Then, the OOL signal goes HIGH again. This procedure is described on the following diagram.

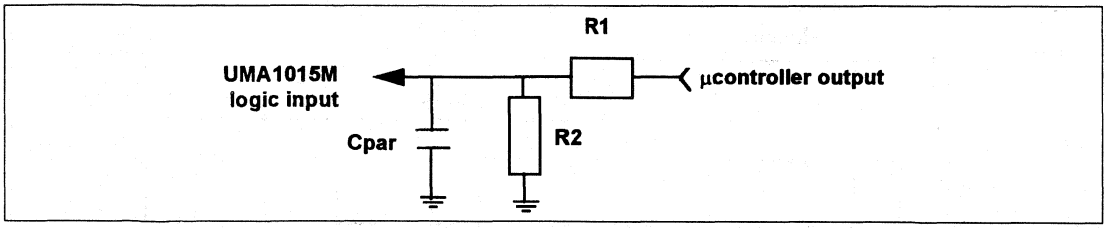


Figure 13. Out-Of-Lock Indication

6 REFERENCES

1. *Product Datasheet UMA1015M*, Philips Semiconductors, 22 June 1995.
2. Data Handbook 1993 *RF/Wireless Communications*, p. 851–895: Cellular Chip Set Design Guide, Philips Semiconductors 1993
3. Gardner, Floyd M., *Phaselock Techniques*, 2d ed., John Wiley & Sons. New York 1979
4. Rohde, Ulrich L., *Digital PLL Frequency synthesizers, Theory and Design*, Prentice–Hall, Englewood Cliffs, New Yersey 1983
5. Best, Roland E., *Phase–Locked Loops, Theory, design, and Applications*, 2d ed., McGraw–Hill, New York 1993, includes disk for PLL simulations
6. *SIMPATA*, PLL simulation program and manual, Philips CTT NatLab, Eindhoven, The Netherlands, 1992. Information or ordering: tel (+31)40–744212, fax (+31)40–744619
7. Technical Marketing Report (CTT94008), *Use the UMA1015M Synthesizer at V_{DD} under 4.5V with serial bus at 5V Logic*, Philips Semiconductors, 1994.

7 APPENDIX UMA1015M DEMOBOARD DATA SHEETS

UMA1015M demo board circuit diagram, PCB layout, component listings.

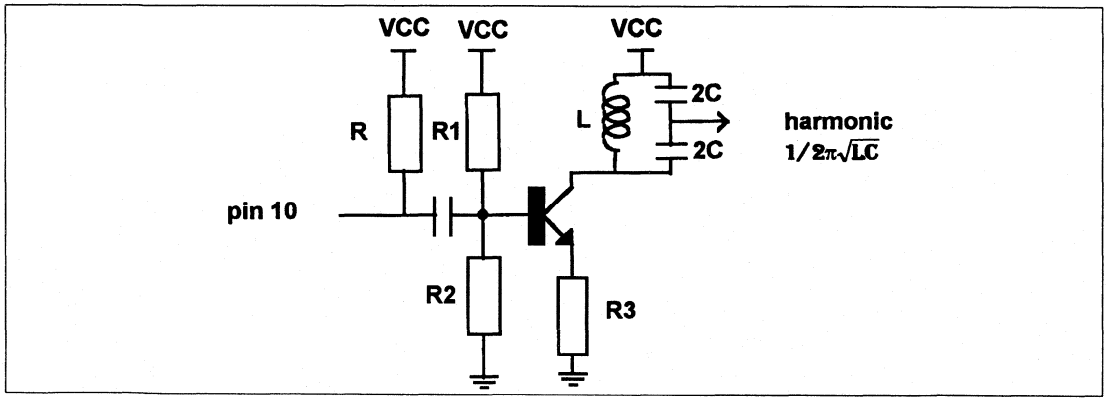


Figure 14.

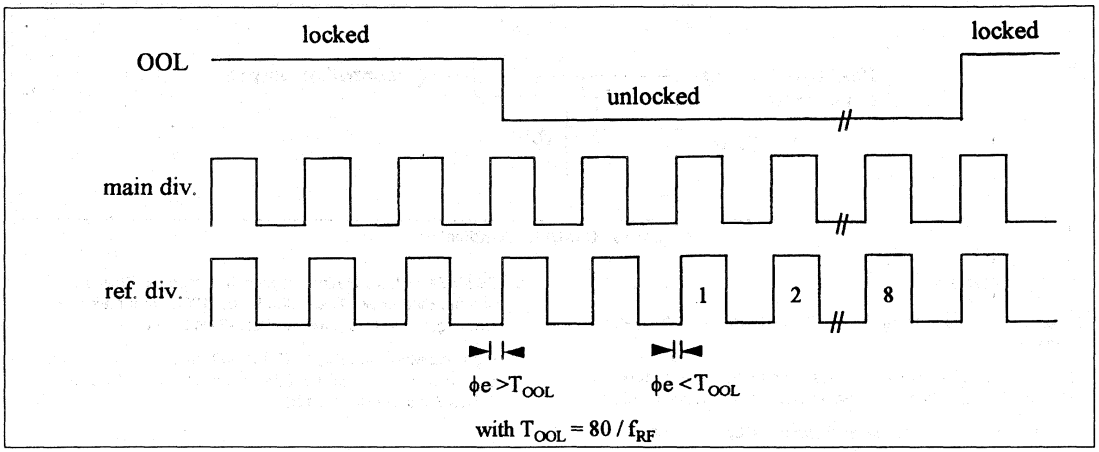

locked
locked
OOL
unlocked
main div.
ref. div.
1
2
8
φe >T_OOL
φe <T_OOL
with T_OOL = 80 / f_RF

Figure 15.

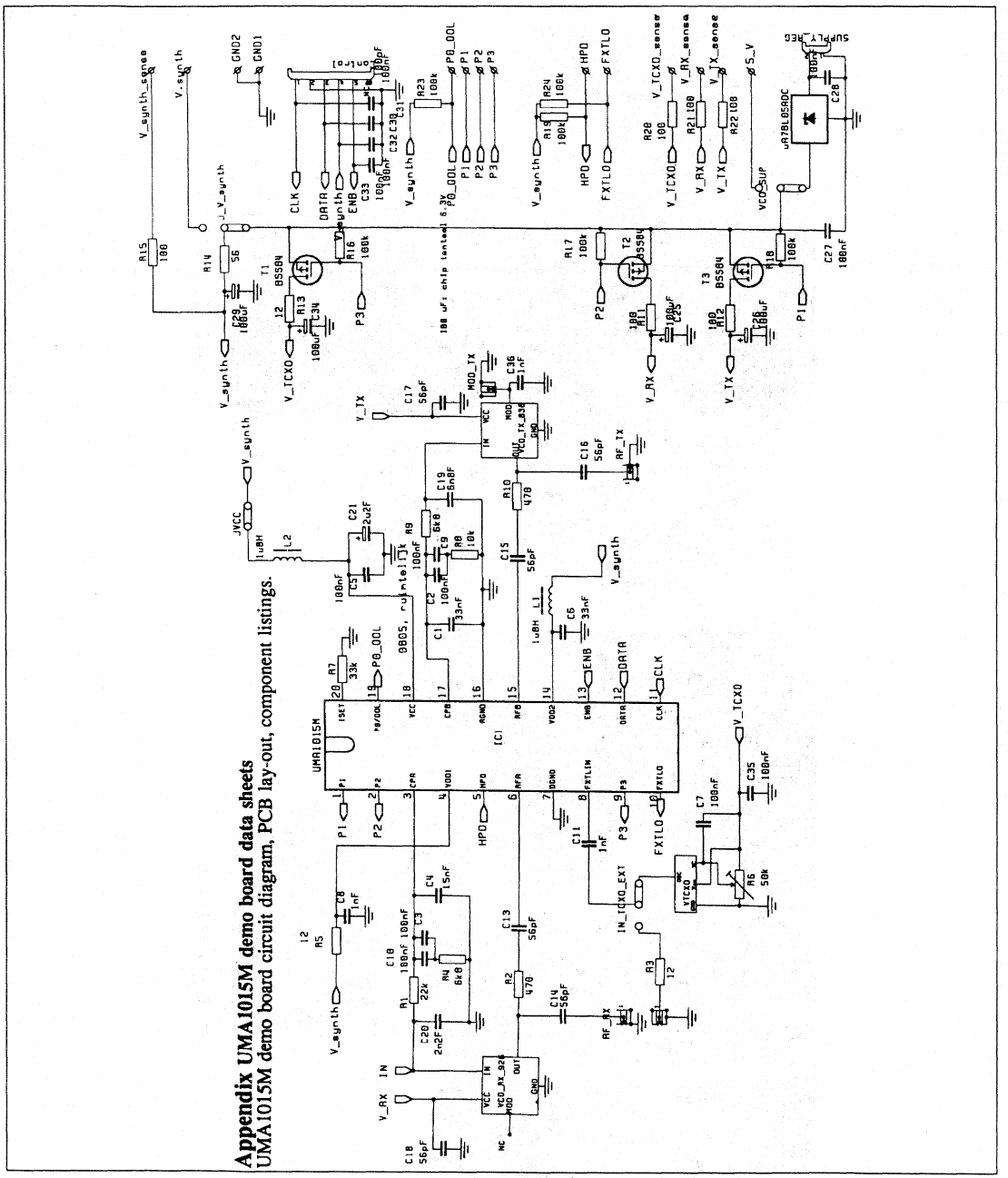

Appendix UMA1015M demo board data sheets
UMA1015M demo board circuit diagram, PCB lay-out, component listings.
UMA1015M
IC1
BS584
uA78L05ADC
VTCXO
VCO_TX_836
VCO_RX_926
0805, rutinel 1k
100 uF; chip tantal 6.3V

Figure 16.

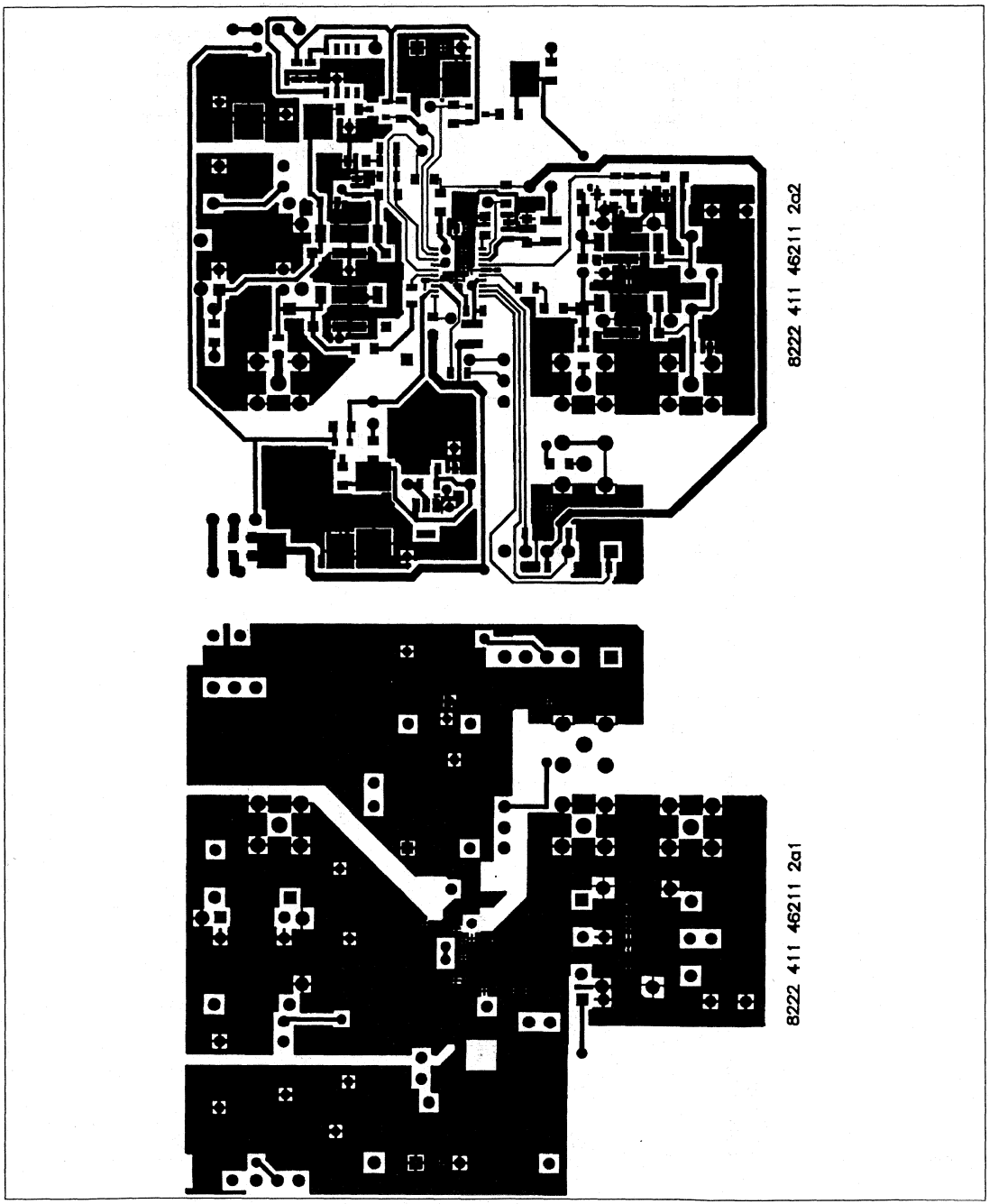


Figure 17.

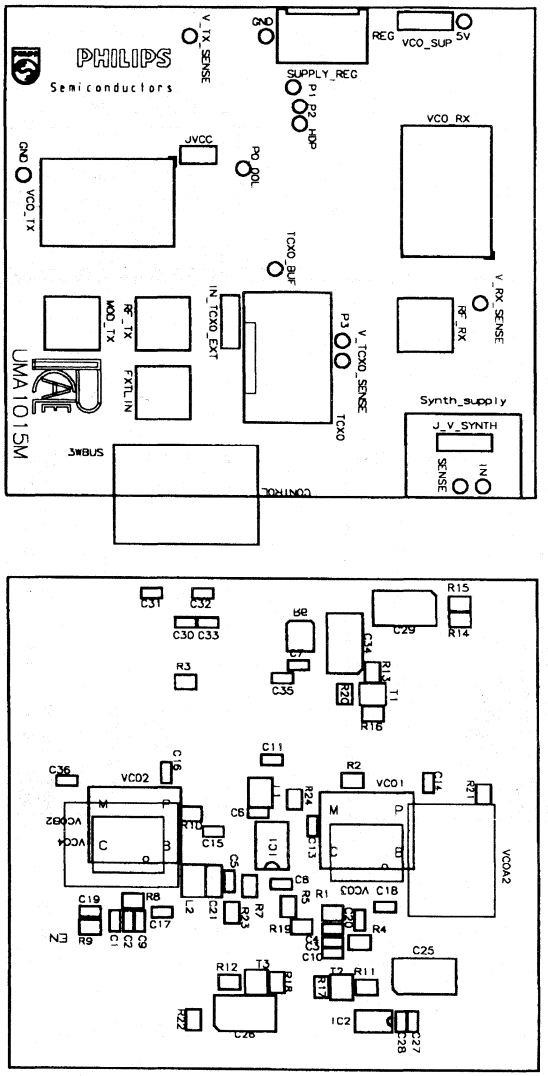
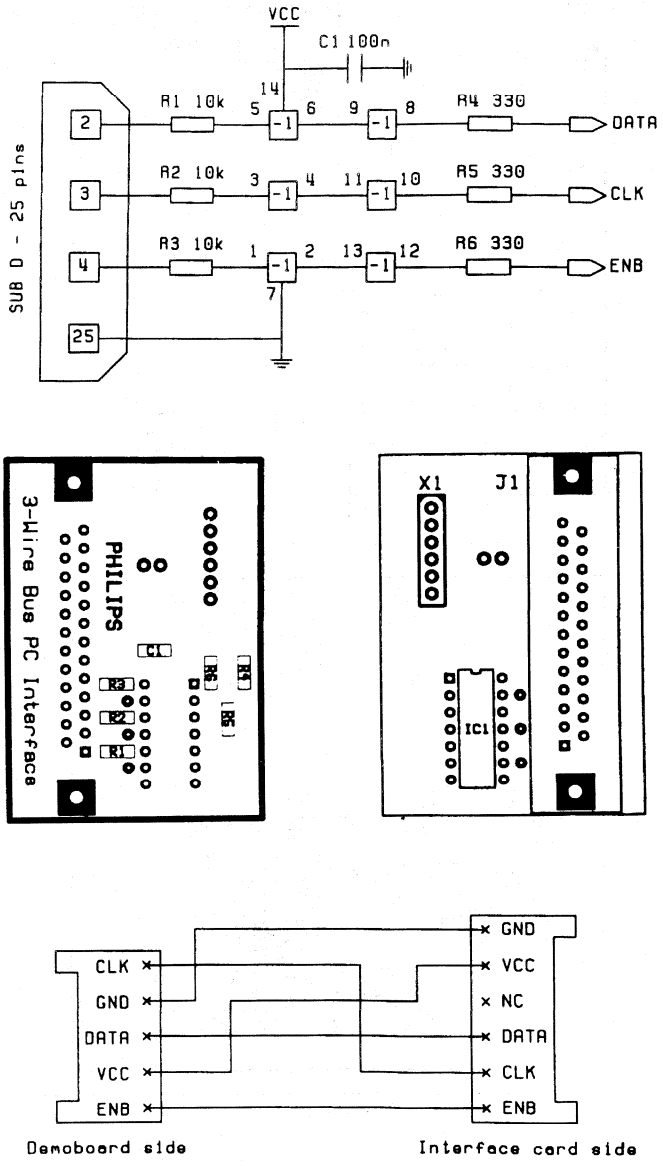

PHILIPS
Semiconductors
V_TX_SENSE
GND
REG
VCO_SUP
5V
SUPPLY_REG
P1
P2
HDP
VCO_RX
JVCC
PO_OOL
GND
VCO_TX
TCXO_BUF
V_RX_SENSE
RF_RX
IN_TCXO_EXT
P3
V_TCXO_SENSE
RF_TX
MOD_TX
FXTL_IN
UMA1015M
TCXO
Synth_supply
J_V_SYNTH
SENSE
IN
3WBUS
CONTROL
C31
C32
C30 C33
R15
R14
C29
C34
C7
C35
R3
R13
T1
R20
R16
C11
C16
C36
VCO2
R2
VCO1
C14
R21
R24
C6
VCOB2
VCO4
R10
C15
C13
VCOA2
C5
C8
C18
C19
R8
R5
R1
VCO3
R7
R23
R19
R4
C17
C20
C2
C9
C1
R9
EN
C3
C10
C25
R12
T3
R18
T2
R11
R17
R22
C26
IC2
C27
C28

Figure 18.



Interface card pcb layout and cable connection.

Figure 19.

Low-voltage frequency synthesizer for radio telephones UMA1017M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 900 MHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1017M BICMOS device integrates prescalers, a programmable divider, and phase comparator to implement a phase-locked loop.

The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The synthesizer operates at RF input frequencies up to 1.25 GHz. The synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. Digital supplies V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} must be equal to or greater than V_{DD} (i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range).

The phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	supply current		–	7.7	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	10	–	μA
f_{VCO}	RF input frequency		50	–	1250	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		−30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1017M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

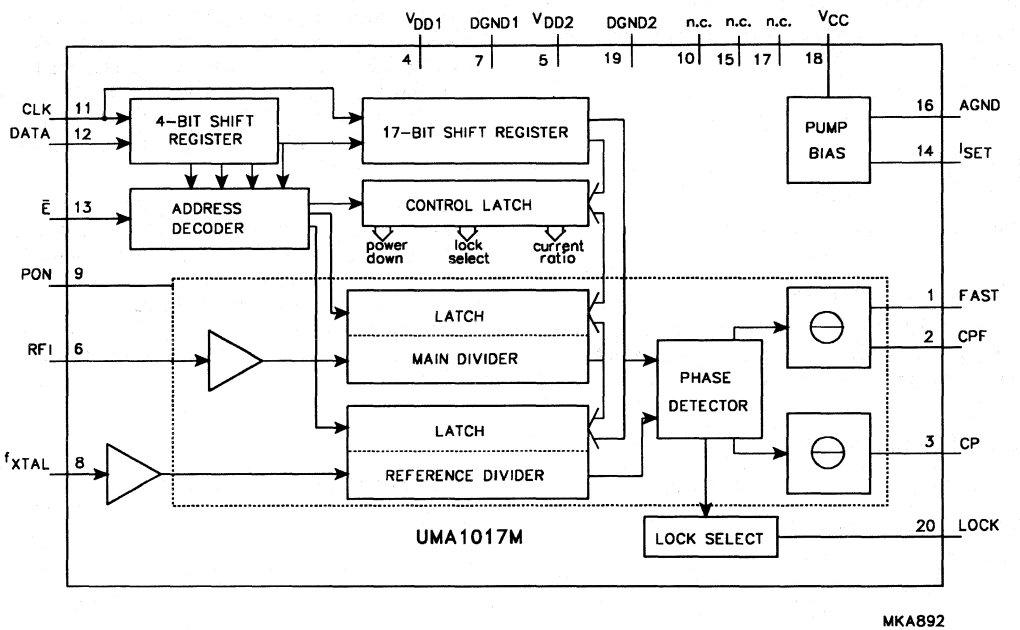


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPF	2	speed-up charge-pump output
CP	3	normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
RFI	6	1 GHz RF main divider input
DGND1	7	digital ground 1
f_{XTAL}	8	crystal frequency input from TCXO
PON	9	power-on input
n.c.	10	not connected
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
n.c.	15	not connected
AGND	16	analog ground
n.c.	17	not connected
V_{CC}	18	supply for charge-pump
DGND2	19	digital ground 2
LOCK	20	in-lock detect output; test mode output

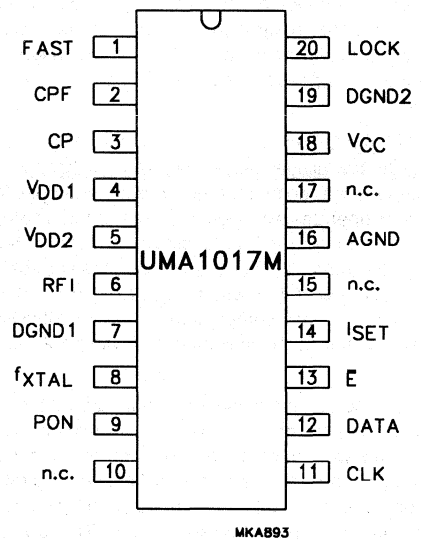


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

Programmable reference and main dividers drive the phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input PON (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The RFI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 50 mV up to 225 mV (RMS), and at frequencies as high as 1.25 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divider ratios (512 to 131071) allow a 1 MHz phase comparison with a 500 MHz RF input, and a 10 kHz phase comparison with a 1.25 GHz RF input.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to reduce noise and breakthrough levels.

The synthesizer speed-up charge pump (CPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector thereby improving linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μA. The output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison, an out-of-lock or an in-lock flag is generated. The out-of-lock function can be disabled via the serial bus.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

However when the synthesizer is powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1017M uses 4 of the 16 available addresses. These are chosen to allow direct compatibility with the UAA2072M integrated front-end. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To ensure that data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Power-down mode

The device can be powered-down either by hardware PON or by software sPON. The dividers are on when both PON and sPON are at logic 1.

When the synthesizer is reactivated after power-down, the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

Table 1 Format of programmed data

LAST IN			PROGRAMMING REGISTER BIT USAGE					FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT					REGISTER BIT ALLOCATION															LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS(2)																	0	0	0	0
X	X	X	X	OOL	X	CR1	CR0	X	X	sPON	X	X	X	X	X	X	0	0	0	1
PM16	MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1

Notes

1. FT = first; LT = last; sPON = software power-up for synthesizer (1 = ON); OOL = out-of-lock (1 = enabled).
2. The test register should not be programmed with any other values except all zeros for normal operation.

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; bias current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
$\Delta V_{CC}-V_{DD}$	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8, 9, 11 to 14 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3}$	voltage at pins 2 and 3	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	$V_{DD} = 5.5$ V	–	6.5	8.5	mA
I_{CC}	charge pumps and analog supply current	$V_{CC} = 5.5$ V; $R_{ext} = 12$ kΩ	–	1.2	2.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF main divider input; pin 6						
f_{VCO}	RF input frequency	$2.7 \text{ V} < V_{DD} < 3.5$ V	50	–	1250	MHz
		$2.7 \text{ V} < V_{DD} < 5.5$ V	50	–	1100	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω; $2.7 \text{ V} < V_{DD} < 3.5$ V; $0.5 < f_{VCO} < 1.25$ GHz; $T_{amb} = -20$ to +85 °C	50	–	225	mV
		$R_s = 50$ Ω; $2.7 \text{ V} < V_{DD} < 5.5$ V; $0.5 < f_{VCO} < 1.1$ GHz; $T_{amb} = -30$ to +85 °C	100	–	300	mV
		$R_s = 50$ Ω; $2.7 \text{ V} < V_{DD} < 5.5$ V; $50 < f_{VCO} < 500$ MHz; $T_{amb} = -30$ to +85 °C	150	–	300	mV
Z_I	input impedance (real part)	$f_{VCO} = 1$ GHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_m	main divider ratio		512	–	131071	
f_{PCmax}	maximum phase comparator frequency		–	2000	–	kHz
f_{PCmin}	minimum phase comparator frequency		–	10	–	kHz
Crystal reference divider input; pin 8						
f_{XTAL}	crystal reference input frequency		5	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	$4.0 \text{ V} < V_{DD} < 5.5$ V	50	–	500	mV
		$2.7 \text{ V} < V_{DD} < 5.5$ V	50	–	250	mV
Z_I	input impedance (real part)	$f_{XTAL} = 30$ MHz	–	6	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_r	reference divider ratio		8	–	2047	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		−25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	V_{cp} = ½V_{CC}	−5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	V_{CC} − 0.4	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage		−0.3	–	0.3V_{DD}	V
I_{bias}	input bias current	logic 1 or logic 0	−5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	2	–	pF
Lock detect output signal; pin 20 (open-drain output)						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	4000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 4 μs provided all the following conditions are satisfied:

   a) Main divider input frequency $f_{VCO} > \frac{256}{t_W}$

   b) Reference divider input frequency $f_{XTAL} > \frac{3}{t_W}$

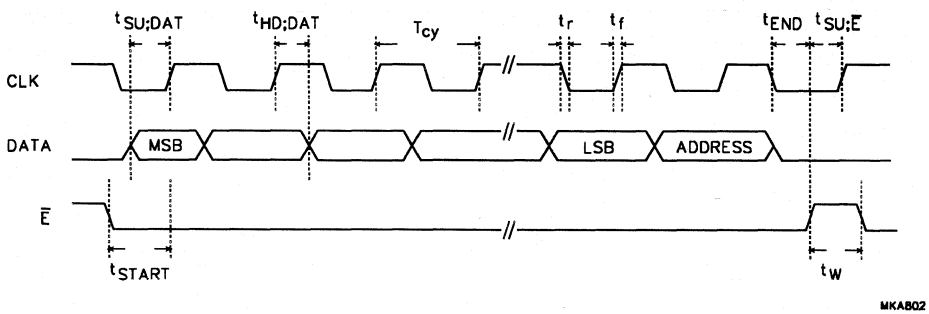


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

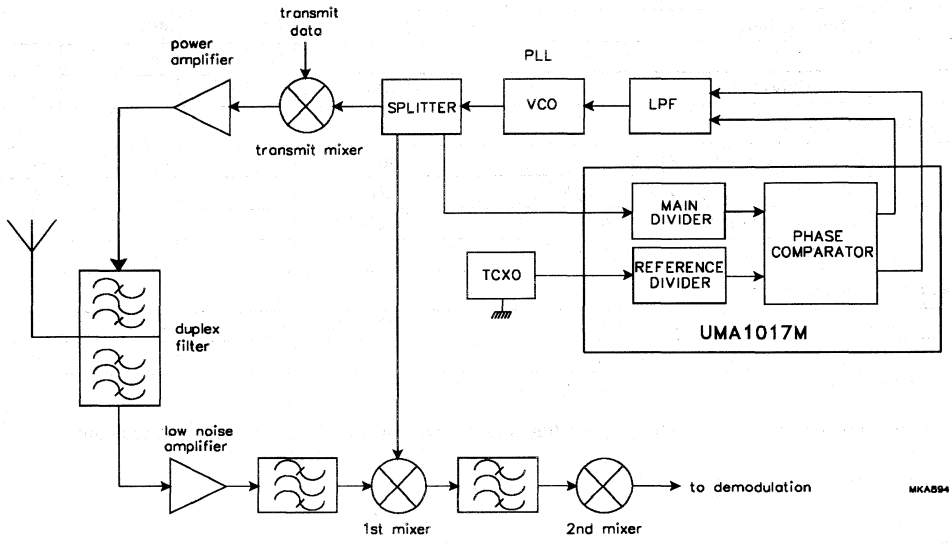


Fig.4 Typical application block diagram.

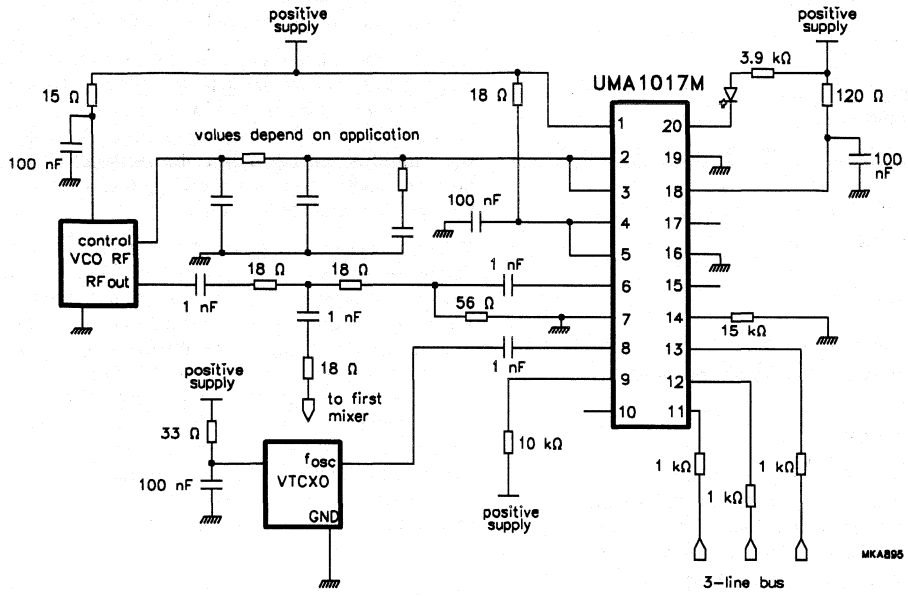


Fig.5 Typical test and application diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1018M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Integrated digital-to-analog converter
- Dual power-down modes.

APPLICATIONS

- 900 MHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1018M BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at RF input frequencies up to1.25 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. Digital supplies V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} must be equal to or greater than V_{DD} (i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range).

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance. An on-chip 7-bit DAC enables adjustment of an external function, such as the temperature compensation of a crystal oscillator in Global System for Mobile communications (GSM).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	principal synthesizer supply current	auxiliary synthesizer in power-down mode	–	7.7	–	mA
	principal and auxiliary synthesizer supply current	principal and auxiliary synthesizers ON	–	10	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	μA
f_{VCO}	principal input frequency		50	–	1250	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principal phase comparator frequency		–	200	–	kHz
f_{APC}	auxiliary phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1018M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

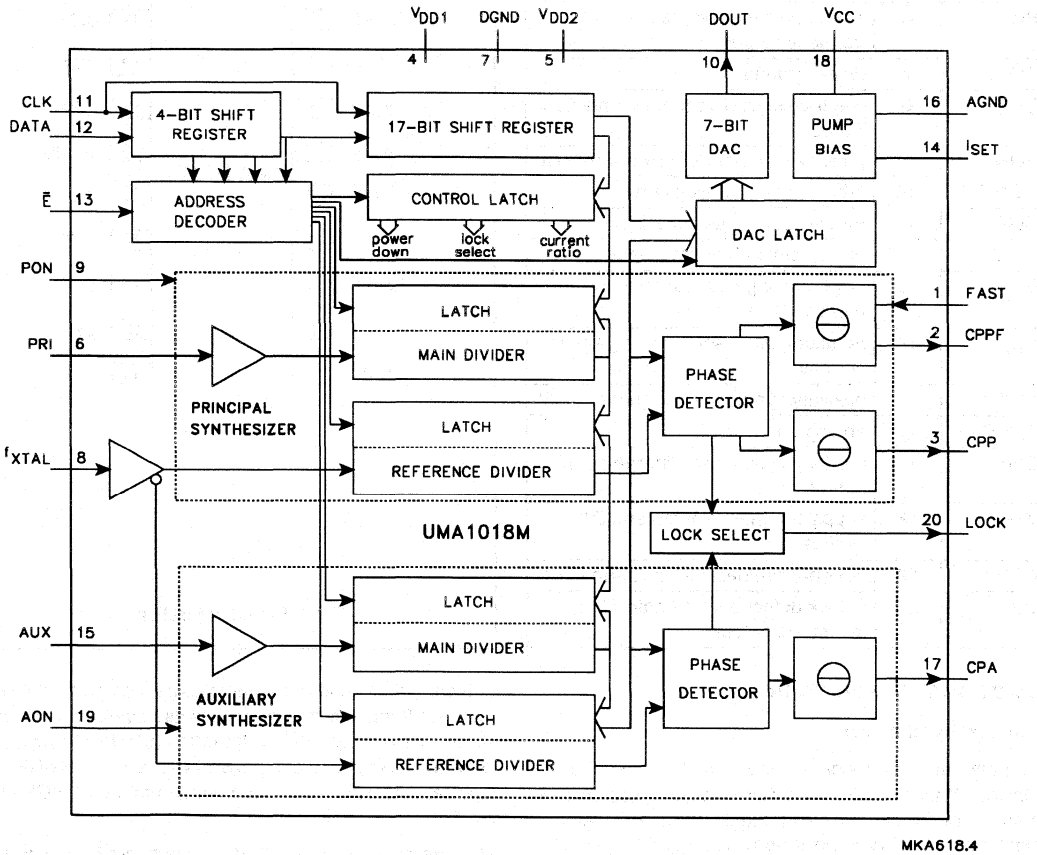


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principal synthesizer speed-up charge-pump output
CPP	3	principal synthesizer normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
PRI	6	1 GHz principal synthesizer frequency input
DGND	7	digital ground
f_{XTAL}	8	common crystal frequency input from TCXO
PON	9	principal synthesizer power-on input
DOUT	10	7-bit digital-to-analog output
CLK	11	Programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump and DAC circuits
AON	19	auxiliary synthesizer power-on input
LOCK	20	in-lock detect output (main PLL); test mode output

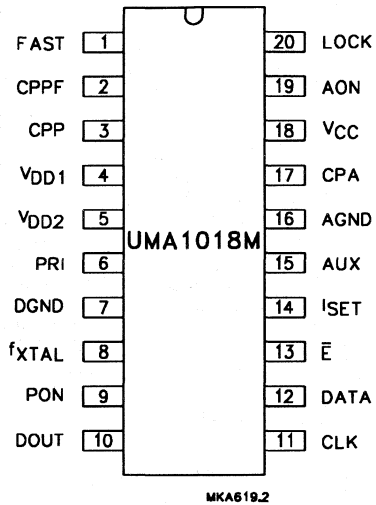


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input PON (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 50 mV up to 225 mV (RMS), and at frequencies as high as 1.25 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divider ratios (512 to 131 071) allow a 1 MHz phase comparison with a 500 MHz RF input, and a 10 kHz phase comparison with a 1.25 GHz RF input.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down.

The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to reduce noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector thereby improving linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 μA. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AON (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the principal reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However, when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first.
The leading bits make up the data field, while the trailing four bits are an address field. The UMA1018M uses 6 of the 16 available addresses. These are chosen to allow direct compatibility with the UAA2072M integrated front-end. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To ensure that the data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.
The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data

LAST IN	PROGRAMMING REGISTER BIT USAGE							FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	REGISTER BIT ALLOCATION																				LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21	
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS				
TEST BITS[2]																	0	0	0	0	
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPON	sAON	X	X	X	X	X	0	0	0	1	
PM16	PRINCIPAL MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0	
X	X	X	X	X	X	PR10	PRINCIPAL REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1	
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0	
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR0	0	1	1	1	
X	X	X	X	X	X	X	X	X	0	DA6	7-BIT DAC					DA0	1	0	0	0	

Notes

1. FT = first; LT = last; sPON = software power-up for principal synthesizer (1 = ON); sAON = software power-up for auxiliary synthesizer (1 = ON).
2. The test register should not be programmed with any other value except all zeros for normal operation.

Table 3 Out-of-lock select

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principal phase error
1	1	both auxiliary and principal

Table 4 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	$I_{CPPF} : I_{CPP}$
0	0	$4 \times I_{SET}$	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$4 \times I_{SET}$	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$4 \times I_{SET}$	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps and DAC.

Table 5 Power-down modes

AON	PON	FAST	PRINCIPAL DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF	DAC AND BIAS
0	0	X	OFF	OFF	OFF	OFF	OFF	OFF
0	1	0	ON	OFF	OFF	ON	OFF	ON
0	1	1	ON	OFF	OFF	ON	ON	ON
1	0	X	OFF	ON	ON	OFF	OFF	ON
1	1	0	ON	ON	ON	ON	OFF	ON
1	1	1	ON	ON	ON	ON	ON	ON

Digital-to-analog converter

The 7-bits loaded via the bus into the appropriate latch drive a digital-to-analog converter. The internal current is scaled by the external resistance (R_{ext}) at pin I_{SET}, similar to the charge pumps. The nominal full-scale current is $2 \times I_{SET}$. The output current is mirrored to produce a full-scale voltage into a user-defined ground referenced resistance, thereby allowing optimum swing from power supply rails within the 2.7 to 5.5 V limits. The band gap reference voltage at pin I_{SET} is temperature and supply independent. The DAC signal is monotonic across the full range of digital input codes to enable fine adjustment of other system blocks. The typical settling time for full-scale switching is 400 ns into a 12 kΩ // 20 pF load. DAC functionality is neither tested nor guaranteed on UMA1018M versions with the /S1 suffix.

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

It should be noted that in Table 5, PON and AON can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 1.

When either synthesizer is reactivated after power-down the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	$V_{DD} = 5.5$ V	–	6.5	8.5	mA
	auxiliary synthesizer digital supply current	$V_{DD} = 5.5$ V	–	2.7	4.0	mA
I_{CC}	charge pumps and analog supply current	$V_{CC} = 5.5$ V; $R_{ext} = 12$ kΩ	–	1.2	2.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 V or V_{DD}	–	12	50	μA
RF principal main divider input; pin 6						
f_{VCO}	RF input frequency	$2.7 \text{ V} < V_{DD} < 3.5$ V	50	–	1250	MHz
		$2.7 \text{ V} < V_{DD} < 5.5$ V	50	–	1100	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω; $2.7 \text{ V} < V_{DD} < 3.5$ V; $0.5 < f_{VCO} < 1.25$ GHz; $T_{amb} = -20$ to +85°C	50	–	225	mV
		$R_s = 50$ Ω; $2.7 \text{ V} < V_{DD} < 5.5$ V; $0.5 < f_{VCO} < 1.1$ GHz; $T_{amb} = -30$ to +85°C	100	–	300	mV
		$R_s = 50$ Ω; $2.7 \text{ V} < V_{DD} < 5.5$ V; $50 < f_{VCO} < 500$ MHz; $T_{amb} = -30$ to +85°C	150	–	300	mV
Z_I	input impedance (real part)	$f_{VCO} = 1$ GHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131071	
f_{PPCmax}	maximum principal phase comparator frequency		–	2000	–	kHz
f_{PPCmin}	minimum principal phase comparator frequency		–	10	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Auxiliary main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 2.7 V < V_{DD} < 4.5 V; T_{amb} = –30 to +85°C	50	–	500	mV
		R_s = 50 Ω; 2.7 V < V_{DD} < 5.5 V; T_{amb} = –20 to +85°C	100	–	500	mV
Z_I	input impedance (real part)	f_{AI} = 100 MHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	
f_{APCmax}	maximum auxiliary phase comparator frequency		–	2000	–	kHz
f_{APCmin}	minimum auxiliary phase comparator frequency		–	10	–	kHz
Crystal reference divider input; pin 8						
f_{XTAL}	crystal reference input frequency		5	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	4.0 V < V_{DD} < 5.5 V	50	–	500	mV
		2.7 V < V_{DD} < 5.5 V	50	–	250	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	6	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference divider ratio		8	–	2047	
R_{ar}	auxiliary reference divider ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 17, 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	V_{cp} = ½V_{CC}	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	V_{CC} – 0.4	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3V_{DD}	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	2	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DAC output signal levels; pin 10; R_{ext} = 12 to 24 kΩ						
I_{DAC}	DAC full scale output current		$1.5 \times I_{SET}$	$2 \times I_{SET}$	$2.5 \times I_{SET}$	mA
V_{10}	output voltage compliance	all codes	0	–	$V_{DD} - 0.4$	V
I_{10min}	minimum DAC current	00 code	–	2	5	μA
I_{monot}	worst case monotonicity test: $\Delta I \times \frac{128}{2 \times I_{SET}}$	note 1	0.1	–	1.9	
Lock detect output signal; pin 20; open-drain output						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

Note

1. ΔI is the change in DAC output current when making the code transitions: 3FH/40H or 1FH/20H.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC}$ = 3 V; T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	−20	–	–	ns
t_W	minimum inactive pulse width	4000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 4 μs provided all the following conditions are satisfied:

   a) Principal main divider input frequency $f_{VCO} > \frac{256}{t_W}$

   b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$

   c) Reference divider input frequency $f_{XTAL} > \frac{3}{t_W}$

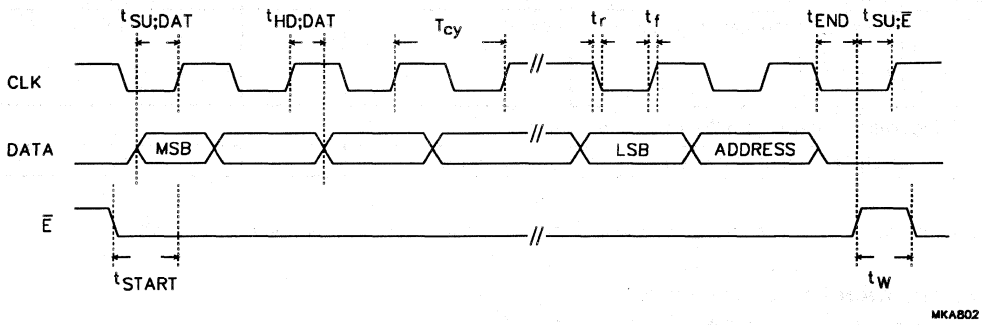


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

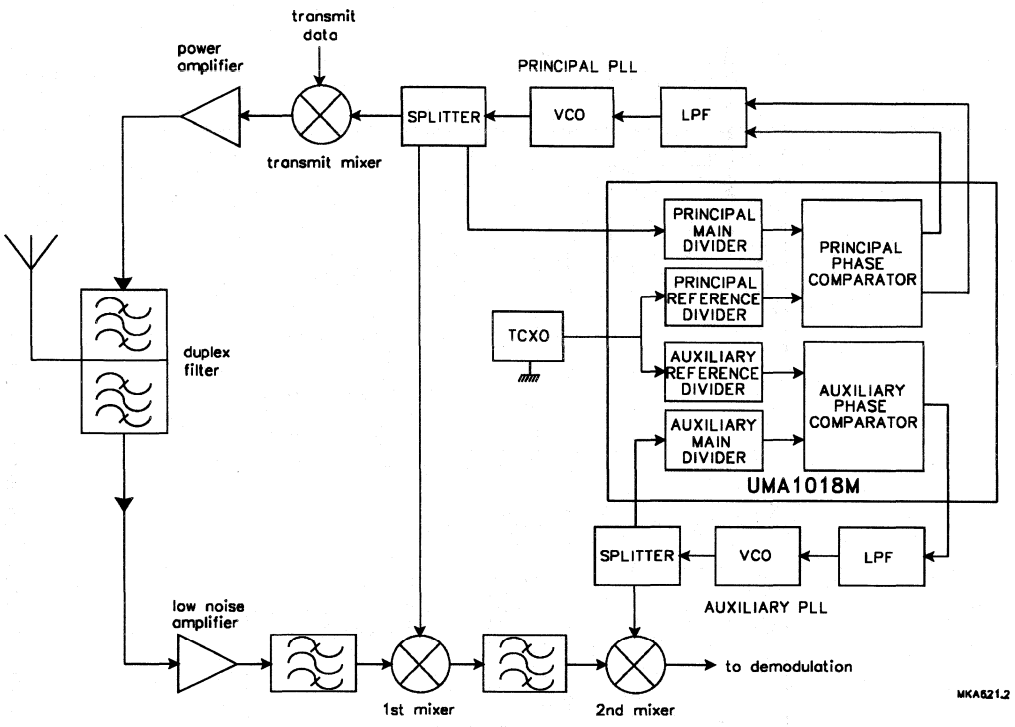


Fig.4 Typical application block diagram.

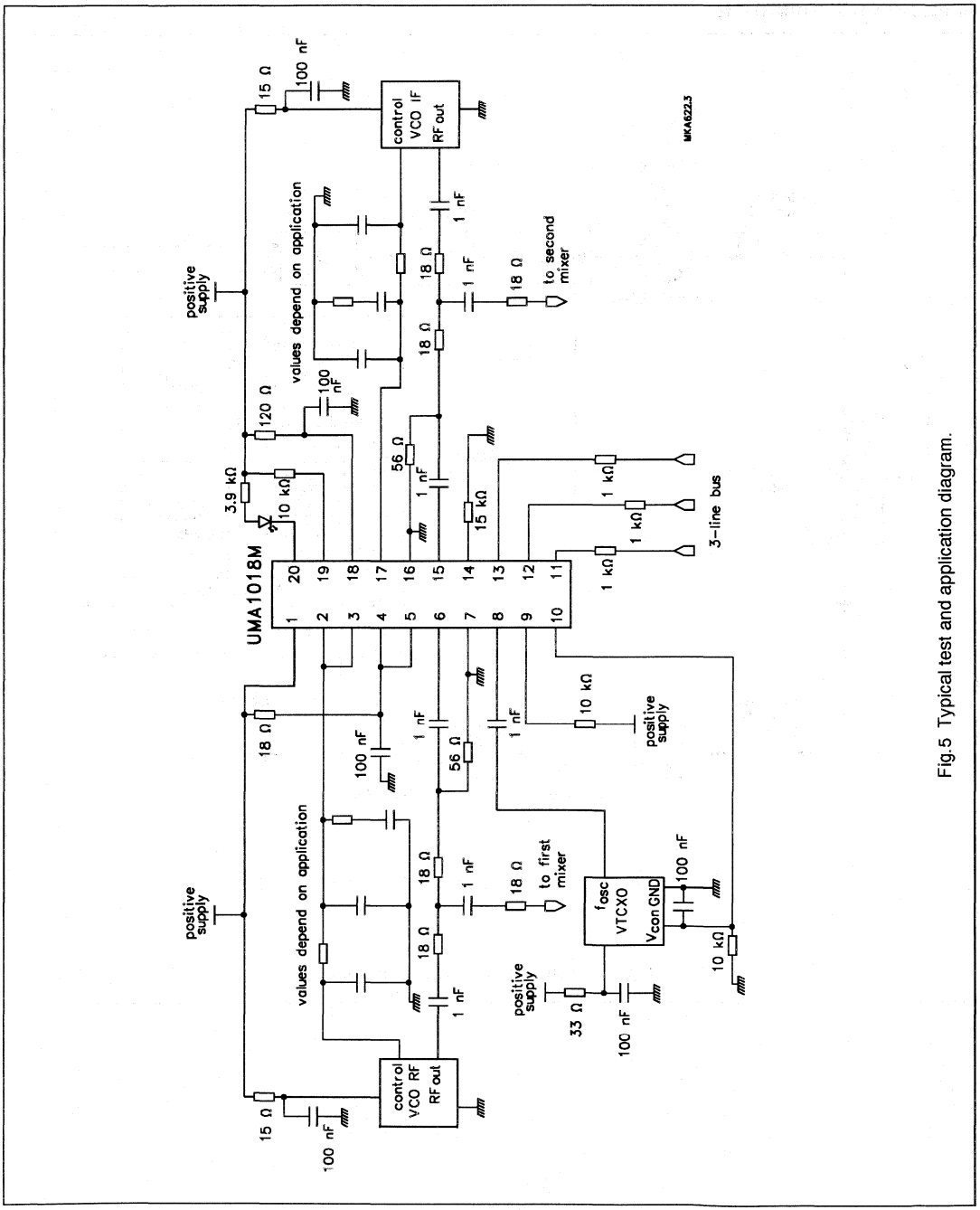


Fig.5 Typical test and application diagram.

Low-voltage frequency synthesizer for radio telephones

UMA1019AM

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 1 to 1.7 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1019AM BICMOS device integrates prescalers, a programmable divider, and phase comparator to implement a phase-locked loop.

The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The synthesizer operates at RF input frequencies up to 1.7 GHz. The synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. Digital supplies V_{DD1}, V_{DD2} and V_{DD3} must also be at the same potential. V_{CC} must be equal to or greater than V_{DD} (i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range).

The phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	supply current		–	9.4	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	µA
f_{VCO}	RF input frequency		1000	1500	1700	MHz
f_{xtal}	crystal reference input frequency		3	–	40	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1019AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

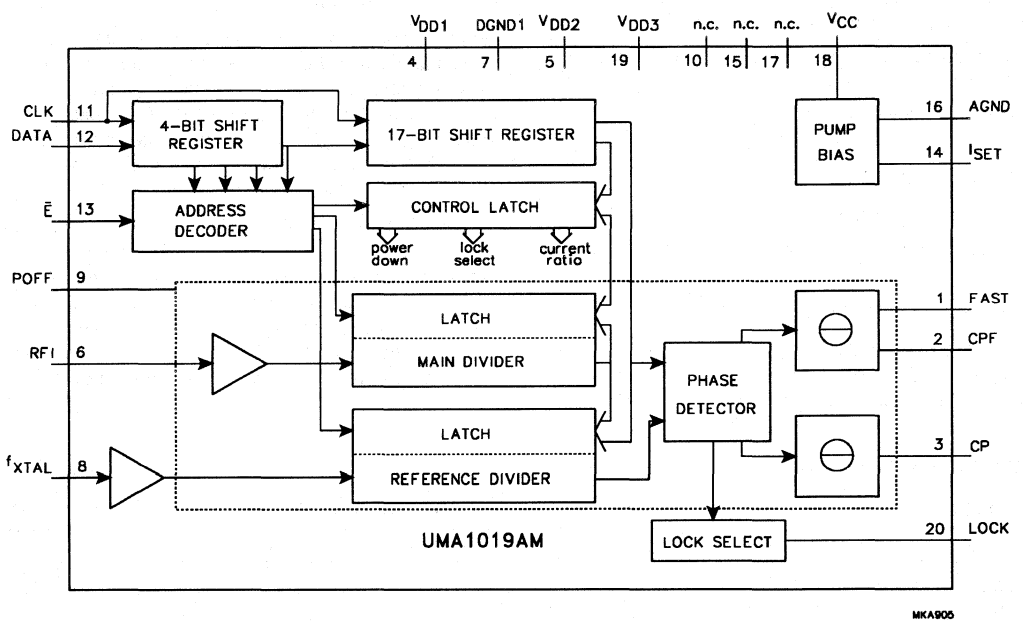


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPF	2	speed-up charge-pump output
CP	3	normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
RFI	6	1.7 GHz RF main divider input
DGND1	7	digital ground 1
f_{XTAL}	8	crystal frequency input from TCXO
POFF	9	power-down input
n.c.	10	not connected
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
n.c.	15	not connected
AGND	16	analog ground
n.c.	17	not connected
V_{CC}	18	supply for charge-pump
V_{DD3}	19	digital power supply 3
LOCK	20	in-lock detect output; test mode output

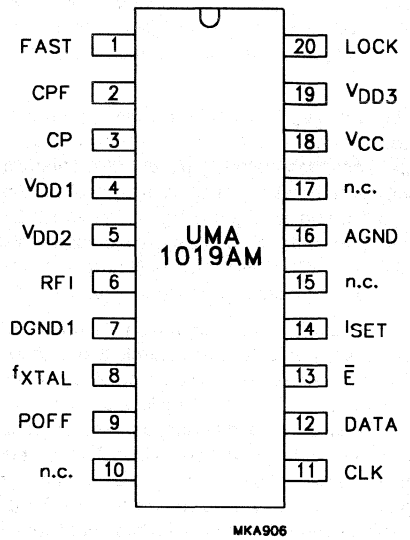


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

Programmable reference and main dividers drive the phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The RFI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 100 mV up to 500 mV (RMS), and at frequencies as high as 1.7 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divider ratios (512 to 131 071) allow up to 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to reduce noise and breakthrough levels.

The synthesizer speed-up charge pump (CPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector improving linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μA. The output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated. The out-of-lock function can be disabled via the serial bus.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

However when the synthesizer is powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1019AM uses 4 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To ensure that data is correctly loaded at first power-up, $\overline{E}$ should be held LOW and only taken HIGH after an appropriate register has been programmed. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Power-down mode

The power-down signal can be either hardware (POFF) or software (sPOFF). The dividers are on when both POFF and sPOFF are at logic 0.

When the synthesizer is reactivated after power-down the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

Table 1 Format of programmed data

LAST IN			PROGRAMMING REGISTER BIT USAGE					FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT							REGISTER ALLOCATION													LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS[2]																	0	0	0	0
X	X	X	X	OOL	X	CR1	CR0	X	X	sPOFF	X	X	X	X	X	X	0	0	0	1
PM16	MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1

Notes

1. FT = first, LT = last; sPOFF = software power-down for synthesizer (1 = OFF); OOL = out-of-lock (1 = enabled).
2. The test register should not be programmed with any other values except all zeros for normal operation.

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; bias current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
$\Delta V_{CC}-V_{DD}$	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8, 9, 11 to 14 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3}$	voltage at pins 2 and 3	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	−	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	−	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

$V_{DD1} = V_{DD2} = V_{DD3}$ = 2.7 to 5.5 V; V_{CC} = 2.7 to 5.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2} = V_{DD3}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	V_{DD} = 5.5 V	–	9	11	mA
I_{CC}	charge pumps analog supply current	V_{CC} = 5.5 V; R_{ext} =12 kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF main divider input; pin 6						
f_{VCO}	RF input frequency		1000	1500	1700	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω	100	–	500	mV
Z_I	input impedance (real part)	f_{VCO} = 1.7 GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_m	main divider ratio		512	–	131071	
f_{PCmax}	maximum phase comparator frequency		–	2000	–	kHz
f_{PCmin}	minimum phase comparator frequency		–	10	–	kHz
Crystal reference divider input; pin 8						
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_r	reference divider ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	V_{cp} = ½V_{CC}	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	V_{CC} – 0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	−5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	2	–	pF
Lock detect output signal; pin 20 (open-drain output)						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	−20	–	–	ns
t_W	minimum inactive pulse width	4000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 4 μs provided all the following conditions are satisfied:

   a) Main divider input frequency $f_{VCO} > \frac{512}{t_W}$

   b) Reference divider input frequency $f_{XTAL} > \frac{3}{t_W}$

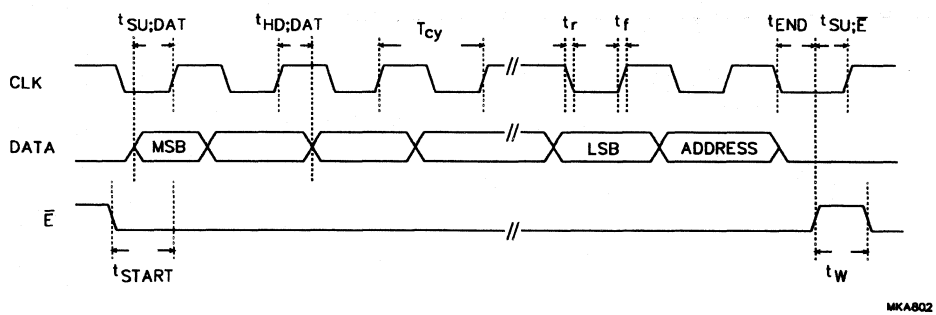


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

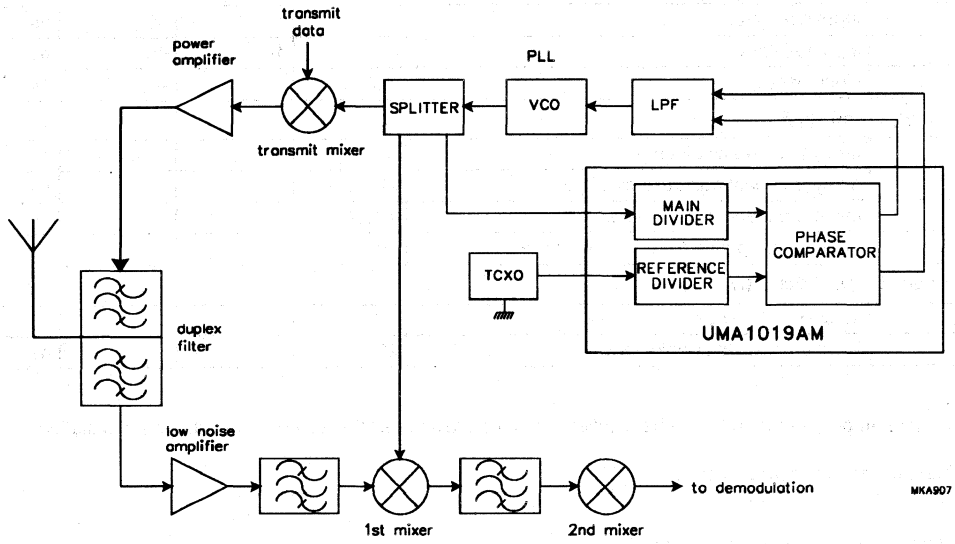


Fig.4 Typical application block diagram.

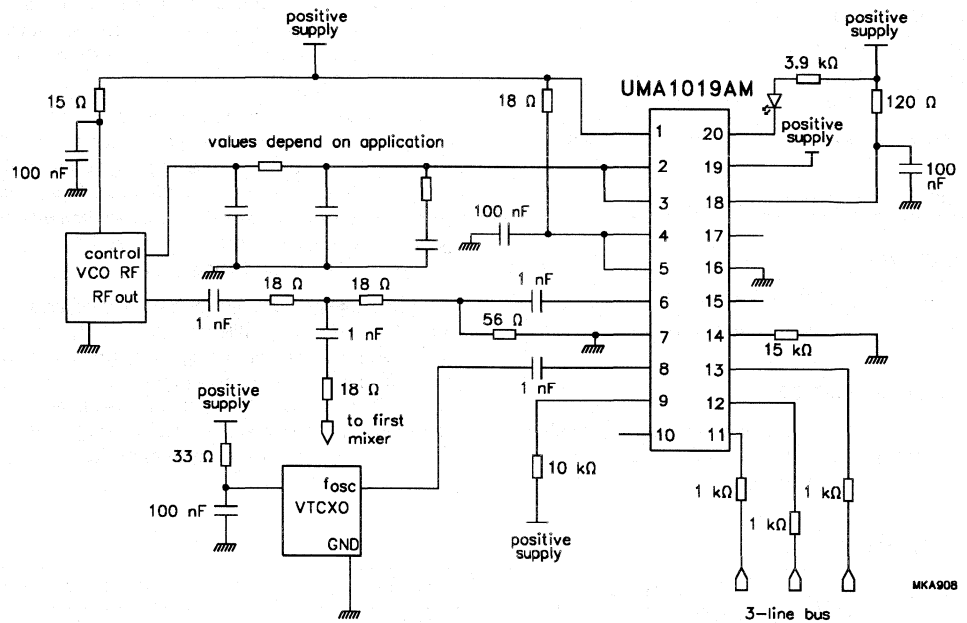


Fig.5 Typical test and application diagram.

Low-voltage frequency synthesizer for radio telephones

UMA1019M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1019M BICMOS device integrates prescalers, a programmable divider, and phase comparator to implement a phase-locked loop.

The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The synthesizer operates at RF input frequencies up to 2.4 GHz. The synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. Digital supplies V_{DD1}, V_{DD2} and V_{DD3} must also be at the same potential. V_{CC} must be equal to or greater than V_{DD} (i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range).

The phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	supply current		–	9.4	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	µA
f_{VCO}	RF input frequency		1700	1900	2400	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1019M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

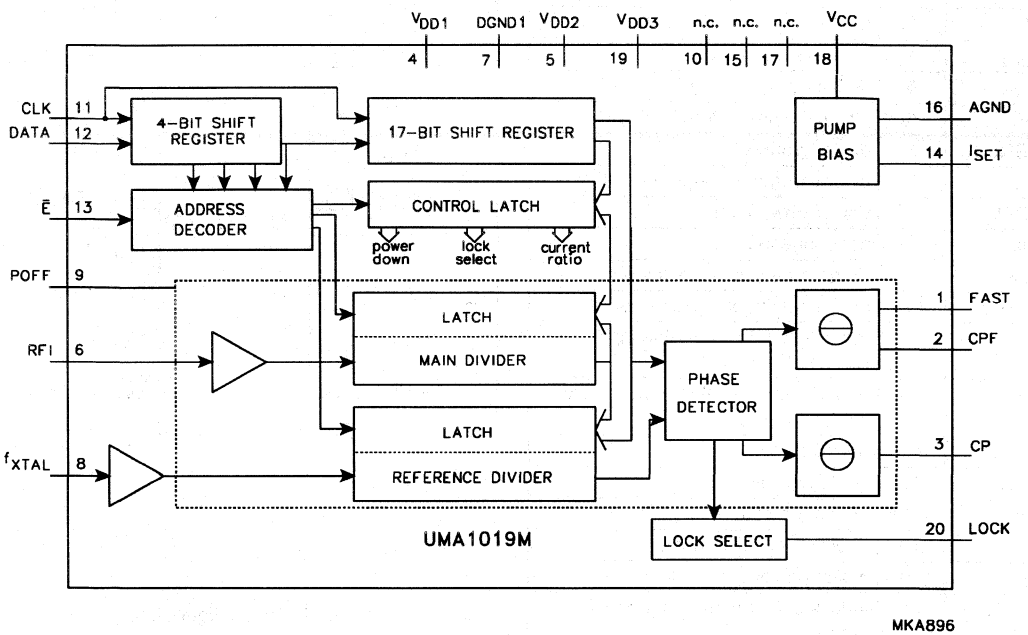


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPF	2	speed-up charge-pump output
CP	3	normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
RFI	6	2 GHz RF main divider input
DGND1	7	digital ground 1
f_{XTAL}	8	crystal frequency input from TCXO
POFF	9	power-down input
n.c.	10	not connected
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
n.c.	15	not connected
AGND	16	analog ground
n.c.	17	not connected
V_{CC}	18	supply for charge-pump
V_{DD3}	19	digital power supply 3
LOCK	20	in-lock detect output; test mode output

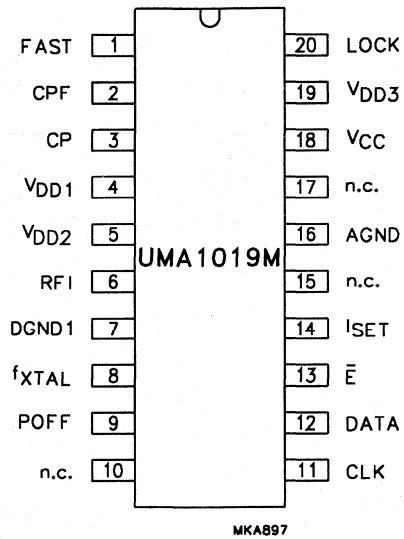


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

Programmable reference and main dividers drive the phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The RFI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 60 mV up to 180 mV (RMS), and at frequencies as high as 2.4 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to reduce noise and breakthrough levels.

The synthesizer speed-up charge pump (CPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector thereby improving linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μA. The output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated. The out-of-lock function can be disabled via the serial programming bus.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

However when the synthesizer is powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1019M uses 4 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To ensure that data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.
The corresponding relationship between data fields and addresses is given in Table 2.

Power-down mode

The power-down signal can be either hardware (POFF) or software (sPOFF). The dividers are on when both POFF and sPOFF are at logic 0.

When the synthesizer is reactivated after power-down the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

Table 1 Format of programmed data

LAST IN	PROGRAMMING REGISTER BIT USAGE							FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	REGISTER BIT ALLOCATION																			LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS(2)																	0	0	0	0
X	X	X	X	OOL	X	CR1	CR0	X	X	sPOFF	X	X	X	X	X	X	0	0	0	1
PM16	MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1

Notes

1. FT = first; LT = last; sPOFF = software power-down for synthesizer (1 = OFF); OOL = out-of-lock (1 = enabled).
2. The test register should not be programmed with any other value except all zeros for normal operation.

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; bias current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
$\Delta V_{CC}-V_{DD}$	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8, 9, 11 to 14 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3}$	voltage at pins 2 and 3	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	−	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	−	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

$V_{DD1} = V_{DD2} = V_{DD3}$ = 2.7 to 5.5 V; V_{CC} = 2.7 to 5.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2} = V_{DD3}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	V_{DD} = 5.5 V	–	9	12.5	mA
I_{CC}	charge pumps analog supply current	V_{CC} = 5.5 V; R_{ext} =12 kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF main divider input; pin 6						
f_{VCO}	RF input frequency		1700	1900	2400	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 1.7 GHz < f_{VCO} < 2 GHz	60	–	400	mV
		R_s = 50 Ω; 2 GHz < f_{VCO} < 2.4 GHz	60	–	180	mV
Z_I	input impedance (real part)	f_{VCO} = 2 GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_m	main divider ratio		512	–	131071	
f_{PCmax}	maximum phase comparator frequency		–	2000	–	kHz
f_{PCmin}	minimum phase comparator frequency		–	10	–	kHz
Crystal reference divider input; pin 8						
f_{XTAL}	crystal reference input frequency		5	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	$V_{6(rms)}$ < 224 mV	50	–	500	mV
		$V_{6(rms)}$ > 224 mV	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_r	reference divider ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	V_{cp} = ½V_{CC}	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	V_{CC} – 0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	−5	–	+5	μA
C_i	input capacitance	indicative, not tested	–	2	–	pF
Lock detect output signal; pin 20 (open-drain output)						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	4000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 4 μs provided all the following conditions are satisfied:

   a) Main divider input frequency $f_{VCO} > \frac{512}{t_W}$

   b) Reference divider input frequency $f_{XTAL} > \frac{3}{t_W}$

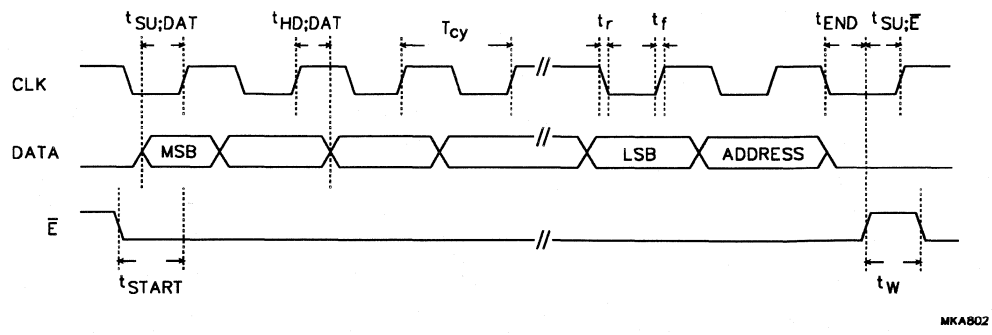


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

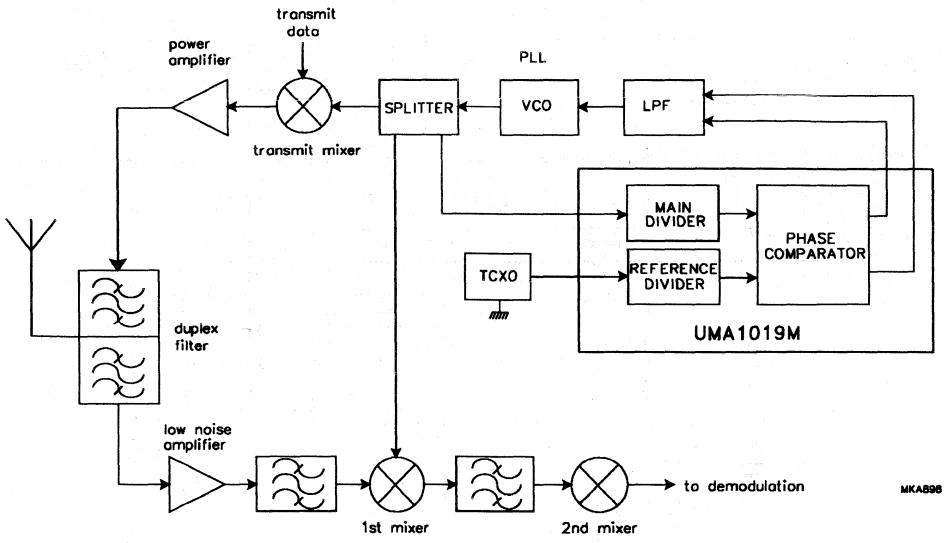


Fig.4 Typical application block diagram.

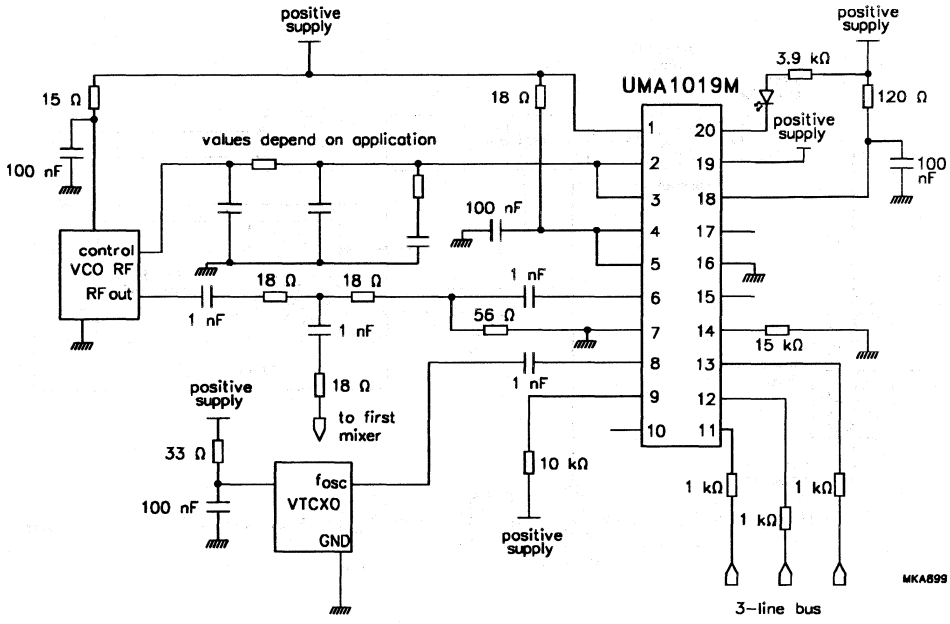


Fig.5 Typical test and application diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020AM

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 1 to 1.7 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1020AM BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at RF input frequencies up to 1.7 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. Digital supplies V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} must be equal to or greater than V_{DD} (i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range).

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	principal synthesizer supply current	auxiliary synthesizer in power-down mode	–	9.4	–	mA
	principal and auxiliary synthesizer supply current	principal and auxiliary synthesizers ON	–	12.1	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	μA
f_{VCO}	principal input frequency		1000	1500	1700	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principal phase comparator frequency		–	200	–	kHz
f_{APC}	auxiliary phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1020AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

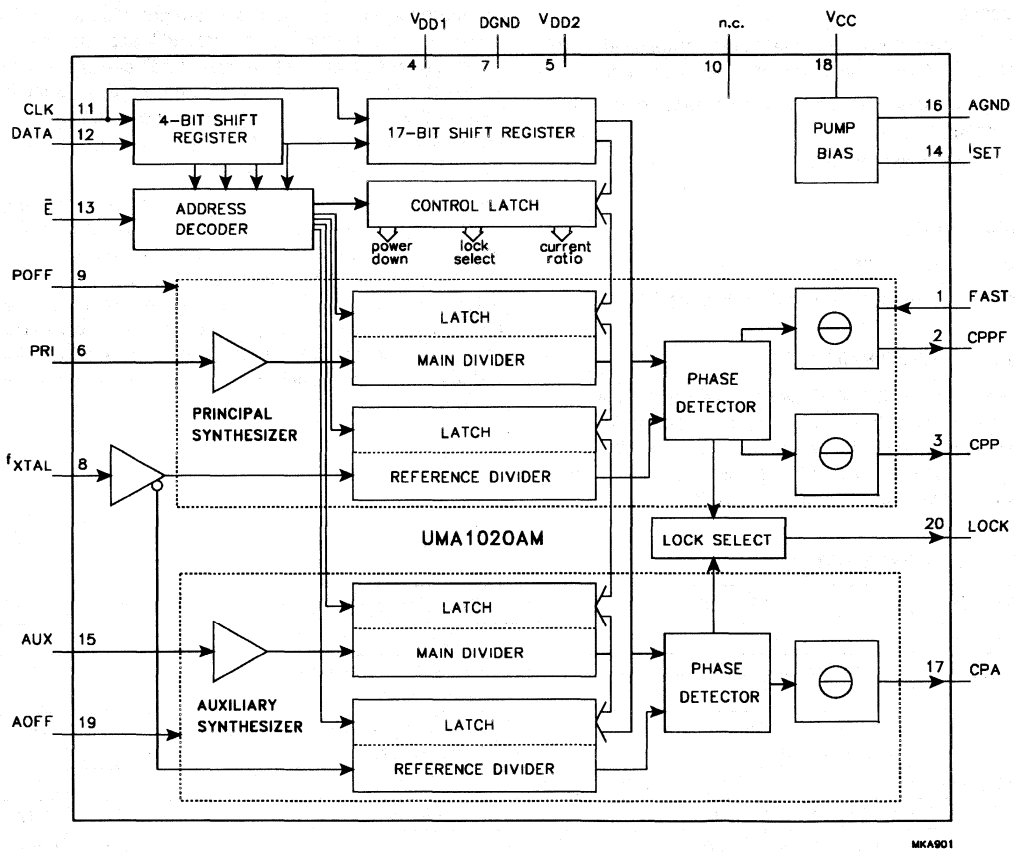


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principal synthesizer speed-up charge-pump output
CPP	3	principal synthesizer normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
PRI	6	1.7 GHz principal synthesizer frequency input
DGND	7	digital ground
f_{XTAL}	8	common crystal frequency input from TCXO
POFF	9	principal synthesizer power-down input
n.c.	10	not connected
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump
AOFF	19	auxiliary synthesizer power-down input
LOCK	20	in-lock detect output (main PLL); test mode output

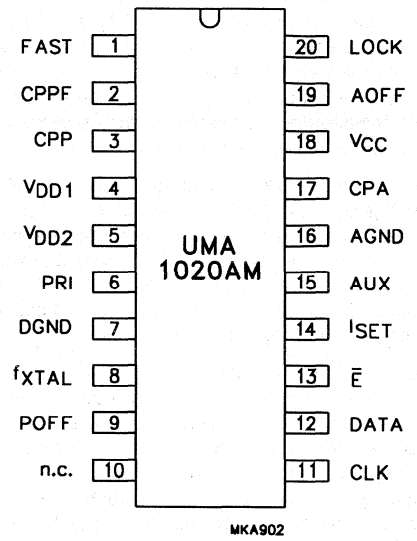


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a preamplifier to provide the clock to the first divider stage. The preamplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 100 mV to 500 mV (RMS), and at frequencies up to 1.7 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divider ratios (512 to 131071) allow up to 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to reduce noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector thereby improving linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 μA. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison, an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AOFF (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the principal reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1020AM uses 5 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To ensure that the data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers.

This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data

LAST IN	PROGRAMMING REGISTER BIT USAGE						FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	REGISTER BIT ALLOCATION																			LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS(2)																	0	0	0	0
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPOFF	sAOFF	X	X	X	X	X	0	0	0	1
PM16	PRINCIPAL MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	PRINCIPAL REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR0	0	1	1	1

Notes

1. FT = first, LT = last; sPOFF = software power-down for principal synthesizer (1 = OFF); sAOFF = software power-down for auxiliary synthesizer (1 = OFF).
2. The test register should not be programmed with any other value except all zeros for normal operation.

Table 3 Out-of-lock select

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principal phase error
1	1	both auxiliary and principal

Table 4 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	$I_{CPPF} : I_{CPP}$
0	0	$4 \times I_{SET}$	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$4 \times I_{SET}$	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$4 \times I_{SET}$	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps.

Table 5 Power-down modes

AOFF	POFF	FAST	PRINCIPAL DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF
1	1	X	OFF	OFF	OFF	OFF	OFF
1	0	0	ON	OFF	OFF	ON	OFF
1	0	1	ON	OFF	OFF	ON	ON
0	1	X	OFF	ON	ON	OFF	OFF
0	0	0	ON	ON	ON	ON	OFF
0	0	1	ON	ON	ON	ON	ON

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

Note that in Table 5, POFF and AOFF can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 0.

When either synthesizer is reactivated after power-down the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	−	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	−	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	$V_{DD} = 5.5$ V	–	9	11	mA
	auxiliary synthesizer digital supply current	$V_{DD} = 5.5$ V	–	2.7	4.0	mA
I_{CC}	charge pumps supply current	$V_{CC} = 5.5$ V; $R_{ext} = 12$ kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF principal main divider input; pin 6						
f_{VCO}	RF input frequency		1000	1500	1700	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω	100	–	500	mV
Z_I	input impedance (real part)	$f_{VCO} = 1.7$ GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131071	
f_{PPCmax}	maximum principal phase comparator frequency		–	2000	–	kHz
f_{PPCmin}	minimum principal phase comparator frequency		–	10	–	kHz
Auxiliary main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω; 2.7 V < V_{DD} < 3.5 V	50	–	500	mV
		$R_s = 50$ Ω; 3.5 V < V_{DD} < 5.5 V	100	–	500	mV
Z_I	input impedance (real part)	$f_{AI} = 100$ MHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	
f_{APCmax}	maximum auxiliary loop comparison frequency		–	2000	–	kHz
f_{APCmin}	minimum auxiliary loop comparison frequency		–	10	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal reference dividers input; pin 8						
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference divider ratio		8	–	2047	
R_{ar}	auxiliary reference divider ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 17, 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	V_{cp} = ½V_{CC}	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	V_{CC} – 0.4	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3V_{DD}	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	2	–	pF
Lock detect output signal; pin 20 open-drain output						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	4000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 4 μs provided all the following conditions are satisfied:

   a) Principal main divider input frequency $f_{VCO} > \frac{512}{t_W}$

   b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$

   c) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$

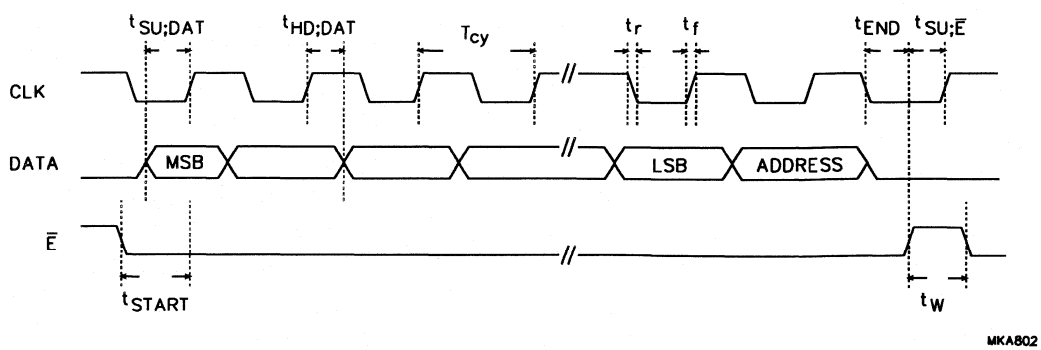


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

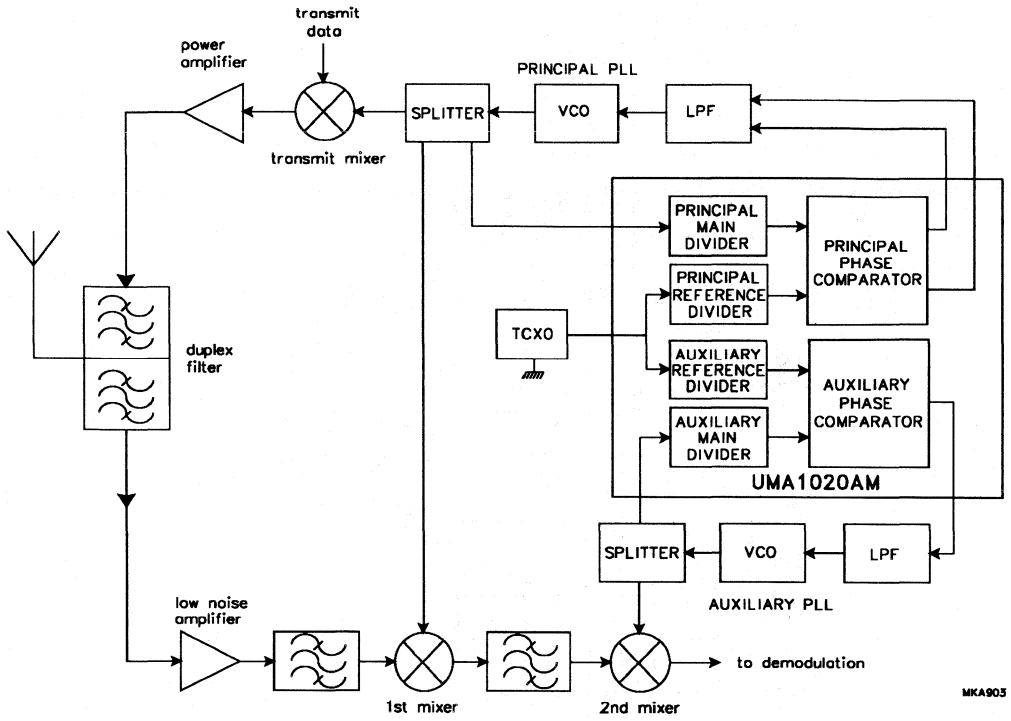


Fig.4 Typical application block diagram.

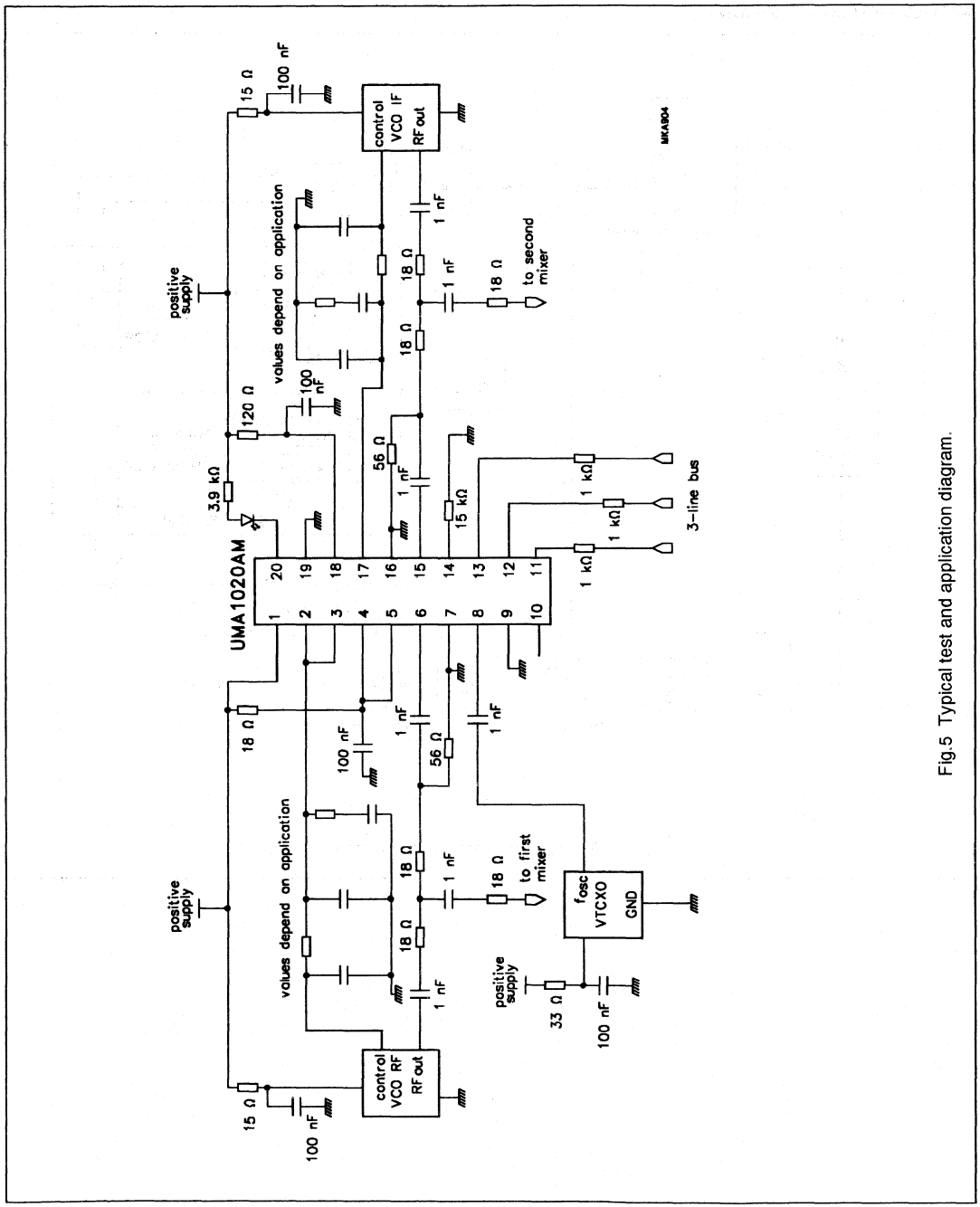


Fig.5 Typical test and application diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Integrated digital-to-analog converter
- Dual power-down modes.

APPLICATIONS

- 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1020M BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at RF input frequencies up to 2.4 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. Digital supplies V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} must be equal to or greater than V_{DD} (i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range).

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance. An on-chip 7-bit DAC enables adjustment of an external function, such as the temperature compensation of a crystal oscillator.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	principal synthesizer supply current	auxiliary synthesizer in power-down mode	–	9.4	–	mA
	principal and auxiliary synthesizer supply current	principal and auxiliary synthesizers ON	–	12.1	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	µA
f_{VCO}	principal input frequency		1700	–	2400	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principal phase comparator frequency		–	200	–	kHz
f_{APC}	auxiliary phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

Low-voltage dual frequency synthesizer for radio telephones

UMA1020M

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1020M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

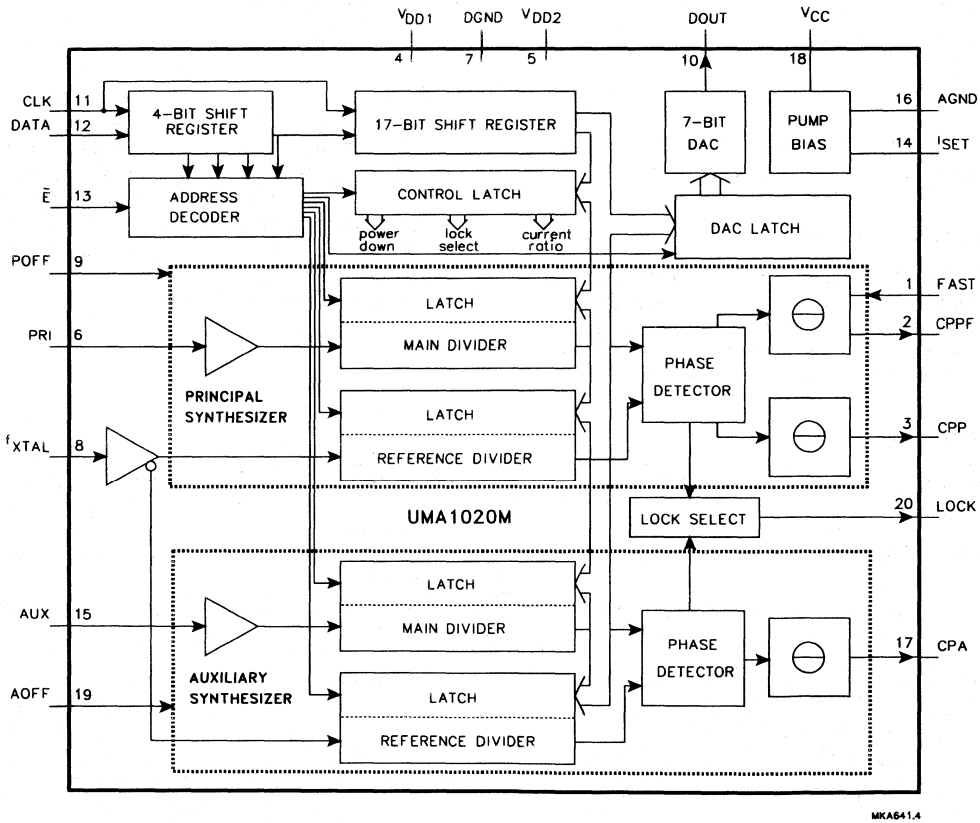


Fig.1 Block diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020M

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principal synthesizer speed-up charge-pump output
CPP	3	principal synthesizer normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
PRI	6	2 GHz principal synthesizer frequency input
DGND	7	digital ground
f_{XTAL}	8	crystal frequency input from TCXO
POFF	9	principal synthesizer power-down input
DOUT	10	7-bit digital-to-analog output
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump and DAC circuits
AOFF	19	auxiliary synthesizer power-down input
LOCK	20	in-lock detect output (main PLL); test mode output

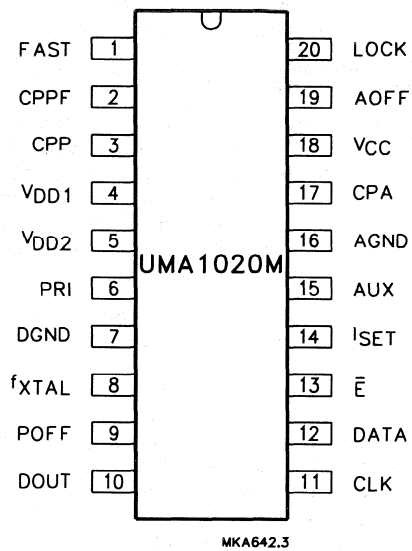


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a preamplifier to provide the clock to the first divider stage. The preamplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 60 mV to 180 mV (RMS), and at frequencies up to 2.4 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131071) allow a 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to reduce noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector thereby improving linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 μA. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison, an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AOFF (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the principal reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1020M uses 6 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To ensure that the data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data

LAST IN			PROGRAMMING REGISTER BIT USAGE					FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT					REGISTER BIT ALLOCATION												LT			
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS[2]																	0	0	0	0
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPOFF	sAOFF	X	X	X	X	X	0	0	0	1
PM16	PRINCIPAL MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	PRINCIPAL REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR0	0	1	1	1
X	X	X	X	X	X	X	X	X	0	DA6	7-BIT DAC					DA0	1	0	0	0

Notes

1. FT = first; LT = last; sPOFF = software power-down for principal synthesizer (1 = OFF); sAOFF = software power-down for auxiliary synthesizer (1 = OFF).
2. The test register should not be programmed with any other value except all zeros for normal operation.

Table 3 Out-of-lock select

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principal phase error
1	1	both auxiliary and principal

Table 4 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	I_{CPPF}: I_{CPP}
0	0	$4 \times I_{SET}$	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$4 \times I_{SET}$	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$4 \times I_{SET}$	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps and DAC.

Table 5 Power-down modes

AOFF	POFF	FAST	PRINCIPAL DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF	DAC AND BIAS
1	1	X	OFF	OFF	OFF	OFF	OFF	OFF
1	0	0	ON	OFF	OFF	ON	OFF	ON
1	0	1	ON	OFF	OFF	ON	ON	ON
0	1	X	OFF	ON	ON	OFF	OFF	ON
0	0	0	ON	ON	ON	ON	OFF	ON
0	0	1	ON	ON	ON	ON	ON	ON

Digital-to-analog converter

The 7-bits loaded via the bus into the appropriate latch drive a digital-to-analog converter. The internal current is scaled by the external resistance (R_{ext}) at pin I_{SET}, similar to the charge pumps. The nominal full-scale current is $2 \times I_{SET}$. The output current is mirrored to produce a full-scale voltage into a user-defined ground referenced resistance, thereby allowing optimum swing from power supply rails within the 2.7 to 5.5 V limits. The bandgap reference voltage at pin I_{SET} is temperature and supply independent. The DAC signal is monotonic across the full range of digital input codes to enable fine adjustment of other system blocks. The typical settling time for full-scale switching is 400 ns into a 12 kΩ // 20 pF load.

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

Note that in Table 5, POFF and AOFF can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 0.

When either synthesizer is reactivated after power-down, the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	$V_{DD} = 5.5$ V	–	9	12.5	mA
	auxiliary synthesizer digital supply current	$V_{DD} = 5.5$ V	–	2.7	4.0	mA
I_{CC}	charge pumps supply current	$V_{CC} = 5.5$ V; $R_{ext} = 12$ kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	µA
RF principal main divider input; pin 6						
f_{VCO}	RF input frequency		1700	–	2400	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω; 1.7 GHz < f_{VCO} < 2.0 GHz	60	–	400	mV
		$R_s = 50$ Ω; 2.0 GHz < f_{VCO} < 2.4 GHz	60	–	180	mV
Z_I	input impedance (real part)	$f_{VCO} = 2$ GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131071	
f_{PPCmax}	maximum principal phase comparator frequency		–	2000	–	kHz
f_{PPCmin}	minimum principal phase comparator frequency		–	10	–	kHz
Auxiliary main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω; 2.7 V < V_{DD} < 3.5 V	50	–	500	mV
		$R_s = 50$ Ω; 3.5 V < V_{DD} < 5.5 V	100	–	500	mV
Z_I	input impedance (real part)	$f_{AI} = 100$ MHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	
f_{APCmax}	maximum auxiliary phase comparator frequency		–	2000	–	kHz
f_{APCmin}	minimum auxiliary phase comparator frequency		–	10	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal reference dividers input; pin 8						
f_{XTAL}	input frequency range from crystal		5	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	$V_{6(rms)} < 224$ mV	50	–	500	mV
		$V_{6(rms)} > 224$ mV	100	–	500	mV
Z_I	input impedance (real part)	$f_{XTAL} = 30$ MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference division ratio		8	–	2047	
R_{ar}	auxiliary reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	$R_{ext} = 12$ kΩ	–	1.15	–	V
Charge pump outputs; pins 17, 3 and 2; $R_{ext} = 12$ kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	$V_{cp} = ½V_{CC}$	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	$V_{CC} - 0.4$	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	µA
C_I	input capacitance	indicative, not tested	–	2	–	pF
DAC output signal levels; pin 10, $R_{ext} = 12$ to 24 kΩ						
I_{DAC}	DAC full scale output current		$1.5 \times I_{SET}$	$2 \times I_{SET}$	$2.5 \times I_{SET}$	mA
V_{10}	output voltage compliance	all codes	0	–	$V_{DD} - 0.4$	V
I_{10min}	minimum DAC current	00 code	–	2	5	µA
I_{monot}	worst case monotonicity test: $\Delta I \times \frac{128}{2 \times I_{SET}}$	note 1	0.1	–	1.9	
Lock detect output signal; pin 20 open-drain output						
V_{OL}	LOW level output voltage	$I_{sink} = 0.4$ mA	–	–	0.4	V

Note

1. ΔI is the change in DAC output current when making the code transitions: 3FH/40H or 1FH/20H.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	4000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 4 µs provided all the following conditions are satisfied:

   a) Principal main divider input frequency $f_{VCO} > \frac{512}{t_W}$

   b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$

   c) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$

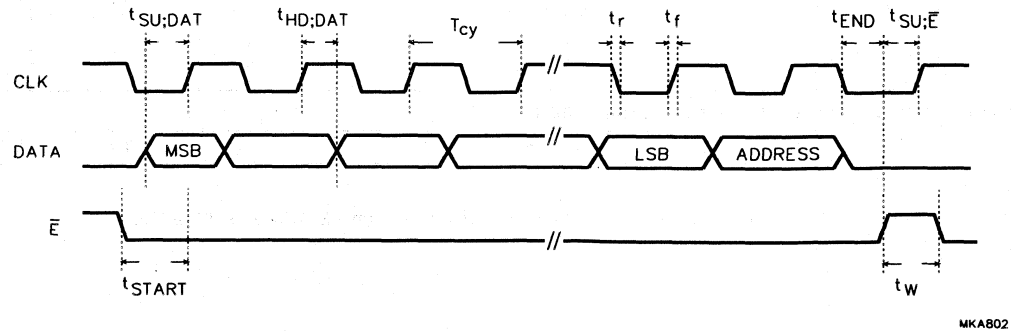


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

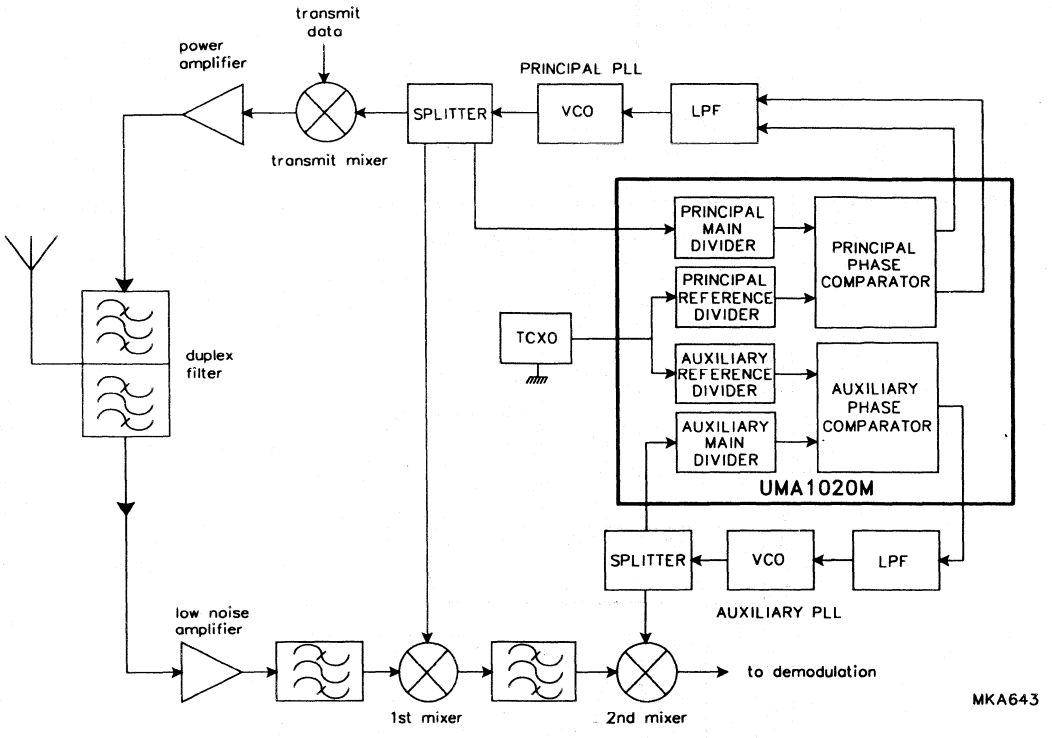


Fig.4 Typical application block diagram.

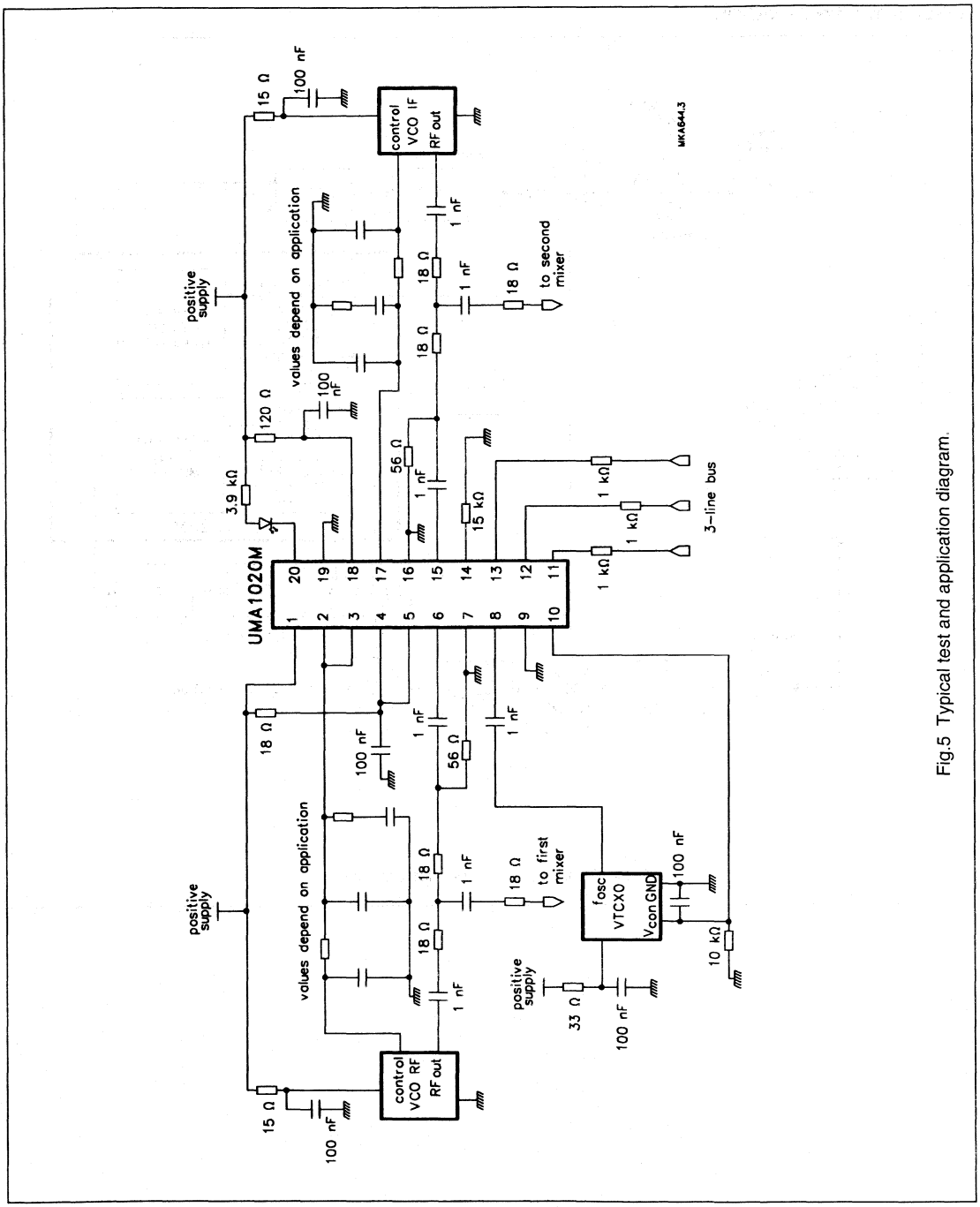


Fig.5 Typical test and application diagram.

Low power single/dual frequency synthesizers: UMA1017M/1018M/1019M(AM)/1020M(AM)

AN95102

Author: P. Hugues

UMA1018M and UMA1020M/UMA1020AM low power dual frequency synthesizers

UMA1017M and UMA1019M/UMA1019AM low power single frequency synthesizers

SUMMARY

This application note describes the UMA1018M and UMA1020M/UMA1020AM from Philips Semiconductors. They permit a low-voltage low-power single-chip solution to designing dual PLL frequency synthesizers. They are intended for use in digital or analogue wireless communications equipment. Typical applications include GSM, DECT and DCS1800.

Three low-voltage low-power solutions to single frequency synthesizers are also briefly described. The UMA1017M and UMA1019M/UMA1019AM are derivatives from UMA1018M and UMA1020M, respectively, and are hence closely related.

The overall performance of any PLL frequency synthesizer system is critically determined by the low pass filter used. Described in this report is a basic loop filter design method with worked examples and some measurement results.

1. INTRODUCTION TO UMA1018M DUAL SYNTHESIZER

1.1 General description

The UMA1018M [1] is a low power low voltage single chip solution to a dual frequency synthesizer used in radiocommunications. Designed in a BICMOS process, it operates from 2.7 (3 NiCd cells) to 5.5 V. The UMA1018M contains all the necessary elements with the exception of the VTCXO, VCO and loop filters to build two PLL frequency synthesizers.

It is intended that the principal synthesizer operates in the 50 to 1250 MHz range, and the auxiliary synthesizer will work between 20 and 300 MHz. For each synthesizer, fully programmable main and reference dividers are integrated on chip. The reference input FXTAL can operate from 5 to 40 MHz. Fast programming is possible via the three wire serial bus with clock speeds of up to 10 MHz.

The principal synthesizer phase detector drives a low current charge pump and a high current charge pump simultaneously. Maximum output current is 0.4 mA with the low current charge pump (pin CPP) and 3.2 mA with the other (pin CPPF). The auxiliary phase detector drives only one charge pump. The programmable charge pump currents are fixed by an external resistance R_{ext} at pin I_{SET}. Only passive loop filters are necessary.

To reduce crosstalk between different parts of the synthesizer, separate power supply and ground pins are provided to the analogue and digital sections.

Each synthesizer can be powered down independently to save current via software programming or hardwire pins AON / PON.

An on-chip 7 bit DAC allows adjustment of external functions, such as temperature compensation of the VTCXO, power amplifier control, etc.

1.2 FEATURES

- Dual frequency synthesizers
- Operating voltage range 2.7 to 5.5 V for battery powered operation
- Low current consumption, 10 mA typically at 5.5 V (two PLLs enabled)
- Integrated fully programmable main divider for each synthesizer
  - Principal: 512 to 131,071 up to 1.25 GHz input
  - Auxiliary: 64 to 16,383 up to 300 MHz input
- Independent fully programmable reference divider for each synthesizer
  - Principal: 8 to 2074 up to 2 MHz output
  - Auxiliary: 8 to 2047 up to 1 MHz output
- 3-wire serial bus (Data, Clock, Enable) for fast programming (f_{max} = 10 MHz)
- Independent hardwire and software power down modes for both synthesizers
- Simple passive loop filters
- Charge pump output current under bus control, with reference current I_{SET} set by an external reference resistor R_{ext}
- Programmable out-of-lock detector
- Integrated D-to-A converter
- Small SSOP-20 package

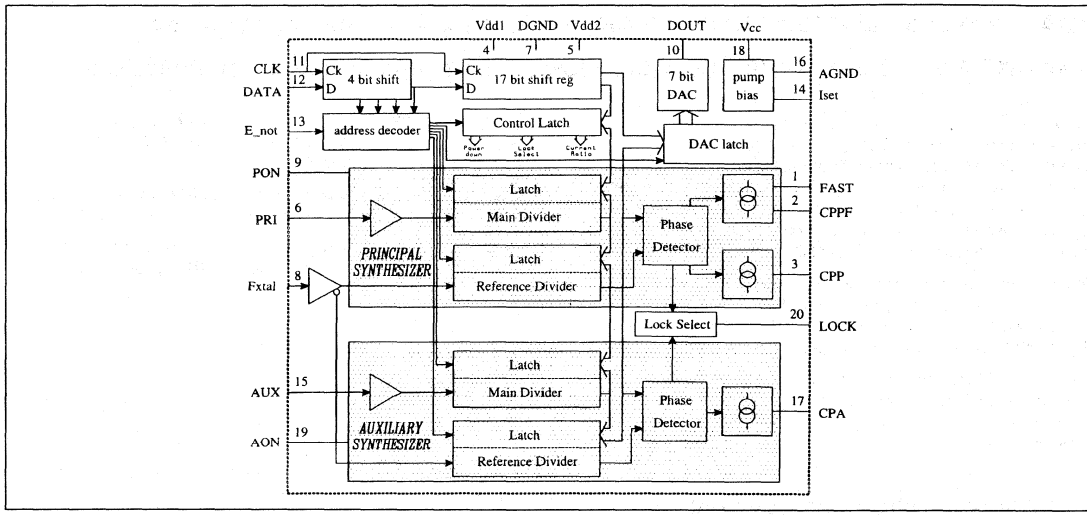


Figure 1–1. UMA1018M Block Diagram

1.3 Typical Application Architecture

UMA1018M integrated circuit is typically used in digital radiotelephone systems like GSM. It is designed to meet the requirements of these systems; low noise (residual and spurious), fast switching and low current consumption (at 5.5 V: 10 mA with both synthesizers ON and 36 µA with both synthesizers OFF).

Figure 1–1 demonstrates a typical application. UMA1018M is integrated on a dual superheterodyne architecture using two local oscillators.

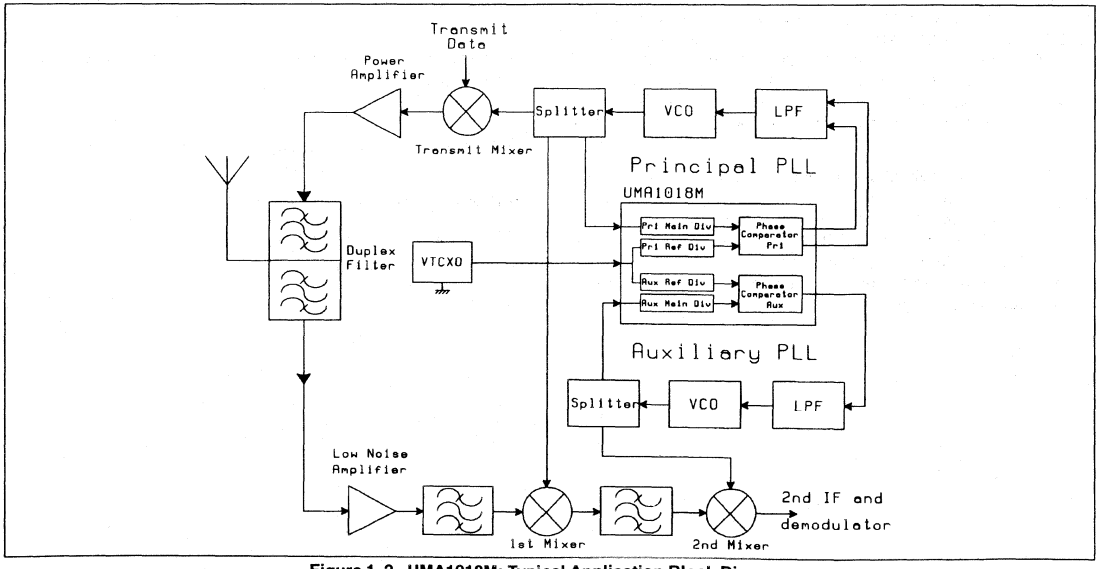


Figure 1–2. UMA1018M: Typical Application Block Diagram

1.4 UMA1018M Family

To satisfy the need of the emerging digital communication systems, a family of synthesizer controls based around the UMA1018M has been developed.

1.4.1 UMA1020M/UMA1020AM Dual Synthesizers

UMA1020M [2] is used in 2 GHz applications, like PHP, DCS1800 or DECT. Its principal synthesizer operates from 1.7 to 2.4 GHz. It offers the same functions as the UMA1018M dual synthesizer including the 7-bit DAC. The UMA1020AM [3] principal synthesizer works from 1 to 1.7 GHz. It does not include the DAC.

1.4.2 UMA1017M and UMA1019M/UMA1019AM Single Synthesizers

The UMA1017M [4] and UMA1019M/UMA1019AM integrated circuits are derivatives from UMA1018M and UMA1020M, respectively with similar pinning. They contain the principal synthesizer only. UMA1017M operates from 50 to 1250 MHz, UMA1019M [5] from 1.7 to 2.4 GHz and UMA1019AM [6] from 1 to 1.7 GHz. Neither contains the auxiliary synthesizer or the DAC (see Figure 1–3).

In this application note, no extra mention will be made about UMA1020AM and the single synthesizers. All UMA1018M and UMA1020M principal synthesizer descriptions and results are valid for other circuits.

Table, overleaf, summarizes characteristics and typical applications of each synthesizer.

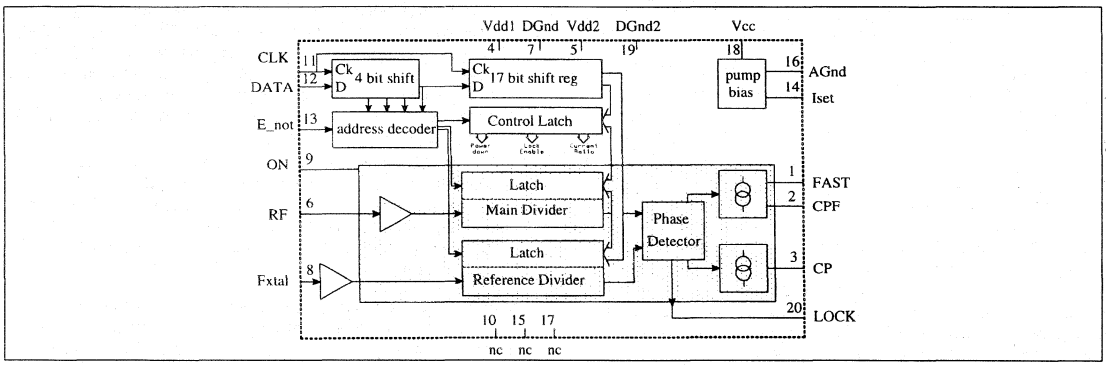


Figure 1–3. UMA1017M and UMA1019M/UMA1019AM Block Diagram

Table 1–1. **Frequency Synthesizers Update**

Part No.	Supply	Consumption	RF Input Frequency	Main Applications
UMA1017M	2.7 to 5.5 V	7.7 mA (5.5 V) 36 µA (PD)	Single 50 to 1250 MHz	CT2 digital cordless GSM digital cellular General purpose
UMA1018M	2.7 to 5.5 V	10 mA (5.5 V) 36 µA (PD)	Dual 50 to 1250 MHz (main) 20 to 300 MHz (aux)	Cellular systems like GSM Applications with UHF and VHF synthesizers
UMA1019AM	2.7 to 5.5 V	9.4 mA (5.5 V) 36 µA (PD)	Single 1 to 1.7 GHz	General purpose
UMA1019M	2.7 to 5.5 V	9.4 mA (5.5 V) 36 µA (PD)	Single 1.7 to 2.4 GHz	DECT Zero IF Cordless and wireless radios
UMA1020AM	2.7 to 5.5 V	12.1 mA (5.5 V) 36 µA (PD)	Dual 1 to 1.7 GHz (main) 20 to 300 MHz (aux)	General purpose
UMA1020M	2.7 to 5.5 V	12.1 mA (5.5 V) 36 µA (PD)	Dual 1.7 to 2.4 GHz (main) 20 to 300 MHz (aux)	Ideal for DECT superhet Digital cordless and wireless radios

2. FUNCTIONAL DESCRIPTION OF THE UMA1018M AND UMA1020M SYNTHESIZERS

The principle of the Phase Locked Loop (PLL) is illustrated in the PLL application block diagram (Figure 3–1).

A crystal (VTCXO) provides a reference frequency to the PLL. A phase detector drives a charge pump to send correction current pulses to a low pass filter. Current pulses are proportional to the difference in phase between the two phase detector input signals. The filter integrates the pulses giving a voltage which controls a Voltage Controlled Oscillator. VCO frequency and crystal frequency are divided down to a common comparison frequency to control the phase detector. The PLL is locked when the phase difference between input signals is maintained null.

2.1 Phase Detector and Charge Pump

2.1.1 Description

The principal and auxiliary phase detectors in the dual synthesizers are sensitive to both phase and frequency. They react to small phase differences between the main divider and reference divider inputs. The design responds to the full $\pm 2\Pi$ radians range of phase inputs.

The operating principle of the phase detectors is depicted in Figure 2–1. The comparison frequency f_{PC} at the inputs of the phase detector is typically the same as the radio system channel spacing. The phase detection is performed once each period of the comparison frequency.

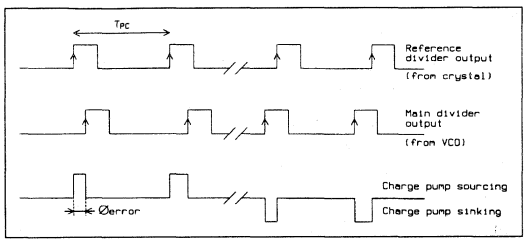


Figure 2–1. Principle of UMA1018M Phase Detectors

The charge pump outputs of the synthesizers are either sourcing, sinking or in high impedance. When the loop is locked, i.e., when the phase error at the input of the phase detector is zero, the charge pump output is in the high impedance state. When the loop is not locked, a phase error between the input signals is seen by the phase detector and the charge pump sends correction current pulses to the loop filter. If the output of the reference divider is leading, then the charge pump sources current pulses to increase the VCO control voltage and frequency. If the output of the reference divider is lagging, then the charge pump sinks current pulses to decrease the VCO control voltage and frequency. The pulse duration is proportional to the phase error. The sinking and sourcing pulses charge or discharge the capacitors in the loop filter, to a voltage required to bring the PLL back into lock.

The principal phase detector drives two charge pumps (pins CPP and CPPF). The charge pump current (the "height" of the positive or negative pulses in Figure 2.1) are switch–selectable by software. I_{CPPF} maximum output current is 3.2 mA, and that for CPP is 0.4 mA. The I_{CPPF}:I_{CPP} current ratio between the two charge pumps varies from 4 to 16. The reference current I_{SET} is set by an external resistance R_{ext} at pin I_{SET}, where a temperature independent voltage of 1.2 volts is generated. R_{ext} should be between 12 kΩ and 60 kΩ to give an I_{SET} between 100 µA and 20 µA. The auxiliary charge pump output current (pin CPA) is always 4 x I_{SET} the charge pump output currents can be programmed as shown below.

Table 2–1. Charge Pumps Current Ratio Relationships

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	I_{CPPF} : I_{CPP}
0	0	4 x I_{SET}	4 x I_{SET}	16 x I_{SET}	4 : 1
0	1	4 x I_{SET}	4 x I_{SET}	32 x I_{SET}	8 : 1
1	0	4 x I_{SET}	2 x I_{SET}	24 x I_{SET}	12 : 1
1	1	4 x I_{SET}	2 x I_{SET}	32 x I_{SET}	16 : 1

There are three ways to connect the charge pump outputs to the principal loop filter:

- Generally, the two charge pump outputs (CPP and CPPF) are connected together to the loop filter. The loop filter design is given in section 3.1.
- In some applications, the PLL is only closed during frequency switching, and opened during time slots where the transmitter (for open loop modulation) or the receiver must be active. In this case, the pin FAST allows opening the loop by disabling the principal fast charge pump. Only this pump should be connected to the loop filter. The principal charge pump (CPP output) is grounded.
- The third way is to have a dual time constant loop. The loop uses both charge pumps during frequency switching. The phase detector drives just the principal charge pump after the required frequency is obtained. The fast charge pump is disabled by the pin FAST. The loop filter design procedure is shown in section 3.3.

The following curves show measurements of sink and source currents of the auxiliary and principal fast charge pumps, as well as leakage currents (high impedance) of the different charge pumps.

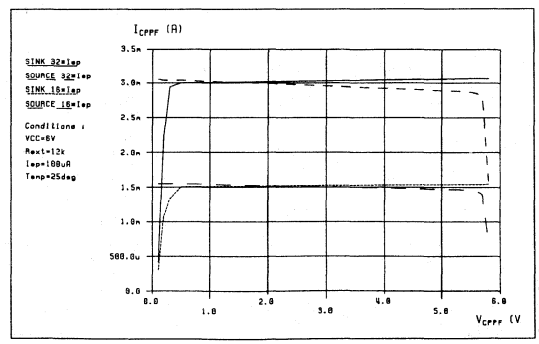


Figure 2–2. Principal Fast Charge Pump (CPPF) Output Current vs Voltage

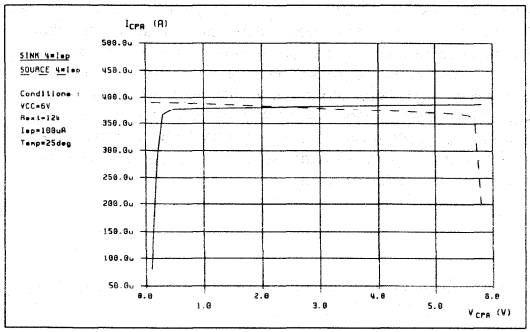


Figure 2–3. Auxiliary Charge Pump (CPA) Output Current vs Voltage

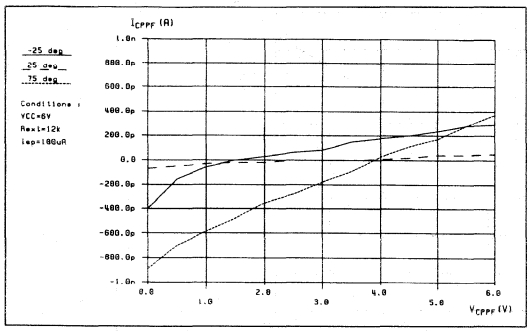


Figure 2–4. Principal Fast Charge Pump Leakage Current vs Voltage and Temperature

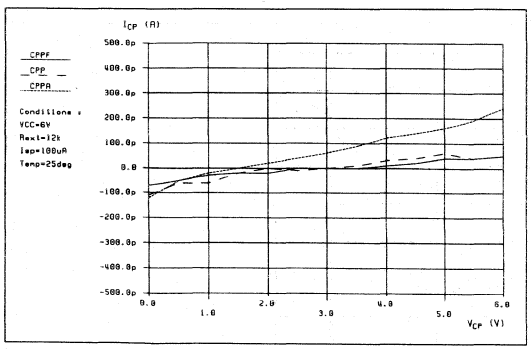


Figure 2–5. Leakage Current of UMA1018M Charge Pumps vs Voltage

2.1.2 Dynamic Characteristics

Two problems occur when the phase detector input signals' edges are very close together, i.e., when the phase error is zero (PLL is locked) or around zero (PLL has nearly settled after switching).

- The first problem is known as the dead–zone. It is due to the finite time the current sources take to switch on. The design of the UMA1018M and UMA1020M takes this into account by introducing a delay in the phase detector reset path. This gives the current sources enough time to respond.
- The second problem is that the charge pump gain is dependent on temperature and VCO control voltage. In this region, the gain varies as a function of the phase error. When the phase error increases outside the defined region, the charge pump gain becomes essentially independent and constant (see curve overleaf). This section is intended to show the linearity of the phase detectors and charge pumps.

Measurement method:

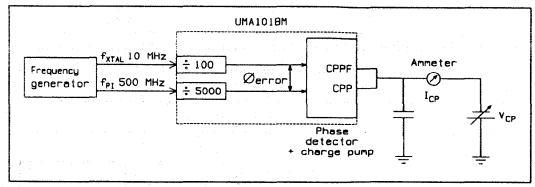
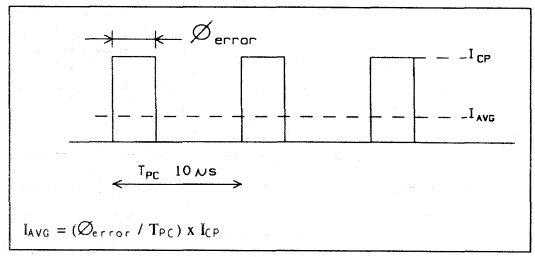
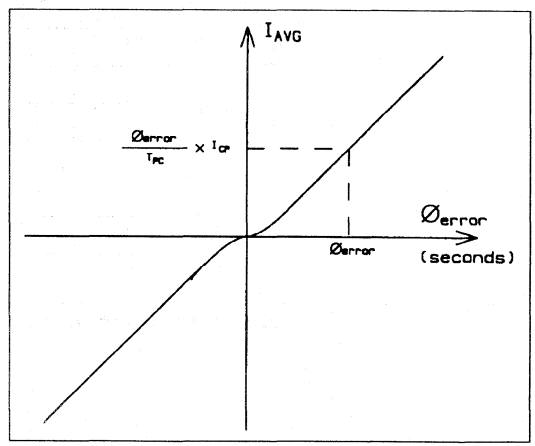


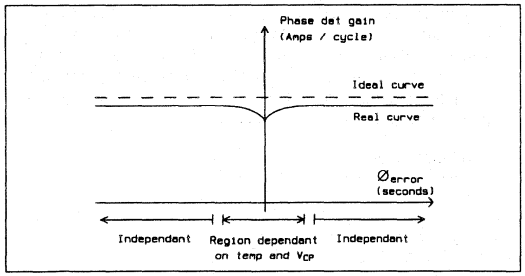
Figure 2–6. UMA1018M Principal Synthesizer Phase Detector Linearity Measurement

A frequency generator supplies the reference frequency f_{XTAL} and the main frequency f_{PI}. These frequencies are divided down to obtain a comparison frequency of 100 kHz. The generator allows controlling the phase of the 500 MHz signal with respect to the 10 MHz reference signal. The I_{AVG} phase detector current is measured as a function of the phase error:





In order to find the real phase detector and charge pump gain for very small phase errors, we transform this curve by the equation: Phase det gain (Amps/cycle) = $I_{AVG} \times (T_{PC}/\Phi error)$



Phase error values are taken in the region of ±10 ns. This is where the phase detector and the charge pump are less linear and where the loop spends most of its time, i.e., when it is locked or nearly locked. The following curves show measurements for source and sink gains around zero, showing the small departure from ideal. The jagged nature of the curves can partly be explained by very small values of I_{AVG}, and phase error giving granularity problems. In any case real charge pump gain for very small phase errors is mostly maintained within 25% of ideal value.

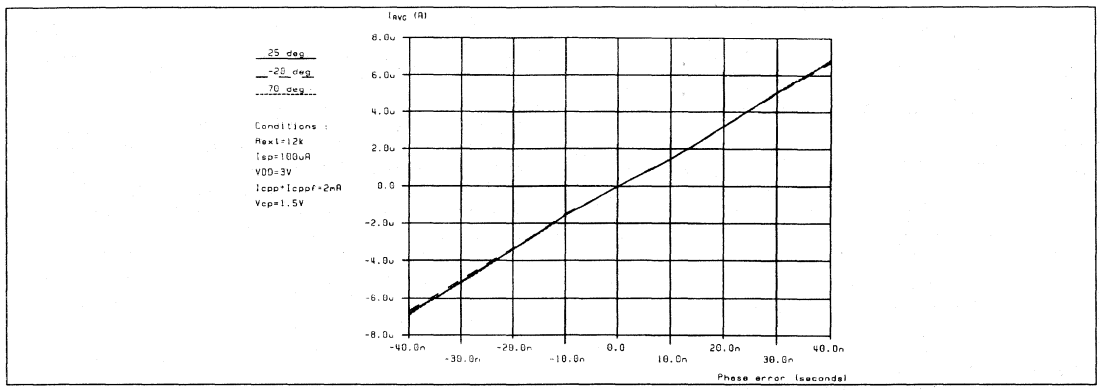


Figure 2–7. Principal Phase Detector and Charge Pump Characteristics vs Temperature

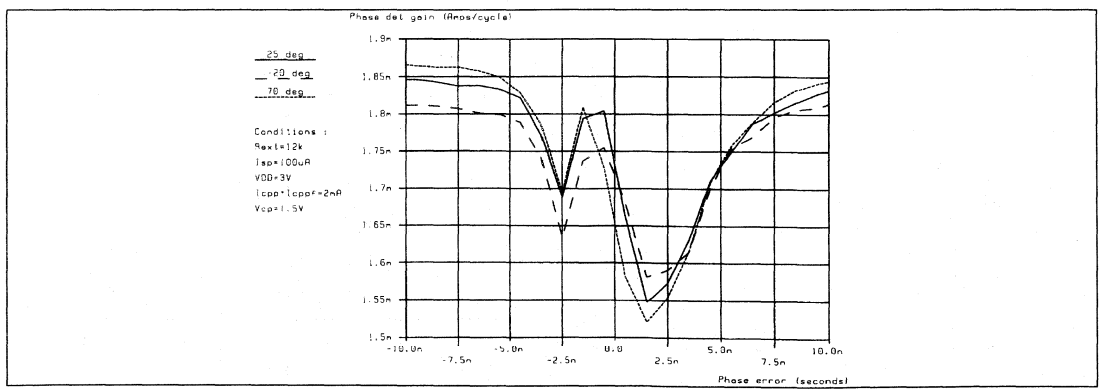


Figure 2–8. Principal Phase Detector and Charge Pump Gain vs Temperature

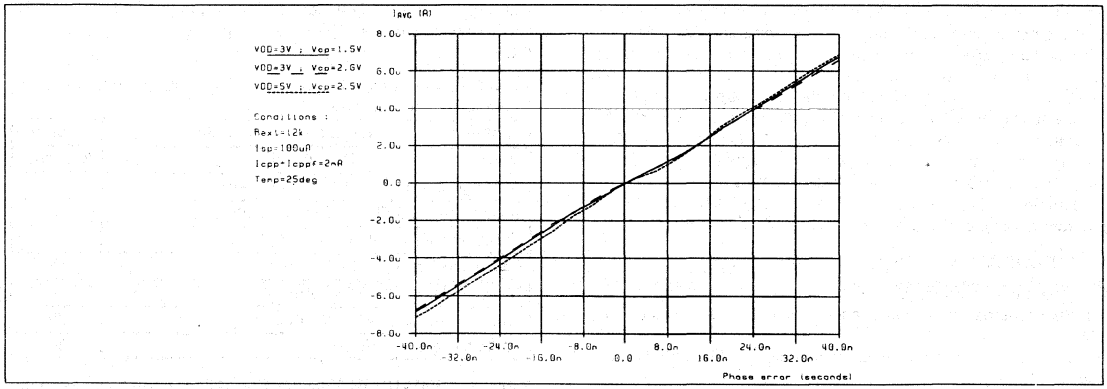


Figure 2–9. Principal Phase Detector and Charge Pump Characteristics vs Temperature

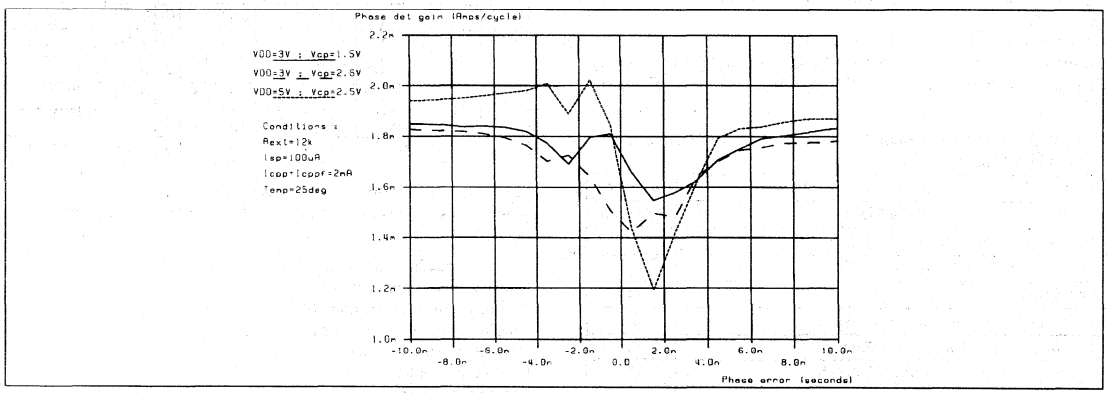


Figure 2–10. Principal Phase Detector and Charge Pump Gain vs V_{DD}

2.2 Programming

A simple 3-wire unidirectional serial bus is used to program the synthesizer. The three lines are DATA, CLK (Clock) and $\overline{E}$ (Enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges are ignored until $\overline{E}$ goes active low. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive high. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power–down of either or both synthesizers.

After software or hardware power down is terminated, it is not necessary to program the device. Previous programming data is preserved during power down.

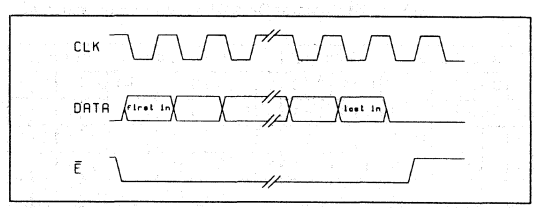


Figure 2–11. Serial Interface Timing Diagram

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are used for the address. The bits are decoded on the rising edge of $\overline{E}$. Two worked examples of programming are shown overleaf.

Special care has to be taken for correct programming when first applying power to the synthesizer. The E signal should be held LOW and only taken HIGH after having programmed an appropriate register on first powering up. If this condition is not achieved, it may result in loading of random data from the serial bus shift register (programming register) into one of the synthesizers data registers including the test register. It should be noted that the test register does not normally need to be programmed. However, if it is programmed, all bits in the data field should be set to 0. In case of random data being loaded into the test register, it is possible to program a frame of zeros, to return to normal operation.

2.2.1 UMA1018M Typical Programming Example

f_{XTAL} input frequency: 13 MHz
Principal synthesizer input frequency: 900 MHz (main divider ratio = PM = 4500)
Principal synthesizer comparison frequency: 200 kHz (main divider ratio = PR = 65)
Auxiliary synthesizer input frequency: 100 MHz (main divider ratio = AM = 1000)
Auxiliary synthesizer comparison frequency: 100 kHz (main divider ratio = AR = 130)
Both synthesizers ON (AON = PON = 1)
Out-of-lock indication from both synthesizer loops (OLP = OLA = 1)
Charge pump currents: $I_{CPPF} = 32 \times I_{SET}$; $I_{CPP} = 4 \times I_{SET}$ (CR1 = 0 CR0 = 1)

Table 2–2. UMA1018M Register Data Allocations Expressed in Decimal and Hexidecimal

First In	Register Bit Allocation	Last In
dt16	Data Field dt0	Address
Test register (must be 0 if programmed)		0h
Control reg = 0 0001 101010110 0000b		1h
Principal main = 4500d = 01194h		4h
Principal reference = 65d = 00041h		5h
Auxiliary main = 1000d = 003E8h		6h
Auxiliary reference = 130d = 00082h		7h
DAC setting is 123d = 0007Bh		8h

Table 2–3. UMA1018M Register Data Allocations Expressed in Binary

First In (MSB)						Data Field							(LSB) Last In					Address			
0	0	0	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1
0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	0	0	0

2.2.2 UMA1020M Typical Programming Example

f_{XTAL} input frequency: 13.824 MHz
Principal synthesizer input frequency: 1890.432 MHz (main divider ratio = PM = 1094)
Principal synthesizer comparison frequency: 1728 kHz (main divider ratio = PR = 8)
Auxiliary synthesizer input frequency: 300.52 MHz (main divider ratio = AM – 3000)
Auxiliary synthesizer comparison frequency: 100.17 kHz (main divider ratio = AR = 138)
Both synthesizers ON (AOFF = POFF = 0)
Out-of-lock indication from both synthesizer loops (OLP = OLA = 1)
Charge pump currents : $I_{CPPF} = 32 \times I_{SET}$; $I_{CPP} = 4 \times I_{SET}$ (CR 1 = 0 CR0 = 1)

Table 2–4. UMA1020M Register Data Allocations Expressed in Decimal and Hexidecimal

First In	Register Bit Allocation	Last In
dt16	Data Field dt0	Address
Test register (must be 0 if programmed)		0h
Control reg = 0 0001 1010 0000 0000b		1h
Principal main = 1094d = 00446h		4h
Principal reference = 8d = 00008h		5h
Auxiliary main = 3000d = 00BB8h		6h
Auxiliary reference = 138d = 00082h		7h
DAC setting is 123d = 0007Bh		8h

Table 2–5. UMA1020M Register Data Allocations Expressed in Binary

First In (MSB)						Data Field							(LSB) Last In					Address			
0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1
0	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	0	0	0

2.2.3 UMA1018M and UMA1020M Preset Values

After the supply voltage is switched on, the preset values are normally:

Principal main divider ratio: 4500
Principal reference divider ratio: 65
Auxiliary main divider ratio: 8000
Auxiliary reference divider ratio: 1040
Control register: all 1 except out-of-lock
DAC register: all 0
Test register: all 0

2.2.4 Enable Pulse Width

With $\overline{E}$, a minimum inactive pulse width (T_W in the specification) is necessary before sending a new data burst. Due to internal synchronization, this minimum width depends on the input frequency to the main dividers and the reference divider. In the specification, this is indicated as 4 µs.

In fact, the minimum pulse width (T_W) can be smaller than 4 µs provided the following conditions are all satisfied:

Principal main divider input frequency > $(256/T_W)$
Auxiliary main divider input frequency > $(32/T_W)$
Reference dividers input frequency > $(3/T_W)$

Example: a pulse width of 500 ns can be used if

$f_{PI} > 256 / 500$ ns $f_{PI} > 512$MHz
$f_{AI} > 32 / 500$ ns $f_{AI} > 64$MHz
$f_{XTAL} > 3 / 500$ ns $f_{XTAL} > 6$MHz

2.3 Reference Divider

The input f_{XTAL} drives a preamplifier to provide the clock input for the reference dividers. The auxiliary reference divider is clocked on the opposite edge to the main reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at

different times. This minimizes the potential for interference between the charge pumps of each loop. Figure 2–12 shows the typical measured input sensitivity of the reference divider.

Some sensitivity to the reference input signal level on overall loop noise performance has been observed. Better performance is obtained for a higher level of f_{XTAL}.

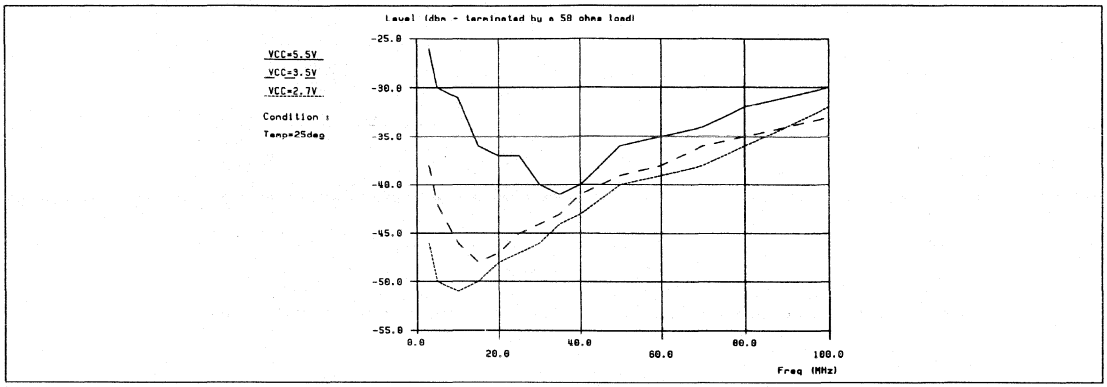


Figure 2–12. Reference Divider Input Sensitivity vs Frequency

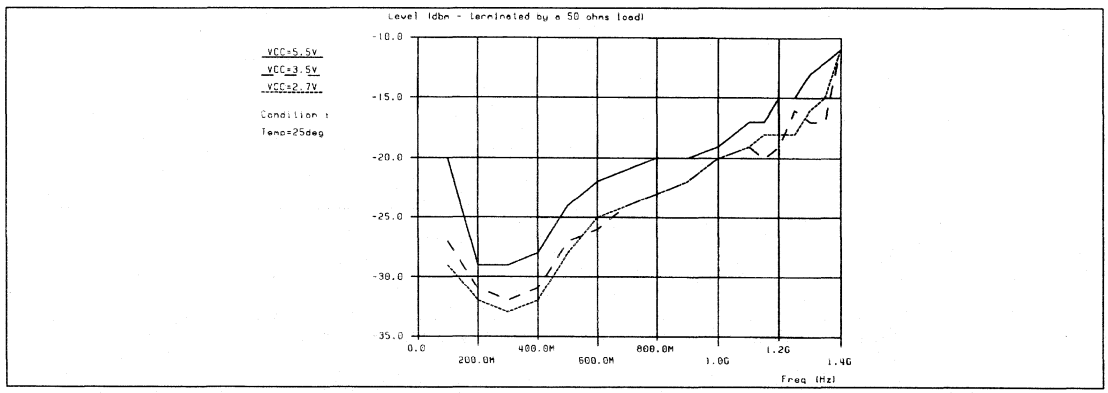


Figure 2–13. UMA1018M Principal Main Divider Input Sensitivity vs Frequency

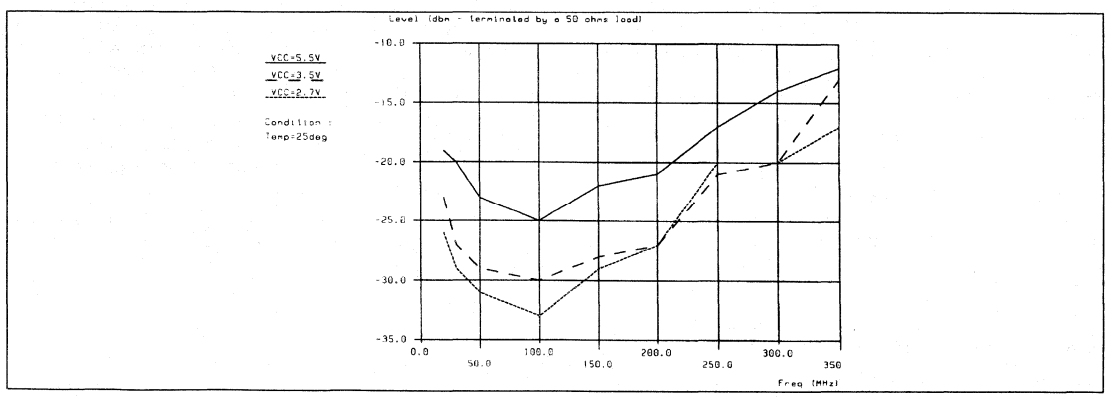


Figure 2–14. Auxiliary Main Divider Input Sensitivity vs Frequency

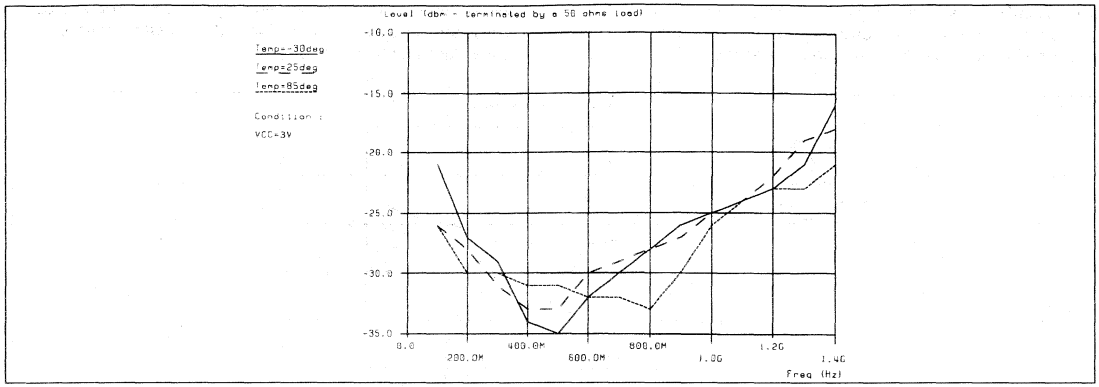


Figure 2–15. UMA1018M Principal Main Divider Input Sensitivity vs Frequency and Temperature

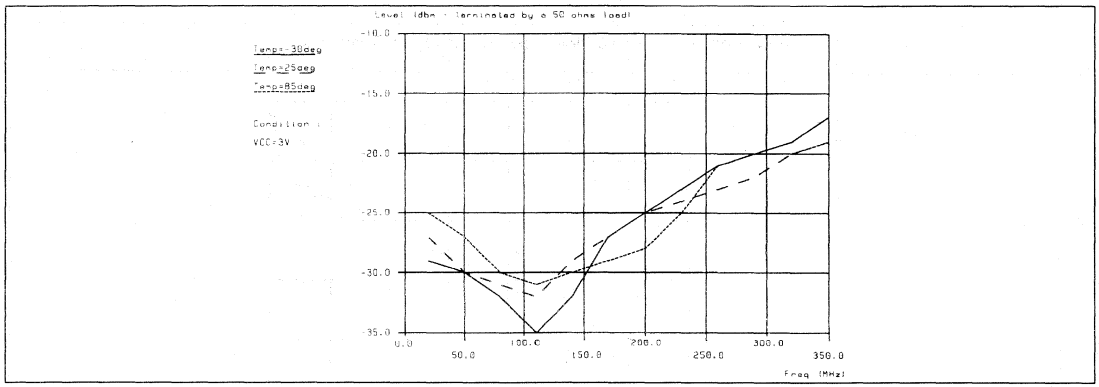


Figure 2–16. Auxiliary Main Divider Input Sensitivity vs Frequency and Temperature

2.4 Main Divider

The RF input drives a preamplifier to provide the clock for the main dividers. The preamplifier has a high input impedance, dominated by pin and pad capacitance. The high frequency sections of the main dividers are implemented using bipolar logic, while the slower sections use lower current CMOS logic. Figures 2–13 to 2–16 show the typical measured input sensitivity of the principal and auxiliary main dividers. Two samples were selected at random, with the device used for frequency versus temperature measurement showing better sensitivity.

2.5 Voltage and Ground Pins

Separate power and ground pins are provided to the analog and digital circuits. To reduce crosstalk between CMOS and bipolar parts, two independent pins supply the digital parts of the integrated circuit (V_{DD1} and V_{DD2}). V_{DD2} pin supplies the principal main divider bipolar section, V_{DD1} pin other digital sections. V_{DD1} and V_{DD2} could be shorted at the pins, however, separate decoupling will be better. The voltages at these pins should be similar.

The ground leads should be externally shorted together otherwise large currents may flow across the die, and damage it.

2.6 In lock Detector

There is a lock detector on-chip for each synthesizer. The lock condition of one, or both loops, can be indicated via an open-drain transistor which drives in-lock detect pin. A pull up resistor must be connected to the output. Whenever a phase difference occurs at the input of a phase detector this produces a pulse that can pass through to the out-of-lock pin (see Figure 2.17).

When integrating the OOL output to convert the pulsed output to a level, a resistor must be added between the OOL pin and the capacitor. This avoids that a current bigger than 400 µA flows through the pin from the capacitor.

The lock output is software selectable as given in Table 2–6 below. Operating principle of out-of-lock is described overleaf.

Table 2–6. Out-Of-Lock Bit Allocations

OLP	OLA	Out-of-Lock Select
0	0	Output disabled
0	1	Auxiliary phase error
1	0	Principal phase error
1	1	Both auxiliary and principal

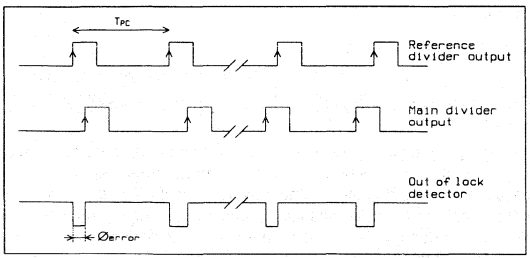


Figure 2–17. Operating Principal of the Out-of-Lock Detector

2.7 Digital-to-Analog Converter

A digital-to-analogue converter is integrated on the UMA1018M and UMA1020M synthesizers.

The DAC output current is scaled by the external resistance R_{ext} at pin I_{SET}, also used by the charge pumps. The nominal full scale current is 2 x I_{SET}. An external user-defined ground referenced resistance connected to the DAC output allows producing a full scale voltage (from 0V to V_{DD1} – 0.4V).

The DAC signal is monotonic across the full range of programmation. A programmed code of 00 corresponds with the minimum DAC leakage current (I_{10min}). It should be less than 5 µA programmed code of 7F corresponds to 2 x I_{SET} x (127 / 128).

The worst monotonic cases occur between 3Fh and 40h, 1Fh and 20h. Here, ΔI measured varies from 0.1 x $\Delta I_{expected}$ to 1.9 x $\Delta I_{expected}$.

Example:

R_{ext} = 12k I_{SET} = 1.2 / 12k = 100 µA
$\Delta I_{expected}$ = I_{SET} x 2 x (3Fh – 40h) / 128 = 1.56 µA
° $\Delta I_{measured}$ can vary between 0.16 µA to 3 µA

The on-board DAC allows adjustment of an external component, such as the central frequency of a VTCXO (Voltage Controlled Temperature Compensated Crystal Oscillator).

3. LOOP FILTER DESIGN

3.1 Basic Loop Filter Design Procedure

This section gives the procedure to ensure a quick and simple loop filter design. The method is based on first order approximations, and provides a working solution without the need for computer simulation. Reading appendices A and B can be useful to clarify some PLL terms and equations of this chapter.

The purpose of a Phase Locked Loop (PLL) in a single loop frequency synthesizer as shown in Figure 3–1 is to transfer the spectral purity and stability of a fixed reference frequency oscillator (TCXO or VTCXO) to that of the Voltage Controlled Oscillator (VCO) output.

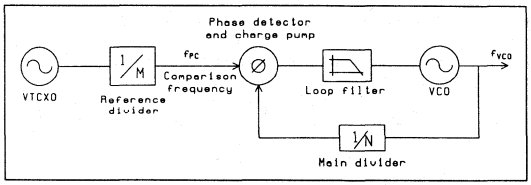


Figure 3–1. Basic Phase Lock Loop Block Diagram

The correct design of the loop filter is of considerable importance to have the optimum performance from the synthesizer. The filter should be designed so as to achieve the required compromise between noise performance and switching time.

Loop filters are usually passive when used with current charge pumps, but can be active if desired. Passive loops have the advantage of reduced noise, fewer parts count and low cost. With UMA1018M or UMA1020M synthesizers, only passive loop filters are necessary. Two common configurations are shown overleaf. The filters in Figure 3–2 are classified in terms of the order of the loop formed.

With the UMA1018M or UMA1020M, the use of the loop filter (a) is often sufficient. For applications requiring further comparison frequency breakthrough rejection, a low pass filter stage (R_3, C_3) can be added. It reduces comparison frequency breakthrough spurs without affecting too much the transient response of the loop when correctly designed.

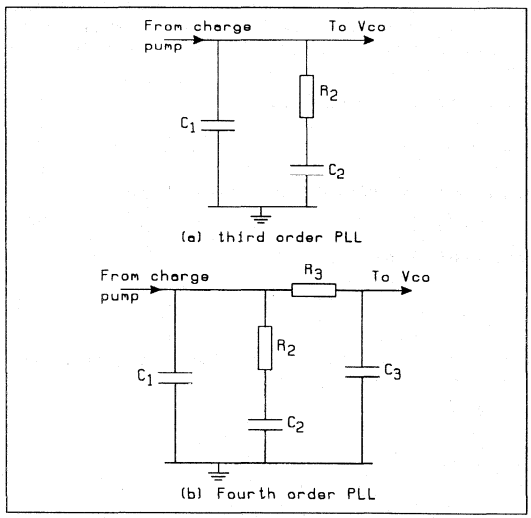


Figure 3–2. Different Types of Passive Loop Filter

Loop parameters are first chosen, they are:

- VCO frequency f_{VCO} (in Hz)
- Phase comparator frequency f_{PC} (in Hz)
- Switching time t_S (in seconds)
- VCO gain K_{VCO} (in Hz/V)

- Phase comparator gain I_{CP} (in amps/cycle)

As the starting point, the equations below are used.

$$W_n = 2 \cdot \Pi \cdot f_n = \left(\frac{K_{VCO} \cdot I_{CP}}{C_2 \cdot N}\right)^{1/2} \quad (1.)$$

$$R_2 = 2 \cdot \rho\left(\frac{N}{(K_{VCO} \cdot I_{CP} \cdot C_2)}\right)^{1/2} \quad (2.)$$

where f_n is the natural frequency (in Hz) and ρ is the damping coefficient.

Calculate the resistor R_{ext} for setting the charge pump output current from

$$R_{ext} = \frac{1.2}{I_{SET}} \quad (3.)$$

I_{CP} is related to I_{SET} according to the relationship given in Table 2–1 and whether the two charge pumps CPP and CPPF are shorted together or not.

Determine the natural frequency f_n

$$f_n = \frac{2.5}{t_S} \quad (4.)$$

It has been found by experience that a good PLL loop filter design takes a switching time (t_S) of less than $2.5/f_n$ to settle to a new frequency. This rule of thumb allows a good compromise between switching time, stability and noise performance when using the UMA1018M and UMA1020M synthesizers. Of course the switching time will also depend on the size of the frequency jump and the definition of when the PLL is settled (i.e., acceptable frequency or phase error with respect to target).

Determine main divider ratio from

$$N = \frac{f_{VCO}}{f_{PC}} \quad (5.)$$

Determine angular velocity W_n (in rad/seconds) from

$$W_n = 2 \cdot \Pi \cdot f_n \quad (6.)$$

Determine C_2 from (1)

$$C_2 = \left(\frac{K_{VCO} \cdot I_{CP}}{W_n^2 \cdot N}\right) \quad (7.)$$

Select damping ratio of approximately 0.9 for a good compromise between switching time and stability.

Determine R_2 from (2)

$$R_2 = 2 \cdot \rho\left(\frac{N}{K_{VCO} \cdot I_{CP} \cdot C_2}\right)^{1/2}$$

Choose C_1 between 1/10 and 1/15 the value of C_2

Determine R_3 from

$$R_3 \geq 2 \cdot R_2 \quad (8.)$$

Determine C3 from

$$C3 < \left(\frac{R_2 \cdot C_2}{20 \cdot R_3}\right) \quad (9.)$$

A program using this cook book method has been written for use on IBM PC (and compatible). It is included with the 3-wire serial bus control software diskette. Values given by the program are approximate and the final values should be optimized. For further optimization, both computer simulation programs, as well as practical experiments, are required.

Capacitors with high leakage currents, such as electrolytic capacitors and capacitors with piezoelectric or delay effects are not preferred because of higher comparison frequency breakthrough and increased switching times. A polyester film capacitor is a good idea for C_2.

3.2 Analysis and Simulation

For analysis, optimization and worst case design of more complex filters, key loops parameters can be entered into a simulation program.

Generally, a stable loop with an acceptable noise performance and a given switching time is needed. Unfortunately, these two requirements are dependent and must be traded off against each other. Stability, being an absolute necessity, gets higher priority. With third order loop filters (see Figure 3–3), the phase margin is the simplest criterion for the stability.

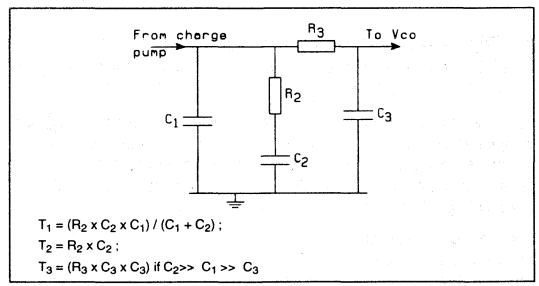


Figure 3–3. Third Order Loop Filter

The phase margin is easily determined from the Bode plot. A Bode plot displays the open loop transfer function magnitude and phase. Figure 3–4 shows Bode plot of a fourth order loop with third order filter (type 3 fourth order system) and a pole in the origin due to the VCO.

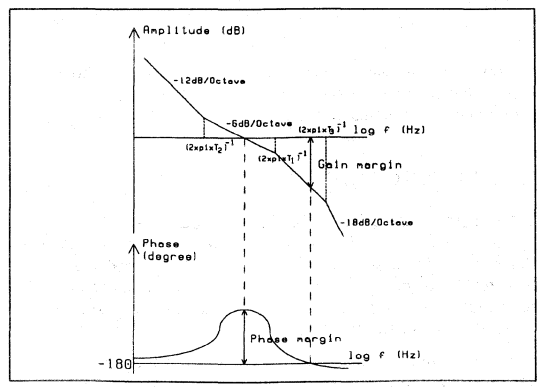


Figure 3–4. Bode Plot 4th Order Open PLL Transfer Function Magnitude and Phase

The phase margin is defined as the difference between 180° and the phase of the open loop transfer function at the frequency where the gain is 1 (gain cross over). The critical point for stability is a phase margin of 0°. The factor by which the system gain would have to be increased for the phase margin to reach the critical value of 0° is called the gain margin.

The time constants in the loop filter are key to controlling the overall loop performance and phase margin. The offset of different time constants can be evaluated from the Bode diagram. The reciprocal of the time constants of the loop filter in Figure 3–3 are the break points in the magnitude plot of Figure 3–4.

When increasing the time constant $T_3 = C_3 \times R_3$, the breakpoint (T_3)–1 will move left and the magnitude curve will start to roll off at a lower frequency. Therefore, the greater the time constant T_3, the better the comparison frequency breakthrough is suppressed. But increasing T_3 will force the point of inflection of the phase margin curve to move to the left as well, this decreasing the phase margin and eventually reducing system stability.

By iteration, inspection of the Bode plot, adjusting the loop filter values and measuring the performance, will yield a compromise between switching time, stability and noise. Simulation programs may give reasonable approximations of PLL behavior, but their accuracy is always limited due to the fact that many practical imperfections and non linearities are not taken into account.

Phase margin between 30° and 70° is required for most applications. The larger the phase margin, the more stable the loop, and the slower the transient response and hence the switching time. A loop with a low phase margin is still stable but may exhibit other problems aside from outright oscillation, low phase margin makes the transient response more oscillatory. A phase margin of 45° is a good compromise between desired stability and the other generally undesired effects.

3.3 Adaptive Loop

Some applications may need to have a dual time constant loop. With two principal charge pumps, UMA1018M and UMA1020M allow this to be implemented. The loop uses both charge pumps for fast frequency switching. Then the phase detector drives just the principal charge pump (CPP) after obtaining the required frequency with a lower bandwidth and hence lower noise. The loop filter used is shown in the Figure 3–5. This filter allows an optimized filter when both charge pumps are ON or when just one charge pump is active.

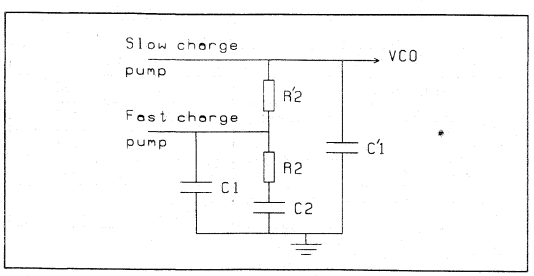


Figure 3–5. Adaptive Loop Filter

The loop filter calculation is given below:

- Use the same design procedure from paragraph 3.2 to calculate the main capacitor C_2, the damping resistor R_2 and the filter capacitor C_1.
- When the fast charge pump CPPF is disabled, loop stability needs to be maintained for the loop which uses only CPP. Recalculate value for the damping resistor with the new value of I_{CP} and $\rho = 0.9$

$$R'_2 = 2 \cdot \rho \left(\frac{N}{(K_{VCO} \cdot I_{CP} \cdot C_2)} \right)^{1/2} - R_2$$

- Determine C'_1 from

$$C'_1 < \frac{R_2 \cdot C_2}{20 \cdot R'_2}$$

Some precautions must be taken when the principal fast charge pump is switched off. A parasitic capacitor, due to the integrated circuit and the printed circuit board, exists between the FAST and CPPF pins. When the signal is sent to the FAST pin, a coupling through the parasitic capacitance on to the CPPF pin, results in a VCO frequency drift. This problem can he reduced by decreasing the slope of the FAST signal with a RC filter.

3.4 PCB Layout Considerations

With frequency synthesizer layout, good RF design techniques should be employed. To avoid crosstalk between synthesizers (auxiliary and principal), the printed circuit board should have a solid ground plane on the non surface mount side (apart from isolated pads for non-grounded connections to leaded components). On the surface mount side of the board, the ground plane should be designed round each synthesizer, and underneath the Philips integrated circuit so as to provide maximum isolation between two PLLs. A good number of plated-through holes must connect the two layers of the ground plane.

Suitable high frequency capacitors (100 nF) in series with a small value resistor (12Ω) should be used for power supply decoupling. V_{DD1} and V_{DD2} can be shorted at the output of the integrated circuit. However, separate decoupling to Pins 4 and 5 will be better. It is very important to de-couple as close as possible to Pins 4 and 5.

3.5 Worked Example

In this chapter, a design example based on the fourth order PLL for GSM specification is shown. Only the loop filter of the UMA1018M principal synthesizer is calculated.

Experiments show that the use of just one charge pump gives better close in noise (about 3dBc/Hz) than two enabled charge pumps with outputs (CPPF + CPP) connected together. Because slow charge pump is better (about 1 dBc/Hz) than fast charge pump, only the slow charge pump is used in this worked example. The fast charge pump is switched off via pin FAST.

- VCO Frequency f_{VCO} = 902MHz
- Phase comparator frequency f_{CP} = 200kHz
- Switching time t_S = 600µs
- VCO gain K_{VCO} = 11MHz/V
- Phase comparator gain I_{CP} = 0.4mA with CR1 bit set to 0 and CR0 bit set to 0. Pins CPP and CPPF connected together. Fast charge pump is switched off by the pin FAST. Following the basic design procedure from paragraph 3.2 yields:

$I_{CP} = 0.4mA = 4 \times I_{SET} \rightarrow I_{SET} = 100\mu A$
$R_{ext} = 1.2 / I_{SET} = 1.2 / 100\mu A = 12k\Omega$
Natural frequency $f_n = 2.5 / t_S = 2.5 / 60\mu s = 4170Hz$
Main divider ratio $N = f_{VCO} / f_{CP} = 902MHz / 200kHz = 4510$

The main components in the loop filter are:

main capacitor C_2 $= K_{VCO} \times I_{CP} / W_n^2 \times N$
$= 11MHz \times 0.4mA / (2 \times 11 \times 4170)^2 \times 4510$
$= 1.5nF$

damping resistor R_2 $= 2 \times \rho \, (N / K_{VCO} \times I_{CP} \times C_2)^{1/2}$
$= 2 \times 0.9 \, (45101 / 11MHz \times 0.4mA \times 1.5nF)_{1\backslash2}$
$= 47k\Omega$

filter capacitor $C_2 / 15 \leq C_1 \leq C_2 / 10$ $C_1 = 100pF$

$R_3 \geq 2 \times R_2$ $R_3 = 100k\Omega$

$C_3 < (R_2 \times C_2 / 20 \times R_3)$ $C_3 = 22pF$

A software simulation program has been used to verify the stability of this loop filter. The phase margin is maximum and equal to 52° at the gain cross-over point. The requirement for basic loop stability is fulfilled (see Figure 3–6).

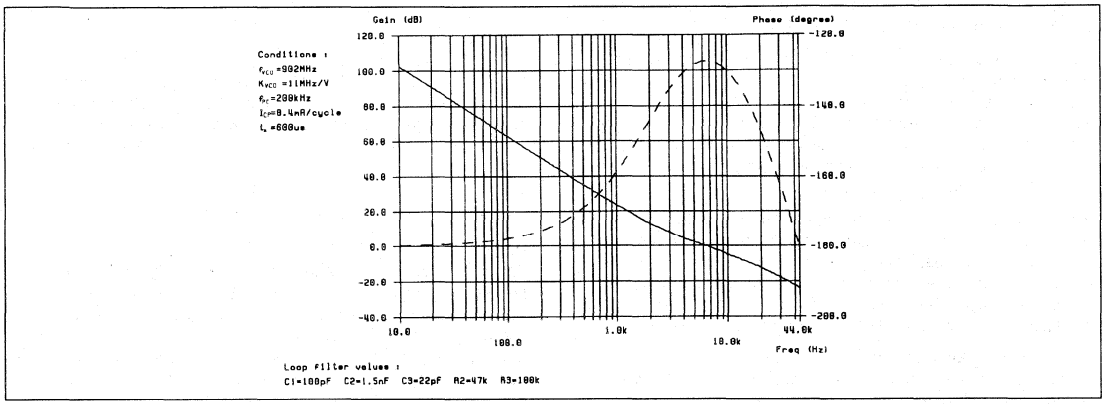


Figure 3–6. Simulated Bode Plot of 4th-Order Open Loop Transfer Function of UMA1018M Principal Synthesizer, Magnitude and Phase vs Frequency

The design procedure is similar with the auxiliary synthesizer and with the UMA1020M for the DCS1800 application. Results are summarized in Table 3–1 and 3–2.

Table 3–1. Design Parameters and Simulation for UMA1018M Dual Synthesizer

Parameter		Principal synthesizer	Auxiliary synthesizer
Loop components (refer to figure 3.3) VCO		C_1 = 100p C_2 = 1.5n C_3 = 22p R_2 = 47k R_3 = 100k	C_1 = 470p C_2 = 10n C_3 = 100p R_2 = 18k R_3 = 39k
VCO gain K_{VCO} VCO frequency f_{VCO}		11MHz/V 902MHz	2.5MHz/V 100MHz
Comparison frequency f_{PC}		200kHz	100kHz
Charge pump	Current gain I_{CP}	0.4mA/cycle	0.4mA/cycle
	R_{ext}	12k	
	Bits CR0, CR1	CR0 = 0, CR1 = 0	
Reference frequency VTCXO		13MHz	
Unity gain phase margin (simulated)		52.6 deg	58.9 deg
Gain margin at 180 deg phase margin (simulated)		24dB	27dB
Unity gain loop bandwidth (simulated)		6.3k	2.8k
Natural frequency (simulated)		4.1k	1.6k
Switching time for a 25MHz step ; freq error < 1kHz (simulated)		540µs	

Table 3–2. Design Parameters and Simulation for UMA1020M Dual Synthesizer

Parameter		Principal synthesizer	Auxiliary synthesizer
Loop components (refer to figure 3.3) VCO		C_1 = 820p C_2 = 13n C_3 = 180p R_2 = 5.6k R_3 = 15k	C_1 = 470p C_2 = 10n C_3 = 100p R_2 = 18k R_3 = 39k
VCO gain K_{VCO} VCO frequency f_{VCO}		20MHz/V 1890MHz	2.5MHz/V 100MHz
Comparison frequency f_{PC}		200kHz	100kHz
Charge pump	Current gain I_{CP}	3.6mA	0.4mA
	R_{ext}	12k	
	Bits CR0, CR1	CR0 = 1, CR1 = 0	
Reference frequency VTCXO		13MHz	
Unity gain phase margin (simulated)		53.2 deg	58.9 deg
Gain margin at 180 deg phase margin (simulated)		25dB	27dB
Unity gain loop bandwidth (simulated)		6.45k	2.8k
Natural frequency (simulated)		3.8k	1.6k
Switching time for a 25MHz step ; freq error < 1kHz (simulated)		550µs	

4. MEASUREMENTS AND TYPICAL RESULTS

This section describes the performance of the UMA1018M and UMA1020M demoboards with the loop filters indicated in Table 3–1 and 3–2.

The relevant performance criteria for a synthesizer are usually:

- Close in phase noise
- Comparison frequency breakthrough
- Switching time
- Integrated phase jitter

Close in noise was measured using a direct reading from the spectrum analyzer and referred to 1Hz bandwidth. This is normally done at a given offset from the carrier while still inside the loop bandwidth.

Integrated phase jitter was measured on a Rohde and Schwartz Modulation Analyzer in a 10Hz to 200kHz audio bandwidth.

Tables 4–1 to 4–3 summarize the measurement results. Figures 4–1 to 4–8 show some of the actual measurements. During the measurements both synthesizers were enabled and locked.

Table 4–1. Demoboard Measurement Results on UMA1018M Principal Synthesizer

VCO supply voltage : 5 volts Both synthesizers enabled UMA1018M supply voltage : 5 volts Temperature=25°C		Principal synthesizer
VCO frequency range		890MHz - 915MHz
Comparison frequency breakthrough	at 200kHz	- 81dBc
	at 400kHz	- 82dBc
	at 600kHz	< -82dBc
Switching time for frequency jump around centre frequency to within 1kHz of the target frequency	200kHz (1 channel)	450µs
	10MHz	500µs
	25MHz (max jump)	580µs
Close in noise (at 1kHz distance from carrier)		-78dBc/Hz
Integrated phase jitter		18 mrad rms

Table 4–2. Demoboard Measurement Results on UMA1020M Principal Synthesizer

VCO supply voltage : 3 volts Both synthesizers enabled UMA1020M supply voltage : 3 volts Temperature=25°C		Principal synthesizer
VCO frequency range		1878MHz - 1903MHz
Comparison frequency breakthrough	at 200kHz	- 77dBc
	at 400kHz	- 81dBc
	at 600kHz	< -82dBc
Switching time for frequency jump around centre frequency to within 2kHz of the target frequency	200kHz (1 channel)	370µs
	10MHz	430µs
	25MHz (max jump)	540µs
Close in noise (at 1kHz distance from carrier)		-70dBc/Hz
Integrated phase jitter (Obtained by integration of close in noise)		53 mrad rms

Table 4–3. Demoboard Measurement Results on Auxiliary Synthesizer

VCO supply voltage : 5 volts Both synthesizers enabled UMA1018M supply voltage : 5 volts Temperature=25°C		Auxiliary synthesizer
VCO frequency		97MHz - 104MHz
Comparison frequency breakthrough	at 100kHz	- 77dBc
	at 200kHz	- 80dBc
	at 400kHz	< -82dBc
Close in noise (at 2kHz from carrier)		-83dBc/Hz
Integrated phase jitter		6 mrad rms

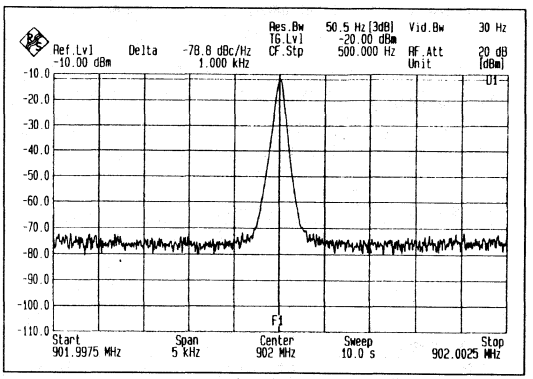


Figure 4–1. UMA1018M Principal Synthesizer Output Spectrum – Close in Noise

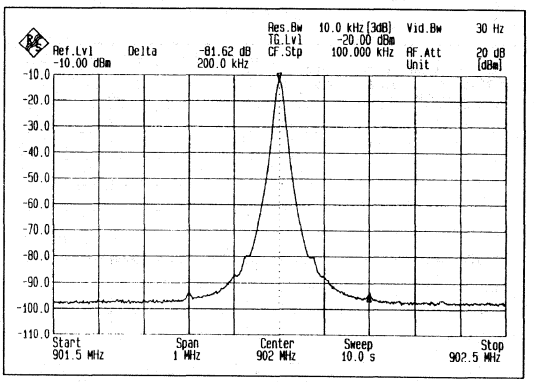


Figure 4–2. UMA1018M Principal Synthesizer – Comparison Frequency Breakthrough

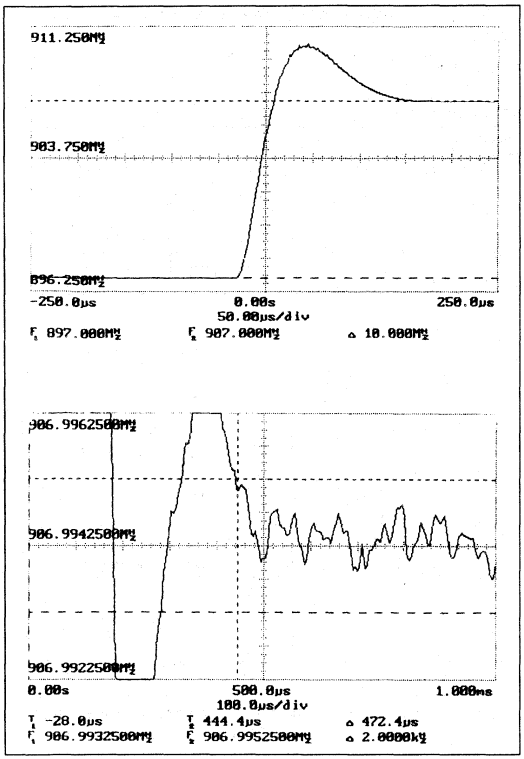


Figure 4–3. UMA1018M Principal Synthesizer – Settling Time for a 10MHz Step

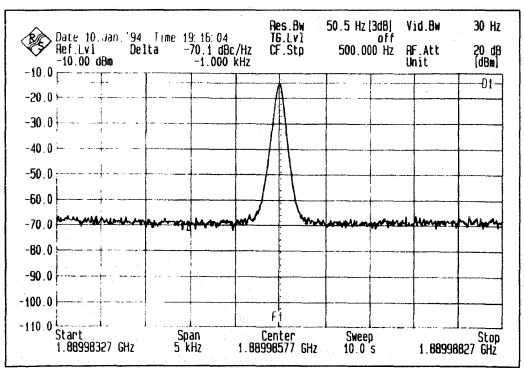


Figure 4–4. UMA1020M Principal Synthesizer Output Spectrum – Close in Noise

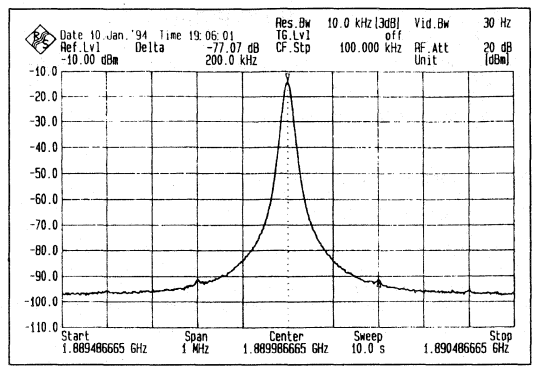


Figure 4–5. UMA1020M Principal Synthesizer – Comparison Frequency Breakthrough

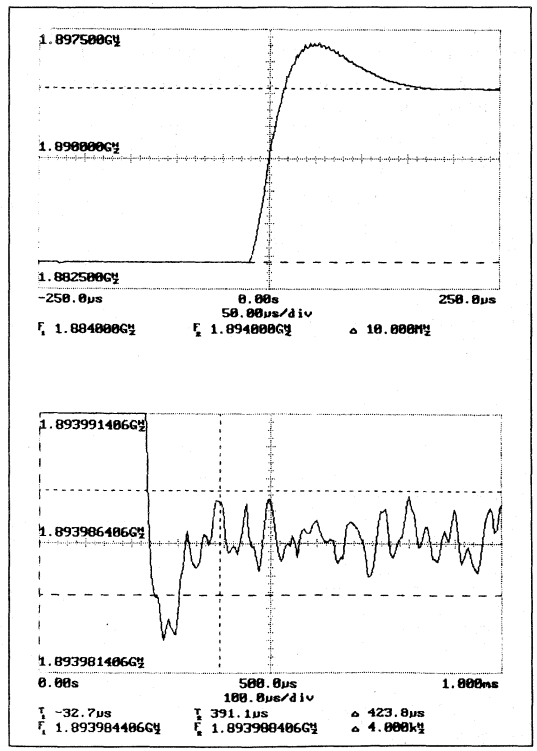


Figure 4–6. UMA1020M Principal Synthesizer – Settling Time for a 10MHz Step

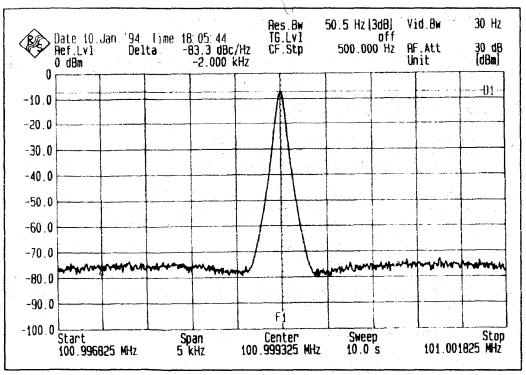


Figure 4–7. UMA1020M Auxiliary Synthesizer Output Spectrum – Close in Noise

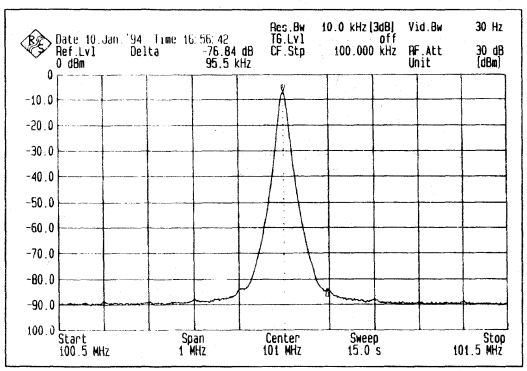


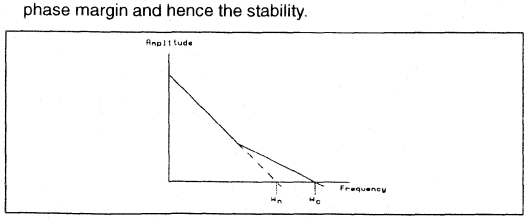
Figure 4–8. UMA1018M Auxiliary Synthesizer – Comparison Frequency Breakthrough

5. APPENDICES

5.1 Appendix A: PLL Terms

The following is a brief glossary of frequently encountered terms in PLL literature.

- **Natural frequency w_n**: the natural frequency of the loop. This is the frequency at which the loop would theoretically oscillate if the damping factor were zero.
- **Open loop cross-over frequency w_C**: this is the frequency at which the open loop gain is unity. It is useful in determining the phase margin and hence the stability.



- **Damping coefficient**: ρ can be used as a measure of the stability in second order systems. It is seldom used as a direct measure of stability in higher order designs.
- **Order of loop**: the order of the loop is the highest power of s (s=jw) in the denominator of the open loop transfer function. The example below shows a second order loop.

  $G(s) \times H(s) = (K_{VCO} \times I_{CP}) \times (s \times T_2 + 1) / (N \times C \times s^2)$
- **Type of loop**: the type of control system formed is defined by the number of perfect integrators in the loop. In the example, above, the loop is a type two system.
- **Phase margin Φm**: The phase margin, in degrees, is expressed as $\Phi m = \Phi(w_C) + 180$ where $\Phi(w_C)$ is the open loop phase shift at the frequency w_C
- **SSB phase noise or close in noise**: It is the noise level within the loop bandwidth relative to carrier at a given frequency offset. It is referred to a 1Hz bandwidth. It is expressed in dBc/Hz.
- **Integrated phase jitter or residual FM**: this is another measure of the noise performance of a signal source. This measure of integrated noise is usually specified over a particular audio bandwidth, e.g., 10 Hz to 200 kHz. It is expressed in degrees rms. An ideal synthesizer would have zero integrated phase jitter.
- **Spurious**: this defines the spectral purity of the oscillator. Common sources of spurious are the comparison frequency and harmonies. Comparison frequency breakthrough is generated by leakage in the loop filter components or the charge pump.
- **Settling time or switching time**: this indicates the time for a given frequency jump to be within a specified distance (frequency or phase) from target value.

5.2 Appendix B: Basic PLL Transfer Function

Figure 5–1 shows the block diagram of a basic control loop.

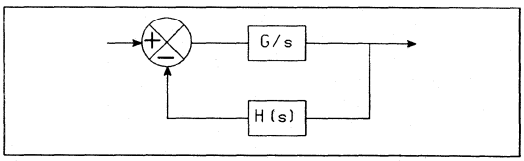


Figure 5–1. Block Diagram of a Loop

In open loop, the transfer function is

$$H(s) \cdot G(s) \quad \text{(a)}$$

In closed loop, the transfer function is

$$\frac{G(s)}{1 + G(s) \cdot H(s)} \quad \text{(b)}$$

If we apply these transfer functions to the Phase Locked Loop in Figure 5–2 with equations expressed in Laplace notation

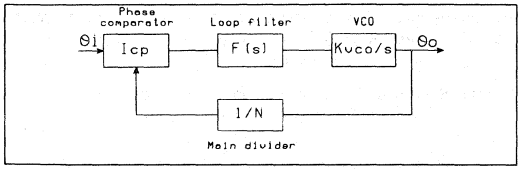


Figure 5–2. Block Diagram of a Phase Locked Loop

$$G(s) = \frac{I_{CP} \cdot K_{VCO} \cdot F(s)}{s} \quad (c)$$

$$H(s) = \frac{1}{N} \quad (d)$$

The PLL open loop transfer function is

$$\frac{I^{CP} \cdot K_{VCO} \cdot F(s)}{s \cdot N} \quad (e)$$

The PLL closed loop transfer function is

$$\frac{\Phi o(s)}{\Phi(s)} \frac{K_{VCO} \cdot I_{CP} \cdot F(s)/s}{1 + (K_{VCO} \cdot I_{CP} \cdot F(s)/s \cdot N)}$$

$$= \frac{N \cdot K_{VCO} \cdot I_{CP} \cdot F(s)}{(s \cdot N) + (K_{VCO} \cdot I_{CP} \cdot F(s)} \quad (f)$$

Basic performance of PLL is determined by R_2 and C_2 (see Figure 3–2) in the loop filter.

Note: when introducing more components in the loop filter, the expression for the transfer function becomes a lot more complicated. Anyway, this design can serve as a starting point for even more complicated filters.

The transfer function of this simple loop filter is

$$F(s) = R_2 + \left(\frac{1}{s \cdot C_2}\right) = \left(\frac{(s \cdot R_2 \cdot C_2) + 1}{(s \cdot C_2)}\right) \quad (g)$$

Then, the closed loop transfer function is

$$\frac{\Phi o(s)}{\Phi i(s)} = \frac{N \cdot K_{VCO} \cdot I_{CP} \cdot F(s)}{s \cdot N + K_{VCO} \cdot I_{CP} \cdot F(s)} =$$

$$\frac{N \cdot K_{VCO} \cdot I_{CP}(s \cdot R_2 \cdot C_2 + 1)/s \cdot C_2}{s \cdot N + K_{VCO} \cdot I_{CP}(s \cdot R_2 \cdot C_2 + 1)/s \cdot C_2} =$$

$$\frac{N(s \cdot R_2 \cdot C_2 + 1)}{\frac{s^2 (C_2 \cdot N)}{(K_{VCO} \cdot I_{CP})} + (s \cdot R_2 \cdot C_2 + 1} \quad (h)$$

If we compare the denominator of (h) with

$$\frac{s^2}{w_n^2} + \frac{2 \cdot \rho \cdot s}{W_n} + 1$$

we find the equations shown below:

$$w_n = \left(\frac{K_{VCO} \cdot I_{CP}}{C_2 \cdot N}\right)^{1/2} \quad (i) \rightarrow (1)$$

$$\rho = \frac{w_n (R_2 \cdot C_2)}{2} \quad (j)$$

$$R_2 = 2 \cdot \rho \left(\frac{N}{K_{VCO} \cdot I_{CP} \cdot C_2}\right)^{1/2} \quad (k) \rightarrow (2)$$

5.3 APPENDIX C: DEMONSTRATION BOARD DOCUMENTATION

Table 5–1 Parts List for UMA1018M/UMA1020M Demonstration Board (GSM/DCS1800)

Reference	Value / Type	Size	Reference	Value / Type	Size
R1	560kΩ	0805 SMD	C1	33pF	0805 SMD
R2	560kΩ	0805 SMD	C2	33pF	0805 SMD
R3	560kΩ	0805 SMD	C3	33pF	0805 SMD
R4	12kΩ	0805 SMD	C4	56pF	0805 SMD
R5	56Ω	0805 SMD	C5	56pF	0805 SMD
R6	18Ω	0805 SMD	C6	560pF	0805 SMD
R7	18Ω	0805 SMD	C7	100pF	1206 SMD
R8	12Ω	0805 SMD	C8	47µ / 25V	Alu 5x11
R9	12Ω	0805 SMD	C9	470pF	0805 SMD
R10	18kΩ	0805 SMD	C10	10nF	0805 SMD
R11	39kΩ	0805 SMD	C11	100pF	0805 SMD
R12	12Ω	0805 SMD	C12	100nF	1206 SMD
R13	100kΩ	0805 SMD	C13	–	
R14	3k9	0805 SMD	C14	100pF (820pF)	0805 SMD
R15	100kΩ	0805 SMD	C15	–	0805 SMD
R16	–		C16	1.5nF (12n//1n)	0805 SMD
R17	–(12)	0805 SMD	C17	22pF (180pF)	0805 SMD
R18	0	0805 SMD	C18	100nF	1206 SMD
R19	47kΩ (5k6)	0805 SMD	C19	100nF	1206 SMD
R20	100kΩ (15kΩ)	0805 SMD	C20	56pF	0805 SMD
R21	12kΩ	0805 SMD	C21	56pF	0805 SMD
R22	12kΩ	0805 SMD	C22	100nF (–)	1206 SMD
R23	56Ω	0805 SMD	C23	47µ / 25V	Alu 5x11
R24	18Ω	0805 SMD	C24	1nF	0805 SMD
R25	18Ω	0805 SMD	C25	10nF	0805 SMD
R26	18Ω	0805 SMD	C26	22nF	0805 SMD
R27	12 (–)	0805 SMD	C27	100nF	1206 SMD
R28	100kΩ	0805 SMD	C28	100nF	1206 SMD
R29	22kΩ	0805 SMD	C29	100nF	1206 SMD
R30	1k8	0805 SMD	C30	1µ / 63V	Alu 5x11
R31	1k2	0805 SMD	C31	–(100nF)	1206 SMD
R32	–	0805 SMD	D1	LED	
R33	12	0805 SMD	L1	4.77nF	1008CT
R34	–(12)	0805 SMD	78L05		T092
VCO1	MQC505-902	MURATA	LM317LZ		T092
VCO2	(URAE8x542A)	ALPS	FXTLIN	PN-Minicoax-Bus SMB	
VCO3	Aux. VCO		RF_PRI	PN-Minicoax-Bus SMA	
VTCX01	13MHz	B8 Philips	RF_AUX	PN-Minicoax-Bus SMB	
VCTX02	13MHz	B9 Philips			

NOTE: All values in between brackets ( ) are related to 1800MHz application.

J1 Controls power down auxiliary synthesizer
J2 Activates the FAST charge pump
J3 Controls power down principal synthesizer
J4 Enables DAC output
J5 Selects VTCXO or external reference frequency
J6 Selects 3V, 5V or external variable voltage
J7 Disconnects the auxiliary VCO
X1 3-Wire bus control
X2, X4 Supply
X3 Modulation

Table 5–2 Parts List for Interface Card and Auxiliary VCO

Reference	Value / Type	Size	Reference	Value / Type	Size
Components for the Auxiliary VCO 100 MHz					
Rf1	27Ω	0805 SMD	Cf1	1pF	0805 SMD
Rf2	150Ω	0805 SMD	Cf2	27pF	0805 SMD
Rf3	1kΩ	0805 SMD	Cf3	68pF	0805 SMD
Rf4	820Ω	0805 SMD	Cf4	–	0805 SMD
Rf5	1kΩ	0805 SMD	Cf5	22pF	0805 SMD
Rf6	1kΩ	0805 SMD	Cf6	33nF//22pF	0805 SMD
Rf7	10kΩ	0805 SMD	Cf7	3p3	0805 SMD
Rf8	100Ω	0805 SMD	Cf8	3p9	0805 SMD
Rf9	270Ω	0805 SMD	Cf9	10pF	0805 SMD
Rf10	82Ω	0805 SMD	Cf10	15pF	0805 SMD
Lf1	120nF	0805 SMD	Cf11	1pF	0805 SMD
Lf2	180nF	0805 SMD	Cf12	8n2	0805 SMD
CVf1	BBY31	SOT-23	Tf1	BFT92	SOT-23
			Tf2	BFR92	SOT-23
Components for PC Interface Card					
R1	10kΩ	0805 SMD	C1	100nF	1206 SMD
R2	10kΩ	0805 SMD	iC1	74HC04	
R3	10kΩ	0805 SMD	J1	Sub D 25 pins	
R4	330Ω	0805 SMD	X1	6 pins	
R5	330Ω	0805 SMD			
R6	330Ω	0805 SMD			

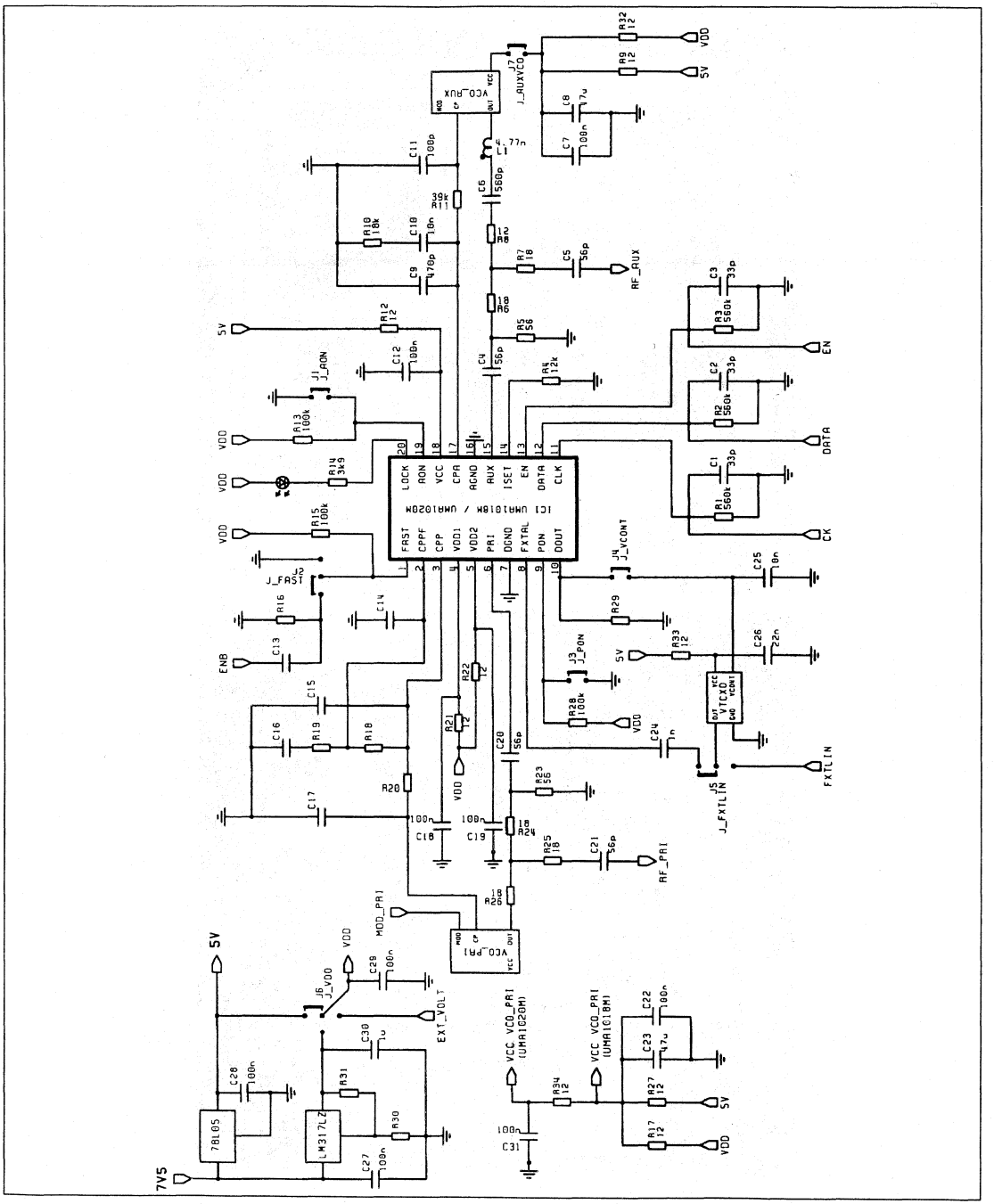


Figure 5–3. Demonstration Board Circuit Diagram

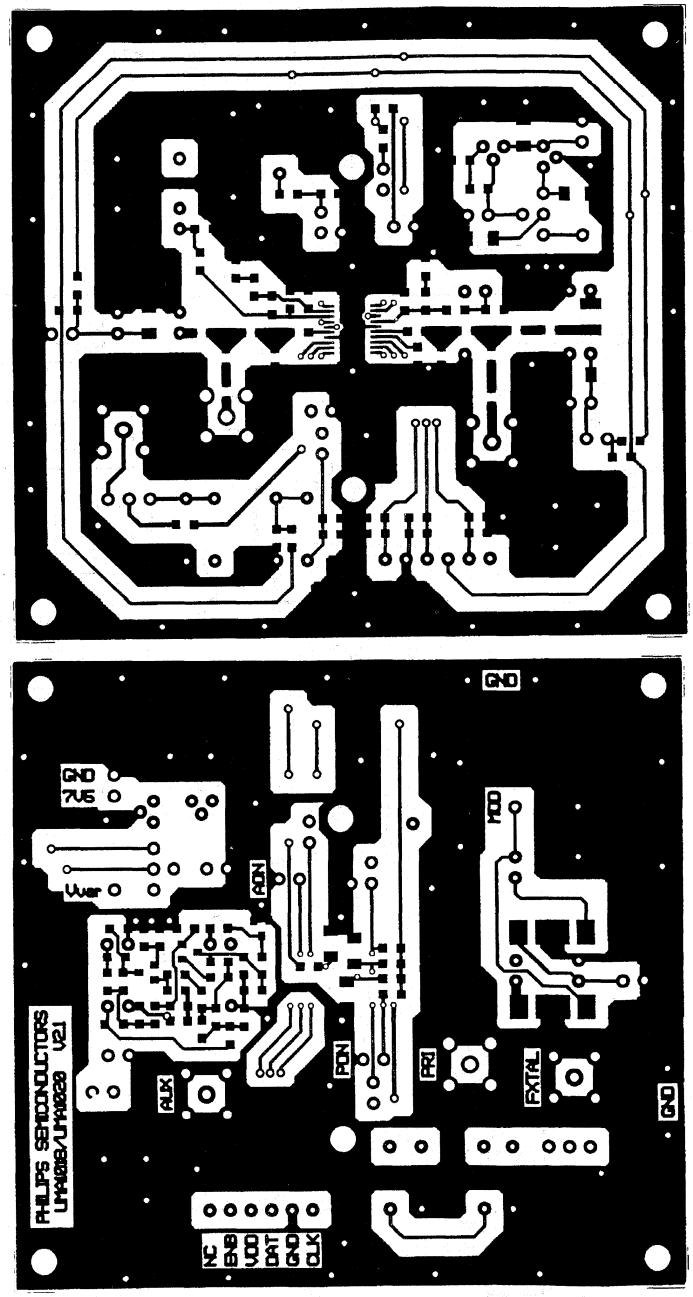


Figure 5–4. Demonstration Board PCB Layout

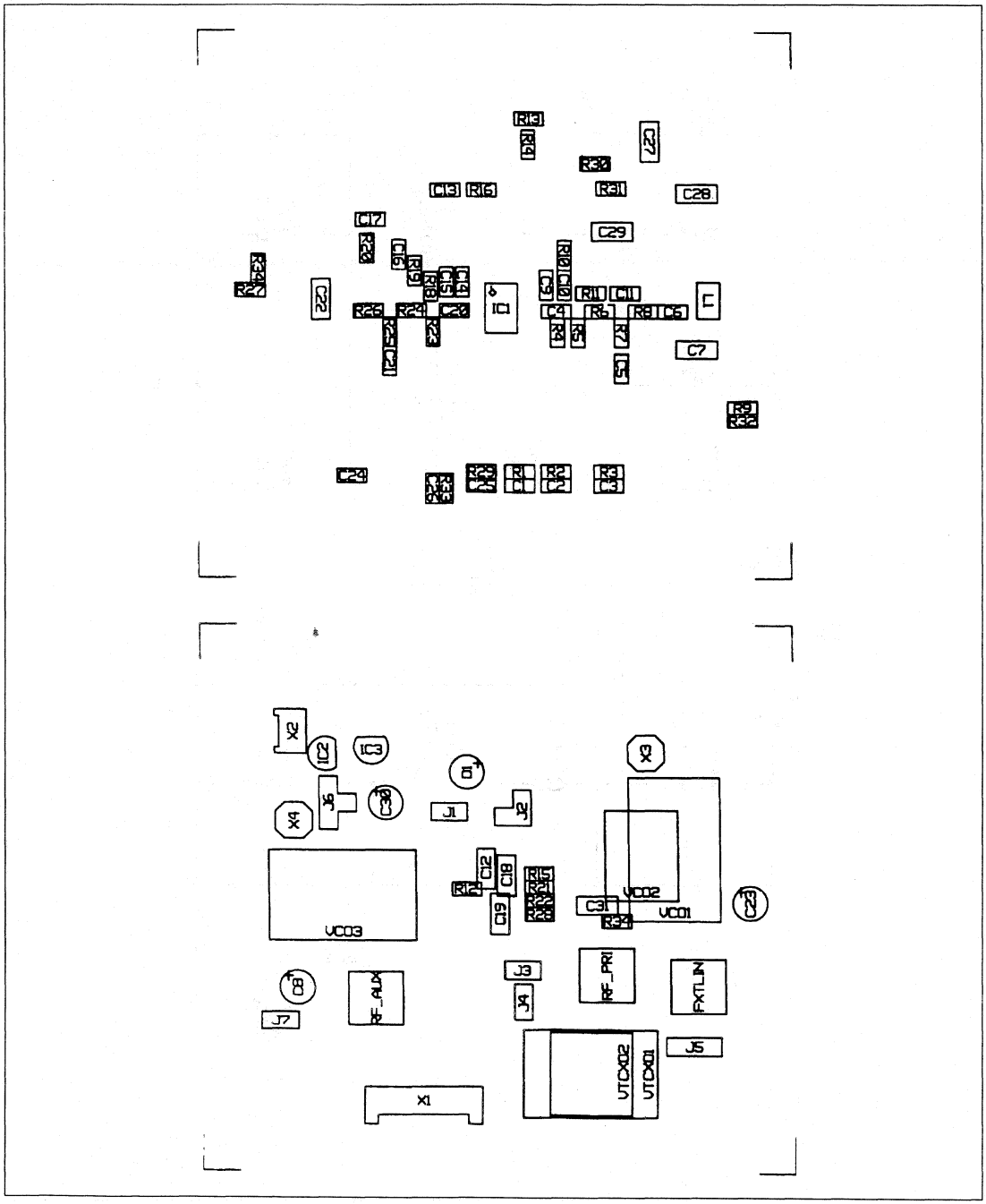


Figure 5–5. Demonstration Board Placement of Components

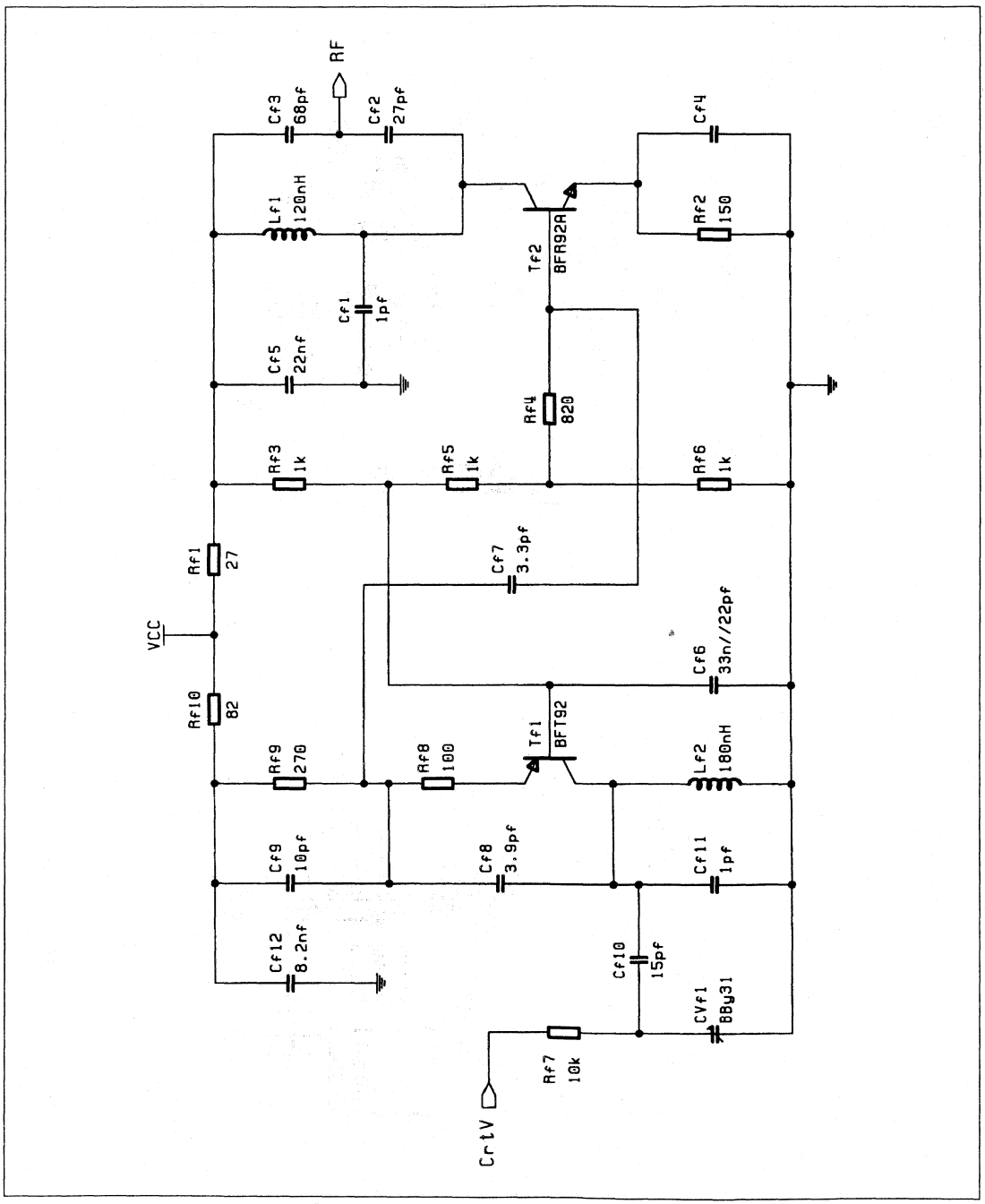


Figure 5–6. Auxiliary 100MHz VCO Circuit Diagram

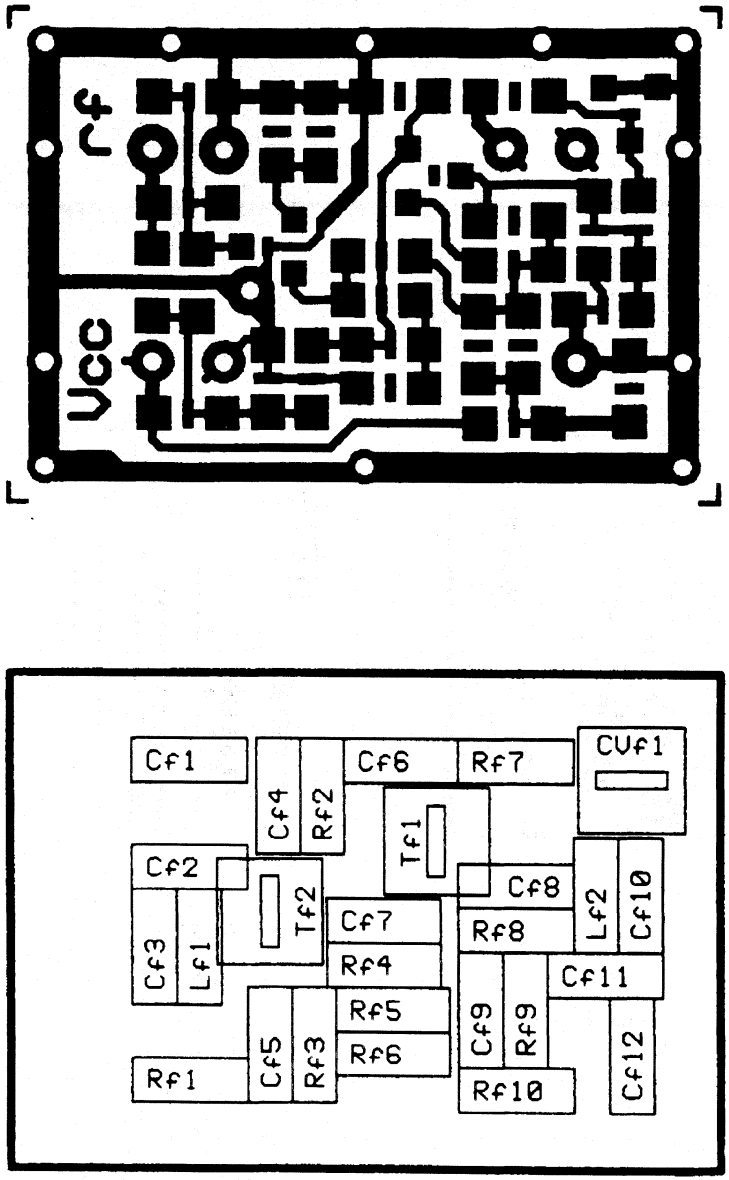


Figure 5–7. Auxiliary 100MHz VCO PCB Layout and Placement of Components

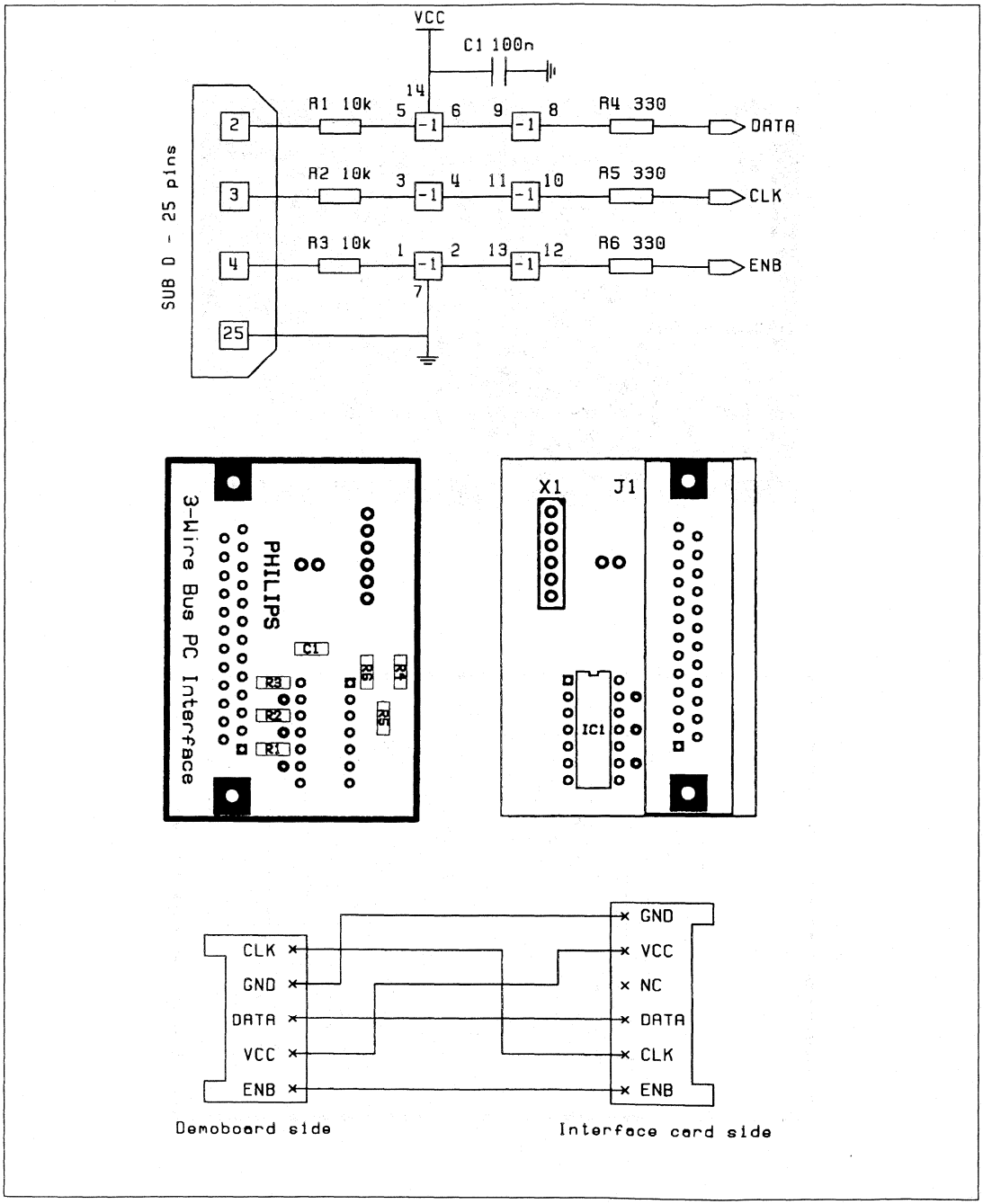


Figure 5–8. Interface Card PCB Layout and Cable Connection

6. FREQUENTLY ASKED QUESTIONS

Q. How can the noise be improved?

A. Five things can be done to improve the noise:

1. Increase the f_{XTAL} level (within specification limits).
2. Use a higher crystal frequency. Doubling the reference frequency improves the close in noise by 3dBc/Hz.
3. Use only one charge pump (CPP or CPPF). The dynamic gain is more constant with supply voltage, frequency and temperature.
4. Use a narrower loop filter. But this increases the switching time.
5. Ensure that supply is well decoupled.

Number 4 does not improve the close in noise, just the phase noise. Other points can improve the close in noise and so, the total phase noise of the PLL.

Q. What is the phase detector gain? Is it charge pump output current divided by 2π or just the charge pump output current, itself?

A. The phase detector gain is equal to the charge pump output current I_{CP} divided by 2π since the phase detector covers 2π range. However, when using the design formulas, the phase detector gain can be replaced directly by I_{CP} because the 2π factor will be cancelled out by the 2π also in the VCO gain.

Q. What kind of main capacitor should be used in the loop filter?

A. Higher leakage current raises comparison frequency breakthrough and the 'memory effect' of higher dielectric capacitor degrades the settling time, Z5U, X7R series and electrolytic capacitors are not used. A polyester film capacitor is generally used with main capacitor of the loop filter.

Q. How to use the synthesizer with $V_{DD} < 4.5$ V whereas DATA, CLK and $\overline{E}$ arc at 5 V logic?

A. Because of protection against electrostatic discharges, the input voltage for these logic pins can not be greater than $V_{DD} + 0.3$ V. An interface between the microcontroller and the synthesizer is then needed to reduce voltage at serial bus pins. A voltage divider using two resistors is a simple and cheap solution to implement. The design of this interface involves performance compromise between the current consumption and the programming speed, which depend on the resistor values in the voltage divider and the parasitic capacitance from the demonstration board. A Technical Marketing Report (TMT94008) describes some measurement results. For different values of $V_{DD} < 4.5$ V, the current consumption and the programming speed are given.

Q. Open loop modulation?

A. Two methods of open loop modulation are briefly described. A complete report "UMA1020M Modulation Capability for DECT" (TMT250894) is available.

Method 1: only the principal fast charge pump is used, and it is enabled/disabled using the pin FAST. The principal charge pump (pin CPP) is grounded. An internal circuit synchronizes the FAST signal with the fast charge pump correction current pulses. This avoids opening the loop when the fast charge pump is still active, which would cause a frequency drift. After the loop is opened, the UMA1020M (or UMA1018M) principal synthesizer can then be powered down to reduce consumption. Some precautions must be taken when the principal fast charge pump is switched off.

Method 2: the loop is opened by powering down (PON pin) the principal synthesizer directly. The signal sent to the PON is externally synchronized with the charge pumps to avoid powering down the synthesizer while they are still active.

Two problems can occur when a synthesizer is powered down:

The first is known as "load pulling". When the synthesizer is switched off, its RF input impedance may change and then an unintended jump in frequency is possible if the VCO is susceptible to load changes. This problem is negligible with the UMA10XX synthesizers, a frequency drift of less than 2kHz has been observed with the UMA1020M in a typical DECT application.

The second problem is called "pushing". The frequency of the VCO moves with changes in its supply voltage. When the principal synthesizer is powered down, it may temporally affect the supply voltage. Two separate voltage supplies (one for the synthesizer, the other for the VCO) will eliminate frequency shift due to "pushing". Alternatively, if using only one voltage supply, proper supply decoupling will attenuate.

7. REFERENCES

1. Product specification UMA1018M, Philips Semiconductors, 27 June 1995.
2. Product specification UMA1020M, Philips Semiconductors, 15 June 1995.
3. Product specification UMA1020AM, Philips Semiconductors, 06 July 1995.
4. Product specification UMA1017M, Philips Semiconductors, 10 July 1995.
5. Product specification UMA1019M, Philips Semiconductors, 07 July 1995.
6. Product specification UMA1019AM, Philips Semiconductors, 07 July 1995.
7. Gardner, Floyd M., PhaseLock Techniques, 2nd ed., Wiley, New York, 1980.
8. Rohde, Ulrich L., Digital PLL Frequency Synthesizers, Theory and Design, Prentice–Hall, Englewood Cliffs, New Jersey 1983.

Low-voltage frequency synthesizer for radio telephones

UMA1021M

FEATURES

- Low phase noise
- Low current from 3 V supply
- Fully programmable main divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual charge pump outputs
- Hard and soft power-down control.

APPLICATIONS

- 900 MHz and 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1021M BICMOS device integrates a prescaler, programmable dividers, and a phase comparator to implement a phase-locked loop.

The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at RF input frequencies up to 2.2 GHz, with a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog (charge-pump) and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential (V_{DD}). V_{CC} must be equal to or greater than V_{DD} (e.g. V_{DD} = 3 V and V_{CC} = 5 V for wider VCO control voltage range).

The phase detector has two charge-pump outputs, CP and CPF, the latter of which is enabled directly at pin FAST. This permits the design of adaptive loops. The charge pump currents (phase detector gain) are fixed by an external resistance at pin I_{SET} and via the serial interface. Only a passive loop filter is necessary; the charge pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$; $V_{CC} \geq V_{DD}$	2.7	–	5.5	V
V_{CC}	charge-pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{DD} + I_{CC}$	supply current		–	10	–	mA
$I_{CC(pd)} + I_{DD(pd)}$	total supply current in power-down mode		–	5	–	μA
f_{RF}	RF input frequency		300	–	2200	MHz
f_{xtal}	crystal reference input frequency		3	–	35	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1021M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

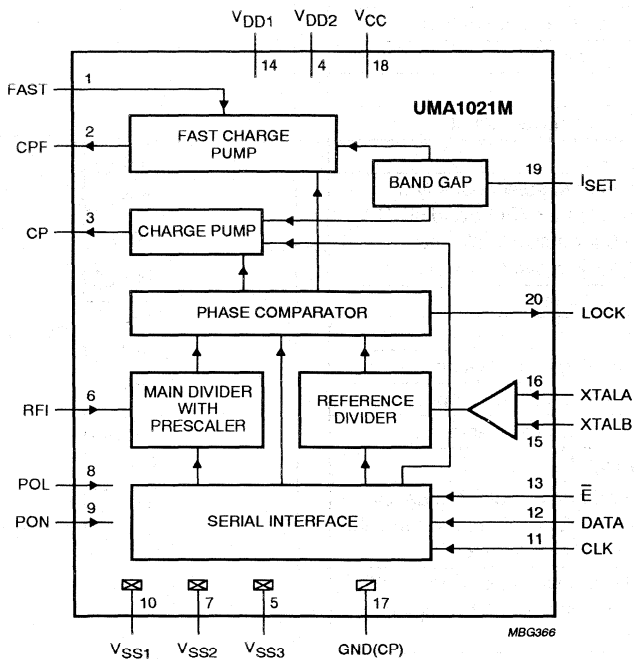


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	enable input for fast charge-pump output CPF
CPF	2	fast charge-pump output
CP	3	normal charge-pump output
V_{DD2}	4	power supply 2
V_{SS3}	5	ground 3
RFI	6	2 GHz main divider input
V_{SS2}	7	ground 2
POL	8	digital input to select polarity of power-on inputs (PON and sPON): POL = 0 for active LOW and POL = 1 for active HIGH
PON	9	power-on input
V_{SS1}	10	ground 1
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input
V_{DD1}	14	power supply 1
XTALB	15	complementary crystal frequency input from TCXO; if not used should be decoupled to ground
XTALA	16	crystal frequency input from TCXO; if not used should be decoupled to ground
GND(CP)	17	ground for charge-pump
V_{CC}	18	supply for charge-pump
I_{SET}	19	external resistor from this pin to ground sets the charge-pump currents
LOCK	20	out-of-lock detector output

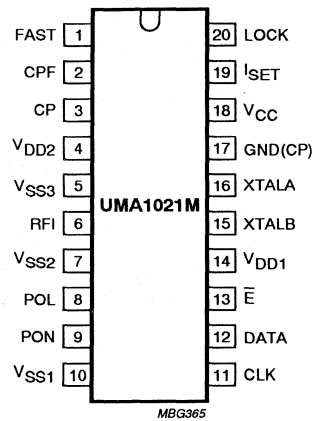


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main divider

The main divider is clocked at pin RFI by the RF signal which is AC-coupled from an external VCO. The divider operates with signal levels from 50 to 225 mV (RMS), and at frequencies from 300 MHz to 2.2 GHz. It consists of a fully programmable bipolar prescaler followed by a CMOS counter. Any divide ratios from 512 to 131 071 inclusive can be programmed.

Reference divider

The reference divider is clocked by the differential signal between pins XTALA and XTALB. If only one of these inputs is used, the other should be decoupled to ground. The applied input signal(s) should be AC-coupled. The circuit operates with levels from 50 up to 500 mV (RMS) and at frequencies from 3 to 35 MHz. Any divide ratios from 8 to 2047 inclusive can be programmed.

Phase detector

The phase detector is driven by the output edges of the main and reference dividers. It produces current pulses at pins CP and CPF whose amplitudes are programmed. The pulse duration is equal to the difference in time of arrival of the edges from the two dividers. If the main divider edge arrives first, CP and CPF sink current. If the reference divider edge arrives first, CP and CPF source current.

The currents at CP and CPF are programmed via the serial bus as multiples of a reference current set by an external resistor connected between pin I_{SET} and V_{SS} (see Table 3). CP remains active except in power-down. CPF is enabled via input pin FAST which is synchronized with respect to the phase detector to prevent output current pulses being interrupted. By appropriate connection to the loop filter, dual bandwidth loops can be designed; short time constant during frequency switching (FAST mode) to speed-up channel changes, and low bandwidth in the settled state to improve noise and breakthrough levels.

Additional circuitry is included to ensure that the gain of the phase detector remains linear even for small phase errors.

Out-of-lock detector

The out-of-lock detector is enabled (disabled) via the serial interface by setting bit OOL HIGH (LOW). An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μA. When the out-of-lock detector is enabled, LOCK is HIGH if the error at the phase detector input is less than approximately 25 ns, otherwise LOCK is LOW. If the out-of-lock detector is disabled, LOCK remains HIGH.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, clock (CLK) and enable ($\overline{E}$). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns HIGH.

During normal operation, $\overline{E}$ should be kept HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

When the synthesizer is powered-on, the presence of a TCXO signal at the reference divider input and a VCO signal at the main divider input is **required** for correct programming.

Data format

The leading bits (dt16 to dt0) make up the data field, while the trailing four bits (ad3 to ad0) are the address field. The UMA1021M uses 4 of the 16 available addresses. These are chosen for compatibility with other Philips Semiconductors radio telephone ICs. The data format is shown in Table 1. The first bit entered is dt16, the last bit is ad0. For the divider ratios, the first bits entered (PM16 and PR10) are the most significant (MSB).

The trailing address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To avoid erroneous divider ratios, the load pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.

The test register (address 0000) does not normally need to be programmed. However if it is programmed, all bits in the data field should be set to logic 0.

Power-down mode

The synthesizer is on when both the input signals PON and the programmed bit sPON are active. The 'active' level for these two signals is chosen at pin POL (see Table 2). When turned on, the dividers and phase detector are synchronized to avoid random phase errors. When turned off, the phase detector is synchronized to avoid interrupting charge-pump pulses. For synchronisation functions to work correctly on power-up or power-down (using either hardware or software programming), the presence of TCXO and VCO signals is required to drive the appropriate divider inputs. The UMA1021M has a very low current consumption in the power-down mode.

Table 1 Bit allocation; note 1

FIRST IN				REGISTER BIT ALLOCATION												LAST IN			
DATA FIELD																ADDRESS			
dt16	dt15	dt14	dt13	dt12	dt11	dt10	dt9	dt8	dt7	dt6	dt5	dt4	dt3	dt2	dt1	dt0	ad3	ad2	ad1	ad0
Test bits[2]																	0	0	0	0
X	X	X	X	OOL[3]	X	CR1	CR0	X	X	sPON[3]	X	X	X	X	X	X	0	0	0	1
PM16[4]	main divider coefficient															PM0	0	1	0	0
X	X	X	X	X	X	PR10[4]	reference divider coefficient									PR0	0	1	0	1

Notes

1. X = don't care.
2. The test register (address 0000) should not be programmed with any other values except all zeros for normal operation.
3. Bit sPON = software power-up for synthesizer (see Table 2); OOL = Out-Of-Lock (1 = enabled).
4. PM16 is the MSB of the main divider coefficient; PR10 is the MSB of the reference divider coefficient.

Table 2 Power-on programming

POL	PON	sPON	SYNTHESIZER STATE	COMPATIBILITY
0	0	0	on	UMA1019M/UMA1019AM
0	1	X	off	UMA1019M/UMA1019AM
0	X	1	off	UMA1019M/UMA1019AM
1	0	X	off	UMA1017M
1	X	0	off	UMA1017M
1	1	1	on	UMA1017M

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$2 \times I_{SET}$	$8 \times I_{SET}$	4 : 1
0	1	$2 \times I_{SET}$	$16 \times I_{SET}$	8 : 1
1	0	$1 \times I_{SET}$	$12 \times I_{SET}$	12 : 1
1	1	$1 \times I_{SET}$	$16 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{SET}}{R_{SET}}$; reference current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	charge-pump supply voltage	−0.3	+5.5	V
$V_{CC} - V_{DD}$	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 6, 8, 9 and 11 to 13	−0.3	V_{DD} + 0.3	V
	voltage at pins 1, 2, 3, 15, 16, 19 and 20	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between any of GND(CP), V_{SS1}, V_{SS2}, and V_{SS3} (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
$T_{j(max)}$	maximum junction temperature	–	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. This device meets class 2 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; $V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25$ °C; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 14 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$; $V_{CC} \geq V_{DD}$	2.7	–	5.5	V
V_{CC}	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{DD1} + I_{DD2}$	synthesizer digital supply current	$V_{DD} = 5.5$ V	–	7	9.5	mA
I_{CC}	charge pump supply current	$V_{CC} = 5.5$ V; $R_{SET} = 5.6$ kΩ	–	3	3.8	mA
$I_{CC(pd)} + I_{DD(pd)}$	total supply current in power-down mode	logic levels 0 V or V_{DD}	–	5	50	μA
RF main divider input; pin 6						
f_{RF}	RF input frequency		300	–	2200	MHz
$V_{RF(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω	50	–	225	mV
R_m	main divider ratio		512	–	131071	
Z_i	input impedance (real part)	$f_{RF} = 1$ GHz	–	1	–	kΩ
		$f_{RF} = 2$ GHz	–	60	–	Ω
C_i	typical pin input capacitance	$f_{RF} = 1$ GHz	–	1	–	pF
		$f_{RF} = 2$ GHz	–	1	–	pF
Synthesizer reference divider input; pins 15 and 16						
f_{xtal}	crystal reference input frequency		3	–	35	MHz
$V_{xtal(rms)}$	sinusoidal input signal level between pins 15 and 16 (RMS value)		50	–	500	mV
R_{ref}	reference division ratio		8		2047	
Z_i	input impedance (real part)	$f_{xtal} = 13$ MHz	–	10	–	kΩ
C_i	typical pin input capacitance	$f_{xtal} = 13$ MHz	–	1.5	–	pF
Phase detector						
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
Charge pump current setting resistor input; pin 19						
R_{SET}	external resistor connected between pin 19 and ground		5.6	–	12	kΩ
V_{SET}	regulated voltage at pin 19	$R_{SET} = 5.6$ kΩ	–	1.2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump outputs; pins 2 and 3; R_{SET} = 5.6 kΩ						
$I_{ocp(err)}$	charge pump output current error		−25	−	+25	%
I_{match}	sink-to-source current matching		−	±5	−	%
I_{LIcp}	charge pump off leakage current	$V_{CP/CPF} = \frac{1}{2}V_{CC}$	−5	±1	+5	nA
$V_{CP/CPF}$	charge pump voltage compliance		0.4	−	$V_{CC} - 0.4$	V
Phase noise						
N_{900}	synthesizer's contribution to close-in phase noise of 900 MHz RF signal at 1 kHz offset (GSM)	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	−	−88	−	dBc/Hz
N_{1800}	synthesizer's contribution to close-in phase noise of 1.8 GHz RF signal at 1 kHz offset (DCS1 800)	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	−	−82	−	dBc/Hz
Interface logic input signal levels; pins 1, 8, 9, 11, 12 and 13						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		−0.3	−	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	−5	−	+5	μA
C_i	input capacitance		−	2	−	pF
Lock detect output signal; pin 20; open-drain output						
V_{OL}	LOW level output voltage	I_{sink} < 0.4 mA	−	−	0.4	V
t_{OOL}	phase error threshold for out-of-lock detector		−	25	−	ns

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
$t_{W(min)}$	minimum inactive pulse width	4000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width ($t_{W(min)}$) can be smaller than 4 μs provided all the following conditions are fulfilled:

   a) Main divider input frequency $f_{RF} > \frac{447}{t_{W(min)}}$.

   b) Reference divider input frequency $f_{xtal} > \frac{3}{t_{W(min)}}$.

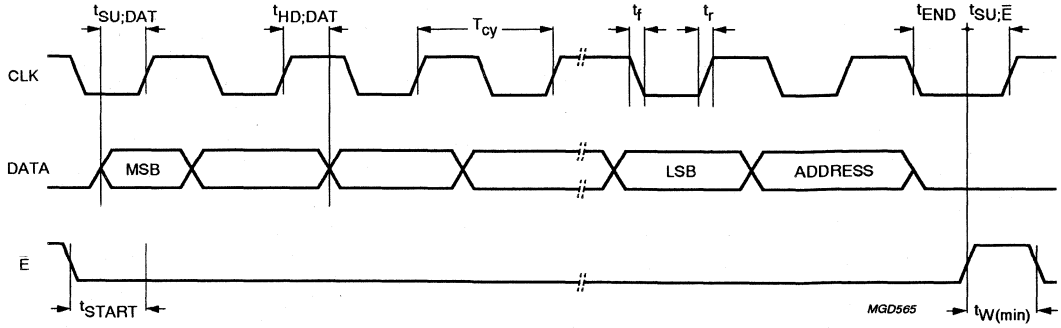


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

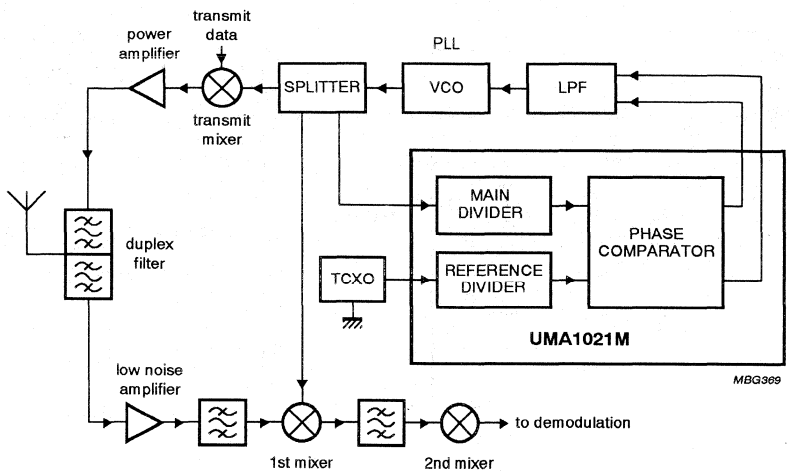
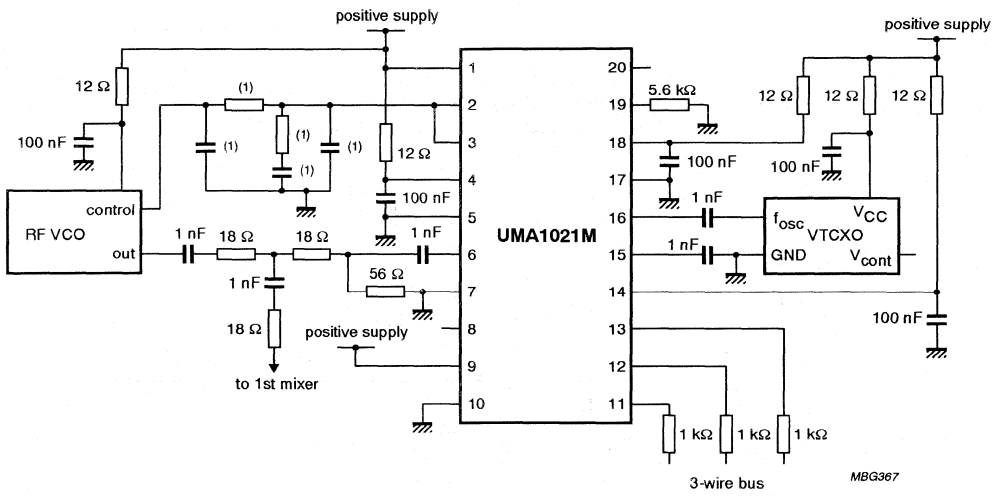


Fig.4 Typical application block diagram.



(1) Values depend on application.

Fig.5 Typical test and application diagram.

Low cost dual frequency synthesizer for radio telephones

UMA1022M

FEATURES

- Low phase noise
- Low current from 3 V supply
- Fully programmable dividers
- 3-line serial interface bus
- Input reference buffer configurable as an oscillator with external crystal resonator
- Wide compliance voltage charge pump outputs
- Two power-down input control pins.

APPLICATIONS

- 900 MHz and 2 GHz digital radio telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1022M BICMOS device integrates prescalers, programmable dividers, a crystal oscillator/buffer and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd or a single LiIon cell in pocket phones, or from an external 3 V supply.

The synthesizers operate at RF input frequencies up to 2.2 GHz and 500 MHz. All divider ratios are supplied via a 3-wire serial programming bus. The reference divider uses a common, fully programmable part and a separate subdivider section. In this way the comparison frequencies are related to each other allowing optimum isolation between charge pump pulses.

Separate power and ground pins are provided to the analog (charge pump, prescaler) and digital (CMOS) circuits. An independent supply for the crystal oscillator section allows maximum frequency stability. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD} and V_{DDX} must be at the same potential. V_{CCA} and V_{CCB} must be equal to each other and equal to or greater than V_{DD} (e.g. V_{DD} = 3 V and V_{CCA} = 5 V for wider VCO control voltage range).

The charge pump currents (phase detector gain) are fixed by internal resistances and controlled by the serial interface. Only passive loop filters are necessary; the charge pumps function within a wide voltage compliance range to improve the overall system performance.

Suitable pin layout is chosen to minimize coupling and interference between signals entering or leaving the chip.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1022M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

Low cost dual frequency synthesizer for radio telephones

UMA1022M

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	V_{CCA} and $V_{CCB} \geq V_{DD}$	2.7	–	5.5	V
V_{CCA}, V_{CCB}	analog supply voltages	V_{CCA} and $V_{CCB} \geq V_{DD}$	2.7	–	5.5	V
V_{DDX}	crystal reference supply voltage	$V_{DDX} = V_{DD}$	2.7	–	5.5	V
I_{tot}	all supply currents ($I_{DD} + I_{CCA} + I_{CCB} + I_{DDX}$) in active mode	$V_{CCA} = V_{CCB} = 3.0$ V; $V_{DDX} = V_{DD} = 3.0$ V; XON = 1; crystal oscillator active	–	13	–	mA
$I_{tot(pd)}$	total supply currents in power-down mode		–	30	–	μA
f_{RF}	RF input frequency		300	–	2200	MHz
f_{IF}	IF input frequency		50	–	500	MHz
f_{xtal}	crystal reference oscillator frequency		3	–	30	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

BLOCK DIAGRAM

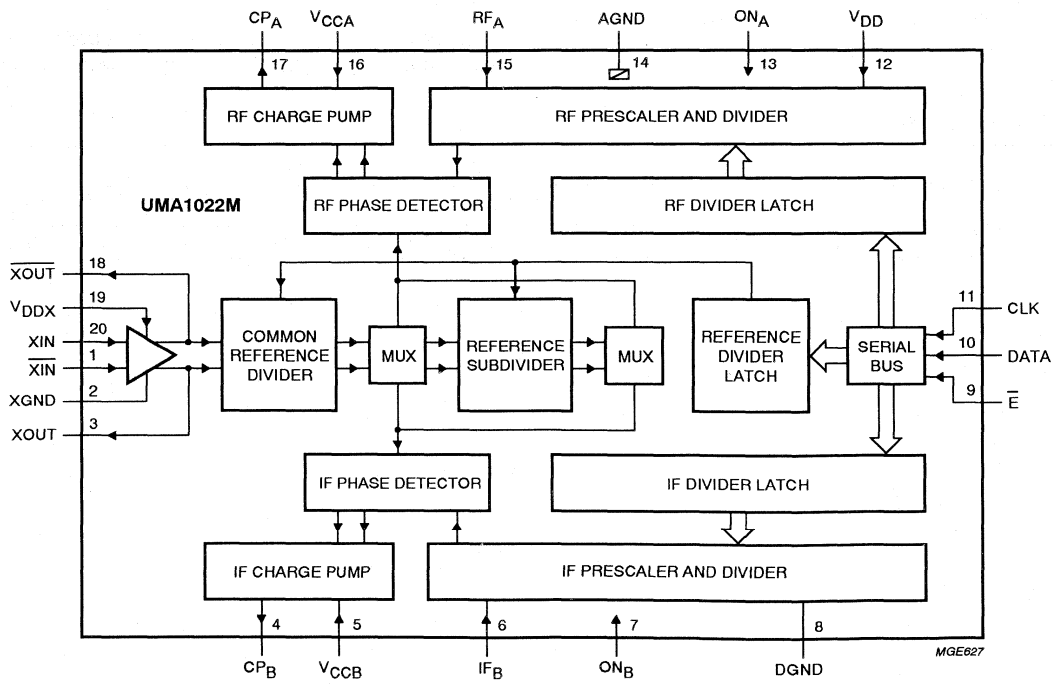


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{XIN}$	1	inverting crystal reference input
XGND	2	ground for crystal oscillator circuits
XOUT	3	crystal oscillator buffer output
CP_B	4	IF synthesizer charge pump output
V_{CCB}	5	analog supply to IF synthesizer
IF_B	6	IF VCO main divider input
ON_B	7	IF power-on input; ON_B = HIGH means IF PLL is active
DGND	8	digital circuits ground
$\overline{E}$	9	programming bus enable input
DATA	10	programming bus data input
CLK	11	programming bus clock input
V_{DD}	12	digital circuits supply voltage
ON_A	13	RF power-on input; ON_A = HIGH means RF PLL is active
AGND	14	analog circuits ground
RF_A	15	RF VCO main divider input
V_{CCA}	16	analog supply to RF synthesizer
CP_A	17	RF synthesizer charge pump output
$\overline{XOUT}$	18	inverting oscillator buffer output
V_{DDX}	19	supply voltage to crystal oscillator circuits
XIN	20	non-inverting crystal reference input

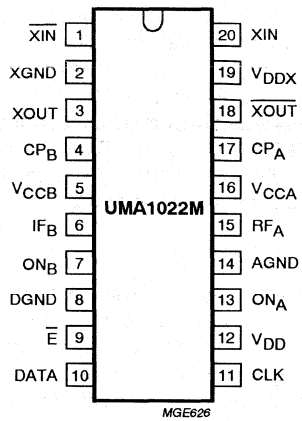


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main dividers

The main dividers are clocked at pin RF_A by the RF oscillator signal and at pin IF_B by the IF oscillator signal. The inputs are AC coupled through external capacitors. Input impedances are high, dominated by parasitic package capacitances, so matching is off-chip.
The sensitive dividers operate with signal levels from 35 to 225 mV (RMS), at frequencies from 300 MHz to 2.2 GHz (RF part) and from 50 to 500 MHz (IF part). Both include programmable bipolar prescalers followed by CMOS counters. The RF main divider allows programmable ratios from 512 to 65535; the IF blocks accept values between 128 and 16383.

Crystal oscillator

A fully differential low-noise amplifier/buffer is integrated providing outputs to drive other circuits, and to build a crystal oscillator; only needed are an external resonance circuit and tuning elements (temperature compensation). A bus controlled power-down mode disables the low-noise amplifier to reduce current if not needed.

The normal differential input pins drive a clock buffer to provide edges to the programmable reference divider at frequencies up to 30 MHz. The inputs are AC coupled through external capacitors, and operate with signals down to 35 mV (RMS) and up to 0.5 V (RMS).

Various crystal oscillator structures can be built using the amplifier. By coupling one output back to the appropriate input through the resonator, and decoupling the other input to ground, the second output becomes available to deliver the reference frequency to other circuits.

Reference dividers

A first common divider circuit produces an output frequency for RF or IF synthesizer phase comparison, depending on the P/A bit. It drives a second independent divider, which delivers the reference edge to the IF or RF synthesizer phase comparator. When P/A is logic 1, the output of the subdivider is connected to the RF phase comparator, whereas the output of the common divider is connected to the IF phase detector.

The phase comparators run at related frequencies with a controlled phase difference to avoid interference when in-lock. The common 10-bit section permits divide ratios from 8 to 1023; the second subdivider allows phase comparison frequency ratios between 1 and 16. Table 2 indicates how to program the corresponding bits to get the wanted ratio.

Phase comparators

The phase detectors are driven by the output edges selected by the main and reference dividers.
Each generates lead and lag signals to control the appropriate charge pump. The pumps output current pulses appear at pins CP_A (RF synthesizer) and CP_B (IF synthesizer). The current pulse duration is at least equal to the difference in time of arrival of the edges from the two dividers. If the main divider edge arrives first, CP_A or CP_B sink current. If the reference divider edge arrives first, CP_A or CP_B source current. For correct PLL operation the VCOs need to have a positive frequency/voltage control slope.

The currents at CP_A and CP_B are programmed via the serial bus as multiples of an internally-set reference current. The passage into power-down mode is synchronized with respect to the phase detector to prevent output current pulses being interrupted. Additional circuitry is included to ensure that the gain of the phase comparators remains linear even for small phase errors.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, clock (CLK) and enable ($\overline{E}$). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns HIGH. During normal operation, $\overline{E}$ should be kept HIGH. Only the last 19 bits serially clocked into the device are retained within the programming register.

Additional leading bits are ignored, and no check is made on the number of clock pulses. The NMOS-rich design uses virtually no current when the bus is inactive; power-up is initiated when enable is taken LOW, and power-down occurs a short time after enable returns HIGH. Bus activity is allowed when either synthesizer is active or in power-down (ON_A and ON_B inputs LOW) mode. Fully static CMOS registers retain programmed data whatever the power-down state, as long as the supply voltage is present.

Data format

The leading bits (dt15 to dt0) make up the data field, while the trailing three bits (ad2 to ad0) comprise an address field. The UMA1022M uses 4 of the 8 available addresses. The data format is shown in Table 1. The first bit entered is dt15, the last bit is ad0. For the divider ratios, the first bits entered (P0 and R0) are the Least Significant Bits (LSB). **This is different from previous Philips synthesizers.**

The trailing address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To avoid erroneous divider ratios, the load pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.

The test register bits should not normally be programmed active (HIGH); normal operation requires them set LOW. When the supply voltage is established an internal power-up initialization pulse is generated to preconfigure the circuit state. Production testing does not verify that all bits are preconfigured correctly.

Power-down mode

The RF and IF synthesizers are **on** when respectively the input signal ON_A and ON_B are HIGH. When turned **on**, the dividers and phase detector are synchronized to avoid random phase errors. When turned **off**, the phase detector is synchronized to avoid interrupting charge pump pulses. The UMA1022M has a very low current consumption in the power-down mode.

Table 1 Bit allocation; note 1

FIRST IN				REGISTER BIT ALLOCATION												LAST IN		
DATA FIELD																ADDRESS		
dt15	**dt14**	**dt13**	**dt12**	**dt11**	**dt10**	**dt9**	**dt8**	**dt7**	**dt6**	**dt5**	**dt4**	**dt3**	**dt2**	**dt1**	**dt0**	**ad2**	**ad1**	**ad0**
Test bits[2]				CPI	S/D	XON[3]	X	X	X	X	P/A[4]	REFDIV2[5]				0	1	1
P0[6]	RF synthesizer main divider coefficient														P15	0	0	0
X	X	X	X	X	X	R0[6]	reference divider coefficient								R9	0	0	1
X	X	A0[6]	IF synthesizer main divider coefficient												A14	0	1	0

Notes

1. X = don't care.
2. The test bits (at address 011) should not be programmed with any other value except all zeros for normal operation.
3. Bit XON = power-on of crystal oscillator low-noise amplifier; logic 1 turns **on** circuit block.
4. Bit P/A = 1 selects the output of the reference subdivider to the RF synthesizer and the output of the common reference divider to the IF synthesizer.
5. The coefficient REFDIV2 (4 bits) selects the phase comparison ratio (1 to 16) between IF and RF synthesizers (see Table 2).
6. P0 is the LSB of the RF main divider coefficient; R0 is the LSB of the reference divider coefficient; A0 is the LSB of the IF main divider.

Table 2 Programming the coefficient REFDIV2 for reference subdivider

dt3 (LSB)	dt2	dt1	dt0 (MSB)	REFDIV2
0	0	0	0	1
1	0	0	0	2
0	1	0	0	3
1	1	0	0	4
0	0	1	0	5
1	0	1	0	6
0	1	1	0	7
1	1	1	0	8
0	0	0	1	9
1	0	0	1	10
0	1	0	1	11
1	1	0	1	12
0	0	1	1	13
1	0	1	1	14
0	1	1	1	15
1	1	1	1	16

Table 3 RF and IF synthesizer nominal charge pump currents (gain)

CPI	SINGLE/DOUBLE	I_{CPA} (μA)	I_{CPB} (μA)
0	0	400	400
0	1	800	800
1	0	1200	400
1	1	2400	800

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}, V_{DDX}	digital and crystal reference supply voltages	−0.3	+5.5	V
V_{CCA}, V_{CCB}	analog charge pump supply voltages	−0.3	+5.5	V
V_C – V_D	difference in voltage between analog and digital supplies	−0.3	+5.5	V
V_n	voltage			
	at pins 9 to 12	−0.3	V_{DD} + 0.3	V
	at pins 1, 3, 18 and 20	−0.3	V_{DDX} + 0.3	V
	at pins 4 and 6	−0.3	V_{CCB} + 0.3	V
	at pins 15 and 17	−0.3	V_{CCA} + 0.3	V
ΔV_{GND}	difference in voltage between any of DGND, AGND and XGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	IC storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
$T_{j(max)}$	maximum junction temperature	–	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit; $V_{DD} = V_{DDX} = 2.7$ to 5.5 V; $V_{CCA} = V_{CCB} = 2.7$ to 5.5 V; $T_{amb} = 25\ ^{\circ}C$; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; pins 5, 12, 16 and 19						
V_{DD}, V_{DDX}	digital and crystal reference supply voltages	$V_{DD} = V_{DDX}$; V_{CCA} and $V_{CCB} \geq V_{DD}$	2.7	–	5.5	V
V_{CCA}, V_{CCB}	charge pump supply voltages	V_{CCA} and $V_{CCB} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	V_{DD} = 5.5 V; $\overline{E}$ = 0; ON_A and ON_B = 1	–	1.5	2.0	mA
I_{DDX1}	reference block supply current	V_{DDX} = 5.5 V; XON = 0	–	0.3	0.4	mA
I_{DDX2}	crystal oscillator and buffer currents	V_{DDX} = 5.5 V; XON = 1	–	1.4	1.6	mA
I_{CCA}	RF synthesizer charge pump and prescaler supply currents	V_{CCA} = 5.5 V; ON_B = 0	–	7.3	8.5	mA
I_{CCB}	IF synthesizer charge pump and prescaler supply currents	V_{CCB} = 5.5 V; ON_A = 0	–	3.3	4	mA
$I_{tot(pd)}$	total supply currents ($I_{CCA(pd)} + I_{DD(pd)} + I_{CCB(pd)} + I_{DDX(pd)}$) in power-down mode	logic levels 0 V or V_{DD}; ON_A and ON_B = 1	–	30	60	μA
RF main divider input; pin 15						
f_{RF}	RF input frequency		300	–	2200	MHz
$V_{RF(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω	35	–	225	mV
R_m	main divider ratio		512	–	65535	
Z_i	input impedance (real part)	f_{RF} = 2 GHz	–	60	–	Ω
C_i	pin input capacitance		–	2	–	pF
IF main divider input; pin 6						
f_{IF}	IF input frequency		50	–	500	MHz
$V_{IF(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω	35	–	225	mV
R_m	main divider ratio		128	–	16383	
Z_i	input impedance (real part)	f_{IF} = 400 MHz	–	60	–	Ω
C_i	pin input capacitance		–	2	–	pF
Synthesizers reference divider input; pins 1 and 20						
f_{xtal}	crystal reference oscillator frequency		3	–	30	MHz
$V_{xtal(rms)}$	sinusoidal input signal level between pins 1 and 20 (RMS value)	differential	35	–	500	mV
		single-ended	35	–	250	mV
R_{refc}	common reference division ratio		8	–	1023	
R_{refa}	reference subdivider division ratio		1	–	16	
Z_i	input impedance (real part) per pin	f_{xtal} = 10 MHz	–	4	–	kΩ
C_i	typical pin input capacitance		–	2	–	pF
NF	small signal differential input noise figure	matched to a 4 kΩ source; XON = 1	–	4	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Phase detectors						
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
Charge pump outputs; pins 4 and 17						
V_{CPA}	output voltage compliance range; RF synthesizer		0.4	–	$V_{CCA} - 0.4$	V
V_{CPB}	output voltage compliance range; IF synthesizer		0.4	–	$V_{CCB} - 0.4$	V
$I_{ocp(err)}$	charge pump output current error	note 1	–25	–	+25	%
I_{match}	sink-to-source current matching		–	±5	–	%
I_{Lcp}	charge pump **off** leakage current	$V_{CPA} = ½V_{CCA}$; $V_{CPB} = ½V_{CCB}$	–5	±1	+5	nA
Phase noise						
N_{1000}	RF synthesizer's contribution to close-in phase noise of 1 GHz VCO signal at 1 kHz offset	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	–83	–	dBc/Hz
N_{1800}	RF synthesizer's contribution to close-in phase noise of 1.8 GHz VCO signal at 1 kHz offset	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	–77	–	dBc/Hz
N_{250}	IF synthesizer's contribution to close-in phase noise of 250 MHz VCO signal at 1 kHz offset	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 1000 kHz	–	–102	–	dBc/Hz
Interface logic input signal levels; pins 7, 9, 10, 11 and 13						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	μA
C_i	input capacitance		–	2	–	pF
Low noise crystal oscillator amplifier output signals; pins 3 and 18						
Z_O	differential output impedance (real part)	f_{xtal} = 10 MHz	–	2	–	kΩ
$G_{v(diff)}$	small signal differential voltage gain	XON = 1; f_{xtal} = 10 MHz	–	20	–	dB
$V_{O(p-p)}$	limiting differential output voltage swing (peak to peak value)	XON = 1	–	2	–	V
$\Delta f/f$ (V_{CC})	frequency tolerance as a function of supply voltage change (reference to initial frequency)	note 2	–	tbf	–	ppm
$\Delta f/f$ (Z)	frequency tolerance as a function of load change (reference to initial frequency)	note 2	–	tbf	–	ppm

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System specification						
$FTRF_{IF}$	RF frequency and close harmonics feedthrough to IF frequency	note 3	tbf	–	–	dB
$FTIF_{RF}$	IF frequency and close harmonics feedthrough to RF frequency	note 3	50	–	–	dB

Notes

1. Conditions: $0.4 < V_{CPA} < (V_{CCA} - 0.4)$ and $0.4 < V_{CPB} < (V_{CCB} - 0.4)$.
2. This value is directly dependent on the external resonator quality factor. Only guaranteed for the application circuit which is given in Fig.5.
3. Only guaranteed on the Philips application board.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{DDX} = V_{CCA} = V_{CCB} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	100	–	–	ns
t_{END}	delay from last falling clock edge	−20	–	–	ns
$t_{W(min)}$	minimum inactive pulse width	4000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width ($t_{W(min)}$) can be smaller than 4 μs when the following conditions are fulfilled:

   a) Main divider input frequency $f_{RF} > \frac{447}{t_{W(min)}}$

   b) Reference divider input frequency $f_{xtal} > \frac{3}{t_{W(min)}}$

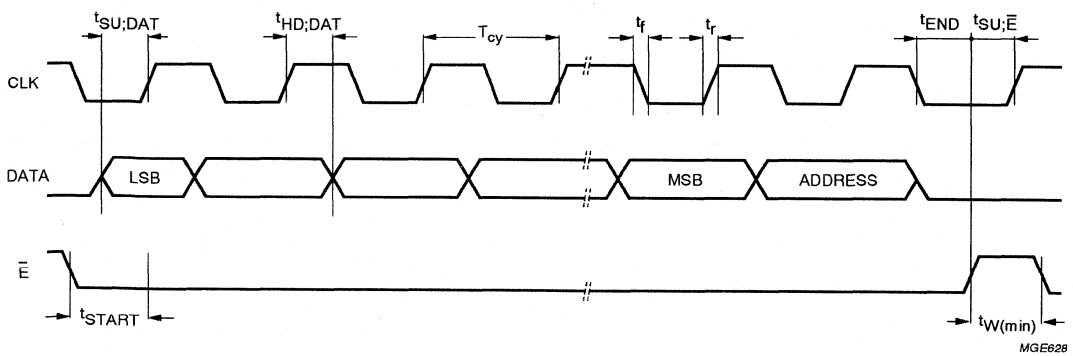


Fig.3 Serial bus timing diagram.

AC TIMING CHARACTERISTICS

$V_{DD} = V_{DDX} = V_{CCA} = V_{CCB} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{PUP}	delay for initial power-up	–	tbf	–	ns
t_{PON}	delay from supply voltage to synthesizer power-on	–	–	tbf	ns
t_{START}	time to turn-on either the RF or IF synthesizer from ON_A/ON_B	–	tbf	–	ns
t_{SEND}	waiting time before sending data on the serial bus	–	–	tbf	ns
t_{LOOP}	time between the active edge of the RF signal and the current output of the charge pump	–	tbf	–	ns
t_{PWRDN}	time to turn-off either the RF or IF synthesizer from ON_A/ON_B	–	tbf	–	ns

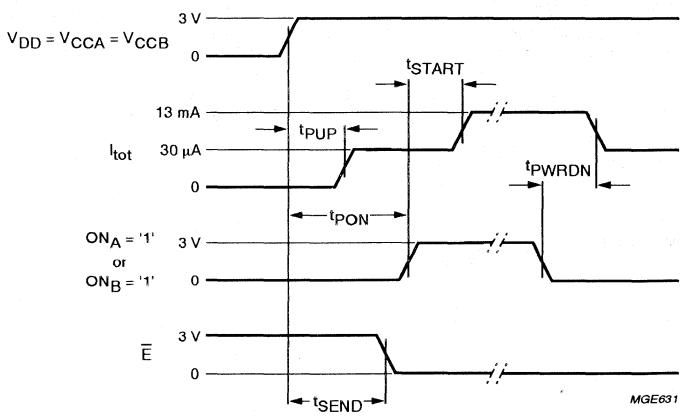
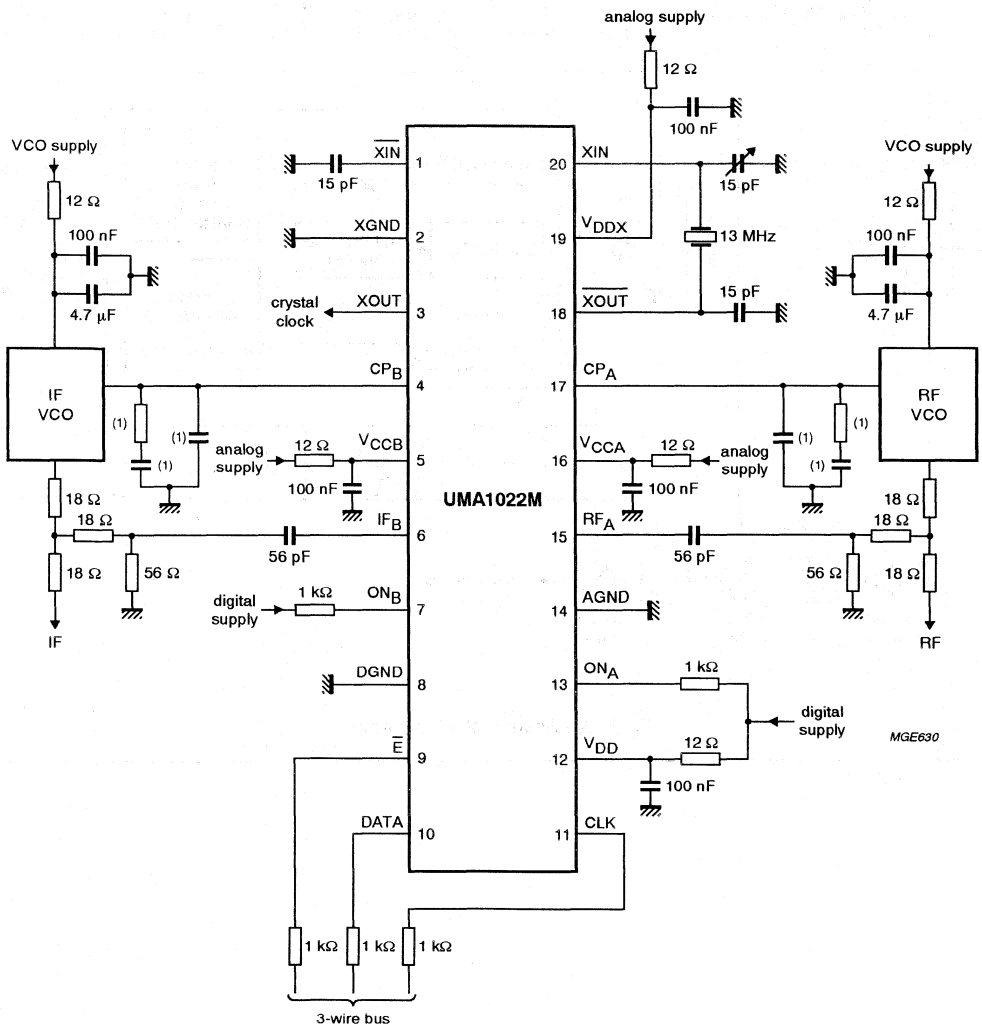


Fig.4 AC timing characteristics.

APPLICATION INFORMATION



(1) Loop filter values depend on the application.

Fig.5 Typical test and application diagram.

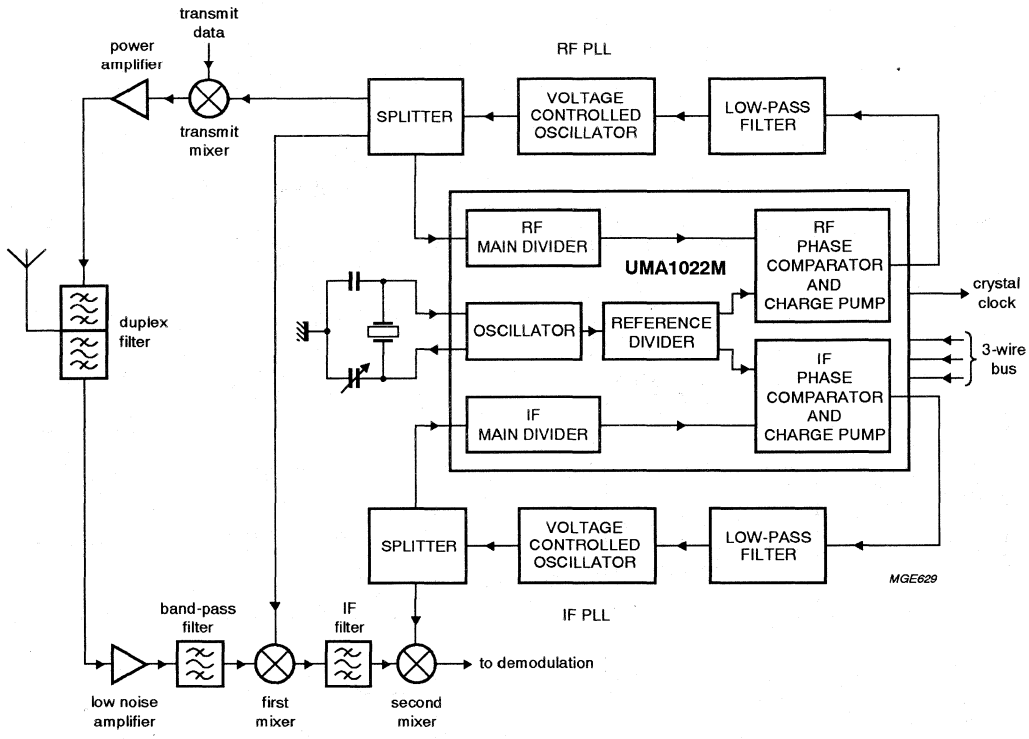


Fig.6 Application block diagram.

Section 8
Transmitters

Wireless Communications

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Single pole double throw (SPDT) switch NE/SA630

DESCRIPTION

The NE630 is a wideband RF switch fabricated in BiCMOS technology and incorporating on-chip CMOS/TTL compatible drivers. Its primary function is to switch signals in the frequency range DC - 1GHz from one 50Ω channel to another. The switch is activated by a CMOS/TTL compatible signal applied to the enable channel 1 pin (ENCH1).

The extremely low current consumption makes the NE/SA630 ideal for portable applications. The excellent isolation and low loss makes this a suitable replacement for PIN diodes.

The NE/SA630 is available in an 8-pin dual in-line plastic package and an 8-pin SO (surface mounted miniature) package.

FEATURES

- Wideband (DC - 1GHz)
- Low through loss (1dB typical at 200MHz)
- Unused input is terminated internally in 50Ω
- Excellent overload capability (1dB gain compression point +18dBm at 300MHz)
- Low DC power (170μA from 5V supply)
- Fast switching (20ns typical)
- Good isolation (off channel isolation 60dB at 100MHz)

PIN CONFIGURATION

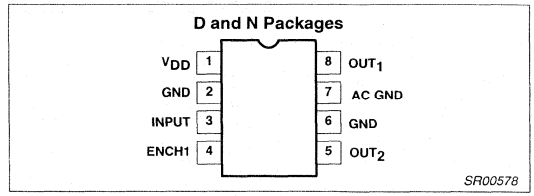


Figure 1. Pin Configuration

- Low distortion (IP_3 intercept +33dBm)
- Good 50Ω match (return loss 18dB at 400MHz)
- Full ESD protection
- Bidirectional operation

APPLICATIONS

- Digital transceiver front-end switch
- Antenna switch
- Filter selection
- Video switch
- FSK transmitter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	NE630N	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to 70°C	NE630D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA630N	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA630D	SOT96-1

BLOCK DIAGRAM

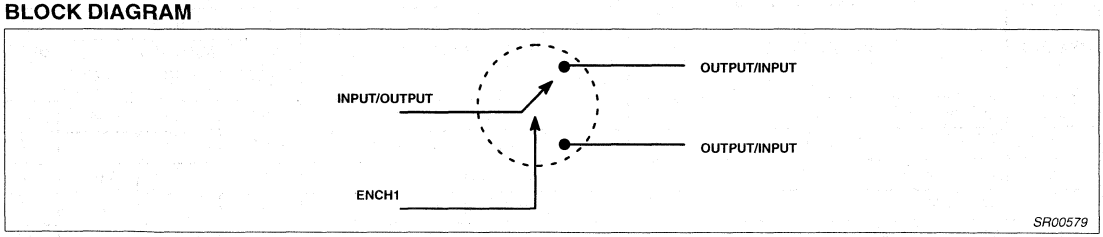


Figure 2. Block Diagram

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	3.0 to 5.5V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

EQUIVALENT CIRCUIT

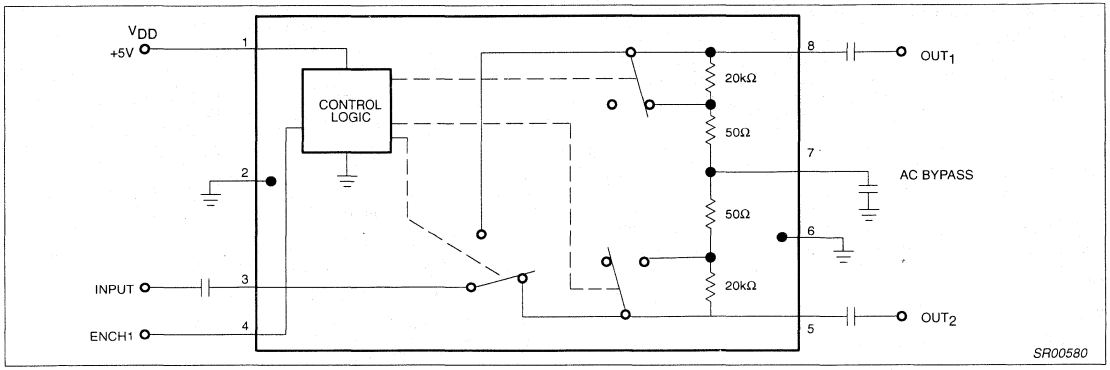


Figure 3. Equivalent Circuit

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	-0.5 to +5.5	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 8-Pin Plastic DIP 8-Pin Plastic SO	 1160 780	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin DIP: θ_{JA} = 108°C/W
   8-Pin SO: θ_{JA} = 158°C/W

DC ELECTRICAL CHARACTERISTICS

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
I_{DD}	Supply current		40	170	300	µA
V_T	TTL/CMOS logic threshold voltage[1]		1.1	1.25	1.4	V
V_{IH}	Logic 1 level	Enable channel 1	2.0		V_{DD}	V
V_{IL}	Logic 0 level	Enable channel 2	-0.3		0.8	V
I_{IL}	ENCH1 input current	ENCH1 = 0.4V	-1	0	1	µA
I_{IH}	ENCH1 input current	ENCH1 = 2.4V	-1	0	1	µA

NOTE:
1. The ENCH1 input must be connected to a valid Logic Level for proper operation of the NE/SA630.

AC ELECTRICAL CHARACTERISTICS[1] - D PACKAGE

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA630			UNITS
			MIN	TYP	MAX	
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2	 2.8	dB
S_{21}, S_{12}	Isolation (OFF channel)[2]	10MHz 100MHz 500MHz 900MHz	70 24	80 60 50 30		dB
S_{11}, S_{22}	Return loss (ON channel)	DC - 400MHz 900MHz		20 12		dB
S_{11}, S_{22}	Return loss (OFF channel)	DC - 400MHz 900MHz		17 13		dB
t_D	Switching speed (on-off delay)	50% TTL to 90/10% RF		20		ns
t_r, t_f	Switching speeds (on-off rise/fall time)	90%/10% to 10%/90% RF		5		ns
	Switching transients			165		mV_{P-P}
P_{-1dB}	1dB gain compression	DC - 1GHz		+18		dBm
IP_3	Third-order intermodulation intercept	100MHz		+33		dBm
IP_2	Second-order intermodulation intercept	100MHz		+52		dBm
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.0		dB

NOTE:
1. All measurements include the effects of the D package NE/SA630 Evaluation Board (see Figure 4B). Measurement system impedance is 50Ω.
2. The placement of the AC bypass capacitor is critical to achieve these specifications. See the applications section for more details.

AC ELECTRICAL CHARACTERISTICS[1] - N PACKAGE

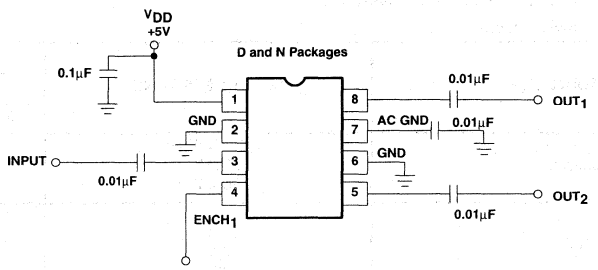
V_{DD} = +5V, T_A = 25°C; all other characteristics similar to the D-Package, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA630			UNITS
			MIN	TYP	MAX	
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2.5		dB
S_{21}, S_{12}	Isolation (OFF channel)	10MHz 100MHz 500MHz 900MHz	58	68 50 37 15		dB
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.5		dB

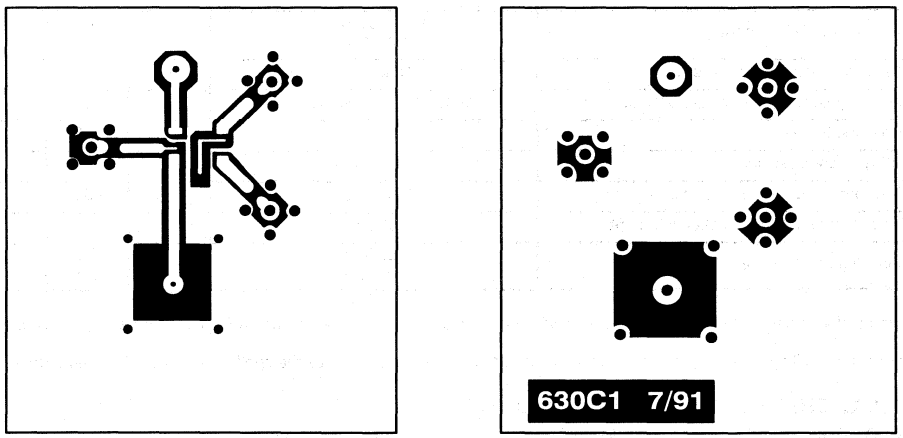
NOTE:
1. All measurements include the effects of the N package NE/SA630 Evaluation Board (see Figure 4C). Measurement system impedance is 50Ω.

APPLICATIONS

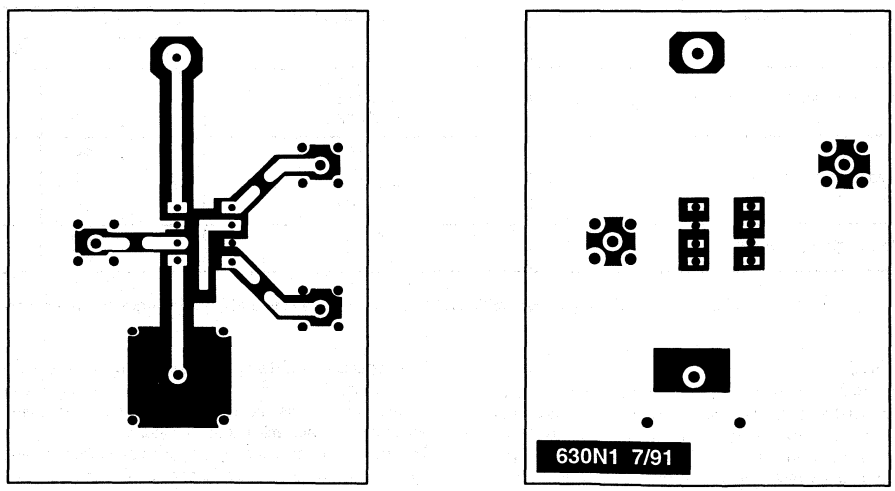
The typical applications schematic and printed circuit board layout of the NE/SA630 evaluation board is shown in Figure 4. The layout of the board is simple, but a few cautions need to be observed. The input and output traces should be 50Ω. The placement of the AC bypass capacitor is *extremely critical* if a symmetric isolation between the two channels is desired. The trace from Pin 7 should be drawn back towards the package and then be routed downwards. The capacitor should be placed straight down as close to the device as practical. For better isolation between the two channels at higher frequencies, it is also advisable to run the two output/input traces at an angle. This also minimizes any inductive coupling between the two traces. The power supply bypass capacitor should be placed close to the device. Figure 10 shows the frequency response of the NE/SA630. The loss matching between the two channels is excellent to 1.2GHz as shown in Figure 13.



a. NE/SA Evaluation Board Schematic



b. NE/SA630 D-Package Board Layout



c. NE/SA630 N-Package Board Layout

SR00581

Figure 4. Board and Package Graphics

The isolation and matching of the two channels over frequency is shown in Figures 15 and 17, respectively.

The NE630 is a very versatile part and can be used in many applications. Figure 5 shows a block diagram of a typical Digital RF transceiver front-end. In this application the NE630 replaces the duplexer which is typically very bulky and lossy. Due to the low power consumption of the device, it is ideally suited for handheld applications such as in CT2 cordless telephones. The NE630 can also be used to generate Amplitude Shift Keying (ASK) or On-Off Keying (OOK) and Frequency Shift Keying (FSK) signals for digital RF communications systems. Block diagrams for these applications are shown in Figures 6 and 7, respectively.

For applications that require a higher isolation at 1GHz than obtained from a single NE630, several NE630s can be cascaded as shown in Figure 8. The cascaded configuration will have a higher loss but greater than 35dB of isolation at 1GHz and greater than 65dB @ 500MHz can be obtained from this configuration. By modifying the enable control, an RF multiplexer/ de-multiplexer or antenna selector can be constructed. The simplicity of NE630 coupled with its ease of use and high performance lends itself to many innovative applications.

The NE/SA630 switch terminates the OFF channel in 50Ω. The 50Ω resistor is internal and is in series with the external AC bypass capacitor. Matching to impedances other than 50Ω can be achieved by adding a resistor in series with the AC bypass capacitor (e.g., 25Ω additional to match to a 75Ω environment).

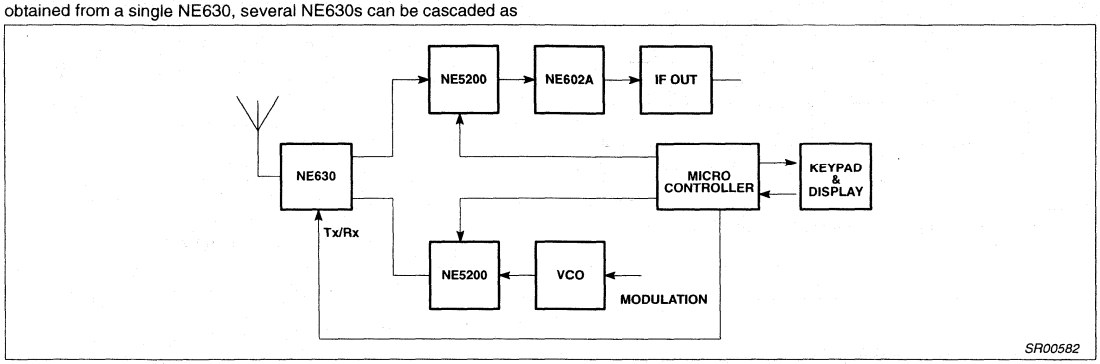


Figure 5. A Typical TDMA/Digital RF Transceiver System Front-End

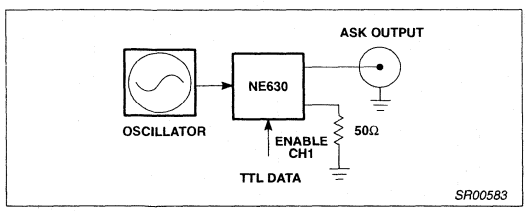


Figure 6. Amplitude Shift Keying (ASK) Generator

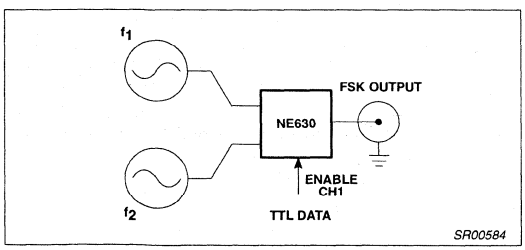


Figure 7. Frequency Shift Keying (FSK) Gnerator

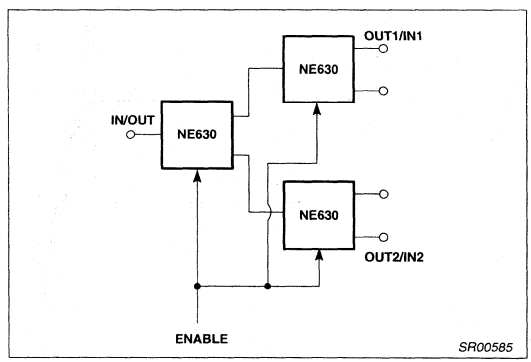


Figure 8.

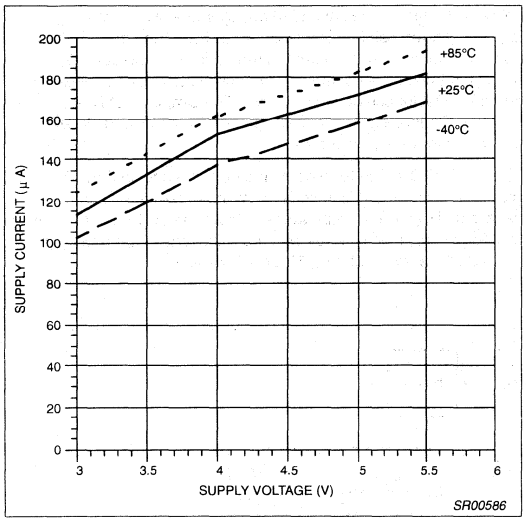


Figure 9. Supply Current vs. V_{DD} and Temperature

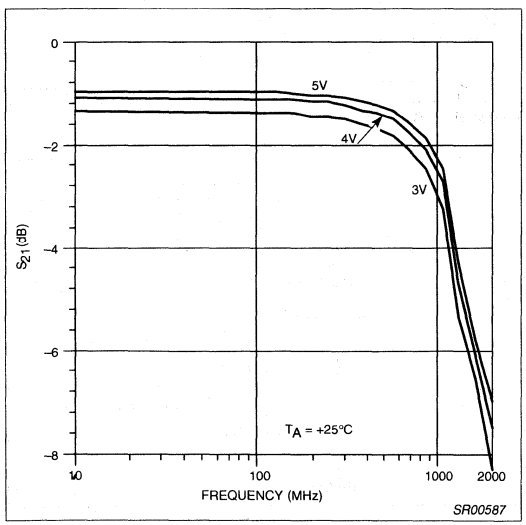


Figure 10. Loss vs. Frequency and V_{DD} for D-Package

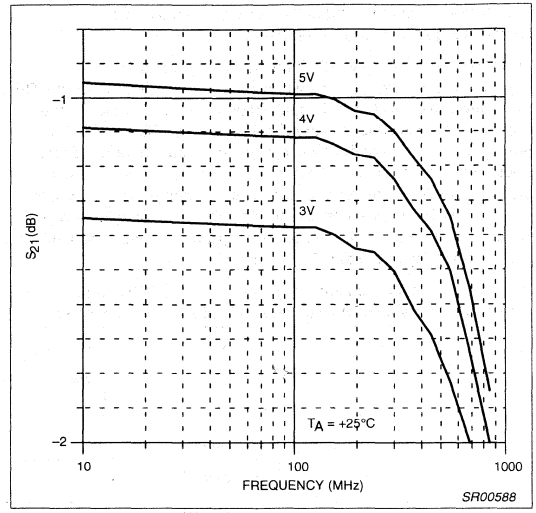


Figure 11. Loss vs. Frequency and V_{DD} for D-Package-Expanded Detail-

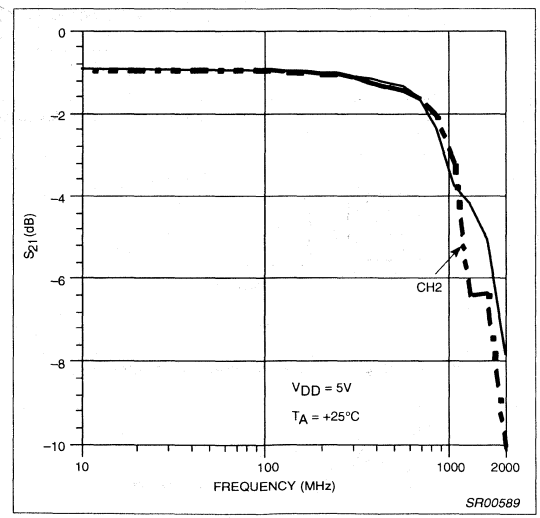


Figure 12. Loss Matching vs. Frequency for N-Package (DIP)

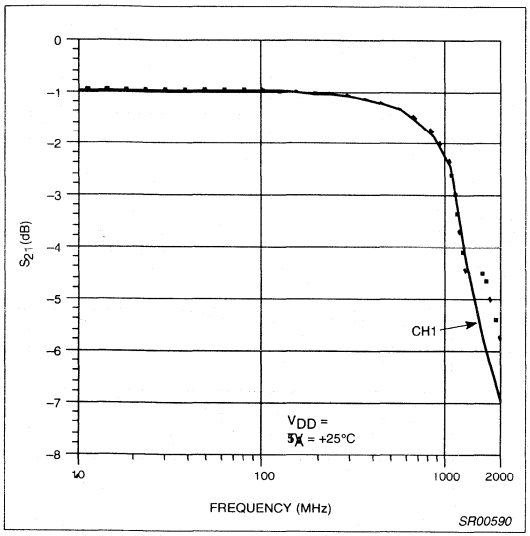


Figure 13. Loss Matching vs. Frequency; CH1 vs. CH2 for D-Pakage

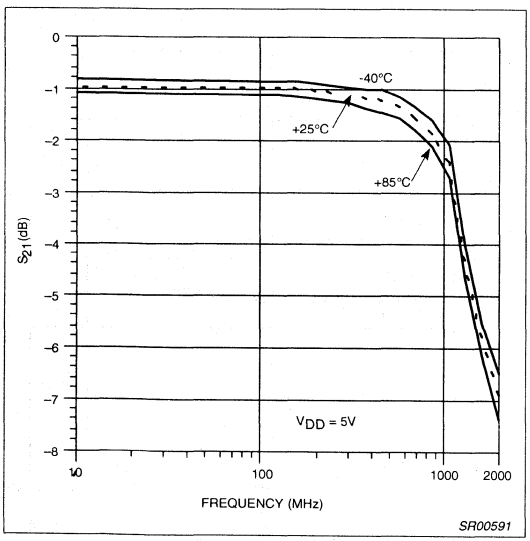


Figure 14. Loss vs. Frequency and Temperature for D-Package

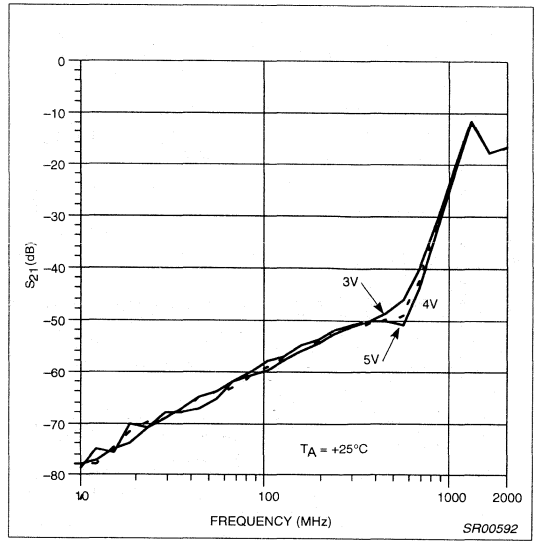


Figure 15. Isolation vs. Frequency and V_{DD} for D-Package

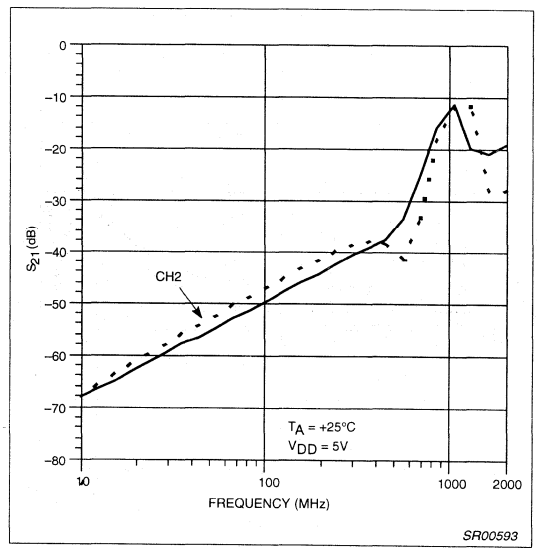


Figure 16. Isolation Matching vs. Frequency for N-Package (DIP)

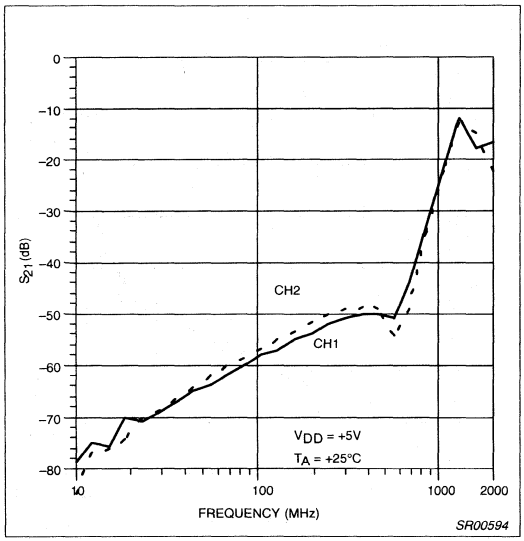


Figure 17. Isolation Matching vs. Frequency; CH1 vs. CH2 for D-Package

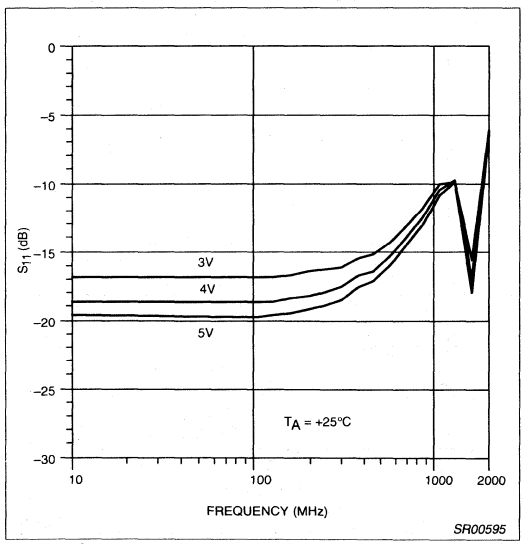


Figure 18. Input Match On-Channel vs. Frequency and V_{DD}

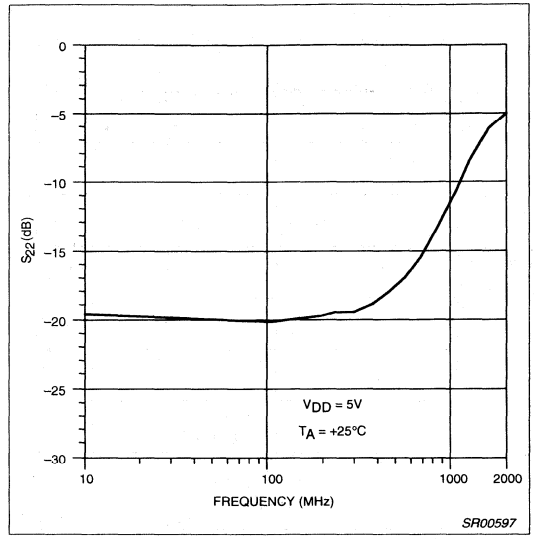


Figure 19. Output Match On-Channel vs. Frequency

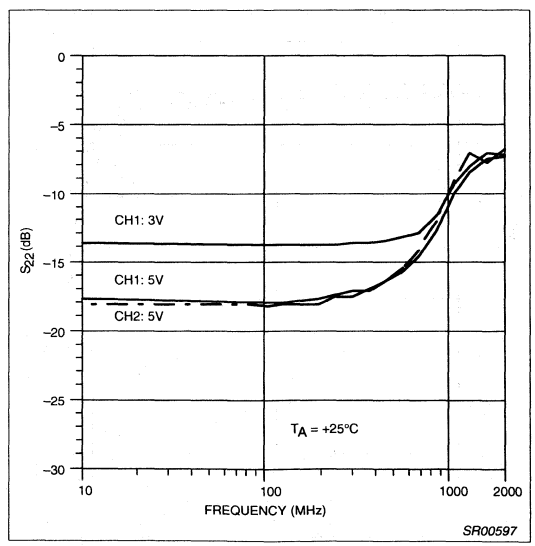


Figure 20. OFF-Channel Match vs. Frequency and V_{DD}

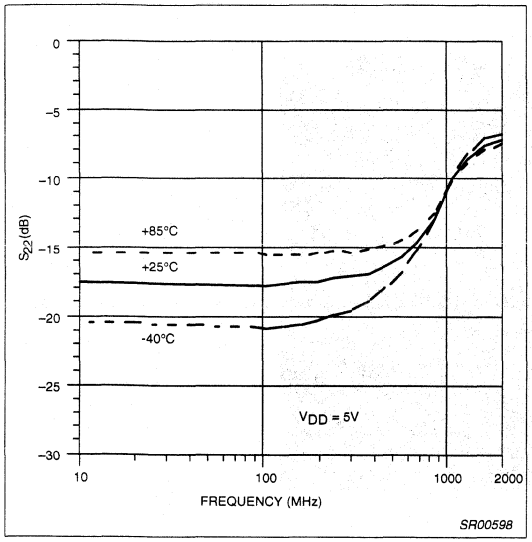


Figure 21. OFF Channel Match vs. Frequency and Temperature

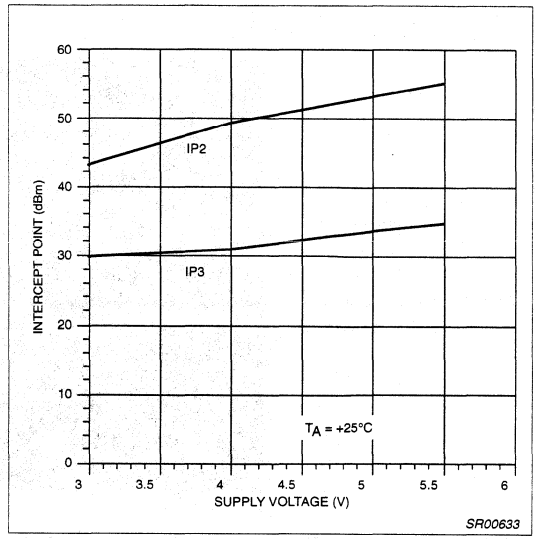


Figure 23. Intercept Points vs.V_{DD}

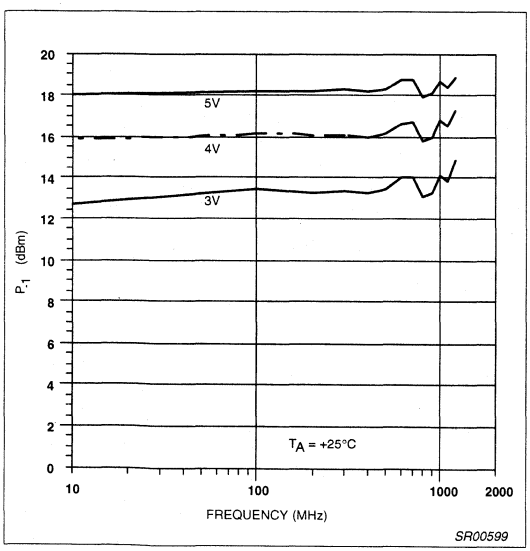


Figure 22. P_{-1} dB vs. Frequency and V_{DD}

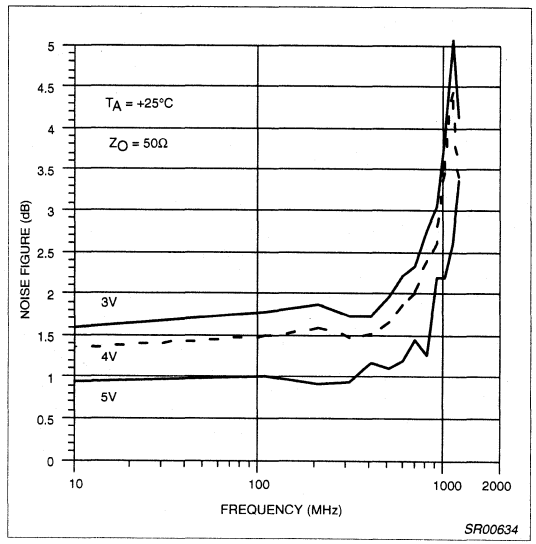


Figure 24. Noise Figure vs. Frequency and V_{DD} for D-Package

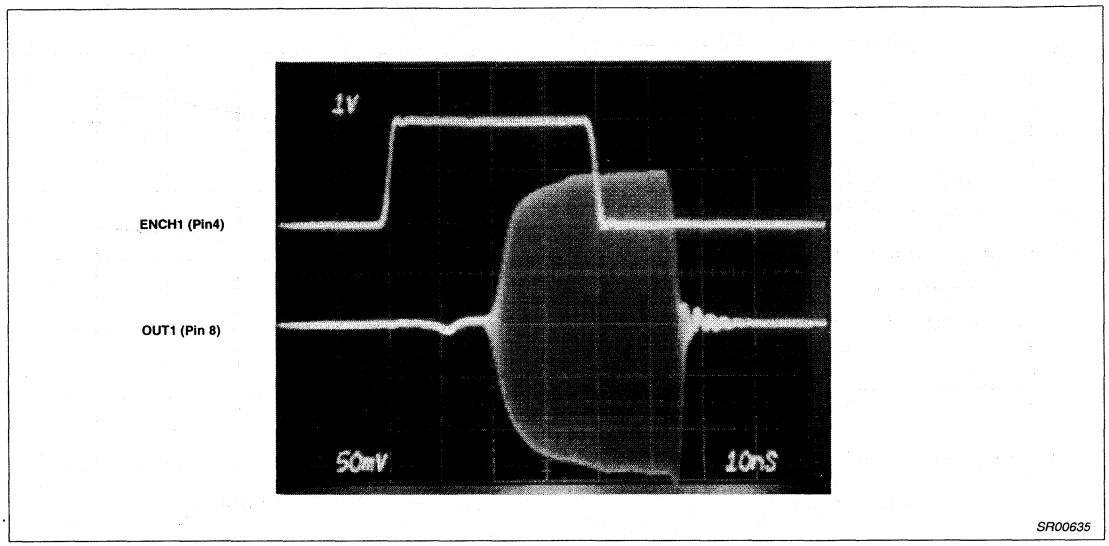


Figure 25. Switching Speed; f_{IN} = 100MHz at -6dBm, V_{DD} = 5V

I/Q transmit modulator SA900

DESCRIPTION

The SA900 is a monolithic high performance, multi-function transmit modulator for use in cellular radio applications, fabricated in QUBiC BiCMOS technology. The SA900 features both analog (AMPS) mode and complex, I/Q digital (NADC IS54) mode quadrature modulation functions, a PLL synthesizer with VCO, crystal oscillator, programmable prescalers and Gilbert cell multiplier phase detector with programmable charge pump output. The DUALTX output can be used in DUAL mode cellular phone applications with the AMPS and NADC modulation being applied to the I/Q baseband inputs. The DUALTX output also provides 6-bit power control with 40dB of gain control in 0.63dB steps. In addition, buffered crystal oscillator programmable prescaler outputs are provided to support system clock reference needs. Programming of the SA900 functions are realized by a high speed 3-wire serial interface. The SA900 can be programmed into a sleep mode (low current mode providing crystal oscillator and Master Clock functions), a standby mode (providing crystal oscillator, Master Clock, System Clock 1 and Transmit LO buffer functions), and the AMPS mode and the DUAL mode configurations.

FEATURES

- V_{CC} = 4.8V
- Tx output frequency = 900MHz
- Direct modulation of RF
- DUAL mode, on-chip PA control
- I/Q modulator
- Single sideband quadrature LO generation with no external adjustments required
- On-chip crystal oscillator with 3 buffered outputs
- AMPS/TACS
- On-chip VCO

PIN CONFIGURATION

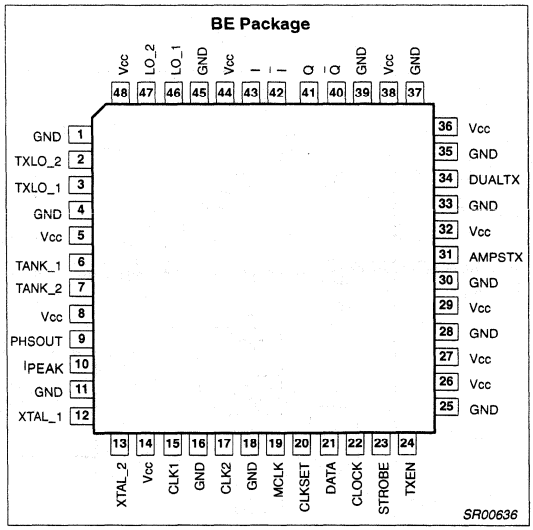


Figure 1. Pin Configuration

- Selective power-down
  - Low power AMPS/TACS mode
  - Low power dual mode NADC
- 48-Pin TQFP package

APPLICATIONS

- North American Digital Cellular (NADC IS-54)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (TQFP)	-40 to +85°C	SA900BE	SOT313-2

BLOCK DIAGRAM

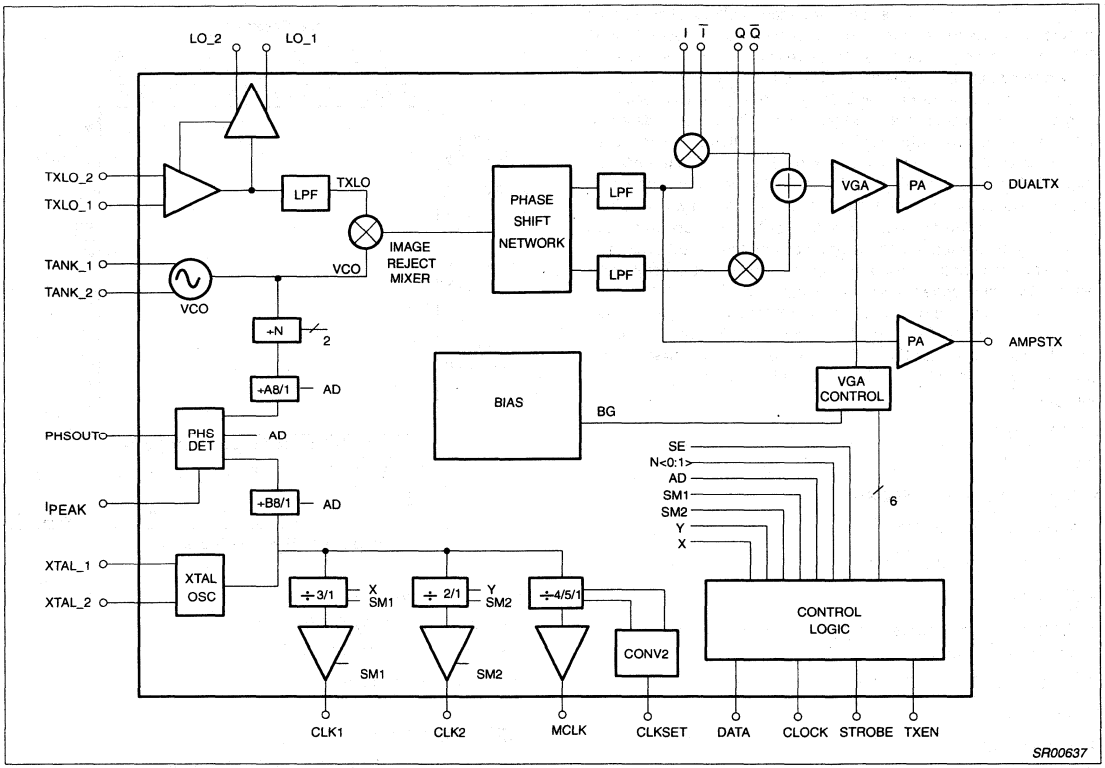


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin	Description
I	Non-inverting I Mod Signal
$\overline{I}$	Inverting I Mod Signal
TXLO_1/2	Second LO Input (differential/single-ended input)
DUALTX	RF output (850MHz) digital (DUAL) mode, complex modulated output
Q	Non-inverting Q Mod Signal
$\overline{Q}$	Inverting Q Mod Signal
CLK1	Buffered oscillator output (XO ÷3/÷1)
MCLK	Buffered oscillator output (XO ÷4/÷5/÷1)
CLK2	Buffered oscillator output (XO ÷2/÷1)
AMPSTX	RF output (850MHz) AMPS mode
V_{CC}	$+5V_{DC}$ power supply
GND	Ground
Data	Serial data input
Clock	Serial clock input
Strobe	Data strobe input
TXEN	AMPS and Dual Mode transmit enable
CLKSET	Program control pin for MCLK prescaler
XTAL1	Crystal oscillator base input
XTAL2	Crystal oscillator emitter output
PHSOUT	Phase comparator charge pump output
TANK_1	VCO differential tank
TANK_2	VCO differential tank
LO_1/2	Buffered differential TXLO output
I_{PEAK}	Phase comparator current programming

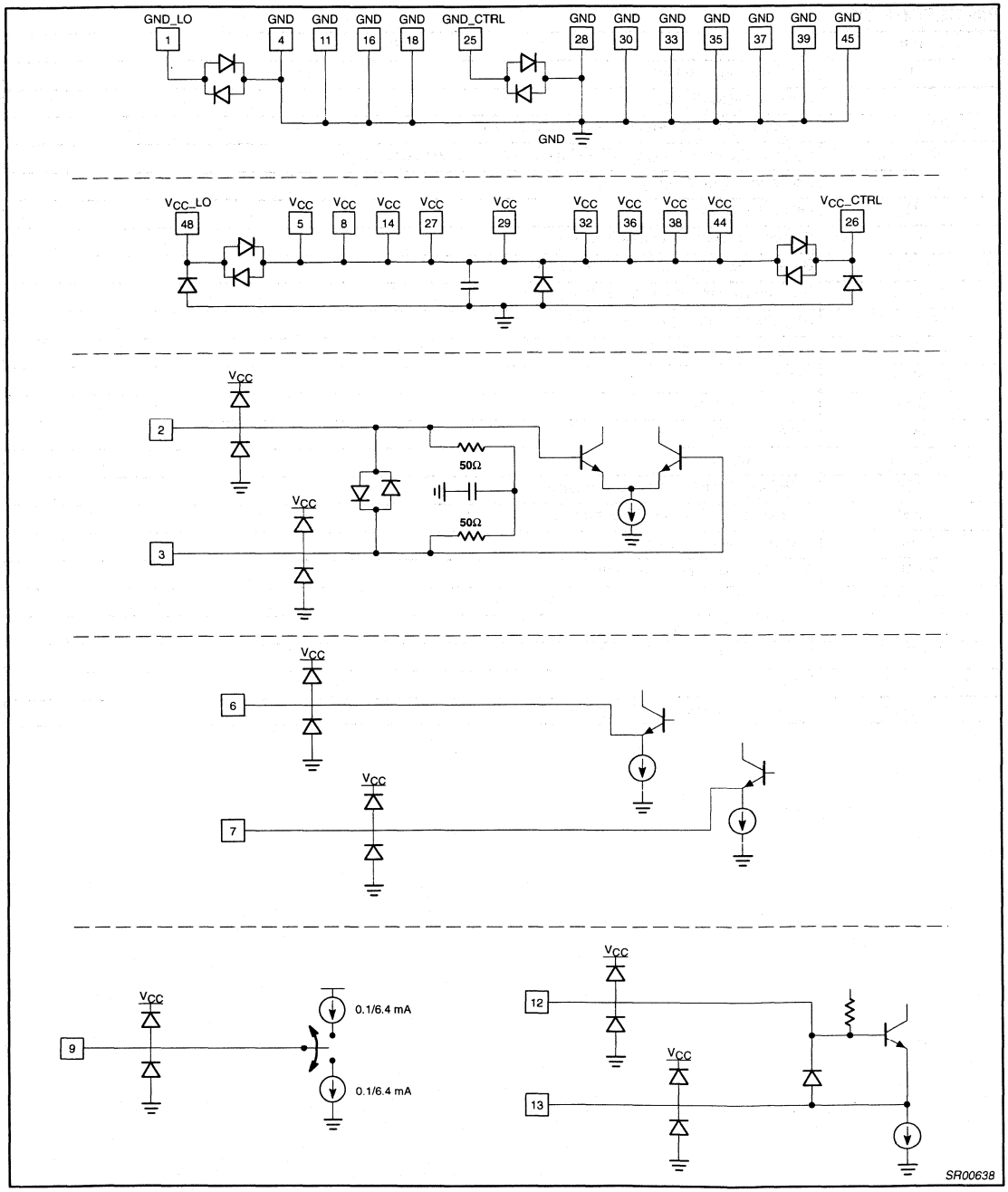


Figure 3. Pin Diagrams

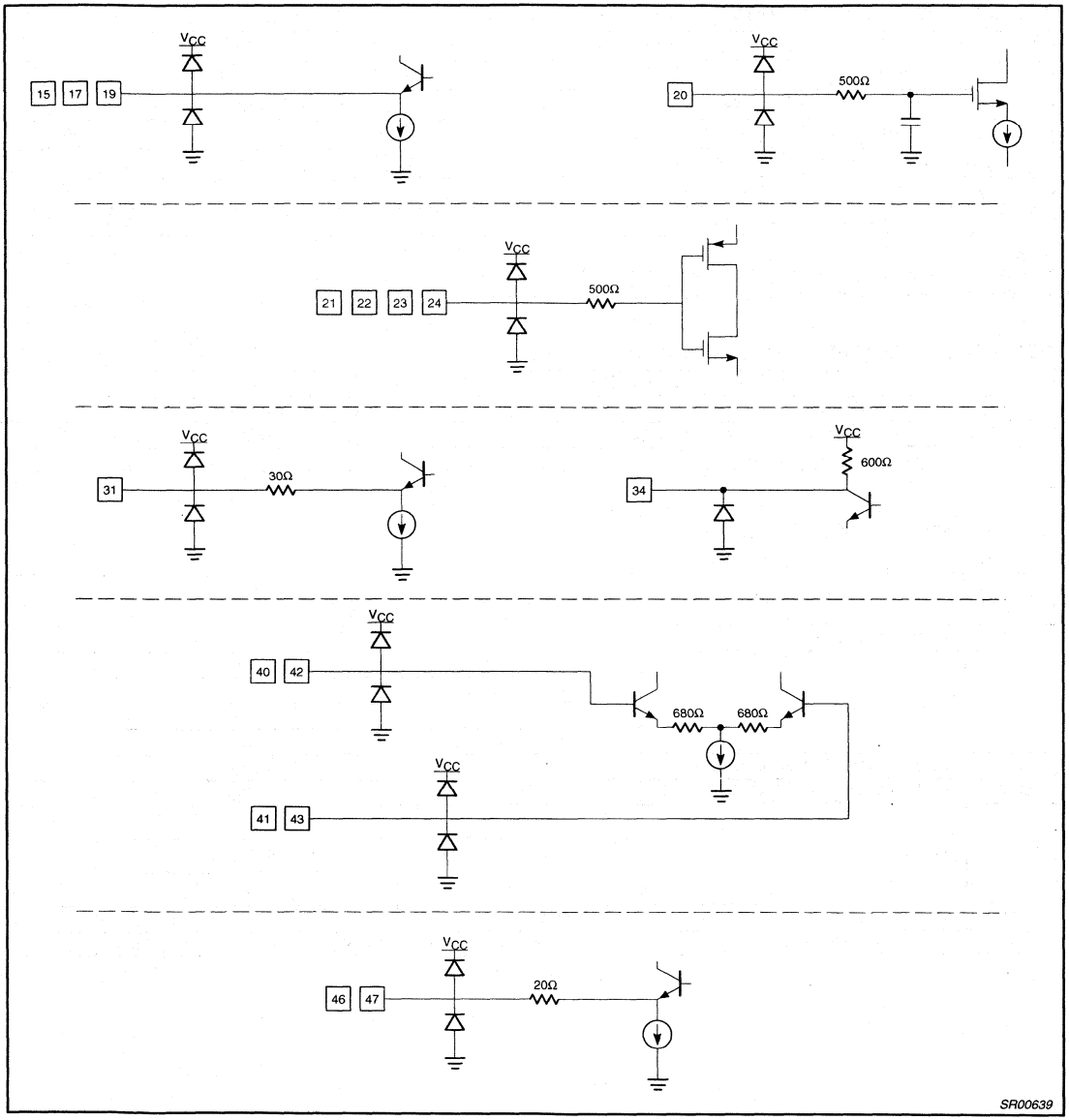


Figure 4. Pin Diagrams (cont.)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)	600	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+10	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}.
   48-pin TQFP: θ_{JA} = 67°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.5 to 5.1	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.8V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply range		4.5		5.1	V
I_{CC}	Supply current	Sleep mode		3.4		mA
		Standby mode		8.7		
		AMPS mode		42		
		DUAL mode		68		
I / $\overline{I}$	In-phase differential baseband input	DC		0.5V_{CC}		V
Q / $\overline{Q}$	Quadraphase differential baseband input	DC		0.5V_{CC}		V
CLKSET	Divide by 4/5/1	÷ 4		V_{CC}		V
		÷ 5		0.5V_{CC}		
		÷ 1		0		
V_{IL}	Clock, data, strobe, TXEN	Input low	–0.3		0.3V_{CC}	V
V_{IH}	Clock, data, strobe, TXEN	Input high	0.7V_{CC}		V_{CC}+0.3	V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.8V, T_A = 25°C; TANK_1 = 120MHz @ 0 dBm; XO_REF = 30MHz @ –5 dBm; TxLO2 = –13 dBm, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
TXLO_1/2	Transmit LO input (AC couple) (50Ω)	Input power	-13		-10[1]	dBm
		VSWR (50Ω)		2:1		
		Frequency range	900		1040	MHz
TANK_1/2	VCO tank differential inputs	Frequency range	90[1]	120	140[1]	MHz
PHSOUT	Phase detector charge pump output	Output level	0.5		V_{CC}–0.5	V
I_{PEAK}	PHSOUT programming	R_{SET} = 24kΩ, AD=0	200	300	400	µA
		R_{SET} = 24kΩ, AD=1	0.9	1.2	1.5	mA
XTAL_1	XO transistor base	XO frequency	10[1]	30	45[1]	MHz
		External drive	150[1]	350	500[1]	mV_{P-P}
CLK1	XO divide 3/1, power down SM1=0, 50% duty cycle	Frequency range	3.33[1]	30	45[1]	MHz
	÷3, X=1, ÷1, X=0	Output level, 5kΩ II 7pF	0.7	1	1.4	V_{P-P}
CLK2	XO divide 2/1, power down SM2=0	Frequency range	5[1]	30	45[1]	MHz
	÷2, Y=1, ÷1, Y=0	Output level, 5kΩ II 7pF	0.7	1	1.4	V_{P-P}
MCLK	XO divide 4/5/1, 50% duty cycle	Frequency range	2[1]		45[1]	MHz
	÷4, CLKSET = V_{CC}, ÷5, CLKSET = 0.5V_{CC}, ÷1, CLKSET = 0V	Output level, 5kΩ II 7pF	0.7	1	1.4	V_{P-P}
CLOCK	Serial data clock input, 33% duty cycle	Max clock rate			10[1]	MHz
	Serial interface (CMOS levels)	Logic LOW			0.3V_{CC}[1]	V
	DATA, CLOCK, STROBE, TXEN	Logic HIGH	0.7V_{CC}			V
AMPSTX	AMPS output, SE=1, AD=0, TXEN=1 (AC couple)	Frequency range	820		860	MHz
		VSWR		2:1		
		Output level	–1.5	+2		dBm
	Spurious output	869 to 894MHz		-104		dBm
		824 to 849MHz		-47		dBc
		2 to 824MHz		-41		dBc
		849 to 869MHz		-41		dBc
		894MHz to 8.49GHz		-41		dBc
	TXLO and harmonics			-21		dBc
	Adjacent channel noise power	@30kHz		-95		dBc/Hz
	Alternate channel noise power	@60kHz		-101		dBc/Hz
	Broadband noise power	869 to 894MHz		-136		dBm/Hz
DUALTX	DUAL output, SE=1, AD=1, TXEN=1 (with external matching Figure 9)	Frequency range	820		920[2]	MHz
		VSWR		2:1		
		Output level (avg) (I and Q quad, 0dB VGA)	0	+2		dBm
		Gain flatness		1		dB

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DUALTX (cont.)	Linearity (0dB VGA, I and Q inphase)	3rd order	-35	-42		dBc
		5th order		-55		dBc
		7th order		-65		dBc
	Carrier suppression (I and Q quadrature)	VGA = 0dB	-35	-45		dBc
	Carrier suppression (I and Q quadrature)	VGA = –40dB	-28	-33		dBc
	Sideband suppression	I and Q quadrature	-35	-45		dBc
	Spurious output	869 to 894MHz		–104		dBm
		824 to 849MHz		–47		dBc
		2 to 824MHz		–41		dBc
		849 to 869MHz		–41		dBc
		894MHz to 8.49GHz		–41		dBc
	TXLO and harmonics			–21		dBc
	Broadband noise (0dB VGA)	869 to 894MHz		–136		dBm/Hz
		935 to 960MHz		–136		dBm/Hz
	Adjacent channel noise power	@30kHz		–95		dBc/Hz
	Alternate channel noise power	@60kHz		–101		dBc/Hz
Q/$\overline{Q}$	Baseband quadrature differential input	Max frequency		0.8	2[1]	MHz
		Differential modulation level	0.6[1]	0.8	1.0[1]	V_{P-P}
		Differential input impedance	10[1]			kΩ
I/$\overline{I}$	Baseband inphase differential input	Max frequency		0.8	2[1]	MHz
		Differential modulation level	0.6[1]	0.8	1.0[1]	V_{P-P}
		Differential input impedance	10			kΩ
LO_1/2	Buffered TXLO differential outputs (AC coupled)	Frequency range	900		1040	MHz
		VSWR (single-ended)		2:1		
	Output impedance	single-ended		50		Ω
		differential		100		Ω
	Output level	single-ended, 50Ω	50	90		mV_{P-P}
		differential, 100Ω	100	180		mV_{P-P}

NOTES:
1. Guaranteed by design.
2. Needs a different matching component. Max test frequency is 850MHz with test circuit shown in Figure 11.

FUNCTIONAL DESCRIPTION

Dual Mode Operation

The SA900 transmit modulator provides direct single sideband quadrature modulation of the difference of the TXLO and VCO frequencies, while providing quadrature LO signals for the I/Q modulator. The quadrature LO signals are modulated with high linearity by the baseband inphase (I) and quadrature (Q) signals. The summed modulator output produces the lower sideband, while rejecting the upper sideband. The I and Q inputs also provide DC biasing for the modulator inputs. The summed output of the modulator goes to a variable gain amplifier (VGA) to control the output level, it has 40.0dB of attenuation control range, with 0.63dB steps. The power control function is programmed by means of a 6-bit word (see Table 3). The VGA output drives the power amp output stage to provide +2dBm average minimum power level (at 0dB power control) into 50Ω, in conjunction with external matching components on DUALTX. The AD (AMPS/DUAL) and the SE (synthesizer enable) bit control the power up/down of the DUAL mode function. The transition of the TXEN, from low to high turns on the modulator. The falling edge of the TXEN signal disables the synthesizer and modulator. The TXLO is a system supplied LO signal. The SA900 buffers the TXLO signal (LO_1/2) for use with the system synthesizer (such as the SA7025) to form the system LO synthesizer loop. The DUAL mode can also be used for AMPS operation. The AMPS and DUAL mode modulation is generated by the system DSP IC to provide the required I/Q baseband modulation for the SA900. The DUAL output provides low broadband noise output power (so that the receiver sensitivity is not degraded) and high linearity to meet cellular phone system needs. Table 1 provides the VGA power control limits.

The SA900 DUALTX output is externally matched with either a shunt inductor to V_{CC} and a series capacitor or a shunt inductor to V_{CC} and a series inductor. This matches the DUALTX output to 50Ω. Values of the matching components are dependent on PCB layout, typical values are shown in Figure 9.

Table 1. VGA Power Control Limits

VGA	Min.	Typ.	Max.	Relative VGA
0	0	0	0	0
1	-1	-.63	-.2	0
2	-1	-.63	-.2	1
3	-1	-.63	-.2	2
4	-1	-.63	-.2	3
5	-1	-.63	-.2	4
6	-1	-.63	-.2	5
7	-1	-.63	-.2	6
15	-6.6	-5	-3	7
23	-6.6	-5	-3	15
31	-6.6	-5	-3	23
39	-6.6	-5	-3	31
47	-6.6	-5	-3	39
55	-6.6	-5	-3	47
63	-6.6	-5	-3	55
63	-43.2	-40.4	-37.2	0

1. Guaranteed to be monotonic.

AMPS Mode Operation

The SA900 can be configured to operate in the AMPS mode, where FM modulation is applied to the SA900's VCO. For the AMPS mode, the VCO is configured with the proper synthesizer bandwidth to allow the application of the AMPS modulation to the VCO varactor tuned tank circuit. The modulated VCO signal is input into an image reject mixer along with the TXLO signal, where the upper sideband is rejected. This single sideband modulated signal then drives the AMPS output power amplifier. The PA provides +2dBm power level into 50Ω, with no external matching components required. The AD (AMPS/DUAL) and the SE (synthesizer enable) bit control the power up/down of the AMPS mode function. The transition of the TXEN signal from low to high turns on the modulator. The falling edge of TXEN signal disables the synthesizer and the modulator.

Synthesizer Operation

The SA900 synthesizer is comprised of the differential VCO circuit, with external tank components, the Gilbert cell multiplier phase detector with programmable charge pump current, crystal oscillator and programmable prescalers. The charge pump output drives an external second order loop filter. The output of the loop filter is used to provide the control voltage to the VCO tuning varactor to complete the PLL synthesizer. The synthesized VCO output frequency is mixed with the TXLO signal to generate the transmit LO from the lower sideband (the difference of the VCO and TXLO frequencies). The output of VCO is fed to a programmable /N prescaler with user selectable divides of 6, 7, 8 and 9 (all divides configured to provide 50% duty cycle). The output of the /N divider drives the A8/1 prescaler. The A8/1 divide is selected by the AD control bit (AD=1 for /1, and AD=0 for /8). The output of the divide A8/1 is fed into one input of the phase detector. The reference input for the phase comparator is generated from the crystal oscillator (XO) output from the B8/1 prescaler. The B8/1 divide is selected by the AD control bit (AD=0 for /8, and AD=1 for /1). The phase detector compares the prescaled XO reference phase to the VCO prescaled phase, to generate a charge pump output current proportional to the phase error. The phase detector, a Gilbert cell multiplier type, having a linear output from 0 to π ($\pi/2 \pm \pi/2$). The charge pump peak output current is programmable from 100µA for the AMPS mode (AD=0) to a maximum of 6.4mA for the DUAL mode (AD=1) by way of an external current setting resistor placed from I_{PEAK} to circuit ground. The typical loop filter network is shown in Figure 5. The charge pump current output is programmed by

$$AD = 0 \qquad I_{OUT} = 6 \cdot \left(\frac{1.25V}{R_{SET}}\right)$$

$$AD = 1 \qquad I_{OUT} = 24 \cdot \left(\frac{1.25V}{R_{SET}}\right)$$

where R_{SET} is placed between I_{PEAK} and GROUND.

The PLL frequency is determined by

$$VCO = XO \cdot N \cdot \frac{\left(\frac{A8}{1}\right)}{\left(\frac{B8}{1}\right)}$$

where N=6, 7, 8, 9 and A8/1 and B8/1 are controlled by the AD bit (AD=1 A8/1 and B8/1 are divide by 1, AD=0 A8/1 and B8/1 are divide 8).

Table 2. Data Word Format

Mnemonics	Bits	Function
A0	1 (MSB)	Address bit 0 (1)
A1	2	Address bit 1 (0)
A2	3	Address bit 2 (1)
A3	4	Address bit 4 (1)
PC0	5	Power control bit 0
PC1	6	Power control bit 1
PC2	7	Power control bit 2
PC3	8	Power control bit 3
PC4	9	Power control bit 4
PC5	10	Power control bit 5
N0	11	Divide N bit 0
N1	12	Divide N bit 1
AD	13	AMPS/DUAL mode select bit
SE	14	Synthesizer enable bit
NA	15	NA
SM1	16	Sleep mode 1 control bit
SM2	17	Sleep mode 2 control bit
X	18	Divide 3/1 control bit
Y	19	Divide 2/1 control bit
NA	20	NA
NA	21	NA
NA	22	NA
NA	23	NA
NA	24 (LSB)	NA

VCO Operation

The VCO is designed to operate from 90MHz to 140MHz. The VCO tank is configured using a parallel inductor and a dual common cathode tuning varactor diodes. DC blocking capacitors are used to isolate the varactor

control voltage from the VCO tank DC bias voltages. The VCO tuning voltage is generated from the output of the PLL loop filter. The VCO tank configuration is shown in Figure 6.

Crystal Oscillator (XO) Operation

For cellular radio applications, the SA900 will most likely utilize an external reference TCXO in order to provide the frequency stability necessary to operate to system requirements. The output of the system TCXO can be AC coupled to the XTAL_1 input. However, for applications that do not require such accuracy the XO circuit can be configured as a Colpitts type oscillator with the addition of two external capacitors along with the reference crystal and a trim capacitor as shown in Figure 7.

Programmable Clock Outputs

The SA900 generates three buffered XO outputs used for external reference signals. The XO feeds three sets of programmable prescalers, the prescaler outputs are buffered to provide the CLK1, CLK2 and MCLK signals. The CLK1 signal is a selectable divide 3/1 (X=1 divide 3, X=0 divide 1), 50% duty cycle, of the XO reference signal. The CLK2 signal is a selectable divide 2/1 (Y=1 divide 2, Y=0 divide 1), 50% duty cycle, of the XO reference signal. The MCLK signal is a selectable divide 4/5/1 (CLKSET = V_{CC} divide 4, CLKSET = V_{CC}/2 divide 5, and CLKSET = 0V divide 1), 50% duty cycle, of the XO reference signal. MCLK is externally set by means of the tri-level CLKSET input to provide a default master system clock prior to programming the SA900.

Programming Operation

The SA900 is configured by means of a 3-wire input (CLOCK, STROBE, DATA) to program the AMPS and DUAL modes, in addition there are two power saving modes of operation, SLEEP and STANDBY. The control logic section of the SA900 is designed using low power CMOS logic. During SLEEP mode only the circuitry required to provide a master clock (MCLK) to the digital portion of the system is enabled. During the STANDBY mode of operation MCLK, CLK1 and the TXLO and buffered LO outputs are powered on, which may be the case when the system is in the receive only mode. In the AMPS or DUAL operational modes all functions of the SA900 are powered on to support receive, transmit and system clock functions. The programming of the SA900 is identical to the programming format of the SA7025 low-voltage 1GHz fractional-N synthesizer, that can be used in conjunction with the SA900 to provide the cellular radio channel selection.

The programming data is structured as a 24 bit long serial data word; the word includes 4 address bits (dedicated 1 0 1 1) for chip select. Data bits are shifted in on the leading edge of the clock, with the least significant bit (LSB) first and the most significant bit (MSB) last. Table 2 shows data word format, the 15th and last 5 bits are not used. Figure 8 shows the chip timing diagram.

Address

A0	A1	A2	A3
1	0	1	1

Divide By N

N0	N1	Divide
0	0	6
1	0	7
0	1	8
1	1	9

AMPS/DUAL Mode

The A/D mode select enables or disables that portion of the circuitry used for either the AMPS or DUAL mode of operation.

AD	Mode
0	AMPS
1	DUAL

Synthesizer Enable

The SE bit turns on and off the synthesizer circuitry.

SE	Operation
0	Disabled
1	Enabled

Sleep Mode 1

The SM1 bit is used to power down the TXLO buffer, the divide 3/1 prescaler and the CLK1 output buffer.

SM1	Operation
0	Power down
1	Power up (STANDBY)

Sleep Mode 2

The SM2 bit is used to power down the divide 2/1 prescaler and the CLK2.

SM2	Operation
0	Power down
1	Power up (with SM1=1 normal operation)

Divide 3

X	Operation
0	Divide 1
1	Divide 3

Divide 2

Y	Operation
0	Divide 1
1	Divide 2

Table 3. Power Control

Attenuation (dB)	PC0 (0.6dB)	PC1 (1.3dB)	PC2 (2.5dB)	PC3 (5.0dB)	PC4 (10.0dB)	PC5 (20.0dB)
0	0	0	0	0	0	0
0.6	1	0	0	0	0	0
1.3	0	1	0	0	0	0
1.9	1	1	0	0	0	0
2.5	0	0	1	0	0	0
3.2	1	0	1	0	0	0
3.8	0	1	1	0	0	0
4.4	1	1	1	0	0	0
5.0	0	0	0	1	0	0
5.7	1	0	0	1	0	0
6.3	0	1	0	1	0	0
• • •						
23.3	1	0	1	0	0	1
• • •						
39.7	1	1	1	1	1	1

Component Designator	Value	
	DUAL Mode	AMPS Mode
R1	560Ω	560Ω
R2	1kΩ	5.6kΩ
C1	2.2nF	2.7µF
C2	No Load	.27µF
C3	33pF	6.8nF
R_{SET}	15kΩ	75kΩ

Typical Filter Network

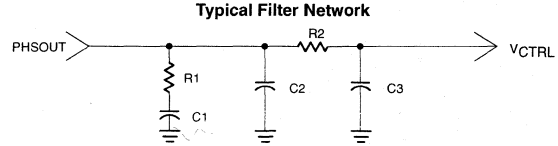


Figure 5. PLL Loop Filter

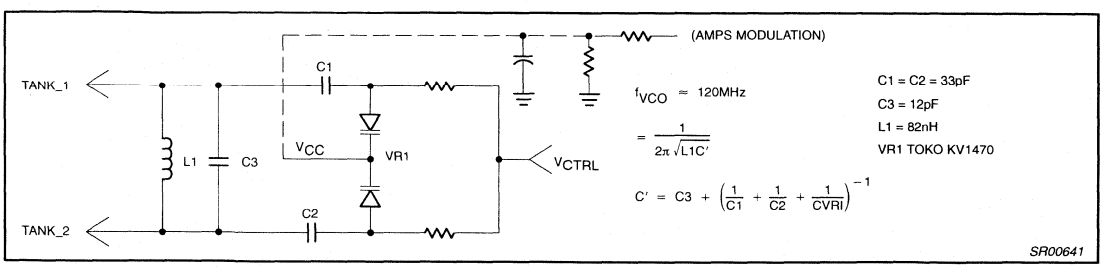


Figure 6. VCO Tank Configuration

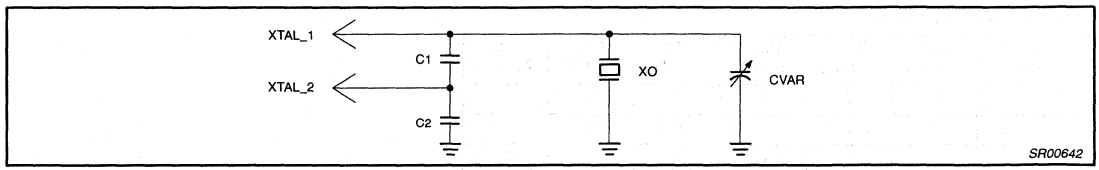


Figure 7. Crystal Oscillator Configuration

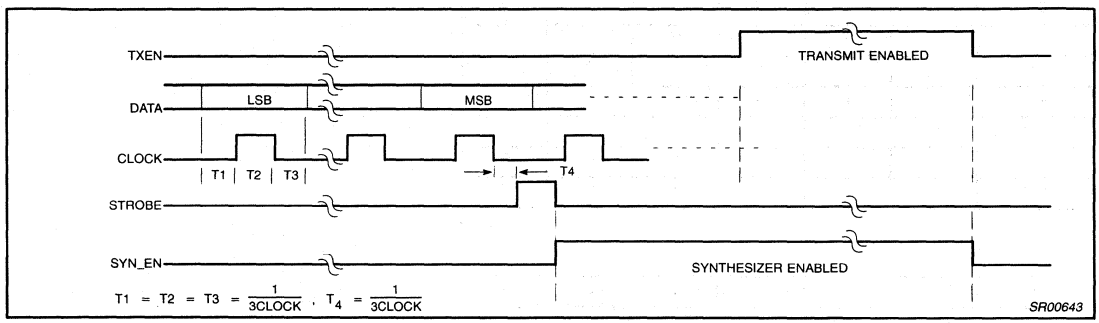


Figure 8. Chip Timing Diagram

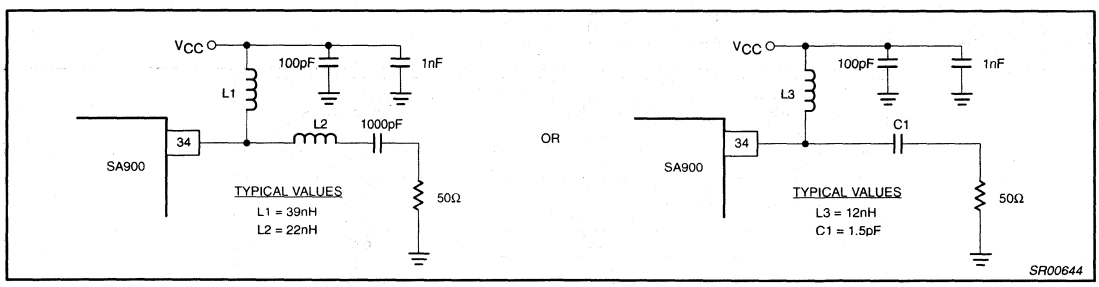


Figure 9. DUALTX Output Matching

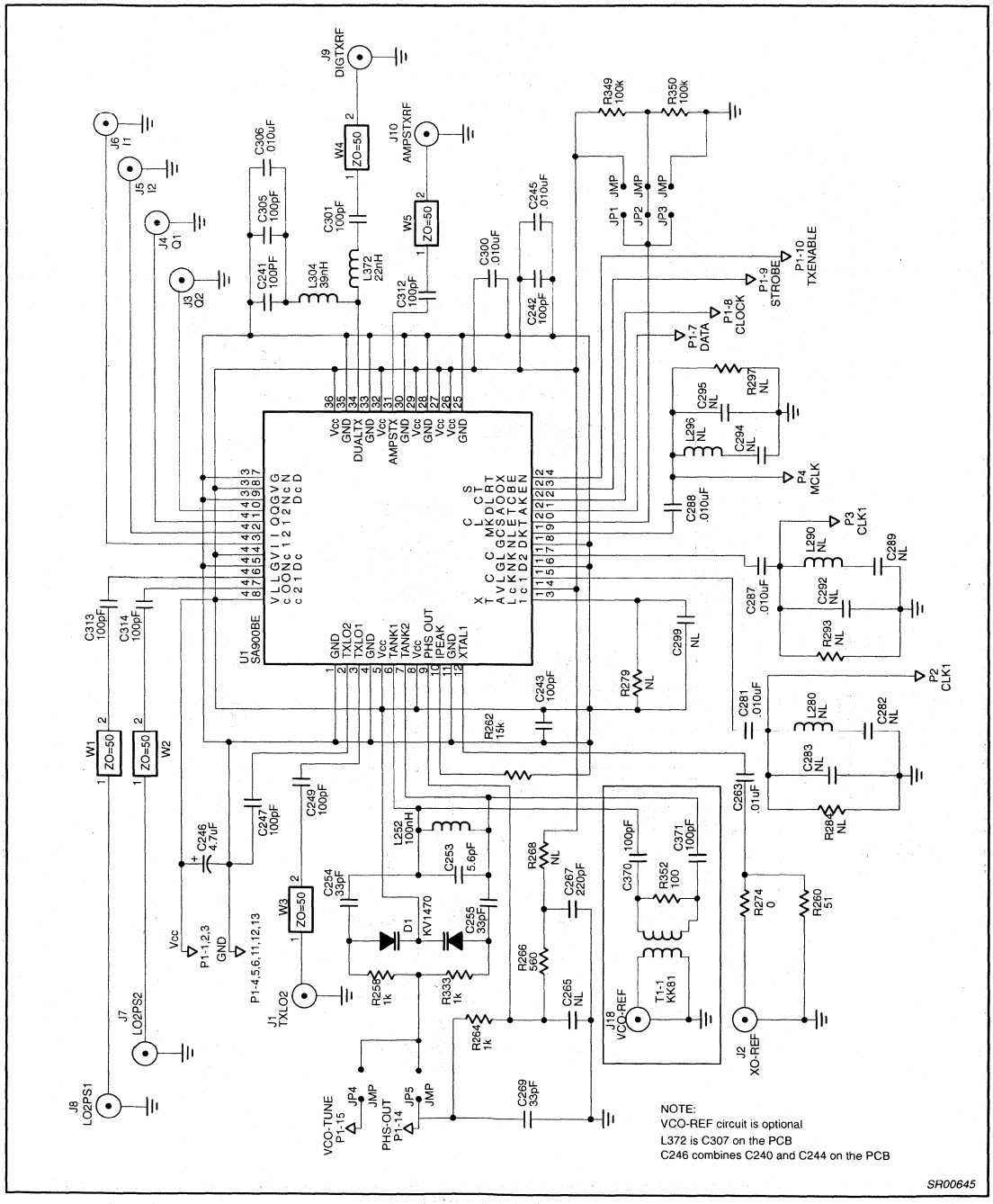


Figure 10. SA900 Application Circuit

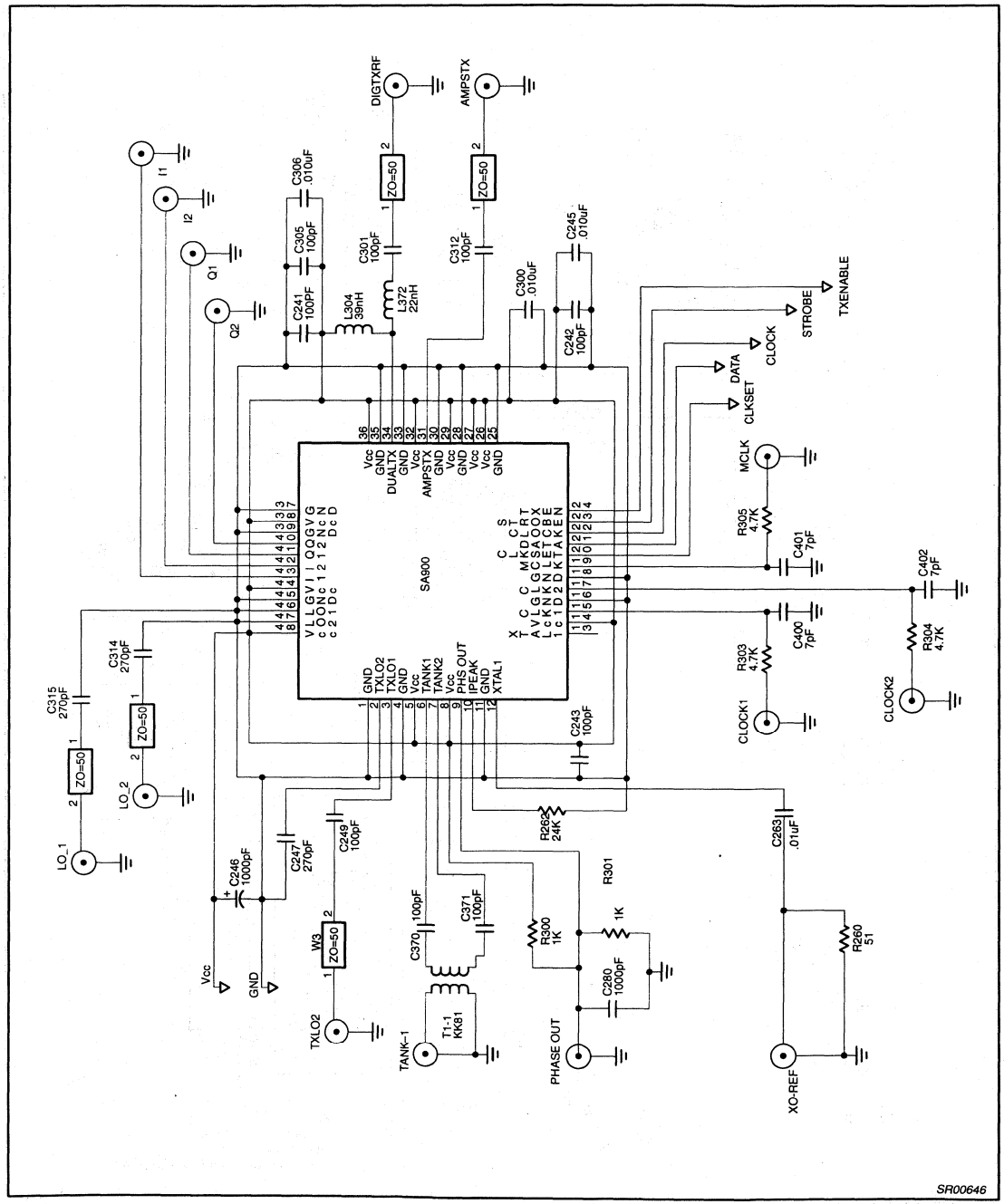
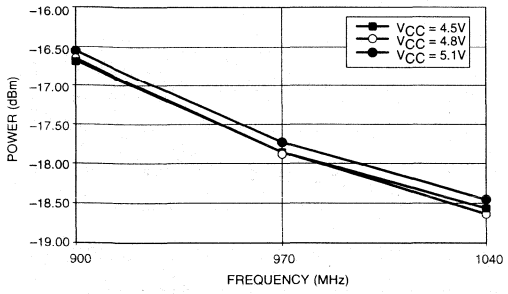
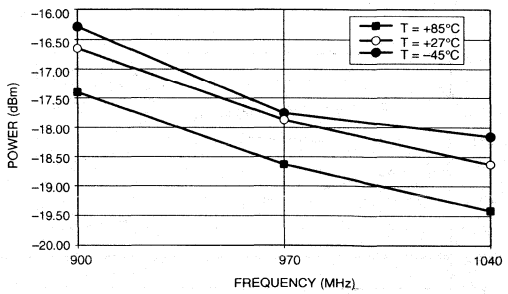


Figure 11. SA900 Test Circuit

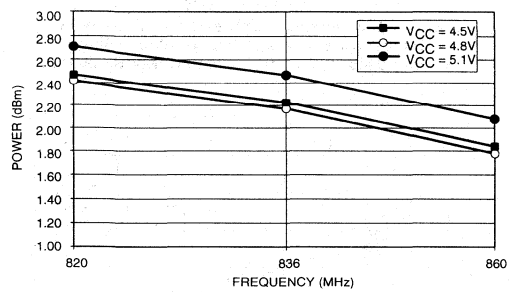
PERFORMANCE CHARACTERISTICS



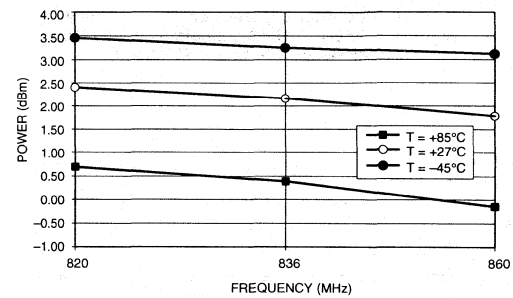
LO Buffer vs. Frequency (27°C, TXLO = –10dBm)



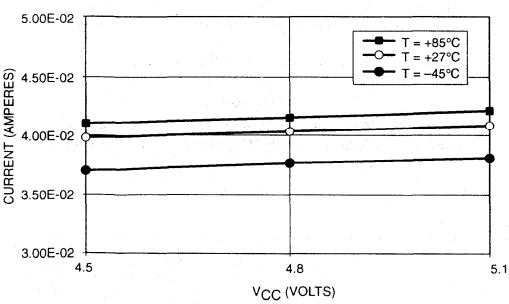
LO Buffer vs. Frequency (V_{CC} = 4.8V, TXLO = –10dBm)



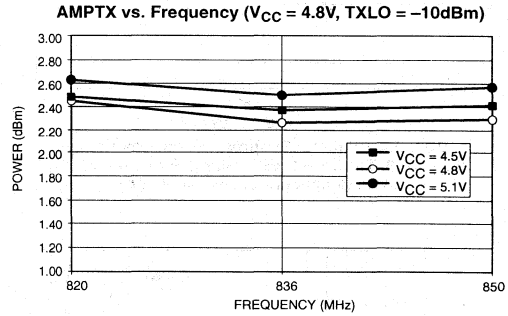
AMPTX vs. Frequency (27°C, TXLO = –10dBm)



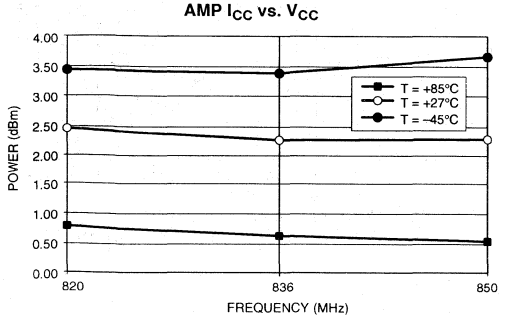
AMPTX vs. Frequency (V_{CC} = 4.8V, TXLO = –10dBm)



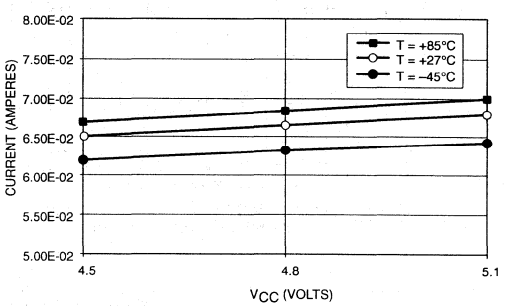
AMP I_{CC} vs. V_{CC}



DUALTX vs. Frequency (27°C, TXLO = –10dBm)



DUALTX vs. Frequency (V_{CC} = 4.8V, TXLO = –10dBm)

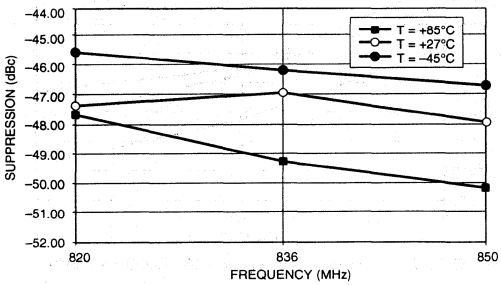


DUAL I_{CC} vs. V_{CC}

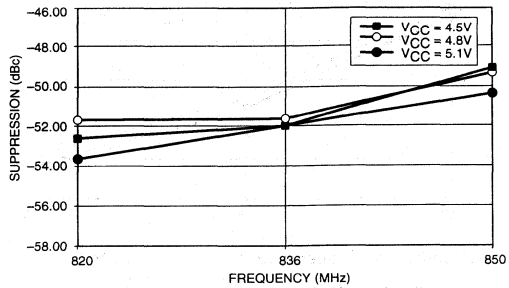
SR00647

Figure 12. Performance Characteristics

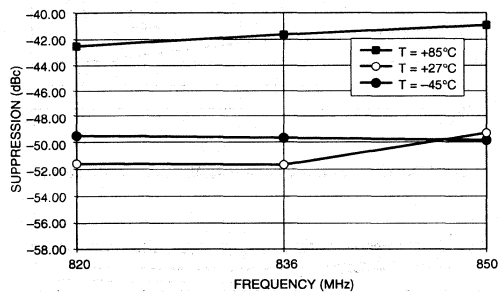
PERFORMANCE CHARACTERISTICS



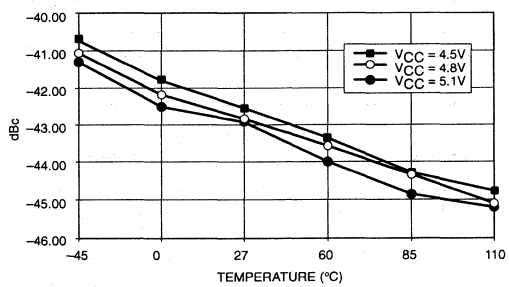
DUALTX Carrier Suppression vs. Frequency (V_{CC} = 4.8, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



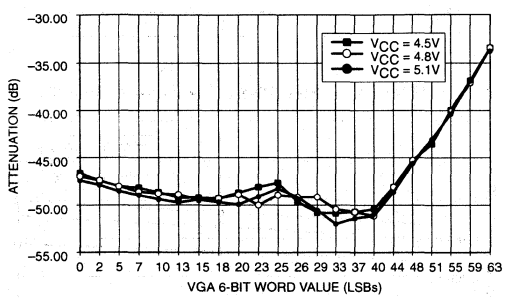
DUALTX Sideband Suppression vs. Frequency (Temperature = 27°C, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



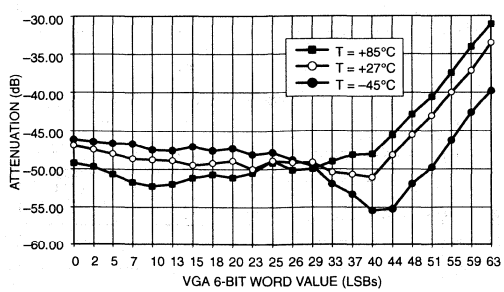
DUALTX Sideband Suppression vs. Frequency (V_{CC} = 4.8, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



DUALTX 3rd Order Products vs Temperature (TXLO = –10dBm, f = 836MHz, 0dB VGA I/Q Inphase)



DUALTX Carrier Suppression vs VGA Range (27°C, f = 836MHz, TXLO = –10dBm)

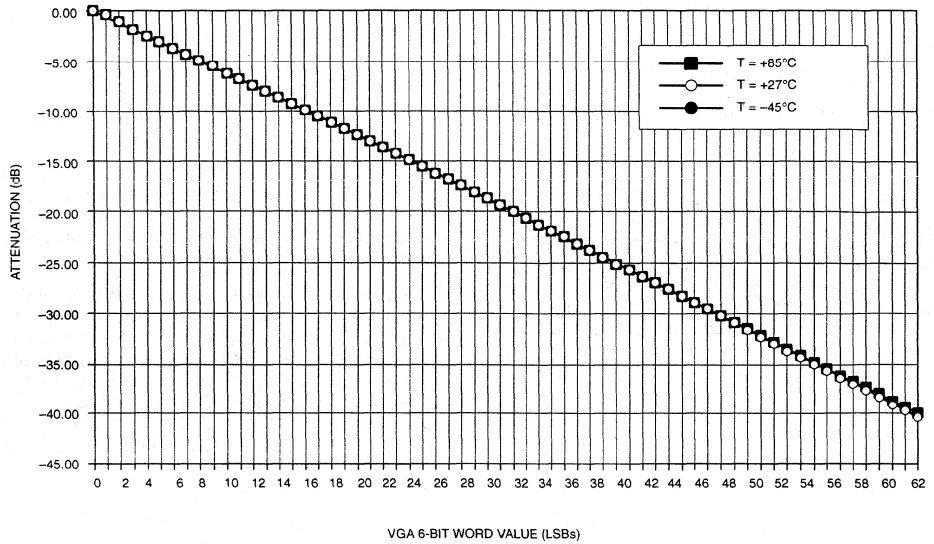


DUALTX Carrier Suppression vs VGA Range (V_{CC} = 4.8V, f = 836MHz, TXLO = –10dBm)

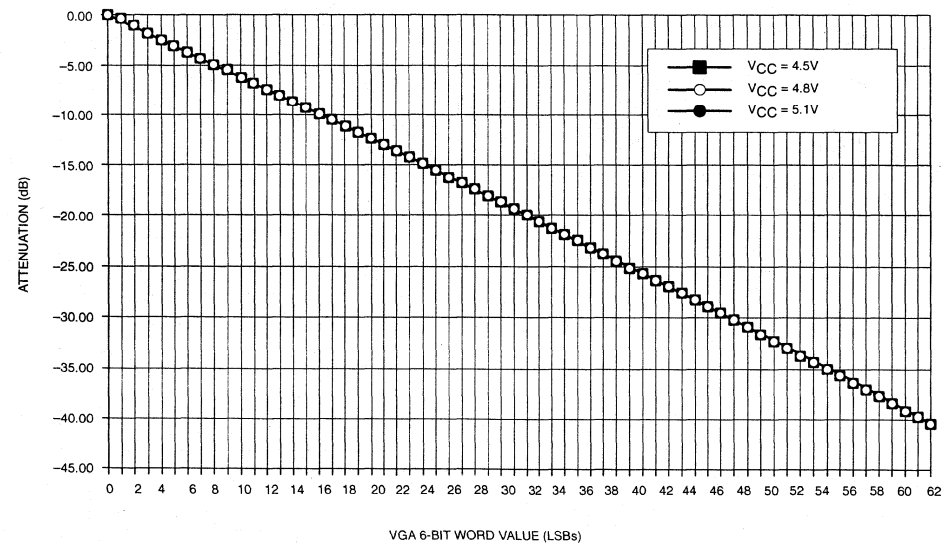
SR00648

Figure 13. Performance Characteristics

PERFORMANCE CHARACTERISTICS



DUALTX VGA Attenuation Profile vs. Temperature (V_{CC} = 4.8V, f = 836MHz, TXLO = −10dBm)



DUALTX VGA Attenuation Profile vs. V_{CC} (27°C, f = 836MHz, TXLO = −10dBm)

SR00649

Figure 14. Performance Characteristics

SA900 I/Q transmit modulator for 1GHz applications AN1892

Author: Wing S. Djen

INTRODUCTION

The SA900 (Figure 1) is a truly universal in-phase and quadrature (I/Q) radio transmitter that can perform many types of analog and digital modulation including AM, FM, SSB, QAM, BPSK, QPSK, FSK, etc. It is a highly integrated system which saves space and cost for the manufacturers producing cellular and wireless products. The device allows baseband signals to directly modulate the I/Q carriers, which are generated by internal phase shift network, in the 1GHz range, and to maintain good linearity required for linear modulation scheme (e.g., π/4-DQPSK). It contains an on-chip frequency divider, phase detector, and VCO, which can be built into a phase-locked loop (PLL) frequency synthesizer to create a transmit offset frequency. Its unique internal design allows frequency conversion without having an external image rejection filter for eliminating the sum term after mixing. The SA900 meets the specifications required by the IS-54, the industry standard for North America Digital Cellular (NADC) system. This application note reviews the basic concept of I/Q modulation and discusses the key points when designing the SA900 for an RF transmitter.

I/Q MODULATION

Any bandpass RF signals can be represented in polar form by

$$s(t) = A(t) \cos [\omega_c t + \phi(t)] \quad \text{(EQ. 1)}$$

where A(t) is the signal envelope and ϕ(t) is the phase. By using the trigonometric identities, we can represent EQ. 1 in rectangular form by

$$s(t) = I(t) \cos [\omega_c t] - Q(t) \sin [\omega_c t] \ , \quad \text{(EQ. 2)}$$

$$I(t) = A(t)\cos[\phi(t)]$$

$$Q(t) = A(t)\sin[\phi(t)]$$

Since the baseband signals I(t) and Q(t) modulate two exactly 90° out-of-phase carriers $\cos(w_c t)$ and $-\sin(w_c t)$ respectively, we call the system implementing EQ. 2 an in-phase and quadrature (I/Q) modulator. Figure 2 shows the mathematics and hardware implementation of an I/Q modulator.

The local oscillator, usually a VCO within a PLL, generates the carrier and is split into two equal signals. One goes directly into a double-balanced mixer to form the I-channel and the other one goes into the other mixer via a 90° phase shifter (realized by passive elements) to provide the Q-channel. The baseband signals I(t) and Q(t), either analog or digital in nature, modulate the carrier to produce the I and Q components which are finally combined to form the desired RF transmitting signal. Since any RF signal can be represented in the I/Q form, any modulation scheme can be implemented by an I/Q modulator.

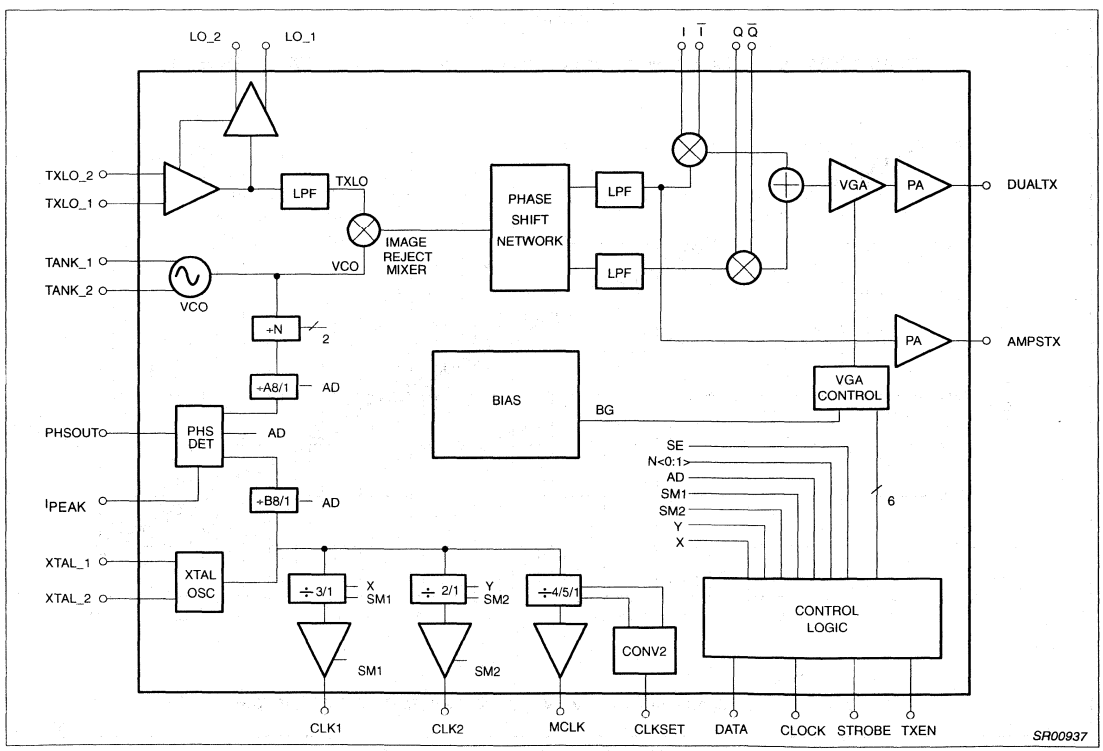


Figure 1. SA900 Transmit Modulator

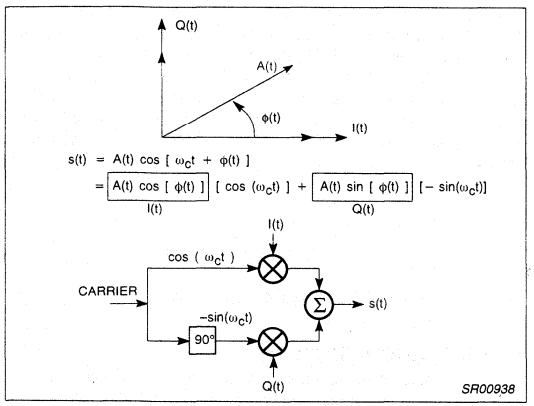


Figure 2. Mathematical Representation and Hardware Implementation of I/Q Modulator

Linear Digital Modulation

Linear digital modulation techniques depend on varying the phase and/or magnitude of an analog carrier according to some digital information: ones and zeros. This digital information can be the output of an analog-to-digital converter (e.g. voice codec), or it can be digital data in some standard formats (e.g. ASCII). The most popular digital signaling format is non return-to-zero (NRZ), where 1s and 0s are converted into signal with amplitude of 1 and -1, respectively, in a symbol duration. Since NRZ signal has infinite bandwidth, transmit filters have to be used to limit the spectral spreading. To ensure each NRZ symbol does not smear into its neighbors due to low-pass filtering and channel distortion causing inter-symbol interference (ISI), the frequency response of the low-pass filter has to satisfy Nyquist criteria. One example of this type of filter is the linear phase square-root-raised cosine filter. Together with the same type of filter for receive low-pass filtering, the signal is guaranteed ISI free in a Gaussian environment. One straight-forward technique of transmitting these bandlimited signals through communication channels would be applying it directly to the mixer of the I-channel to generate the RF signal. This is known as binary phase shift keying (BPSK), where the phase of the carrier is shifted 180° to transmit a data change from 0 to 1 or 1 to 0.

Quadrature or quaternary phase shift keying (QPSK) is a much more common type of modulation scheme used in mobile and satellite communications. It has four possible states (90° apart) and each of them represents two bits of data. Figure 3 shows the baseband generator for QPSK (without the differential phase encoder). NRZ data bits go through the serial-to-parallel converter (see Figure 4) and are mapped in accordance to some rules to generate I and Q values. The generic rule will be the values of I and Q components are 1 and 1 for the data bits "11" (45°) and -1 and -1 for the data bits "00" (-135°). These discrete signals have to be bandlimited by Nyquist low-pass filters to be ISI free.

A more sophisticated way of mapping results in $\pi/4$-DQPSK (D for differential encoding), which is chosen for North America Digital Cellular (IS-54), Personal Digital Cellular (PDC) in Japan, and Personal Handy Phone System (PHS) in Japan. In this scheme, consecutive pairs of bits are encoded into one of the four possible phases: $\pi/4$ for "11", $3\pi/4$ for "01", $-3\pi/4$ for "00", and $-\pi/4$ for "10".

However, unlike the previous case that "11" is always $\pi/4$ and "00" is always $-3\pi/4$, the encoded phases are the degrees that the carrier has to shift at each sampling instances. Thus, the information is contained in the phase difference (differential) instead of absolute phase for $\pi/4$-DQPSK.

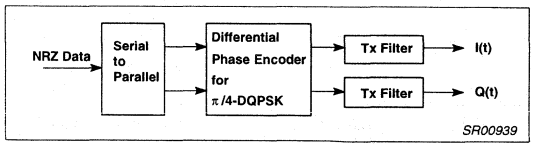


Figure 3. QPSK and $\pi/4$-DQPSK Baseband Generator

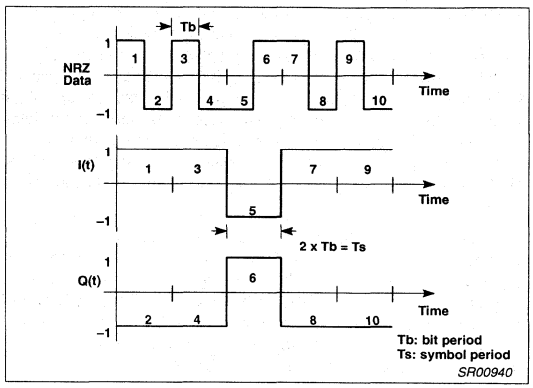


Figure 4. Serial-to-Parallel Conversion

A better way to tell the difference between QPSK and $\pi/4$-DQPSK is by looking at the signal constellation diagram, shown in Figure 5, which displays the possible values of I and Q vectors and change of states. Constellation diagram is also known as phase diagram because it shows the phase of the carrier at the sampling point. Notice that the phases of QPSK are assigned for every two bits of data; therefore, it can transmit twice as much information as BPSK in a given bandwidth, i.e., more bandwidth efficient. 8-PSK is another type of modulation used for high efficiency requirements. It maps three bits into 8 phases, 45° apart, in the constellation. More spectral efficient modulation can be created by mapping more bits into one phase at each sampling point. However, as you put more dots in the signal constellation, the signal susceptibility to noise is lower because the decision distance is shorter (dots are closer). Then, it requires higher carrier-to-noise (C/N) ratio to maintain the same bit error rate (BER).

One common misconception is that since $\pi/4$-DQPSK has 8 states in the constellation, it is just another type of 8-PSK. Notice that at every sampling instant, the carrier of $\pi/4$-DQPSK is only allowed to switch to one of the 4 possible states (see Figure 5). So, we still have two data bits which get encoded into 4 phases. Thus, it has the same spectral efficiency as QPSK for the same carrier power. The reason for using this modulation scheme is twofold. First, the envelope fluctuation, which causes spectral spreading due to nonlinearity of transmitter and amplifier, is reduced because the maximum phase shift is 135° instead of 180°. Second, the signal can be demodulated non-coherently which simplifies the receiver circuitry by eliminating the need for carrier recovery.

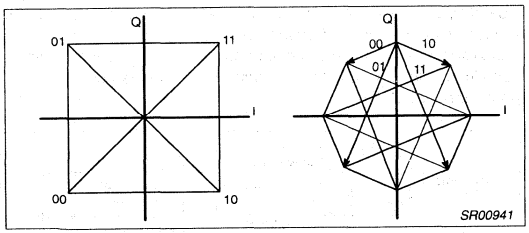


Figure 5. Signal Constellation of QPSK and π/4-DQPSK

Digital and Analog FM

Another family of digital modulation is categorized by frequency change of the carrier instead of phase and/or amplitude change. One of them is frequency shift keying (FSK), where the carrier switches between two frequencies. FSK is also known as digital FM because it can be generated by feeding the NRZ data stream into an analog VCO. FSK appears as a unit circle in the signal constellation because the RF signal envelope is constant and the phase is continuous. Baseband filtering is usually applied for FSK to limit the RF bandwidth of the signal so that more channels can fit into a given frequency band.

One common modulation of this type is known as Gaussian minimum shift keying (GMSK), which is used for GSM and some other wireless applications. GMSK can be generated by following its definition: bandlimit the NRZ data stream by a Gaussian low-pass filter, then modulate a VCO with modulation index (2 x frequency deviation/bit rate) set to 0.5. In other words, the single-sided frequency deviation is one fourth of the bit rate ($\Delta f = R/4$).

Another way of generating GMSK is by I/Q modulator. Referring back to EQ. 2, any RF signal can be split into I and Q components. Unlike the QPSK mentioned before, baseband I(t) and Q(t) are not discrete points for FM signals; rather, they are continuous functions of time. The way to produce FM is shown in Figure 6. We first store all the possible values of cos[φ(t)] and sin[φ(t)] in a ROM lookup table, which will be addressed by the incoming data to generate the I and Q samples. The output data from the ROM is then applied to D/A converters, after low-pass filtering for signal smoothing, to produce the analog baseband I and Q signals. This method guarantees the modulation index to be exactly 0.5, which is required for coherent detection of GMSK (e.g. GSM system). The same I/Q principle can also be applied to generating analog FM signals.

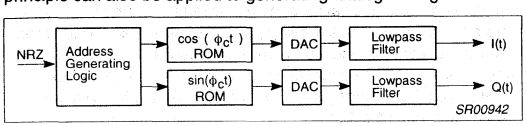


Figure 6. Digital FM (e.g. GMSK) Baseband I/Q Generator

Single sideband AM (SSB-AM)

AM signals can be divided into 3 types: the conventional AM, double sideband suppressed carrier AM (DSB-AM) and SSB-AM. The first type is not attractive because for 100% modulation, two-thirds of the transmit signal power appears in the carrier, which itself conveys no information at all. By using a balanced mixer (e.g. Gilbert cell), one can generate DSB-AM, where the carrier is totally suppressed and only the upper and lower sidebands are present. However, this is still not the best because the information is transmitted twice, once in each sideband. To further increase the efficiency of transmission, only one sideband is needed to deliver the information. The SSB-AM can be generated by an I/Q modulator with the baseband information feeding the modulator (by quadrature), as shown in Figure 7. This modulation technique can greatly reduce the bandwidth of the signal and allows more signals to be transmitted in a given frequency band. This topic is discussed in detail in Philips RF application note, #AN1981, "New low-power single sideband circuits".

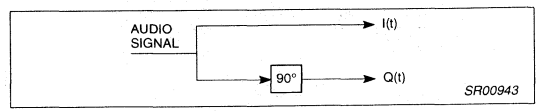


Figure 7. Baseband Processing for SSB-AM

SYSTEM ARCHITECTURE

There are usually two schemes, the dual conversion and direct conversion, used for implementing transmit modulators. Dual conversion is simpler to implement by modulating an oscillator at lower frequency and then up-converting to the carrier frequency. This scheme, however, is more expensive due to the need for additional filtering and more PC board space. By using only one mixer, direct conversion requires fewer components but is harder to implement.

The problems that direct conversion suffers are carrier leakage and modulated signal coupling. Poor RF isolation of the surface mount packages will allow the carrier to be present at the transmitter output thus making it difficult to have -40dBc carrier suppression. In addition to that, modulated RF signal would couple back to the oscillator (usually a VCO in a PLL synthesizer loop) and cause modulation distortion.

Based on the concept of dual conversion, the SA900 uses an image rejection mixer to eliminate the need for IF filtering and allow monolithic integration. The transmit carrier (LO) is down-converted by the frequency synthesized by the on-chip VCO, which operates from 90 to 140MHz. This LO is then modulated by the baseband I/Q signals to obtain a complex modulation scheme. The image (sum term) after mixing and LO is sufficiently suppressed by the image rejection mixer. Any residual amounts can be further suppressed by an external duplex filter.

Figures 8 and 9, respectively, show how the SA900 can be used in frequency division duplex (FDD) and time division duplex (TDD) transceivers. Notice that the LO for both systems is running at a frequency which is higher than the transmit frequency, thus minimizing carrier leakage. In the FDD system only one external VCO is required for generating both transmit and receive LO when using the SA900.

Figure 10 shows the IS-54 front-end chip set which consists of the SA601, SA7025, SA900, and SA637. This receiver architecture (SA637) supports a digital magnitude/phase baseband demodulator. An alternate configuration will be using the SA606 FM/IF receiver in conjunction with an external I/Q demodulator IC. The following table shows the possible configurations for the IS-54 handsets using the SA900 as transmitters.

Rx 1st IF	On-Chip VCO Frequency	On-Chip ÷N Value	Crystal Frequency
83.16MHz	128.16MHz	6	21.36MHz
71.64MHz	116.64MHz	6	19.44MHz
45MHz	90MHz	6	15MHz
84.6MHz	129.6MHz	9	14.4MHz

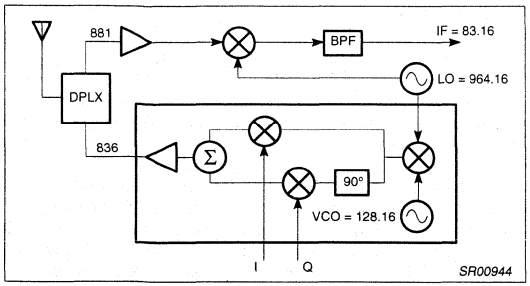


Figure 8. FDD System Using SA900

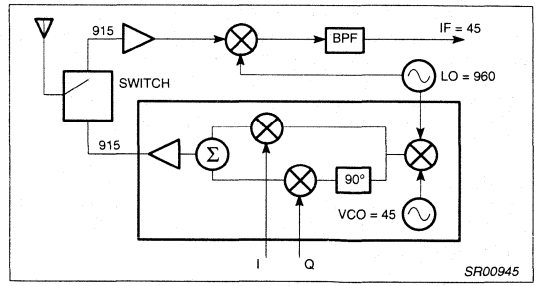


Figure 9. TDD System Using SA900

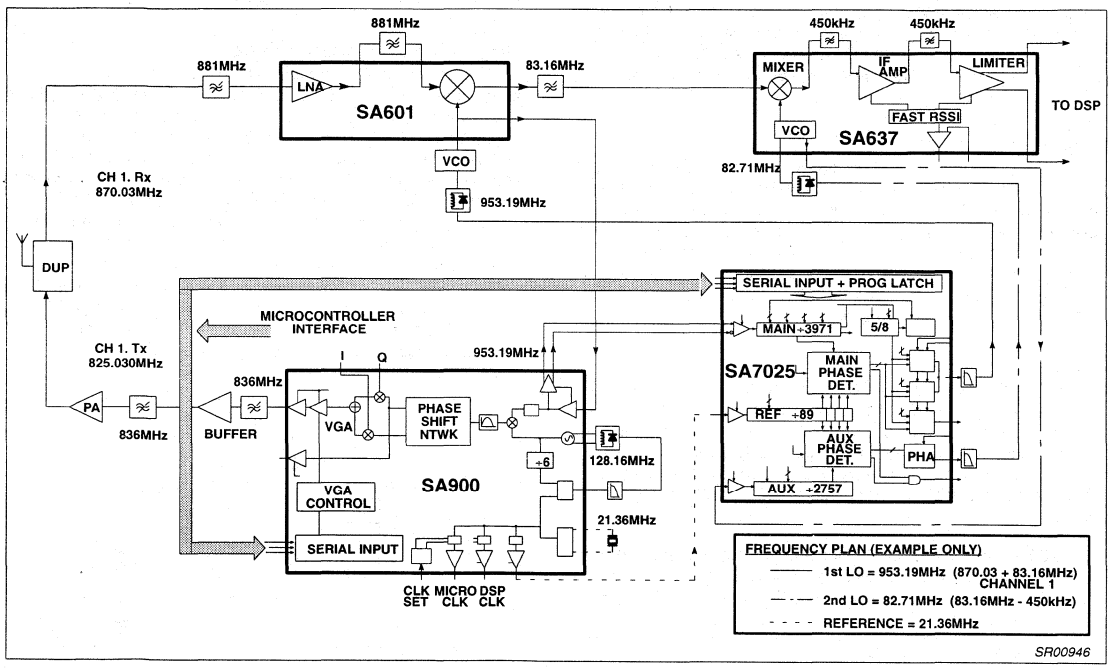


Figure 10. IS-54 front-end chip set from Philips

DESIGNING WITH THE SA900

Baseband I/Q Inputs

The baseband modulation inputs are designed to be driven differentially for the SA900 to operate at its best. The I and Q inputs should have a DC offset of V_{CC} /2, which is externally provided by common DSP chips. If all four inputs are biased from the same source, the device can tolerate $\pm 0.5V_{DC}$ error; however, inaccuracy of DC bias between I1/I2 or Q1/Q2 causes reduced suppression of the carrier. Thus, it is important to have a well regulated DC supply for I and Q signal biasing. The bandwidth of the inputs is much higher than the specified 2MHz. Approximately 2dB of power loss will be experienced if the I and Q inputs are 50MHz.

The SA900 generates a minimum of 0dBm of power to a 50Ω load when the amplitude of the I and Q signals are $400mV_{P-P}$. The output power will decrease by 6dB for every 50% decrease in I/Q amplitude. Single-ended I and Q sources can be used but are not recommended due to the degradation in carrier suppression (more than 10dB compared to differential). In addition, the entire noise performance of the device will suffer. V_{CC} /2 should be applied to I2 and Q2 pins if the part is driven single-endedly.

Transmit Local Oscillator

The transmit local oscillator path consists of a TXLO input buffer, LO output buffer, VCO, image rejection mixer and phase shift network. Together with a few external components, this section provides the I and Q carrier for modulation.

The TXLO inputs and LO outputs are designed to be used in an external PLL which synthesizes different frequencies for channel selection. The RF signal being generated is fed into TXLO inputs and then comes out of LO outputs to complete the system synthesizer loop. The TXLO inputs are differential in nature and

have a VSWR of 2:1 with input impedance of 50Ω. Single-ended sources can be used by AC grounding the TXLO_2, as done on the demoboard. This signal should also be AC coupled into the TXLO_1. The frequency range for these inputs is from 900 to 1040MHz while the input power should be between -10 to -13dBm. The output level will be changed significantly if the input level is below -25dBm.

The output power of the LO buffered signal changes by about 2dB when the SA900 is in a different mode of operation. Typical values are -13.5dBm and -15.5dBm for DUAL mode and STANDBY mode, respectively.

The 90° phase shift network, realized by RC networks, is capable of operating over a wide frequency range. Even though their frequency characteristics are optimized for cellular band, the part can also be used in other applications in a different band. In such cases, designers have to test the part experimentally to find out the performance, such as sideband suppression, carrier suppression, and image rejection.

Crystal Oscillator

The crystal oscillator (XTAL_1 and XTAL_2 pins) is used to provide reference frequency between 10 and 45MHz for the phase detector and the three on-chip clocks. It can be configured as a crystal oscillator using external crystal and capacitors, or it can be driven by an external source. In the latter case, pin XTAL_2 can be left floating. Information regarding crystal oscillator design can be found in Philips RF application note, #AN 1982, "Apply the Oscillator of the NE602 in Low-Power Mixer Applications."

VCO

The VCO, together with the phase detector, the divider and external low-pass filter, can form a PLL for the transmit offset frequency. The image reject mixer down-converts the TXLO signal to the RF carrier by the amount of VCO frequency. Thus, the TXLO frequency should be the desired channel frequency plus the IF offset generated by the VCO. Notice that the part will not function if the VCO section is not used.

The VCO is designed for generating IF frequency between 90MHz and 140MHz. Together with an external varactor diode and resonator, it can be configured as an oscillator as shown in Figure 11.

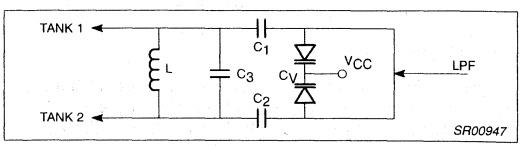


Figure 11. VCO Tank Circuit

The resonant frequency of such a circuit is

$$f_{VCO} = \frac{1}{2\pi\sqrt{LC_T}} \qquad \text{(EQ. 3)}$$

where $C_T = (C_1 // C_2 // C_V) + C_3$. C_V is a varactor diode of which capacitance changes linearly with the voltage across it.

Calculation:
$C_1 = C_2 = 33pF$
$C_3 = 5.6pF$
$C_V = 33.5pF$ @ 2.5V
$L = 100nH$

$C_T = 5.6 + (1/33 + 1/33 + 1/33.5)^{-1} = 16.7pF$

$$f_{VCO} = \frac{1}{2\pi\ (100e\text{-}9 \cdot 16.7e\text{-}12)^{0.5}} = 123MHz$$

On the demoboard, a 1:1 ratio RF transformer is also included to allow single-ended external source driving differential inputs when the VCO is not used.

When designing the VCO, careful PCB layout has to be made. Traces have to be short to avoid the parasitic capacitance and inductance which may cause unwanted oscillation. Referring to EQ. 3, there is a large combination of L and C_T values that will give the same resonant frequency. If undesired spurs are found in the design due to PCB layout, experimenting with a different set of LC values may sometimes solve the problem.

Output impedance matching

The equivalent output impedance at the DUALTX pin is approximately equal to 600Ω in parallel with 2pF at 830MHz. It has to be matched properly to generate maximum power into a 50Ω load (e.g. SAW filter). Figure 12 shows the recommended matching network. The shunt inductor (L1) is used to provide maximum swing at the output (short at DC) and also provide reactance to make the real impedance 50Ω looking into the matching network. The remaining negative reactance is canceled by the series inductor (L2). The values used on the demoboard can be used as a reference but may not be suitable if a different layout is implemented. The two shunt capacitors are included to bypass the high frequency RF signal, avoiding direct coupling into V_{CC}. The series AC coupling capacitor is used to maintain the proper bias for the output stage. Their values are big enough to be left out in impedance matching calculation.

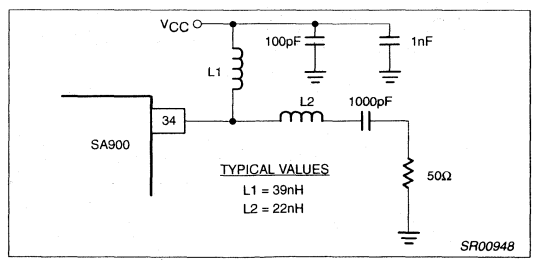


Figure 12. DUALTX Output Matching Network

Using a network analyzer to measure the S characteristic is necessary for obtaining optimum matching which generates maximum output power. Figure 13a-d shows how to match the output impedance to a 50Ω load at 915MHz. First, calibrate the network analyzer to the DUALTX SMA connector on the demoboard. Then, short the point where the series inductor is located and use the DELAY feature of the network analyzer to move the point of reference in the Smith Chart to the leftmost point. Now the network analyzer is calibrated to the beginning of the matching network, not just the SMA connector. The frequency response (Figure 13a) shows that the "dip" is around 830MHz, the frequency where the board was originally matched. The Smith Chart shows that it requires less inductance to bring the marker to the center of the chart (50Ω). By using a 15nH series inductor, the "dip" was moved closer to 915MHz (-15dB) and a better matching is achieved (Figure 13b).

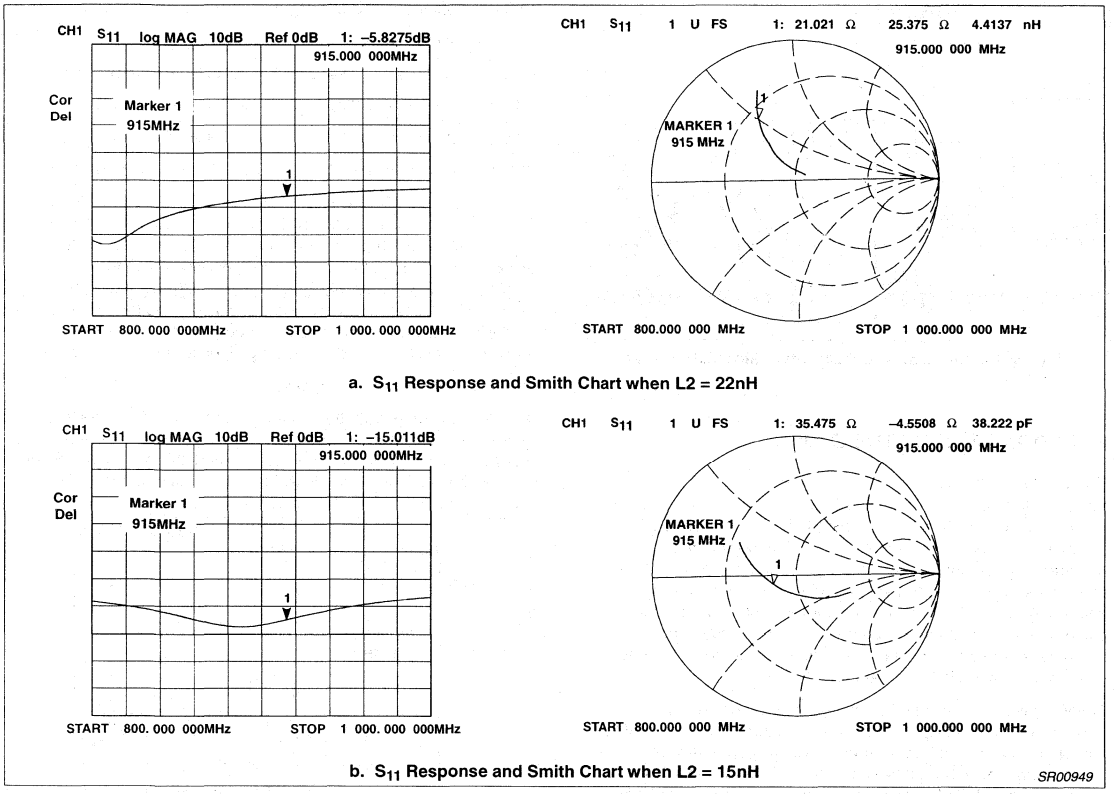


Figure 13.

On-Chip Clocks

The crystal oscillator is buffered to provide three external clock signals: CLK1, CLK2, and MCLK. Table 1 shows the divide ratio and the controlling mechanism:

Table 4.

CLK1	divide by 3	X (bit 18) = 1
	divide by 1	X (bit 18) = 0
CLK2	divide by 2	Y (bit 19) = 1
	divide by 1	Y (bit 19) = 0
MCLK	divide by 4	CLKSET pin = V_{CC}
	divide by 5	CLKSET pin = $V_{CC}/2$
	divide by 1	CLKSET pin grounded

CLK1 is usually used for the system synthesizer (e.g. SA7025) reference. Since MCLK is active all the time, it is ideal for providing the master clock for the microcontroller. When the device is in STANDBY mode, CLK1 and MCLK provide the clock signals necessary for receiving RF signals. CLK2 can also be used as a clock for digital signal processing (DSP) chip.

Modes of Operation

The SA900 is intended for either AMPS mode (analog cellular) or DUAL mode (digital cellular, IS-54) operation. When the device is running in AMPS mode, the I/Q modulator, variable gain amplifier (VGA) and phase shifter are disabled. The fixed gain amplifier is powered up during AMPS mode operation. However, since the divide ratio is too low (6, 7 or 8), the comparison frequency of the on-board PLL is too high, making it very difficult for the loop bandwidth to be less than 300Hz for analog FM modulation.

The device includes two power saving modes of operation which disable partial circuitry to reduce the power consumption of the overall chip. The SLEEP mode disables all the circuitry except the master clock (MCLK pin) of the SA900. The STANDBY mode shuts down everything except the TXLO buffer, MCLK, and CLK1, which allows the system synthesizer (e.g. SA7025) to continue running. These two power saving modes are common to both AMPS and DUAL mode operation. The SA900 draws 60mA in DUAL mode, reduced to 3mA and 8mA, respectively, in SLEEP and STANDBY modes.

TXEN pin is for hardware powering down the modulator and synthesizer. The falling edge of the signal disables the modulator and synthesizer while the rising edge enables the modulator. To power down the synthesizer using software, send a data word with SE bit set to '0' ('1' for enable). The synthesizer will be disabled right after the strobe signal is transmitted. Either SE or TXEN going low will turn off the synthesizer. This operation is common to both AMPS and DUAL mode.

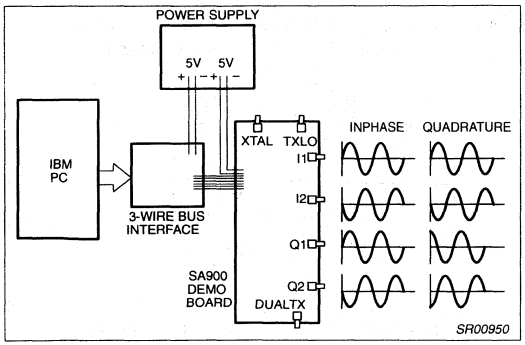


Figure 14. In-phase and Quadrature Modulation Test

PERFORMANCE OF THE SA900

Performance Criteria

Since the I/Q modulator is a universal transmitter, measuring only the frequency stability and modulation index of a generated FM signal would not be useful for other modulation schemes. Measurement parameters should be general enough so that they can represent the performance of modulators when applying different types of modulation and allow fair comparisons among different I/Q modulators. Based on this idea, two measurement techniques, in-phase modulation and quadrature modulation, are used for evaluating I/Q modulators.

The in-phase modulation relies on injecting two equal frequencies and phase signals at f_{mod} into the I and Q inputs. The result of this modulation is two sidebands appearing at f_{mod} offset from the carrier, with the carrier totally suppressed. This is also known as double-sideband (DSB) conversion. The quadrature modulation requires two equal frequencies (but 90° out-of-phase signals) being injected into the I and Q inputs. The result is a single-sideband suppressed carrier (SSB-SC) signal with either the upper or lower sideband at f_{mod} carrier offset being suppressed. This is also known as single-sideband (SSB) up-conversion. Figure 14 summarizes these two tests.

In a practical system, imperfection of an I/Q modulator is directly related to these two measurements. Sideband and carrier suppression from the quadrature modulation test will show the amount of gain imbalance, phase imbalance, and DC offset. On the other hand, intermodulation product suppression from the in-phase modulation test will show the linearity of an I/Q modulator. When making measurements, it is important to have well-balanced I and Q baseband modulating signals for measurement since the signal imperfection will translate into degradation in sideband and carrier suppression.

Performance Graphs

In making those measurements for the demoboard, the following parameters were used:

In-phase modulation:

PIN 43 I1=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=0°

PIN 42 I2=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=180°

PIN 41 Q1=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=0°

PIN 40 Q2=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=180°

Quadrature modulation:

PIN 43 I1=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=0°

PIN 42 I2=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=180°

PIN 41 Q1=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=90°

PIN 40 Q2=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=270°

Figures 15a and 15b illustrate what the typical output spectrum would be if in-phase and quadrature modulation were applied to an I/Q modulator. Quadrature modulation will produce lower sideband (LSB) or upper sideband (USB) signal, depending on the phase angle between the I and Q signals. The SA900 was designed to have USB suppressed when the I signal is leading the Q signal. The undesired signals are carrier breakthrough and the harmonic products of the baseband modulating signals sitting at

$f_c \pm nf_{mod}$, where n is an integer ≥2.

Referring to Figure 15a, the output power is 1.3dBm (cable loss = 0.7dB) for the LSB while better than -38dBc of carrier, sideband, and harmonics suppression is measured. The USB better than -26dBc implies the residual AM of the transmit signal is better than 5%, a requirement of the IS-54 specification.

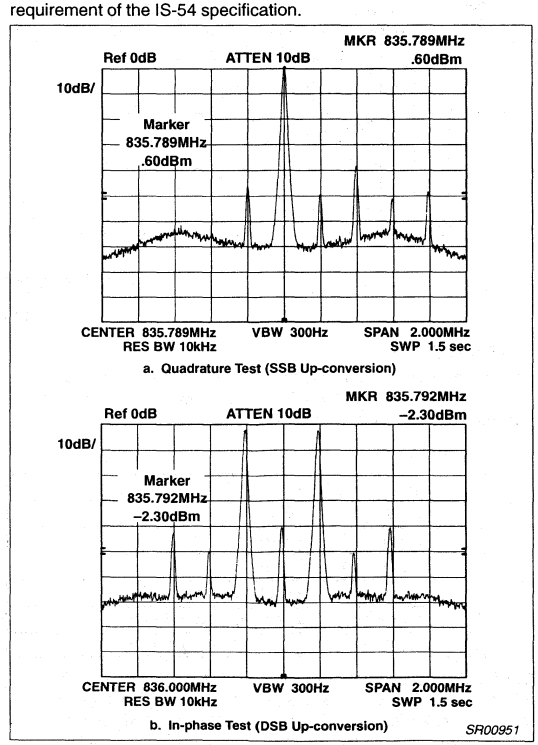


Figure 15.

In-phase modulation test will generate both LSB and USB. Beside these two tones, the carrier breakthrough and the harmonics, intermodulation (IM) products will all appear at the output. The odd IM products are dominant, and they satisfy the following rules:

Let $f_1 = f_c - f_{mod}$, $f_2 = f_c + f_{mod}$

3rd order IM:	$2f_1 - f_2 = f_c - 3f_{mod}$,	$2f_2 - f_1 = f_c + 3f_{mod}$
5th order IM:	$3f_1 - 2f_2 = f_c - 5f_{mod}$,	$3f_2 - 2f_1 = f_c + 5f_{mod}$
7th order IM:	$4f_1 - 3f_2 = f_c - 7f_{mod}$,	$4f_2 - 3f_1 = f_c + 7f_{mod}$

Referring to Figure 15b, both LSB and USB are -1.6dBm (cable loss = 0.7dB) in power, which is 3dB less than the measured power for the quadrature modulation test. The IM3 is better than -35dBc. Much higher order IM products are totally suppressed.

Amplitude and phase unbalance

Both amplitude and phase unbalance (error) of an I/Q modulator can be calculated directly from the SSB performance plots. Assume phase error equals ϕ radian and amplitude error equals K, the sideband suppression, X, in dBc can be expressed as follows (see APPENDIX for derivation):

$$\text{SSB suppression, } X(\text{dBc}) = 10\log\left(\frac{K^2 + 2\cdot K\cdot\cos(\phi) + 1}{K^2 - 2\cdot K\cdot\cos(\phi) + 1}\right) \quad \text{(EQ. 4)}$$

Collecting the like terms and express ϕ in terms of K and X, it becomes:

$$\phi = \cos^{-1}\left(\frac{10^{X/10}\cdot K^2 + 10^{X/10} - 1 - K^2}{2\cdot K + 2\cdot K\cdot 10^{X/10}}\right) \quad \text{(EQ. 5)}$$

For a given X, there will be a set of ϕ and K that satisfies EQ. 5. We can represent this relationship graphically, as shown in Figure 16. The contours show the phase and amplitude errors for SSB suppression, X, from -44 to -26dBc. When X equals -40dBc, phase error is less than 1.2° with a 0dB amplitude error. By the same token, the amplitude error is less than 0.2dB with a 0° phase error.

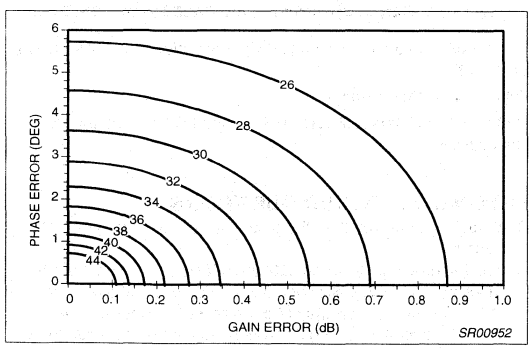


Figure 16. SSB Suppression Contours

Spectral mask

To fully characterize the performance of an I/Q modulator, measurements of the power spectral density of various digital modulation schemes have to be made. Figures 17a and 17b show the measured spectral masks of IS-54 and PDC standards, which designate $\pi/4$-DQPSK as the modulation format.

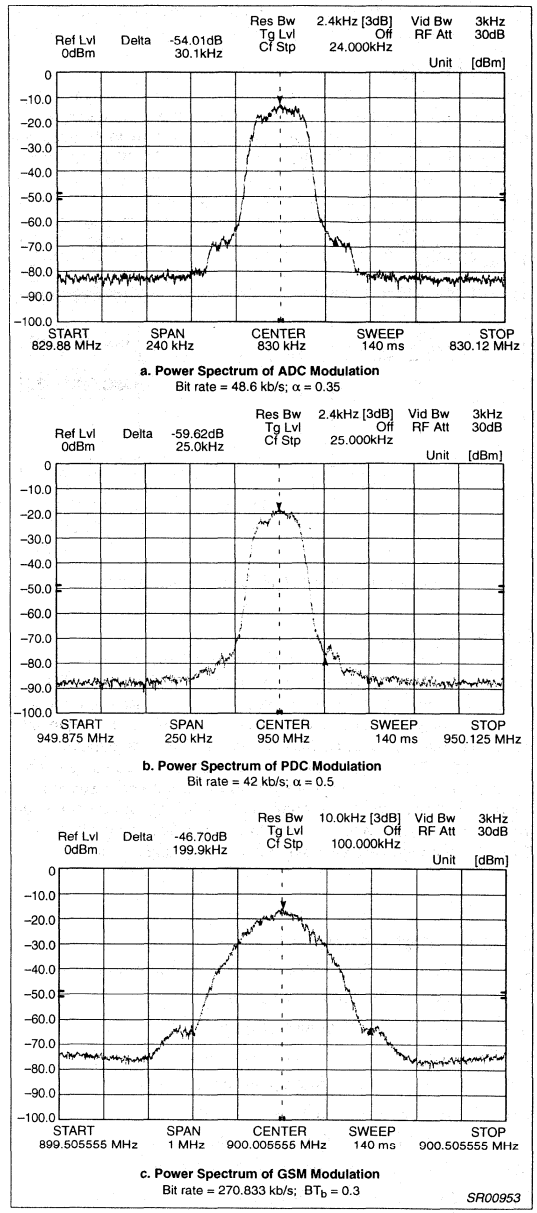


Figure 17.

GMSK is a digital modulation scheme widely used for wireless and mobile communications. Figure 17c shows the spectral mask of the modulation format required by GSM, the digital cellular standard in Europe. At 200kHz and 300kHz carrier offset, the power of the

signal is suppressed by 46dB and 58dB, respectively, which is well within the GSM specification.

Power ON time

The power ON time for the SA900 is mainly determined by the loop bandwidth of the on-board PLL frequency synthesizer. It can be measured by using the HP 53310A Modulation Domain Analyzer set to the EXTERNAL TRIGGERED mode. The STROBE signal from 3-wire bus is used to trigger the equipment. Figure 18 shows that the part can be powered up and locked in about 62µs.

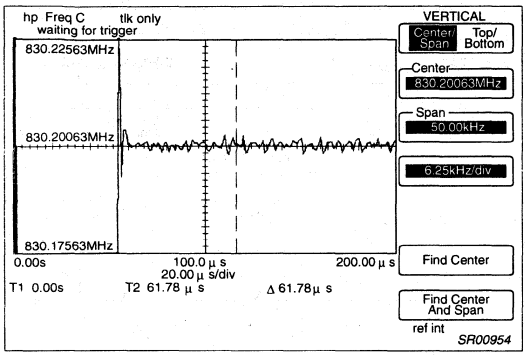


Figure 18. Power ON Time Measurement

ISM band application

The FCC has recently assigned three bands for ISM type of application. The one below 1GHz is from 902 to 928MHz. This band becomes very attractive because users are allowed, without having a license, to transmit up to 1 Watt of power when frequency hopping or direct sequence CDMA is used. The wide bandwidth nature of the SA900 fits well into this application. Figures 19a and 19b are the output spectrum of the SA900 showing how well the image reject mixer works. A common IF (45MHz) was chosen to be the offset frequency, and then injected externally into the VCO pins. The closest images are sitting at 45MHz apart and are better than -36dBc.

COMPONENTS FUNCTION

C241, C242, C243, C245, C246 - Supply bypassing capacitors

C247 - provides AC ground for TXLO2 pin

C249 - AC couples an external signal into TXLO1 pin

C253, C254, C255 - part of the LC tank circuit

C263 - AC couples an external signal into XTAL1 pin

C267, C269 - part of the PLL low-pass filter

C281, C287, C288 - AC coupling capacitors for the clocks

C301 - AC coupling capacitor for the DUALTX pin

C305, C306 - Bypass RF signal coming from DUALTX pin

C312, C313, C314 - AC coupling capacitors

C370, C371 - AC couples an external signal into TANK1 and TANK2 pins when on-board PLL is not used

L252 - part of the LC tank circuit

L304, L372 - matching network for the DUALTX output

R260 - termination resistor

R262 - current setting resistor for the charge pump

R264, R266 - part of the PLL low-pass filter

R274 - jumper

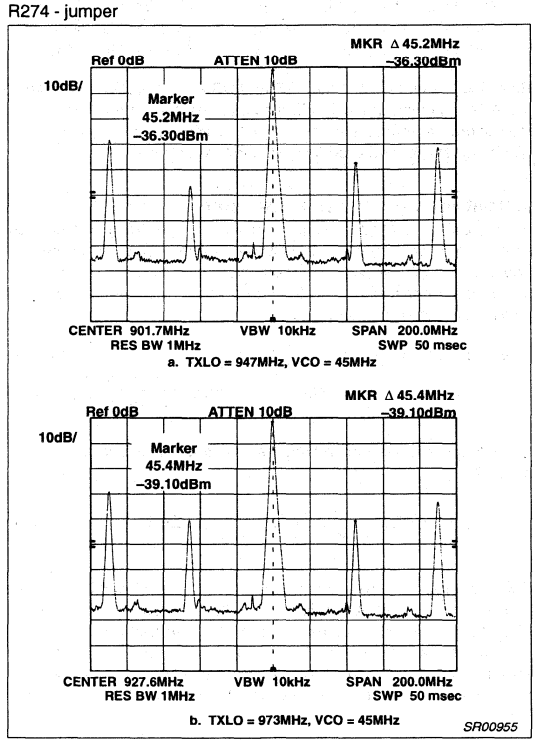


Figure 19. Output Spectrum of the SA900 in the ISM Band

R349, R350 - make up a voltage divider for selecting divide ratio of the MCLK

R352 - termination resistor

R333, 358 - isolation resistors between the LC tank and the PLL low-pass filter

FREQUENTLY ASKED QUESTIONS

Q. What is the bandwidth of the phase shifter for generating I/Q carriers?

A. The bandwidth is between 820 and 920MHz. The part is still functional below 820MHz and above 920MHz, but the carrier and sideband suppression are not guaranteed. In addition, the DUALTX output matching network needs to be optimized for a different frequency.

Q. Can I frequency modulate (FM) the on-board VCO to generate RF signal for AMPS system?

A. Since the divide ratio for the VCO is too low, it is very difficult to obtain the required loop bandwidth (<300Hz) to do AMPS modulation.

Q. What signals constitute the spurious output referred to under the DUALTX function of the AC electrical characteristics in the data sheet?

A. Those spurs could be N*TXLO, N*VCO, TXLO+VCO, N*XO, and TXLO ±N*VCO.

Q. Can external circuitry be added or modified to reduce the broadband noise floor below -136dBm/Hz?
A. Customers can put a bandpass SAW filter at the output of the TXLO to improve the broadband noise floor.

Q. Can the SA900 generate BPSK signal?
A. Yes, it can. Feed the baseband signal into I1 and I2 and leave Q1 and Q2 open or tie them to V_{CC} /2.

Q. What is the response of the image rejection filter?
A. It is actually a SSB mixer; not an image rejection filter.

Q. What happens if the VCO is not used?
A. There will not be any signal at the DUALTX and AMPS output if the VCO is not used.

REFERENCES:

"Implementation of a 900 MHz Transmitter System Using Highly Integrated ASIC", Wing S. Djen and Prasanna M. Shah, Proceedings of the 44th IEEE Vehicular Technology Conference, June 1994, pp. 1341-1345.

"Digital and Analog Communications Systems," Leon W. Couch II, Macmillan, 1990.

"Cellular System Dual-Mode Mobile Station-Base Station Compatibility Standard", IS-54-B, EIA/TIA, April 1992.

"Physical Layer on the Radio-Path", GSM Standard, July 1988.

"π/4-QPSK MODEMS for Satellite Sound/Data Broadcast Systems", Chia-Liang Liu and Kamilo Feher, IEEE Transactions on Broadcasting, March 1991, pp. 1-8.

"PCD5070 GSM Baseband Interface", Preliminary specification, Philips Semiconductors, September, 1992.

APPENDIX

Assume an imperfect I/Q modulator with gain error, K, and phase error, ϕ, modulated by quadrature I/Q signals (SSB up-conversion) wm. Then the signal, s(t), at the output of the I/Q modulator becomes,

$$s(t) = K\cos(\omega_c t + \phi)\cos(\omega_m t) - \sin(\omega_c t)\cos(\omega_m t + 90^o) \quad \text{(EQ. A.1)}$$

Using trigonometric identity and let $\omega c - \omega_m = A$ and $\omega_c + \omega_m = B$, we obtain,

$$s(t) = \frac{K}{2}\cos[At + \phi] + \frac{K}{2}\cos[Bt + \phi] + \frac{1}{2}\cos[At] - \frac{1}{2}\cos[Bt] \quad \text{(EQ. A.2)}$$

Assume the information is in LSB, i.e. A, and the spur is the USB, i.e., B, we have,

$$\text{Signal} = \frac{K}{2}\cos A\cos\phi + \frac{1}{2}\cos A - \frac{K}{2}\sin A\sin\phi \quad \text{(EQ. A.3)}$$

$$\text{Noise} = \frac{K}{2}\cos B\cos\phi + \frac{1}{2}\cos B - \frac{K}{2}\sin B\sin\phi \quad \text{(EQ. A.4)}$$

To find the power, we have to evaluate the envelope (amplitude) of these two signals. Recall that for any given bandpass signal in rectangular form,

Bandpass signal = X cos ωt - Y sin ωt,

the envelope is

Envelope = $(X^2 + Y^2)^{0.5}$

Therefore, from EQ. A.3 and A.4,

$$\text{Signal} = \left[\left(\frac{K}{2}\cos\phi + \frac{1}{2}\right)^2 + \left(\frac{K}{2}\sin\phi\right)^2\right]^{0.5} \quad \text{(EQ. A.5)}$$

$$\text{Noise} = \left[\left(\frac{K}{2}\cos\phi - \frac{1}{2}\right)^2 + \left(\frac{K}{2}\sin\phi\right)^2\right]^{0.5} \quad \text{(EQ. A.6)}$$

Finally, the S/N ratio can be found by taking 20 log the ratio of EQ. A.5 and A.6.

$$\frac{S}{N} = 10\log\left(\frac{K^2 + 2K\cos\phi + 1}{K^2 - 2K\cos\phi + 1}\right)$$

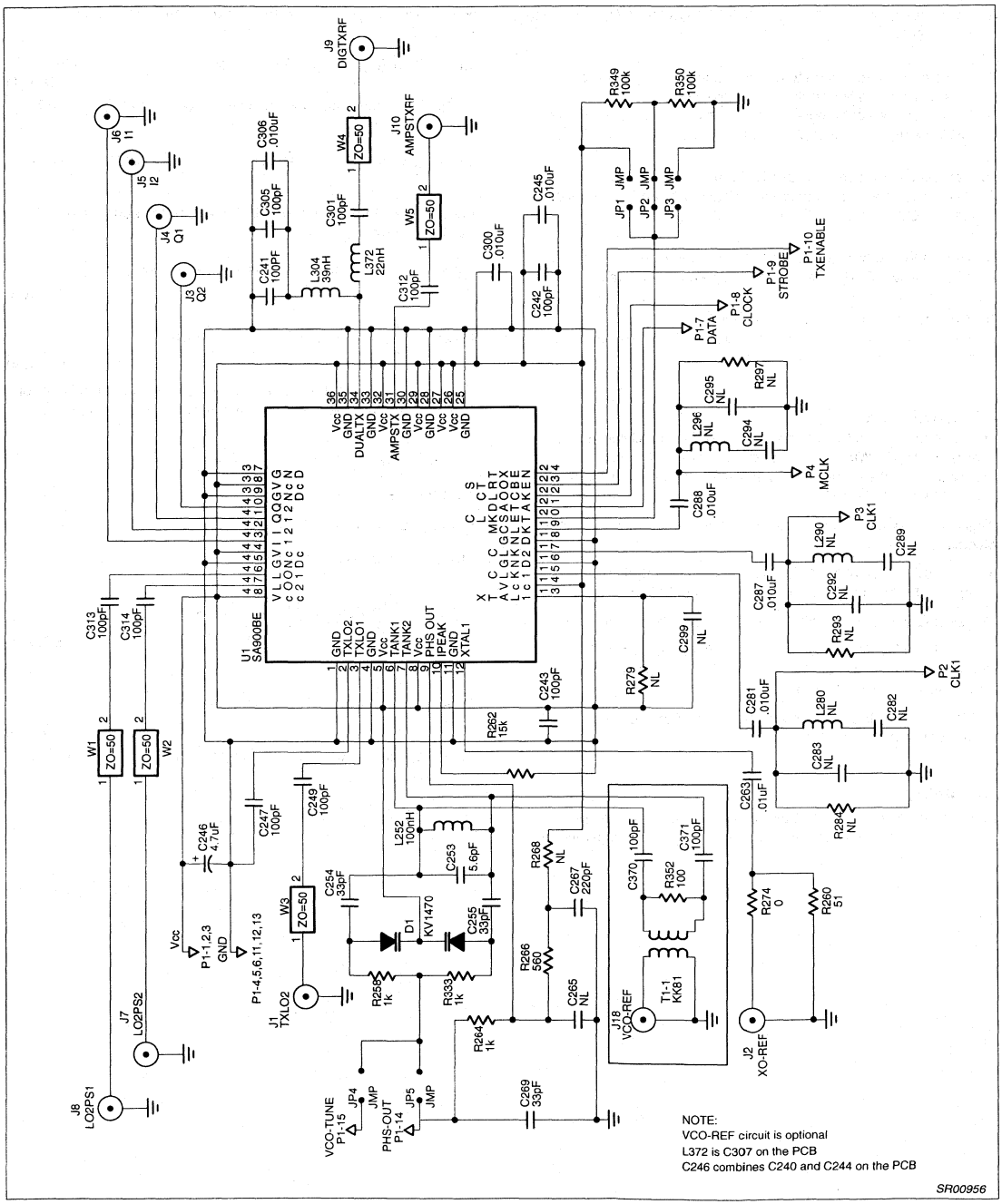


Figure 20. SA900 Demoboard

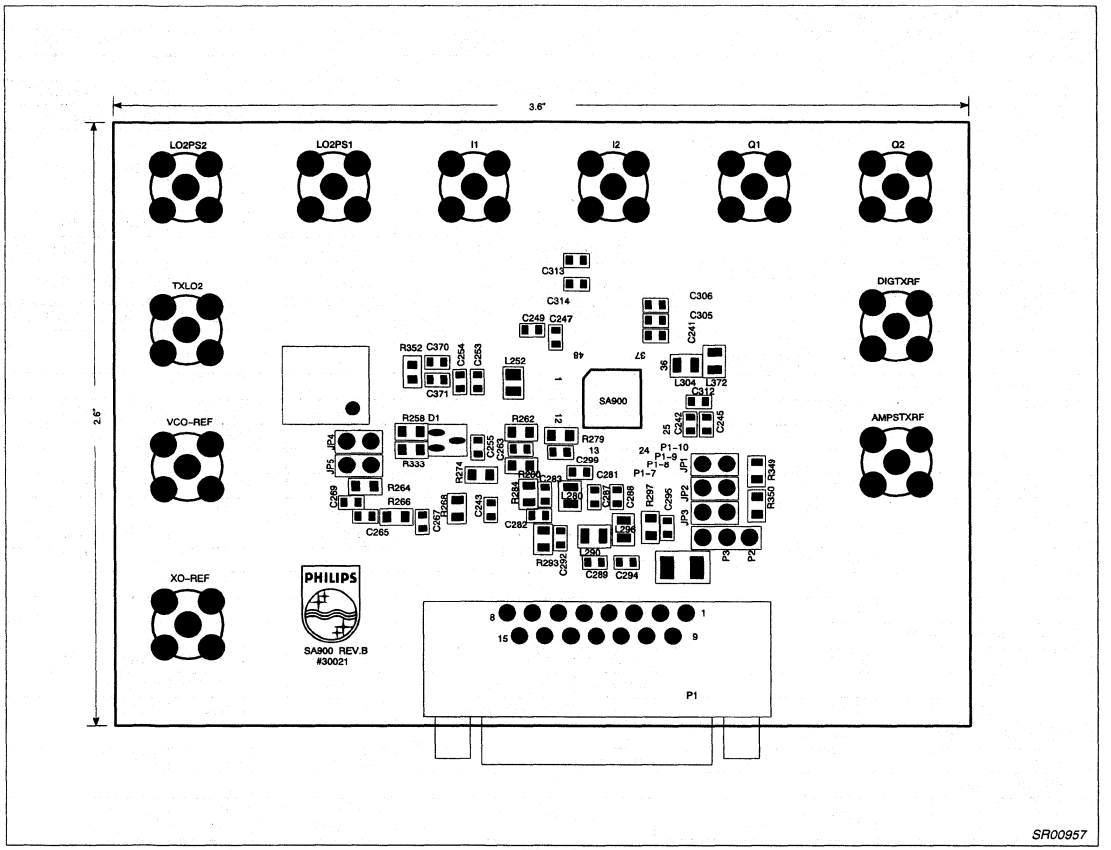


Figure 21. SA900 Board Layout

Table 5. Customer Application Component List for SA900BE

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	5.6pF	50V	C253	Cap. cer. 0603 NPO ±0.25pF	Garrett	Rohm	MCH185A5R6CK
3	33pF	50V	C254, C255, C269	Cap. cer. 0603 NPO ±5%	Garrett	Rohm	MCH185A330JK
13	100pF	50V	C241, C242, C243, C247, C249, C300, C301, C305, C312, C313, C314, C370, C371	Cap. cer. 0603 NPO ±5%	Garrett	Rohm	MCH185A101JK
1	1000pF	50V	C301	Cap. cer. 0603 X7R ±10%	Garrett	Rohm	MCH185C102KK
1	2200pF	50V	C267	Cap. cer. 0603 X7R ±10%	Garrett	Rohm	MCH185C222KK
6	0.01µF	25V	C245, C263, C281, C287, C288, C306	Cap. cer. 0603 X7R ±10%	Garrett	Philips	MCH182C103KK
1	4.7µF	10V	C246	Tant. chip cap. B 3528 ±10%	Garrett	Philips	49MC475B010KOAS
8	NL		C265, C282, C283, C289, C292, C294, C295, C299				
Surface Mount Resistors							
1	0Ω		R274	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW000E
1	51Ω		R260	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW510E
1	100Ω		R352	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW101E
1	560Ω		R266	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW561E
1	1KΩ		R258, R264, R333	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW102E
1	15KΩ		R262	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW153E
2	100KΩ		R349, R350	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW104E
Surface Mount Diodes							
1			D1	SMD Diode (Varactor)	Digikey	TOKO	KV1470TR00
Surface Mount Inductors							
1	0.022µH		L372	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R022M
1	0.039µH		L304	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R039M
1	0.10µH		L252	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R10M
Surface Mount Integrated Circuits							
1			U1	I/Q Transmit modulator	Philips	Philips	SA900BE
Miscellaneous							
1			K353	RF Transformer	Mini-Circuits	Mini-Circuits	T1-1 KK81
11			J1, J2, J3, J4, J5, J6, J7, J8 ,J9, J10, J18	SMA Right Angle Jack Receptacle	Newark	EF Johnson	142-0701-301
5			JP1, JP2, JP3, JP4, JP5	straight, dual row	Newark	IPI	929836-01-36-ND
1			P1	15 pins receptacle D-sub. conn.	Newark	Dupont	51F2456
1				Printed circuit board	Philips	Philips	SA900-30021
66 Total Parts							

Variable gain RF predriver amplifier SA910

DESCRIPTION

The SA910 is a variable gain predriver amplifier designed for handheld analog cellular telephones. When used with the Philips BLT61 UHF power transistor, it forms a cost-effective, low-profile, surface mount power amplifier solution (+32 with 55% efficiency +32dBm). The SA910 integrates power detection and control circuitry that is stabilized over temperature and voltage. In power down mode, the SA910 draws less than 10µA of current. The SA910 is fabricated using Philips QUBiC BiCMOS process.

FEATURES

- MMIC BiCMOS predriver amplifier
- Low voltage 2.7 to 5.5V single supply operation
- 820 to 905MHz bandwidth
- High power gain >20dB
- High power output >23dBm (typical) @ 3V
- Efficiency >35% (typical)
- Wide gain control range: >32dB
- Few external components required
- Integrated power detector and comparison gain control circuitry
- 50Ω input, open-collector output
- SSOP-20 package
- Integrated regulator with offset adjustment for biasing an external output stage

PIN CONFIGURATION

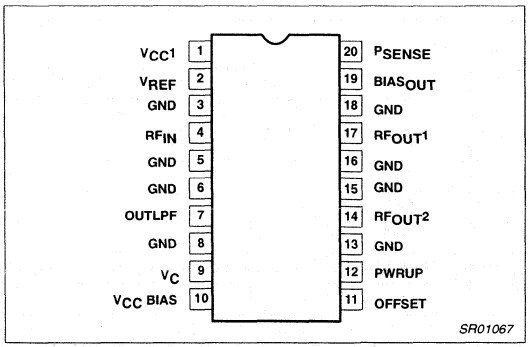


Figure 1. Pin Configuration

- Powerdown I_{CC} < 0.5µA

APPLICATIONS

- 900MHz analog cellular
- Handheld transmitting equipment in the 820 to 905MHz frequency range

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic SSOP (Shrink Small Outline Package)	-40 to +85°C	SA910	SOT266-1

BLOCK DIAGRAM

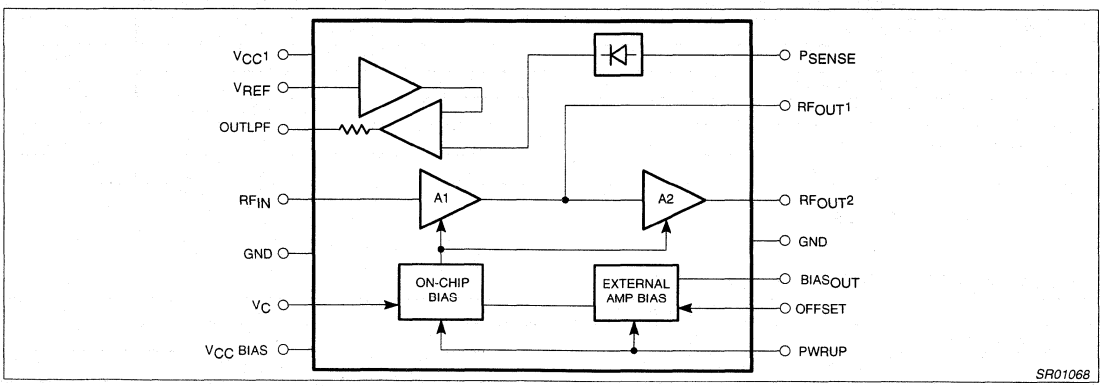


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$V_{CC}1$	Power supply for power sense loop and off-chip bias
2	V_{REF}	Power sense reference voltage input
3	GND	Ground
4	RF_{IN}	Pre-driver input
5	GND	Ground
6	GND	Ground
7	OUTLPF	Power sense detected output
8	GND	Ground
9	VC	Gain control input
10	V_{CC} BIAS	Power supply for on-chip bias
11	OFFSET	External power amp bias offset adjustment
12	PWRUP	Power-up input
13	GND	Ground
14	$RF_{OUT}2$	Pre-driver output
15	GND	Ground
16	GND	Ground
17	$RF_{OUT}1$	Output of first stage
18	GND	Ground
19	$BIAS_{OUT}$	Output to bias external power amplifier stage
20	P_{SENSE}	Power sense input

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC}1/V_{CC}$BIAS	DC supply voltages	-0.3 to +6.0	V
	Voltage applied to any other pin[1]	-0.3 to ($V_{CC}1$ + 0.3)	V
P_D	Power dissipation	1.5	W
P_{IN}	Input drive power	5	mW
P_{DET}	Input detect power	20	mW
P_L	Load power	500	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Except $RF_{OUT}1$ and $RF_{OUT}2$ which can have 8V max.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC}1/V_{CC}$BIAS	Supply voltage	3 to 3.6	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	<125	°C

AC ELECTRICAL CHARACTERISTICS

$V_{CC}1 = V_{CC}BIAS = +3V; V_{CC}(RF_{OUT}1, RF_{OUT}2) = 3.6V$; $T_A = 25°C$, $Z_S = Z_L = 50\Omega$; $V_C = 2V$; $RF_{IN} = 1mW$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
f_{RF}	Frequency range		820	830	905	MHz
P_L	Load power at $RF_{OUT}2$	Saturated[1]		24.5		dBm
S_{21}	Small signal gain			31		dB
η	Efficiency	P_L = 23dBm		35		%
S_{11}	Return loss	Small signal input		–12		dBm
G_C	Gain control from V_c.	dP/dV <120dB/V	32			dB
S_{12}	Reverse isolation			-40		dB
GOFF	Gain at RF_{OUT2} during power-down (RF_{IN} = -20dBm)			-30		dB
PSENSE	Power detector range		-28	25	0	dBm

NOTE:
1. Needs proper matching.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}1 = V_{CC}BIAS$ = +3V, V_{CC} ($RF_{OUT}1$, $RF_{OUT}2$) = 3.6V; $T_A = 25°C$, $Z_S = Z_L = 50\Omega$, ; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-3σ	TYP	+3σ	MAX	
V_{CC}	Power supply voltage range		2.7		3.0		5.5	V
I_{CC}	Total DC current from all V_{CC}	Pin 12 = HIGH; Pin 9 > V_{BE}					300	mA
I_{2B}	I_{CC} under zero bias mode	Pin 12 = HIGH; Pin 9 < V_{BE}					0.3	mA
I_{OFF}	Powerdown current	Pin 12 = low			0.5			µA
I_{PU}	Input current to PWRUP	Pin 12 = HIGH					100	µA
		Pin 12 = LOW					0	
V_{PU}	Input level for PWRUP (Pin 12)	Pin 12 = LOW	0				$0.3V_{CC}$	V
		Pin 12 = HIGH	$0.7V_{CC}$				V_{CC}	V
I_{REF}	Input current to V_{REF} (Pin 2)						1	µA
V_{REF}	Power control reference voltage (Pin 1)		0				2.0	V
V_{BIAS}	Bias-OUT voltage (Pin 19)	$V_C \geq 0.7V$			0.6			V
I_{BIAS}	DC current available @ Bias-OUT (Pin 19)		50					mA
V_C	Control voltage (Pin 9) range		0				2	V
I_{VC}	Input current to VC (Pin 9)						0.5	mA
t_{ON}	Power up time				20			µs
t_{OFF}	Power down time				20			µs
	Power up settling time				100			µs

GSM 4 W power amplifiers CGY2010G; CGY2011G

FEATURES

- Power Amplifier (PA) overall efficiency 45%
- 35.5 dB gain
- 0 dBm input power
- Gain control range >55 dB
- Integrated power sensor driver
- Low output noise floor of PA < −129 dBm/Hz in GSM RX band
- Wide operating temperature range −20 to +85 °C
- LQFP 48 pin package
- Compatible with power ramping controller PCA5075
- Compatible with GSM RF transceiver SA1620.

GENERAL DESCRIPTION

The CGY2010G and CGY2011G are GSM class 4 GaAs Monolithic Microwave Integrated Circuits (MMICs) power amplifiers specifically designed to operate at 4.8 V battery supply. These ICs also include a power sensor driver so that no directional coupler is required in the power control loop.

Both ICs have the same performance but are issued from different wafer fabs.

The PAs require only a 30 dB harmonic low-pass filter to comply with the GSM transmit spurious specification. They can be switched off and their power controlled by monitoring the actual drain voltage applied to the amplifier stages.

APPLICATIONS

- 880 to 915 MHz hand-held transceivers for E-GSM applications
- 900 MHz TDMA systems.

QUICK REFERENCE DATA

SYMBOL	PARAMETER (1)	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	4.2	–	V
I_{DD}	positive peak supply current	–	1.8	–	A
$P_{out(max)}$	maximum output power	–	35.5	–	dBm
T_{amb}	operating ambient temperature	−20	–	+85	°C

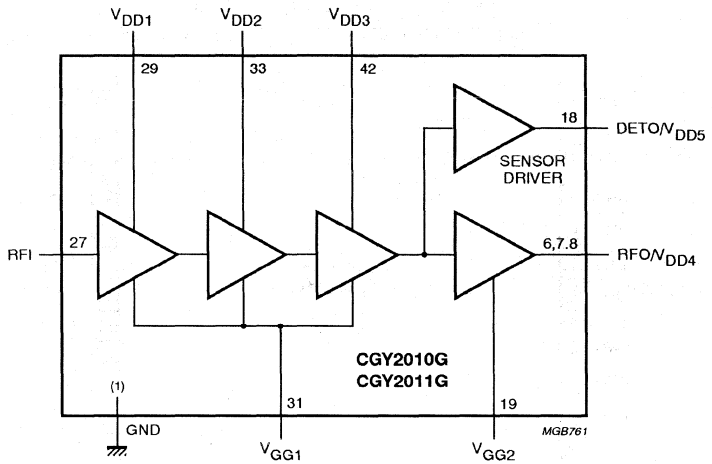
Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2010G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
CGY2011G			

BLOCK DIAGRAM



(1) Ground pins 1 to 5, 9 to 17, 20 to 26, 28, 30, 32, 34 to 41 and 43 to 48.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 5	ground
RFO/V_{DD4}	6 to 8	power amplifier output and fourth stage supply voltage
GND	9 to 17	ground
DETO/V_{DD5}	18	power sensor output and supply voltage
V_{GG2}	19	fourth stage negative gate supply voltage
GND	20 to 26	ground
RFI	27	power amplifier input
GND	28	ground
V_{DD1}	29	first stage supply voltage
GND	30	ground
V_{GG1}	31	first three stages negative gate supply voltage
GND	32	ground
V_{DD2}	33	second stage supply voltage
GND	34 to 41	ground
V_{DD3}	42	third stage supply voltage
GND	43 to 48	ground

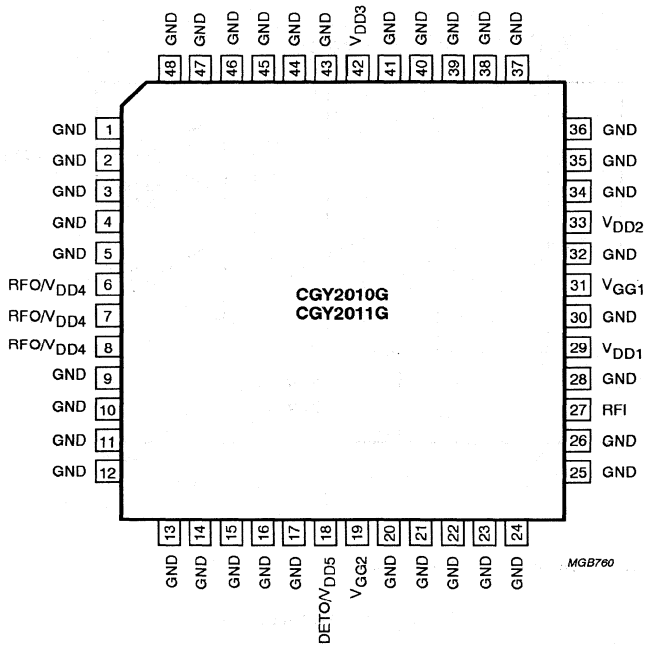


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating conditions

The CGY2010G and CGY2011G are designed to meet the European Telecommunications Standards Institute (ETSI) GSM documents, the *"ETS 300 577 specification"*, which are defined as follows:

- t_{on} = 542.8 µs
- T = 4.3 ms
- Duty cycle = 1/8

The devices are specifically designed for pulse operation allowing the use of a LQFP48 plastic package.

Power amplifier

The power amplifier consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

The amplifier bias is set by means of a negative voltage applied at pins V_{GG1} and V_{GG2}. This negative voltage must be present before the supply voltage is applied to the drains to avoid current overstress for the amplifier.

Power sensor driver

The power sensor driver is a buffer amplifier that delivers a signal to the DETO output pin which is proportional to the amplifier power. This signal can be detected by external diodes for power control purpose. As the sensor signal is taken from the input of the last stage of the PA, it is isolated from disturbances at the output by the reverse isolation of the PA output stage.

Impedance mismatch at the PA output therefore, does not significantly influence the signal delivered by the power sensor as this normally occurs when power sense is made using a directional coupler. Consequently the cost and space of using a directional coupler are saved.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	7	V
V_{GG}	negative supply voltage	–	−10	V
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
T_{stg}	IC storage temperature	–	150	°C
P_{tot}	total power dissipation	–	1.5	W

THERMAL CHARACTERISTICS

General operating conditions applied.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case; note 1	32	K/W

Note

1. This thermal resistance is measured under GSM pulse conditions.

DC CHARACTERISTICS

V_{DD} = 4.5 V; T_{amb} = 25 °C; general operating conditions applied; peak current values during burst; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	positive supply voltage		0	4.2	5.5	V
I_{DD}	positive peak supply current		–	1.8	2.2	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	–	–2	–	V
V_{GG2}	negative supply voltage	note 1	–	–2	–	V
$I_{GG1} + I_{GG2}$	negative peak supply current		–	2.5	5	mA

Note

1. The negative bias V_{GG1} and V_{GG2} must be applied 10 μs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

AC CHARACTERISTICS

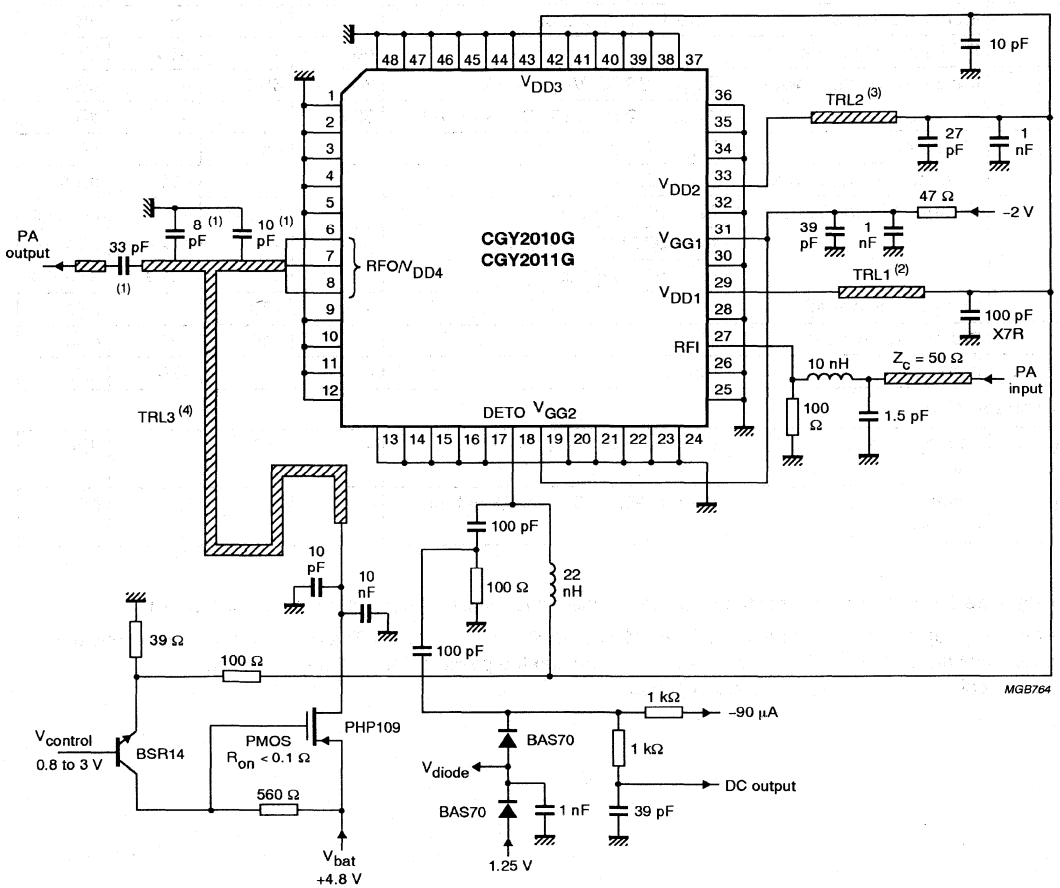
V_{DD} = 4.5 V; T_{amb} = 25 °C; general operating conditions applied; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_{in}	input power		−1.5	–	+1.5	dBm
S_{11}	input return loss	note 1; 50 Ω source	–	–	−6	dB
f_{RF}	RF frequency range		880	–	915	MHz
$P_{out(max)}$	maximum output power	T_{amb} = 25 °C; V_{DD} = 4.5 V	34.5	35.5	–	dBm
		T_{amb} = −20 to +85 °C; V_{DD} = 4.2 V	32.5	–	–	dBm
η	efficiency	V_{DD} = 4.2 V	–	45	–	%
$P_{out(min)}$	minimum output power	V_{DD} < 0.1 V	–	–	−20	dBm
N_{RX}	output noise in RX band	f_{RF} = 925 MHz at $P_{out(max)}$	–	–	−117	dBm/Hz
		f_{RF} = 935 MHz at $P_{out(max)}$	–	–	−129	dBm/Hz
		f_{RF} = 960 MHz at $P_{out(max)}$	–	–	−129	dBm/Hz
H2	2nd harmonic level		–	−33	−30	dBc
H3	3rd harmonic level		–	−40	−37	dBc
Stab	stability	note 2	–	–	−70	dBc
Power sensor driver						
$P_{out(DET)}$	sensor driver output power	R_L = 100 Ω; relative to PA output power into 50 Ω load	–	−23	–	dBc
$\Delta P_{out(DET)}$	driver output power variation	load VSWR < 6 : 1 at PA output	–	–	2	dB

Notes

1. Including the 100 Ω resistor connected in parallel at the power amplifier input on the evaluation board.
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 second period.

APPLICATION INFORMATION



(1) These capacitors are type: SMD0402; rest of the capacitors: SMD0603.
(2) TRL1: width: 0.3 mm; length: 16 mm.
(3) TRL2: width: 0.3 mm; length: 6.3 mm.
(4) TRL3: width: 0.3 mm; length: 20 mm.

Fig.3 Evaluation board schematic (FR4, 0.8 mm).

GSM 4 W power amplifier CGY2013G

FEATURES

- Power Amplifier (PA) overall efficiency 45%
- 35.5 dB gain
- 0 dBm input power
- Gain control range >55 dB
- Integrated power sensor driver
- Low output noise floor of PA < −129 dBm/Hz in GSM RX band
- Wide operating temperature range −20 to +85 °C
- LQFP 48 pin package
- Compatible with power ramping controller PCA5075
- Compatible with GSM RF transceiver SA1620.

APPLICATIONS

- 880 to 915 MHz hand-held transceivers for E-GSM applications
- 900 MHz Time Division Multiple Access (TDMA) systems.

GENERAL DESCRIPTION

The CGY2013G is a GSM class 4 GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate at 3.6 V battery supply. The IC also includes a power sensor driver so that no directional coupler is required in the power control loop.

The PA requires only a 30 dB harmonic low-pass filter to comply with the GSM transmit spurious specification. It can be switched off and its power controlled by monitoring the actual drain voltage applied to the amplifier stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER [1]	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	3.3	–	V
I_{DD}	positive peak supply current	–	2.4	–	A
$P_{o(max)}$	maximum output power	–	35.5	–	dBm
T_{amb}	operating ambient temperature	−20	–	+85	°C

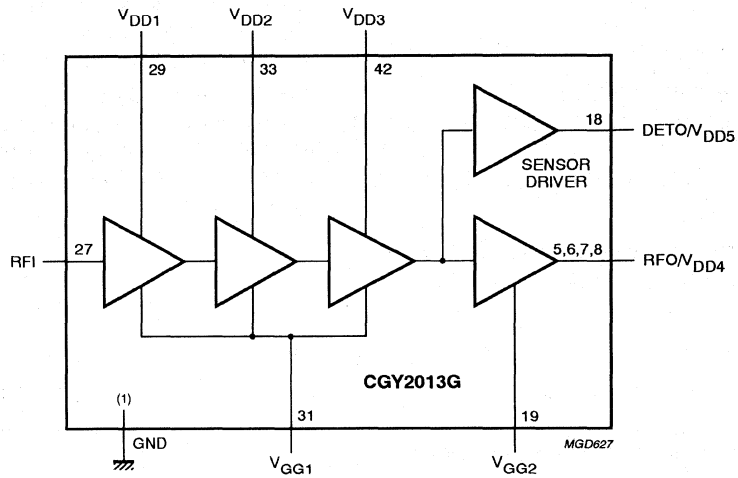
Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2013G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM



(1) Ground pins 1 to 4, 9 to 17, 20 to 26, 28, 30, 32, 34 to 41 and 43 to 48.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 4	ground
RFO/V_{DD4}	5 to 8	power amplifier output and fourth stage supply voltage
GND	9 to 17	ground
DETO/V_{DD5}	18	power sensor output and supply voltage
V_{GG2}	19	fourth stage negative gate supply voltage
GND	20 to 26	ground
RFI	27	power amplifier input
GND	28	ground
V_{DD1}	29	first stage supply voltage
GND	30	ground
V_{GG1}	31	first three stages negative gate supply voltage
GND	32	ground
V_{DD2}	33	second stage supply voltage
GND	34 to 41	ground
V_{DD3}	42	third stage supply voltage
GND	43 to 48	ground

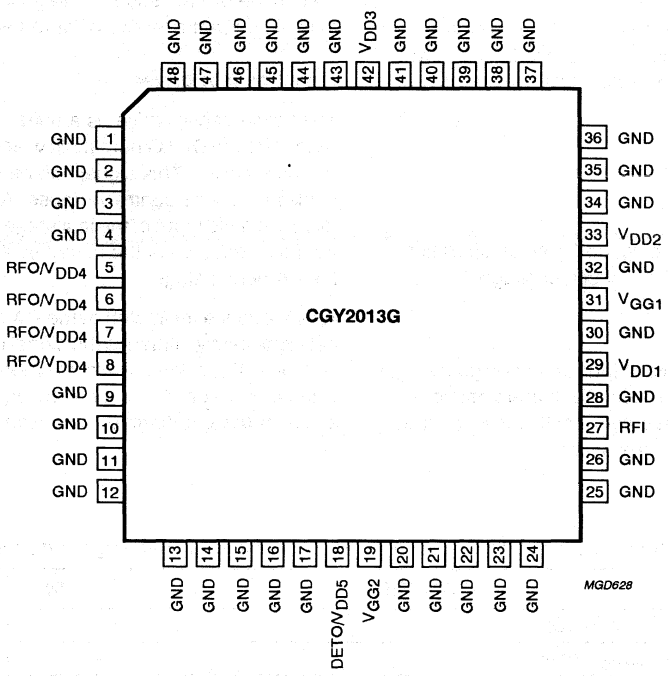


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating conditions

The CGY2013G is designed to meet the European Telecommunications Standards Institute (ETSI) GSM documents, the *"ETS 300 577 specification"*, which are defined as follows:

- t_{on} = 542.8 μs
- T = 4.3 ms
- Duty cycle = 1/8.

The device is specifically designed for pulse operation allowing the use of a LQFP48 plastic package.

Power amplifier

The power amplifier consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

The amplifier bias is set using a negative voltage applied at pins V_{GG1} and V_{GG2}. This negative voltage must be present before the supply voltage is applied to the drains to avoid current overstress for the amplifier.

Power sensor driver

The power sensor driver is a buffer amplifier that delivers a signal to the DETO output pin which is proportional to the amplifier power. This signal can be detected by external diodes for power control purpose. As the sensor signal is taken from the input of the last stage of the PA, it is isolated from disturbances at the output by the reverse isolation of the PA output stage.

An impedance mismatch at the PA output therefore, does not significantly influence the signal delivered by the power sensor as this normally occurs when power sense is made using a directional coupler. Consequently the cost and space of using a directional coupler are saved.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	7	V
V_{GG}	negative supply voltage	–	−10	V
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
T_{stg}	IC storage temperature	–	150	°C
P_{tot}	total power dissipation	–	1.5	W

THERMAL CHARACTERISTICS

General operating conditions applied.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case; note 1	32	K/W

Note

1. This thermal resistance is measured under GSM pulse conditions.

DC CHARACTERISTICS

V_{DD} = 3.3 V; T_{amb} = 25 °C; general operating conditions applied; peak current values during burst; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	positive supply voltage		0	3.3	5.5	V
I_{DD}	positive peak supply current		–	2.4	3.0	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	–	–2	–	V
V_{GG2}	negative supply voltage	note 1	–	–2	–	V
$I_{GG1} + I_{GG2}$	negative peak supply current		–	2.5	5	mA

Note

1. The negative bias V_{GG1} and V_{GG2} must be applied 10 μs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

AC CHARACTERISTICS

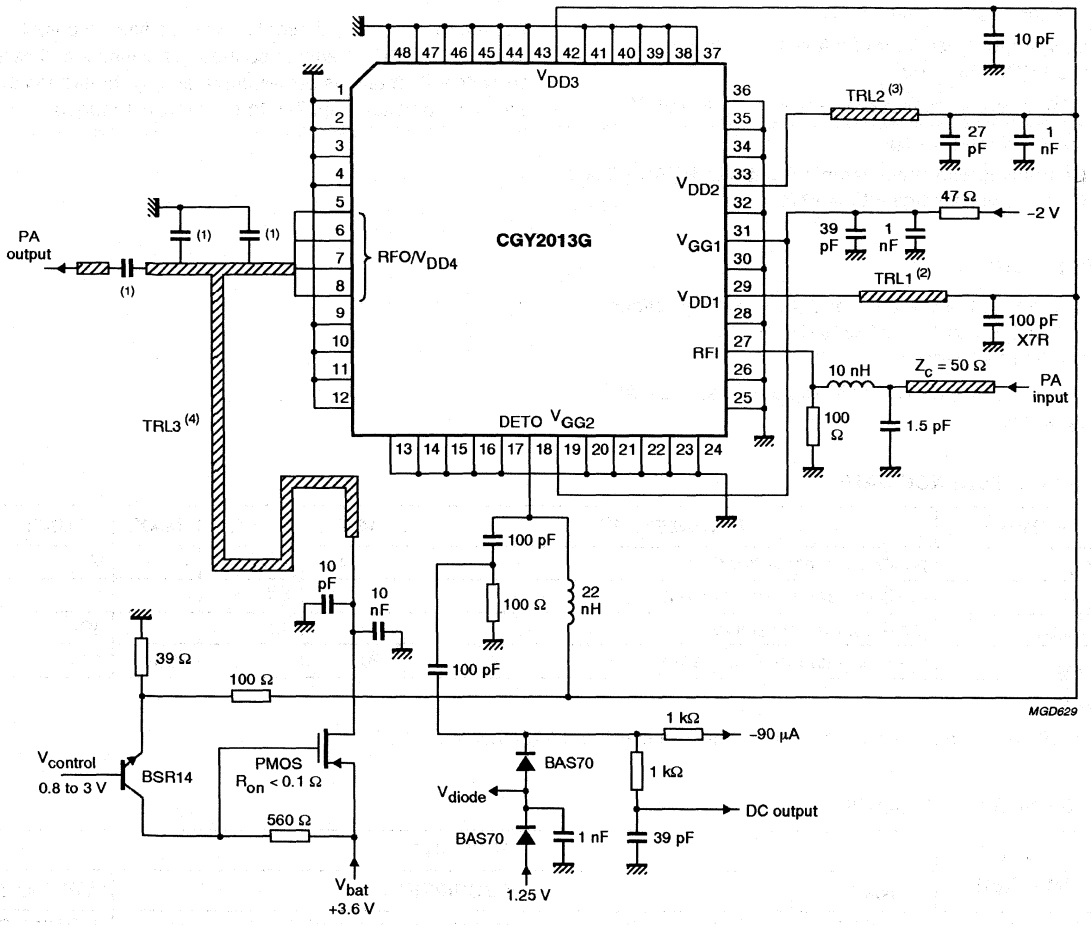
V_{DD} = 3.3 V; T_{amb} = 25 °C; general operating conditions applied; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_i	input power		−1.5	–	+1.5	dBm
S_{11}	input return loss	note 1; 50 Ω source	–	–	−6	dB
f_{RF}	RF frequency range		880	–	915	MHz
$P_{o(max)}$	maximum output power	T_{amb} = 25 °C; V_{DD} = 3.3 V	34.5	35.5	–	dBm
		T_{amb} = −20 to +85 °C; V_{DD} = 2.9 V	32.5	–	–	dBm
η	efficiency	V_{DD} = 2.9 V	–	45	–	%
$P_{o(min)}$	minimum output power	V_{DD} < 0.1 V	–	–	−20	dBm
N_{RX}	output noise in RX band	f_{RF} = 925 MHz at $P_{o(max)}$	–	–	−117	dBm/Hz
		f_{RF} = 935 MHz at $P_{o(max)}$	–	–	−129	dBm/Hz
		f_{RF} = 960 MHz at $P_{o(max)}$	–	–	−129	dBm/Hz
H2	2nd harmonic level		–	−33	−30	dBc
H3	3rd harmonic level		–	−40	−37	dBc
Stab	stability	note 2	–	–	−70	dBc
Power sensor driver						
$P_{o(DET)}$	sensor driver output power	R_L = 100 Ω; relative to PA output power into 50 Ω load	–	−23	–	dBc
$\Delta P_{o(DET)}$	driver output power variation	load VSWR < 6 : 1 at PA output	–	–	2	dB

Notes

1. Including the 100 Ω resistor connected in parallel at the power amplifier input on the evaluation board.
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 second period.

APPLICATION INFORMATION



(1) These capacitors are type: SMD0402; rest of the capacitors: SMD0603.
(2) TRL1: width: 0.3 mm; length: 16 mm.
(3) TRL2: width: 0.3 mm; length: 6.3 mm.
(4) TRL3: width: 0.3 mm; length: 20 mm.

Fig.3 Evaluation board schematic (FR4, 0.8 mm).

DCS/PCS 2 W power amplifier CGY2021G

FEATURES

- Power Amplifier (PA) overall efficiency 48% (DCS)
- 33 dB gain
- 0 dBm input power
- Gain control range >50 dB
- Integrated power sensor driver
- Low output noise floor of PA <−121 dBm/Hz in DCS/PCS RX band
- Wide operating temperature range −20 to +85 °C
- LQFP 48-pin package
- Compatible with power ramping controller PCA5075 and GaAs power controller UBA1710.

APPLICATIONS

- Hand-held transceivers for DCS/PCS applications (DCS: 1710 to 1785 MHz and PCS: 1850 to 1910 MHz)
- 1800 MHz Time Division Multiple Access (TDMA) systems.

GENERAL DESCRIPTION

The CGY2021G is a DCS/PCS class 1 GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate at 4.8 V battery supply.

The chip also includes a power sensor driver so that no directional coupler is required in the power control loop.

The PA requires only a simple low-pass filter to comply with the DCS/PCS transmit spurious specification. It can be switched off and its power controlled by monitoring the actual drain voltage applied to the amplifier stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER[1]	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	4.5	–	V
I_{DD}	positive peak supply current	–	1.1	–	A
$P_{o(max)}$	maximum output power	–	33	–	dBm
T_{amb}	operating ambient temperature	−20	–	+85	°C

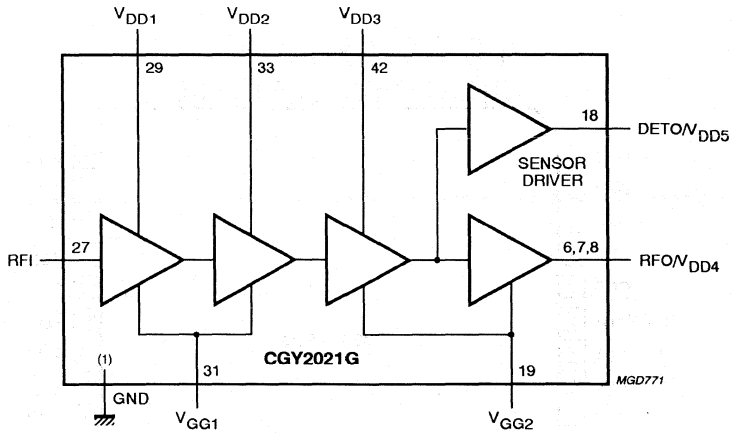
Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2021G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM



(1) Ground pins 1 to 5, 9 to 17, 20 to 26, 28, 30, 32, 34 to 41 and 43 to 48.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 5	ground
RFO/V_{DD4}	6 to 8	PA output and fourth stage supply voltage
GND	9 to 17	ground
DETO/V_{DD5}	18	power sensor output and supply voltage
V_{GG2}	19	third and fourth stage negative gate supply voltage
GND	20 to 26	ground
RFI	27	PA input
GND	28	ground
V_{DD1}	29	first stage supply voltage
GND	30	ground
V_{GG1}	31	first and second stage negative gate supply voltage
GND	32	ground
V_{DD2}	33	second stage supply voltage
GND	34 to 41	ground
V_{DD3}	42	third stage supply voltage
GND	43 to 48	ground

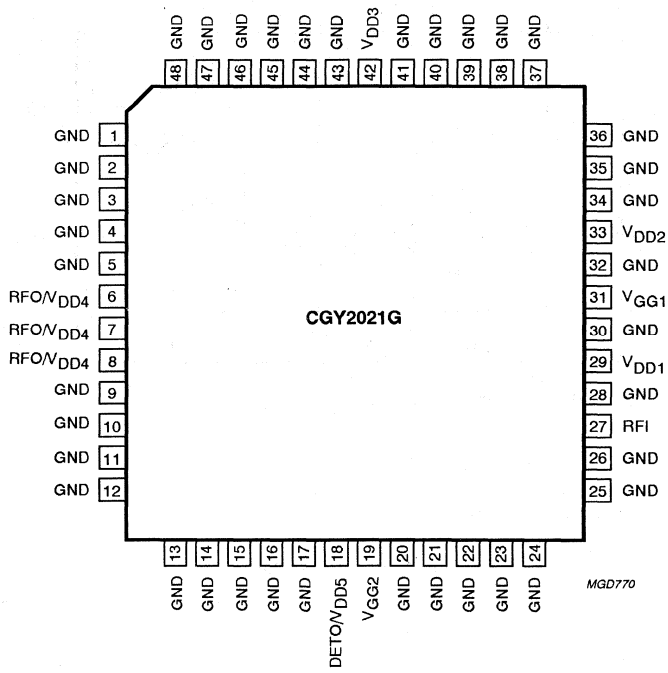


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating conditions

The CGY2021G is designed to meet the European Telecommunications Standards Institute (ETSI) DCS documents, the ETS 300 577 specification, which are defined as follows:

- t_{on} = 542.8 µs
- T = 4.3 ms
- Duty cycle = 1/8.

This amplifier is specifically designed for pulse operation allowing the use of a LQFP48 plastic package.

Power amplifier

The Power Amplifier (PA) consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

The amplifier bias is set by using a negative voltage applied at pins V_{GG1} and V_{GG2}. This negative voltage must be present before the supply voltage is applied to the drains to avoid current overstress of the amplifier.

Power sensor driver

The power sensor driver is a buffer amplifier that delivers an output signal at the DETO pin which is proportional to the amplifier power. This signal can be detected by external diodes for power control purpose. As the sensor signal is taken from the input of the last stage of the PA, it is isolated from disturbances at the output by the reverse isolation of the PA output stage. An impedance mismatch at the PA output therefore does not significantly influence the signal delivered by the power sensor as this normally occurs when power sense is made using a directional coupler. Consequently, the cost and space of using a directional coupler are saved.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	7	V
V_{GG}	negative supply voltage	–	–10	V
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
T_{stg}	IC storage temperature	–	150	°C
P_{tot}	total power dissipation	–	600	mW

THERMAL CHARACTERISTICS

General operating conditions applied.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case; note 1	tbf	K/W

Note

1. This thermal resistance is measured under DCS/PCS pulse conditions.

DC CHARACTERISTICS

V_{DD} = 4.5 V; T_{amb} = 25 °C; peak current values during burst; general operating conditions applied; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	positive supply voltage		–	4.5	–	V
I_{DD}	positive peak supply current		–	1.1	–	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	–	–1.8	–	V
V_{GG2}	negative supply voltage	note 1	–	–1.8	–	V
$I_{GG1} + I_{GG2}$	negative peak supply current		–	0.5	2	mA

Note

1. The negative bias V_{GG} must be applied 10 μs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

AC CHARACTERISTICS

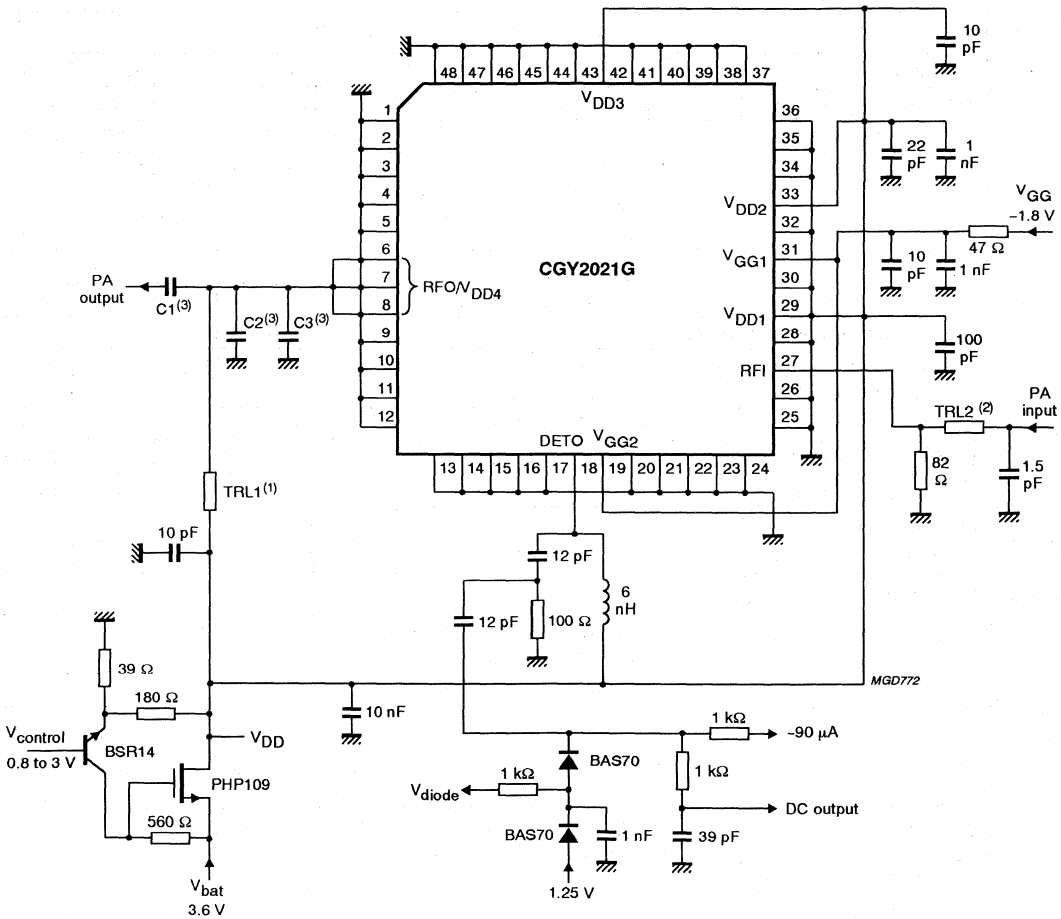
V_{DD} = 4.5 V; T_{amb} = 25 °C; general operating conditions applied; unless otherwise specified.
Measured and guaranteed on CGY2021G evaluation board.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_i	input power		–2	–	+2	dBm
S_{11}	input return loss	50 Ω source; note 1	–	–	–10	dB
f_{RF}	RF frequency range	DCS	1710	–	1785	MHz
		PCS	1850	–	1910	MHz
$P_{o(max)}$	maximum output power	T_{amb} = 25 °C; V_{DD} = 4.5 V	–	33	–	dBm
		T_{amb} = –20 to +85 °C; V_{DD} = 4.2 V	31	–	–	dBm
η	efficiency	DCS; at $P_{o(max)}$	42	48	–	%
		PCS; at $P_{o(max)}$	–	45	–	%
R_S	optimum series load resistance		–	6	–	Ω
C_S	optimum series load capacitance		–	11	–	pF
$P_{o(off)}$	isolation	PA OFF; P_i = 0 dBm	–	–45	–	dBm
N_{RX}	output noise in RX band		–	–	–121	dBm/Hz
H2	2nd harmonic level		–	–	–40	dBc
H3	3rd harmonic level		–	–	–35	dBc
Stab	stability	note 2	–	–	tbf	dBc
Power sensor driver						
$P_{o(DET)}$	sensor driver output power	R_L = 100 Ω; relative to PA output power into 50 Ω load	–23	–20	–18	dBc
$\Delta P_{o(DET)}$	driver output power variation	load VSWR < 6 : 1 at PA output	–	–	tbf	dB

Notes

1. Including the 82 Ω resistor connected in parallel at the power amplifier input on the evaluation board.
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 seconds test period.

APPLICATION INFORMATION



All capacitors are type: SMD0603.

Thickness: 0.8 mm; substrate: FR4; $\varepsilon_r = 4.7$.

(1) TRL1: width = 0.3 mm; length = 16 mm.

(2) TRL2: width = 0.5 mm; length = 10 mm.

(3) the component values are:

SYSTEM	C1 (pF)	C2 (pF)	C3 (pF)
DCS	2.2	1.8	2.2
PCS	47	1.5	2.2

Fig.3 Evaluation board schematic.

DCS 2 W power amplifier CGY2023G

FEATURES

- Power Amplifier (PA) overall efficiency 38%
- 33 dB gain
- 0 dBm input power
- Gain control range >50 dB
- Integrated power sensor driver
- Low output noise floor of PA <–121 dBm/Hz in DCS RX band
- Wide operating temperature range –20 to +85 °C
- LQFP 48 pin package
- Compatible with power ramping controller PCA5075.

APPLICATIONS

- 1710 to 1785 MHz hand-held transceivers for DCS applications
- 1800 MHz Time Division Multiple Access (TDMA) systems.

GENERAL DESCRIPTION

The CGY2023G is a DCS class 1 GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate at 3.6 V battery supply.

The chip also includes a power sensor driver so that no directional coupler is required in the power control loop.

The PA requires only a simple low-pass filter to comply with the DCS transmit spurious specification. It can be switched off and its power controlled by monitoring the actual drain voltage applied to the amplifier stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER[1]	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	3.3	–	V
I_{DD}	positive peak supply current	–	1.7	–	A
$P_{o(max)}$	maximum output power	–	33	–	dBm
T_{amb}	operating ambient temperature	–20	–	+85	°C

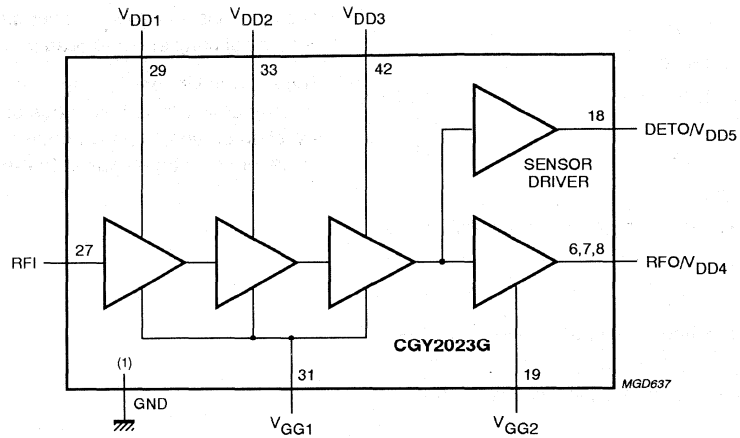
Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2023G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm	SOT313-2

BLOCK DIAGRAM



(1) Ground pins 1 to 5, 9 to 17, 20 to 26, 28, 30, 32, 34 to 41 and 43 to 48.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 5	ground
RFO/V_{DD4}	6 to 8	power amplifier output and fourth stage supply voltage
GND	9 to 17	ground
DETO/V_{DD5}	18	power sensor output and supply voltage
V_{GG2}	19	fourth stage negative gate supply voltage
GND	20 to 26	ground
RFI	27	power amplifier input
GND	28	ground
V_{DD1}	29	first stage supply voltage
GND	30	ground
V_{GG1}	31	first three stages negative gate supply voltage
GND	32	ground
V_{DD2}	33	second stage supply voltage
GND	34 to 41	ground
V_{DD3}	42	third stage supply voltage
GND	43 to 48	ground

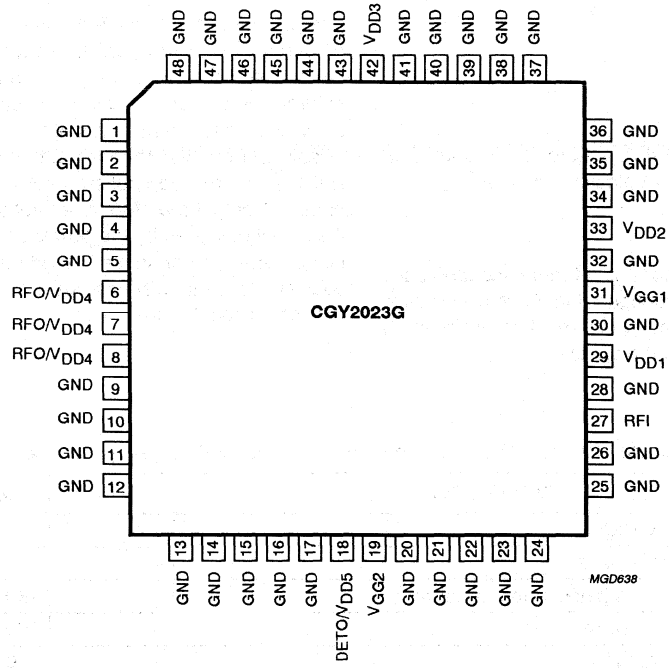


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating conditions

The CGY2023G is designed to meet the European Telecommunications Standards Institute (ETSI) DCS documents, the ETS 300 577 specification, which are defined as follows:

- t_{on} = 542.8 µs
- T = 4.3 ms
- Duty cycle = 1/8.

This amplifier is specifically designed for pulse operation allowing the use of a LQFP48 plastic package.

Power amplifier

The Power Amplifier (PA) consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

The amplifier bias is set by using a negative voltage applied at pins V_{GG1} and V_{GG2}. These negative voltages must be present before the supply voltage is applied to the drains to avoid current overstress of the amplifier.

Power sensor driver

The power sensor driver is a buffer amplifier that delivers an output signal at the DETO pin which is proportional to the amplifier power. This signal can be detected by external diodes for power control purpose. As the sensor signal is taken from the input of the last stage of the PA, it is isolated from disturbances at the output by the reverse isolation of the PA output stage. An impedance mismatch at the PA output therefore does not significantly influence the signal delivered by the power sensor as this normally occurs when power sense is made using a directional coupler. Consequently, the cost and space of using a directional coupler are saved.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	7	V
V_{GG}	negative supply voltage	–	–10	V
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
T_{stg}	IC storage temperature	–	150	°C
P_{tot}	total power dissipation	–	600	mW

THERMAL CHARACTERISTICS

General operating conditions applied

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case; note 1	tbf	K/W

Note

1. This thermal resistance is measured under DCS pulse conditions.

DC CHARACTERISTICS

V_{DD} = 3.3 V; T_{amb} = 25 °C; peak current values during burst; general operating conditions applied; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	positive supply voltage		0	3.3	5.5	V
I_{DD}	positive peak supply current		–	1.7	–	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	–	–2	–	V
V_{GG2}	negative supply voltage	note 1	–	–2	–	V
$I_{GG1} + I_{GG2}$	negative peak supply current		–	0.5	2	mA

Note

1. The negative bias V_{GG1} and V_{GG2} must be applied 10 μs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

AC CHARACTERISTICS

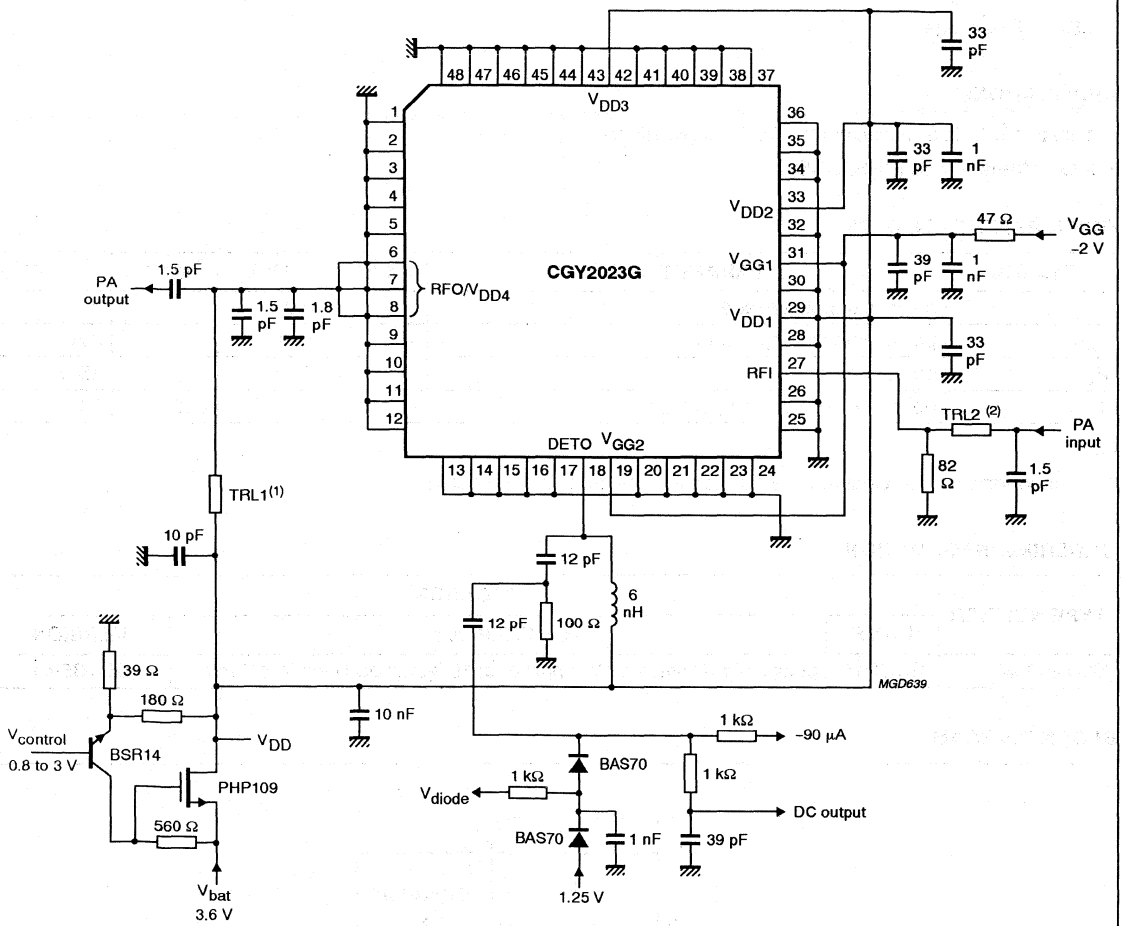
V_{DD} = 3.3 V; T_{amb} = 25 °C; general operating conditions applied; unless otherwise specified.
Measured and guaranteed on CGY2023G evaluation board.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_i	input power		−2	–	+2	dBm
S_{11}	input return loss	note 1; 50 Ω source	–	–	−10	dB
f_{RF}	RF frequency range		1710	–	1785	MHz
$P_{o(max)}$	maximum output power	T_{amb} = 25 °C; V_{DD} = 3.3 V	–	33	–	dBm
		T_{amb} = −20 to +85 °C; V_{DD} = 2.9 V	31	–	–	dBm
η	efficiency	at $P_{o(max)}$	–	38	–	%
R_S	optimum series load resistance		–	tbf	–	Ω
C_S	optimum series load capacitance		–	tbf	–	pF
$P_{o(off)}$	isolation	PA OFF; P_i = 0 dBm	–	−45	–	dBm
N_{RX}	output noise in RX band		–	–	−121	dBm/Hz
H2	2nd harmonic level		–	–	−40	dBc
H3	3rd harmonic level		–	–	−35	dBc
Stab	stability	note 2	–	–	tbf	dBc
Power sensor driver						
$P_{o(DET)}$	sensor driver output power	R_L = 100 Ω; relative to PA output power into 50 Ω load	−19	−17	−15	dBc
$\Delta P_{o(DET)}$	driver output power variation	load VSWR < 6 : 1 at PA output	–	–	tbf	dB

Notes

1. Including the 82 Ω resistor connected in parallel at the power amplifier input on the evaluation board.
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 seconds test period.

APPLICATION INFORMATION



All capacitors are type: SMD0603.
Thickness: 0.8 mm; substrate: FR4; $\varepsilon_r = 4.7$.
(1) TRL1: width = 0.3 mm; length = 16 mm.
(2) TRL2: width = 0.5 mm; length = 10 mm.

Fig.3 Evaluation board schematic.

DECT 500 mW power amplifier CGY2030M

FEATURES

- Power Amplifier (PA) overall efficiency 40%
- 27 dB gain
- 0 dBm input power
- Operation possible without negative supply
- Wide operating temperature range –20 to +85 °C
- SSOP16 package.

GENERAL DESCRIPTION

The CGY2030M is a GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate at 3.6 V battery supply. When power control is not required, it can be operated without negative supply voltage.

APPLICATIONS

- 1.88 to 1.9 GHz transceivers for DECT applications
- 2 GHz transceivers (PHS, DCS).

QUICK REFERENCE DATA

SYMBOL	PARAMETER [1]	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	3.2	–	V
I_{DD}	positive peak supply current	–	400	–	mA
P_o	output power	–	27	–	dBm
T_{amb}	operating ambient temperature	–20	–	+85	°C

Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2030M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

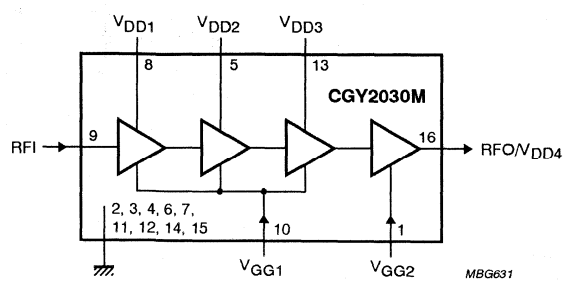


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{GG2}	1	fourth stage negative gate supply voltage
GND	2 to 4	ground
V_{DD2}	5	second stage supply voltage
GND	6 and 7	ground
V_{DD1}	8	first stage supply voltage
RFI	9	PA input
V_{GG1}	10	first second and third stages negative gate supply voltage
GND	11 and 12	ground
V_{DD3}	13	third stage supply voltage
GND	14 and 15	ground
RFO/V_{DD4}	16	PA output and fourth stage supply voltage

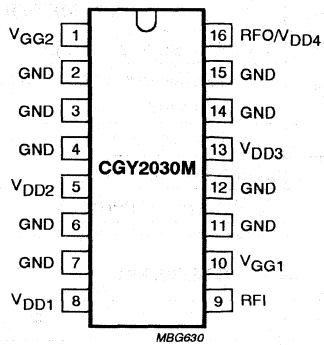


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Amplifier

The CGY2030M is a 4-stage GaAs MESFET power amplifier capable of delivering 500 mW (typ.) at 1.9 GHz into a 50 Ω load. Each amplifier stage has an open-drain configuration. The drains have to be loaded externally by adequate reactive circuits which must also provide a DC path to the supply.

The amplifier can be switched off by means of an external PNP or PMOS series switch connected between the battery and the amplifier drains. This switch can also be used to vary the actual supply voltage applied to the amplifier and hence, control the output power.

This device is specifically designed to work with a duty factor of 25%.

Biasing

Two modes of operation are possible:

- Mode 1
- Mode 2.

MODE 1

In the first mode, the pins V_{GG1} and V_{GG2} are simply connected to the ground via resistors (10 kΩ in the evaluation board; see Fig.4). The amplifier biases itself internally to a negative voltage by action of the incoming RF signal. In this mode, power control cannot be achieved by varying the amplifier supply voltage; therefore it is suitable only for applications where power control is not required such as DECT.

MODE 2

If a negative bias is available, a second mode of operation is possible, in which the amplifier is biased by providing adequate negative voltages at pins V_{GG1} and V_{GG2}. In this mode, the amplifier internal bias does not depend on the incoming RF level, nor on the drain voltage, so that power control is possible by variation of the supply voltage.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		–	–	5.2	V
$V_{DD} - V_{GG}$	voltage difference between supply voltage and gate bias voltage	no input signal	–	–	8	V
$T_{j(max)}$	maximum operating junction temperature		–	–	150	°C
P_{tot}	total power dissipation		–	–	400	mW
T_{stg}	IC storage temperature		–55	–	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	145	K/W

HANDLING

Do not operate or store near strong electrostatic fields. Meets class 1 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

DC CHARACTERISTICS

V_{DD} = 3.2 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2} and V_{DD1}						
V_{DD}	positive supply voltage	note 1	2.6	3.2	4.2	V
I_{DD}	positive supply current		–	400	500	mA
Pins V_{GG1} and V_{GG2}; in mode 2						
V_{GG1}	bias voltage for input stages	note 2	–	–1.2	–	V
V_{GG2}	bias voltage for output stage	note 2	–	–2.0	–	V
$I_{GG(tot)}$	total gate current	note 3	–1	–	+1	mA

Notes

1. Self biasing guaranteed in mode 1 at minimum input power (–3 dBm) and minimum recommended supply voltage V_{DD} (2.6 V).
2. Negative voltages V_{GG1} and V_{GG2} must be applied before supply voltage V_{DD}.
3. Due to non linear effects at high power levels, the gate current can be either negative or positive.

AC CHARACTERISTICS

V_{DD} = 3.2 V; f_{RF} = 1900 MHz; P_i = 0 dBm; T_{amb} = 25 °C; duty factor δ = 25%; 50 Ω impedance system; measured and guaranteed on CGY2030M evaluation board (see Fig.4).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_i	input power		–3	–	+5	dBm
δ	duty factor		–	–	25	%
Measured in mode 1; without negative biasing; V_{GG1} and V_{GG2} connected to ground						
P_o	output power		26	27	28.5	dBm
η	efficiency		–	40	–	%
P_{leak}	RF leakage to output in power off state	V_{DD} = 0 V	–	–40	–	dBm
H2, H3	second and third harmonics level		–	–35	–	dBc
Stab	stability (spurious levels)	note 1	–	–60	–	dBc
Measured in mode 2; with negative biasing at pins V_{GG1} and V_{GG2}						
P_o	output power		25.5	26.5	28	dBm
η	efficiency		–	35	–	%
P_{leak}	RF leakage to output in power off state	V_{DD} = 0 V	–	–50	–	dBm

Note

1. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 seconds test period.

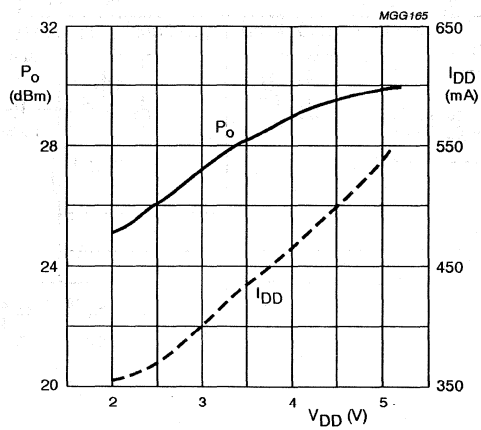
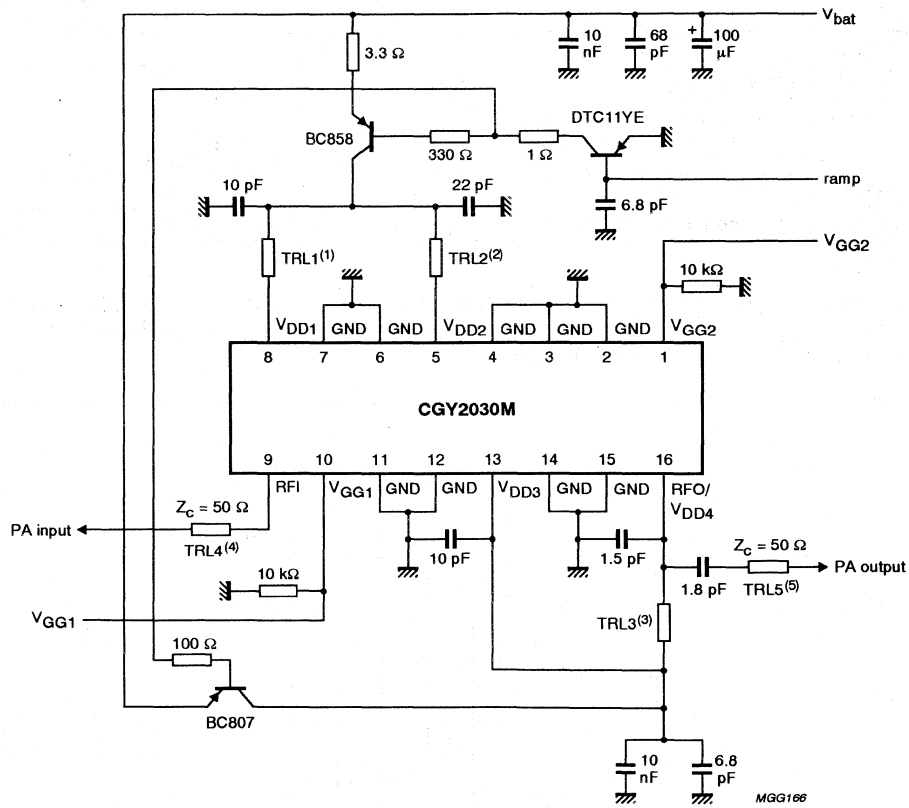


Fig.3 Typical power and current characteristics in mode 1.

APPLICATION INFORMATION

The CGY2030M is operated and tested in accordance with the circuit diagram shown in Fig.4. Supply voltage switching is achieved by two bipolar PNP transistors. One transistor switches the first and second stages and the other switches the third and fourth stages.

By switching on the last amplifier stages with some delay compared to the first stages, it is possible to get the last stages already self-biased before their supply voltage has reached its steady state value. This enables smooth power up-ramping without any power overshoot. A simpler drain switching circuit can be used if the amplifier is operated with negative biasing of the pins V_{GG1} and V_{GG2}.



Thickness: 0.8 mm; substrate: FR4; $\varepsilon_r = 4.7$.

(1) TRL1: width = 500 µm; length = 11200 µm.
(2) TRL2: width = 500 µm; length = 7770 µm.
(3) TRL3: width = 300 µm; length = 15450 µm.
(4) TRL4: width = 1600 µm; length = 12000 µm.
(5) TRL5: width = 1600 µm; length = 11000 µm.

Fig.4 Evaluation board schematic.

2.45GHz RF power amplifier and T/R switch SA2410

DESCRIPTION

The SA2410 is a GaAs monolithic power amplifier with an integrated T/R switch designed to meet requirements for 802.11 (WLAN). The SA2410 uses an on–chip 4 GHz oscillator to generate the negative bias, thus eliminating the need for a negative supply. It operates from 3V to 5.5V and consumes 125 mA with an output power of 18.5 dB (typ). It is suitable for other 2.45 GHz ISM band applications.

FEATURES

- V_{CC}=3V–5.5V
- No negative bias needed
- I_{CC}=125mA (typ) @ 3.3V
- P_{OUT}=18.5 dB(typ)
  IM3<–30dBc
  IM5<–50dBc
- Gain=28dB (typ)
- Attenuation range=14dB (typ)
- TQFP–32 package

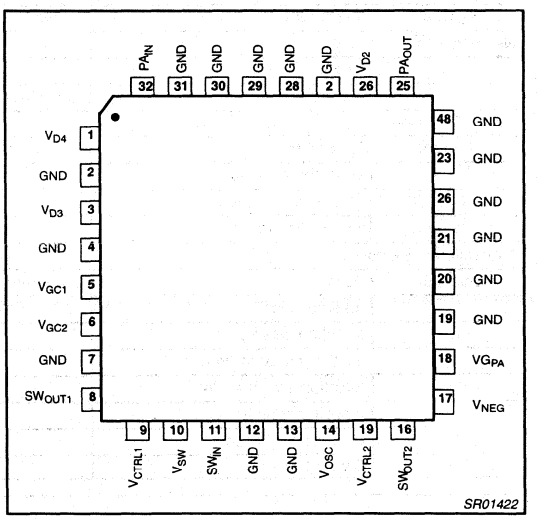


Figure 1. Pin Configuration

APPLICATIONS

- 802.11 WLAN
- 2.4–2.5 GHz ISM BAND

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
32–Pin Plastic Thin Quad Flat Package	–40° C+85°C	SA2410	SOT358–2

GENERAL SPECIFICATIONS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T	Temperature		–40		+85	C
V_{CC}	Supply V		3		5.5	V
I_{CC}	Supply I	3.3 volts		125		mA
Power Amplifier						
f_{RF}	Frequency Range		2.4		2.5	GHz
IM3	IM3 2 tones		30			dBc
IM5	IM5 2 tones		50			dBc
T_{on}	Transmit power on	Including neg. supply			2	µs
T_{off}	Xmit power down				2	µs
Gain	Small signal gain			28		dB
P_{out}	Output power	IM3=30dBc IM5=50dBc 125mA@3.3 volts	17.5	18.5		dBm
Eff.	Efficiency			25		%
Δ Gt1	Gain variation with temp	–40 to +85°C		2.5		dB
Δ Gt2	Gain variation with temp	0–70°C		2.0		dB
Δ Gr	Ripple	2.45 ± 0.05 GHz		0.3		dB
Δ Gvd	Gain variation with supply	3.3 volts ± 0.3 V		0.5		dB
Z_{in}	Input impedance			50		Ω

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Negative voltage supply						
t_{on}	Power on time		10		100	nS
	4 GHz spur	Xmit Mode		TBD		dBm
Linear Gain Control						
Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
V_{GC}	Gain control voltage			TBD		Volt
C_{GC}	Input C at gain pin			TBD		pF
G_{CR}	Attenuation range			14		dB
Transmit/receive switch						
Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
L_{tx}	Insertion loss T_x				2	dB
L_{rx}	Insertion loss R_x				1	dB
t_{sw}	Switch response time				400	nS
ISO_{PA}	Isolation switch to PA		30			dB
Z_{in}	Input impedance			50		Ω
Z_{out}	Output impedance			50		Ω
ISO_{SW}	Switch Isolation		20			dB

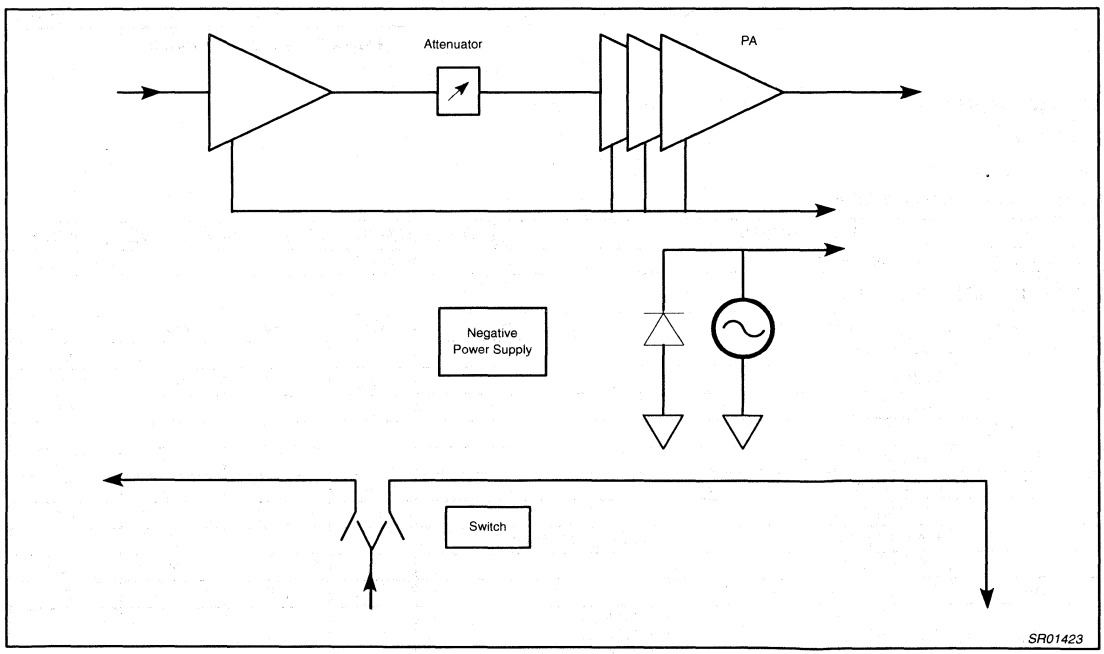


Figure 2. Block Diagram

Low voltage mono/stereo power amplifier TDA7050T

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example).

QUICK REFERENCE DATA

Supply voltage range	V_P		1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ.	3,2	mA
Bridge tied load application (BTL)				
Output power at R_L = 32 Ω				
V_P = 3 V; d_{tot} = 10%	P_o	typ.	140	mW
D.C. output offset voltage between the outputs	$\lvert\Delta V\rvert$	max.	70	mV
Noise output voltage (r.m.s. value)				
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	140	μV
Stereo application				
Output power at R_L = 32 Ω				
d_{tot} = 10%; V_P = 3 V	P_o	typ.	35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ.	75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ.	40	dB
Noise output voltage (r.m.s. value)				
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A); SOT96-1; 1996 July 24.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig.1		
Storage temperature range	T_{stg}		−55 to + 150 °C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration			
at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

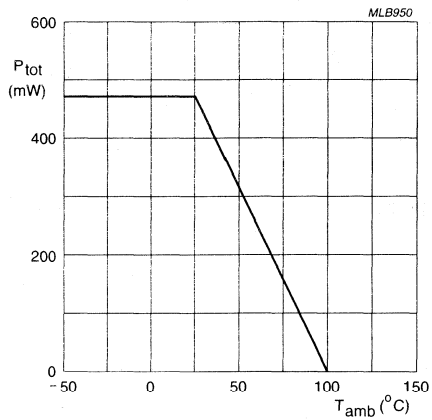


Fig.1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100 - 60}{160} = 0.25\ W$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig.4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig.5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig.2 (BTL application) and Fig.3 (stereo application).

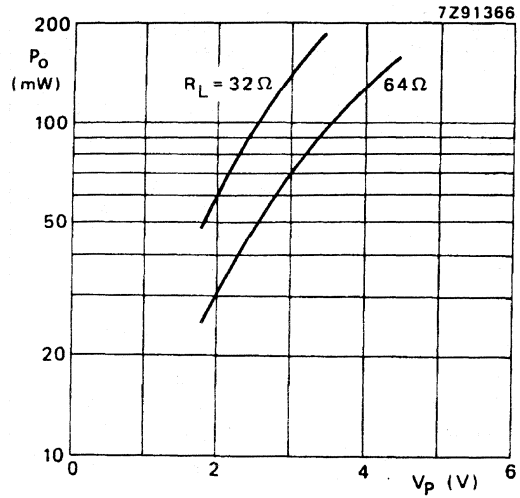


Fig.2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

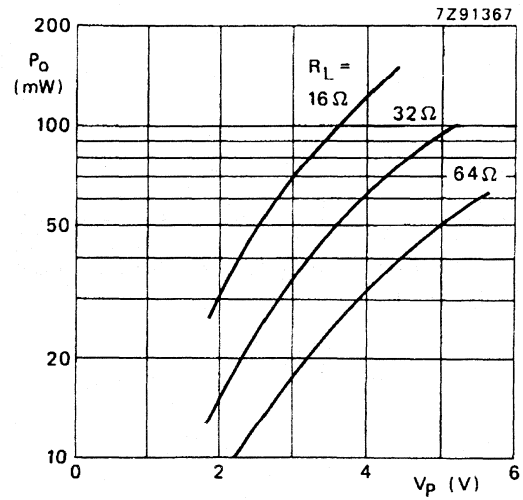


Fig.3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

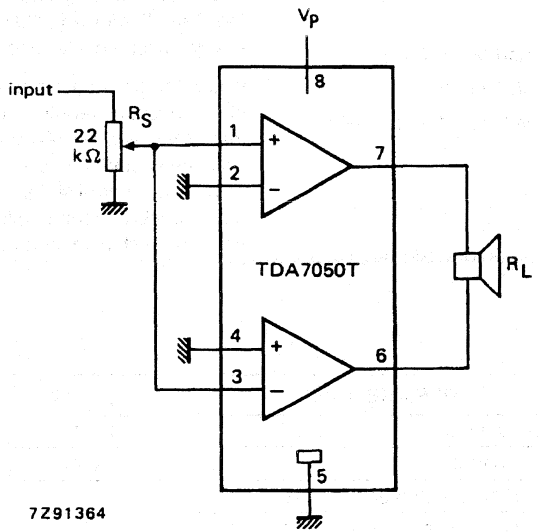


Fig.4 Application diagram (BTL); also used as test circuit.

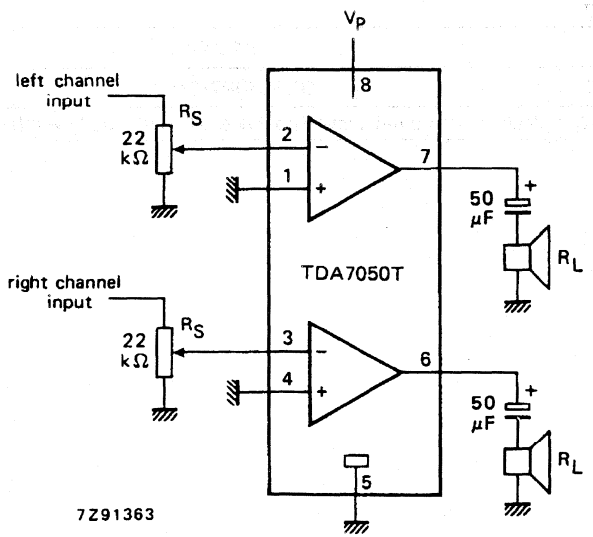


Fig.5 Application diagram (stereo); also used as test circuit.

Modulator for GaAs power amplifiers UBA1710

FEATURES

- Power MOS modulators for control of GaAs power amplifier drain voltage
- Power control loop amplifier and MOS driver
- Voltage tripler for supply of MOS driver
- Positive-to-negative DC converter for GaAs power amplifier gate biasing.

APPLICATIONS

- Control of GaAs power amplifiers for GSM and DCS hand-held transceivers.

GENERAL DESCRIPTION

The UBA1710 integrates the functions required to operate the GaAs Power Amplifiers (PAs) from the CGY20xx family which are intended for GSM and DCS applications.

It includes a negative supply for PA gate biasing and most of the functions required to implement power control so that only a very few external component are required. The power control section integrates two power MOS devices for control of the PA drain voltages, an MOS driver and a feedback loop amplifier. The MOS driver is supplied from an on-chip voltage tripler.

QUICK REFERENCE DATA

SYMBOL	PARAMETER[1]	MIN.	TYP.	MAX.	UNIT
V_{CC}	analog supply voltage	4.2	4.8	6.8	V
V_{DD}	digital supply voltage	4.2	4.8	6.8	V
$I_{CC} + I_{DD}$	peak supply current in power-up mode	–	10	–	mA
T_{amb}	operating ambient temperature	–20	–	+85	°C

Note

1. For conditions, see Chapter "Characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA1710M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

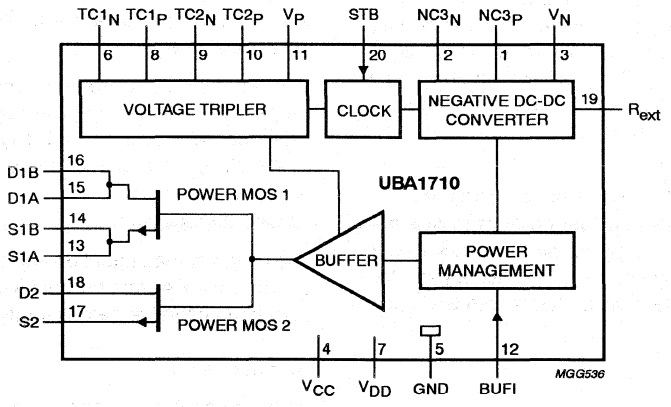


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$NC3_P$	1	charge pump tank capacitor
$NC3_N$	2	charge pump tank capacitor
V_N	3	negative bias voltage
V_{CC}	4	analog supply voltage
GND	5	ground
$TC1_N$	6	charge pump tank capacitor
V_{DD}	7	digital supply voltage
$TC1_P$	8	charge pump tank capacitor
$TC2_N$	9	charge pump tank capacitor
$TC2_P$	10	charge pump tank capacitor
V_P	11	positive tripler voltage
BUFI	12	buffer input
S1A	13	power MOS 1 source A
S1B	14	power MOS 1 source B
D1A	15	power MOS 1 drain A
D1B	16	power MOS 1 drain B
S2	17	power MOS 2 source
D2	18	power MOS 2 drain
R_{ext}	19	external resistance for V_N
STB	20	standby input (active HIGH)

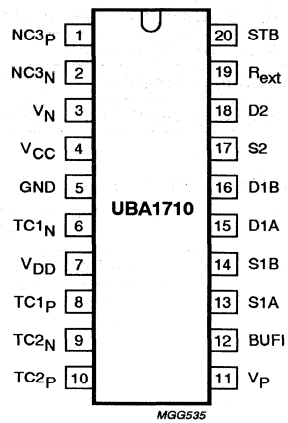


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Power control section

Power control for GaAs PAs from the CGY20xx family is achieved by varying the drain voltage. This is achieved with the UBA1710 by means of the two power MOS devices integrated on-chip. They enable separate control of the PA output stage from the pre-amplifier stages. They have a very low 'on' resistance for low drop voltage at high RF output power.

The MOS devices are driven by a buffer. The buffer amplifier, in association with power MOS, is included in a feedback loop to exhibit a high cut-off frequency (3 MHz) over the whole control dynamic range. This buffer allows fast switching of the MOS in accordance with GSM power ramping requirements.

DC-DC converters

One DC-DC converter is required to provide negative gate biasing to the GaAs PA.

The standard value is typically –2 V, without any external resistor connected. The other one is a voltage tripler and is required to supply the MOS driver. The driver is required to raise the MOS gate voltage well above the battery voltage in order to open the MOS switches ('high side' driver).

These DC-DC converters are operated at a typical frequency of 600 kHz supplied by an internal oscillator. Five external capacitors with a typical value of 0.1 μF (0603 SMD) are required to operate these converters.

Power management

The power management disables the PA drain voltage and prevents the PA from burnout if drain voltage is supplied before the negative gate voltage is available.

Standby mode

An additional feature includes a standby mode, reducing the current consumption to typically 2 μA.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	analog supply voltage	–0.5	+9.0	V
V_{DD}	digital supply voltage	–0.5	+9.0	V
V_I	DC input voltage on all pins (except BUFI)	–0.5	+9.0	V
I_I	DC current into any signal pin	–10	+10	mA
P_{tot}	total power dissipation	–	0.65	W
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–20	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	100	K/W

CHARACTERISTICS

$V_{CC} = V_{DD} = 4.8$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	analog supply voltage		4.2	4.8	6.8	V
V_{DD}	digital supply voltage		4.2	4.8	6.8	V
$I_{CC} + I_{DD}$	peak supply current	power-up mode; PA on	–	10	tbf	mA
		power-down mode; PA off	–	6	tbf	mA
I_{stb}	standby current	standby mode	–	2	tbf	μA
Power MOS 1						
R_{DSon1}	on resistance	$I_{DS} = 1.5$ A	–	0.2	tbf	Ω
Power MOS 2						
R_{DSon2}	on resistance	$I_{DS} = 0.5$ A	–	0.6	tbf	Ω
Clock circuit						
f_{clk}	clock frequency		–	600	–	kHz
Voltage tripler						
V_{Po}	output voltage	with $I_{Po} = 2$ mA	11.5	11.8	12.1	V
$V_{R(p-p)}$	amplitude ripple (peak-to-peak value)	with $I_{Po} = 2$ mA; C1 = C2 = 100 nF; $C_P = 100$ nF	–	2	–	mV
t_{on}	turn-on time		–	100	tbf	μs
Negative DC/DC converter						
V_{No}	output voltage	with $I_{No} = 250$ μA; $R_{ext} = 470$ kΩ	–1.6	–1.8	–2.0	V
$V_{R(p-p)}$	amplitude ripple (peak-to-peak value)	with $I_{No} = 250$ μA; C3 = 100 nF; $C_N = 100$ nF	–	2	tbf	mV
t_{on}	turn-on time		–	280	tbf	μs
MOS buffer amplifier						
V_i	input voltage		1.2	–	3.2	V
t_{sw}	switching time from 0 to 4.5 V	2 Ω load at MOS outputs	–	1	–	μs

APPLICATION INFORMATION

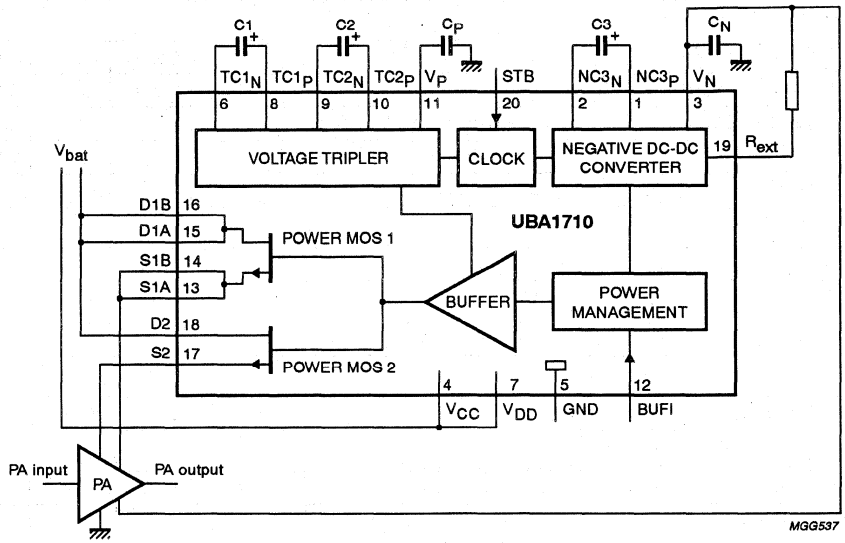


Fig.3 Application diagram.

Section 9
Baseband Processing: Audio and Data

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Baseband Processors

Part No.	Part Type	Application	V_{DD}	I_{DD}	Package
PCD5032	ADPCM Codec	DECT	2.7-6.0V 2.7-6.0V	7mA Typ. Active 20µA Typ. Stdby	28-Pin SO28 44-Pin QFP
PCD5041	BMC (Burst Mode Controller)	DECT	2.7-6.0V	15mA Typ. Active	64-Pin QFP
NE/SA5750	Audio Companding Amplifier	AMPS TACS	5.0V	8.4mA Typ. 1.8mA Stdby	24-Pin DIP 28-Pin SOL
NE/SA5751	Audio Filter and Control	AMPS TACS	5.0V	2.7mA Typ. 0.9mA Stdby	24-Pin DIP 28-Pin SOL
SA5752	Audio Companding VOX and Amplifier	AMPS TACS	2.7V	31mA Typ. 125µA Stdby	20-Pin SOL 20-Pin SSOP
SA5753	Audio Filter and Control	AMPS TACS	2.7V	2.7mA Typ. 600µA Stdby	20-Pin SOL 20-Pin SSOP
PCF5001	POCSAG Decoder	PAGERS	1.5-6.0V	60µA Typ.	28-Pin Mini-Pak 32-Pin QFP
PCD5003	Advanced POCSAG Decoder	PAGERS	1.5-6.0V	50µA Typ. (ON) 25µA Typ. (OFF)	32-Pin TQFP
UMA1000LT	Data Processor for Cellular Radio	AMPS TACS	3.0-5.5V	2.5mA Typ.	28-Pin SOL
UMA1002	Data Processor for Cellular Radio	AMPS TACS	2.7-5.5V	2.5mA Typ.	28-Pin SOL 32-Pin LQFP

*Amplifier: Enabled/Disabled

Audio processor - companding and amplifier section NE/SA5750

DESCRIPTION

The NE/SA5750 is a high performance low power audio signal processing system. The NE/SA5750 subsystems include a low noise microphone preamplifier with adustable gain, a noise cancellation switching amplifier with adjustable threshold, a voice operated transmitter (VOX) switch, VOX control, an audio compressor with buffered input, audio expandor, a unity gain power amplifier to drive a speaker, a summing power amplifier for sidetone attenuation and headphone (earpiece) drive, and an internal bandgap voltage regulator with power down capability. When used with Philips Semiconductors NE/SA5751, the complete audio processing function of an AMPS or TACS cellular telephone is easily implemented. The NE/SA5750 can also be used without the NE/SA5751 in a wide variety of radio communications applications.

FEATURES

- High performance
- 5V supply
- Adjustable VOX and noise cancellation threshold
- Adjustable gain preamplifier
- Audio companding
- ESD protected
- Open collector VOX output
- Logic inputs CMOS compatible
- Power down mode
- Built-in drivers for speaker and earpiece
- Few external components
- SOL and DIP packages

PIN CONFIGURATION

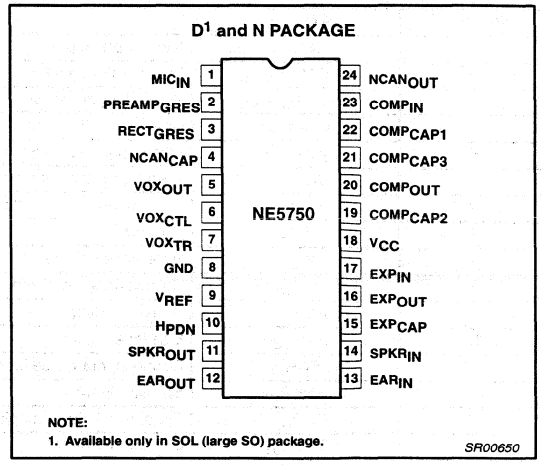


Figure 1. Pin Configuration

BENEFITS

- Very compact applications
- Long battery life in portable equipment
- Complete cellular audio function with the SA5751

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5750N	SOT248-1
24-Pin Plastic Small Outline Large (SOL) package	0 to +70°C	NE5750D	SOT137-1
24-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5750N	SOT248-1
24-Pin Plastic Small Outline Large (SOL) package	-40 to +85°C	SA5750D	SOT137-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage Voltage applied to any pin	6 -0.3 to (V_{CC} + 0.3)	V V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature NE5750 SA5750	 0 to 70 -40 to +85	°C

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	MIC_{IN}	Microphone input
2	$PREAMP_{GRES}$	Preamplifier gain resistor
3	$RECT_{GRES}$	Reactifier gain resistor
4	$NCAN_{CAP}$	Noise cancellation timing capacitor
5	VOX_{OUT}	Voice operated transmission output
6	VOX_{CTL}	Voice operated transmission control
7	VOX_{TR}	Voice operated transmission threshold resistor
8	GND	Ground
9	V_{REF}	Reference voltage
10	H_{PDN}	Hardware power down
11	$SPKR_{OUT}$	Speaker output
12	EAR_{OUT}	Earpiece output
13	EAR_{IN}	Earpiece input, side tone input
14	$SPKR_{IN}$	Speaker input
15	EXP_{CAp}	Expandor timing capacitor
16	EXP_{OUT}	Expandor output
17	EXP_{IN}	Expandor input
18	V_{CC}	Positive supply
19	$COMP_{CAP2}$	Compressor timing capacitor 2
20	$COMP_{OUT}$	Compressor output
21	$COMP_{CAP3}$	Compressor timing capacitor 3
22	$COMP_{CAP1}$	Compressor timing capacitor 1
23	$COMP_{IN}$	Compressor input
24	$NCAN_{OUT}$	Noise cancellation output

BLOCK DIAGRAM

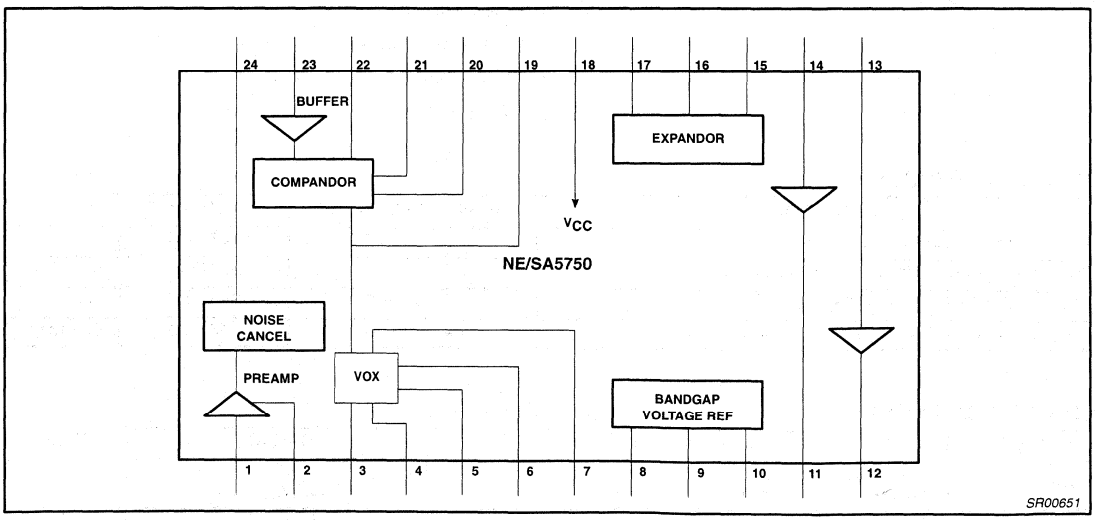


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5.0V, 0dB = 77.5mV_{RMS}. See test circuit, Figure 6.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
I_{CC}	Supply current	No signal Power down mode		8.4 1.8	12.0 3.0	mA mA
Z_L	Load impedance pins $NCAN_{OUT}$, EXP_{OUT}		50			kΩ
	$COMP_{OUT}$[1]		10			kΩ
Z_{IN}	Input impedance $COMP_{IN}$, MIC_{IN}, $SPKR_{IN}$		40	50	60	kΩ
	EXP_{IN}[2]		2.0	2.5		kΩ
	Noise cancellation current[4]	Pin 7, grounded	40	50	60	µA
V_{OS}	DC offset $NCAN_{OUT}$[3]		-50		50	mV

NOTES:
1. Compressor is tested in production with 50kΩ load.
2. Not tested in production.
3. Offset values are identical for both gain states of noise reduction circuit.
4. VOX threshold resistor at Pin 7, R3, should be greater than 3kΩ.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5.0V, 0dB level = 77.5mV_{RMS}. See test circuit, Figure 6.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Preamplifier gain range Preamplifier voltage gain 0dB Preamplifier voltage gain 40dB	 Pin 2 open Pin 2 AC ground	0 -1.0 39.0	 0 40	40 1.0 41.0	dB dB dB
	Preamplifier noise density	Pin 2 AC grounded RS = 0 - 50kΩ unweighted 20Hz-20kHz		7		$nV/\sqrt{Hz}$
		weighted CCIR DIN45405 20-20kHz		8		
	Switch amplifier gain		9	10	11	dB
	Sidetone attenuation range				30	dB
Compandor 1kHz, all tests[1]						
$COMP_{OUT}$	Compressor error at -21dB output level	Input level = -42dB		0.38		dB
$COMP_{OUT}$	Compressor error at -10dB output level	Input level = -20dB	-1.0		1.0	dB
$COMP_{OUT}$	Compressor error at 0dB output level	Input level = 0dB	-1.5	0.12	1.5	dB
$COMP_{OUT}$	Compressor error at +5dB output level	Input level = +10dB	-1.0		1.0	dB
$COMP_{OUT}$	Compressor error at +12.3dB output level	Input level = +24.6dB	-1.0		1.0	dB
EXP_{OUT}	Expandor error at -42dB output level	Input level = -21dB		-0.41		dB
EXP_{OUT}	Expandor error at -21dB output level	Input level = -10.5dB	-1.0		1.0	dB
EXP_{OUT}	Expandor error at -10dB output level	Input level = -5dB	-1.0		1.0	dB
EXP_{OUT}	Expandor error at 0dB output level	Input level = 0dB	-1.5	-0.18	1.5	dB
EXP_{OUT}	Expandor error at +10dB output level	Input level = +5dB	-1.0		1.0	dB
EXP_{OUT}	Expandor error at +24.6dB output level[2]	Input level = +12.3dB	-1.5		1.5	dB
EXP_{OUT}	Expandor V_{OS}	No signal	-50.0		50.0	mV
EXP_{OUT}	Expandor output DC shift	No signal to 0dB	-100		100	mV

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5.0V, 0dB level = 77.5mV_{RMS}. See test circuit, Figure 6.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Timing capacitors compandor			2.2		µF
THD	Total harmonic distortion					%
	Compressor	1kHz, 0dB		0.09	1	
	Expandor	1kHz, 0dB		0.09	1	
	$NCAN_{OUT}$	1kHz. Pin 2 open output level = 0dB		0.18	1	
		1kHz, Pin 2 open output level = +25dB		0.13	1	
	Speaker amplifier Drive capability				40	mA_{P-P}
	Output swing (<1% THD)	50Ω load	2	3.2		V_{P-P}
		100Ω load	3	4.1		V_{P-P}
		No load	4	4.9		V_{P-P}
	Ear amplifier Drive capability				10	mA_{P-P}
	Output swing (<1% THD)	300Ω load	3	4.3		V_{P-P}
		2000Ω load	4	4.9		V_{P-P}
		No load	4	4.9		V_{P-P}
VOX_{OUT}	Sink current				0.5	mA
	Low level	Open collector I_L = 0.5mA		0.07	0.4	V
	High level		4	5		V
VOX_{CTL}	Input current Low		-50	-21	0	µA
	High		-10		+10	µA
	Input level Low		0		1.5	V
	High		3.5		5	V
H_{PDN}	Input current Low		-10		+10	µA
	High		-10		+10	µA
	Input level Low		0		1.5	V
	High		3.5		5	V
	Reference filter capacitor			10		µF

NOTE:
1. Measurements are relative to 0dB output.
2. Measurement is absolute and indicative of the output dynamic range capability.

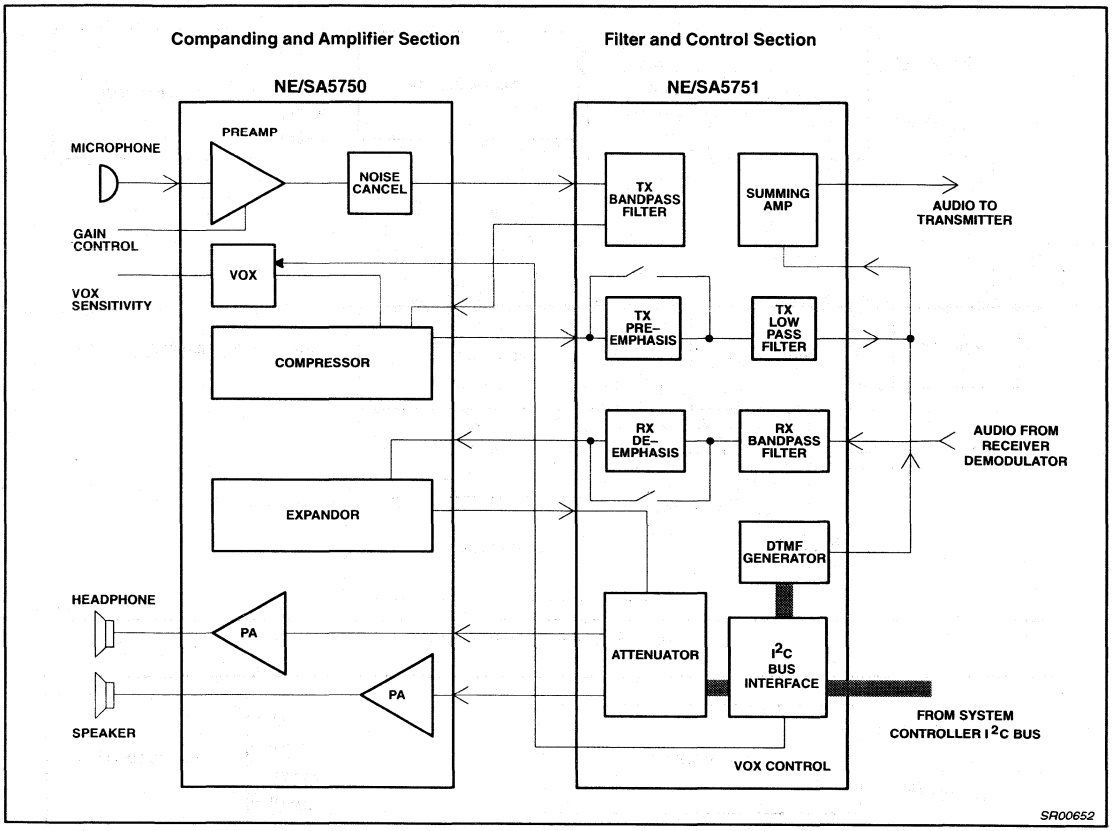


Figure 3. Typical Configuration of Audio Processor (APROC) System Chip Set

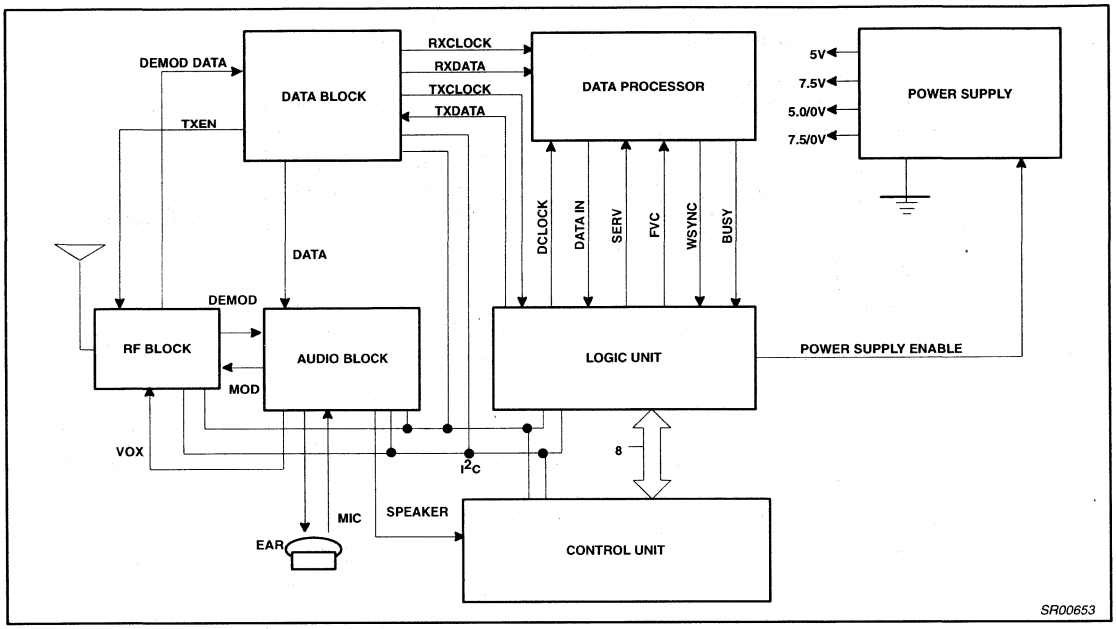


Figure 4. Cellular Radio System

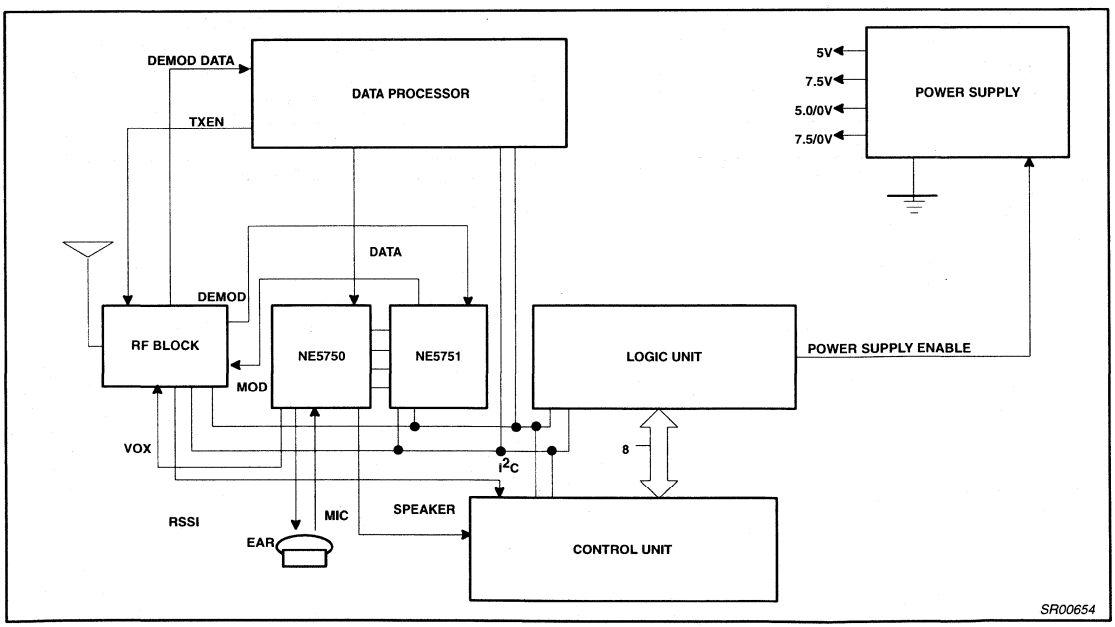


Figure 5. APROC Application Diagram

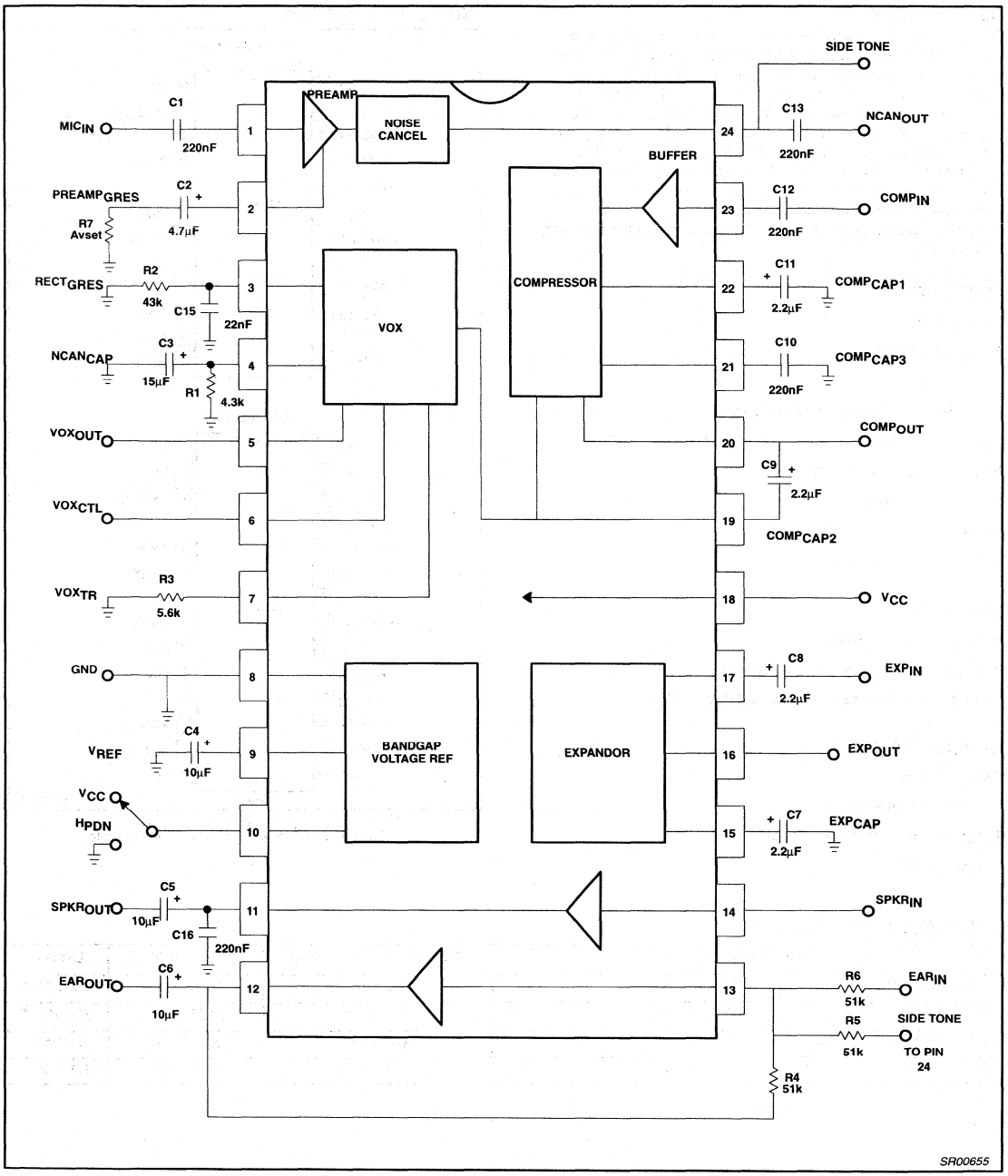


Figure 6. NE/SA5750 Test and Application Circuit

Audio processor - filter and control section | NE/SA5751

DESCRIPTION

The NE/SA5751 is a high performance low power CMOS audio signal processing system. The NE/SA5751 subsystems include complementary transmit/receive voice band (300-3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, a digitally controlled volume control with 30dB range (in 2dB steps), audio path mute switches, a programmable DTMF generator, power- down circuitry for low current standby, power-on reset capability, and an I²C interface. When the SA5751 is used with an SA5750 (companding function), the complete audio processing system of an AMPs or TACs cellular telephone is easily implemented.

FEATURES

- Low power
- High performance
- 5V supply
- Built-in programmable DTMF generator
- Built-in digitally controlled volume control
- Built-in peak-deviation limit
- I²C Bus controlled
- Power-on reset
- Power-down capability

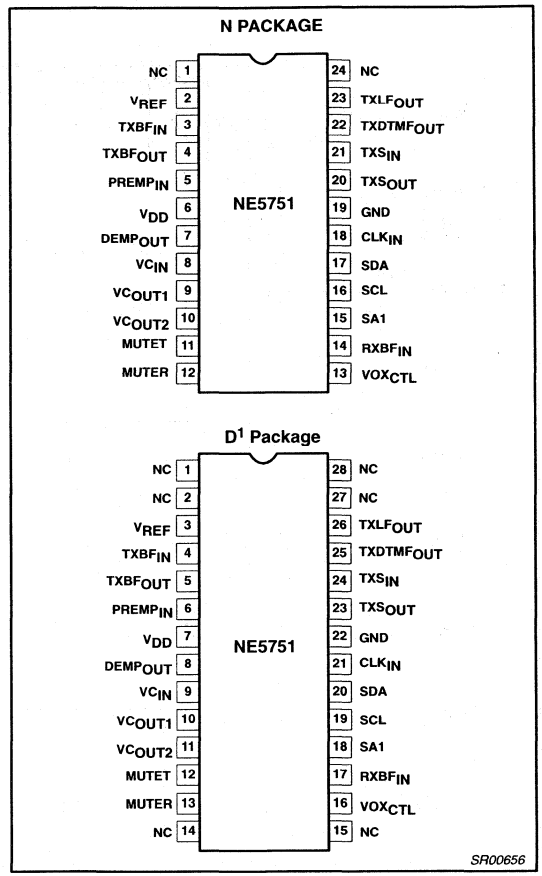
BENEFITS

- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5750

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION



NOTE:
1. Available in SOL (large surface mount) package only.

Figure 1. Pin Configurations

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5751N	SOT248-1
28-Pin Plastic Small Outline Large (SOL) package	0 to +70°C	NE5751D	SOT136-1
24-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5751N	SOT248-1
28-Pin Plastic Small Outline Large (SOL) package	-40 to +85°C	SA5751D	SOT136-1

PIN DESCRIPTIONS

PIN NO.		SYMBOL	DESCRIPTION
	(1)	NC	Not connected
1	(2)	NC	Not connected
2	(3)	V_{REF}	Reference voltage
3	(4)	$TXBF_{IN}$	Transmit bandpass filter input
4	(5)	$TXBF_{OUT}$	Transmit bandpass filter output
5	(6)	$PREMP_{IN}$	Pre-emphasis input
6	(7)	V_{DD}	Positive supply
7	(8)	$DEMP_{OUT}$	De-emphasis output
8	(9)	VC_{IN}	Volume control input
9	(10)	VC_{OUT1}	Volume control output 1
10	(11)	VC_{OUT2}	Volume control output 2
11	(12)	MUTET	TX analog voice path mute input
12	(13)	MUTER	RX analog voice path mute input
	(14)	NC	Not connected
	(15)	NC	Not connected
13	(16)	VOX_{CTL}	Vox control output
14	(17)	$RXBF_{IN}$	Receive bandpass filter input
15	(18)	SA1	Serial bus address
16	(19)	SCL	Serial clock line
17	(20)	SDA	Serial data line
18	(21)	CLK_{IN}	Clock input
19	(22)	GND	Ground
20	(23)	TXS_{OUT}	Transmit summer output
21	(24)	TXS_{IN}	Transmit summer input
22	(25)	$TXDTMF_{OUT}$	Transmit DTMF output
23	(26)	$TXLF_{OUT}$	Transmit low-pass filter output
24	(27)	NC	Not connected
	(28)	NC	Not connected

NOTE:
1. Callouts are for N package; those in parentheses are for the D (SOL) package.

BLOCK DIAGRAM

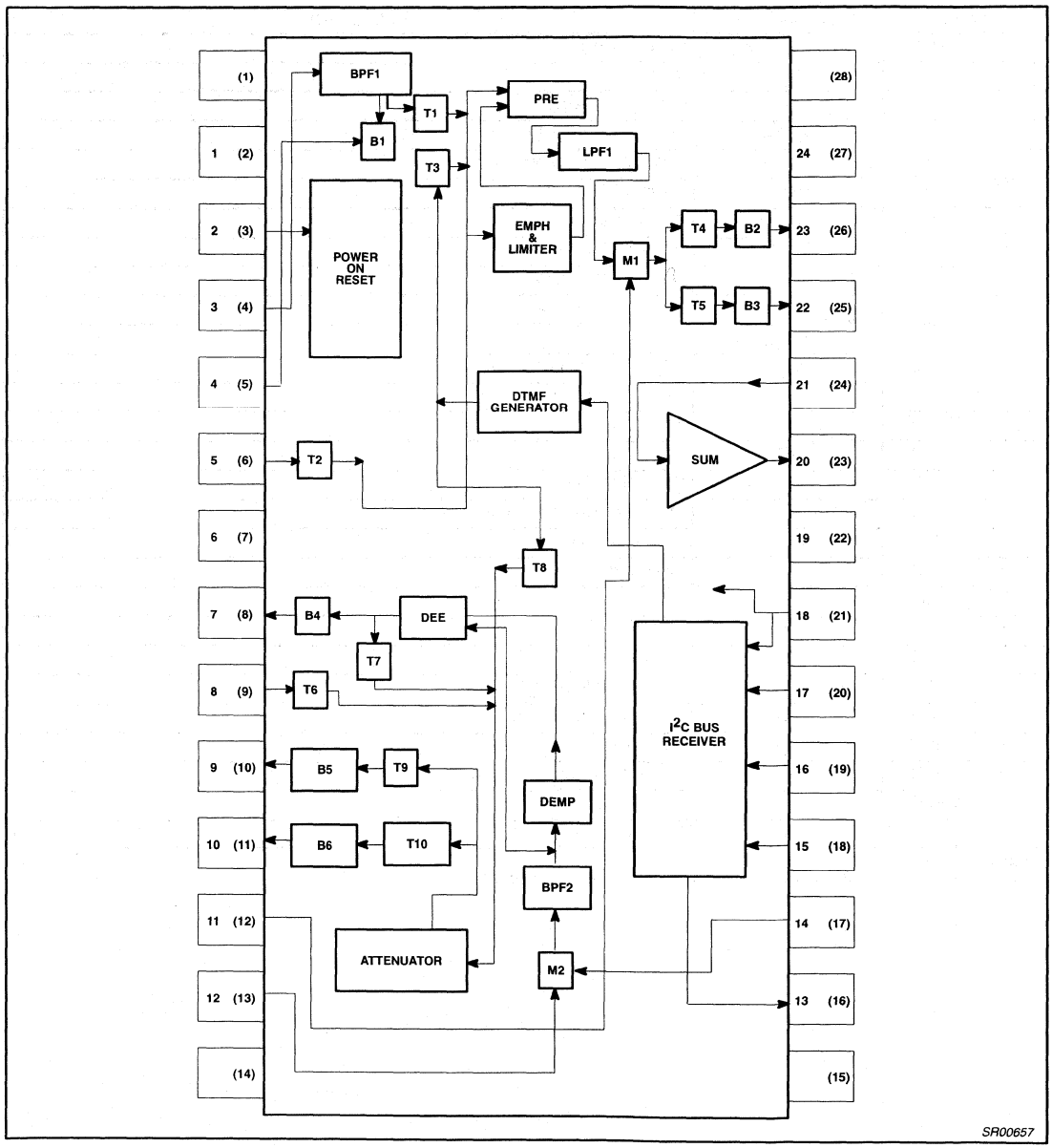


Figure 2. Block Diagram

NOTES:
1. T1 to T10 represent the signal path switches.
2. M1 and M2 represent the mute switches.
3. PRE and DEE represent the bypass switches for pre-emphasis and de-emphasis, respectively.
4. B1 to B6 represent the output buffers.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Power supply voltage[1]	6	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature NE5751	0 to 70	°C
	SA5751	-40 to +85	°C

NOTE:
1. Voltage applied to any pin -0.3 to V_{DD} +0.3V

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V, unless otherwise specified. See test circuit, Figure 6.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Power supply voltage range		4.75	5.0	5.25	V
I_{DD}	Supply current	Operating Standby		2.7 0.9	5.0 2.0	mA mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V. See test circuit, Figure 6. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV_{RMS} = -20dBm, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		500		kΩ
	RX BPF gain with de-emphasis	f = 1kHz	-0.5	0	0.5	dB
	RX BPF gain with de-emphasis	f = 100Hz		-31	-29	dBm0
	RX BPF gain with de-emphasis	f = 300Hz	9.0	9.6	11.0	dBm0
	RX BPF gain with de-emphasis	f = 3kHz	-11.0	-10.0	-9.0	dBm0
	RX BPF gain with de-emphasis	f = 5.9kHz		-68	-50	dBm0
	RX BPF noise with de-emphasis	300Hz-3kHz		170		μV_{RMS}
	RX dynamic range	with deemphasis		80		dB
	$DEMP_{OUT}$ output impedance	f = 1kHz		40		Ω
	$DEMP_{OUT}$ output swing (1%)	2.3kΩ to V_{REF}; f = 1kHz	V_{DD} -3	3.5		V_{P-P}
	VC_{OUT1} ouput swing (1%)	50kΩ toV_{REF}; f = 1kHz	V_{DD} -1	4.5		V_{P-P}
	VC_{OUT2} output swing (1%)	50kΩ to V_{REF}; f = 1kHz	V_{DD} -1	4.5		V_{P-P}
	VC_{OUT1} noise	VC_{IN} grounded C - message		25		μV_{RMS}
	VC_{OUT2} noise	VC_{IN} grounded C - message		25		μV_{RMS}
	Mute threshold off		0		0.8	V
	Mute threshold on		2.0		5.0	V
	CLK1, 2 high		4.0		5.0	V
	CLK1, 2 low		0		1.0	V
	TX BPF anti alias rejection			40		dB
	TX BPF input impedance	f = 3kHz		500		KΩ

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	TX BPF noise	300 - 3000kHz		90		μV_{RMS}
	TX LPF gain	f = 5.9kHz		-39	-36	dB
	TX LPF gain with pre-emphasis	f = 1kHz, 20dBV		12.06		dB
	TX LPF gain with pre-emphasis	f = 100Hz		-19		dBm0
	TX LPF gain with pre-emphasis	f = 300Hz		-10.45		dBm0
	TX LPF gain with pre-emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre-emphasis	f = 5900Hz		-39		dBm0
	TX LPF gain with pre-emphasis	f = 9kHz		-51		dBm0
	TX overall gain	1kHz	11.3	11.8	12.5	dB
	TX overall gain	100Hz		-47	-45	dBm0
	TX overall gain	300Hz	-11	-10.4	-9	dBm0
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		-52	-45	dBm0
	TX BPF output impedance	f = 1kHz		360		Ω
	TX BPF output swing (1%THD)	50kΩ to V_{REF} f = 1kHz		4.5		V_{P-P}
	TX BPF dynamic range			90		dB
	$PREMP_{IN}$ input impedance	f = 3kHz		500		kΩ
	Summing op amp					
	Slew rate	C_L = 15pF		0.75		V/μs
	Output impedance	Unity gain; f = 3kHz		40		Ω
	Output swing (1% THD)	1kHz, 5kΩ load (25°C)		4.3		V_{P-P}
	Volume control accuracy	-30dB to 0dB	-1	0	+1	dB
	Analog switches					
	Insertion loss			60		dB
	On time transition	MUTET, MUTER 0.8V ->2.0V		3		μs
	Off time transition	MUTET, MUTER 2.0V ->0.8V		0.25		μs

I²C CHARACTERISTICS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are high. Data transfer may be initiated only when the bus is not busy.

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired-AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

Due to the variety of different devices which can be connected to the I²C bus, the levels of the logical "0" and "1" are not fixed and depend on the appropriate level of V_{DD}. For the typical supply voltage of 5V which is chosen here, logical "1" and logical "0" are, however, fixed respectively on maximum input LOW voltage, 1.5V and minimum input HIGH voltage, 3.0V.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock's cycle. If it does not remain HIGH, it may be interrupted as a control signal.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition S. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

SYSTEM CONFIGURATIONS

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master"; and devices which are controlled by the master are the "slaves".

ACKNOWLEDGE

The number of data bytes transferred between the start and the stop condition from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set up and hold times must be taken into account.

I²C BUS DATA CONFIGURATIONS

The NE5751 is always a slave receiver in the I²C bus configuration (R/W bit-0). The slave address consists of seven bits in the serial mode where the least significant bit is selectable by hardware on input A0 and the other more significant bits are internally fixed.

POWER ON RESET

In order to avoid undefined states of the NE5751 when the power is switched on, a power on reset is supplied. The reset is active when Pin V_{REF} is held below 0.8V. The reset is off when Pin V_{REF} is above 2.0V. Pin V_{REF} is normally at 2.5V generated by a resistive divider from V_{DD}. Nominal impedance is 20kΩ. In a typical application a capacitor is connected to Pin V_{REF} to improve power supply rejection. The time delay of the network resets the internal registers when power is first applied. The signal paths are off in the reset condition. The NE5751 must be programmed via the I²C bus for normal operation. The Power Down mode is defined only when all register values are zero.

CONTROL REGISTERS

Register Map

The address register is as follows:

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	SA1	0

SA1 is controlled by serial bus address pin.

Signal Path Register

MSB							LSB
T10	T9	T8	T6	VOX_{EN}	T4	T3T5	T2

T2 is the transmission gate between Pin $PREEMP_{IN}$ and the emphasis input.

T3T5 connects the output of the DTMF generator to the emphasis input and connects the output of the XMT LPF to Pin $TXDTMF_{OUT}$.

T4 connects the output of the XMT LPF to Pin $TXLF_{OUT}$.

VOX_{EN} enables the VOX function of NE5750.

T6 connects Pin VC_{IN} to the volume control.

T8 connects the output of the DTMF generator to the volume control.

T9 enables VC_{OUT1}.

T10 enables VC_{OUT2}.

Volume Control and Test Register

MSB							LSB
PDW	T1T7	DEE	PRE	V1	V2	V3	V4

V4 is volume control bit 4. This is the MSB. A zero is 16dB attenuation.

V3 is volume control bit 3. A zero is 8dB attenuation.

V2 is volume control bit 2. A zero is 4dB attenuation.

V1 is volume control bit 1. A zero is 2dB attenuation.

PRE is the bypass for the pre-emphasis.

DEE is the bypass for the de-emphasis.

T1T7 is the bypass for the compressor and expandor.

PDW is the control for power down mode.

This mode is defined only when all register values are reset to zero.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

High Frequency = 1200kHz/6/HD
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

Low Frequency = 1200kHz/12/LD
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading the two DTMF registers before 96ms have elapsed.

Single tones can be obtained by loading 0, 1 or 2 into one of the registers to silence it.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during operation.

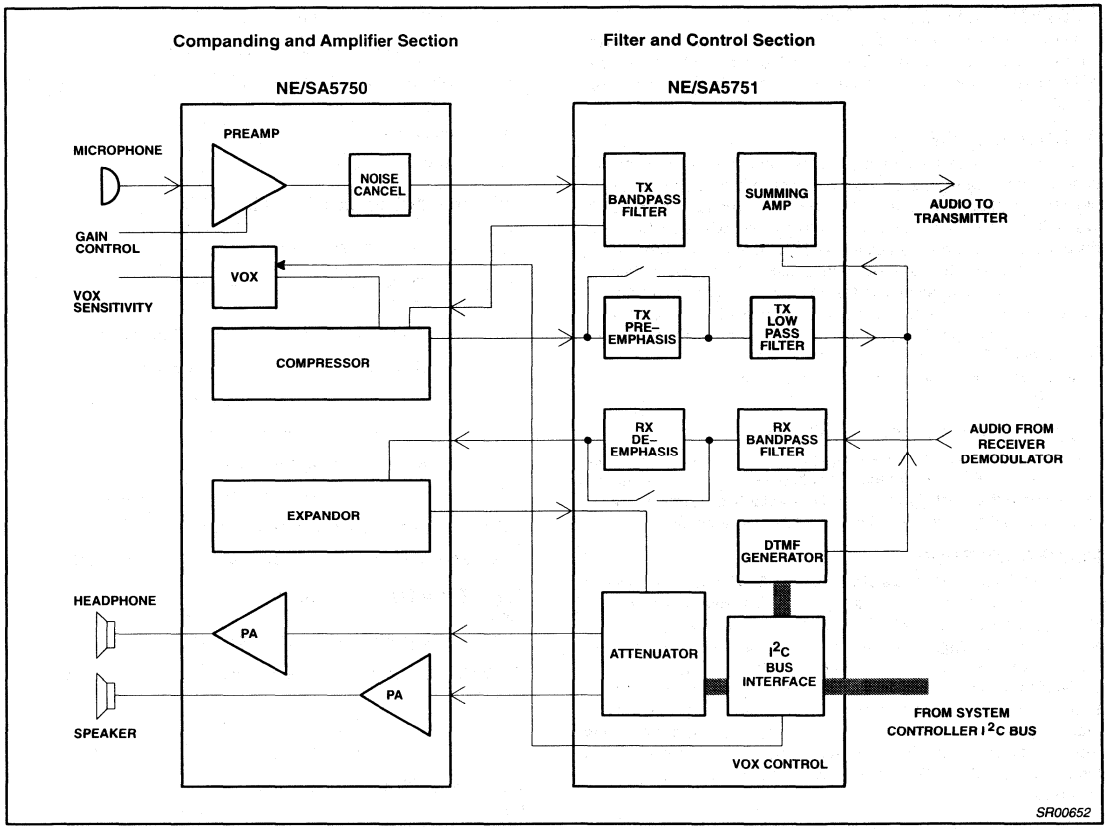


Figure 3. Typical Configuration of Audio Processor (APROC) System Chip Set

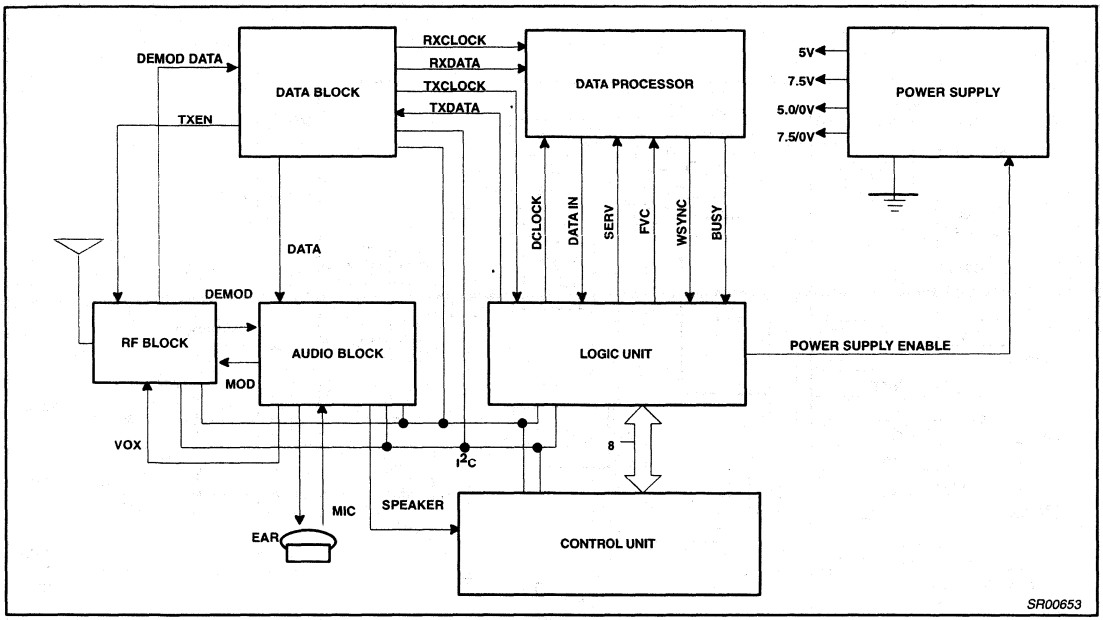


Figure 4. Cellular Radio System

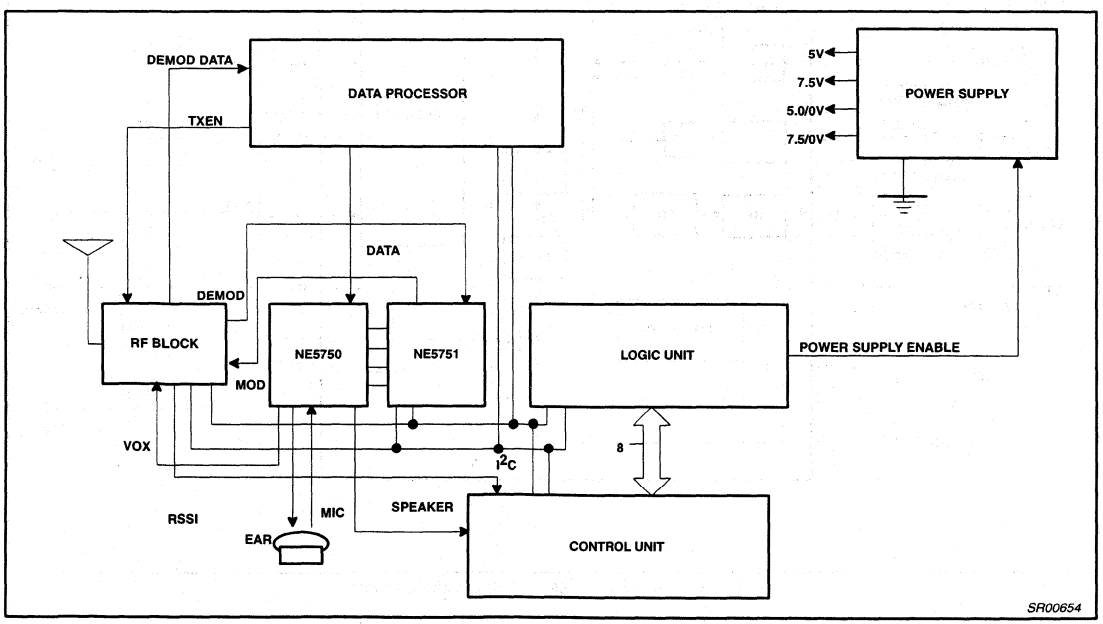


Figure 5. APROC Application Diagram

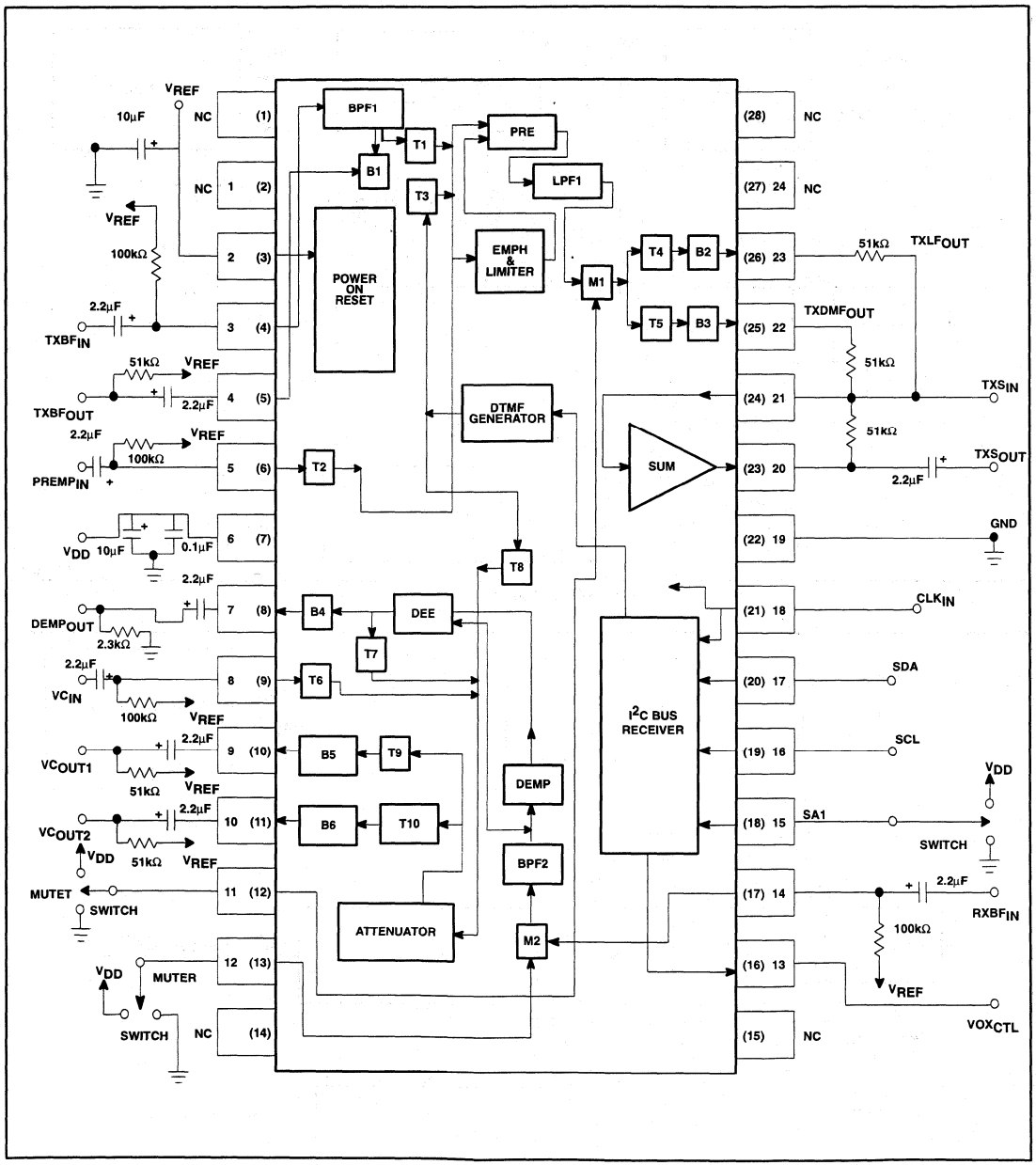


Figure 6. NE/SA5751 Test and Application Circuit

PERFORMANCE CHARACTERISTIC

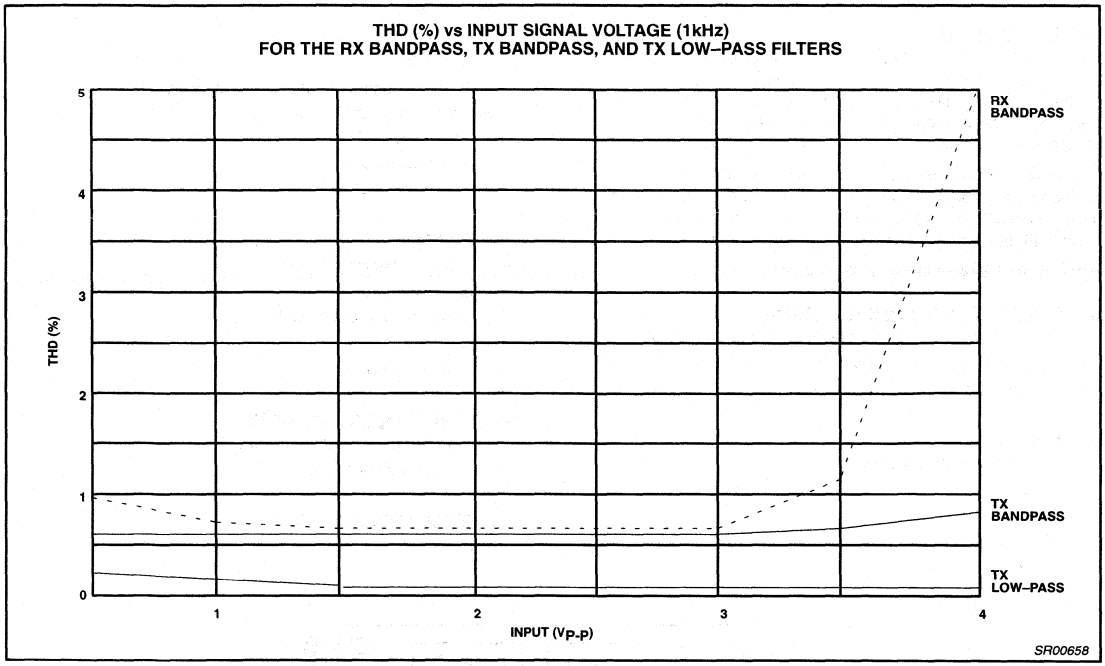


Figure 7. Performance Characteristics

Using the NE5750 and NE5751 for audio processing AN1741

Author: Alvin K. Wong

INTRODUCTION

The NE5750 and the NE5751 are two audio processor chips that can be used in RF communications. The chip-set processes a voice so that by the time it is transmitted and received, the quality is preserved. This is accomplished through the use of compression/expansion and pre-emphasis/ de-emphasis.

The audio processor chip-set (APROC) has a wide variety of high performance applications such as cellular phones, cordless voice microphones, cordless intercom systems, standard phones, and hand-held, base, or mobile two-way communications equipment.

Below is an outline of this application note:

I. WHAT IS AUDIO PROCESSING

- How the Voice is Processed by the NE5750 and NE5751
- More Detail on the Key Features
- Performance Graphs

II. NE5750

- A Breakdown of the NE5750
  - •preamp
  - •noise canceller
  - •VOX
    - ♦VOX_{OUT} and VOX_{CTRL}
    - ♦setting the threshold
  - •Compandor
    - ♦compressor
    - ♦expandor
    - ♦how to measure the attack and recovery time
  - •Amplifier Section
    - ♦speaker amplifier
    - ♦earphone amplifier
- How to Power Down

III. NE5751

- A closer look at the NE5751
  - •transmit path
    - ♦limiter and all-pass circuit
  - •receive path
- I^2C Bus Receiver

IV. APROC DEMO-BOARD

- How to Power Down the Chip set
- Component list and layout

V. NE5750 DEMO-BOARD

- Component list and layout

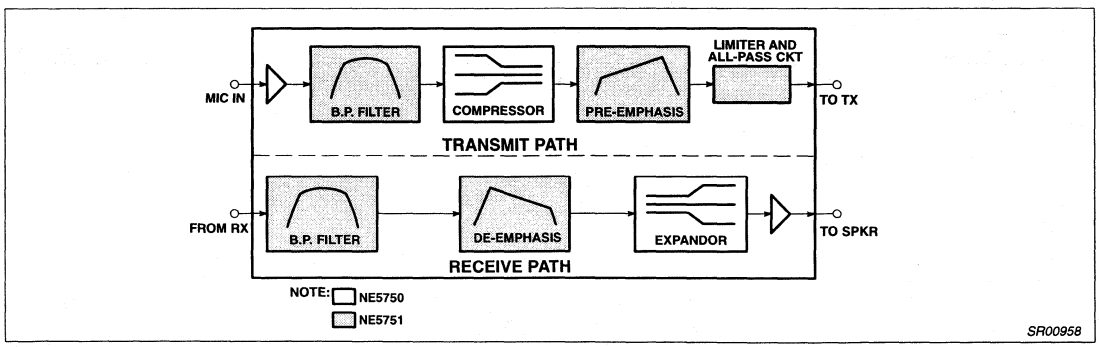


Figure 1. Key Functions of the NE5750 and NE5751 That Contribute to Improving the S/N Ratio and Sensitivity in the System.

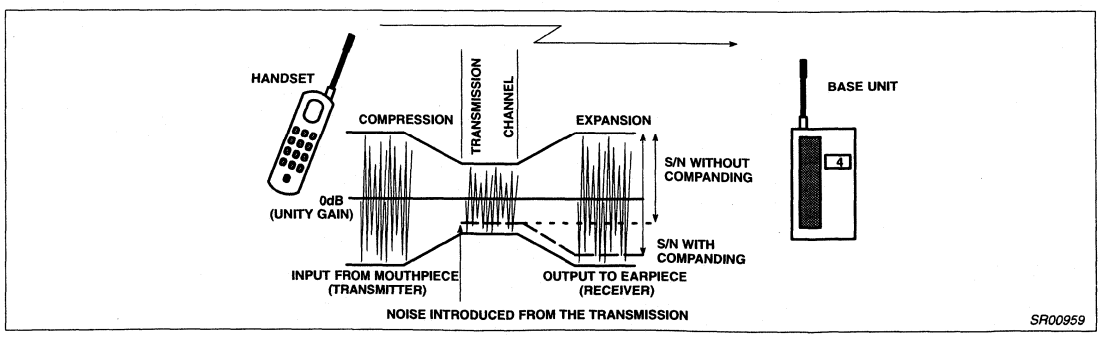


Figure 2. S/N Ratio With Companding vs Without Companding

VI. QUESTION AND ANSWER SECTION

I. WHAT IS AUDIO PROCESSING

HOW THE VOICE IS PROCESSED BY THE NE5750 and NE5751:

Audio processing begins when a person speaks into a microphone (see Figure 1). The signal is first amplified by the preamp, then screened by a bandpass filter. After the noise is filtered out, the voice signal is processed by the compressor. The function of the compressor is to attenuate loud voices and amplify soft ones. The upper voice frequencies are then amplified by pre-emphasis before their voltage amplitudes are restricted by the limiter and all-pass circuit. When this is completed, the processed voice is ready for transmission.

Since the voice signal was processed by the APROC before transmission, it must be unprocessed upon reception. The received signal is screened again so that the unwanted received noise is blocked before it goes

through de-emphasis. In de-emphasis, the upper voice frequencies are attenuated. Then the signal is expanded back to its primary dynamic range by the expandor. Because the voice is restored to its original state, it is ready for amplification by the power amp whose output can be connected to an external speaker. The receiving party will now be able to hear the transmitting party.

MORE DETAIL ON THE KEY FEATURES:

During compression, low level signals are amplified to "jump" over the transmitter channel noise, while the high level signals are compressed to prevent distortion. In general, because we are dealing with a limited dynamic range transmission medium, it is desirable to compress the signal prior to transmission. However, in order to preserve the dynamic range of the original voice signal, the compressed signal is expanded at reception. Figure 2 shows a diagram of a cordless phone application using companding. Note the signal-to-noise ratio with and without companding.

Another key function of the APROC is the pre-emphasis/de-emphasis capability which is used to overcome the "colored" noise, present in all FM receivers, generated by the FM demodulator. This noise worsens at the upper voice band as shown in Figure 3. Therefore, to keep the same signal-to-noise ratio in the lower and upper voice bands, pre-emphasis/de-emphasis is required. A person with a high-pitched voice will now be heard just as well as a person with a low, deep voice.

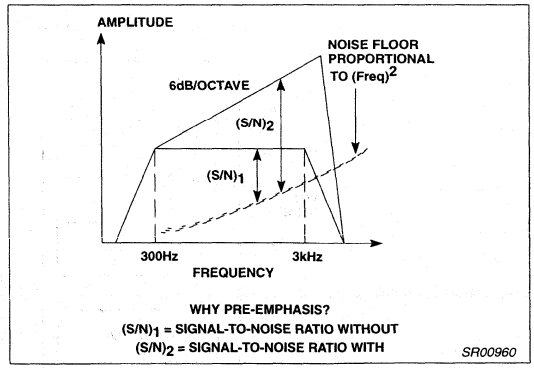


Figure 3. Pre-emphasis Response

Another key stage of the APROC is the limiter with the all-pass circuit. Its main function is to limit the amplitude of the voice signal so that the maximum frequency deviation is limited to 12kHz. Cellular radio specifications allow for a 30kHz channel spacing with an audio bandwidth of 3kHz. Therefore, by Carson's rule the maximum frequency deviation of the limiter must be 12kHz as shown below.

1. Bandwidth = 2 (Modulating Freq + Max Freq Dev)

or

2. Max Freq Dev = Bandwidth/2 – (Mod Freq)
= 30kHz/2 - 3kHz
= 15kHz-3kHz
= 12kHz

PERFORMANCE GRAPHS OF APROC DEMO-BOARD:

Figure 4 shows the general diagram of the audio processor chip set without the external components. External components for the chip set can be found in Figure 31, and the values were chosen for AMPS/TACS specs. To demonstrate the performance of the chip set, data was taken in the lab and resulted in the following figures.

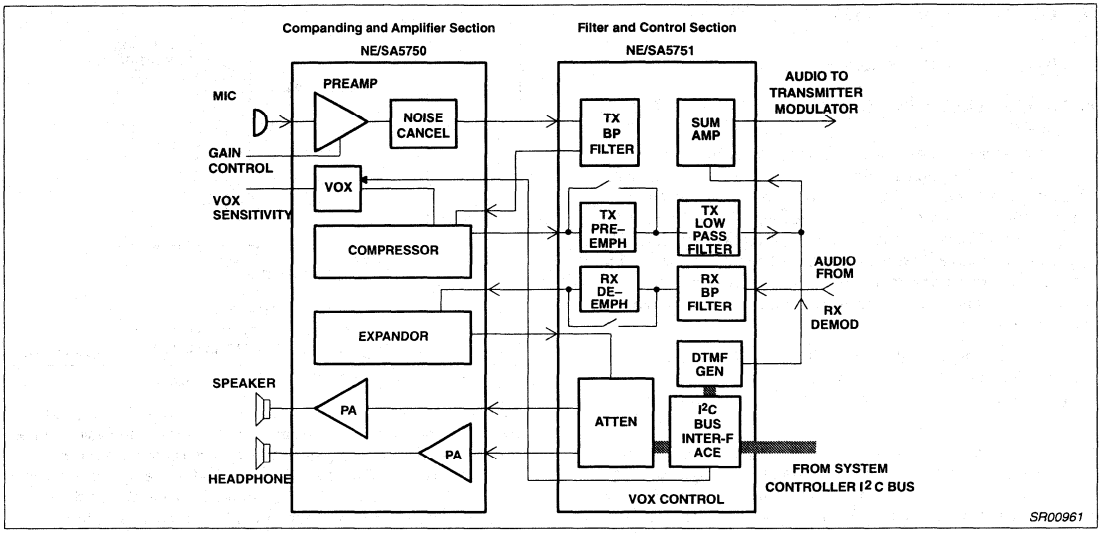


Figure 4. Typical Configuration of Audio Processor (APROC) System Chip Set

Figure 5 Description

Figure 5 reveals what the signal would look like on the bench with different input levels. Figures 5a, b, and c all use the same audio input signal. The audio signal (0-6kHz) varies from 20dB to -30dB in 10dB steps.

Figure 5a

This graph shows the Tx channel. Notice the signal's increase in amplitude as the frequency is increased due to pre-emphasis. Additionally, the slope of the signal decreases as the input increases.

The compressor function is readily shown where a 5dB change in the output level occurs for every 10dB change in the input.

Figure 5b

The 2:1 expansion of audio (20dB change for every 10dB), bandpass filtering and the de-emphasis filter response (300-3kHz) are shown. The graph shows the Rx channel. Notice the signal's decrease in amplitude as the frequency increases due to de-emphasis.

Figure 5c

This shows that a flat frequency response is achieved upon normal reception. Notice the 20dB gap, although the input steps are for 10dB. This is due to the noise canceller turning on. The decrease in amplitude for higher level, higher frequency tones is the result of the deviation limiter action.

After studying these figures, a designer will have a graphical understanding of how the APROC processes a signal.

Figure 6 shows the test set-up using the APROC demo-board to simulate a real cellular phone call. Audio noise is added to the input of the microphone and RF noise is added to the receiver. The table for Figures 7-10 describes what the associated waveforms reveal when certain key stages of the APROC are activated or bypassed.

As seen from the following figures, there is a definite advantage in using the chip set in high performance communication systems.

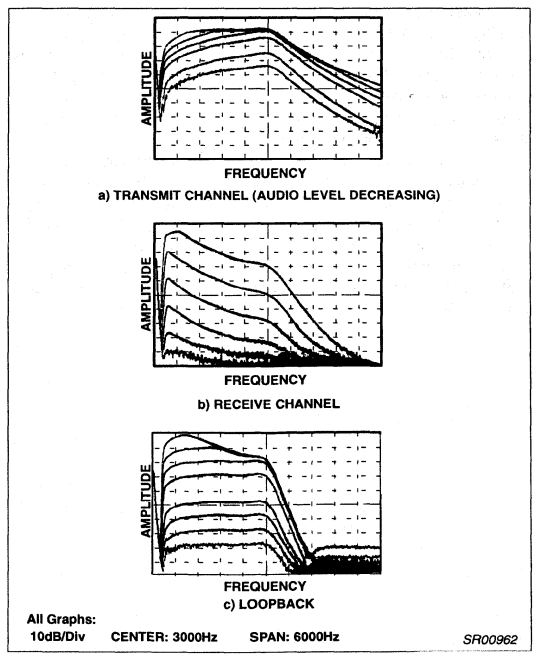


Figure 5.

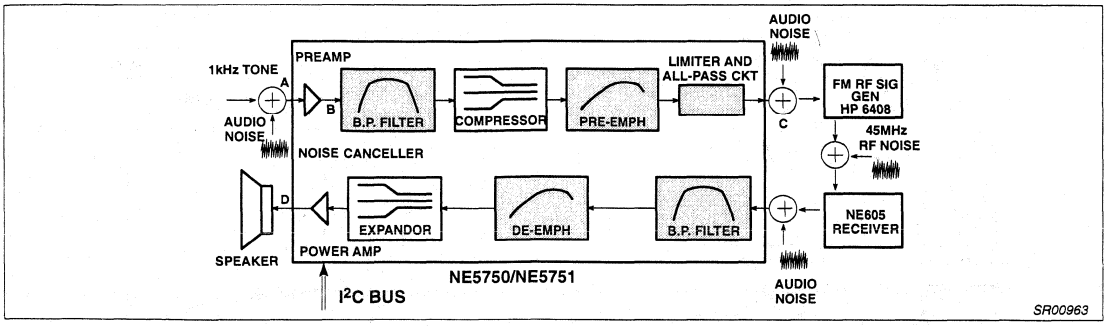


Figure 6. NE5750/NE5751 Test Set-Up

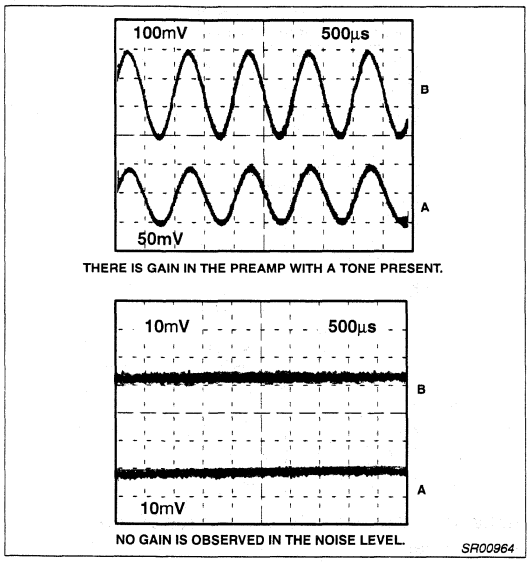


Figure 7.

Figure	Description
7	No noise gain is observed at the output of the Tx channel because of the noise canceller circuit.
8	Shows why companding and emphasis are needed to improve the quality of the audio signal when BASEBAND NOISE is present in the system
9	Shows why companding and emphasis are needed to improve the quality of the audio signal when RF NOISE is present in the system.
10	Shows that the sensitivity and the signal-to-noise ratio of a receiver improved due to audio processing.

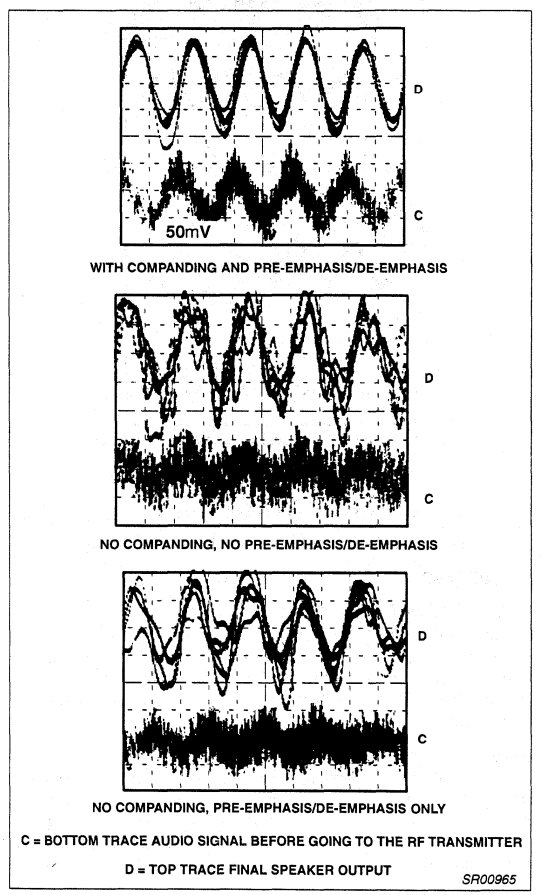


Figure 8. Audio Output with Baseband Channel Noise

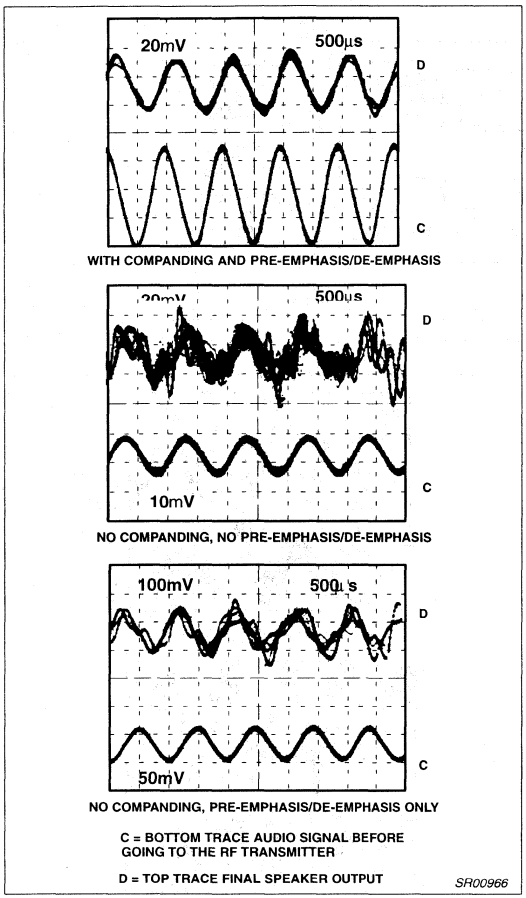


Figure 9. Audio Output with a Noisy RF Channel

II. NE5750

A CLOSER LOOK AT THE NE5750:

Referring to Figure 11, the NE5750 has seven main features which make this chip unique: preamp, noise canceller, VOX, compressor, expandor, buffer, and power amplifiers. (NOTE: All component labels in this section are referenced to Figure 11, unless otherwise indicated.)

Preamp:

The NE5750 provides a preamp with adjustable gain. This allows the designer to boost the low level audio signal coming out of the microphone. The microphone can be connected to Pin 1 through a DC blocking capacitor, C1 (see Figure 12). The input impedance at this Pin is 50kΩ.

The preamp gain of the NE5750 can be adjusted from 0dB to 40dB by an external resistor, R7, connected to Pin 2 through a capacitor C2. Below is a formula which allows the designer to determine the value of R7 for a certain value of gain.

If a designer wanted a preamp gain of 20dB, a 5kΩ resistor would be required (see Table 6).

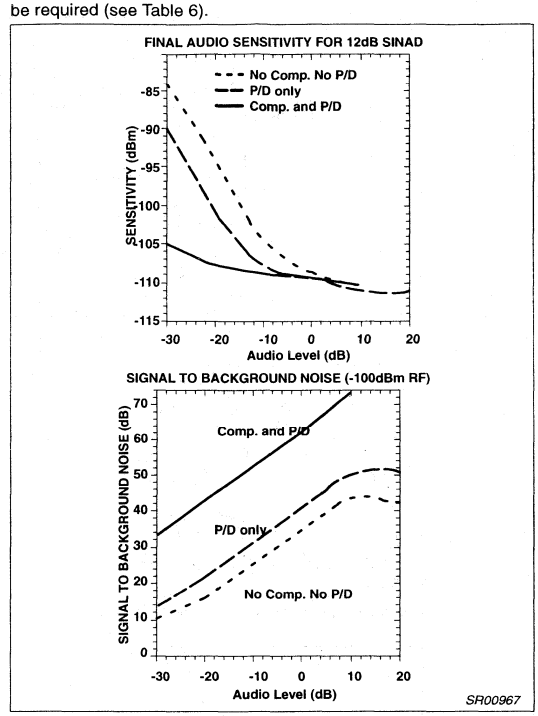


Figure 10.

$$R7 = \left[\frac{50,000}{10^{\left(\frac{X(dB)}{20}\right)} - 1}\right] - 500 \qquad (1)$$

"X" in dB

Table 6. Calculated R7 Values for Different Preamp Gains

X (dB)	R7
0	Leave Pin 2 open
5	64k
10	22k
15	10k
20	5.1k
25	2.5k
30	1.1k
35	405
40	Pin 2 AC grounded

Noise Canceller:

The output of the preamp is connected to the input of the noise canceller circuit which is internal to the device. The function of the noise canceller is to automatically provide a
set gain of either 0dB when no signal is present, or 10dB when a signal is present. With this feature, background noise is minimized from transmission.

This automatic gain setting can only be implemented when the noise canceller circuitry is used in conjunction with the VOX circuitry. The threshold and attack and release time can be set externally. This will be described in more detail in the "VOX" section.

Although the noise canceller circuit is really designed to be used with the VOX circuitry, it can be implemented without it. The noise canceller circuit can be set up to provide either 0dB or 10dB of gain at all times (regardless of the presence of a signal). Table 7 shows how to achieve either gain settings when the VOX function is bypassed.

Table 7. Setting Up the Gain of the Noise Canceller

Pin No.	Gain of Noise Canceller	
	0dB	10dB
3	Ground	Ground
4	Ground	V_{CC}
7	10k to GND	Ground

The output of the noise canceller is accessible to the designer at Pin 24. C13 is used as a DC blocking capacitor.

VOX:

As mentioned earlier, the VOX circuitry works together with the noise canceller circuit. Pins 3, 4, 5, 6, and 7 all deal with the VOX's performance.

All of the resistor and capacitor values given in the NE5750 data sheet are chosen to meet AMPS/TACS specification for cellular radio. So any deviation from these values should be considered carefully if the application is in cellular radio.

Connected to Pin 3 is a resistor R2 and capacitor C15, as shown in Figure 13. These components set the gain of the VOX. The values here are for internal use only and have no direct relationship with the performance. So the values should be kept as shown. In some special applications, R2 may be adjusted such that the voltage on Pin 4 can be increased. By increasing this voltage, the voltage on Pin 7 can be set to a higher range (more details later).

Pin 4 has C3 and R1 connected to it which affects the attack and release time of the VOX circuit. In general the attack time should be faster than the release time.

The values given for C3 and R1 provide an approximate attack time of 12ms and release time of 120ms. These values should be kept as shown.

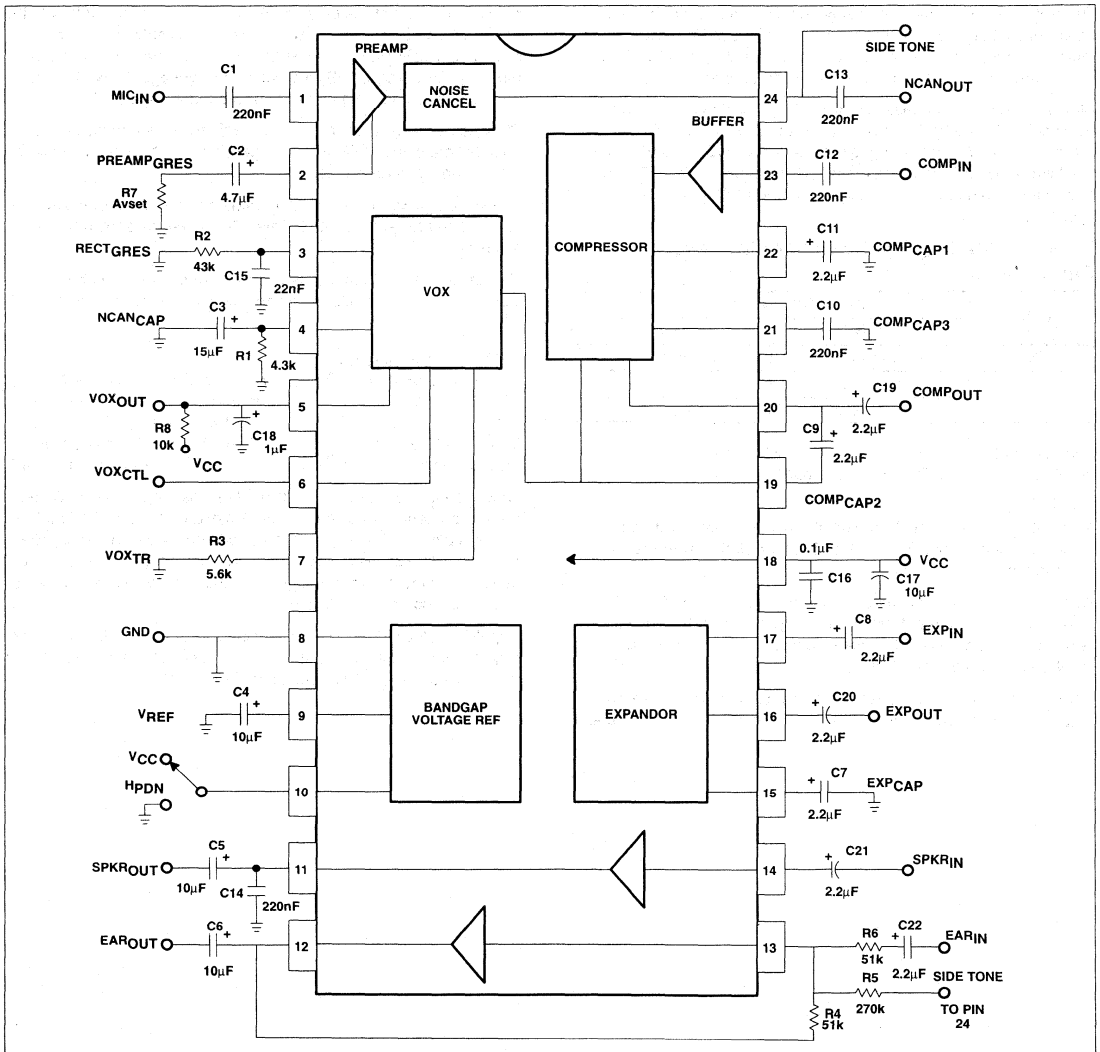
The timing of the VOX circuit is important because it controls the gain of the noise canceller, and can also turn the transmitter on and off.

- VOX_{OUT} and VOX_{CTRL}

By using VOX_{OUT} and VOX_{CTRL}, Pins 5 and 6 respectively, the NE5750 can control the status of the transmitter. The VOX_{OUT} Pin should have a 10kΩ pull-up resistor to V_{CC}. When probing Pin 5, a logic '1' or '0' will be read. The VOX_{CTRL} pin should have a logic '1' or '0' connected to it. Table 8 shows how Pins 5 and 6 can be used:

Having a logic '0' on Pin 6 is sufficient in most applications. When voice is present, the noise canceller kicks on while the VOXout Pin supplies a logic '1'; when voice is not present, VOXout Pin supplies a logic '0'. In a cordless phone application this logic level could be used to turn the transmitter on and off, thereby conserving power for any battery operated applications.

Supplying a logic '1' on Pin 6 would cause the transmitter to stay on regardless of any signal input to Pin 1. However, the functionality of the noise canceller will still be signal dependent.



NE5750 COMPONENT LIST

- C1 DC blocking cap for Mic amp
- C2 DC blocking cap for Mic gain
- C3 used to set attack and release time of VOX
- C4 V_{REF} filter capacitor
- C5 DC blocking cap for speaker at Pin 11
- C6 DC blocking cap for EAR_{OUT} pin
- C7 sets attack and release time for expandor
- C8 DC blocking cap for expandor's input
- C9 AC bypassing for compressor
- C10 passes AC to GND
- C11 sets attack and release time of compressor
- C12 DC blocking cap for compressor's input
- C13 DC blocking cap
- C14 low pass filtering for speaker output
- C15 used for filtering, internal use only
- R1 used to set release time of VOX
- R2 set gain of VOX, but for internal use only effects voltage on Pin 4
- R3 sets threshold level of VOX
- R4 feedback resistor for ear amp
- R5 sets gain of ear amp for side tone signals
- R6 sets gain of ear amp for baseband signals
- R7 sets microphone preamp gain

ADDED FOR NE5750 DEMO-BOARD

- R8 pull-up resistor to get logic levels out
- C16 bypass capacitor
- C17 bypass capacitor
- C18 passes AC to GND (low pass)
- C19 DC blocking cap for compandor out
- C20 DC blocking cap for expandor out
- C21 DC blocking cap for speaker in
- C22 DC blocking cap for ear in

SR00968

Figure 11. NE/SA5750 Application Demo-Board

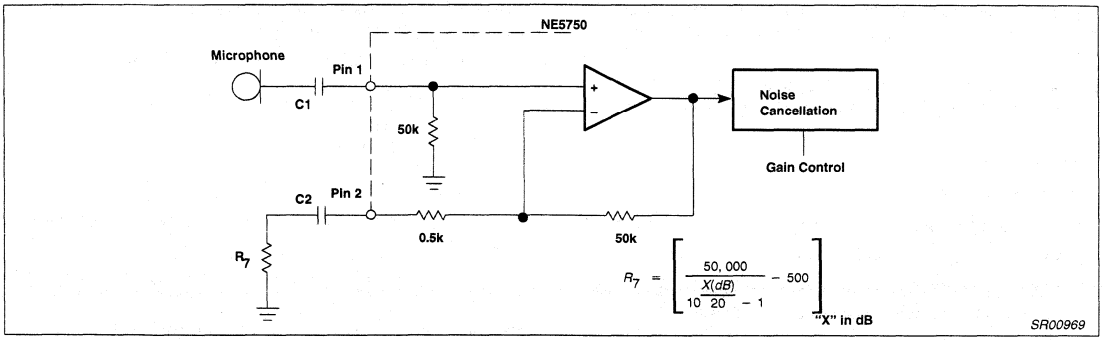


Figure 12. Setting Microphone Preamplifier Gain

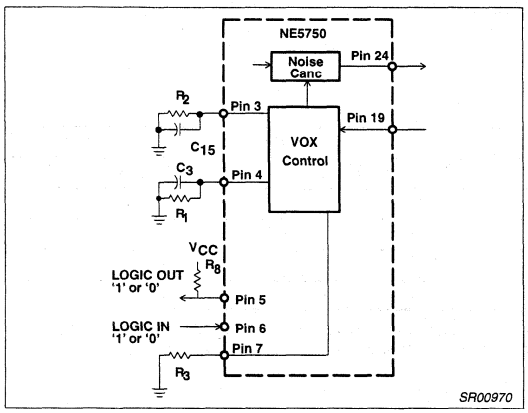


Figure 13. VOX Circuit

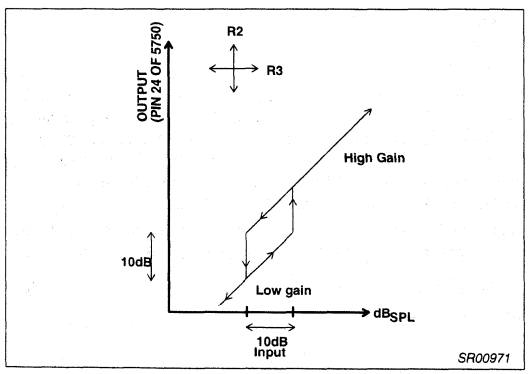


Figure 14.

This condition is mainly used if the battery consumption is not a problem. Such a condition would be for any car cellular radios.

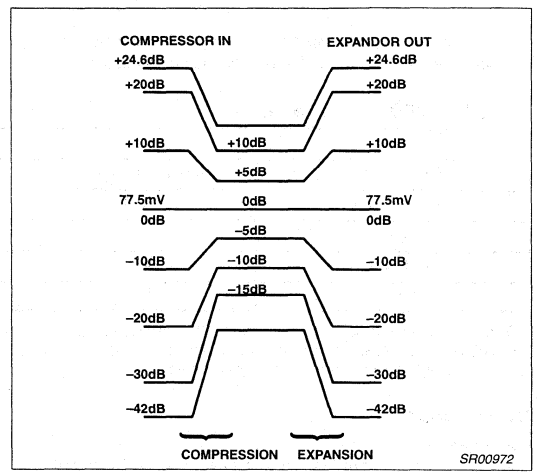


Figure 15. Compandor Dynamic Range

- setting the threshold

R3 at Pin 7 is used to set the threshold of the VOX. Setting the threshold determines the voltage level input at which the noise canceller and VOX will activate. Formula 4 shows how to calculate the VOX's threshold.

$$VOX_{THRESH}\ (mV) = 50\mu A \cdot R3\ (K\Omega) \quad (4)$$

Where R3 > 3kΩ)

If R3 = 5.6k, the measured voltage at Pin 7 should be approximately 280mV.

The way to adjust the VOX is to first determine what signal level is desired at Pin 1 to activate the VOX noise canceller circuits. Once that level is applied to Pin 1, connect a voltmeter to Pin 4. The voltage level measured here should be plugged into formula 4 to determine R3.

As mentioned earlier, the voltage at Pin 4 can be increased by R2. But one should only deviate from the R2 value if the voltage at Pin 7 cannot come down. In most cases, setting R2 to 43kΩ and setting Pin 7 to the voltage at Pin 4 is sufficient.

Figure 14 shows graphically how R3 and R2 affect the location of the "box". The "box" is always 10dB, which is due to the noise canceller circuit.

EXAMPLE I : Set the VOX threshold such that it "kicks on" when $30mV_{P-P}$ is applied to Pin 1 of the NE5750 with a preamp gain of 0dB.

Step 1: Make sure:

a. Pin 7 is left open.

b. The VOX attack and recovery components are in place at Pin 4.

c. R2 and C15 are connected to Pin 3.

d. If using the NE5750 alone, be sure to connect the preamp output (Pin 24) to the compressor input (Pin 23) with a DC blocking cap.

e. The preamp gain is already set (in this instance the preamp gain is 0dB).

f. Make sure that the compressor's components are also connected; compressor's attack time has to be functional

Step 2: Apply a constant 1kHz sinewave signal to Pin 1 with the desired threshold. In this case, $30mV_{P-P}$.

Step 3: Measure the DC voltage on Pin 4; V4=260mV

Step 4: Calculate R3:

$$R3 = V4(V)/(50\mu A) = 0.260/50\mu A = 5.2k$$

let's use a 5.3kΩ

Step 5: Connect R3 to Pin 7 and verify that VOX "kicks on" at the desired threshold.

- This set-up has the VOX kicking on at $30mV_{P-P}$ and kicking off at $11mV_{P-P}$.

Referring to the above example, if a preamp gain of 10dB was chosen before setting the threshold, the threshold will also change. So it is vital that the preamp gain be set before setting the VOX threshold.

Table 8. VOX Truth Table

Inputs		Outputs	
Voice (Pin 1)	**VOX_{CTRL} (Pin 6 of NE5750)**	**Noise Canceller Gain**	**VOX_{OUT}**
Not Present	logic '0'	0dB	logic '0'
Present	logic '0'	10dB	logic '1'
Not Present	logic '1'	0dB	logic '1'
Present	logic '1'	10dB	logic '1'

NOTE: To apply a logic '0' on Pin 6 by the I^2C evaluation program, be sure that the VOX_{EN} is high, and low for a logic '1' on Pin 6. If the NE5750 is used alone, be sure that the output of the noise canceller is AC coupled to the input of the compressor. Also, make sure that all of the components for the compressor are connected.

Compandor:

- compressor

The compressor input at Pin 23 requires an external DC blocking capacitor (C12). The input impedance is roughly 50kΩ. Unlike the older compandors, this input can be directly driven from CMOS circuits (e.g. NE5751).

The gain from the preamp should be adjusted such that there is enough signal getting to the compandor. However, one must be careful not to overdrive the inputs. Additionally, do not forget the extra 10dB gain from the noise canceller (assuming it is being used).

Figure 15 shows the typical dynamic range of the compandor. The maximum input signal that the compressor can handle is $3.72V_{P-P}$ or 24.6dB. The minimum input is approximately $1.74mV_{P-P}$ or -42dB. Knowing that the 0dB point of the compandor is at $77.5mV_{RMS}$, one can easily convert from volts to dB. Formula 5 shows the conversion from V_{RMS} to dB.

$$X(dB) = 20 \log \left(\frac{V_{RMS}}{77.5(mV_{RMS})} \right) \quad (5)$$

where
X = value in dB
V = voltage in RMS.

Usually it is easier to work in voltages, but in this case it is better to work in dB. If one knows the input signal in dB, the designer can predict the output of the compressor (also in dB) to be half or two times the input. For instance, if the input were 10dB, we could expect the output to be 5dB. On the other hand, if the input was -20dB, we could expect the output to be -10dB.

Capacitor C11 on Pin 22 controls both the attack and release time of the compressor. The attack time may be calculated by Formula 6.

$$\text{Attack time} = R \cdot C \quad (6)$$

where R=10kΩ

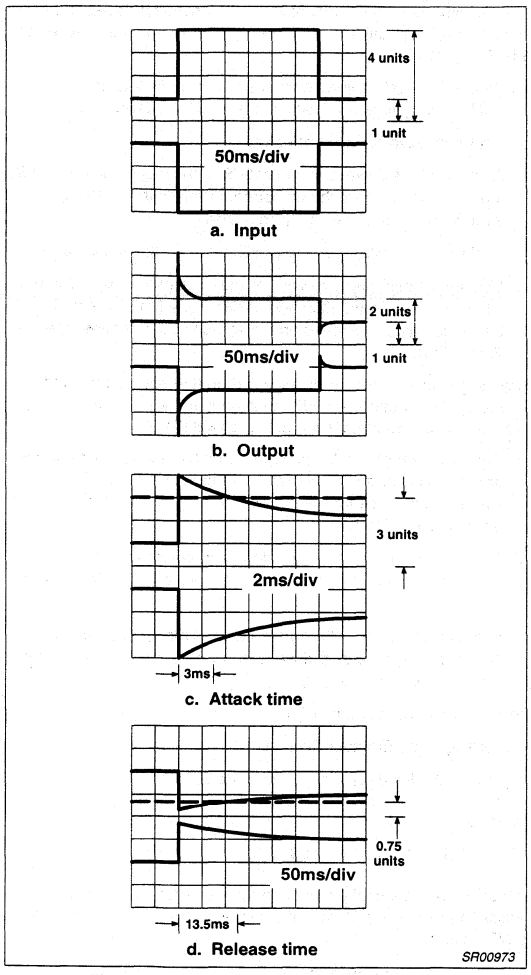


Figure 16. Compressor Dynamic Response

NOTE: The release time is roughly 4 times slower than the attack time by design.

Release time = 4 · Attack time

Capacitor C10 on Pin 21 is used for AC bypassing. Capacitor C9 on Pins 19 and 20 is also for AC bypassing.

- expandor

The expandor input at Pin 17 requires an external DC blocking capacitor (C8). The input impedance is around 2.5kΩ. Referring to Figure 15, the input range of the expandor is from 19.53mV$_{P-P}$ (-21dB) to 903mV$_{P-P}$ (12.3dB). The output range is from 1.74mV$_{P-P}$ (-42dB) to 3.72V$_{P-P}$ (24.6dB).

Capacitor C7 is used to set the attack and release time of the expandor. Formula 6 can also be used to determine those values.

- how to measure attack and recovery time

In this section we will briefly describe the bench procedure for measuring attack and recovery times. Additional information can be found in AN174 in the "Attack and Decay Time" section.

Let's assume that C_{RECT} =2µF and $R_{INTERNAL}$=10k. Since T=R · C, then T=20ms. If we wanted a different "RC" time constant we would change the C_{RECT} value ($R_{INTERNAL}$ is a fixed value).

Using these component values let's measure the attack and recovery times to see if the CCITT and EIA specifications are met.

measurement at compressor:

EIA Specifications

Attack time is the time required for the transmitter deviation to settle to a value equal to "1.5" times the final steady state value, for a 12dB step up.

Release time is the time required for the transmitter deviation to settle to a value equal to "0.75" times the final steady state value, for a 12dB step down.

The compressor must have a nominal attack time of 3ms and a nominal recovery time of 13.5ms as defined by CCITT.

Bench Procedure for Compressor Test

1. Apply a 1kHz sinewave signal at 0dB to the input of the compressor (0dB is defined where the compandor passes the input signal through to the output — unity gain level for the APROC is 77.5mV$_{RMS}$.
2. Modulate the 1kHz input signal with a 1Hz-2Hz square wave.
3. Connect an oscilloscope probe to the input of the compressor and adjust both the modulation and oscilloscope (uncalibrate it) so that a 1:4 ratio is achieved on the screen of the oscilloscope (see Figure 16a).

Adjusting for a 1:4 ratio produces a 0dB to 12dB step at the input. The unit "1" represents the 0dB input level and the unit "4" represents the 12dB input level (20log (4/1) =12dB).

4. Connect another oscilloscope probe to the output of the compressor and observe the waveform (see Figure 16b). The "final steady-state" value for the attack time is "2" units while the release time is "1" unit. These output values are expected because, for a compressor, the ratio is 2:1 unless the input is at 0dB, in which case, the ratio is 1:1.
5. Now to measure the attack and release time, capture the beginning and end of the output waveform where the changes occur (see Figures 16c and 16d).

To measure the attack time (T_A):

-According to the EIA specifications:

T_A = 1.5 · Final Steady – State Value

-therefore

T_A = 1.5 · 2 units = 3 units

-Measure the time it takes for the output to drop to the 3rd unit. According to Figure 16c, our attack time is 3ms. This indeed meets CCITT specs..

To measure the release time (T_R):

-According to the EIA specifications:

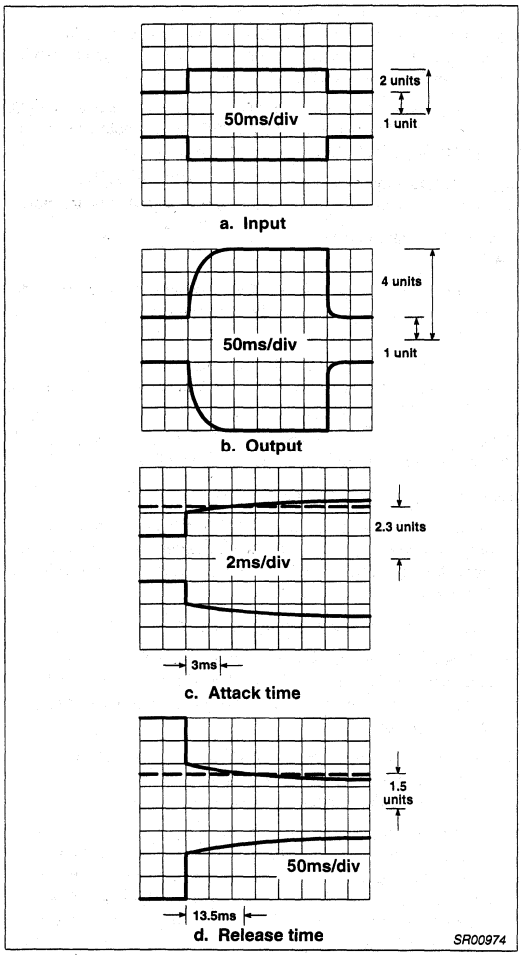


Figure 17. Expandor Dynamic Response

T_R = 0.75 · Final Steady – State Value

-therefore

T_A = 0.75 · 1 unit = 0.75 units

-Measure the amount of time it takes for the output to rise up to 0.75 units. According to Figure 16d, our release time is 13ms. Again the CCITT spec. is met.

measurement at expandor:
EIA Specifications

Attack time is the time required for the transmitter deviation to settle to a value equal to "0.57" times the final steady state value, for a 6dB step up.

Release time is the time required for the transmitter deviation to settle to a value equal to "1.5" times the final steady state value, for a 6dB step down.

The expandor must have a nominal attack time of 3ms and a nominal recovery time of 13.5ms as defined by CCITT.

Bench Procedure for Expandor Test

1. Apply a 1kHz sinewave signal at 0dB to the input of the expandor (0dB is defined where the compandor passes the input signal through to the output — unity gain level).
2. Modulate the 1kHz input signal with a 1Hz-2Hz square wave.
3. Connect an oscilloscope probe to the input of the expandor and adjust both the modulation and oscilloscope (uncalibrate it) so that a 1:2 ratio is achieved on the screen of the oscilloscope (see Figure 17a).

Adjusting for a 1:2 ratio produces a 0dB to 6dB step at the input. The unit "1" represents the 0dB input level and the unit "2" represents the 6dB input level (20log(2/1)=6dB).

4. Connect another oscilloscope probe to the output of the expandor and observe the waveform (see Figure 17b). The "final steady-state" value for the attack time is "4" units while the release time is "1" unit.
5. These output values are expected because for an expandor the ratio is 1:2 unless the input is at 0dB, in which case, the ratio is 1:1.
6. Now to measure the attack and release time, capture the beginning and end of the output waveform where the changes occur (see Figures 17c and 17d).

To measure the attack time (T_A):

-According to the EIA specifications:

T_A = 0.57 · Final Steady – State Value

-therefore

T_A = 0.57 · 4 units = 2.28 units

-Measure the time it takes for the output to reach 2.28 units. According to Figure 17c, our attack time is 3ms. This indeed meets CCITT specs..

To measure the release time (T_R):

-According to the EIA specs.:

T_R = 1.5 · Final Steady – State Value

-therefore

T_A = 1.5 · 1 unit = 1.5 units

-Measure the amount of time it takes for the output to drop to 1.5 units. According to Figure 17d, our release time is 13ms. Again the CCITT specification is met.

These results show that the release time is about 4 times slower than the attack time. All Signetics compandors are internally set up this way so that once the attack time is set by C_{RECT}, the release time is automatically set.

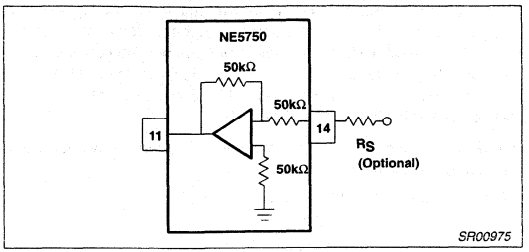


Figure 18. Speaker Amplifier for the NE5750

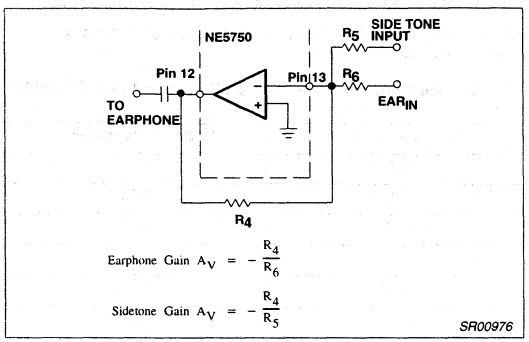


Figure 19. Setting Gain for Earphone Amplifier

Special Note: In AN174, Figures 10 and 11 show the X-axis as being in fractions of the time constant. The way to clarify this is by multiplying 20ms to these numbers to convert them to the measured attack and recovery time. The 20ms comes from the "RC" time constant which can be varied by varying the C_{RECT} value. But again, once these numbers are converted, one can see that these figures show similar results as ours in the lab.

Amplifier Section:

-speaker amplifier

The speaker amplifier is a unity gain amplifier with a high input impedance. Located on Pin 11, the output of the amplifier, are two capacitors C5 and C16. Capacitor C5 is for DC blocking, while C16 is for high pass filtering.

Since the amplifier's input is not directly accessible to the designer (see Figure 18), it is impossible to exceed a gain of one. However, if external attenuation is desired, use formula 7 to determine the series resistor that would connect to Pin 14.

$$A_V = \frac{-R_F}{R_{IN}} \qquad (7)$$

$$= \frac{-50k}{(50k + R_S)}$$

In most cases, the attenuation takes place in the NE5751 before the signal gets to the amplifier. Therefore, adding external attenuation is rare.

-earphone amplifier:

Unlike the speaker amplifier, the gain of the earphone amplifier can be set by external resistors. In this case, the required output and input are directly accessible. Figure 19 is a diagram of the earphone amplifier with the required equations. Sidetone gain can also be implemented with an external resistor.

How To Power Down

"Power down" or "power up" can be implemented by Pin 10 of the NE5750. When Pin 10 is connected to V_{CC}, the chip is in the "power up" state. In this mode, the chip is fully functional. However, when Pin 10 is connected to ground, the chip is in the "power down" state where the current consumption drops dramatically (CMOS or TTL levels will suffice). In this mode, the chip is not expected to be functional, but all of the capacitors remain charged so that "power up" can occur quickly. Having this capability allows the system to conserve battery power.

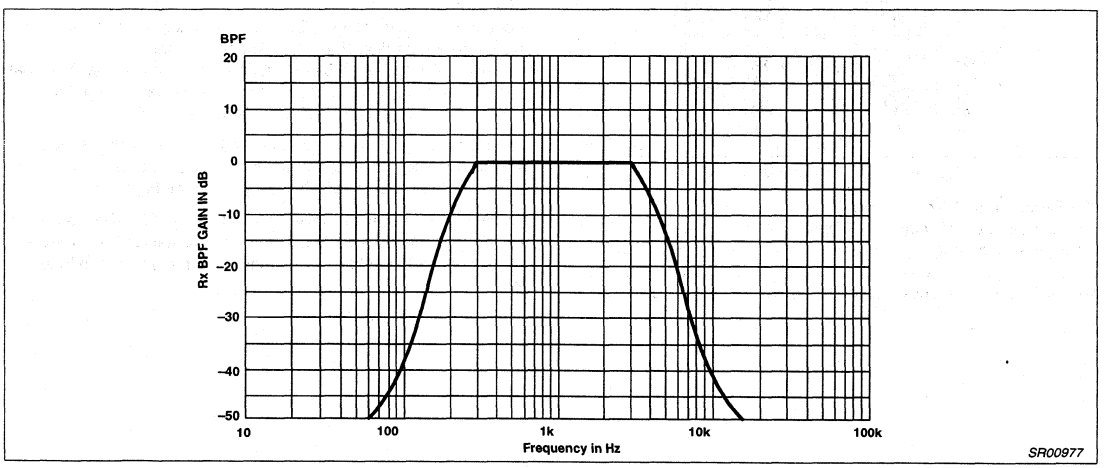


Figure 20. NE5751 Tx Bandpass Filter

III. NE5751

A CLOSER LOOK AT THE NE5751:

Figure 24 shows a block diagram of the NE5751. Key functions for this chip include a TX bandpass filter, TX pre-emphasis filter, TX low pass filter, summing amplifier, RX bandpass filter, RX de-emphasis, programmable DTMF generator, programmable attenuator, and an I^2C bus interface.

-TX path

The input and output of the TX bandpass filter are located on Pins 3 and 4, respectively. The 4th-order Chebyshev bandpass filter is designed to pass 300 to 3000Hz (voice band). (see Figure 20).

The input to the pre-emphasis circuit is accessible through Pin 5. This filter shapes the spectrum with a +6dB per octave slope in the pass band (see Figure 21). The output is then connected internally to a low pass filter and limiter circuit (see Figure 22). The functions of the last two filters guarantee that the 12kHz maximum frequency deviation for cellular radio is not violated.

The output of the limiter filter (Pin 23) and the output of the programmable DTMF generator (Pin 22) can be connected to the input of the summing amplifier. The gain of this amplifier can be controlled with external resistors. In Figure 24, the resistors are all 51kΩ which creates a unity gain configuration. The output of the amp is then connected to the transmitter.

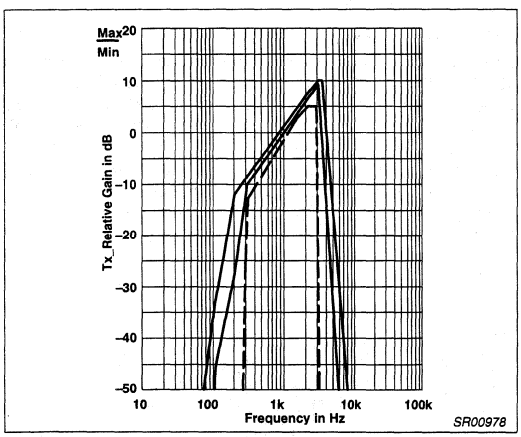


Figure 21. Pre-emphasis Curve

The Limiter and All-pass Circuit:

An important aspect of the AMPS specification is concerned with the 12kHz maximum frequency deviation. The output of the APROC should be less than 12kHz regardless of the input signal. Figure 23 shows the equipment used for the test measurements and how the signal was processed. A 1kHz signal was applied to the input of the demo-board until a 5% distorted signal was measured at the limiter output. This waveform's peak-to-peak voltage was recorded as a reference, then, at various chosen frequencies, the input of the demo-board was overdriven so we could record the distorted peak-to-peak waveform. (See Figure 26)

Formula 8 was used to calculate maximum frequency deviation from the waveforms shown in Figure 26.

$$\text{Max Freq Dev with All-Pass Ckt} = \frac{BW_F}{BW_R} \cdot 8\text{kHz} \quad (8)$$

where

BW_F = the bottom waveform's peak-to-peak voltage from one of the observed Figures.

BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure.

Table 9. Maximum Frequency Deviation Results for the 12kHz Test

Frequency (Hz)	With All-Pass (kHz)
300	5.91
500	9.04
800	10.09
1000	10.09
1200	10.09
2000	11.13
3000	10.78

Table 9 reveals the calculated results for maximum frequency deviation over the voice band. The test results show that the NE5750 and NE5751 will meet the 12kHz AMPS specification. If a customer needs further assurance that the 12kHz specification will be satisfied, an Automatic Level Control (ALC) circuit can be placed after the summing amplifier output of the NE5751. Keep in mind, though, that this ALC will only provide attenuation.

- RX path

For the receive side of the NE5751, the signal goes to the input of the RX bandpass filter (Pin 13) which has the same characteristics as the TX bandpass filter. The only difference is that this filter also has a stop-band notch filter at 6kHz to reject the Supervisory Audio Tone (SAT) signals as seen in Figure 27.

The output is then internally connected to the de-emphasis filter. This filter provides a -6dB/octave slope over the passband to compensate for the pre-emphasis function (see Figure 28).

The attenuator can be digitally programmed by I^2C. The input signal level can be attenuated 16 steps in 2dB increments. This gives a range from 0dB to -30dB. The attenuator error is shown in Figure 29.

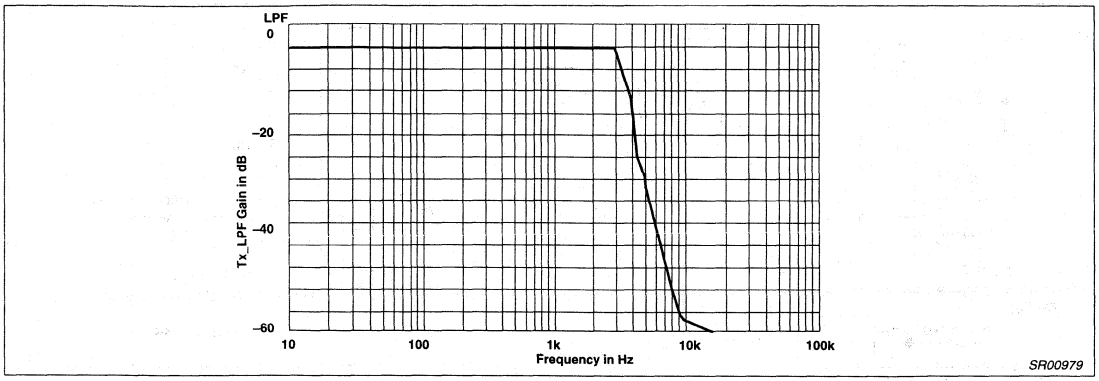


Figure 22. NE5751 Tx Low Pass Filter

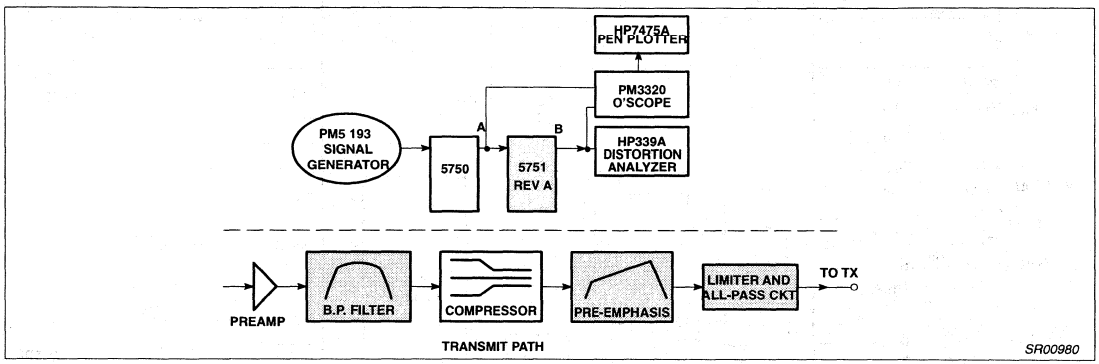


Figure 23. Test Set-up and Tx Path of Signal

I²C Bus Interface:

The NE5751 is controlled by a serial control bus comprised of a clock input, serial bus address, serial clock line, and serial data line.

A designer who is unfamiliar with I²C can refer to the following documents for assistance: 1) I²C Bus Specification and 2) Signetics AN168. Both of these documents can be found in the 1989 Signetics Linear Data Manual or the 1991 RF Communications Handbook.

The clock input requires an input frequency of 1.2MHz. This frequency is vital for the operation of the part because it effects the DTMF generator and the 3dB point of all the switch capacitor filters.

The output of the DTMF generator can be determined by Formula 8.

$$\text{Low Freq} = \frac{\frac{\text{Clock Input Freq}}{12}}{\text{LD}} \quad (8a)$$

where LD is the value of the register This translates to: DTMF LO REG = 100000/ LO REG (Hz)

$$\text{High Freq} = \frac{\frac{\text{Clock Input Freq}}{6}}{\text{HD}} \quad (8b)$$

where HD is the value of the register

This translates to: DTMF HI REG = 200000/ HI REG (Hz)

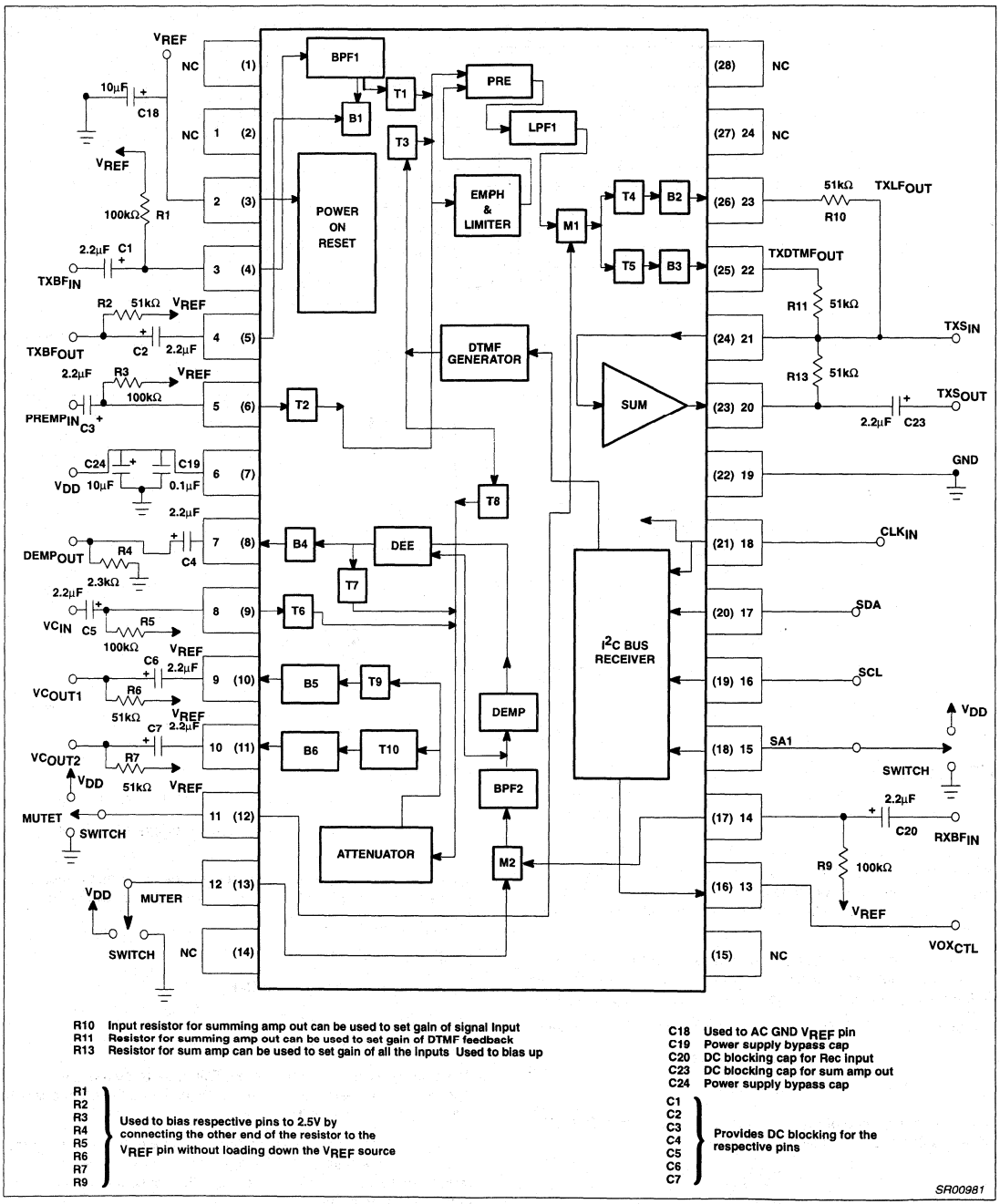
Table 10 can be used to help the designer program the DTMF generator.

There are a few key points that should not be overlooked when programming the NE5751. The control registers consist of the

1. Register map
2. Signal path register
3. Volume control and test register
4. High tone DTMF register
5. Low tone DTMF register

To generate a single tone from the DTMF generator, use the appropriate registers (high or low DTMF) and load the other one with a '0', '1', or '2' to silence it.

The order of these registers is important. If the programmer wanted to turn down the volume, he/she would have to re-program the register map, signal path, and then give the new data to the volume control and test register.



R10 Input resistor for summing amp out can be used to set gain of signal input
R11 Resistor for summing amp out can be used to set gain of DTMF feedback
R13 Resistor for sum amp can be used to set gain of all the inputs Used to bias up

R1, R2, R3, R4, R5, R6, R7, R9 — Used to bias respective pins to 2.5V by connecting the other end of the resistor to the V_{REF} pin without loading down the V_{REF} source

C18 Used to AC GND V_{REF} pin
C19 Power supply bypass cap
C20 DC blocking cap for Rec input
C23 DC blocking cap for sum amp out
C24 Power supply bypass cap

C1, C2, C3, C4, C5, C6, C7 — Provides DC blocking for the respective pins

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Figure 24. NE/SA5751 Test and Application Circuit

Table 10. Maximum Frequency Deviation Results for the 12kHz Test

Number Dialed	High Freq.	Low Freq.	DTMF HI	DTMF LO
1	1209	697	A5	8F
2	1336	697	96	8F
3	1477	697	87	8F
4	1209	770	A5	82
5	1336	770	96	82
6	1477	770	87	82
7	1209	852	A5	75
8	1336	852	96	75
9	1447	852	87	75
0	1336	941	96	6A
*	1209	941	A5	6A
#	1477	941	87	6A

IV. APROC DEMO-BOARD

About the APROC demo-board:

The NE5750/51 demo-board layout can be seen in Figures 30, 31, and 32. It incorporates the use of DIP packages. However, an SO adapter could be made to test the SO APROC chips.

A separate board is used to interface the APROC demo-board with the computer's parallel port. This converter utilizes the 74LS05 as a buffer scheme.

An I^2C program for the APROC is provided so that a designer can easily program and evaluate the chip set. This eliminates the need to write an evaluation program. However, it does not eliminate the need for a final system program.

The evaluation program has a graphic display that shows the transmit and receive path of the APROC on the terminal, as seen in Figure 33. By selecting a function, one can toggle the space bar on the key board to turn on or off any key features. The designer could also type in the codes for any registers to control the functions.

Figure 25 shows how the interface board and the demo-board can be used in conjunction with a computer. Once everything is connected properly, one can make his own evaluations on the chip set.

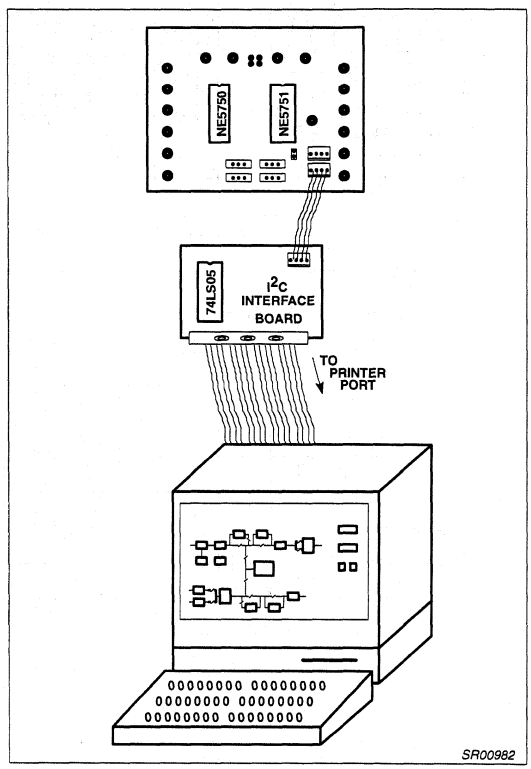


Figure 25. Interfacing the APROC Demo-board with the I^2C Evaluation Program

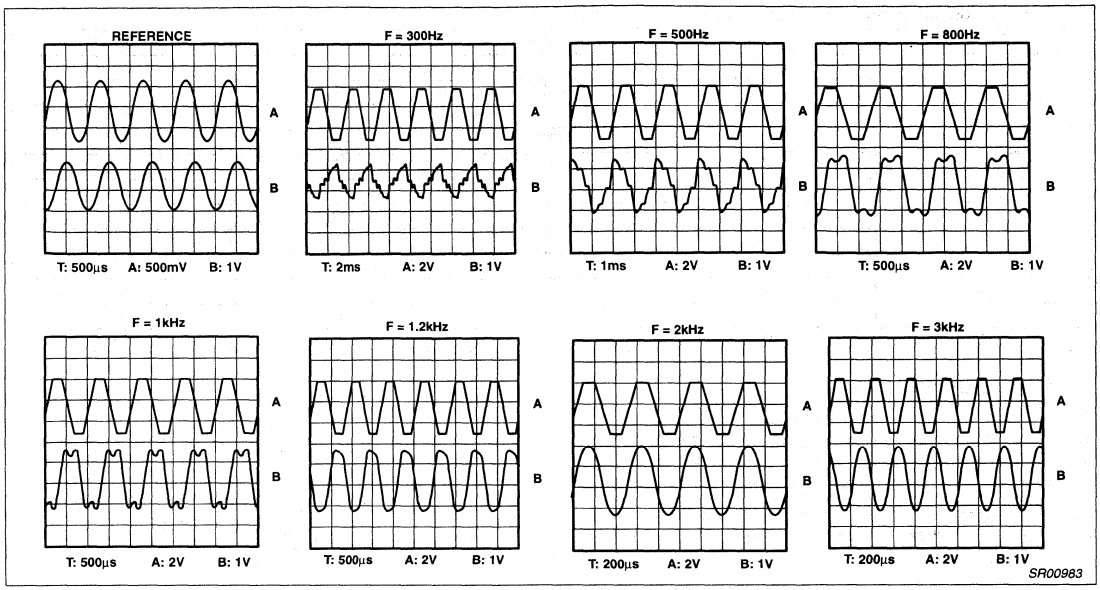


Figure 26. Results From the 12kHz Maximum Frequency Deviation Test

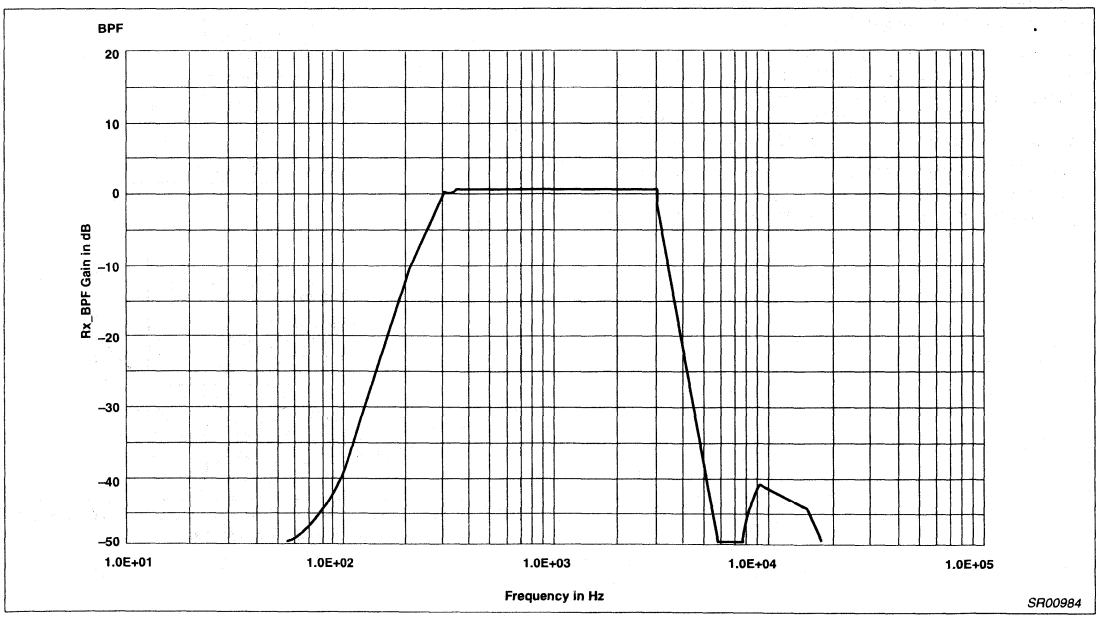


Figure 27. NE5751 Rx Bandpass Filter

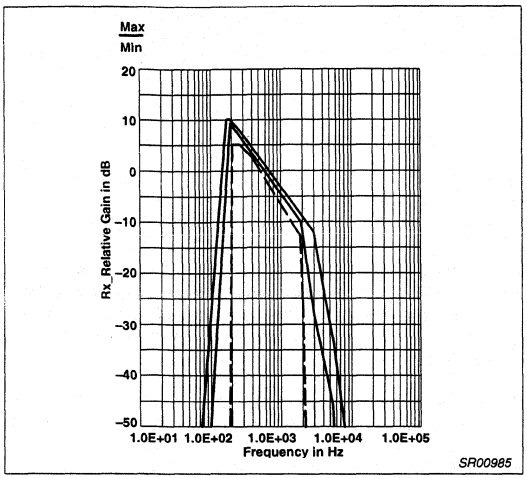


Figure 28. NE5751 Rx De-emphasis

How to Power Down on the NE5750/51 Demo-Board:

In general, power down mode is a condition where a system has just enough power to "stay alive" and, therefore, is not expected to be fully operational. When called upon, the system can quickly get out of this mode and into the power up mode and be ready to perform its functions. This fast reaction time is possible because all of the capacitors have maintained their charges. This is because power was not cut-off completely. The power down function reduces overall current consumption when the system is not fully operational, and is especially helpful when the system is operating from a battery powered source.

There are three power down conditions when we refer to to the NE5750/51 demo-board. They are listed and described as follows:

1. NE5750 Power Down

Purpose:

- to reduce current consumption

- to maintain all DC voltages on the device pin to keep the capacitors charged

How To:

- use hardware switch on demo-board which forces Pin 10 to ground

- or use a CMOS logic output into Pin 10

Benefits:

- reduces current consumption while maintaining readiness

- current drops from 8.4mA to 1.8mA (typically)

Mode of Operation:

- Everything is semi-functional, although performance is not, and will not be, guaranteed

2. NE5751 Power Down

Purpose:

- to reduce current consumption

- to maintain all DC voltages on the device Pin to keep the capacitors charged up

- to open all voice paths so that no signals will flow

How To:

- program the I^2C bus under the condition that all registers are set to zero

Benefits:

- all the registers are always at zero when powering up from the power down mode

- reduces current consumption while maintaining readiness

- current drops from 2.7mA to 1.1mA (typically)

Mode of Operation:

- Everything is semi-functional, although performance is not, and will not be, guaranteed

3. Chip-Set Power Down

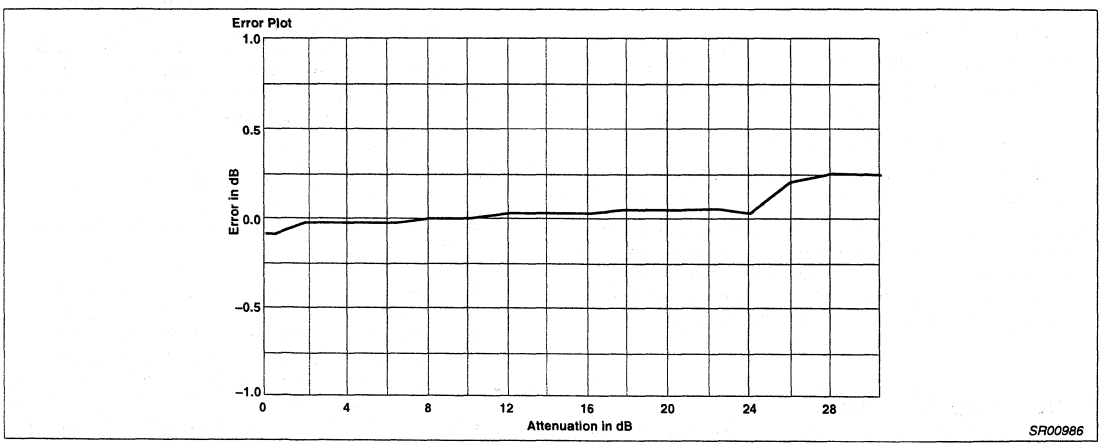


Figure 29. NE5751 Attenuation Error

Definition:

-the NE5750 and NE5751 demo-board is in the power down mode when:

1. The transmitter and receiver are muted on the NE5751
2. The NE5751 is powered down (all registers are set to zero), and
3. The NE5750 is powered down

How to Power Down the Chip-Set Properly (1st Choice):
Please follow this recommended sequence;

1. Mute both the transmitter and receiver on the NE5751.
2. Program the following registers as follows:

Signal Path Register: 00000000

Volume Control Register: 00000000

High DTMF Register: 00

Low DTMF Register: 00

3. Power Down the NE5750.

How to Simulate the Power Down on the Chip-Set (2nd choice)*
Please follow this recommended sequence;

1. Program the following registers as follows:

Signal Path Register: 00010000

Volume Control Register: 01100000

High DTMF Register: 00

Low DTMF Register: 00

2. Power Down the NE5750

*NOTE: this method is only used when the NE5751 mute switches are not accessible, by design.

Comments

1. Muting both the transmitter and receiver on the NE5751 can be done by the two "hardware" switches on the demo-board (forces Pins 11 and 12 to V_{CC}).
2. Powering down the NE5751 can be done by programming the correct assigned register to zero (For more details, consult the NE5751 data sheet).
3. Powering down the NE5750 can be done by the "hardware" switch on the demo-board (forces Pin 10 to ground).
4. When coming out of the power down mode to the power up mode, reverse the procedure given above.
5. If functions are activated while in the power down mode before power up occurs, the "chip-set power down" is no longer valid.
6. We recommend that a 2.2µF capacitor be placed between the NE5751 de-emphasis output to the NE5750 expandor input. The purpose of this capacitor is to block any DC offset that might occur between the two chips while in the power down mode. If this capacitor is not used, an abnormal reaction might occur where white noise is generated.

V. NE5750 DEMO-BOARD

Figure 34 shows the layout for the NE5750 demo-board. This board can be used to evaluate the NE5750, alone, and allows the designer to do extensive testing without having to worry about other external factors. Again, this board makes use of dip packages only. However, a SO adapter can be made to implement the SO version of the NE5750.

VI. QUESTION AND ANSWER SECTION

NE5750 and NE5751 (APROC):

Q: Is it OK to connect the V_{REF} pins together for the NE5750 and NE5751? My circuit seems to be working properly.

A: No, this is not a good idea. Although both V_{REF}s are at 2.5V ($V_{REF} = V_{CC}/2$), there is no guarantee that they will be exactly equal over temperature. One of the V_{REF}s might influence the function of the other chip which, in turn, might have a detrimental effect on the performance of the chips.

Q: Will the APROC chip set work for TACS, NMT or NAMPS specifications as it does for AMPS specification?

A: The APROC was designed to meet AMPS and TACS specifications, however, as it stands now, the chip set will also meet the NAMPs requirements. The chip set will not work for NMT specifications.

Q: In the power down mode, is it OK to program the DTMF registers before powering up?

A: No. This will break the rules of powering down. All the registers are set to zero in this mode. Please review the section on powering down the chip set properly.

NE5750:

Q: Even though I have all the required external components in place on Pins 1,2,3,4,5,6 and 7, my VOX circuit does not work. What is wrong?

A: The VOX circuit is not a trivial connection. Even though all the components are connected, be sure that the output of the NE5750 noise canceller is AC coupled to the input of the compressor to complete the VOX loop. This holds true if the NE5750 is used alone. However, if the NE5751 is used make sure that the signal is fed from the band-pass filter to the input of the NE5750 compressor input. For further advice, please read example 1 in the "setting the threshold" section of this application note.

Q: Do I have to use I^2C if I use the NE5750 alone?

A: No, the NE5750 can be used by itself and does not require the use of I^2C.

Q: Can I speed up the release time of the compressor?

A: Not directly. The release time is dependent on the attack time setting. Once the attack time is set by C11 on Pin 22 of the NE5750, the release time is set internally to be four times slower. So to increase the release time requires that the attack time be increased. One should be careful because setting the attack time too fast could cause more distortion on the output.

Q: The NE5750 compressor input impedance is around 50kΩ. Why is this impedance higher than that of others in your family of compandors?

A: The NE5750 was designed to be compatible with the NE5751. The NE5750 compressor input was modified to accept CMOS driven outputs like the NE5751. This internal modification eliminates the need for an external buffer.

NE5751:

Q: Can I change the filter characteristics?

A: Yes, by changing the master clock input frequency the 3dB points will be effected. For example, if F=1.2MHz, then BPF1=3kHz. Now, if F=600kHz, BPF1=1.5kHz; and if F=2.4MHz, BPF1=6kHz. This type of application is not recommended because the part was not designed to be used this way and, therefore, performance will not be guaranteed. Additionally, the DTMF generator will be off in frequency from the calculated values because of the assumption of a 1.2MHz clock, and the I^2C interface will not be functional.

Q: Besides I^2C, can I communicate to the NE5751 with another type of operating scheme?

A: Yes, by bit banging. Instead of using the I^2C hardware one can supply the clock and data defined in the I^2C protocol software. But this takes up a lot of memory, therefore, it is preferable to implement the I^2C hardware.

Q: The limiter seems to work when I overdrive the input with a strong signal. However, when I try to pass DTMF tones, the limiter's level varies when switches T3/T5 and T4 are set to different settings Why is this? Isn't the output supposed to stay constant regardless of the input being overdriven or passing DTMF tones?

A: Yes, the limiter should hold the output constant when an overdriven signal is applied, but only when the switches are used properly. When passing DTMF tones, T1, T2, and T4 should be left open, while T3/T5 are closed. The voice path should be disconnected when DTMF tones are being passed. Hence, T3/T5 should be left open when DTMF is not used.

Q: When I program a DTMF tone, it only stays on for 96ms. How can I make it stay on longer?

A: The way to make it stay on longer than 96ms is to re-load the DTMF registers (re-program the DTMF registers before 96ms expires).

REFERENCES:

"Audio Processing for Cellular Radio or High Performance Transceivers", proceedings of R.F. Expo 1989, A. Fotowat, S. Navid, L. Engh, pp. 195-203.

"Designing Cellular Radios with the Philips Components-Signetics Cellular Chip Set", Cellular Radio Chip Set Design Manual, Feb. 25, 1990.

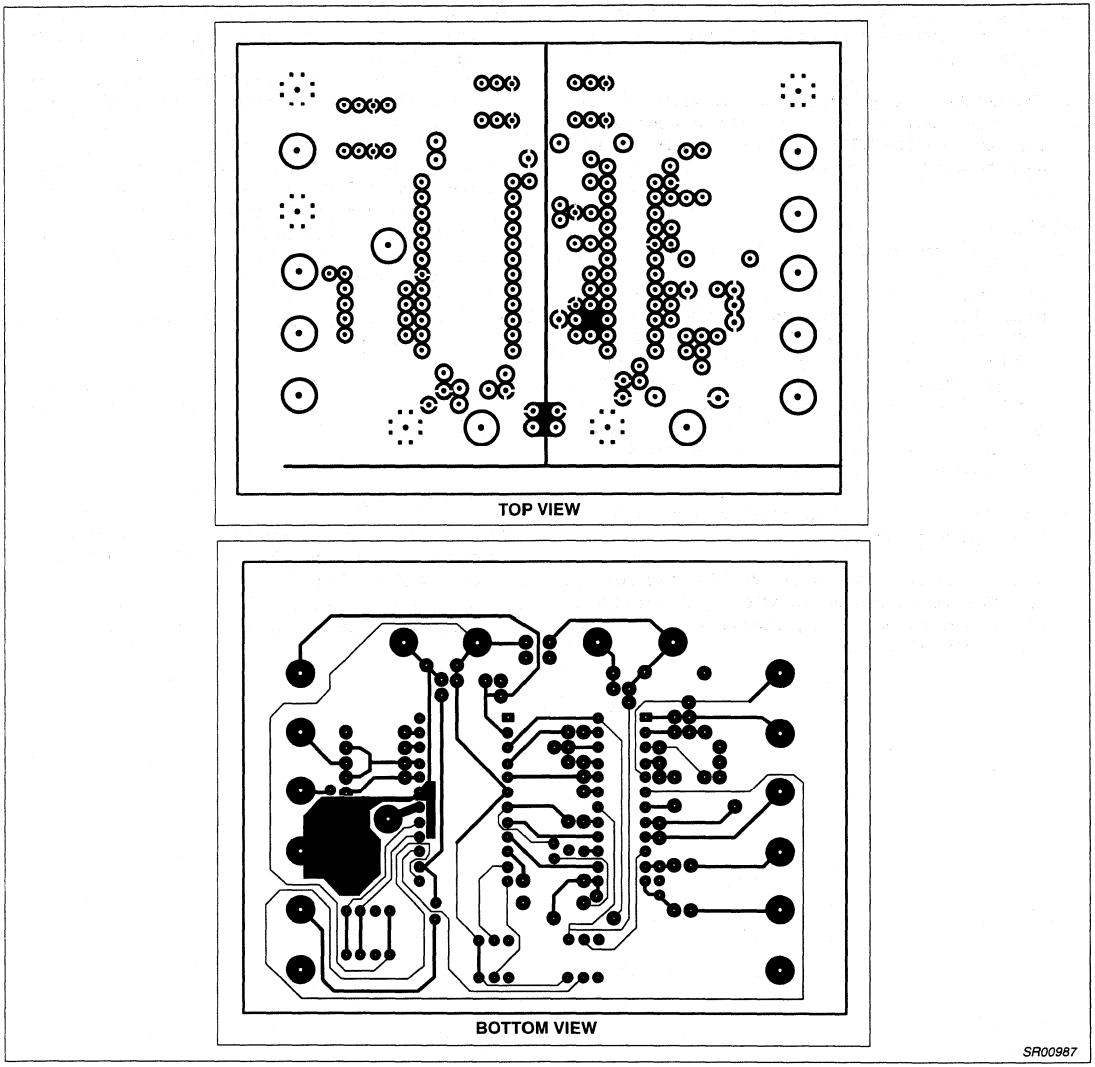


Figure 30. Layout of the APROC Demo-board

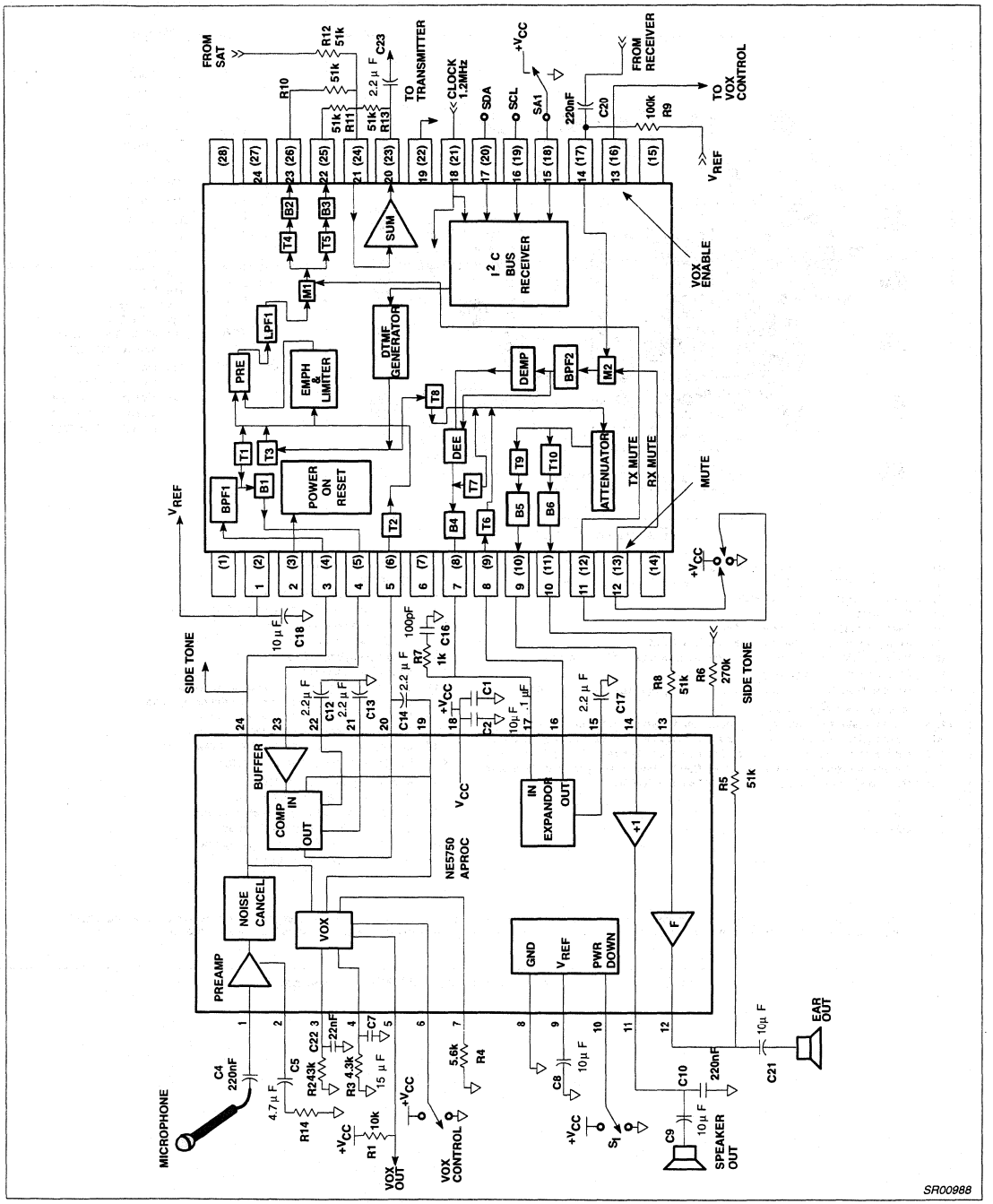
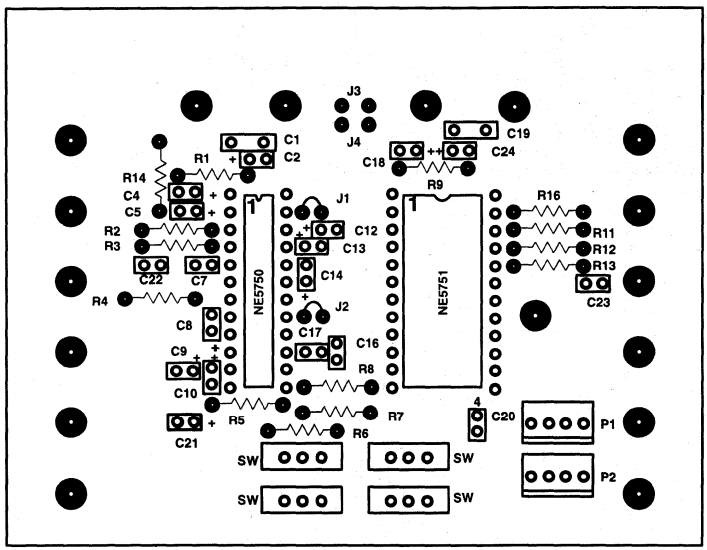


Figure 31. NE5750, NE5751 Cellular Radio Application Circuit



Component Values

C1	0.1µF	R1	10kΩ
C2	10µF	R2	43kΩ
C4	0.22µF	R3	4.3kΩ
C5	4.7µF	R4	5.6kΩ
C7	15µF	R5	51kΩ
C8	10µF	R6	270kΩ
C9	10µF	R7	1kΩ
C10	0.22µF	R8	51kΩ
C12	2.2µF	R9	100kΩ
C13	2.2µF	R10	51kΩ
C14	2.2µF	R11	51kΩ
C16	100pF	R12	51kΩ
C17	2.2µF	R13	51kΩ
C18	10µF	R14	OPTIONAL
C19	.1µF	J1	JUMPER
C20	0.22µF	J2	JUMPER
C21	10µF	IC	NE5750 NARROW 24-PIN SOCKET
C22	.022µF	IC	NE5751 WIDE 24-PIN SOCKET
C23	2.2µF	P1	4 PRONG HEADER
C24	10µF	P2	4 PRONG HEADER
		SW	MINI SLIDE SWITCH

Component Functions

R1 Pull-up resistor for VOX_{OUT} logic levels
R2 Sets gain of VOX, but for internal use only effects voltage on Pin 4
R3 Used to set release time of VOX
R4 Sets threshold level of VOX
R5 Feedback resistor for ear amplifier
R6 Sets gain of ear amplifier for the side tone input
R7 Used in conjunction with C10 to filter out unwanted noise. Optional
R8 Sets gain of ear amplifier
R9 Used to bias up Pin 14 to 2.5V by connecting V_{THRESH} to V_{REF} without loading down V_{REF} source
R10 Input resistor for summing amp out. Can be used to set gain of signal
R11 Input resistor for summing amp out. Can be used to set the gain of the DTMF
R12 Input resistor for summing amp. Can be used to set gain of the side tone input
R13 Feedback resistor for summing amp. Can be used to set gain of all the inputs
R14 Used to set gain of the preamp of NE5750 (OPTIONAL)

J1 JUMPER
J2 JUMPER

C1 Bypass cap for VCC of NE5750
C2 Bypass cap for VCC of NE5750
C4 DC blocking cap for mic input
C5 DC blocking cap for mic gain setting resistor
C7 Used to set attack a release time of VOX
C8 Used to AC ground the V_{REF} pin (5750)
C9 DC blocking cap for speaker out
C10 filter for speaker out
C12 Sets attack and release time of compressor
C13 Used to AC short the DC path for the compressor
C14 Provides AC path to the VOX circuitry
C16 OPTIONAL. Basically to filter out noise
C17 Sets attack and release time for the expandor
C18 Used to AC ground V_{REF} pin (5751)
C19 Bypass cap for V_{CC} of NE5751
C20 DC blocking cap for receiver input
C21 DC blocking cap for ear amplifier output
C22 Sets gain of VOX, internal use only
C23 DC blocking cap for summing amp out
C24 Bypass cap for V_{CC} of NE5751

NOTE: The board is constructed in such a way as to allow a single power supply to power the chip set, or for each chip to be powered by a separate power supply. Using separate power supplies will permit monitoring of current consumption of each part when Jumpers 3 and 4 are removed.

SR00989

Figure 32. Parts and Function List of APROC Demo-board

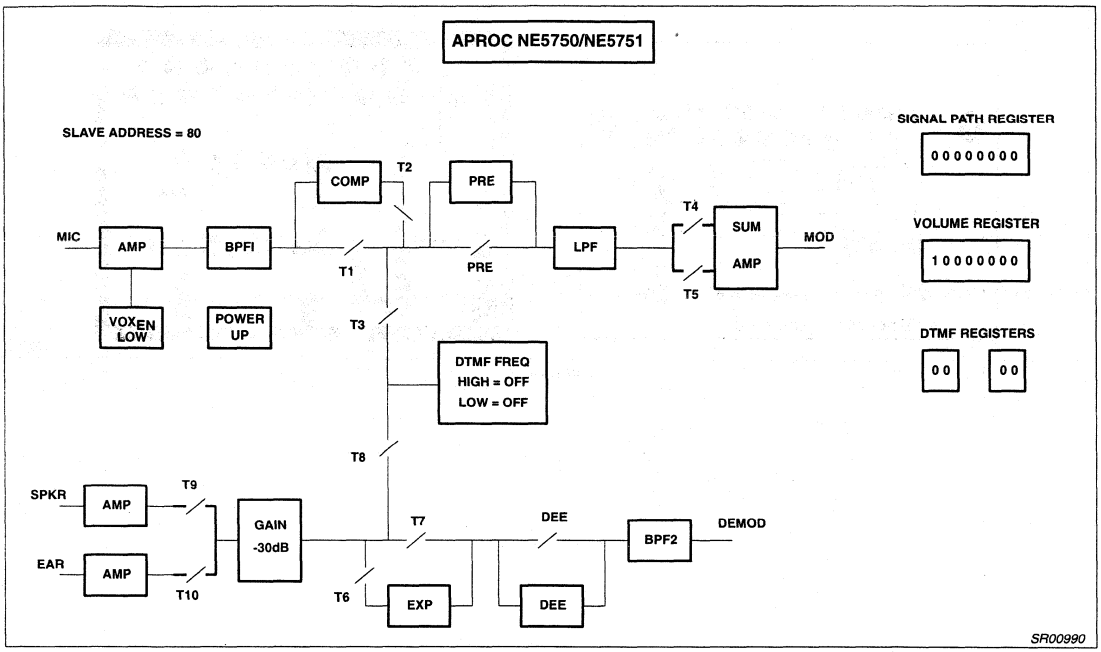


Figure 33. Graphical Display of the I²C Evaluation Program

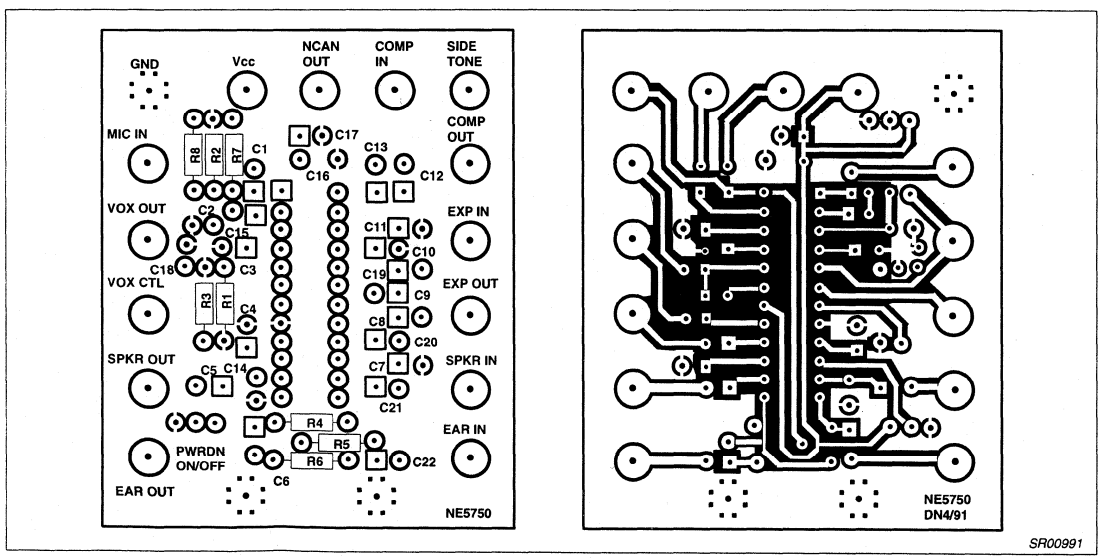


Figure 34. NE5750 Demo-board Layout

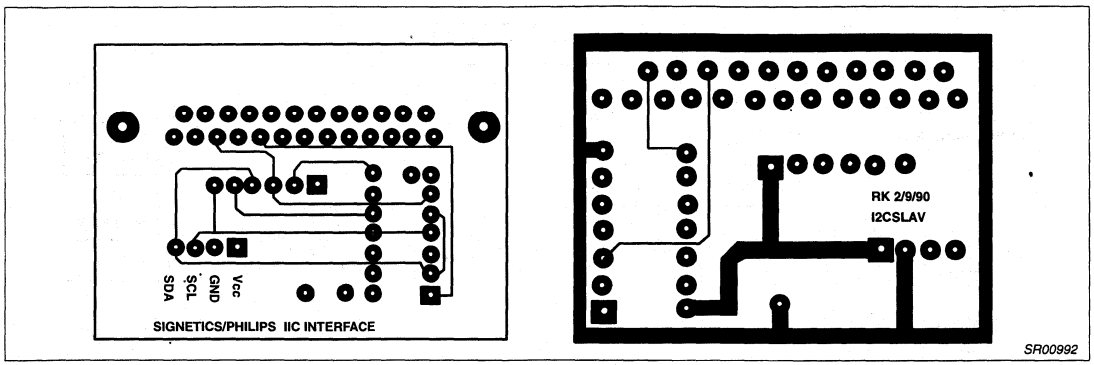

SDA
SCL
GND
Vcc
SIGNETICS/PHILIPS IIC INTERFACE
RK 2/9/90
I2CSLAV
SR00992

Figure 35.

Audio processor – companding, VOX and amplifier section SA5752

DESCRIPTION

The SA5752 is a high performance low power audio signal processing system especially designed to meet the requirements for small size and low voltage operation of hand-held equipment. The SA5752 subsystem includes a low noise microphone preamplifier with adustable gain, a noise cancellation switching amplifier with adjustable threshold, a voice operated transmitter (VOX) switch, VOX control, an audio compressor with buffered input, audio expandor, and an internal bandgap voltage regulator with power down capability. When used with Philips Semiconductors' SA5753, the complete audio processing function of an AMPS or TACS cellular telephone is easily implemented. The system also meets the requirements of the proposed NAMPS or NTACS specifications. The SA5752 can also be used without the SA5753 in a wide variety of radio communications applications.

FEATURES

- Operating voltage range: 2V to 5.5V
- Miniature SSOP and SO packages
- High performance
- Adjustable VOX and noise cancellation threshold
- Adjustable gain preamplifier
- Audio companding
- ESD protected
- Open collector VOX output
- Logic inputs CMOS compatible
- Power down mode
- Few external components
- Meets AMPS/TACS/NAMPS/NTACS requirements

PIN CONFIGURATION

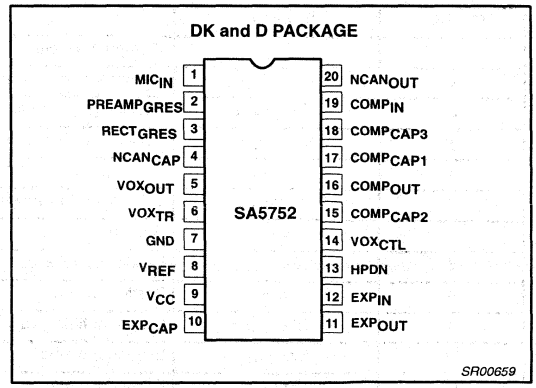


Figure 1. Pin Configuration

BENEFITS

- Very compact applications
- Long battery life in portable equipment
- Complete cellular audio function with the SA5753

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package	-40 to +85°C	SA5752D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA5752DK	SOT266-1

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	MIC_{IN}	Microphone input
2	$PREAMP_{GRES}$	Preamplifier gain resistor
3	$RECT_{GRES}$	Rectifier gain resistor
4	$NCAN_{CAP}$	Noise cancellation timing capacitor
5	VOX_{OUT}	Voice operated transmission output
6	VOX_{TR}	Voice operated transmission threshold resistor
7	GND	Ground
8	V_{REF}	Reference voltage
9	V_{CC}	Positive supply
10	EXP_{CAP}	Expandor timing capacitor
11	EXP_{OUT}	Expandor output
12	EXP_{IN}	Expandor input
13	HPDN	Hardware power-down
14	VOX_{CTL}	Voice operated transmission control
15	$COMP_{CAP2}$	Compressor capacitor 2 DC block
16	$COMP_{OUT}$	Compressor output
17	$COMP_{CAP1}$	Compressor timing capacitor 1
18	$COMP_{CAP3}$	Compressor capacitor 3 DC block
19	$COMP_{IN}$	Compressor input
20	$NCAN_{OUT}$	Noise cancellation output

BLOCK DIAGRAM

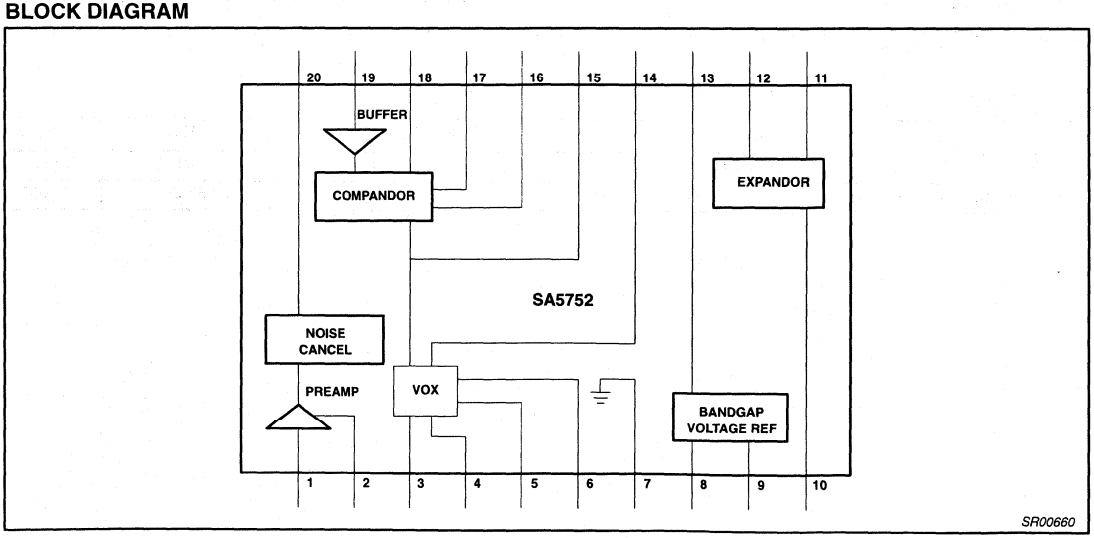


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage range	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature	-40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +3.0V, 0dB = 77.5mV_{RMS}. See test circuit, Figure 6.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		2.7[4]	3.0	5.5	V
I_{CC}	Supply current	No signal Power down mode		3.1 125	4.0	mA µA
Z_L	Load impedance pins $NCAN_{OUT}$, EXP_{OUT}		50			kΩ
	$COMP_{OUT}$[1]		10			kΩ
Z_{IN}	Input impedance $COMP_{IN}$, MIC_{IN}		40	50	60	kΩ
	EXP_{IN}[2]		2.0			kΩ
	Noise cancellation current	Pin 6		25		µA
V_{OS}	DC offset $NCAN_{OUT}$[3]		-50	–3.0	50	mV

NOTES:
1. Compressor is tested in production with 50kΩ load.
2. Not tested in production.
3. Offset values are identical for both gain states of noise reduction circuit.
4. Operational down to V_{CC} = 2V.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +3.0V, 0dB level = 77.5mV_{RMS}. See test circuit, Figure 6.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Preamplifier gain range Preamplifier voltage gain 0dB Preamplifier voltage gain 40dB	 Pin 2 open Pin 2 AC ground	0 -1.0 39.0	 0 40	40 1.0 41.0	dB dB dB
	Preamplifier noise density	Pin 2 AC grounded RS = 50kΩ unweighted 20Hz-20kHz		7		nV/√Hz
		weighted CCIR DIN45405 20-20kHz		8		nV/√Hz
	Switch amplifier gain		9	10	11	dB
Compandor 1kHz, all tests[1]						
$COMP_{OUT}$	Compressor error at -21dB output level	Input level = -42dB	–1.0	–0.16	1.0	dB
$COMP_{OUT}$	Compressor error at -10dB output level	Input level = -20dB	-1.0	–0.11	1.0	dB
$COMP_{OUT}$	Compressor error at 0dB output level	Input level = 0dB	-1.5	+0.1	1.5	dB
$COMP_{OUT}$	Compressor error at +5dB output level	Input level = +10dB	-1.0	+0.04	1.0	dB
$COMP_{OUT}$	Compressor error at +10dB output level	Input level = +20dB	-1.0	+0.02	1.0	dB
EXP_{OUT}	Expandor error at -42dB output level	Input level = -21dB	–1.0	–0.12	1.0	dB
EXP_{OUT}	Expandor error at -21dB output level	Input level = -10.5dB	-1.0	+0.1	1.0	dB
EXP_{OUT}	Expandor error at -10dB output level	Input level = -5dB	-1.0	+0.03	1.0	dB

AC ELECTRICAL CHARACTERISTICS (Contineud)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
EXP_{OUT}	Expandor error at 0dB output level	Input level = 0dB	-1.5	–0.2	1.5	dB
EXP_{OUT}	Expandor error at +10dB output level	Input level = +5dB	-1.0	+0.03	1.0	dB
EXP_{OUT}	Expandor error at +20dB output level[2]	Input level = +10dB	-1.0	–0.1	1.0	dB
EXP_{OUT}	Expandor V_{OS}	No signal	-50.0	+3.0	50.0	mV
EXP_{OUT}	Expandor output DC shift	No signal to 0dB	-100	+2.0	100	mV
	Timing capacitors compandor			2200		nF
THD	Total harmonic distortion					
	Compressor	1kHz, 0dB BW=300-3kHz		0.2	1	%
	Expandor	1kHz, 0dB BW=300-3kHz		0.1	1	%
	$NCAN_{OUT}$	1kHz. Pin 2 open output level = 0dB		0.02	1	%
		1kHz, Pin 2 open output level = +20dB		0.06	1	%
VOX_{OUT}	Sink current				0.5	mA
	Low level High level	Open collector I_L = 0.5mA		 V_{CC}	0.4	V V
VOX_{CTL}	Input current Low		-50	–6.6	0	µA
	High		-10	–0.02	+10	µA
	Input level Low High		0 $0.7V_{CC}$		$0.3V_{CC}$ V_{CC}	V V
H_{PDN}	Input current Low		-10	–4.1	+10	µA
	High		-10	–0.2	+10	µA
	Input level Low High		0 $0.7V_{CC}$		$0.3V_{CC}$ V_{CC}	V V
	Reference filter capacitor			10		µF

NOTE:
1. Measurements are relative to 0dB output.
2. Measurement is indicative of the output dynamic range capability.

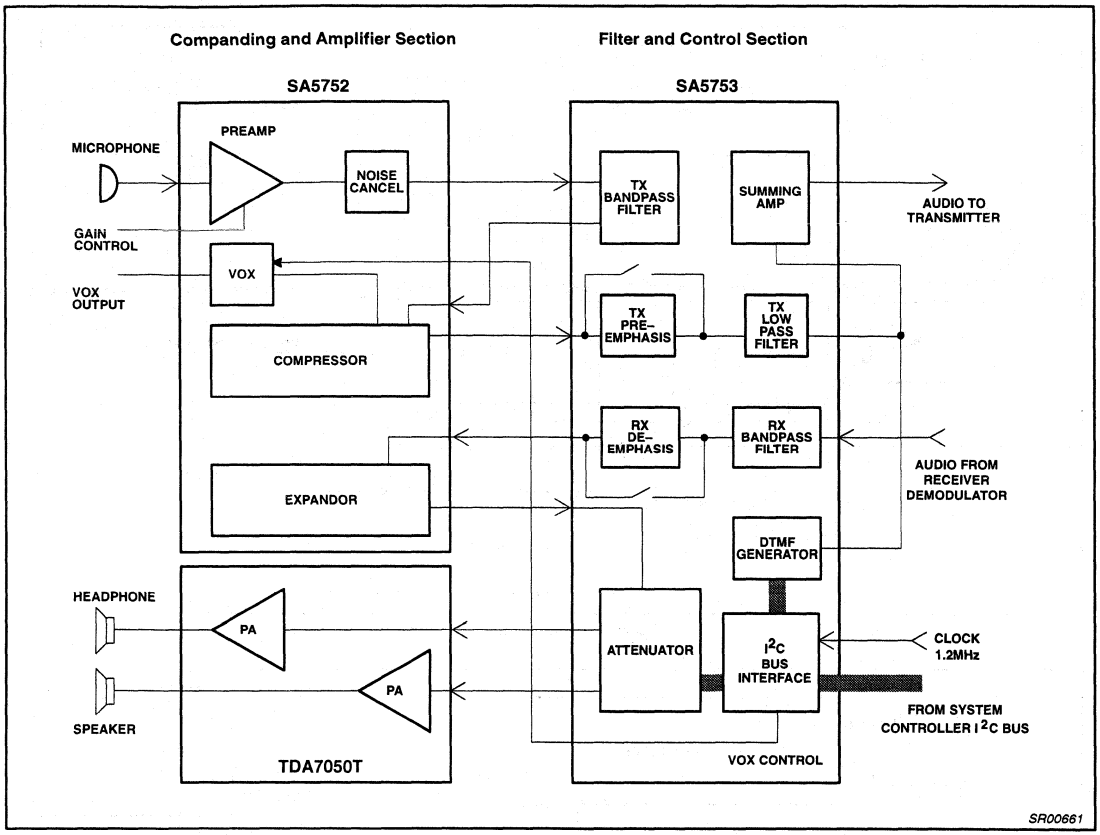


Figure 3. Typical Configuration of Audio Processor (APROC) System Chip Set

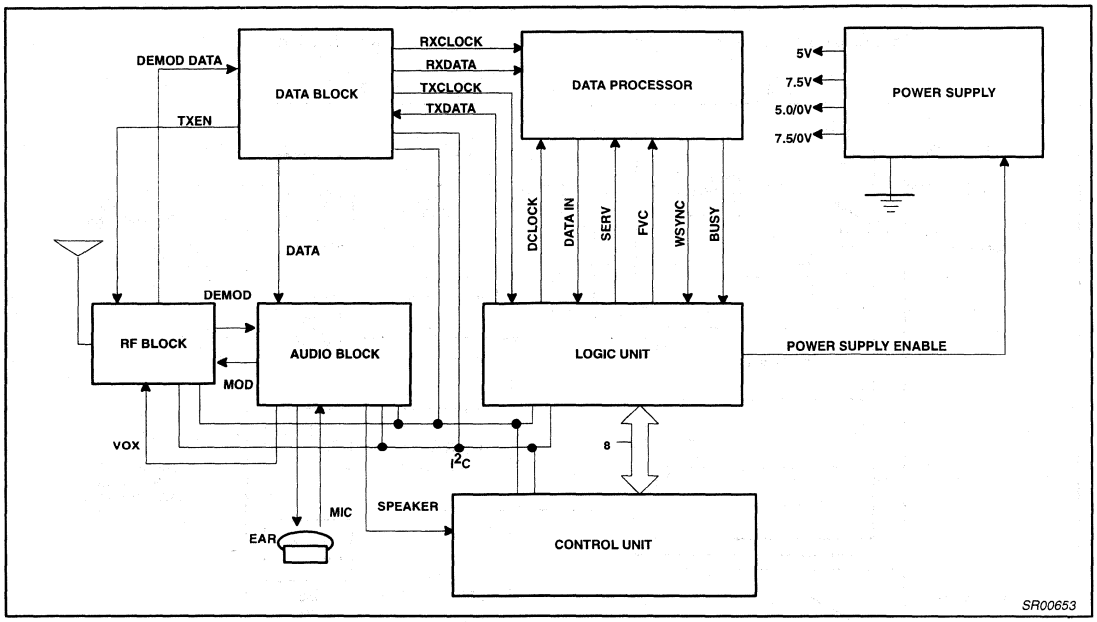


Figure 4. Cellular Radio System

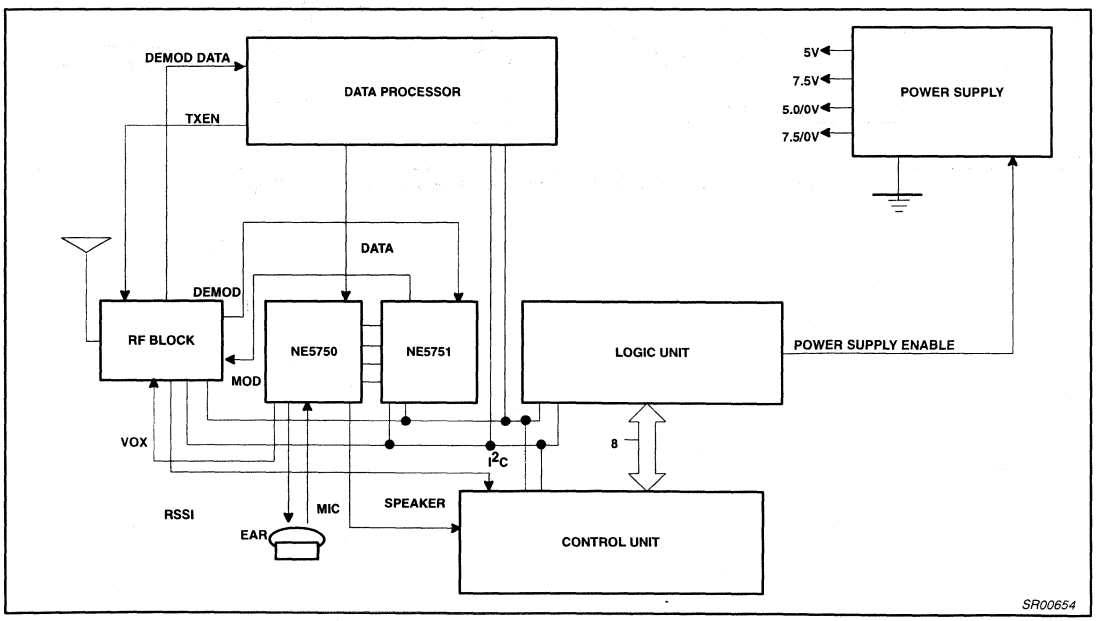


Figure 5. APROC Application Diagram

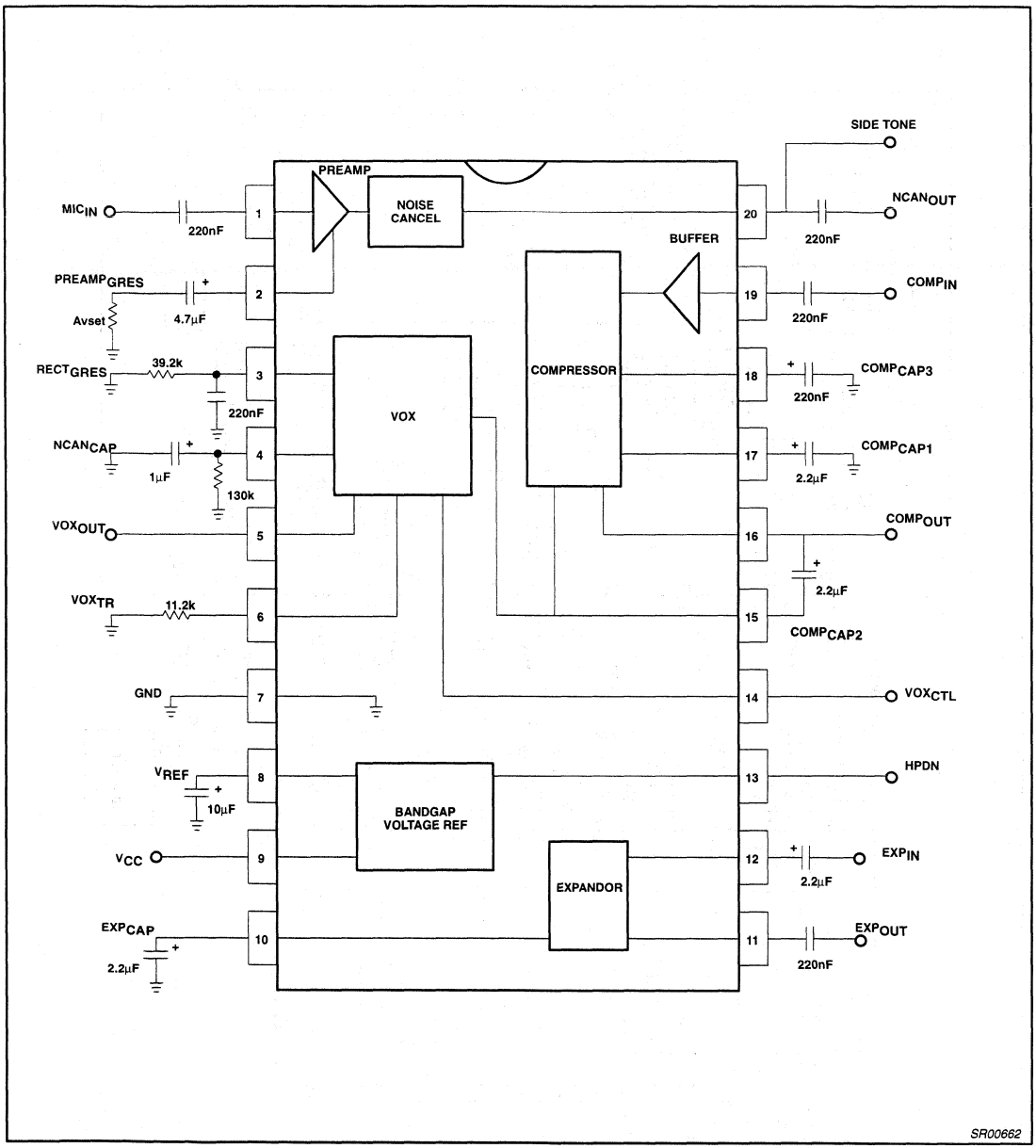


Figure 6. SA5752 Test and Application Circuit

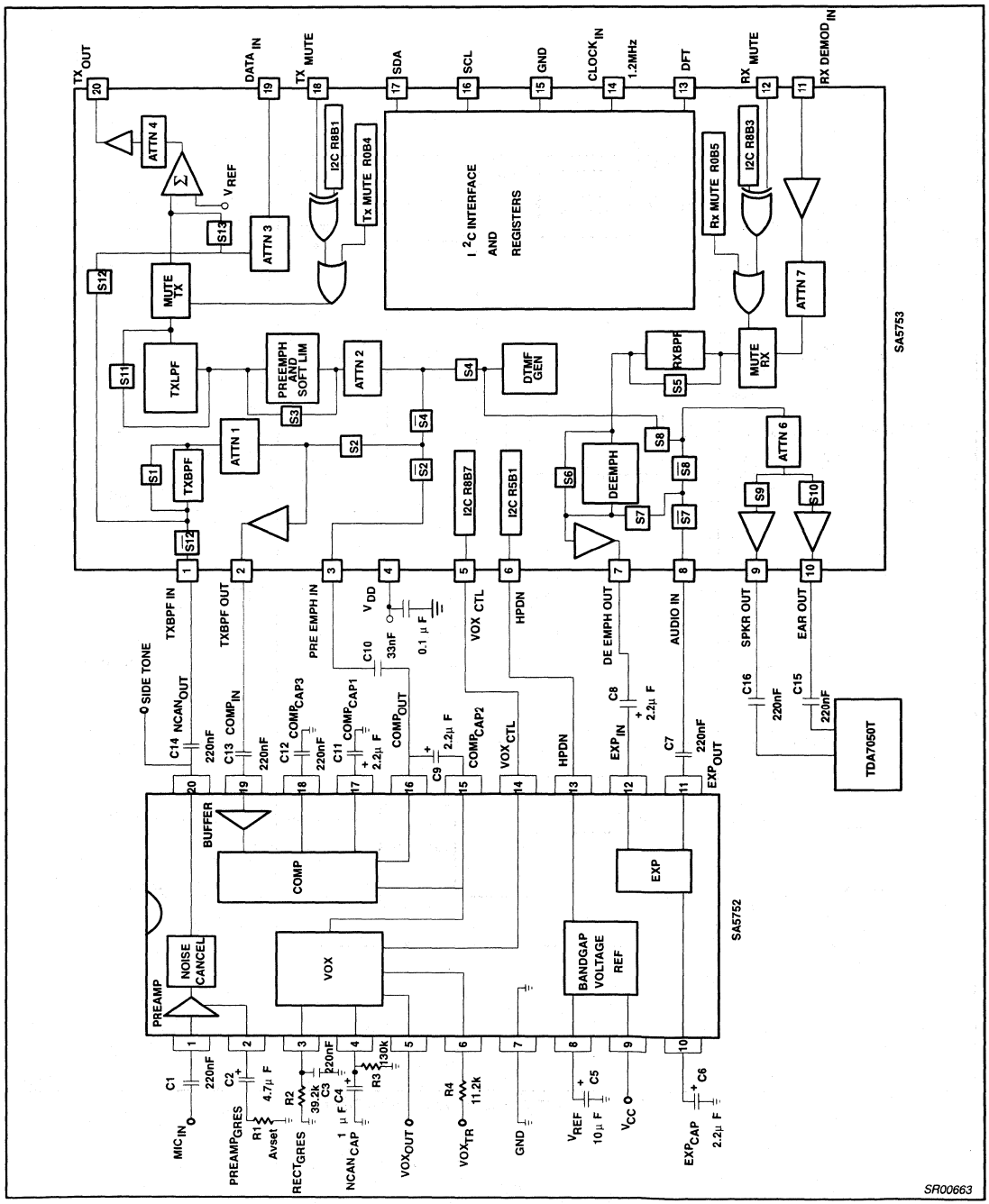


Figure 7. Application Diagram for the Audio Processor

TYPICAL PERFORMANCE CHARACTERISTICS

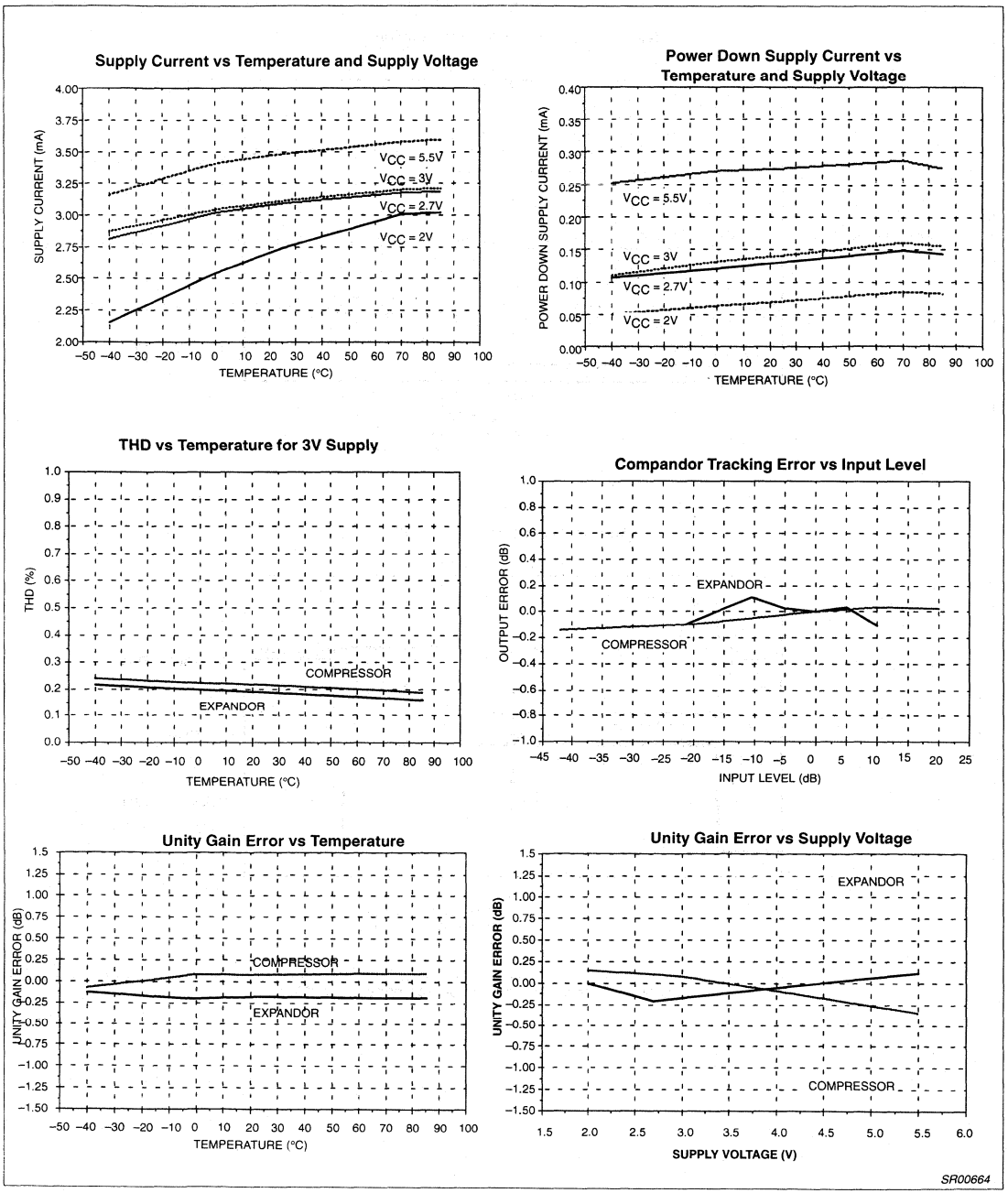
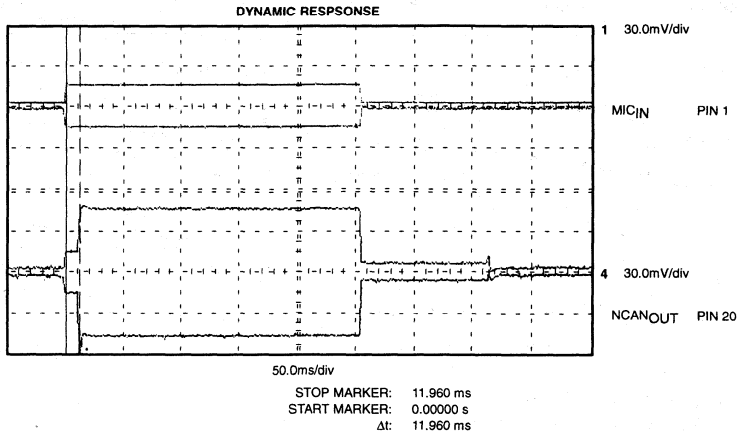


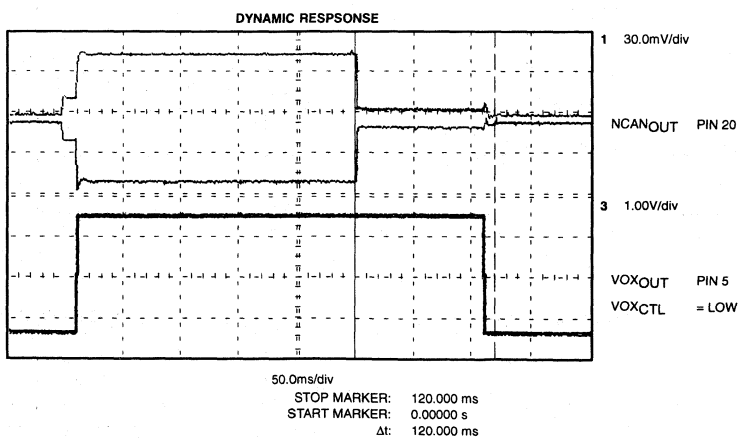
Figure 8. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Noise Cancellation Switching Amplifier



Voice Activated Transmitter (VOX)



SR00665

Figure 9. Typical Performance Characteristics (cont.)

Audio processor – filter and control section | SA5753

DESCRIPTION

The SA5753 is a high performance low power CMOS audio signal processing system especially designed to meet the requirements for small size and low voltage operation of hand-held equipment. The SA5753 subsystem includes complementary transmit/receive voice band (300-3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, digitally controlled attenuators for signal level and volume control, audio path mute switches, a programmable DTMF generator, power-down circuitry for low current standby, power-on reset capability, and an I^2C interface. When the SA5753 is used with an SA5752 (companding function), the complete audio processing system of an AMPS, TACS, NAMPS or NTACS cellular telephone is easily implemented.

The system also meets the requirements of the proposed NAMPS or NTACS specification, and can be used in cordless telephone applications.

The SA5753 can be operated without the I^2C bus interface by pulling DFT (Pin 13) HIGH.

BENEFITS

- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5752

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION

D and DK Packages

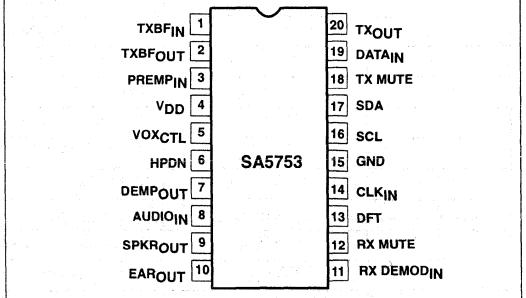


Figure 1. Pin Configuration

FEATURES

- Low 3V supply
- Miniature SSOP package
- Low power
- High performance
- Built-in programmable DTMF generator
- Built-in digitally controlled attenuators for modulation and volume control
- Built-in peak-deviation limiter
- I^2C Bus controlled
- Power-on reset
- Power down capability
- Programmable mute control
- Meets AMPS/TACS/NAMPS/NTACS requirements

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	-40 to +85°C	SA5753D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA5753DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Power supply voltage range	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to V_{DD}+0.3	V
	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature	-40 to +85	°C

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	$TXBF_{IN}$	Transmit bandpass filter input
2	$TXBF_{OUT}$	Transmit bandpass filter output
3	$PREMP_{IN}$	Pre-emphasis input
4	V_{DD}	Positive supply
5	VOX_{CTL}	Vox control output
6	HPDN	Power-down I/O
7	$DEMP_{OUT}$	De-emphasis output
8	$AUDIO_{IN}$	Audio input
9	$SPKR_{OUT}$	Audio output to speaker
10	EAR_{OUT}	Audio output to earpiece
11	RX $DEMOD_{IN}$	Rx demodulated audio signal input
12	RX MUTE	RX audio signal mute input
13	DFT	Default input, non-I^2C or stand-alone operation
14	CLK_{IN}	Clock input (1.2MHz)
15	GND	Ground
16	SCL	I^2C serial clock line
17	SDA	I^2C serial data line
18	TX MUTE	Tx audio signal mute input
19	$DATA_{IN}$	Data input
20	TX_{OUT}	Transmit output

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +3.3V, unless otherwise specified. See test circuit, Figure 2.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Power supply voltage		3.0	3.3	5.5	V
I_{DD}	Supply current	Operating IDLE Power Down (PWDN)		1.7 600 200		mA µA µA
I_{IH}	Input current high TX MUTE, RX MUTE, HPDN DFT	$V_{IN} = V_{DD}$	 –10 0	 0 +10	 +10 +30	 µA µA
I_{IL}	Input current low TX MUTE, RX MUTE, HPDN, DFT	V_{IN} = GND	 –30 –10	 –10 0	 0 +10	 µA µA
V_{IH}	Input voltage high		$0.7V_{DD}$		V_{DD}	V
V_{IL}	Input voltage low		0		$0.3V_{DD}$	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +3.3V. See test circuit, Figure 2. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV_{RMS} = -20dBm, unless otherwise specified. All gain control blocks (Attenuators) = 0dB gain, NAMPS and VCO bits set to 0.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		100		kΩ
	RX BPF gain with de-emphasis	f = 1kHz	-1.0	0	1.0	dB
	RX BPF gain with de-emphasis	f = 100Hz		-30		dBm0
	RX BPF gain with de-emphasis	f = 300Hz	8.5	9.6	11.5	dBm0
	RX BPF gain with de-emphasis	f = 3kHz	-11.5	-10.0	-8.5	dBm0
	RX BPF gain with de-emphasis	f = 5.9kHz		-58		dBm0
	RX BPF noise with de-emphasis	300Hz-3kHz		200		μV_{RMS}
	RX dynamic range	with deemphasis		80		dB
	$DEMP_{OUT}$ output impedance	f = 1kHz			40	Ω
	$DEMP_{OUT}$ output swing (1%)	2kΩ to $V_{DD/2}$; f = 1kHz		2.4		V_{P-P}
	$SPKR_{OUT}$ ouput swing (1%)	50kΩ to$V_{DD/2}$; f = 1kHz	V_{DD} -1	2.4		V_{P-P}
	EAR_{OUT} output swing (1%)	50kΩ to $V_{DD/2}$; f = 1kHz	V_{DD} -1	2.4		V_{P-P}
	$SPKR_{OUT}$ noise / EAR_{OUT} noise			200		μV_{RMS}
	CLK_{IN} high		2.1		3.0	V
	CLK_{IN} low		0		1.0	V
	TX BPF anti alias rejection	f > 50kHz		40		dB
	TX BPF input impedance	f = 3kHz		100		KΩ
	TX BPF noise	300 - 3000kHz		200		μV_{RMS}
	TX LPF gain	f = 5.9kHz		-39	-36	dBm0
	TX LPF gain with pre-emphasis	f = 1kHz, 0dBV		2.43		dB
	TX LPF gain with pre-emphasis	f = 100Hz		-19		dBm0
	TX LPF gain with pre-emphasis	f = 300Hz		-10.45		dBm0
	TX LPF gain with pre-emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre-emphasis	f = 5900Hz		-28		dBm0
	TX LPF gain with pre-emphasis	f = 9kHz		-48		dBm0
	TX overall gain	1kHz		2.43		dB
	TX overall gain	100Hz		-58	-44	dBm0
	TX overall gain	300Hz	-11.5	-10.4	-8.5	dBm0

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		-52	-45	dBm0
	TX BPF dynamic range			TBD		dB
	$PREMP_{IN}$ input impedance	f = 3kHz		100		kΩ
	TX_{OUT} Slew rate	C_L = 15pF		0.75		V/µs
	Output impedance	f = 3kHz			40	Ω
	Output swing (limiting)			1.2		V_{P-P}
	Output swing (1% THD)	5kΩ load (25°C)		1.0		V_{P-P}
	Tx DTMF signal with TXLPF and pre-emphasis			0.45		V/kHz
	Rx DTMF sidetone		-0.8		5.2	dBm0
	Time delay to mute from RX MUTE or TX MUTE transition	$V_{IN} = V_{IL}$ to V_{IH} $V_{IN} = V_{IH}$ to V_{IL}		0.5 0.5		µs µs

Table 1. Gain Control Blocks (Bit 0 is Least Significant Bit)

SYMBOL	Bits	TYPICAL STEP (dB)	TYPICAL GAIN (dB)	
			MIN	MAX
A1	4	-0.8	-12.0	0
A2a	5	±0.25	-3.75	+3.75
A2b	2	-6, (-12 on first)	-24.0	0
A3	4	-1.0	-17.0	-2.0
A4	4	±0.5	-3.5	+3.5
A6	4	-2.0	-30.0	0
A7	4	±0.5	-3.5	+3.5
NAMPS	1		+1.9 in A2b -7.6 in A4	
VCO	1		+6.0 in A4	
For A2a, A4 and A7:		MSB sets the sign of the gain MSB = 0 for gain MSB = 1 for attenuation		
For all Gain Blocks:		All bits set to 0 = 0dB gain All bits set to 1 = maximum gain or attenuation		

FUNCTIONAL DESCRIPTION

The SA5753 is an audio signal processor designed to meet the requirements of compact low voltage radio telephone equipment. It includes transmit and receive bandpass filters for voiceband (300-3000Hz) with pre-emphasis and de-emphasis respectively, a transmit peak deviation limiter, voice channel mute switches and a data path which can be summed into the transmit channel. An I^2C interface is provided for software programmability of a DTMF generator, mute polarity, selection of different power down and operating modes and control of the gain in both the transmit and receive channels.

Software programmable gain control allows the device to be automatically optimized during equipment production and offers flexibility during normal operation.

Gain Blocks

The programmable gain blocks are shown in Table 1 and Figure 2. The purpose for each block is as follows:

a. A1 compensates for microphone gain variations in the transmit path.

b. A2a compensates for transmitter dynamic range variations due to manufacturing tolerances of the SA5753 and SA5752 compandor companion device. To meet AMPS requirements, the dynamic range between the zero crossing signal level of the compandor and the peak signal allowed by the deviation limiter is adjusted to 12.34dB.

c. A2b allows coarse attenuation to be inserted in the transmit path to eliminate positive feedback effects in hands-free speaker applications. First step is 12dB followed by two steps of 6dB.

d. A3 sets the gain between the $DATA_{IN}$ pin (Pin 19) and the TX_{OUT} pin (Pin 20) and should be adjusted after A2a and A4 have been previously optimized. The SA5753 will interface directly with the UMA1000T data processor (which produces a 2Vpk data signal). For NAMPS applications an additional 10 to 14dB resistive divider must be added at the $DATA_{IN}$ pin (Pin 19) for a 2V data signal.

e. A4 compensates for transmit gain variations due to manufacturing tolerances of the SA5753, SA5752 and VCO connected to TX_{OUT} (Pin 20). After A2a has been adjusted to set dynamic range then A4 is used to set the peak output voltage at TX_{OUT} (Pin 20) such that a nominal 10kHz/V VCO produces a peak deviation of 12kHz to meet AMPS specifications.

f. A6 is the volume control for both the $SPKR_{OUT}$ and EAR_{OUT}.

g. A7 compensates for manufacturing tolerances in the SA5753 and preceeding demodulator. For AMPS requirements, a 1kHz tone with 2.9kHz deviation should produce an output signal at $DEMP_{OUT}$ (Pin 7) corresponding to the zero crossing signal level of the expandor.

NAMPS and VCO Offsets

For NAMPS applications, a '1' programmed into R5B3 (register 5, bit 3) will offset the transmit gain for NAMPS applications. It is recommended that A2a and A4 be programmed after the NAMPS option is set to compensate for manufacturing tolerances in the NAMPS offset, itself.

When the VCO bit of R5B2 is a '1', an extra gain of 6dB is provided at TX_{OUT} for direct interface to VCOs with a nominal gain of 5kHz/V.

Operation Using the I²C Communications Bus

The SA5753 includes on-chip gain blocks and options which can be programmed through an I²C interface bus. To use this capability, the DFT pin (Pin 13) must be pulled LOW. In this mode, all signal level adjustments can be made through software with no external potentiometers required.

With DFT pulled LOW, the HPDN pin (Pin 6) is an OUTPUT having the same value as the program bit in register 5 bit 1 (R5B1) of the control register bit map. The value at the VOX_{CTL} output (Pin 5) is the same as the program bit in R8B7. The HPDN and VOX_{CTL} outputs can be used to control the state of the SA5752 companion device.

Power On Reset and Power Down Modes

In order to avoid undefined states of the SA5753 when power is initially applied, a power-on-reset circuit is incorporated which defaults RxP and TxP such that the receive and transmit paths are muted if a 'high' voltage is applied to RX MUTE and TX MUTE (Pins 12 and 18). RX MUTE and TX MUTE include on-chip pull up resistors so, during power up, the user may apply a logic '1' to these pins or leave them floating. After power up, the registers can be programmed and the mutes removed by a quick access write to R0.

Three software controlled low power modes are provided on the SA5753. These are POWER DOWN (PWDN), IDLE and DENA and can be selected by programming a '1' into R6B2, R6B1 or R6B0 as follows. In PWDN mode (R6B2=1) both the voice and data channels are powered down with the respective I/O pins at a high impedance. In DENA mode (R6B1=1) the voice channels are powered down, but the data channel (from $DATA_{IN}$ and TX_{OUT}) is fully active. In IDLE mode (R6B1=1, R6B0=1) both voice and data channels are powered down. (See Table on page 8.)

The difference between selecting IDLE and PWDN is that the former maintains the normal operational bias voltages at all voice and data I/O pins and provides a glitch-free transfer from power down to a fully active mode and vice-versa.

Although the POWER DOWN mode exhibits lower power consumption, glitches may occur when transferring to an active mode because of the previous high impedance of the I/O pins.

The VOX_{CTL} and HPDN pins (Pins 5 and 6) still have the same value as R8B7 and R5B1 in all low power modes.

Operation Without Using the I²C Bus

The SA5753 can be operated in a default mode with the I²C bus bypassed. To use this mode, the DFT pin (Pin 13) is pulled HIGH, then the I²C bus is bypassed and the SA5753 operates as if all register bits in the I²C address map table are set to '0' except R1B2 (S13), R0B0 (S10) and R0B1 (S9), which are set to '1' to enable the receiver output. R6B2 (PWDN), which is controlled by the state of the HPDN pin (Pin 6), which is an input in DEFAULT mode.

When HPDN is pulled HIGH, the R6B2 bit is set to '0' and the SA5753 is placed in it's normal operating mode with all Gain Control Blocks set to 0dB except A3, which is set to –2dB.

When HPDN is pulled LOW, the R6B2 bit is set to '1' and the SA5753 enters POWER DOWN.

There is no on-chip pull-up or pull-down structure on the HPDN pin and so it must not be allowed to float in DEFAULT mode since the operating mode of the SA5753 will then be undetermined.

The Tx MUTE and Rx MUTE pins must be pulled LOW to enable the transmit and receive paths, respectively.

The VOXCTL pin (Pin 5) will follow the value of the control bit stored in R8B7 prior to pulling DFT HIGH.

The DTMF is disabled in the DEFAULT mode.

Programming Without the I²C Protocol

In the default mode, with DFT (Pin 13) and HPDN (Pin 6) pulled HIGH, the registers in the control register bit map are chained together so that bit 0 of a register is connected to bit 7 of the preceeding register with R0B6, R0B7, R1B6 and R1B7 bypassed, i.e., R0B5 is connected to R1B0, R1B5 is connected to R2B0, R2B7 is connected to R3B0, etc. Bits can then be loaded as a serial stream through the SDA pin of the I²C bus by the negative edge of a shifting clock applied at the SCL pin of the I²C bus. When a bit is loaded at SDA it will load first into R0B0 and then will be shifted to R8B7 after 68 clock edges.

A total of 68 clock pulses (applied at SCL) are therefore required to completely load the registers.

In this mode of operation the contents of the register map are also shifted out from the VOX_{CTL} pin since it takes the same value as R8B7. After power up there is no reset within the registers so the first 68 bits clock out at the VOX_{CTL} pin will have an indeterminate value.

Summary: To use this capability, the DFT pin and the HPDN pin must be pulled HIGH, the serial bit stream loaded through SCL synchronous with the negative clock edge applied at SCL for 68 clock pulses, and then the DFT pin pulled LOW.

NOTE: Default Mode is not tested in production.

Cordless Telephone Applications

For cordless telephone applications, a switch S12 is provided (R5B0) to route data through the complete transmit path while inhibiting the voice channel. In the receive path, a quick access mode is provided through the I²C to disable both EAR_{OUT} and $SPKR_{OUT}$, by setting R0B0 and R0B1, when data is detected at the $DEMP_{OUT}$ pin (Pin 7).

I²C CHARACTERISTICS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. Data transfer may be initiated only when the bus is not busy (both lines HIGH).

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired-AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

For devices operating over a wide range of supply voltages, such as the SA5753, the following levels have been defined for a logical LOW and HIGH;

$V_{ILMAX} = 0.3V_{DD}$ (max. input LOW voltage)
$V_{IHMIN} = 0.7V_{DD}$ (min. input HIGH voltage)

Data Transfer

Data is transferred from a transmitting device to a receiving device with one data bit transferred during each clock pulse on the SCL line. The transmitter also generates the clock once arbitration has given it control of the SCL line. The data on the SDA line must remain stable during the HIGH period of the clock cycle, otherwise it may be interpreted as a control signal.

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

Acknowledgement

Following each byte of data transfered, the receiver must acknowledge successful reception. To do this the transmitter releases the SDA line (allowing it to go HIGH) at the end of each transmitted byte, and it is pulled LOW by the receiver. If this condition is maintained during the next HIGH period of the clock pulse (called the acknowledge clock pulse) then data transfer is resumed. If the receiver does not pull the SDA line LOW, the transmitter will abort the transfer.

I²C Bus Data Configurations

The SA5753 is always a slave receiver in the I²C bus configuration). The slave address consists of eight bits in the serial mode and is internally fixed.

Control Registers

The control register bit map is shown below. Either a quick access or normal address mode can be used, determined by the two MSB bits in the first word following the SA5753 address word. If the quick access mode is used, the registers R0 or R1 can be updated by sending only two bytes of information (address plus update). If R0 or R1 are updated using the address mode, then B7 and B6 of the data word are ignored. In all access modes, incremental register addressing is supported with following words updating the next register until a 'stop' bit is sent.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

High Frequency = 1200kHz/6/HD
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

Low Frequency = 1200kHz/14/LD
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading DTC = 1 in R1, bit 5.

Single tones can be obtained by loading 2 into the unused tone register to silence it.

Loading a value of 1 or 0 into the registers will default the register value to 257 or 256 for high tone or low tone, respectively.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during continuous operation (DTC=1).

I²C Address and Access

S	A7 A6 A5 A4 A3 A2 A1 A0	ACK	F7 F6 F5 F4 F3 F2 F1 F0	ACK	...	P

S = start, A0 = 0, ACK = acknowledge, P = stop, A7–0 = SA5753 address fixed internally at 1000000.
Access mode is determined by F7, F6.

All access modes support incremental addressing.

Mode	F7	F6	Action
quick access	0	0	Load F5–F0 to R0B5 – R0B0
quick access	0	1	Load F5-F0 to R1B5 – R1B0
test mode	1	0	For test only. DO NOT USE.
address mode	1	1	F3–F0 point to register

Address Map

REG	Address				Register Bits							
	F3	F2	F1	F0	B7	B6	B5	B4	B3	B2	B1	B0
R0	0	0	0	0	Y	Y	RxM	TxM	A2bb1	A2bb0	S9	S10
R1	0	0	0	1	Y	Y	DTC	S4	S8	S13	S7	S2
R2	0	0	1	0	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0
R3	0	0	1	1	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
R4	0	1	0	0	A1b3	A1b2	A1b1	A1b0	A4b3	A4b2	A4b1	A4b0
R5	0	1	0	1	A6b3	A6b2	A6b1	A6b0	NAMPS	VCO	HPDN	S12
R6	0	1	1	0	A2ab4	A2ab3	A2ab2	A2ab1	A2ab0	PWDN	IDLE 1	IDLE 0
R7	0	1	1	1	A3b3	A3b2	A3b1	A3b0	A7b3	A7b2	A7b1	A7b0
R8	1	0	0	0	VOX_{CTL}	S3	S5	S6	S11	RxP	TxP	S1

Y = ignored in address mode.
For all bits TRUE = '1'

A1b3–0 = program bits for gain block A1
A2ab4–0 = program bits for gain block A2a
A2bb1–0 = program bits for gain block A2b
A3b3–0 = program bits for gain block A3
A4b4–0 = program bits for gain block A4
A5b2–0 = program bits for gain block A5
A6b3–0 = program bits for gain block A6
A7b3–0 = program bits for gain block A7
HD7–0 = high tone DTMF
LD7–0 = low tone DTMF
NAMPS = program bit for NAMPS offset
VCO = 6dB higher TX_{OUT}
RxM = receive mute
TxM = transmit mute
RxP = receive mute polarity
TxP = transmit mute polarity
DTC = DTMF continuous
S1 = bypass TXBPF
S2 = bypass compressor in TX path, inhibit pre-emph input
S3 = bypass pre-emp and limiter in Tx path
S4 = enable DTMF to TX path and inhibit $PREMP_{IN}$ and S2.
S5 = bypass RXBPF
S6 = bypass de-emph in RX path
S7 = bypass expandor in RX path, inhibit audio input
S8 = enable DTMF to RX path and inhibit $AUDIO_{IN}$ and S7.
S9 = enable $SPKR_{OUT}$
S10 = enable EAR_{OUT}
S11 = bypass TXLPF
S12 = cordless data option established
S13 = enable data path
VOX_{CTL} = enable VOX of compandor/expander circuit. This bit appears at the VOX_{CTL} pin (Pin 5) of the SA5753.
HPDN = enable power down of compandor circuit. This bit appears at the HPDN pin (Pin 6) of the SA5753
PWDN, IDLE1, IDLE0 see Table below

Low Power Modes (R6B0 – R6B2)

PWDN	IDLE1	IDLE0	
1	X	X	(PWDN) Complete power down except I²C, I/Os high impedance.
0	1	0	(DENA) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} enabled.
0	1	1	(IDLE) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} disabled.
0	0	0	Normal operation.
0	0	1	$DATA_{IN}$ to TX_{OUT} disabled.

X = don't care.

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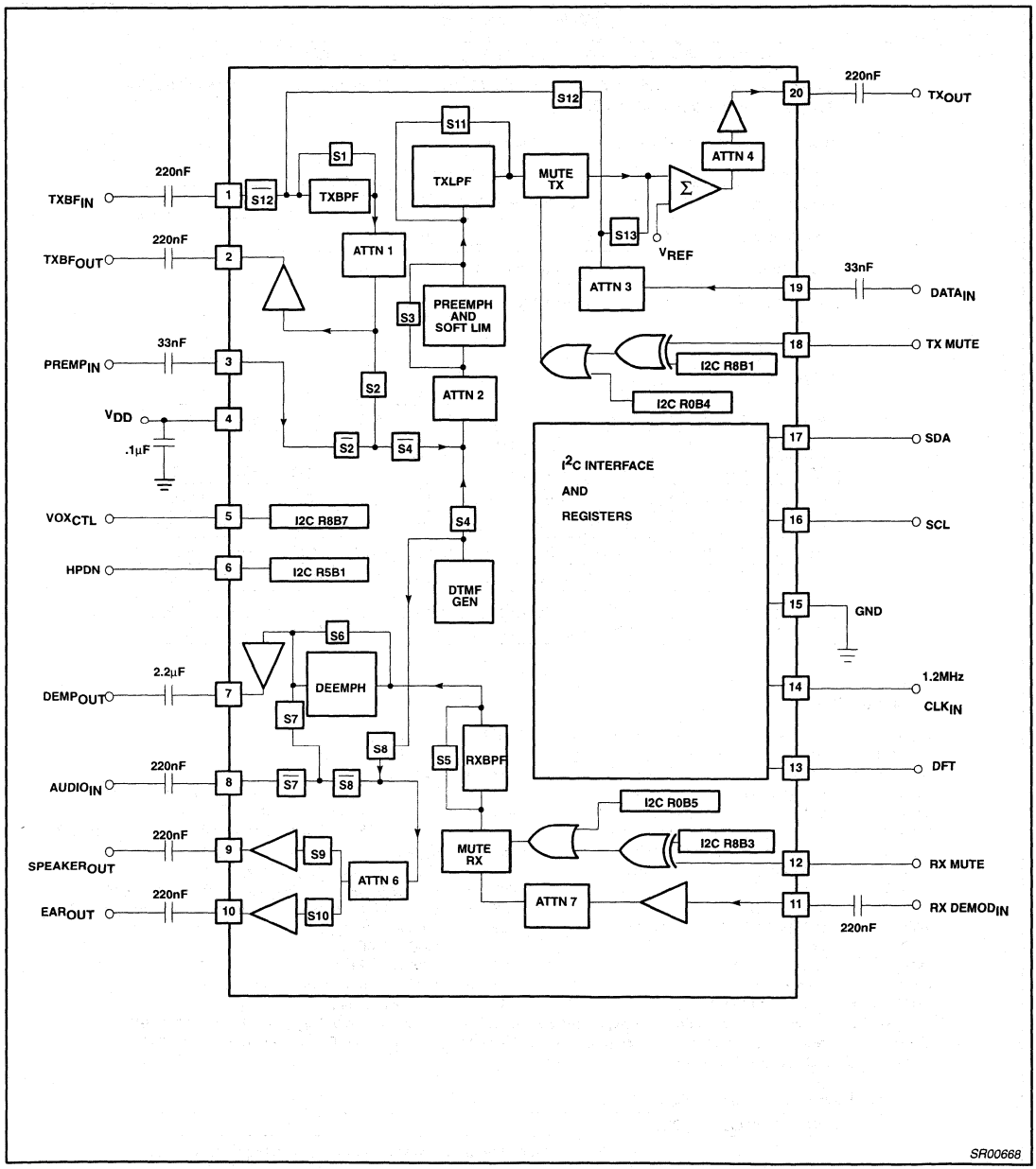


Figure 2. SA5753 Test and Application Circuit

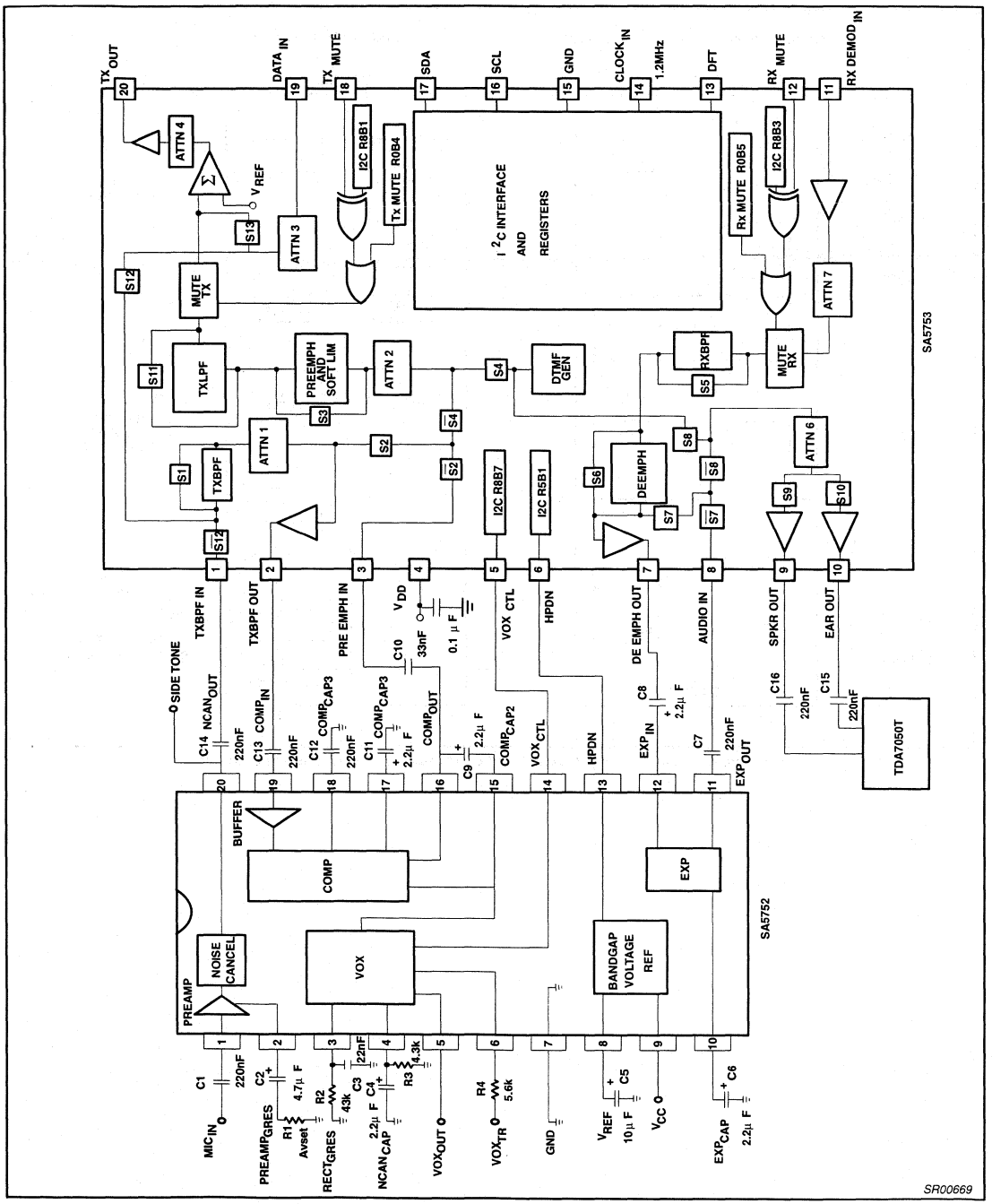


Figure 3. Application Diagram for the Audio Processor

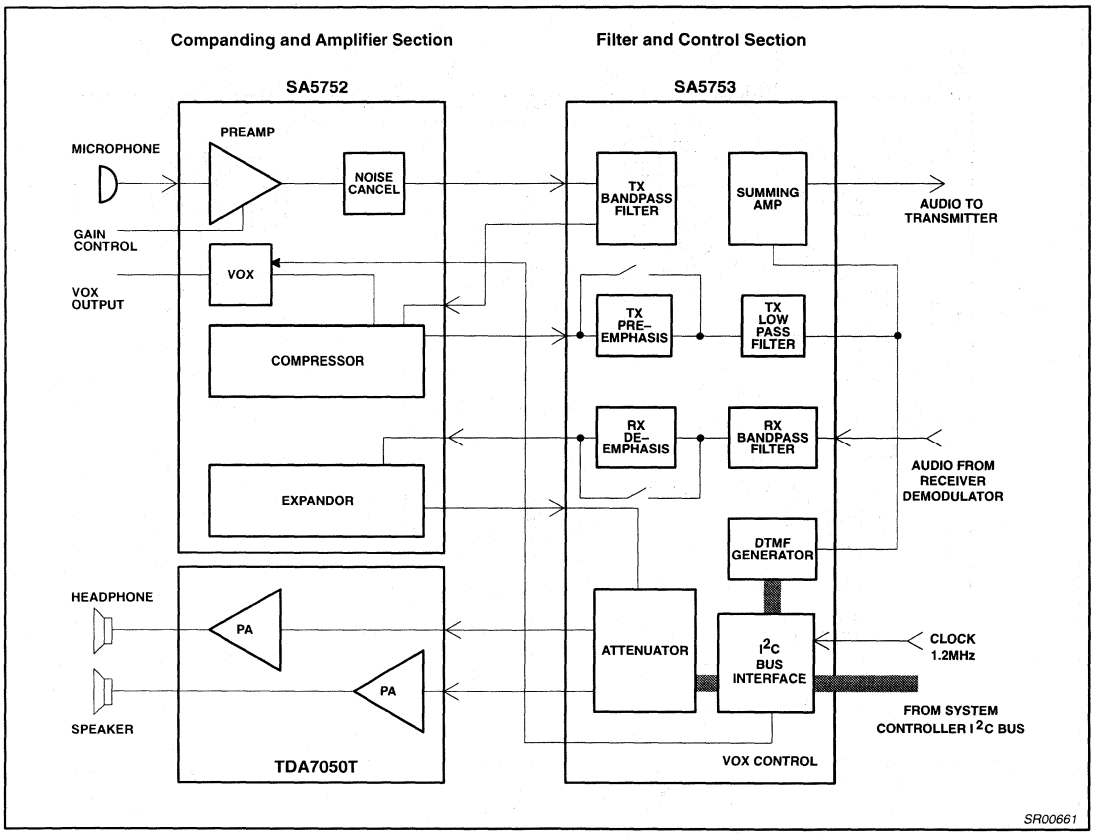


Figure 4. Typical Configuration of Audio Processor (APROC) System Chip Set

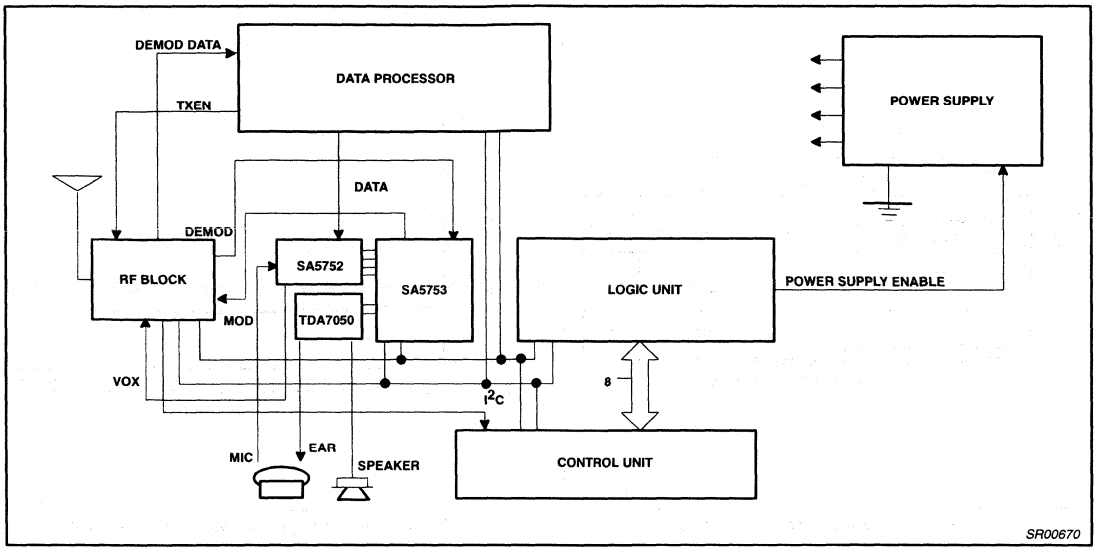


Figure 5. APROC Application Diagram

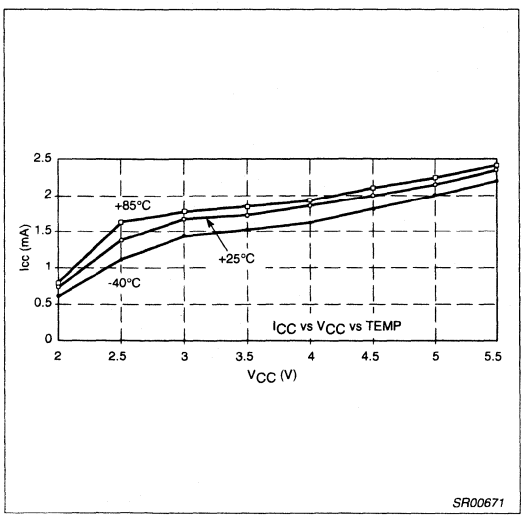


Figure 6. SA5753 Normal Operation

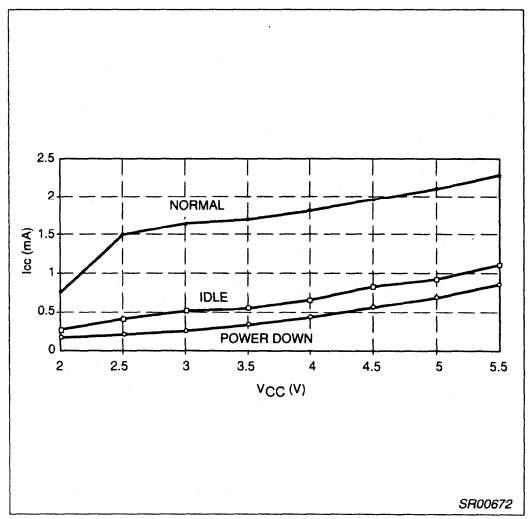


Figure 7. SA5753 Power Mode Comparison (I_{CC})

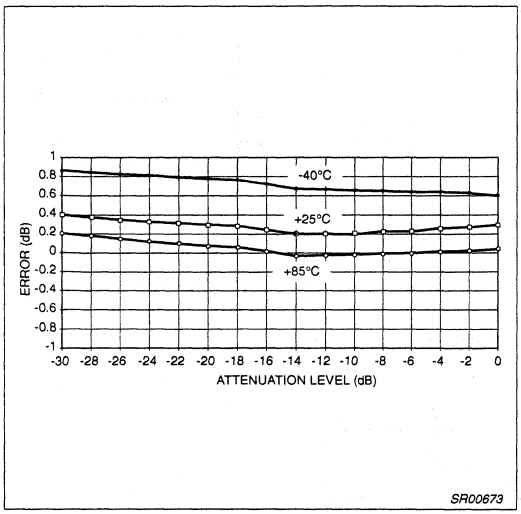


Figure 8. Gain Control, A6 Linearity

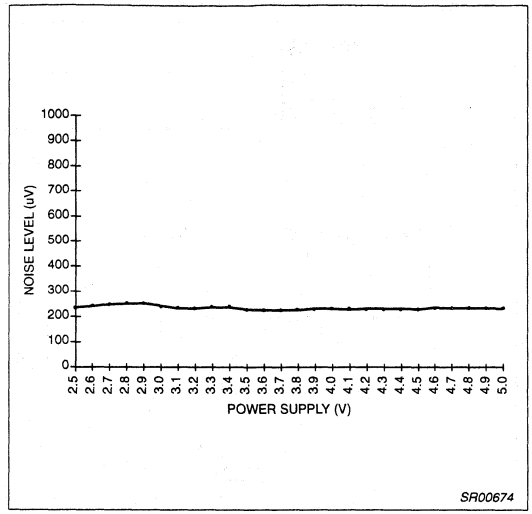


Figure 9. Power Supply vs Noise at TXBPF (25°C)

Using the SA5752 and SA5753 for low voltage designs AN1742

Author: Alvin K. Wong

INTRODUCTION

The SA5752 and the SA5753 are two audio processor chips that can be used in designs that require 3 volt operation. This chip set, known as the APROC II (SA5752 and SA5753), is functionally similar to the APROC I (SA5750 and SA5751), but with a number of enhancements which allow more design flexibility for the designer. Additionally, the APROC II offers the same high performance as the APROC I. The SA5752 is the low voltage version of the SA5750, and the SA5753 is the low voltage version of the SA5751. Figures 1 and 2 show the block diagrams of the APROC II and APROC I, respectively. Notice that the differences are subtle and pertain primarily to the amplifier section.

If a designer is not familiar with the APROC I chip set, he/she can refer to AN1741 which discusses the basics of audio processing and the key functions used to meet the strict requirements for cellular specifications. Additionally, it describes how to design with the chip set and how to measure attack and release times for the compandor section.

This application note should be used in conjunction with AN1741 to fully understand audio processing. Experience with the APROC I will help aid the designer in learning the APROC II, but this is not a necessity. This application note will focus on the main differences between the APROCs and highlight key areas of the APROC II.

I. KEY DIFFERENCES BETWEEN APROC I AND APROC II

- Comparing the SA5750 and SA5752
  - Packaging
  - External Amplifier
  - Power Consumption
- Comparing the SA5751 and SA5753
  - Packaging
  - Power Consumption
  - Programmable Gain Attenuators
  - Power Down
  - Programmable Transmit and Receive Mute Polarity Function
  - Non-I²C Operation (Default Mode)
  - Cordless Application
  - VCO Mode
  - NAMPS Mode

II. SA5752

- Preamp
- VOX
- Noise Canceller
- Compressor
- Power Down

III. SA5753

- Non-I²C Operation (Default Mode)
- Programming Without the I²C Protocol
- DTMF
- The Limiter and All-Pass Circuit

IV. EVALUATION SOFTWARE AND DEMOBOARD

- DTMF

V. QUESTIONS AND ANSWERS

I. KEY DIFFERENCES BETWEEN APROC I AND APROC II

Table 2 shows the main differences between the APROC I and II. One noticeable difference is the power consumption and power down currents. Moreover, the SA5753 has three power down modes which will be discussed in detail in the Power Down Mode section of this application note.

Comparing the SA5750 and SA5752

The SA5750 and SA5752 differ in the following ways:

Packaging

There are minimal differences between the SA5750 and the SA5752. Instead of a 24 pin package, the SA5752 is offered in a 20 pin package. This change allows the SA5752 to come in the SSOP package. The SSOP package is smaller in dimension than the standard SO package which saves space.

External Amplifiers

Since many APROC I customers use their own external speaker and ear amplifiers, the SA5752 was designed without them (see Figures 1 and 2). However, the other key blocks are present, like the preamp, VOX, compressor, expandor, and noise canceller circuit.

Since the SA5752 does not supply the ear and speaker amplifiers internally, an external one can be used. The Philips TDA7050T is the recommended choice because of its low voltage operation and high performance capabilities.

Power Consumption

The current consumption and power down mode has been improved in the SA5752. For normal operation, the SA5752 only draws an I_{CC} of 3.1mA for a 3 volt supply compared to the SA5750, where I_{CC} = 8.4mA for V_{CC} = 5V. Additionally, in the power down mode, the SA5752 only draws 0.2mA of current, compared to 1.8mA for the SA5750. Recall that the power down mode is implemented when the chip is not being used to conserve battery life. The power down feature is preferred instead of completely turning off the power to the chip because the turn on time to normal operation is faster.

Comparing the SA5751 and SA5753

The SA5751 and SA5753 differ in the following ways:

Packaging

The SA5751 is available in a 24 pin DIP package or a 28 pin SO package.

Similar to the SA5752, the SA5753 is also offered in the 20 pin SSOP package. The combination of these packages allows all the audio processing functions to be done in a minimal amount of board space.

Power Consumption

The current and voltage specification has also improved for the SA5753. This chip draws 2.1mA at 3V compared to 2.7mA at 5V for the SA5751. There is also additional current economy from the three different power-down modes, PWDN, DENA and IDLE (see Power-Down section). These power-down currents are 0.2mA, 0.6mA and 0.7mA compared to 0.9 for the SA5751.

Programmable gain attenuators

The SA5753 has the same key block functions as the SA5751, but there are additional features. The SA5753 has nine programmable gain attenuators throughout the transmit and receive path. This allows the designer the flexibility to tailor the signal level at different ports. The SA5751 has only one programmable gain attenuator in the receive path which can be used as the volume control. Table 3 shows the programmable gain attenuators' range for the SA5753.

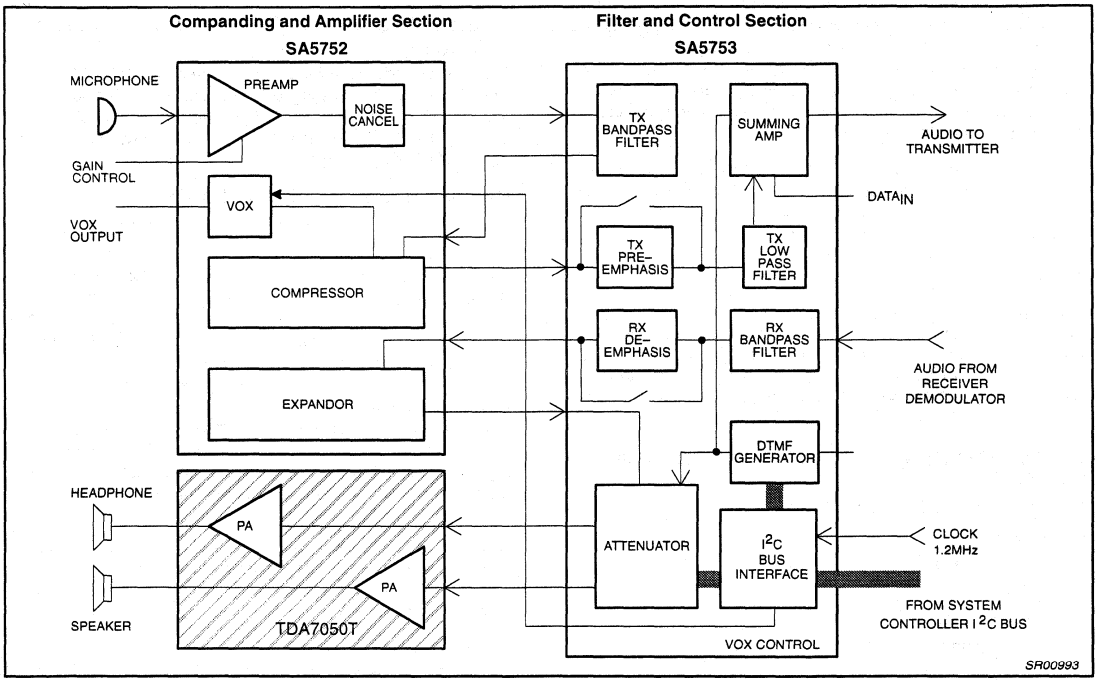


Figure 1. Block Diagram of Audio Processor (APROC II) System Chip Set

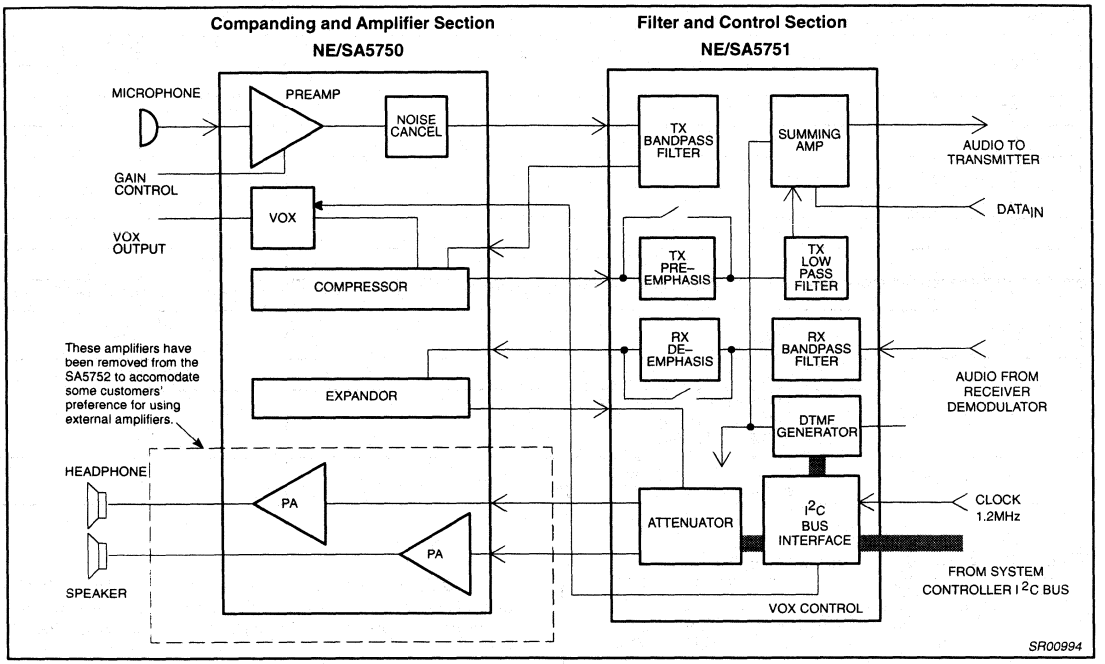


Figure 2. Block Diagram of Audio Processor (APROC I) System Chip Set

Table 2. Key Differences Between APROC I and APROC II (All values are Typical)

	APROC I		APROC II	
	SA5750	**SA5751**	**SA5752**	**SA5753**
V_{CC} (V)	4.5 – 5.5	4.5 – 5.5	2.7 – 5.5	2.7 – 5.5
I_{CC} (mA)	8.4 @ 5V	2.7 @ 5V	3.1 @ 3V	2.1 @ 3V
Total I_{CC} (mA)	11.10		5.4	
Power Down Modes	PWDN		PWDN, IDLE and DENA	
Power Down I_{CC} (mA)	1.8	0.9	0.2	PWDN 0.2 IDLE 0.6 DENA 0.7
Packages:				
NE: 0 to +70°C	NE5750N NE5750D	NE5751N NE5751D		
SA: –40 to +85°C	SA5750N SA5750D	SA5751N SA5751D	SA5752D SA5752DK	SA5753D SA5753DK
No. of Pins	24	24 or 28	20	20
Programmable Gain Attenuators	0	1	0	9
I2C Protocol	Not required	Required	Not Required	Optional*

Package Codes:
N: Plastic Dual In-Line Package (DIP)
D: Plastic Small Outline (SO)
FE: Ceramic Dual In-Line Package
DK: Shrink Small Outline Package (SSOP)

*Operating the SA5753 without the I2C protocol means DTMF generator and gain attenuators are no longer functional. See SA5753 section for more details.

Table 3. Attenuator Gain Blocks (SA5753)

SYMBOL	Bits	TYPICAL STEP (dB)	TYPICAL GAIN (dB)	
			MIN	MAX
A1	4	-0.8	–12.0	0
A2a	5	±0.25	–3.75	+3.75
A2b	2	–6, (–12 on first)	–24.0	0
A3	4	–1.0	–17.0	–2
A4	4	±0.5	–3.5	+3.5
A6	4	–2.0	–30	0
A7	4	0.5	–3.5	+3.5
NAMPS	1		+1.9 in A2b –7.6 in A4	
VCO	1		+6.0 in A4	
For A2a, A4 and A7:		MSB sets the sign of the gain MSB = 0 for gain MSB = 1 for attenuation		
For all Gain Blocks:		All bits set to 0 = 0dB gain All bits set to 1 = maximum gain or attenuation		

Table 4. Power-Down Modes (SA5753)

PWDN	IDLE1	IDLE0	
1	X	X	(PWDN) Complete power down except I^2C, I/Os high impedance.
0	1	0	(DENA) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} enabled.
0	1	1	(IDLE) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} disabled.
0	0	0	Normal operation.
0	0	1	$DATA_{IN}$ to TX_{OUT} disabled.
X = don't care			

The benefit of having signal amplitude control throughout the signal path is that a designer will no longer have to add an external amplifier to boost signals. Additionally, external resistors are no longer needed to attenuate the signal. The SA5753 programmable gain attenuators make a design more flexible which saves cost and board space from external components.

Power Down

The SA5753 has three different power down modes compared to only one for the SA5751. The three power down modes are PWDN, IDLE, and DENA (see Table 4). All three power down modes have different current consumptions and provide different options to the designer.

In the PWDN mode, the voice and data channels are powered down. This allows for maximum power conservation. In the IDLE mode, both the voice and data channels are also powered down, but are glitch free when going from power down to power up.

The IDLE mode trades a higher standby current against glitch-free power-up. Hence, the IDLE mode is used for power conservation, whereas PWDN mode is mainly used for absolute maximum power conservation.

For the DENA mode, the voice channels are powered down, but the data channel is still fully active. This allows the chip set to transmit on reverse control channel without powering up the whole APROC II.

In the PWDN mode, the SA5753 transmit path from the Tx bandpass filter in to the Tx filter out pin has only 6dB of attenuation. This means that, if a signal is present and a designer does not want this signal through, he/she should use the IDLE (or DENA) mode.

Programmable Transmit and Receive Mute Polarity Function

The SA5753 also has programmable transmit and receive mute polarity functions (TxP and RxP). A designer can mute the transmit or receive path with a logic '1' or '0' on the TxMute or RxMute pin depending on how the SA5753 is programmed by I^2C.

The benefit of having programmable transmit and receive mute polarity functions is that it eliminates the need for an inverter chip which saves on costs, power, and space. If the microcontroller or data processor (DPROC) can only provide a logic '1' to mute the Tx and Rx signal path, then to mute the chip-set the standard way, an inverter gate is needed because the logic '1' needs to be converted to a logic '0'. This logic '0' is then applied to the TxMute and RxMute pin. But with the SA5753, a logic '1' applied to the TxMute and RxMute pins will mute the Tx and Rx path if the SA5753 is programmed to mute for a logic '1'.

Figure 3 shows a diagram of how the inverter gate chip is eliminated. Additionally, a logic '0' applied to the TxMute or RxMute pin can mute the signal path if the SA5753 is programmed to mute when a logic '0' is applied to the TxMute and RxMute pins. Because of this feature the APROC II can now interface directly with the Philips Semiconductors UMA1000 DPROC.

Since the TxMute and RxMute pins are separate, the Tx and Rx path can also be muted separately. For example, if a user wants to mute his/her side of the conversation (such that the other party cannot hear), but still wants to hear the other party, the Tx path needs to be muted while the Rx path is left on. Therefore, a

designer can provide a mute button on the keypad to provide this function to the user.

Since there are separate pins to mute the Tx and Rx paths, a designer is also given full flexibility in programming these pins separately. He/she can define a logic '1' to have the Tx path mute while programming a logic '0' to have the Rx path mute, or vice versa (see Figure 4). However, in most designs a logic '0' is programmed to have the Tx and Rx path muted.

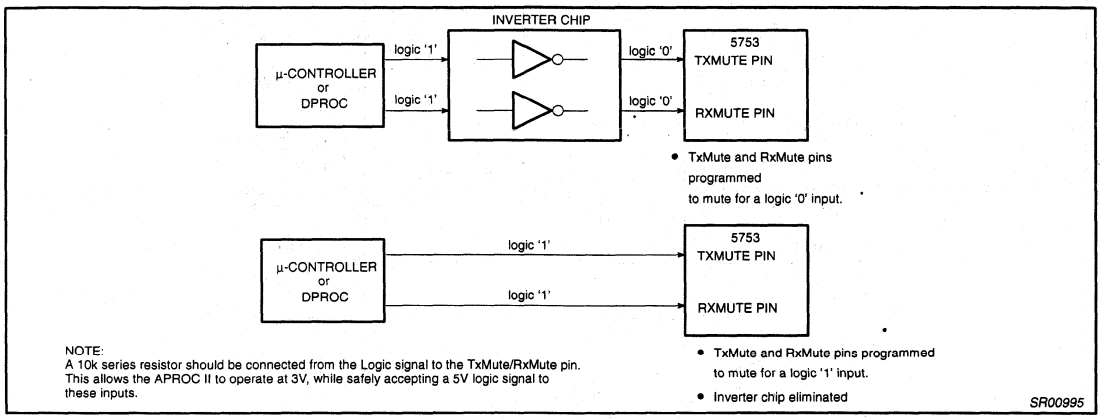


Figure 3. Benefit of Having Programmable Transmit and Receive Mute Pins

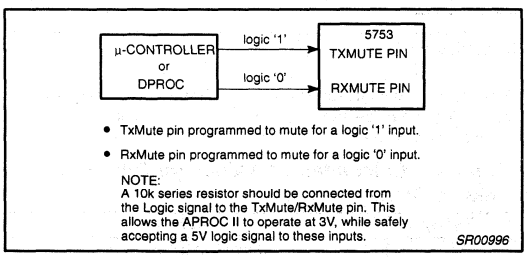


Figure 4. Muting the Tx and Rx Path for Separate Programmable Inputs

Non-I²C Operation (Default Mode)

The SA5753 can also be used without the I²C protocol by pulling the DFT (default pin) and HPDN pin HIGH. This non-I²C operation does not give the designer the flexibility to tailor the signal or use the internal DTMF generator. However, if the SA5753 is loaded serially, the SA5753 can be programmed. More information can be found in any I²C documentation. See the SA5753 section for more detailed information.

Cordless Application

Unlike the SA5751, the SA5753 can be implemented more readily for cordless phone applications. The data path can be routed through the transmit path while inhibiting the voice channel. In the receive path, the EAR_{OUT} and $SPKR_{OUT}$ can be disabled when the data is detected at the $DEMP_{OUT}$ pin.

To allow design flexibility, a designer can attenuate the data signal internally before it is passed through the TX_{OUT} pin. This eliminates the need for external components and allows programmable attenuation steps

such that different data amplitude inputs can be tailored in real-time.

VCO Mode

If the VCO bit on the SA5753 is programmed correctly, the TX_{OUT} provides an extra 6dB of gain through Attenuator 4. Therefore, the new range is 2.5dB to 9.5dB. Normally the TX_{OUT} signal is connected to a VCO (Voltage Controlled Oscillator) with a slope of 10kHz/V. The designer can implement the VCO bit to get a stronger output from the SA5753 to match 5kHz/V VCOs.

NAMPS Mode

Another key difference between the SA5753 and the SA5751 is that the SA5753 can be programmed for NAMPS mode by tailoring the gain attenuator settings.

There are two attenuators that receive the modified gain adjustments. Attenuator 4 is reduced by –7.6dB and Attenuator 2B is boosted by 1.9dB. Therefore, the new ranges are –11.1dB to –4.1dB for Attenuator 4 and –22.1dB to 1.9dB for Attenuator 2B.

The reason the gain settings are reduced is because the signal amplitude needs to be reduced before going to the transmitter. Recall that for the NAMPS mode the frequency deviation is less, so less amplitude is required.

II. SA5752

Figure 5 shows the main blocks of the SA5752: preamp, noise canceller, VOX, compressor, and expandor. This part does not require any programming blocks and therefore, no I²C is needed to operate this part. However, the SA5752 can be powered down via the SA5753 HPDN bit, which is under I²C control.

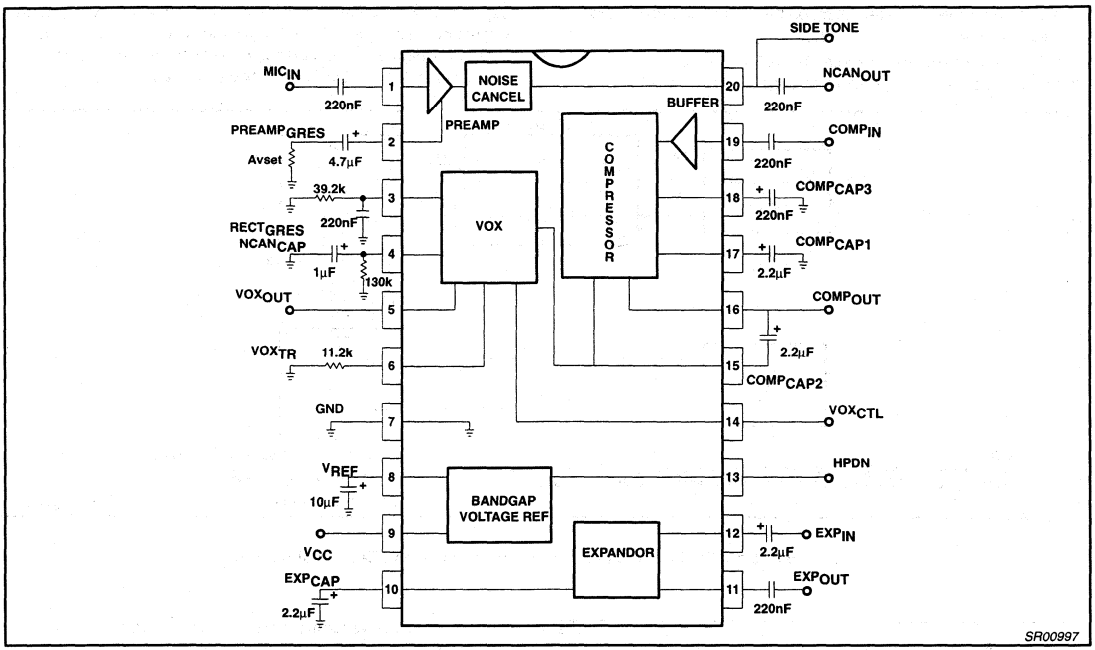


Figure 5. SA5752 Block Diagram

Preamp

The SA5752 provides a preamp which has an adjustable gain range from 0 to 40dB. The gain may be adjusted with an external resistor which connects to Pin 2 (see Equation 1, below). Table 5 shows the resistor values needed to get the appropriate gain. If a designer wants to calculate for a different value, the equation below shows how to do so.

When a designer sets the preamp gain, be sure that the output signal does not clip due to the power supply rails. To prevent this, apply the predicted strongest signal to the preamp input and observe the output while setting the gain.

Additionally, if the VOX is implemented, be sure that the extra 10dB of gain is on from the noise canceller circuit (see VOX section for more details).

$$R1 = \left[\frac{50,000}{10^{\left(\frac{X(dB)}{20}\right)} - 1}\right] - 500 \qquad (1)$$

"X" in dB

where 0 < XdB < 40dB

The preamp input impedance is 50kΩ. The output of the preamp is connected to a noise canceller which can drive a minimum load impedance of 50kΩ.

Table 5. Calculated R1 Values for Different Preamp Gains

X (dB)	R1
0	Leave Pin 2 open (∞)
5	64k
10	22k
15	10k
20	5.1k
25	2.5k
30	1.1k
35	405
40	Pin 2 AC grounded

When measuring the SA5752 preamp gain, be sure to measure the signal from Pin 20 to Pin 1. If the signal is measured from the SA5752 preamp input to the TX_{OUT} of the SA5753, the signal's amplitude will not be the expected value due to the compressor,

pre-emphasis, and attenuator settings. Therefore, remember to measure the preamp gain from the SA5752 preamp out to in.

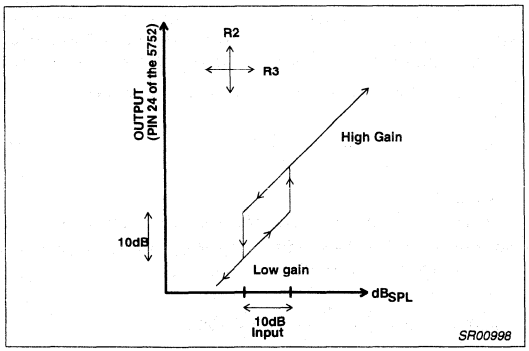


Figure 6. VOX Threshold Points

VOX

The SA5752 VOX circuitry operates like the SA5750 in that it works in conjunction with the noise canceller circuit. With the VOX activated, the noise canceller circuit will provide 10dB of gain when the input signal surpasses the "on" threshold point. When the input signal drops below the "off" threshold point, the noise canceller provides 0dB of gain. Figure 6 illustrates this function.

The VOX circuitry is useful for hands-free operation. This function is normally used in mobile conversation. Because there is road noise present in a moving vehicle, it is desirable to be able to prevent this noise from being heard. If the VOX threshold is set correctly, the noise canceller will provide 10dB of gain when the user speaks and a gain of 0dB when the user stops speaking. The other party will not hear the road noise in the background as loudly. Another feature of the VOX circuitry is that it can be used to save power. The transmitter can be switched off during non-speech periods if voice discontinuous mode (AMP) is enabled.

The VOX_{OUT} and VOX_{CTRL}, Pins 5 and 14 respectively, can be used to determine the status of the noise canceller. Since the VOX_{OUT} pin is an open collector output, a designer should connect a 10k pull up resistor to V_{CC}. This allows the output to read a high or low reading to determine the status of the noise canceller. Table 6 shows how Pins 5 and 14 can be used.

Having a logic '0' on Pin 14 (VOX_{CTRL}) is sufficient in most applications. When the voice is present, the noise canceller kicks on while the VOX_{OUT} pin supplies a logic '1'. When voice is not present, VOX_{OUT} pin supplies a logic '0'.

Supplying a logic '1' on Pin 14 would cause the VOX_{OUT} pin to stay as a logic '1' regardless of any signal input to the preamp

Table 6. VOX Truth Table

Inputs		Outputs	
Voice (Pin 1)	**VOX_{CTRL} (Pin 14 of NE5752)**	**Noise Canceller Gain**	**VOX_{OUT} (Pin 5 of NE5752)**
Not Present	logic '0'	0dB	logic '0'
Present	logic '0'	10dB	logic '1'
Not Present	logic '1'	0dB	logic '1'
Present	logic '1'	10dB	logic '1'

NOTE: If the NE5752 is used alone, be sure that the output of the noise canceller is AC coupled to the input of the compressor. Also, make sure that all of the components for the compressor are connected.

(Pin 1 of SA5752). However, the functionality of the noise canceller will still be signal dependent.

Pins 3, 4, 5, 6, and 14 all deal with the VOX's performance. Resistor R2 and capacitor C3 are connected to Pin 3. These components set the gain of the VOX. The values chosen here are for internal use only and should not be altered.

The following steps are the procedure for setting the VOX threshold. Remember that this setting can be set externally by the user using an external potentiometer or by a microprocessor which can sample the sound in the car and electronically set the "automatic environment VOX function" threshold. This can be done by implementing different resistor settings for different threshold points.

Step 1: Make sure:

a. Pin 6 is left open
b. The VOX attack and recovery components are in place at Pin 4.
c. R2 and C3 are connected to Pin 3.
d. If using the SA5752 alone, be sure to connect the preamp output (Pin 20) to the compressor input (Pin 19) with a DC blocking capacitor.
e. The preamp gain is already set (in this instance the preamp gain is 0dB)
f. Make sure that the compressor's components are also connected; compressor's attack time has to be functional.

Step 2. Apply a constant 1kHz sinewave signal to Pin 1 through a DC blocking cap (if the Philips evaluation board is used, apply the signal to the MIC input pin) with the desired threshold. In this case, $30mV_{P-P}$.

Step 3. Measure the DC voltage on Pin 4: V4=275mV

Step 4. Calculate R5:

$$R5 = \frac{V4(V)}{25\mu A} = \frac{275mV}{25\mu A} = 11k \quad (2)$$

Step 5. Connect R5 to Pin 6 and verify that VOX kicks on at the desired threshold. This set-up has the VOX kicking on at $30mV_{P-P}$ and kicking off at $11mV_{P-P}$ (for better accuracy use a 1% resistor value for R5).

Referring to the above example, if a preamp gain of 10dB was chosen before setting the threshold, the threshold will also change. So it is vital that the preamp gain be set before setting the VOX threshold.

Noise Canceller

The output of the preamp is connected to the input of the noise canceller circuit which is internal to the device. The function of the

noise canceller is to automatically provide a set gain of either 0dB or 10dB when a voice is present or not present. The gain setting can be set by implementing the VOX functions.

Although the noise canceller circuit is really designed to be used with the VOX circuitry, it can be implemented without it. The noise canceller circuit can be set up to provide either 0dB or 10dB of gain at all times, regardless of the presence of a signal. Table 7 shows how to achieve either gain settings when the VOX function is bypassed.

Table 7. Setting Up the Gain of the Noise Canceller

Pin No.	Gain of Noise Canceller	
	0dB	10dB
3	Ground	Ground
4	Ground	V_{CC}
6	10k to GND	Ground

The output of the noise canceller is accessible to the designer at Pin 20.

Compressor

The SA5752 compandor operates with a unity gain level (0dB level) of 77.5mV$_{RMS}$. It operates like the rest of the Philips Compandor family where any signal above the 0dB level in the compressor mode is half in dB, and any signal below the 0dB level is multiplied by 2 (assuming the unit is in dB)

As for the Expandor, the levels above and below the 0dB level are modified by the opposite of what the compressor does. This allows the signal to be restored to its original level with reduction of noise.

To determine the amplitude, the following formula is used.

$$XdB = 20\log\left(\frac{\text{AC level mV}_{RMS}}{77.5\text{mV}_{RMS}}\right) \quad (3)$$

Example:

Determine the compressor's AC voltage output if a 200mV$_{RMS}$ signal is applied to the compressor's input.

1. Convert 200mV$_{RMS}$ to dB as in Equation 3

$$XdB = 20\log\left(\frac{200\text{mV}_{RMS}}{77.5\text{mV}_{RMS}}\right) = 8.23\text{dB}$$

2. Because 8.23dB is above the 0dB level, by definition of the compressor the signal is halved to 4.12dB
3. Now converting back to voltage using Equation 3 the output is 124.5mV$_{RMS}$.

Figure 7 shows the diagram with other numbers for practice.

Power Down

The HPDN (Hardware Power Down) pin on the SA5752 can be left open or connected to V_{CC} for normal operation. For power down, a designer needs to ground this pin.

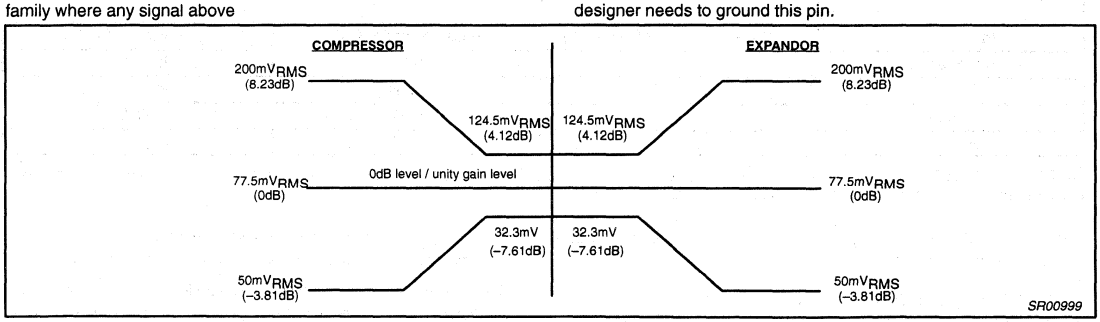


Figure 7. Determining the AC Signal Level Through a Compandor

Table 8. Programmable Divide Ratio Number

Decimal Value	Binary Value	Hi DTMF Frequency	Lo DTMF Frequency
2	0000 0010	OFF	OFF
3	0000 0011	66.66kHz	28.57kHz
4	0000 0100	50kHz	21.43kHz
5	0000 0101	40kHz	17.14kHz
• • •	• • •	• • •	• • •
254	1111 1110	787.40Hz	337.46Hz
555	1111 1111	784.31Hz	336.13Hz
256	0000 0000	781.25Hz	334.82Hz
257	0000 0001	778.21Hz	333.52Hz

III. SA5753

Figure 8 shows the main blocks of the SA5753; the Transmit and Receive Bandpass filters, the Transmit Low Pass Filter, Pre-emphasis and De-emphasis, DTMF generator, attenuators and I^{2}C controls.

Non-I^{2}C Operation (Default Mode)

The SA5753 can be used without the I^{2}C protocol. To implement this feature, the DFT pin (default, Pin 13) and HPDN (Pin 6) must be connected to V_{CC}. In the default mode, a designer has less flexibility in programming the SA5753. The only way to program the SA5753 without the I2C protocol is to load the register serially (see next section).

If a designer decides not to program the SA5753 registers, they can no longer bypass key functions or attenuate/gain the signal. Additionally, they can no longer make use of the DTMF generator.

The TxMute and RxMute pins are also no longer programmable, but are controllable externally.

A designer does not have a choice of programming the mute polarity pins. Muting the transmit and receive path now requires a

designer to supply V_{CC} to the TxMute pin (Pin 18) and RxMute pin (Pin 12). To unmute the paths, a ground connection on these pins is required.

Pin 6 must be grounded for powering down the SA5753 in the default mode. For normal operations without the I²C protocol, Pin 6 must be connected to V_{CC}. Although the SA5753 might be functional with Pin 6 left open, this is not advisable. This pin should either have V_{CC} or ground connected for a defined state. See the SA5753 data sheet for more information on non-I²C operation.

The following is a list of features when the Default Mode is implemented:

1. All previous settings in the registers are ignored except for R8B7 (VOX_{CTL}).
2. VOX_{CTL} = the setting in R8B7 before DFT goes high.
3. All attenuators are set to 0dB.
4. HPDN is now an input, LOW=PWDN Mode.
5. DTMF = OFF
6. DEEMPH = ON
7. PREEMPH = ON
8. AMPS mode
9. Closed = S9, S10, S13
10. Open = S1, S2, S3, S4, S5, S6, S7, S8, S11, S12
11. RX is muted when RXMUTE = HI
12. TX is muted when TXMUTE = HI

NOTE: When the SA5753 is changed from DFT=HIGH (Default Mode) to DFT=LOW, the register settings will have an indeterminate value and all registers will need to be reloaded to avoid undefined states.

Programming Without the I²C Protocol

In the default mode, with DFT (Pin 13) and HPDN (Pin 6) pulled HIGH, the registers in the control register bit map are chained together so that bit 0 of a register is connected to bit 7 of the preceding register with R0B6, R0B7, R1B6 and R1B7 bypassed, i.e., R0B5 is connected to R1B0, R1B5 is connected to R2B0, R2B7 is connected to R3B0, etc. Bits can then be loaded as a serial stream through the SDA pin of the I²C bus by the negative edge of a shifting clock applied at the SCL pin of the I²C bus. When a bit is loaded at SDA it will load first into R0B0 and then will be shifted to R8B7 after 68 clock edges.

A total of 68 clock pulses (applied at SCL) are, therefore, required to completely load the registers.

In this mode of operation the contents of the register map are also shifted out from the VOX_{CTL} pin since it takes the same value as R8B7. After power up there is no reset within the registers so the first 68 bits clock out at the VOX_{CTL} pin will have an indeterminate value. Once the registers are loaded, the DFT pin can be pulled low to enable the interface between the control registers and the program functions.

Summary: To use this capability, the DFT pin and the HPDN pin must be pulled HIGH, the serial bit stream loaded through SCL synchronous with the negative clock edge applied at SCL for 68 clock pulses, and then the DFT pin pulled LOW.

DTMF

The DTMF generator generates its tones by using the 1.2MHz I²C clock and dividing it down to the desired frequency. There are high and low DTMF tones, so different divide ratios are used. To tailor the exact frequency, a programmable divide ratio number is provided to the designer. Figure 9 shows the basic scheme and the formulas to calculate the desired DTMF frequency.

The programmable divide ratio number ranges from 3 to 257 for both the high and low DTMF functions. This means that the high DTMF frequency range is from 778.21Hz to 66.66kHz. The low DTMF frequency range is from 333.52Hz to 28.57kHz.

The only caution in using the DTMF generator is when the programmable divide ratio decimal number is 256 or 257. For the SA5753, decimal values 256 and 257 are defined as a binary '0' and '1', respectively (see Table 8). The reason the decimal values 256 and 257 were defined this way is because of the actual length of their binary numbers.

Decimal 256 is binary 1 0000 0000 and decimal 257 is binary 1 0000 0001. These binary numbers exceed the 8-bit register, so 256 and 257 were replaced with a decimal '0' and '1' since these values were not previously used.

Other decimal divide ratio numbers can be converted directly to a binary number which is then loaded into the 8-bit register. To turn off the high or low DTMF generator, a decimal 2, converted to a binary 0000 0010, needs to be loaded into the register.

Below are two examples of loading the DTMF generator.

Step 1: Determine what frequency is desired for the High and Low frequencies.

Step 2: Use formulas in Figure 9 to calculate the programmable 'divide ratio number' for both High and Low tones.

Step 3: Convert the calculated 'divide ratio number' to a binary number and load into the proper register. NOTE: If the 'divide ratio number' is 256 or 257, load a binary 0000 0000 or 0000 0001, respectively. To turn off the high or low

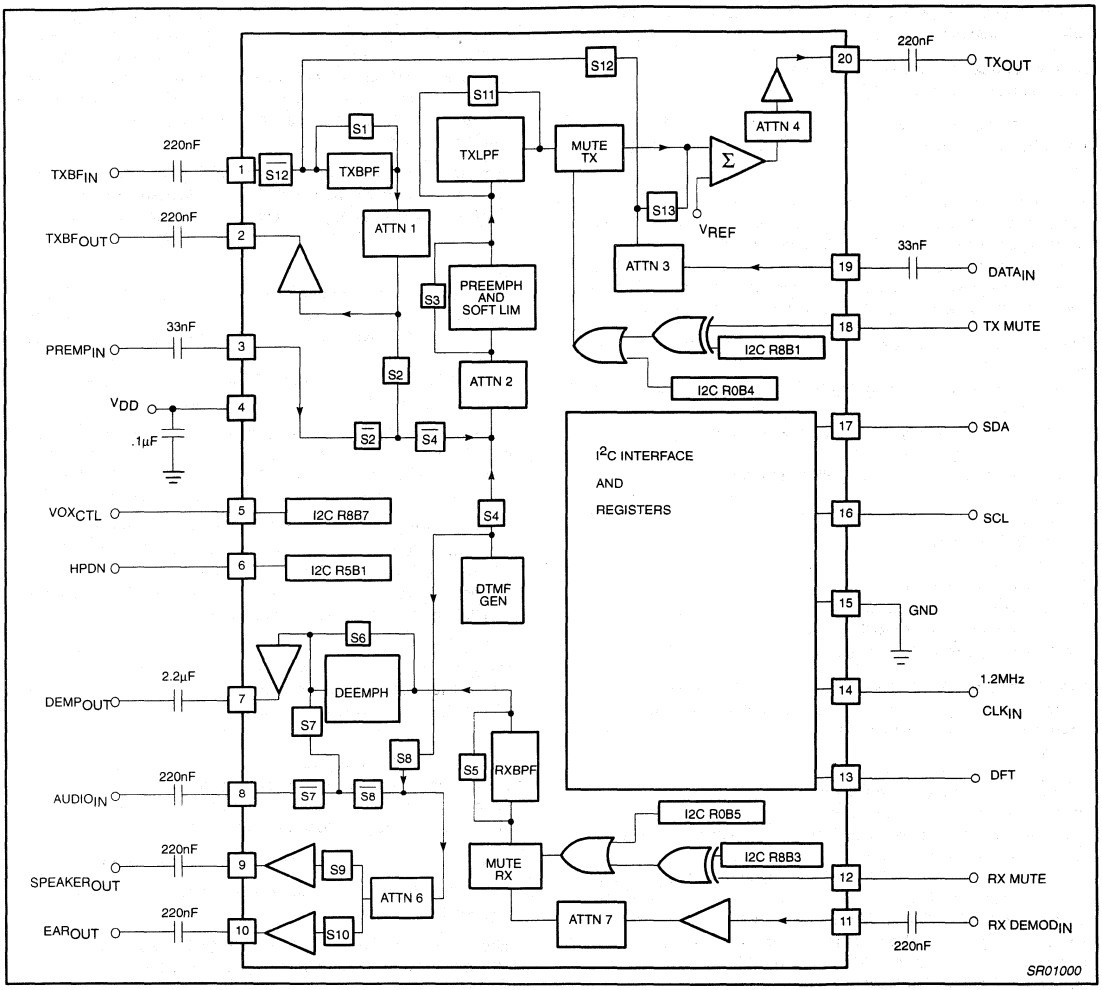


Figure 8. NE/SA5753 Test and Application Circuit

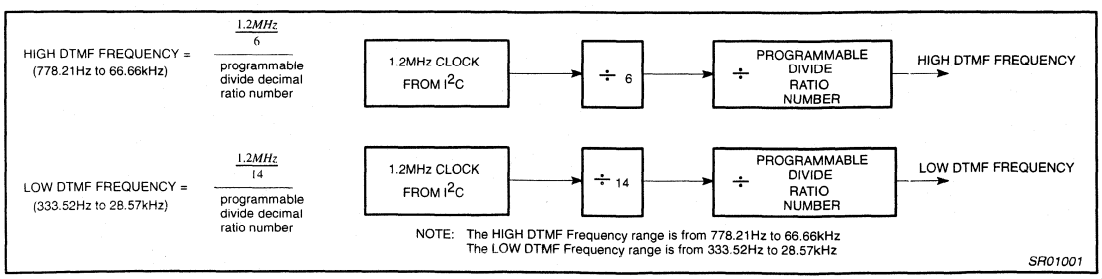


Figure 9. DTMF Formula

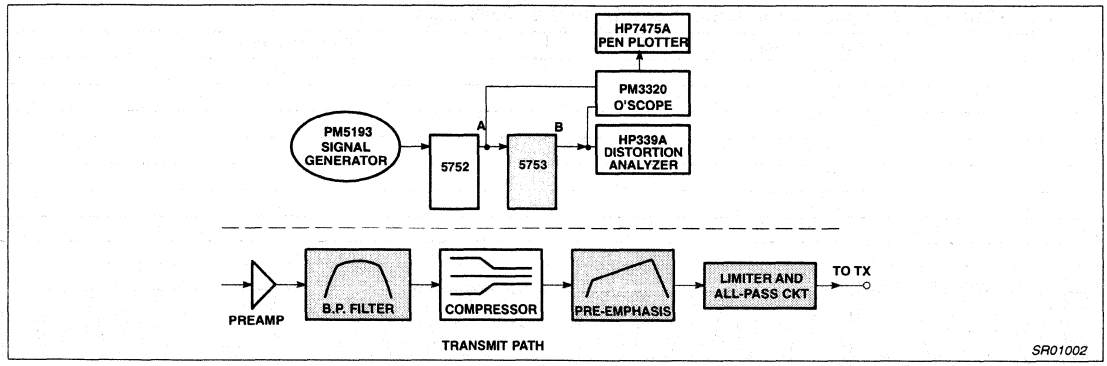


Figure 10. . Test Set-up and Tx Path of Signal

tone DTMF generator, load a binary 2 or 0000 0010 to the register.

Example 1
Program the SA5753 DTMF generator such that High DTMF = 4000Hz and Low DTMF = 3061.22Hz.

1. Using the formula in Figure 9,
   High DTMF 'divide ratio number' = 50
   Low DTMF 'divide ratio number' = 28
2. Convert 'divide ratio number' into a binary number
   High DTMF binary 'divide ratio number' = 0011 0010
   Low DTMF binary 'divide ratio number' = 0001 1100.
3. Load binary numbers into proper registers and observe on a spectrum analyzer.

Example 2
Program the SA5753 DTMF generator such that High DTMF = 778.21Hz and Low DTMF = OFF.

1. Calculate 'divide ratio number' using the formula in Figure 9,
   High DTMF 'divide ratio number' = 257
   Low DTMF 'divide ratio number' = 2, by definition for OFF see Table 8.
2. Converting 'divide ratio numbers'
   High DTMF binary 'divide ratio number' = 0000 0001 (remember the special case that applies here)
   Low DTMF binary 'divide ratio number' = 0000 0010.
3. Load binary numbers into proper registers and observe on a spectrum analyzer.

Programmable Transmit and Receive Mute Polarity Function

If a designer wants to operate the SA5753 at 3V and wants to mute the TxMute and RxMute pins with a 5V logic '1' signal, a series 10k resistor should be used. If the 10k resistor is not used, the SA5753 will draw more current. To eliminate the 10k resistor the designer should make sure that the logic '1' signal never exceeds V_{CC}.

The Limiter and All-Pass Circuit

An important aspect of the AMPS specification is concerned with the 12kHz maximum frequency deviation. The output of the APROC TX_{OUT} should be limited at a level which causes a maximum frequency deviation of 12kHz for the transmitter, regardless of the amplitude of the input signal. Figure 10 shows the equipment used for the test measurements and how the signal was processed. A 1kHz signal was applied to the input of the demo-board until a 5% distorted signal was measured at the limiter output. This waveform's peak-to-peak voltage was recorded as a reference. Then, at various chosen frequencies, the input of the demo-board was overdriven so we could record the distorted peak-to-peak waveform. (See Figure 11)

Formula 4 was used to calculate maximum frequency deviation from the waveforms shown in Figure 11.

$$\text{Max Freq Dev with All-Pass Ckt} = \left(\frac{BW_F}{BW_R}\right) 8\text{kHz} \quad (4)$$

where

BW_F = the bottom waveform's peak-to-peak voltage from one of the observed figures.

BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure 11.

Table 9. Maximum Frequency Deviation Results for the 12kHz Test

Frequency (Hz)	With All-Pass (kHz)
300	3.58
500	5.61
800	10.13
1000	10.01
1200	9.21
2000	10.01
3000	9.61

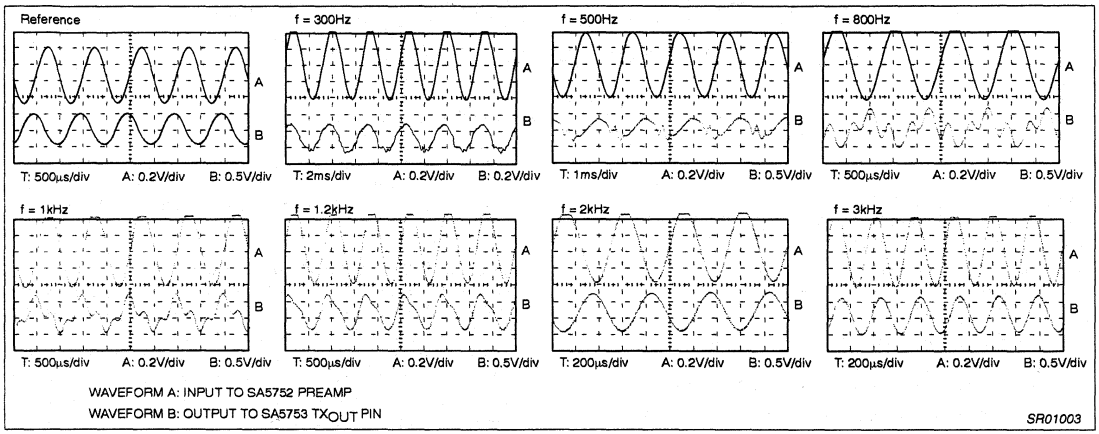


Figure 11. Results from the AMPS 12kHz Maximum Frequency Deviation Test

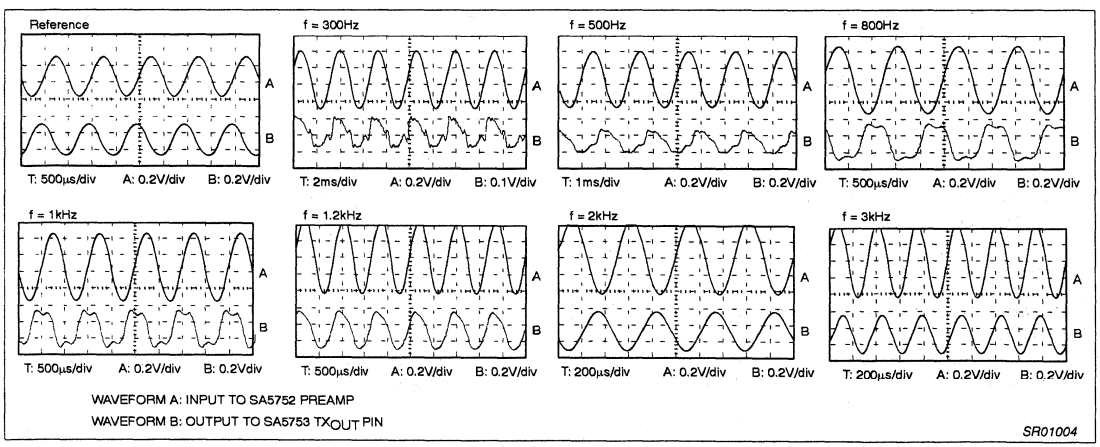


Figure 12. Results from the NAMPS 5kHz Maximum Frequency Deviation Test

Table 9 reveals the calculated results for maximum frequency deviation over the voice band. The test results show that the NE5752 and NE5753 will meet the 12kHz AMPS specification.

The same test set-up was used for the NAMPS measurements, however, the maximum frequency deviation formula changes. The following formula shows how to calculate the maximum frequency deviation for NAMPS:

$$\text{Max Freq Dev with All-Pass Ckt} = \left(\frac{BW_F}{BW_R}\right) 2.9\text{kHz} \quad (5)$$

where

BW_F = the bottom waveform's peak-to-peak voltage from one of the observed figures.

BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure 12.

Table 10. Maximum Frequency Deviation Results for the 5kHz Test

Frequency (Hz)	With All-Pass (kHz)
300	1.48
500	2.11
800	3.27
1000	3.46
1200	3.42
2000	3.65
3000	3.56

Formula 5 was used to calculate the maximum frequency deviation in Table 10 from the waveforms shown in Figure 12. These test results show that the APROC II will meet the 5kHz maximum frequency deviation for NAMPS.

IV. EVALUATION SOFTWARE AND DEMOBOARD

The APROC II demoboard and evaluation software are for evaluation purposes only. It can help a designer understand the hardware and software functionality. The APROC II schematic and layout can be seen in Figures 13 and 14, respectively. The function of each external component is briefly shown in Figure 13.

In this software package, the screen (see Figure 15) only shows the signal path for the SA5753. Recall that for the audio processing chip, the signal is routed between the SA5752 and SA5753. The appropriate pin numbers are labeled to show where the signal enters and leaves the SA5753.

The upper half of the screen is the Tx path and the lower half of the window is the Rx path. To complete the signal path, a designer can use the computer's arrow keys to get to the area of interest. The space bar is used to toggle on and off path switches and key functions (like NAMPS, VCO, HPDN, VOX_{CTRL} etc).

The 'greater than' (>) or 'less than' (<) symbol keys on the key board are used to vary the value of the gain attenuator blocks. The way the gain attenuator blocks are programmed does not follow the logical way where the 'greater than' symbol key means going up in gain and the 'less than' symbol means decreases gain. Instead, the set up is programmed logically by the bits. So a user should use the 'greater than' and 'less than' symbol keys to vary the value, but continue to use the keys until the values stop changing. (See Table 11.)

To power down the chip set the following steps should be taken:

1. To power down the SA5752, move the marker to HPDN and hit the space bar to implement this function.

2. To implement one of the SA5753 three power down modes move the marker to the Power = 000 Bin and program the appropriate mode.

- For PWDN, set Power=1xx Bin; X=don't care
- For IDLE, set Power = 011 Bin
- For the DENA mode, set Power= 010 Bin
- For normal operation, set Power= 000 Bin
- For $DATA_{IN}$ to TX_{OUT} disabled, set Power= 001 Bin. This can be used for cordless applications

To power up the chip set, a designer needs to set the Power=000 Bin (for the SA5753) and toggle the HPDN section (for the SA5752).

DTMF

To implement the DTMF tones, a user can program the high and low tones by typing in the frequencies or programming the I^2C bits.

The high decimal value is from 2 to 257 where the frequency range is from off to 778.21Hz–66.66kHz. The low decimal value is from 2 to 257 where the frequency range is from off to 333.52Hz up to 28.57kHz.

The difference between the SA5753 DTMF generator and the SA5751 is that when the cycle is completed, the DC voltage goes back to 0V, whereas the SA5751 might not return to 0V. Therefore, upon switching back to the Tx voice path, a glitch may be heard from the SA5751, but not from the SA5753.

V. QUESTIONS AND ANSWERS SECTION

Q: I connected your evaluation board and software program but I do not see any output signal on the Transmit path. My input signal is connected to the Mic input of the SA5752. What is the problem?

A: There are several issues to look at. Make sure that the TxMute and RxMute pins are defined. If the registers are programmed such that the TxMute and/or RxMute pins need to be grounded for a signal to flow, please be sure that those pins are grounded.

If the registers are defined such that the TxMute and RxMute pins need V_{CC} connected to them for a completed signal path, please connect V_{CC} to the pins. Although leaving these pins open may work, it defines an open state and is, therefore, not guaranteed.

Q: When I program a DTMF tone, it only stays on for 96ms. How can I make it stay on longer?

A: The DTMF generator is designed to stay on for only 96ms. If a longer tone is desired, the DTMF registers must be re-loaded before the 96ms expires or set DTC = 1. For the evaluation program, the DTMF register can be loaded up automatically to observe the DTMF tone. Just toggle the space bar on the "DTMF frequency DTC" section.

Q: On the evaluation program, there are ADD field and REG values. What are these?

A: These are the registers (ADD = Address field and REG = the register) that must be programmed when using the SA5753 in the I^2C mode. The address field defines which portion of the chip is being accessed (See SA5753 data sheet for a detail look). The register bits control the functions of the block.

If a designer toggles in/out functions, they can see the registers which control that function. The Evaluation software is meant as a learning tool to aid the designer in getting up to speed.

Q: The SA5753 seems to be consuming more current than usual. Is this part damaged?

A: One area to look at is the I^2C clock. If the I^2C clock goes below ground, the SA5753 will draw more current. Therefore, be sure

that the I^2C clock is set at 1.2MHz square wave and it is from ground to V_{CC}.

Q: I have a Philips APROC II demoboard and a 5V I^2C interface board. At the present moment, I use two supplies to run the APROC II board at 3V and the Interface board at 5V. Is there a 3V chip available that can be used for the interfacing between the computer's printer port to the I^2C section of the chip?

A: Yes, there is a 3V interface chip; the Philips PC74HC4049T. When a customer purchases an APROC II demoboard, he/she should receive an interface board. Most likely it will be the 3V version.

Q: The APROC II seems to draw more current than usual when I mute the TxMute and RxMute pins with a 5V logic '1' signal. The APROC II is operating at 3V. Is this normal, and if not, what can I do?

A: If you are going to operate the APROC II at 3V and apply 5V to the RxMute and TxMute pins, a series 10k resistor should be used to allow for this configuration.

If the logic '1' input is 3V and the APROC II is operating at 3V, the 10k resistor is not required. In general, it is safe to say that the logic '1' input should be no higher than V_{CC} if the 10k resistor is not used.

Q: I am evaluating your DTMF generator using the Philips evaluation program and demoboard. The frequency calculated and the frequency measured is correct but The evaluation screen, however, sometimes shows a different number, but the number shown is not too far off. Is there a bug in the program?

A: Yes, the program display is not correct. What you calculate and measure is fine. The program is incorrect at this time.

Q: I am evaluating the current consumption of the APROC II demoboard. I read a higher current than what is spec'd in the data sheet. What am I doing wrong?

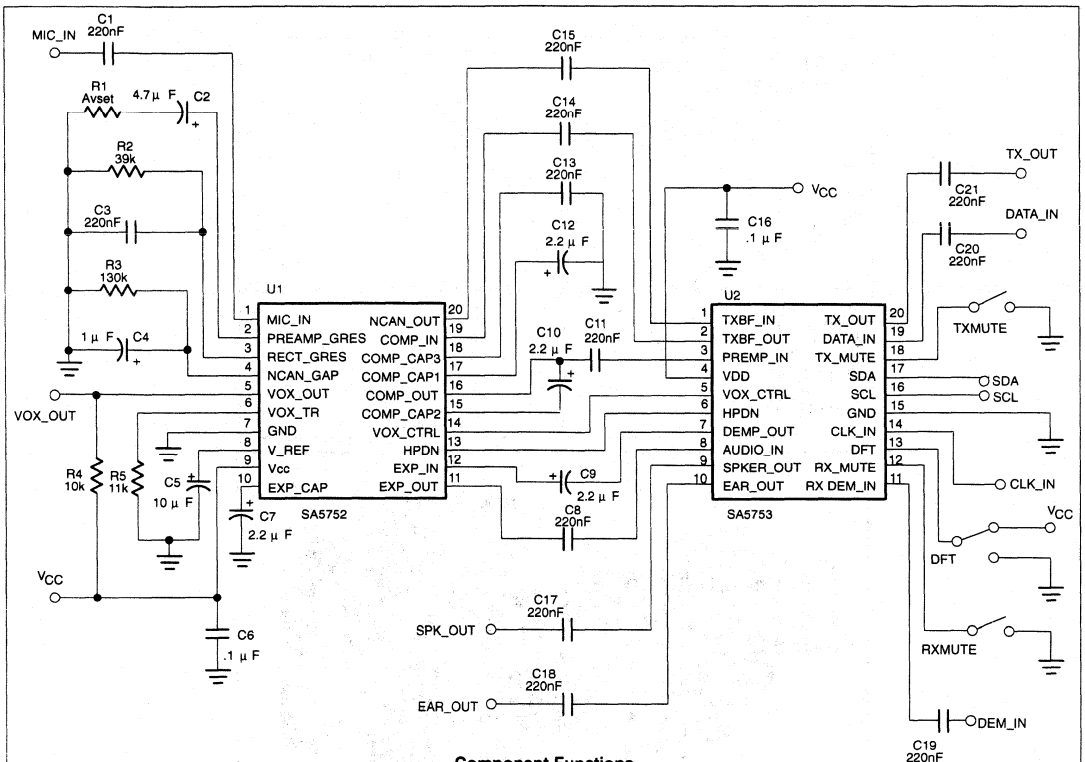
A: Remember that the I^2C interface card will draw some current away from the APROC II board (if it's connected that way). To avoid this problem, operate the I^2C interface card with a separate power supply and then measure the APROC II current.

Q: I have your APROC II evaluation demoboard. I am applying an input signal of 1kHz at $100mV_{RMS}$ to the MIC input and I am not getting any signal output on the TX_{OUT} pin. Any suggestions?

A: Your transmit path is probably open. To close the path you can do one of two things: either ground the TxP Mute pin (Pin 18) or redefine TxP to mute for a different input. You should also make sure that the SA5752 and SA5753 are in the power up state.

Q: I have a very unique situation using the SA5753. I would like to use the Default mode and I^2C mode in different situations. I know that the HPDN pin becomes an output when I^2C mode is implemented; and I know that the HPDN pin becomes an input when the Default mode is implemented. In my application I do not care about current consumption, therefore, the HPDN pin is not important to me. What can I do so that I don't leave the HPDN undefined, but at the same time, I allow myself to switch back and forth between the two modes?

A: For ease of use in the Default Mode without worrying about the function of the HPDN pin, the user can add an external pull-up resistor of 100kΩ between HPDN (Pin 6) and V_{DD}. This will put the SA5753 in Normal (active) Default operation when DFT (Pin 13) is pulled HIGH. For Power Down Mode the user will need to pull the HPDN pin LOW.



Component Functions

C1	DC blocking capacitor for MIC IN pin
C2	DC blocking capacitor for Preamp gain
C3	Used for filtering, internal use only
C4	Used to set attack and release time of VOX
C5	V_{REF} filter capacitor
C6	V_{CC} bypass capacitor
C7	Sets attack and release time of expandor
C8	DC blocking cap for Expandor out
C9	DC blocking cap for De-emphasis out
C10	AC bypassing for compressor
C11	DC blocking cap for Pre-emphasis in
C12	Sets attack and release time for compressor
C13	Passes AC to GND
C14	DC blocking cap for compressor in
C15	DC blocking cap for TXBF in
C16	V_{CC} bypass cap
C17	DC blocking cap for SPKR OUT
C18	DC blocking cap for EAR OUT
C19	DC blocking for Demodulation in pin
C20	DC blocking for Data in pin
C21	DC blocking cap for Tx OUT
R1	Sets microphone preamp gain
R2	Sets gain of VOX, but for internal use only. Effects voltage on Pin 4.
R3	Used to set the release time of VOX
R4	Pull-up resistor to get logic level out
R5	Sets threshold level of VOX

SR01005

Figure 13. APROC II Evaluation Board Schematic

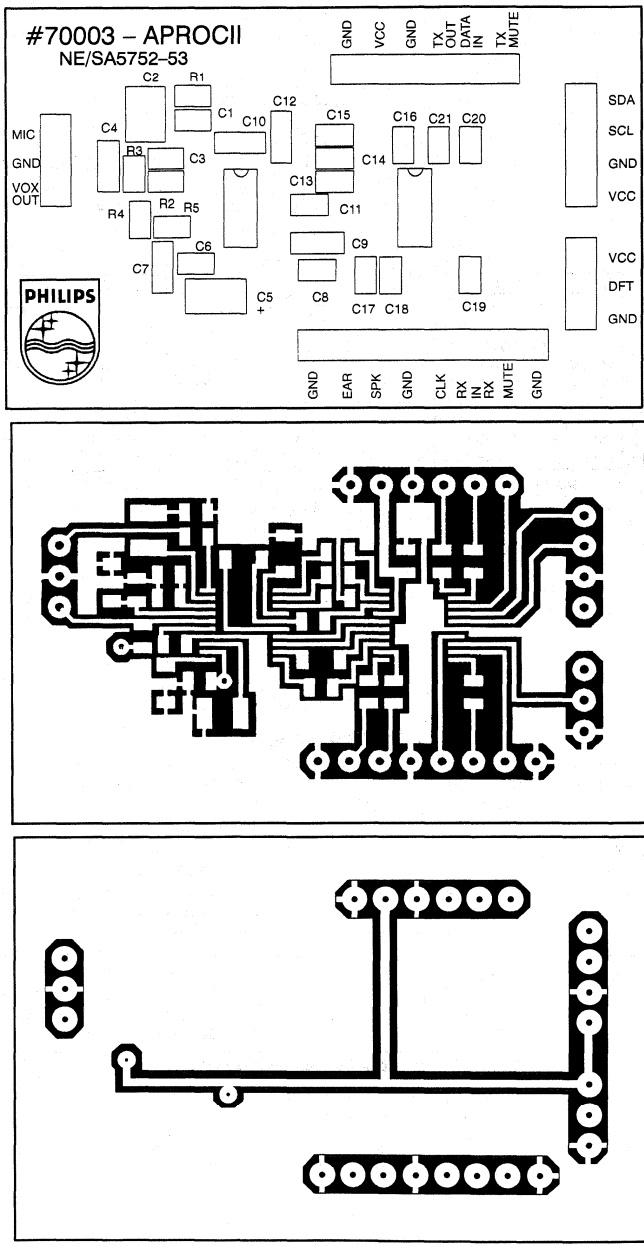


Figure 14. APROC II Evaluation Board Layouts

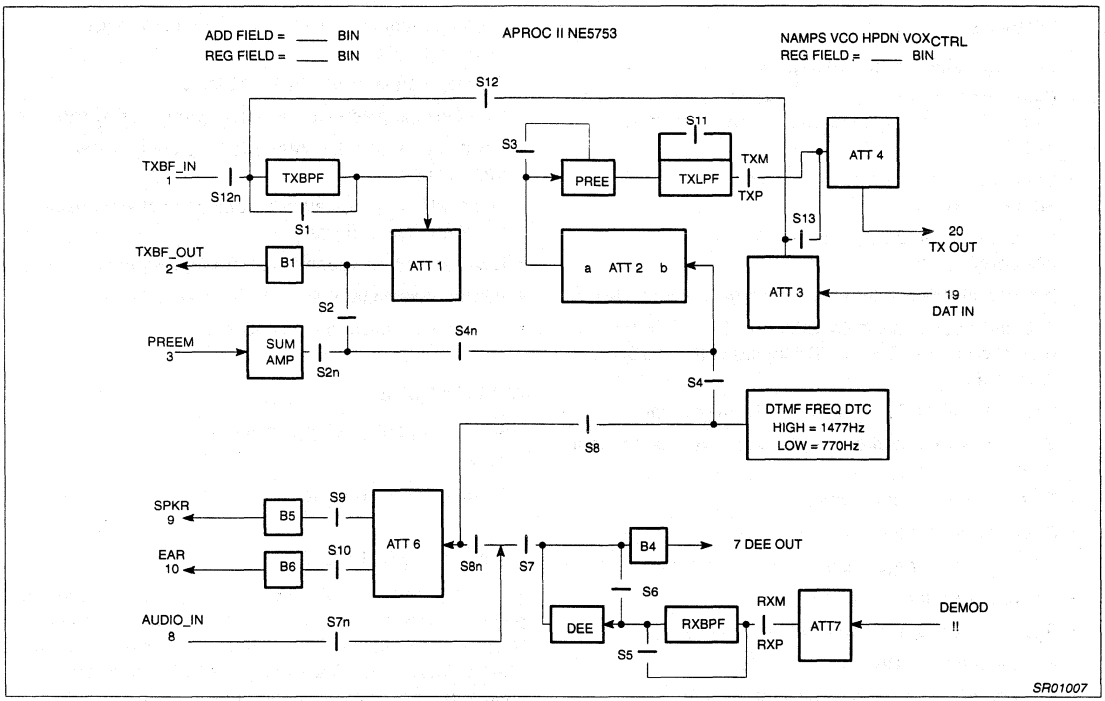


Figure 15. Graphical Display of SA5753 I²C Evaluation Program

Table 11. Gain Attenuator Steps

SYMBOL	Sequence of Gain Attenuator Steps
A1	0, –0.8, –1.6, –2.4, –3.2, –4.0, –4.8, –5.6, –6.4, –7.2, –8.0, –8.8, –9.6, –10.4 –11.2, –12
A2a	0, 0.25, 0.50, 0.75, 1.00, 1.25, 1.50, 1.75, 2.00, 2.25, 2.50, 2.75, 3.00, 3.25, 3.50, 3.75, 0, –0.25, –0.50, –0.75, –1.00, –1.25, –1.50, –1.75, –2.00, –2.25, –2.50, –2.75, –3.00, –3.25, –3.50, –3.75
A2b	0, –12, –18, –24
A3	–2, –3, –4, –5, –6, –7, –8, –9, –10, –11, –12, –13, –14, –15, –16, –17
A4	0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 0, –0.5, –1.0, –1.5, –2.0, –2.5, –3.0, –3.5
A6	0, –2, –4, –6, –8, –10, –12, –14, –16, –18, –20, –22, –24, –26, –28, –30
A7	0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5, 0, –0.5, –1, –1.5, –2, –2.5, –3, –3.5

POCSAG paging decoder PCF5001

FEATURES

- Wide operating supply voltage range (1.5 to 6.0 V)
- Extended temperature range: –40 to +85 °C (between –40 to –10 °, minimum supply voltage restricted to 1.8 V)
- Very low supply current (60 μA typ. with 76.8 kHz crystal)
- Decodes CCIR radio paging Code No. 1 (POCSAG-code)
- Programmable call termination conditions
- 512 and 1200 bits/s data rates (2400 bits/s with some restrictions), see Section "Decoding of the POCSAG data stream"
- Improved ACCESS synchronization algorithm
- Supports 4 user addresses (RICs) in two independent frames
- Eight different alert cadences
- Directly drives magnetic or piezo ceramic beeper
- High level alert requires only a single external transistor
- Optional vibrator type alerting
- Silent call storage, up to eight different calls
- Repeat alarm facility
- Programmable duplicate call suppression
- Interfaces directly to UAA2050T, UAA2080 and UAA2082 digital paging receivers
- Programmable receiver power control for battery economy
- On-chip non-volatile EEPROM storage
- On-chip voltage converter with improved drive capability
- Serial microcontroller interface for display pager applications
- Optional visual indication of received call data using a modified RS232 format
- Level shifted microcontroller interface signals
- Alert on low battery
- Optional out-of-range indication.

APPLICATIONS

- Alert-only pagers, display pagers
- Telepoint
- Telemetry/data receivers.

GENERAL DESCRIPTION

The PCF5001 is a fully integrated low-power decoder and pager controller. It decodes the CCIR radio paging Code No.1 (POCSAG-Code) at 512 and 1200 bits/s data rates. The PCF5001 is fabricated in SACMOS technology to ensure low power consumption at low supply voltages.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5001T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCF5001H	LQFP32[1]	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

BLOCK DIAGRAMS

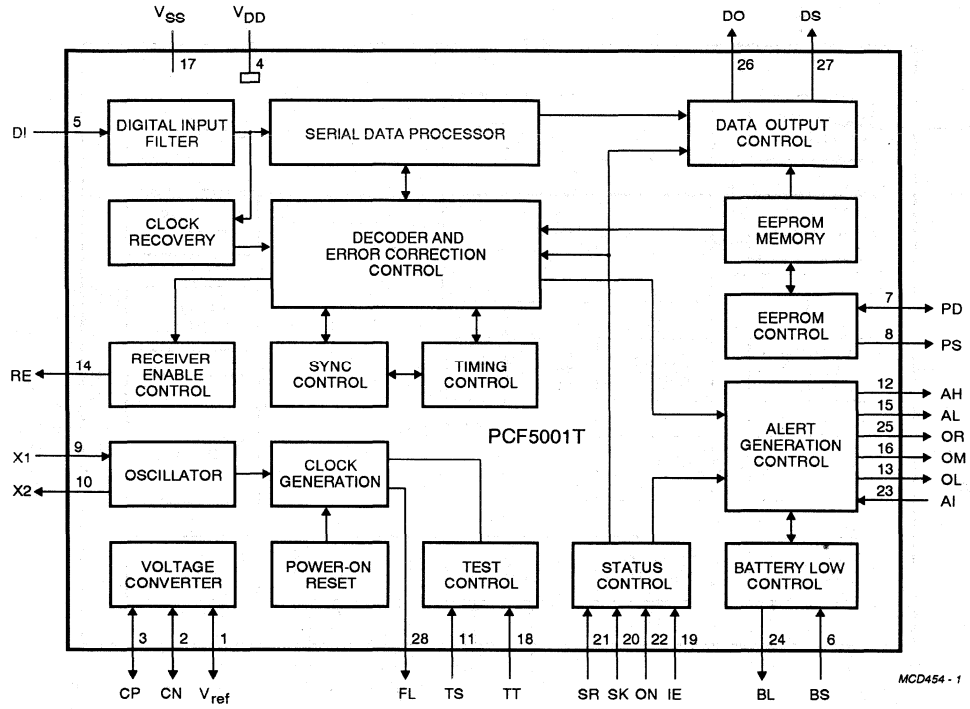


Fig.1 Block diagram (SO28; SOT136-1).

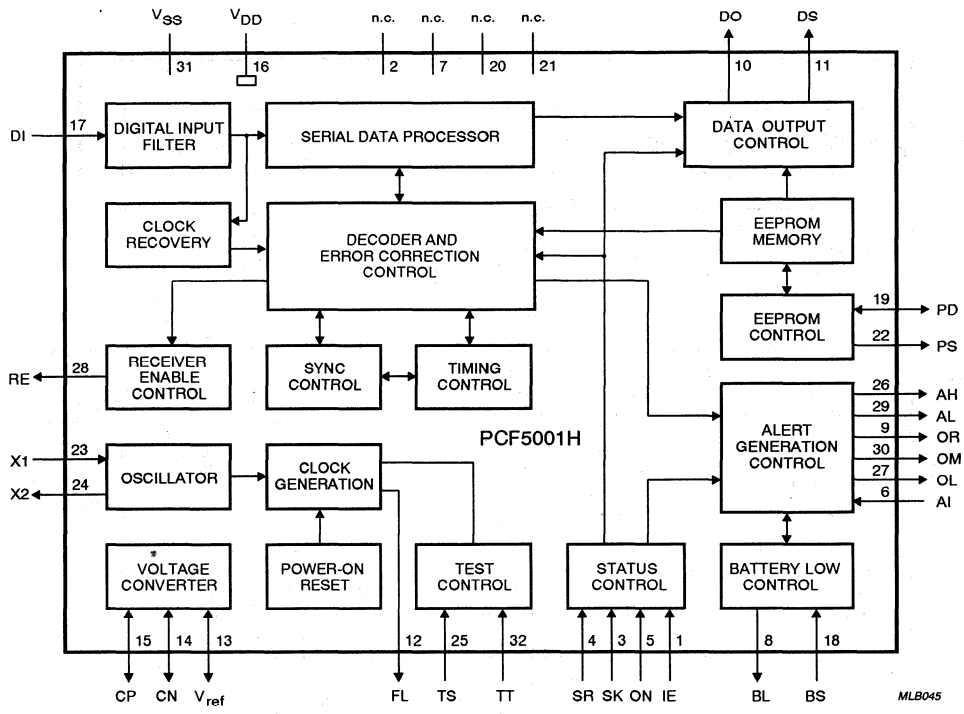


Fig.2 Block diagram (LQFP32; SOT358-1).

PINNING

SYMBOL	PIN		DESCRIPTION
	SO28 SOT136-1	LQFP32 SOT358-1	
V_{ref}	1	13	Microcontroller interface reference voltage output. The LOW level of pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE is related to the voltage on V_{ref}. May be driven from an external negative voltage source or must be connected to V_{SS}, if pins CN and CP are left open-circuit. When the on-chip voltage converter is used, this pin provides a negative output voltage.
CN	2	14	Voltage converter external shunt capacitance, negative side. Connect the negative side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
CP	3	15	Voltage converter external shunt capacitor, positive side. Connect the positive side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
V_{DD}	4	16	Main positive power supply. This pin is common to all supply voltages and is referred to as 0 V (common).
DI	5	17	Serial data input (POCSAG code). The serial data signal train applied to this pin is processed by the decoder. Pulled LOW by an on-chip pull-down when the receiver is disabled (RE = LOW).
BS	6	18	Battery-low indication input. The decoder samples this input during synchronization scan, when it is in ON or SILENT status and the receiver is enabled (RE = HIGH). A battery-low condition is assumed, if the decoder detects four consecutive samples HIGH. An audible battery-low indication is made by the decoder, when operating in ON status. Normally LOW by the operation of an on-chip pull-down.
PD	7	19	EEPROM programming data input and output. Normally HIGH by the operation of an on-chip pull-up. During programming of the on-chip EEPROM, PD is a bidirectional data and control signal.
PS	8	22	EEPROM programming strobe input. Normally LOW by the operation of an on-chip pull-down. During programming of the on-chip EEPROM, PS is a unidirectional control input.
X1	9	23	Crystal oscillator input. Connect a 32768 Hz or 76800 Hz crystal and a biasing resistor between this pin and X2. In addition, provide a load capacitance to V_{DD}, which may also be used for frequency tuning.
X2	10	24	Crystal oscillator output. Return connection for the external crystal and resistor at X1.
TS	11	25	Scan test mode enable input. Always LOW by operation of an on-chip pull-down.
AH	12	26	Alert HIGH-level output. This output can directly drive an external bipolar transistor to control HIGH-level alerting in conjunction with AL, by means of an alerter or beeper.
OL	13	27	LED indication output. This output can directly drive an external bipolar transistor to control the visual alert function by means of an LED. It may also be used for visual indication of received call data during call reception.

SYMBOL	PIN		DESCRIPTION
	SO28 SOT136-1	LQFP32 SOT358-1	
RE	14	28	Receiver enable output. May be used to control the paging receiver power control input, to minimize power consumption. The decoder provides a HIGH-level at this pin, when receiver operation is requested. Each time the decoder does not require any input data at DI the receiver enable output is LOW.
AL	15	29	Alert LOW-level output. Open drain alert output in anti-phase to AH, to provide LOW-level alerting. HIGH-level alerting is generated in conjunction with AH.
OM	16	30	Vibrator output. This output can directly drive an external bipolar transistor to control a vibrator type alerter.
V_{SS}	17	31	Main negative supply voltage.
TT	18	32	Test mode enable input. Always LOW by operation of an on-chip pull-down.
IE	19	1	Interface enable input. While the interface enable input is active HIGH, operation of the ON, SK, SR, AI, BL and OR inputs and outputs is possible. When IE is LOW the inputs do not respond to applied signals and the outputs are made high-impedance. In alert only pager mode the interface enable input does not have any effect on the operation of inputs ON, SK and SR, but IE must be referenced to LOW or HIGH.
SK	20	3	Silent state control input. The silent control input selects the decoder ON status (LOW-level) or SILENT status (HIGH-level), if the ON input is active HIGH. An on-chip pull-up is provided, if the decoder has been programmed for alert-only pager mode, whereby the pull-up is disabled for display pager mode. In display pager mode status change is possible provided the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
SR	21	4	Status request and reset input. A HIGH-going pulse on this input causes (a) status indication cadence to be generated, if the decoder is not alerting or (b) resetting of a call alert, repeated call alert or battery-low alert, if active or (c) triggers the call store re-alert facility, if repeat mode is active. In display pager mode operation of SR is possible only, if the interface control input is active. Normally LOW by the operation of an on-chip pull-down.
ON	22	5	On/off control input. The on/off control input selects the decoder ON status (HIGH-level) or OFF status (LOW-level). An on-chip pull-up resistor is provided, if the decoder has been programmed for alert-only pager mode, but the pull-up resistor is disabled for display pager mode. In display pager mode status change is possible provided the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
AI	23	6	Alarm input. A HIGH-level on this input causes generation of a continuous HIGH-level alert via AH and AL outputs, if the decoder operates in ON status or OFF status. In addition, the LED output is active independent from the decoder status, but in accordance with AI. Pulsing the input may be used to modulate the alert and LED indication. Normally LOW in alert-only pager mode by operation of an on-chip pull-down.

SYMBOL	PIN		DESCRIPTION
	SO28 SOT136-1	LQFP32 SOT358-1	
BL	24	8	Battery-low indication output. If the decoder encounters a battery-low condition a battery-low output latch is set HIGH. The battery-low output latch may be tested for a battery-low condition, whenever the interface enable input (IE) is active (HIGH), otherwise the battery-low output is made high-impedance. The battery-low output latch is reset only, by switching the decoder to OFF status.
OR	25	9	Out-of-range indication output. Whenever the decoder detects an out-of-range condition an out-of-range output latch is set HIGH after expiry of the programmed out-of-range hold-off time selected by means of special programming (SPF06 and SPF07) of the EEPROM. The out-of-range latch may be tested for an out-of-range condition, whenever the interface enable input (IE) is active (HIGH), otherwise the out-of-range output is made high-impedance. The out-of- range output is reset by detection of a valid data transmission or by switching the decoder to OFF status.
DO	26	10	Serial interface data output. During normal decoder operation, accepted calls and possibly subsequent message data are serially output via this pin in conjunction with the data strobe output (DS). This pin is also used to output the EEPROM contents upon special command, if the decoder is programmed for display pager.
DS	27	11	Serial interface data strobe output. Provides a clock signal for the received call data and EEPROM data appearing at the data output (DO). Each time this output is LOW the data at DO is valid. Additional start and stop conditions allow easy identification of data sequence start and end.
FL	28	12	Frequency reference output. When programmed for display pager mode, this output provides a clock reference with 16384 or 32768 Hz per second, selected by SPF32. See Chapter "Functional description".
n.c.	–	2, 7, 20, 21	Not connected.

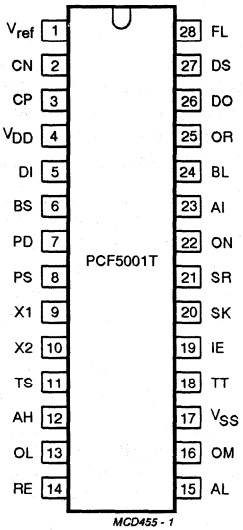


Fig.3 Pin configuration (SO28; SOT136-1).

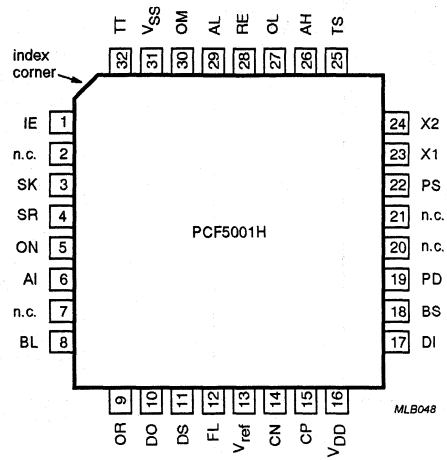


Fig.4 Pin configuration (LQFP32; SOT358-1).

FUNCTIONAL DESCRIPTION

The PCF5001 is a very low power Decoder and Pager Controller specifically designed for use in new generation radio pagers. The architecture of the PCF5001 allows for flexible application in a wide variety of radio pager designs.

The PCF5001 is fully compatible with *"CCIR radio paging Code Number 1"* (also known as the POCSAG code) operating at the originally specified 512 bits/s data rate, and also at the newly specified 1200 bits/s data rate (2400 bits/s operation is also possible). The PCF5001 also offers features which extend the basic flexibility and efficiency of this code standard.

The PCF5001 supports two basic modes of operation

In Alert-Only-Pager mode only a minimum number of external components are required to build a complete tone-only pager. Selection of operating states ON, OFF or SILENT is achieved using a slider switch interface.

In Display-Pager mode the state input logic is switched to a bus interface structure. Received calls and messages are transferred to an external microcontroller via the serial microcontroller interface. A built-in voltage converter with increased drive capabilities can supply doubled supply voltage output, and appropriate logic level shifting on microcontroller interface signals is provided.

Upon reception of valid calls one of eight different call cadences is generated; upon status interrogation status indication tones make the current status of the decoder available to the user.

On-chip non-volatile 114-bit EEPROM storage is provided to hold up to four user addresses, two frame numbers and the programmed decoder configuration.

Synchronization to the input data stream is achieved using the improved ACCESS algorithm, which allows for data synchronization and re-synchronization without preamble detection while minimizing battery power consumption by receiver power control. One of four error correction algorithms is applied to the received data to optimize the call success rate.

The POCSAG paging code

A transmission using the CCIR radio paging Code No.1 (POCSAG code) is constructed in accordance with the following rules (see Fig.5).

The transmission is started by sending a preamble, which is a sequence of at least 576 continually alternating bits (10101010...). The preamble precedes a number of batch blocks. The transmission is terminated after the last batch.

Each batch comprises a synchronization codeword with a fixed 32-bit pattern followed by eight frames (numbered 0 to 7). Only complete batches are transmitted.

A frame consists of two codewords, each 32-bits long. A codeword is either an address or a message or an idle codeword. Idle codewords are transmitted to fill empty batches or to separate messages.

An address codeword is coded as shown in Fig.5. The upper 18-bits of the 21-bit digital user address (or RIC = Receiver Identification Code) are coded in the codeword itself (bits 2 to 19), which is protected against transmission errors by a number of CRC check bits (bits 22 to 31). Bit 32 is a simple overall even-parity bit. The lower three bits of the digital user address are coded in the number of the frame, in which the address codeword is transmitted. Two function bits (bits 20 and 21) allow distinguishing of four different calls to one user address.

In a message codeword 20-bits of any display information can be put into the message bits, which are protected again by additional check bits.

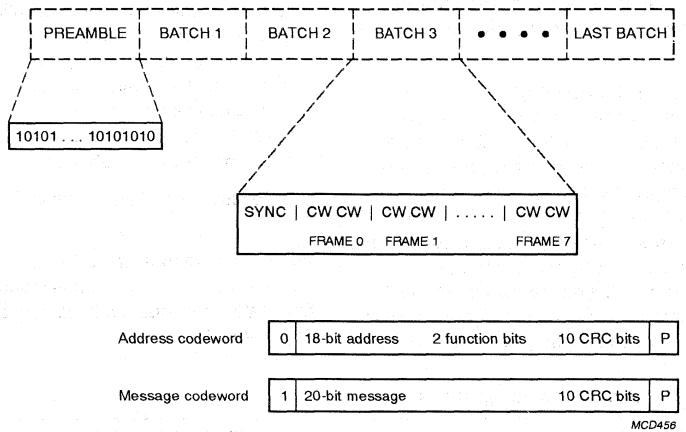


Fig.5 POCSAG code structure.

Modes and states of the decoder

The PCF5001 supports two basic operating modes:

- Alert-only pager
- Display pager mode.

Two further modes, the Programming mode and the Test mode, are implemented to program and verify the EEPROM contents and to support pager production and approval tests, respectively.

In Alert-only pager mode no external microcontroller is required, see Fig.21. A three position slider switch interface is provided to select the internal state of the decoder. The decoder performs regular scanning of the switch inputs to detect a status change. A push-button interface is provided on the SR input, which is used as input for user acknowledgment actions and status interrogation. Upon reception of valid calls, tone alert cadences are generated. A call storage is provided to store calls received while operating in Silent status and to recall cadences upon repeat mode operation. The voltage doubler and the frequency reference output are disabled in this mode.

In Display pager mode the PCF5001 operates as decoder and pager controller in combination with an external microcontroller, see Fig.22. The internal states of the decoder are determined by appropriate logic levels on the status inputs. A bus type interface structure is used to interface the decoder to the microcontroller. The decoder's on-chip voltage converter provides doubled supply voltage output to provide a higher supply voltage to the microcontroller and any additional hardware. The logic levels of the interface's input and output signals are level shifted to allow for direct coupling between microcontroller and the decoder. Upon detection of a valid call, address and message information are transferred to the external microcontroller using the serial microcontroller interface. In addition, appropriate call alert cadences are generated.

If the decoder is in one of the two operating modes, it is always in one of the following three internal states:

- OFF status. This is the power saving, inactive status of the PCF5001. The paging receiver is disabled, no decoding of input data takes place. However, the crystal oscillator is kept running to ensure that scanning of the status inputs/status switch is maintained to allow changing into one of the following two active states.
- ON status. This is the normal active status of the decoder. Incoming calls are compared with the user addresses stored in the internal EEPROM. Upon detection of valid calls, alert cadences and LED indication are generated and data is shifted out at the serial microcontroller interface.
- SILENT status. The Silent status is the same as the On status with the exception that valid calls no longer cause generation of call alert cadences. Instead, if programmed as alert-only pager, the decoder stores up to eight different calls and generates appropriate alert cadences after the decoder has been put back into the On status. However, special silent override calls will cause generation of alert cadences, if enabled.

The decoder operating status is selected as indicated in Table 1.

When programmed for alert-only pager a switch debounce period is applied to the status inputs. For status change and status interrogation in display pager mode, see Figs 6 and 7.

Table 1 Truth table for decoder operating status

ON INPUT	SK INPUT	OPERATING STATUS
0	0	OFF
0	1	OFF (EEPROM transfer mode; note 1)
1	0	ON
1	1	SILENT

Note

1. The EEPROM transfer mode applies to display pager mode only.

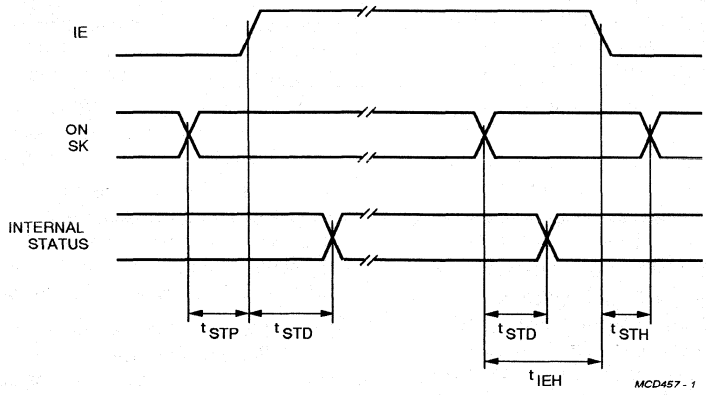


Fig.6 Status change in display pager mode.

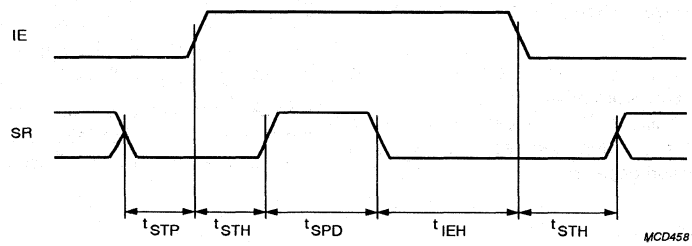


Fig.7 Status interrogation in display pager mode.

Decoding of the POCSAG data stream

The POCSAG coded input data stream is first noise filtered by a digital filter. From the filtered data a sampling clock synchronous to the data rate is derived. The PCF5001 supports 512 bits/s and 1200 bits/s data rates. This results in a 512 Hz or 1200 Hz sampling clock frequency, respectively. Synchronization on the POCSAG code structure is performed using the improved Philips ACCESS algorithm, which employs a state machine with six internal states.

A data rate of 2400 bits/s is possible if an external clock generator of 153.6 kHz is connected to X1. The minimum supply voltage is then −1.8 V.

The receiver enable output is activated a period equal to t_{RXON} before the input data is actually needed. The decoder has first to achieve bit and word synchronization before it can receive calls. The algorithm searches first for the preamble and then for synchronization codeword patterns. This is carried out for the duration of 3 batches in Power-on mode or 1 batch (=preamble duration) in

Preamble Receive mode. Error correction algorithms are applied to the data before it is compared with preamble and synchronization codeword patterns. The synchronization process is terminated and thus Data Receive mode entered as soon as synchronization codewords are seen at the beginning of each batch.

The decoder handles loss of synchronization in three steps:

1. If the decoder fails to detect the synchronization pattern at the beginning of the current batch it continues data reception as normal. This Data Fail mode is signalled in the message output when an address codeword was received, as shown in Table 4.
2. If also at the beginning of the next batch no synchronization codeword can be detected, the algorithm assumes a small bit shift in the Fade Recovery mode and performs more synchronization codeword checks around the expected position for the following 15 batches. Call reception is suspended.
3. If it fails to re-synchronize in the Fade Recovery mode, the Carrier Off mode is selected, in which the decoder attempts to regain synchronization by bit-wise shifting its synchronization scan window. Using this technique re-synchronization is obtained within a continuous data stream of at least 18 batches without preamble detection.

In Data Receive mode, the input data stream is sampled at the synchronization codeword position and the programmed frame positions. The received codewords are error corrected and then, if address codewords, compared with the stored user addresses related to that frame.

On detection of a valid call, the decoder performs the following three operations:

1. Set a store for call alert cadence generation according to the combination of the function bits in the accepted address codeword. The call alert cadence will not be generated before the call has been terminated.
2. Keep the receiver enable output (RE) active and receive subsequent message codewords, until any of the call termination criteria are fulfilled.
3. Trigger the serial message transfer by sending a start condition and transfer deformatted message codewords as attached to the address codeword via the serial microcontroller interface to an external microcontroller, followed by a stop condition.

Normally call termination is assumed, when a valid idle or address codeword is received. On reception of uncorrectable codewords, call termination takes place in accordance with conditions shown in Table 2.

Generation of output signals

The PCF5001 provides output indications for call alert, repeat mode alert, out of range alert, battery-low alert, status indication alert and start-up alert. Some of the alert functions may be freely configured by programming of SPF bits within the EEPROM. Table 3shows the outputs which are used for special output indications, if the decoder operates in ON status.

Remark: reception of special silent override calls causes the decoder to generate call alert indication via AL and AH even if it operates in SILENT status.

Table 2 Call termination on error

SPF12	SPF13	CALL TERMINATION EVENT
0	X[1]	Any two consecutive codewords or the codeword directly following the address codeword uncorrectable.
1	0	Any single codeword uncorrectable.
1	1	Any two consecutive codewords uncorrectable.

Note

1. X = don't care.

Table 3 Output signals

ALERT FUNCTION	OUTPUT ACTIVE[1]					
	AL	AH	OL	OM	OR	BL
Start-up	(yes)	–	yes	yes	–	–
Status indication	yes	–	–	–	–	–
Call reception	(yes)	(yes)	yes	SPF11	–	–
Repeat mode	(SPF16)	(SPF16)	SPF16	–	–	–
Out-of-range	–	–	SPF15	–	yes	–
Battery-low	(yes)	(yes)	–	–	–	yes
Alarm input	(yes)	(yes)	yes	–	–	–

Note

1. Entries in parenthesis are not valid, if the decoder operates in SILENT status.

Alerter

The PCF5001 provides the AL and AH outputs for acoustical LOW-level and HIGH-level signalling. LOW-level alerting is provided by the AL output only. For HIGH-level alerting both, AL and AH are active in anti-phase. The square-wave output signals produce tone alert cadences by means of a magnetic or piezo ceramic beeper. The alert frequency, 2048 Hz or 2731 Hz square-wave, is selected by programming of SPF31.

When valid calls are received while operating in ON status, the PCF5001 generates call alert cadences. The first four seconds are generated at LOW-level, a further twelve seconds are generated at HIGH-level. Alert tone generation and LED indication automatically terminate after sixteen seconds unless terminated by pulsing the status request and reset input (SR). Call alert generation is inhibited until completion of message codeword reception and the termination word is sent by the decoder. Call alert generation commences after an alert delay period, t_{ALD}, at the earliest, see Fig.8. Call alert deletion is possible during the alert delay period.

The call alert cadence is modulated according to the two function bits (FC) in the received address codeword, see Fig.9.

Valid calls received on RIC B or RIC D cause the alerter frequency to be warbled by means of an additional 16 Hz and 1024 Hz signal (respective 1365 Hz for SPF31 = 1) as opposed to RIC A and RIC C where no alert frequency warble takes place. Thus, eight different call cadences are distinguishable.

On status interrogation by the status request and reset input (SR) the PCF5001 generates a status cadence at LOW-level, in accordance with the present internal decoder status (see Fig.10).

When detecting a battery-low condition the PCF5001 provides a battery-low indication. Operating in ON status causes generation of a battery-low alert at HIGH-level for sixteen seconds or until terminated by pulsing SR. Operating in SILENT status or repeat mode the battery-low alert is stored and inhibited until switching to ON status.

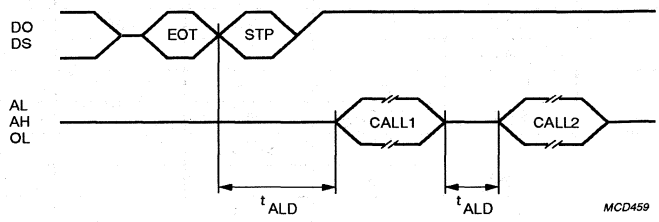


Fig.8 Call alert delay.

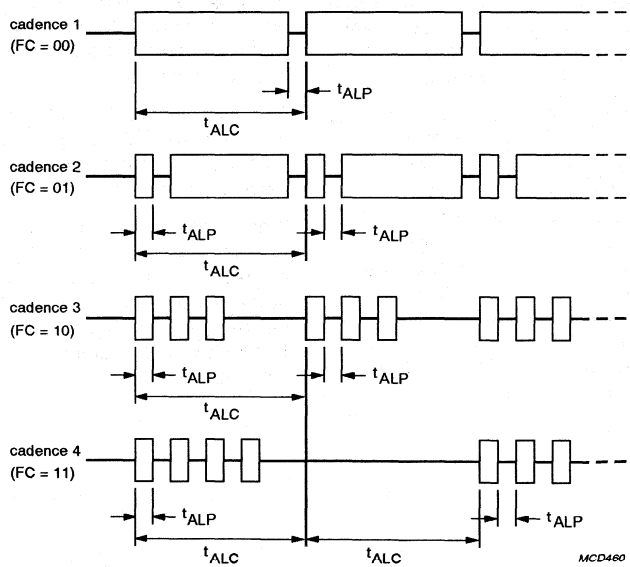


Fig.9 Call alert cadences.

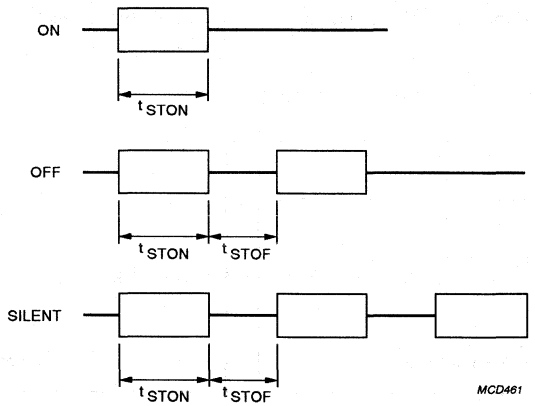


Fig.10 Status indication cadences.

Silent call storage and Repeat mode

When programmed for alert only pager the PCF5001 provides a call alert storage for storing of call alerts received during SILENT status or for call alerts which caused the decoder to enter Repeat mode. Call alert is not stored, when call indication is terminated by action of the status request and reset input (SR).

Allowing the call indication to time-out by expiration of a sixteen second alert operation causes the Repeat mode to be entered, while operating in ON status or SILENT status. Such call alerts are stored for later repeated call alert on interrogation by the user. When Repeat mode has been entered and the decoder operates in ON status, the repeat call store is interrogated by pulsing the status request and reset input (SR) or on switching to ON status if the decoder operates in SILENT status. When silent override calls are received, which entered the Repeat mode, interrogation of repeat call store operates as in decoder ON status. After interrogation of repeat call store and subsequent generation of all stored call alerts the call store is cleared and the Repeat mode is terminated.

When programmed by means of SPF16, a repeat alert cadence is generated periodically, whenever Repeat mode has been entered. Operating in ON status causes the repeat alert cadence to be generated at HIGH-level and warbled by means of an additional 16 Hz and 1024 Hz signal (respective 1365 Hz for SPF31 = 1) as shown in Fig.11. The LED output indicates the same alert cadence and alert warble. In SILENT status only the LED output is active.

No call alert storage occurs when the decoder is programmed for display pager mode.

Duplicate Call Suppression

The PCF5001 provides a Duplicate Call Suppression with time-out facility, to identify duplicate call reception. When selected by programming of SPF14, the PCF5001 inhibits any duplicate call alert in alert-only pager mode. In display pager mode, duplicate call indication is achieved only via the serial microcontroller interface. A call is assumed to be duplicate if its address and function bit setting is equal to the latest received call, which initialized the call address and function bit reference. The Duplicate Call Suppression time-out is selectable by programming of SPF06 and SPF07.

LED indicator

The PCF5001 provides for visual signalling using a LED via output OL.

Call alert indication is provided by the LED with the same cadence and warble modulation as for the alerter outputs AL and AH. Call alert indication occurs in ON and SILENT status and automatically terminates after sixteen seconds time-out unless terminated by pulsing the status request and reset input (SR).

When detecting an out-of-range condition and enabled by programming of SPF15, the LED output provides an out-of-range indication as shown in Fig.12.

The LED output can be made to provide message data by programming SPF17. Alert signals are inhibited during message data transfer.

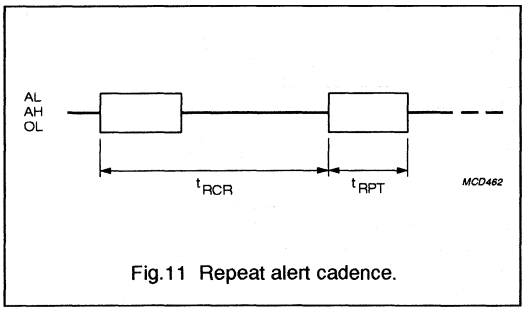


Fig.11 Repeat alert cadence.

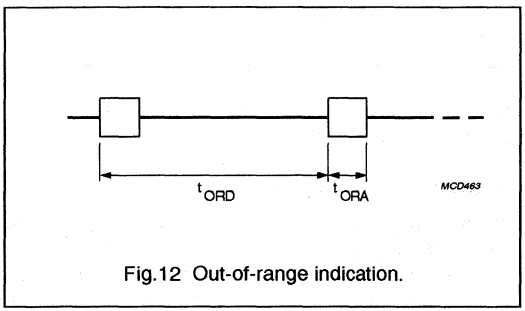


Fig.12 Out-of-range indication.

Vibrator output

The PCF5001 provides the OM output for activating a vibrator-type alerter for call alert indication. The vibrator output is enabled by programming of SPF11.

Calls received while operating in SILENT status cause activation of the vibrator output for the normal call alert cadence or until terminated by operation of the status request and reset input (SR). Silent override calls, calls received in decoder ON status and repeated call alerts are alerted normally by the AL and AH outputs.

Start-up alert

To indicate the establishment of operational condition whenever the decoder status has been changed from OFF to ON or SILENT status, the PCF5001 provides a start-up alert indication. Switching from OFF to ON status causes generation of a start-up alert cadence at LOW-level and on the LED output OL (see Fig.13).

When changing from OFF to SILENT status, the start-up alert will be indicated on the LED output and the vibrator output OM.

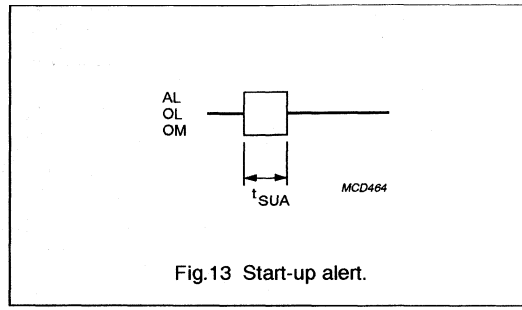


Fig.13 Start-up alert.

Serial communication interface

To transmit any call message data received to an external microcontroller for post-processing, a serial communication interface has been provided by a serial data output signal DO and a data strobe signal DS as shown in Fig.14.

Upon interrogation the PCF5001 is also able to transfer EEPROM contents via the serial communication interface, see Section "Read-back operation via Microcontroller Interface".

Message data transfer

The transfer of message data via DO and DS is organized in 8-bit words providing additional start and stop conditions as shown in Fig.15.

On reception of a valid call address the PCF5001 generates a start condition and outputs an address word as shown in Fig.15a.

The address word indicates call address, function bit setting and decoder flags as shown in Table 4.

Message codewords received and concatenated to a valid call address are transferred after completion of the address word. The message bits received in the message codewords are split into blocks and are converted to obtain the message words. The message words comprise an error flag to indicate message words, which are derived from uncorrectable message codewords as shown in Table 5.

Message data is output at a rate of 2048 bits/s with a minimum delay of 2 bits between consecutive message words.

Termination of call reception causes a termination word to be transferred, which indicates successful or unsuccessful call termination as shown in Table 6.

Serial data transfer for a received call ends with a stop condition as shown in Fig.15c.

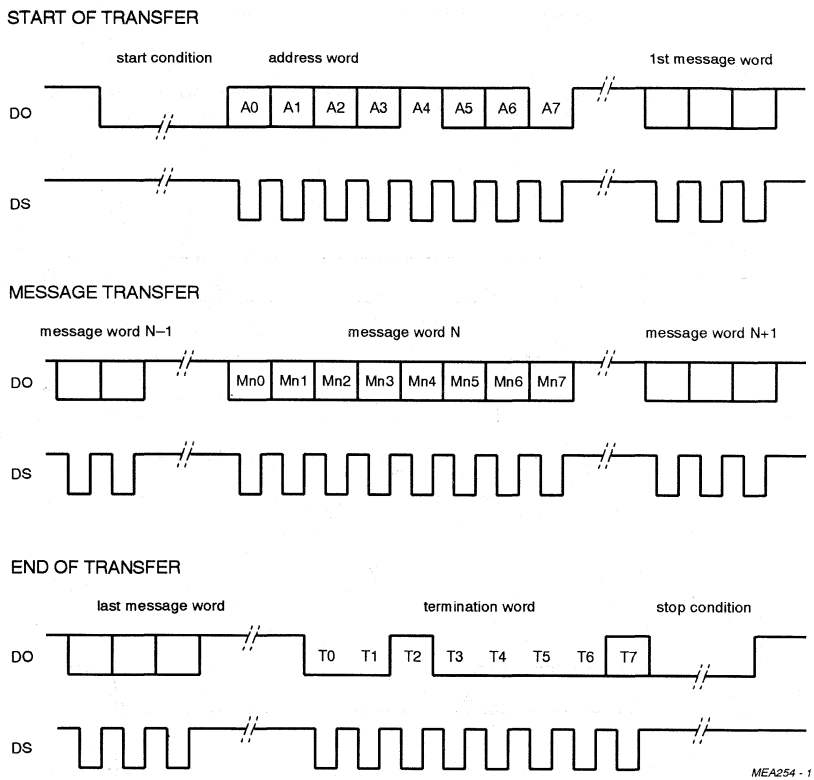
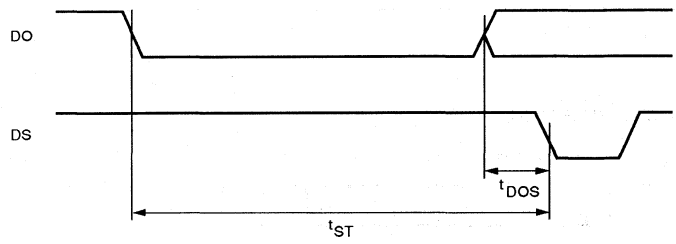
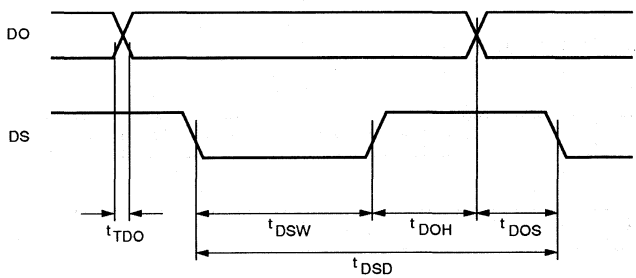


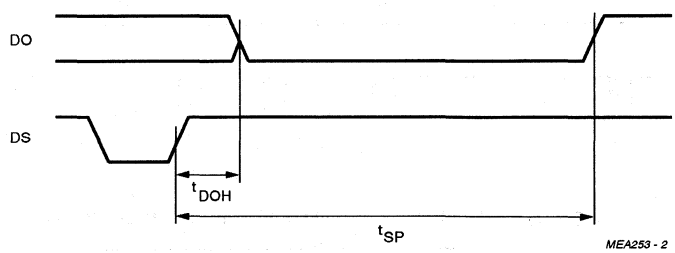
Fig.14 Call data transfer on the serial communication interface.



a.



b.



c.

a. Start condition.
b. Data bit.
c. Stop condition.

Fig.15 Serial communication interface timing.

Call Data output on LED

When enabled by programming of SPF17 = 1, message data will appear on the LED output OL. The data format and timing are equal to the signal on DO, except that the start/stop conditions are replaced with start/stop bits (respectively 1 and 0). The data format is shown in Fig.16. No alert signals will appear on OL during message data transfer. Consecutive message words have a minimum separation of 1 start bit and 1 stop bit.

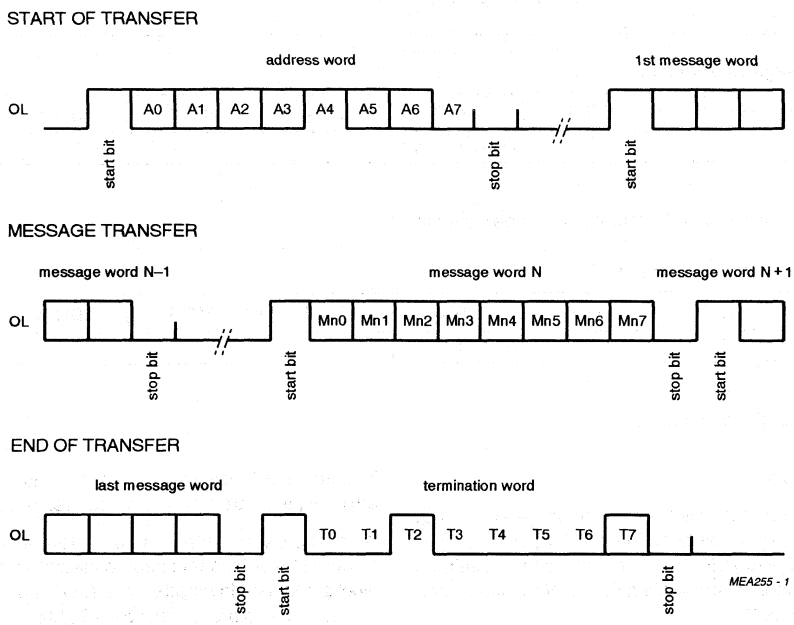


Fig.16 Call data transfer on the LED output.

Serial communication call data format

Table 4 Address word format

FUNCTION CODE		CALL ADDRESS			BIT 4	SYNC STATUS	DUPLEX CALL	BIT 7
BIT 0 (LSB)	BIT 1 (MSB)	BIT 2	BIT 3	RIC		BIT 5	BIT 6	
Bit 21 of address codeword	bit 20 of address codeword	0	0	A	1	0 = Data Receive; 1 = Data fail	1 = Duplex Call time-out active	0
		0	1	B				
		1	0	C				
		1	1	D				

Table 5 Message word format

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7[1]
LSB			message bits			MSB	error flag

Note

1. Bit 7 = 1, if message codeword could not be corrected.

Table 6 Termination word format

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7[1]
0	0	1	0	0	0	0	error flag

Note

1. Bit 7 = 1, if call termination on error.

Data conversion

The PCF5001 automatically converts message codewords received in numeric or alphanumeric format into ASCII format. Depending on SPF13 and the function bit setting in the received address codeword a conversion takes place as shown in Table 7.

When a conversion from alphanumeric format to ASCII takes place, the received message codewords are split into message blocks, seven bits in length. After adding the error flag they are transferred as message words.

When a conversion from numeric format to ASCII takes place, the received message codewords are split into blocks, four bits in length. Each four bit block is converted to a seven bit block as shown in Table 8. After adding the error flag they are transferred as message words.

Table 7 Message data conversion

SPF13	FUNCTION BITS		MESSAGE FORMAT
	BIT 20 (MSB)	BIT 21 (LSB)	
0	X[1]	X[1]	numeric
1	0	0	numeric
1	X[1]	1	alphanumeric
1	1	X[1]	alphanumeric

Note

1. X = don't care.

Table 8 Numeric format to ASCII conversion

4-BIT BLOCK				CHARACTER	7-BIT BLOCK						
LSB			MSB		LSB						MSB
0	0	0	0	'0'	0	0	0	0	1	1	0
1	0	0	0	'1'	1	0	0	0	1	1	0
0	1	0	0	'2'	0	1	0	0	1	1	0
1	1	0	0	'3'	1	1	0	0	1	1	0
0	0	1	0	'4'	0	0	1	0	1	1	0
1	0	1	0	'5'	1	0	1	0	1	1	0
0	1	1	0	'6'	0	1	1	0	1	1	0
1	1	1	0	'7'	1	1	1	0	1	1	0
0	0	0	1	'8'	0	0	0	1	1	1	0
1	0	0	1	'9'	1	0	0	1	1	1	0
0	1	0	1	'*'	0	1	0	1	0	1	0
1	1	0	1	'U'	1	0	1	0	1	0	1
0	0	1	1	' '	0	0	0	0	0	1	0
1	0	1	1	'–'	1	0	1	1	0	1	0
0	1	1	1	']'	1	0	1	1	1	0	1
1	1	1	1	'['	1	1	0	1	1	0	0

Memory Organization

The PCF5001 POCSAG decoder contains non-volatile EEPROM memory to store four user addresses, two frame numbers and specially programmed function bits (SPF01 to SPF32) for decoder application configuration. The EEPROM is organized as three arrays of 38 bits each as shown in Fig.17.

A user address (or RIC) in POCSAG code comprises of 21 bits, but the three least significant bits are coded in the frame number and therefore not explicitly transmitted. In the PCF5001, addresses A/B and C/D must share the same frame number: addresses A and B reside in frame FR1 (FR10, FR11 and FR12), addresses C and D reside in frame FR2 (FR20, FR21 and FR22). Figure 18 shows an example of decimal address to EEPROM content conversion. Each address must be explicitly enabled by resetting of the associated enable bit.

EEPROM ARRAY 1

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	$\overline{ENA}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
B17	B16	B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00	$\overline{ENB}$

EEPROM ARRAY 2

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
C17	C16	C15	C14	C13	C12	C11	C10	C09	C08	C07	C06	C05	C04	C03	C02	C01	C00	$\overline{ENC}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
D17	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	$\overline{END}$

EEPROM ARRAY 3

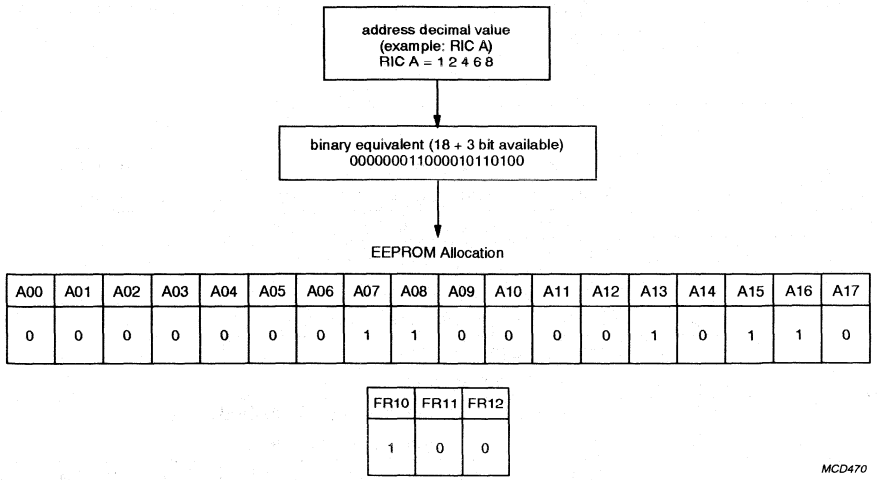
BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SPF13	SPF12	SPF11	SPF10	SPF09	SPF08	SPF07	SPF06	SPF05	SPF04	SPF03	SPF02	SPF01	FR20	FR21	FR22	FR10	FR11	FR12

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
SPF32	SPF31	SPF30	SPF29	SPF28	SPF27	SPF26	SPF25	SPF24	SPF23	SPF22	SPF21	SPF20	SPF19	SPF18	SPF17	SPF16	SPF15	SPF14

MCD469

A00 represents the MSB of RIC A, B00 is the MSB of RIC C, etc.
FR10 represents the MSB of Frame 1 (valid for RICs A and B), FR20 is the MSB of Frame 2 (RICs C and D).

Fig.17 EEPROM memory organization.



A00 is the MSB of RIC A, FR10 is the MSB of Frame 1.

Fig.18 Decimal address to memory contents conversion example.

Description of the Special Programmed Function (SPF) bits

The following features can be selected by appropriate programming of the special programmed function bits as shown in Table 9.

Table 9 Special Programmed Function (SPF) bits

SPF	BIT	FUNCTION
SPF01	0	Alert-only mode.
	1	Display pager mode.
SPF02	0	512 bits/s data rate.
	1	1200 bits/s data rate, possible with 76.8 kHz crystal only.
SPF03	0	32768 Hz crystal configuration.
	1	76800 Hz crystal configuration.
SPF04, SPF05		Receiver establishment time (depending on data rate).
	00	7.8 ms/512 bits/s; 53.3 ms/1200 bits/s.
	01	15.6 ms/512 bits/s; 6.7 ms/1200 bits/s.
	10	31.3 ms/512 bits/s; 13.3 ms/1200 bits/s.
	11	62.5 ms/512 bits/s; 26.7 ms/1200 bits/s.

SPF	BIT	FUNCTION
SPF06, SPF07		Duplicate call suppression time-out and out-of-range hold-off time-out.
	00	30 s.
	01	60 s.
	10	120 s.
	11	240 s.
SPF08	0	Voltage converter disabled, if SPF01 = 1 (Display pager mode).
	1	Voltage converter enabled, if SPF01 = 1 (Display pager mode).
SPF09	0	Silent override on address C disabled.
	1	Silent override on address C enabled.
SPF10	0	Silent override on address D disabled.
	1	Silent override on address D enabled.
SPF11	0	Vibrator output disabled.
	1	Vibrator output enabled.
SPF12	0	Call termination criteria combination method (note 1).
	1	Call termination criteria defined by SPF13.
SPF13	0	Numeric data deformatting, call termination on first uncorrectable codeword.
	1	Numeric data deformatting on function code 00 only, call termination on two uncorrectable codewords.
SPF14	0	Duplicate call suppression disabled.
	1	Duplicate call suppression enabled.
SPF15	0	Out of range indication at OL output disabled, hold-off period is zero regardless of SPF06 and SPF07 setting.
	1	Out of range indication at OL output enabled, hold-off period is according to SPF06 and SPF07 setting.
SPF16	0	Repeat alert disabled.
	1	Repeat alert enabled.
SPF17	0	Call data output on OL disabled.
	1	Call data output on OL enabled.
SPF18	–	Spare.
SPF19	–	Program always 0.
SPF20 to SPF30	–	Spares.
SPF31	0	Alerter frequency 2048 Hz.
	1	Alerter frequency 2731 Hz.
SPF32	0	Frequency reference output 16384 Hz if SPF01 = 1 (Display pager mode).
	1	Frequency reference output 32768 Hz if SPF01 = 1 (Display pager mode).

Note

1. Call termination on:
   a) First codeword immediately following address codeword uncorrectable.
   b) Two consecutive codewords uncorrectable.

EEPROM Write operation

The program mode is entered in OFF status by setting the PD input LOW and the PS input HIGH at any time. The program mode is left and normal operation resumed by either removing the power supply or setting the PD input HIGH after the 38th data bit while continuing to clock the PS input. The three EEPROM arrays can be programmed in any order. Selection of array is made during the second and third pulse on the PS input. The program mode has to be left after programming of each array.

After entering the program mode, keeping input PD LOW during the first pulse on PS selects Memory Write operation. After selection of the current array an erase cycle of duration t_{PEW} has to be carried out, during which the supply voltage at V_{SS} input must be at least V_{PG}. Program data for the selected array is entered bit by bit using PD as data input and the rising edge on PS as data strobe pulse. See Fig.19 for timing during an EEPROM write operation.

After the last bit a special write cycle of duration t_{PEW} has to be carried out again, during which the supply voltage at V_{SS} input must be V_{PG}. During conditions when the supply voltage is increased to V_{PG} the maximum DC ratings at V_{ref} must not be exceeded. When the on-chip voltage converter is enabled a voltage regulator diode or a damping resistor of sufficiently low impedance has to be connected between V_{ref} and V_{SS} to limit the voltage level at V_{ref} during program operation.

EEPROM Read operation

After entrance to the program mode, keeping input PD HIGH during the first pulse on PS selects Memory Read operation. After selection of the current array the programmed data is output bit-by-bit using PD as data output. A positive edge on PS input switches to the next bit. See Fig.19 for timing during an EEPROM read operation.

Read-back operation via Microcontroller Interface

In display pager mode, the PCF5001 is capable of delivering the EEPROM contents to an external microcontroller using the serial interface outputs DO and DS. The EEPROM data transfer mode is selected by applying a LOW to input ON and a HIGH to input SK while pulsing the SR input, and the interface is enabled (IE is HIGH). The data transfer is started by a logic HIGH level on SR. The HIGH level on SR must be removed before the end of the tenth output byte, otherwise the transfer is aborted and restarted. The minimum pulse duration corresponds with t_{SPD} in the status interrogation timing (see Fig.7). The transfer is organized as 15-byte transfers. The contents of each array are extended to 40 bits by trailing zeros. The EEPROM data transfer starts with array 1, bit 0. A valid data bit at DO is indicated by a LOW-level on DS as shown in Fig.20.

During EEPROM Read-back operation, the PCF5001 configuration and the outputs FL, OL are undefined. After completion of the Read-Back operation, the PCF5001 will re-enter the programmed configuration.

Voltage converter

The PCF5001 contains a switched capacitor-type on-chip voltage converter, which can provide doubled supply voltage to the external microcontroller and display control devices. The microcontroller interface signals are level shifted accordingly.

A capacitor of 100 nF (C_S) must be connected between pins CP and CN while a load capacitor of 10 µF is connected to V_{ref} as shown in Fig.22. The voltage converter operates in display pager mode only, when enabled by programming SPF08 (see Table 9).

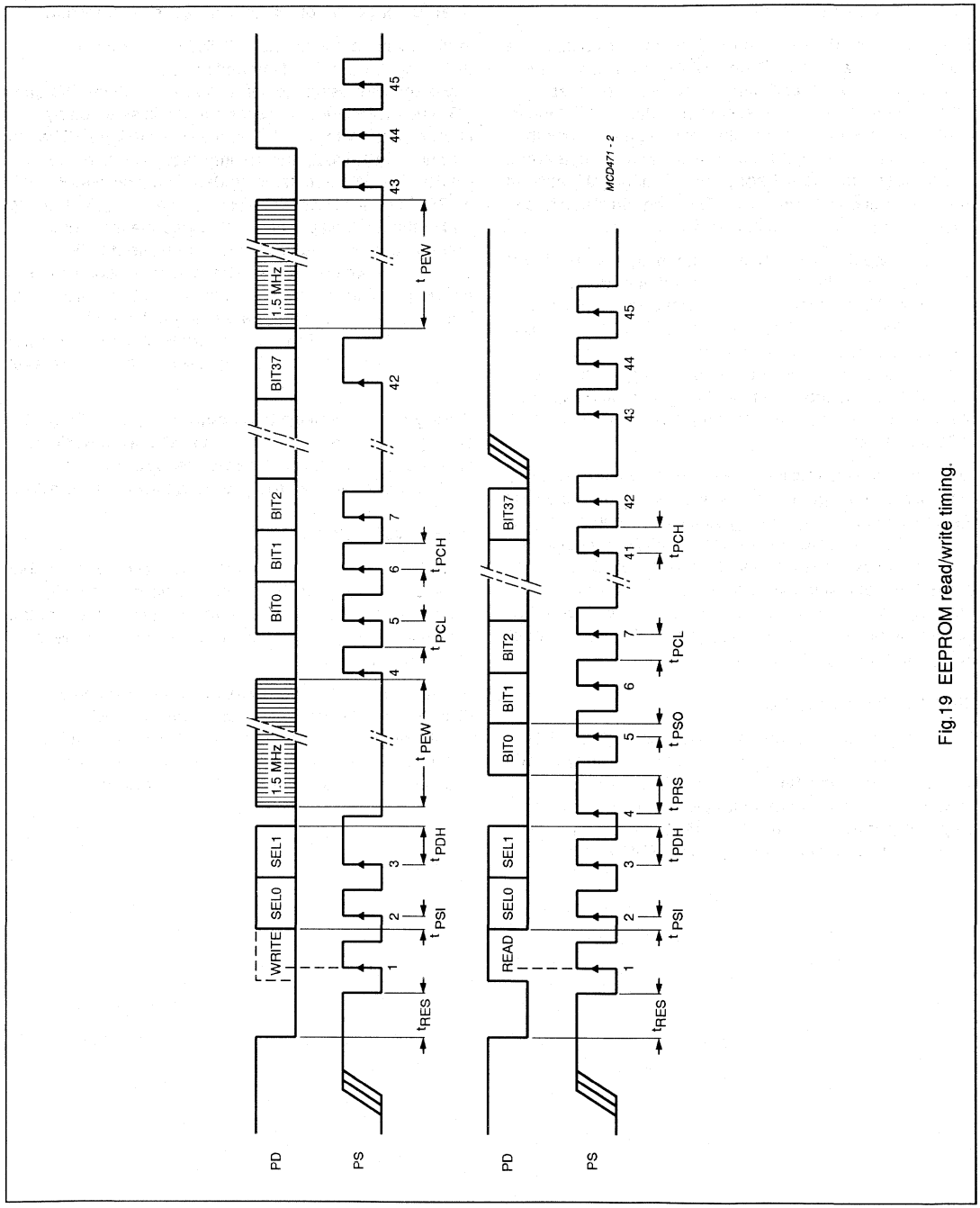


Fig.19 EEPROM read/write timing.

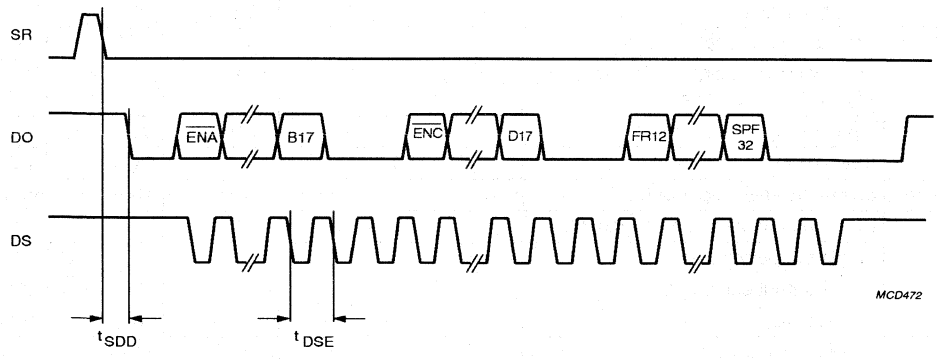


Fig.20 EEPROM data transfer to microcontroller timing.

Test modes of the decoder

The decoder supports two test modes, which are intended for use during pager production and type approval tests.

BOARD TEST MODE

Board test mode is selected by setting the PD input LOW at any time. In this test mode the following features are provided:

1. Receiver enable output is set constantly HIGH.
2. Output AL is activated by a LOW-level on ON input.
3. Output AH is activated by a HIGH-level on SR input.
4. Outputs OL and OM are activated by a HIGH-level on SK input.

Exit from board test mode is achieved by setting input PD HIGH.

PAGER TEST MODE (TYPE APPROVAL MODE)

Pager test mode is entered by reception of a valid call while board test mode is active, see above. In pager test mode:

1. Call alert cadences are terminated after 2 seconds.
2. Duplicate call suppression is disabled.

Exit from pager test mode is achieved by disconnecting the power supply from the decoder.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SS}	supply voltage	note 1	+0.5	−8.0	V
V_{PG}	programming supply voltage		−5.5	−	V
V_I	input voltage on pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE		+0.8	V_{ref} − 0.8	V
V_I	input voltage on any other pin		+0.8	V_{SS} − 0.8	V
P_{tot}	total power dissipation		−	250	mW
P_O	power dissipation per output		−	100	mW
I_I	maximum input current (any input)		−	10	mA
$I_{O(max)}$	maximum output current				
	any output except AL		−	20	mA
	output AL		−	70	mA
T_{stg}	storage temperature		−55	+125	°C
T_{amb}	operating ambient temperature		−40	+85	°C

Note

1. Input V_{DD} is referred to as common, 0 V.

DC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; V_{ref} = 2.7 V; T_{amb} = 25 °C; unless otherwise specified.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Alert-only (SPF01 = 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	supply voltage	all outputs open-circuit				
		T_{amb} = −10 to +85 °C	−1.5	−2.7	−6.0	V
		T_{amb} = −40 to +85 °C	−1.8	−2.7	−6.0	V
I_{SS}	supply current	note 1	−	−60	−100	μA
V_{PG}	programming supply voltage	note 2	−4.5	−5.0	−5.5	V
I_{PG}	programming supply current		−	−500	−	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
V_{IL1}	LOW level input voltage PD, PS, DI, BS, TS, TT and X1		$0.7V_{SS}$	–	–	V
V_{IL2}	LOW level input voltage AI, ON, SR, SK and IE		$0.7V_{ref}$	–	–	V
V_{IH1}	HIGH level input voltage PD, PS, DI, BS, TS, TT and X1		–	–	$0.3V_{SS}$	V
V_{IH2}	HIGH level input voltage AI, ON, SR, SK and IE		–	–	$0.3V_{ref}$	V
I_I	input current					
	BS, PS, TS and TT	$V_I = V_{DD}$	7.0	–	20.0	µA
	PD	$V_I = V_{SS}$	–9.0	–	–24.0	µA
	DI	$V_I = V_{DD}$; RE = 0	7.0	–	20.0	µA
	DI	$V_I = V_{DD}$; RE = 1	0	–	0.5	µA
	ON and SK	$V_I = V_{SS}$	–0.5	–0.8	–1.1	µA
	AI and SR	$V_I = V_{DD}$	7.0	–	20.0	µA
C_I	input capacitance BS, DI, PD, PS, TS, TT, AI, ON, SR, SK, IE and X1		2	–	–	pF
Outputs						
I_{OL}	LOW level output current					
	OL, OM and AH	V_{OL} = –1.35 V	100	–	–	µA
	DO, DS, BL, FL and OR	V_{OL} = –1.35 V	100	–	–	µA
	AL	V_{OL} = –1.5 V	17.5	–	–	mA
	RE	V_{OL} = 2.2 V	200	–	–	µA
I_{OH}	HIGH level output current					
	OL, OM and AH	V_{OH} = –1.35 V	–0.8	–	–1.8	mA
	DO, DS, BL, FL and OR	V_{OH} = –1.35 V	–100	–	–	µA
	AL	AL high-impedance	–	–	–0.2	µA
	RE	V_{OH} = –0.5 V	–1.0	–	–	mA
Oscillator						
C_{XO}	output capacitance X2		–	40	–	pF
g_m	oscillator transconductance	V_{SS} = –1.5 V	15	29	43	µS
		V_{SS} = –6.0 V	25	39	55	µS
V_{PU}	power-up reset threshold voltage		–	–1.2	–	V

Notes

1. All inputs = V_{SS}; voltage converter off; all outputs open-circuit.
2. See Section "EEPROM Write operation"and Chapter "Limiting values"for limitations of V_{ref} when programming while the voltage converter is enabled.

DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 0 V; V_{SS} = −3.0 V; V_{ref} = −6.0 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display Pager (SPF01 = 1).
Voltage converter enabled (SPF08 = 1); C_s = 100 nF.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	supply voltage		−1.5	−	−3.0	V
Voltage converter						
V_{ref0}	output voltage; no load	V_{SS} = −3.0 V	−5.8	−	−6.0	V
V_{ref}	output voltage	V_{SS} = −2.0 V; I_{ref} = 250 μA	−3.0	−3.5	−	V
I_{ref}	output current	V_{SS} = −2.0 V; V_{ref} = −2.7 V	400	600	−	μA
		V_{SS} = −3.0 V; V_{ref} = −4.5 V	600	900	−	μA
Inputs						
I_I	input current					
	AI, ON, SR and SK	V_I = V_{ref}	−	0	−0.5	μA
	ON and SK	V_I = V_{DD}	−	0	±0.5	μA
	SR	V_I = V_{DD}; V_{ref} = −6.0 V	−	17	−	μA

AC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only Pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Alert frequency						
f_{AL}	alert frequency	SPF31 = 0	−	2048	−	Hz
f_{AWH}	high alert warble frequency		−	1024	−	Hz
f_{AWL}	low alert warble frequency		−	16	−	Hz
f_{AL}	alert frequency	SPF31 = 1	−	2731	−	Hz
f_{AWH}	high alert warble frequency		−	1365	−	Hz
f_{AWL}	low alert warble frequency		−	16	−	Hz
f_{FL}	frequency reference FL	SPF32 = 0	−	16384	−	Hz
		SPF32 = 1	−	32768	−	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Call alert duration						
t_{ALT}	time-out period		–	16	–	s
t_{ALL}	alert time LOW (AL output only)		–	4	–	s
t_{ALH}	alert time HIGH (AH and AL outputs)		–	12	–	s
t_{ALC}	call alert cycle time	see Fig.9	–	1	–	s
t_{ALP}	call alert pulse duration	see Fig.9	–	125	–	ms
t_{ALD}	call alert hold off period	see Fig.8	52	–	–	ms
t_{RPT}	repeat alert duration	see Fig.11	–	–	4	s
t_{RCR}	repeat alert recurrence time	see Fig.11	–	–	15	s
t_{RCP}	repeat alert cycle time		–	–	500	ms
t_{RPD}	repeat alert pulse duration		–	–	250	ms
t_{STON}	status alert time	see Fig.10	–	–	62.5	ms
t_{STOF}	status alert delay	see Fig.10	–	–	62.5	ms
t_{SUA}	start-up alert time	SPF02 = 0; see Fig.13	–	–	500	ms
		SPF02 = 1; see Fig.13	–	–	453	ms
t_{ORA}	out-of-range alert pulse width	see Fig.12	–	–	62.5	ms
t_{ORD}	out-of-range alert time	see Fig.12	–	–	2	s
t_{BLAL}	battery LOW-level alert time		–	–	16	s
Receiver control						
t_{RXT}	RE transition time	C_L = 5 pF	–	–	100	ns
t_{RXON}	RE establishment time	SPF04 = 0; SPF05 = 1	–	7.8	62.5	ms
Data output						
f_{DO}	data output rate		–	2048	–	bits/s
t_{DSD}	strobe period call data	see Fig.15	480	–	495	µs
t_{DSE}	strobe period EEPROM data	see Fig.20	200	488	1150	µs
t_{DSW}	data strobe pulse width	see Fig.15	230	–	250	µs
t_{TDO}	data output transition time	C_L = 10 pF; see Fig.15	–	–	100	ns
t_{DOS}	data output set-up time	see Fig.15	–	–	135	µs
t_{DOH}	data output hold time	see Fig.15	115	–	–	µs
t_{BYD}	consecutive byte delay		1210	–	1225	µs
t_{CWD}	inter-codeword delay	1200 bits/s numeric message	3420	–	–	µs
t_{ST}	start condition set-up time	see Fig.15	4750	–	–	µs
t_{SP}	stop condition set-up time	see Fig.15	595	–	615	µs
t_{STL}	start bit period OL output		480	–	495	µs
t_{SPL}	stop bit period OL output		480	488	495	µs
t_{SDD}	SPF output delay	see Fig.20	1	–	10	ms

TIMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only Pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating frequency dependent						
f_{osc}	oscillator frequency	SPF03 = 0	–	32768	–	Hz
		SPF03 = 1	–	76800	–	Hz
t_{TDI}	data input transition time		–	–	100	µs
t_{DI1}	data input logic 1		–	∞	–	
t_{DI0}	data input logic 0		–	∞	–	
f_{DI}	data input rate	SPF02 = 0	–	512	–	bits/s
t_{BIT}	bit period		–	1.9531	–	ms
t_{CW}	codeword duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms
f_{DI}	data input rate	SPF02 = 1; f_{osc} = 76800 Hz	–	1200	–	bits/s
t_{BIT}	bit period		–	833.3	–	ms
t_{CW}	codeword duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
Alert only mode (SPF01 = 0)						
t_{SDB}	switch debounce period		–	62.5	–	ms
Display pager mode (SPF01 = 1); see Figs 6 and 7						
t_{STP}	status set-up time	f_{osc} = 32768 Hz	35	–	–	µs
t_{STD}	status change delay		–	–	35	µs
t_{IEH}	interface enable hold time		35	–	–	µs
t_{STH}	status hold time		35	–	–	µs
t_{SPD}	status pulse duration		35	–	–	µs
t_{STP}	status set-up time	f_{osc} = 76800 Hz	15	–	–	µs
t_{STD}	status change delay		–	–	15	µs
t_{IEH}	interface enable hold time		15	–	–	µs
t_{STH}	status hold time		15	–	–	µs
t_{SPD}	status pulse duration		15	–	–	µs

PROGRAMMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = V_{PG} = −5.0 V (see notes 1, 2 and 3); V_{ref} = V_{SS}; pins 2 and 3 open-circuit; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder in OFF status.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programming; see Fig.19						
t_{RES}	power-up reset pulse width	note 4	35	–	–	µs
t_{PEW}	erase/write time		10	–	–	ms
f_{EW}	erase/write frequency		1.0	1.5	2.0	MHz
t_{EW}	erase/write cycles		1000	10000	–	–
t_{DR}	data retention time	T_{amb} = 85 °C	10	–	–	years
t_{PCH}	data clock HIGH time	note 4	65	–	–	µs
t_{PCL}	data clock LOW time	note 4	65	–	–	µs
t_{PRS}	read set-up time	note 4	–	–	35	µs
t_{PSI}	data set-up time on input	note 4	35	–	–	µs
t_{PSO}	data set-up time on output	note 4	–	–	35	µs
t_{PDH}	data hold time	note 4	35	–	–	µs

Notes

1. V_{SS} = V_{PG} only required during erase/write (t_{PEW} in Fig.19), otherwise $V_{SS(min)}$ = −1.5 V.
2. Maximum voltage for programming (V_{PG}) is −5.5 V.
3. See Section "EEPROM Write operation" and Chapter "Limiting values" for limitations of V_{ref} when programming while the voltage converter is enabled.
4. EEPROM programming is also possible at higher frequencies (76.8 kHz or 153.6 kHz). The timings shown then become proportionally smaller.

APPLICATION INFORMATION

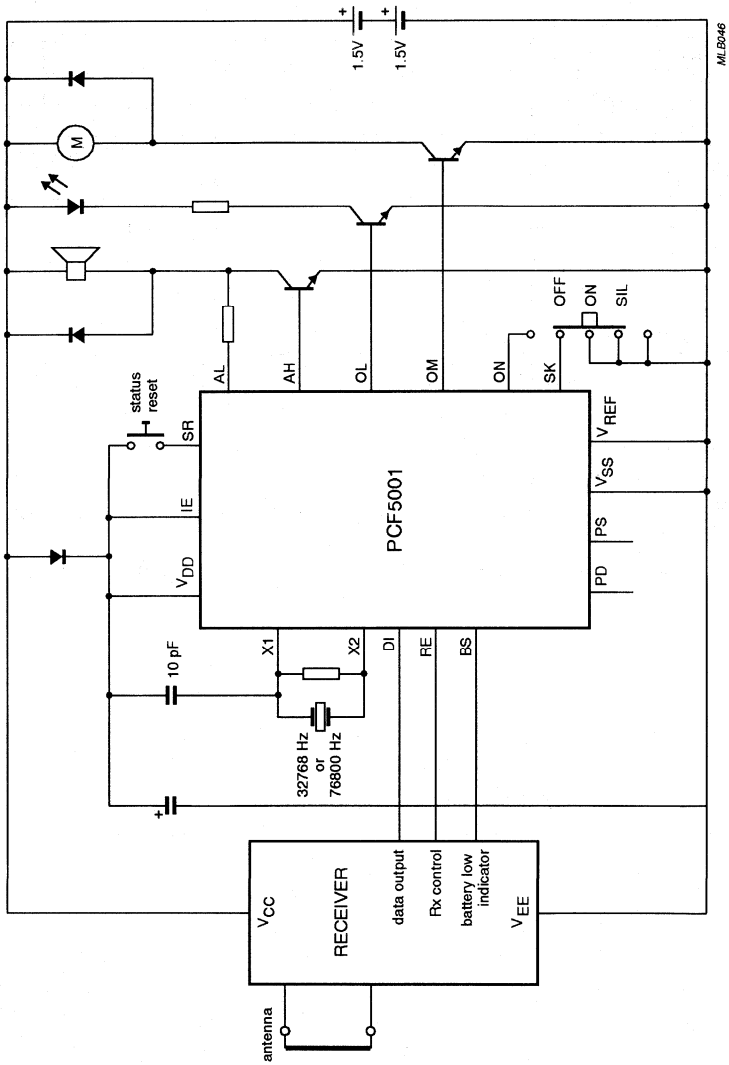


Fig.21 Alert-only pager application example.

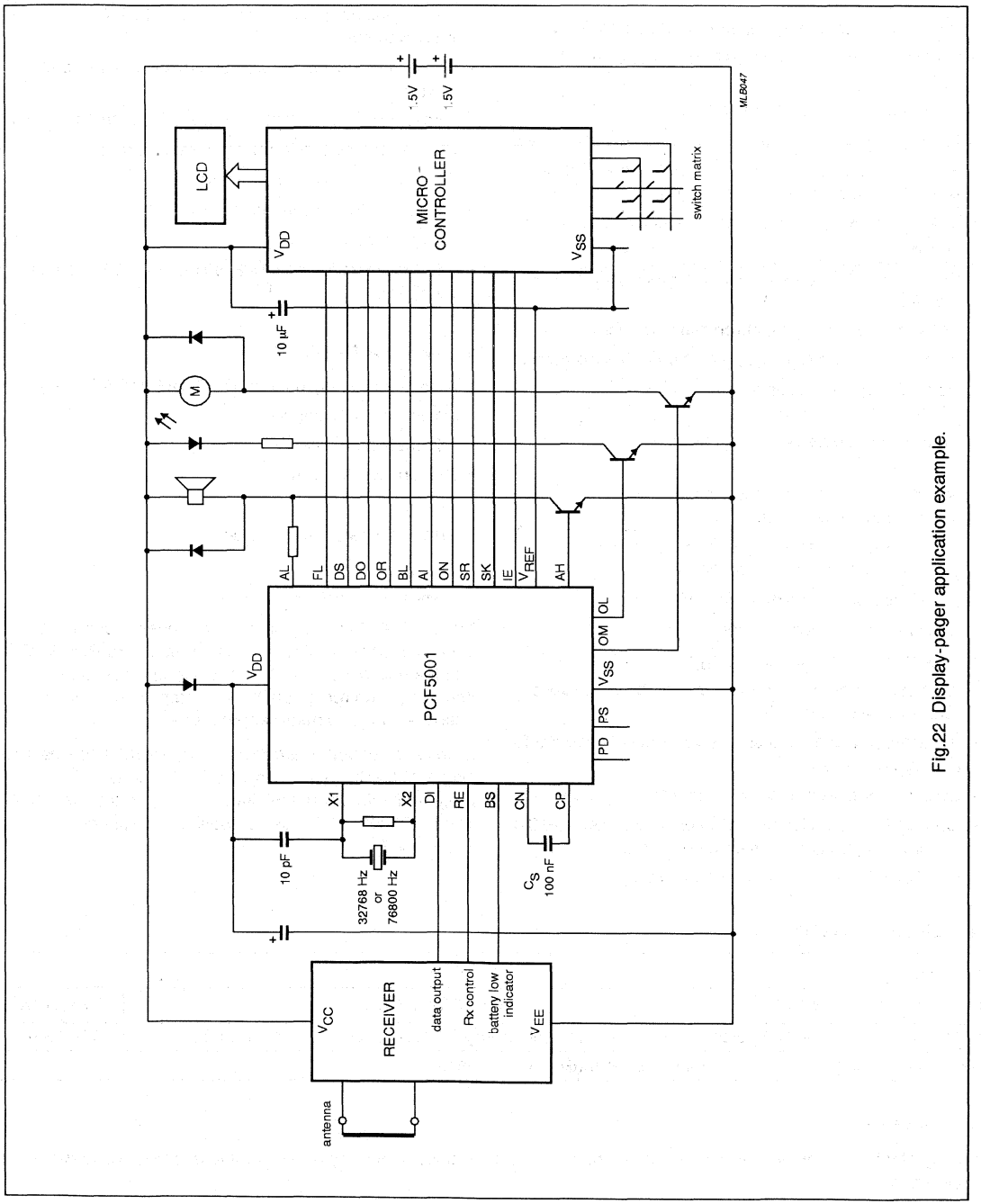


Fig.22 Display-pager application example.

Advanced POCSAG and APOC-1 Paging Decoder

PCD5002

1 FEATURES

- Wide operating supply voltage range: 1.5 to 6.0 V
- Low operating current: 50 μA typ. (ON), 25 μA typ. (OFF)
- Temperature range −25 to +70 °C
- *"CCIR radio paging Code No. 1"* (POCSAG) compatible
- Supports Advanced Pager Operator's Code Phase 1 (APOC-1) for extended battery economy
- 512, 1200 and 2400 bits/s data rates using 76.8 kHz crystal
- Built-in data filter (16-times oversampling) and bit clock recovery
- Advanced ACCESS synchronization algorithm
- 2-bit random and (optional) 4-bit burst error correction
- Up to 6 user addresses (RICs), each with 4 functions/alert cadences
- Up to 6 user address frames, independently programmable
- Standard POCSAG sync word, plus up to 4 user programmable sync words
- Continuous data decoding upon reception of user programmable sync word (optional)
- Received data inversion (optional)
- Call alert via beeper, vibrator or LED
- 2-level acoustic alert using single external transistor
- Alert control: automatic (POCSAG type), via cadence register or alert input pin
- Separate power control of receiver and RF oscillator for battery economy
- Synthesizer set-up and control interface (3-line serial)
- On-chip EEPROM for storage of user addresses (RICs), pager configuration and synthesizer data
- On-chip SRAM buffer for message data
- Slave I²C-bus interface to microcontroller for transfer of message data, status/control and EEPROM programming
- Wake-up interrupt for microcontroller, programmable polarity
- Direct and I²C-bus control of operating status (ON/OFF)
- Battery-low indication (external detector)
- Out-of-range condition indication
- Real time clock reference output
- On-chip voltage doubler
- Interfaces directly to UAA2080 and UAA2082 paging receivers.

2 APPLICATIONS

- Advanced display pagers (POCSAG and APOC-1)
- Basic alert-only pagers
- Information services
- Personal organizers
- Telepoint
- Telemetry/data transmission.

3 GENERAL DESCRIPTION

The PCD5002 is a very low power pager decoder and controller, capable of handling both standard POCSAG and the advanced APOC-1 code. Continuous data decoding upon reception of a dedicated sync word is available for news pager applications.

Data rates supported are 512, 200 and 2400 bits/s using a single 76.8 kHz crystal. On-chip EEPROM is programmable using a minimum supply voltage of 2.5 V. The PCD5002 is I²C-bus compatible (maximum 100 kbits/s).

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5002H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
PCD5002U/10	–	film-frame carrier (naked die) 32 pads	–

5 LICENSE

Supply of this IC does neither convey nor express an implied license under any patent right to use this in any APOC application.

6 BLOCK DIAGRAM

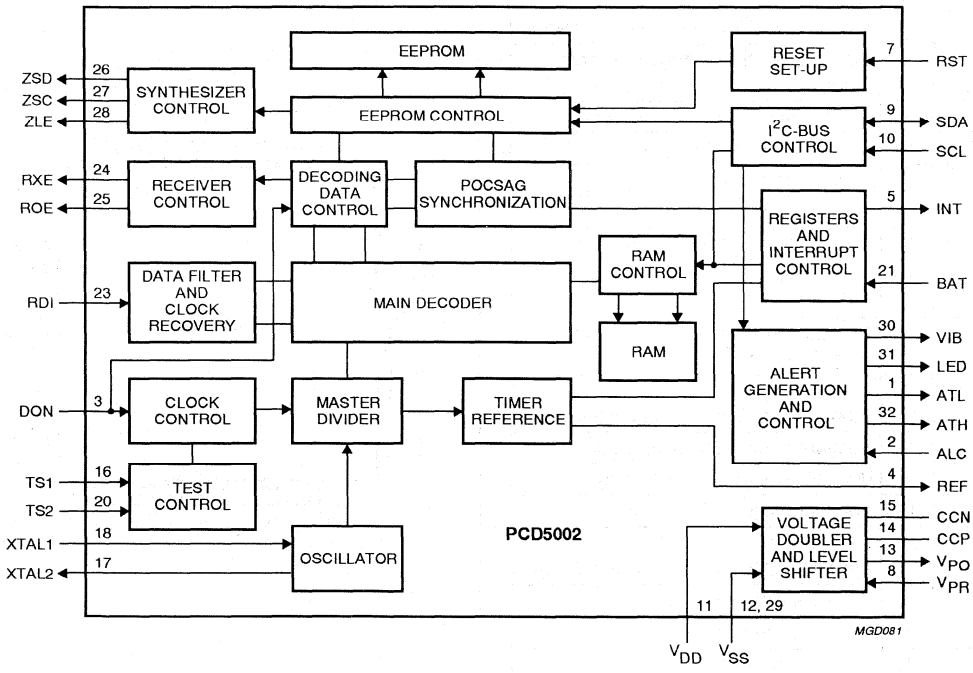


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
ATL	1	alert LOW level output
ALC	2	alert control input (normally LOW by internal pull-down)
DON	3	direct ON/OFF input (normally LOW by internal pull-down)
REF	4	real time clock frequency reference output
INT	5	interrupt output
n.c.	6	not connected
RST	7	reset input (normally LOW by internal pull-down)
V_{PR}	8	external positive voltage reference input
SDA	9	I^2C-bus serial data input/output
SCL	10	I^2C-bus serial clock input
V_{DD}	11	main positive supply voltage
V_{SS}	12	main negative supply voltage
V_{PO}	13	voltage converter positive output
CCP	14	voltage converter shunt capacitor (positive side)
CCN	15	voltage converter shunt capacitor (negative side)
TS1	16	test input 1 (normally LOW by internal pull-down)
XTAL2	17	decoder crystal oscillator output
XTAL1	18	decoder crystal oscillator input
n.c.	19	not connected
TS2	20	test input 2 (normally LOW by internal pull-down)
BAT	21	battery sense input
n.c.	22	not connected
RDI	23	received data input (POCSAG or APOC-1)
RXE	24	receiver circuit enable output
ROE	25	receiver oscillator enable output
ZSD	26	synthesizer serial data output
ZSC	27	synthesizer serial clock output
ZLE	28	synthesizer latch enable output
V_{SS}	29	main negative supply voltage
VIB	30	vibrator motor drive output
LED	31	LED drive output
ATH	32	alert HIGH level output

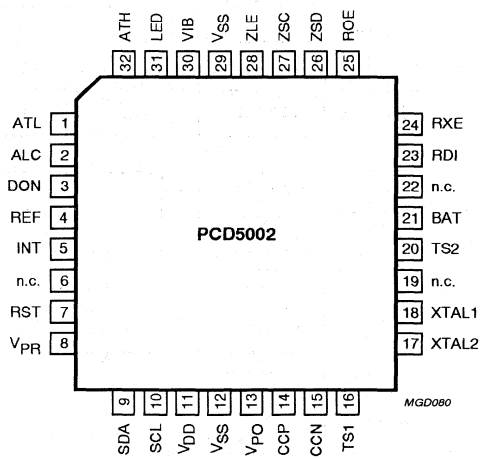


Fig.2 Pin configuration for SOT358-1 (LQFP32).

8 FUNCTIONAL DESCRIPTION

8.1 Introduction

The PCD5002 is a very low power decoder and pager controller specifically designed for use in new generation radio pagers. The architecture of the PCD5002 allows for flexible application in a wide variety of radio pager designs.

The PCD5002 is fully compatible with *"CCIR Radio paging Code No. 1"* (also known as the POCSAG code) operating at data rates of 512, 1200 and 2400 bits/s using a single oscillator crystal of 76.8 kHz.

The PCD5002 also supports the new Advanced Pager Operator's Code Phase 1 (APOC-1). This compatible extension to the POCSAG code improves battery economy by introducing 'cycles' and batch numbering. A cycle consists of 5 or 15 standard POCSAG batches. Each pager will be allocated a batch number in addition to its POCSAG address and it will only search for its address during this batch.

In addition to the standard POCSAG sync word (used also in APOC-1) the PCD5002 is also capable of recognizing up to 4 User Programmable Sync Words (UPSWs). This permits the reception of both private services and POCSAG or APOC-1 transmissions via the same radio channel. As an option reception of a UPSW may activate Continuous Data Decoding (CDD).

Used together with the Philips UAA2080 or UAA2082 paging receiver, the PCD5002 offers a highly sophisticated, miniature solution for the radio paging market. Control of an RF synthesizer circuit is also provided to ease alignment and channel selection.

On-chip EEPROM provides storage for user addresses (Receiver Identity Codes or RICs) and Special Programmed Functions (SPFs) and UPSWs, which eliminates the need for external storage devices and interconnection. For other non-volatile storage 20 bytes of general purpose EEPROM are available. The low EEPROM programming voltage makes the PCD5002 well suited for 'over-the-air' programming/reprogramming.

On request from an external controlling device or automatically (by SPF programming), the PCD5002 will provide standard POCSAG alert cadences by driving a standard acoustic 'beeper'. Non-standard alert cadences may be generated via a cadence register or a dedicated control input.

The PCD5002 can also produce a HIGH level acoustic alert as well as drive an LED indicator and a vibrator motor via external bipolar transistors.

The PCD5002 contains a low-power, high-efficiency voltage converter (doubler) designed to provide a higher voltage supply to LCD drivers or microcontrollers. In addition, an independent level shifted interface is provided allowing communication to a microcontroller operating at a higher voltage than the PCD5002.

Interface to such an external device is provided by an I^2C-bus which allows received call identity and message data, data for the programming of the internal EEPROM, alert control and pager status information to be transferred between the devices. Pager status includes features provided by the PCD5002 such as battery-low and out-of-range indications. A dedicated interrupt line minimizes the required microcontroller activity.

A selectable low frequency timing reference is provided for use in real time clock functions.

Data synchronization is achieved by the Philips patented ACCESS® algorithm ensuring that maximum advantage is made of the POCSAG code structure particularly in fading radio signal conditions. The algorithm allows for data synchronization without preamble detection whilst minimizing battery power consumption. The APOC-1 code uses an extended version of the ACCESS synchronization algorithm.

Random (and optional) burst error correction techniques are applied to the received data to optimize the call success rate without increasing the falsing rate beyond specified POCSAG levels.

8.2 The POCSAG paging code

A transmission using the *"CCIR Radio paging Code No. 1"* (POCSAG code) is constructed in accordance with the following rules (see Fig.3).

The transmission is started by sending a **preamble**, consisting of at least 576 continuously alternating bits (10101010...). The preamble is followed by an arbitrary number of batch blocks. Only complete batches are transmitted.

Each **batch** comprises 17 code-words of 32 bits each. The first code-word is a synchronization code-word with a fixed pattern. The **sync** word is followed by 8 frames (0 to 7) of 2 code-words each, containing message information. A code-word in a frame can either be an address, message or idle code-word.

Idle code-words also have a fixed pattern and are used to fill empty frames or to separate messages.

Address code-words are identified by an MSB at logic 0 and are coded as shown in Fig.3. A user address or RIC consists of 21 bits. Only the upper 18 bits are encoded in the address code-word (bits 2 to 19). The lower 3 bits designate the frame number in which the address is transmitted.

Four different **call types** can be distinguished on each user address. The call type is determined by two function bits in the address code-word (bits 20 and 21), as shown in Table 1.

Alert-only calls consist only of a single address code-word. Numeric and alphanumeric calls have message code-words following the address.

Message code-words are identified by an MSB at logic 1 and are coded as shown in Fig.3. The message information is stored in a 20-bit field (bits 2 to 21).

The standard data format is determined by the call type: 4 bits per digit for numeric messages and 7 bits per (ASCII) character for alphanumeric messages.

Each code-word is protected against transmission errors by 10 CRC check bits (bits 22 to 31) and an even-parity bit (bit 32). This permits correction of a maximum of 2 random errors or up to 3 errors in a burst of 4 bits (a 4-bit burst error) per code-word.

8.3 The APOC-1 paging code

The APOC-1 paging code is fully POCSAG compatible and involves the introduction of batch grouping and a Batch Zero Identifier. This reserved address code-word indicates the start of a 'cycle' of 5 or 15 batches long and is transmitted immediately after a sync word.

Cycle transmission must be coherent i.e. a transmission starting an integer number of cycle periods after the start of the previous one.

Broadcast message data may be included in a transmission. This information may occupy any number of message code-words and immediately follows the batch zero identifier of the first cycle after preamble.
The presence of data is indicated by the function bits in the batch zero identifier: 1,1 indicates 'no broadcast data'. Any other combination indicates a broadcast message.

The PCD5002 can be configured for POCSAG or APOC-1 operation via SPF programming. The batch zero identifier is programmable and can be stored in any identifier location in EEPROM.

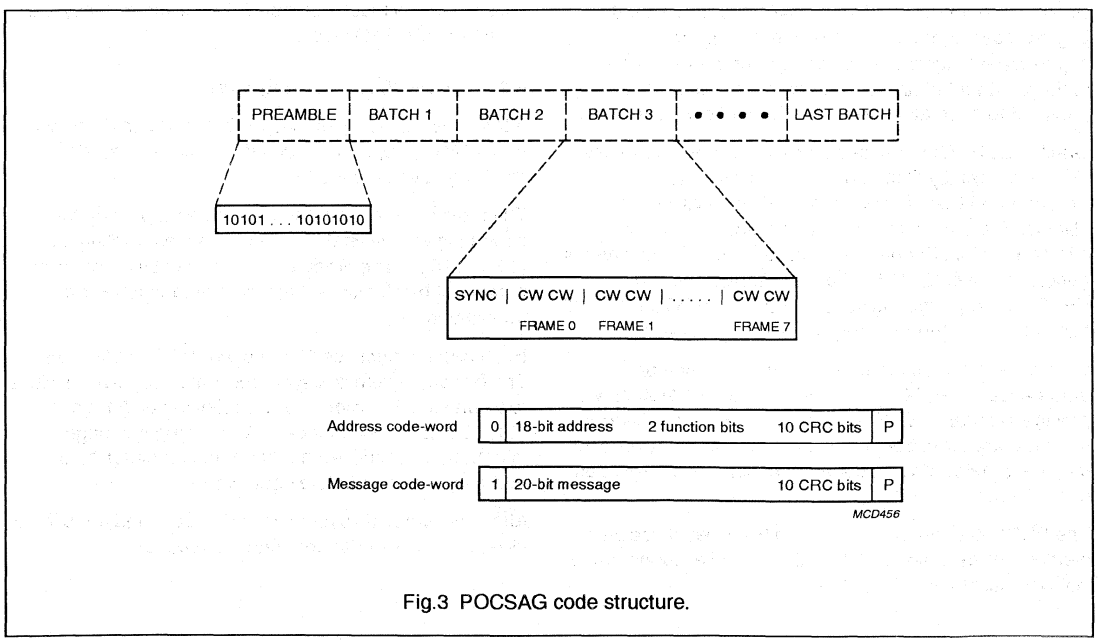


Fig.3 POCSAG code structure.

Table 1 POCSAG call types and function bits

BIT 20 (MSB)	BIT 21 (LSB)	CALL TYPE	DATA FORMAT
0	0	numeric	4-bits per digit
0	1	alert only	–
1	0	alert only	–
1	1	alphanumeric	7-bits per ASCII character

The POCSAG standard only allows combinations of data formats and function code bits as given in Table 1. However, other (non-standard) combinations will be decoded normally by the PCD5002.

8.4 Error correction

In the PCD5002 error correction methods have been implemented as shown in Table 2.

Random error correction is default for both address and message code-words. In addition, burst error correction can be enabled by SPF programming. Up to 3 erroneous bits in a 4-bit burst can be corrected.

The error type detected for each code-word is identified in the message data output to the microcontroller, allowing rejection of calls with too many errors.

Table 2 Error correction

ITEM	DESCRIPTION
Preamble	4 random errors in 31 bits
Synchronization code-word	2 random errors in 32 bits
Address code-word	2 random errors, plus; 4-bit burst errors (optional)
Message code-word	2 random errors, plus; 4-bit burst errors (optional)

8.5 Operating states

The PCD5002 has 2 operating states;

- ON status
- OFF status.

The operating state is determined by a Direct Control input (DON) and bit D4 in the control register (see Table 3).

Table 3 Truth table for decoder operating status

DON INPUT	CONTROL BIT D4	OPERATING STATUS
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

8.6 ON status

In the ON status the decoder pulses the receiver and oscillator enable outputs (RXE and ROE respectively) according to the code structure and the synchronization algorithm. Data received serially at the data input (RDI) is processed for call reception.

The data protocol can be POCSAG or APOC-1. Continuous data decoding upon reception of a special sync word is also supported. The data protocol is selected by SPF programming.

Reception of a valid paging call is signalled to the microcontroller by an interrupt signal. The received address and message data can then be read via the I²C-bus interface.

8.7 OFF status

In the OFF status the decoder will neither activate the receiver or oscillator enable outputs, nor process any data at the data input. The crystal oscillator remains active to permit communication with the microcontroller.

In both operating states an accurate timing reference is available via the REF output. Using SPF programming the signal periodicity may be selected as 32.768 kHz, 50 Hz, 2 Hz or $1/60$ Hz.

8.8 Reset

The decoder can be reset by applying a positive pulse on input pin RST. A power-on reset circuit consisting of an RC network can also be connected to this input. Conditions during and after a reset are described in Chapter "Operating instructions".

8.9 Bit rates

The PCD5002 can be configured for data rates of 512, 1200 or 2400 bit/s by SPF programming. These data rates are derived from a single 76.8 kHz oscillator frequency.

8.10 Oscillator

The oscillator circuit is designed to operate at 76.8 kHz. Typically, a tuning fork crystal will be used as a frequency source. Alternatively, an external clock signal can be applied to pin XTAL1 (amplitude = V_{DD} to V_{SS}), but a slightly higher oscillator current is consumed. A 2.2 MΩ feedback resistor connected between XTAL1 and XTAL2 is required for proper operation.

To allow easy oscillator adjustment (e.g. by a variable capacitor) a 32.768 kHz reference frequency can be selected at output REF by SPF programming.

8.11 Input data processing

Data input is binary and fully asynchronous. Input bit rates of 512, 1200 and 2400 bits/s are supported. As a programmable option, the polarity of the received data can be inverted before further processing.

The input data is noise filtered by a digital filter. Data is sampled at 16 times the data rate and averaged by majority decision.

The filtered data is used to synchronize an internal clock generator by monitoring transitions. The recovered clock phase can be adjusted in steps of $1/8$ or $1/32$ bit period per received bit.

The larger step size is used when bit synchronization has not been achieved, the smaller when a valid data sequence has been detected (e.g. preamble or sync word).

8.12 Battery saving

Current consumption is reduced by switching off internal decoder sections whenever the receiver is not enabled.

To further increase battery efficiency, reception and decoding of an address code-word is stopped as soon as the uncorrected address field differs by more than 3 bits from the enabled RICs. If the next code-word must be received again, the receiver is re-enabled thus observing the programmed establishment times t_{RXE} and t_{ROE}.

The current consumption of the complete pager can be minimized by separately activating the RF oscillator circuit (using output ROE) before activating the rest of the receiver. This is possible using the UAA2082 receiver which has external biasing for the oscillator circuit.

8.13 POCSAG Synchronization strategy

In the ON status the PCD5002 synchronizes to the POCSAG data stream by the Philips ACCESS® algorithm. A flow diagram is shown in Fig.4. Where 'sync word' is used, this implies both the standard POCSAG sync word and any enabled User Programmable Sync Word (UPSW).

Several modes of operation can be distinguished depending on the synchronization state. Each mode uses a different method to obtain or retain data synchronization. The receiver and oscillator enable outputs (RXE and ROE respectively) are switched accordingly, with the appropriate establishment times (t_{RXON} and t_{ROON} respectively).

Before comparing received data with preamble, an enabled sync word or programmed user addresses, the appropriate error correction is applied.

Initially, after switching to the ON status, the decoder is in **Switch-on** mode. Here the receiver will be enabled for a period up to 3 batches, testing for preamble and the sync word. Failure to detect preamble or the sync word will cause the device to switch to the carrier-off mode.

When preamble is detected it will causes the device to switch to the **Preamble Receive** mode, in which a sync word is searched for. The receiver will remain enabled while preamble is detected. When neither sync word nor preamble is found within a 1 batch duration the carrier-off mode is entered.

Upon detection of a sync word the **Data Receive** mode is entered. The receiver is activated only during enabled user address frames and sync word periods. When an enabled user address has been detected, the receiver will be kept enabled for message code-word reception until the call termination criteria are met.

During call reception data bytes are stored in an internal SRAM buffer, capable of storing 2 batches of message data.

Messages are transmitted contiguously, only interrupted by sync words at the beginning of each batch. When a message extends beyond the end of a batch no testing for sync takes place. Instead, a message data transfer will be initiated by an interrupt to the external controller. Data reception continues normally after a period corresponding to the sync word duration.

If any message code-word is found to be uncorrectable, the data-fail mode is entered and no data transfer will be attempted at the next sync word position. Instead, a test for sync word will be carried out.

In the **Data Fail** mode message reception continues normally for 1 batch duration. When a sync word is detected at the expected position the decoder returns to the data receive mode. If the sync word again fails to appear, then batch synchronization is deemed lost. Call reception is then terminated and the fade recovery mode is entered.

The **Fade Recovery** mode is intended to scan for sync word and preamble over an extended window (nominal position ± 8 bits). This is performed for a period of up to 15 batches, allowing recovery of synchronization from long fades in the radio signal. Detection of preamble causes switching to the preamble receive mode, while sync word detection causes switching to the data receive mode. When neither is found within a period of 15 batches, the radio signal is considered lost and the carrier-off mode is entered.

The purpose of the **Carrier-Off** mode is to detect a valid radio transmission and synchronize to it quickly and efficiently. Because transmissions may start at random, the decoder enables the receiver for 1 code-word in every 18 code-words looking for preamble or sync word.
By using a buffer containing 32 bits (n bits from the current scan, 32-n from the previous scan) effectively every batch bit position can be tested within a continuous transmission of at least 18 batches. Detection of preamble causes the device to switch to the preamble receive mode, while sync word detection switches to the data receive mode.

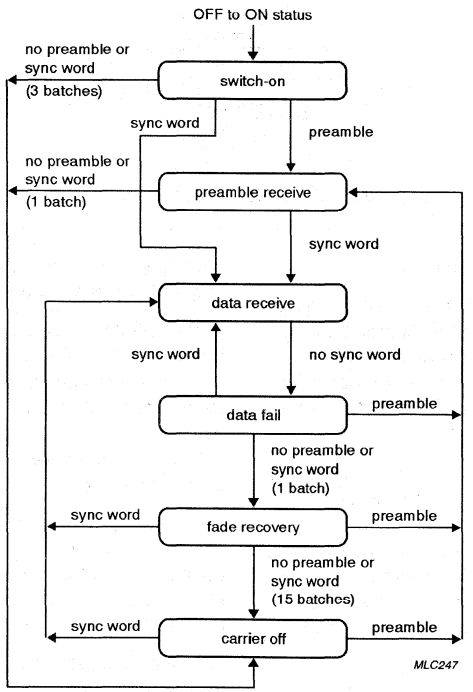


Fig.4 ACCESS® synchronization algorithm for POCSAG.

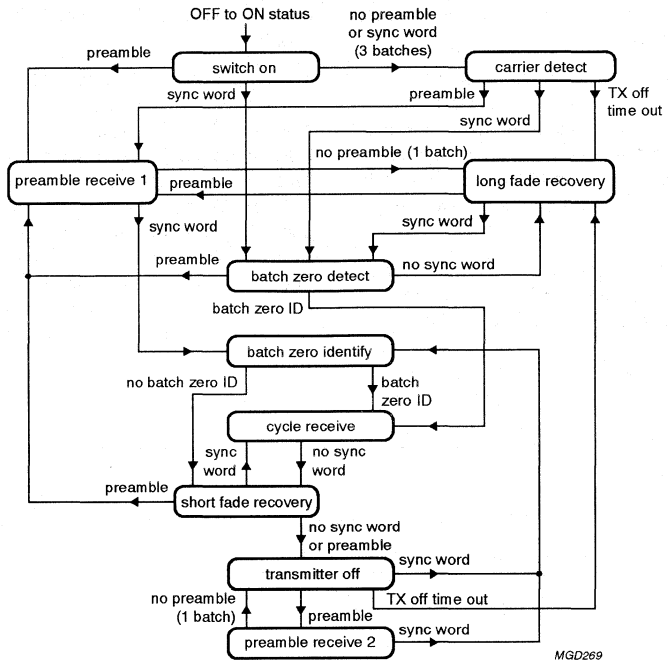


Fig.5 APOC-1 synchronization algorithm.

8.14 APOC-1 synchronization strategy

The synchronization strategy in APOC-1 is an extended version of the ACCESS scheme and is illustrated in Fig.5. The PCD5002 counts the number of batches in a transmission, starting from the first batch received after preamble. Counter overflow occurs due to the size of a cycle, as determined by SPF programming.

Initially, after switching to the ON status, the decoder will be in the **Switch-on** mode. Here the receiver will be enabled for up to 3 batches, testing for preamble and sync word. Detection of preamble causes the device to switch to the preamble receive mode, while any enabled sync word enters the batch zero detect mode. Failure to detect either will cause the device to switch to the carrier detect mode.

In the **Preamble Receive 1** mode the PCD5002 searches for a sync word, the receiver remaining enabled while preamble is detected. As soon as an enabled sync word is found the batch zero identify mode is started.

If preamble is not found within one batch duration then the long fade recovery mode is entered.

When in **Batch Zero Detect** mode the PCD5002 switches on every batch to maintain synchronization and check for the batch zero identifier. Detection of the batch zero identifier activates the cycle receive mode. When synchronization is lost the long fade recovery mode is entered. Preamble receive mode is entered when preamble is detected.

In the **Batch Zero Identify** mode the first code-word immediately after the sync word of the first batch is compared with the programmed batch zero identifier. Failure to detect the batch zero identifier will cause the device to enter the short fade recovery mode.

When this comparison is successful the function bits determine whether any broadcast message will follow. Any function bit combination other than '1,1' will cause the PCD5002 to accept message code-words until terminated by a valid address code-word. After reception of any

broadcast message data the PCD5002 continues to operate in the cycle receive mode.

In the **Cycle Receive** mode the PCD5002 enables call reception in only one programmed batch per cycle. Sync word detection takes place from 2 bits before to 2 bits after the expected sync word position of this batch. If the sync word is not detected then the position of the current sync word will be maintained and the short fade recovery mode will be entered.

When a valid sync word is found user address code-word detection takes place, as in normal POCSAG code. Any following message code-words are received normally. If a message extends into a subsequent batch containing a batch zero identifier, then the batch zero identifier is detected normally and message reception will continue.

Data reception is suspended after the programmed batch until the same batch position in the next cycle. The exception being when a received call continues into the next batch.

In the **Short Fade Recovery** mode the programmed data receive batch will continue to be checked for user address code-words. In addition the first code-word after the programmed batch is checked for sync word or preamble.

When a valid sync word is detected the cycle receive mode is re-entered, while detection of preamble causes the device to switch to the preamble receive mode. When neither is found then the transmitter off mode is entered.

In the **Transmitter Off** mode a time-out is set to a pre-programmed duration. This time-out corresponds to the maximum time between subsequent transmissions (preamble to preamble).

The PCD5002 then checks the first batch of every cycle for sync word or preamble. The programmed data receive batch is ignored (unless it is batch 0).

Table 4 Synchronization window tolerance as a function of bit rate

TIME FROM LOSS OF SIGNAL	TOLERANCE		
	512 (bit/s)	1200 (bit/s)	2400 (bit/s)
≤ 30 s	4 bits	4 bits	4 bits
≤ 60 s	4 bits	4 bits	8 bits
≤ 120 s	4 bits	8 bits	16 bits
≤ 240 s	8 bits	16 bits	32 bits

Synchronization checking is performed over a window ranging from 'n' bits before to 'n' bits after the expected sync word position. The window tolerance 'n' depends on the time since the transmitter off mode was entered and on the selected bit rate (see Table 4).

When a sync word is detected in this widened synchronization window the PCD5002 enters the batch zero identify mode. Time-out expiry before a sync word has been detected causes the device to switch to the long fade recovery mode.

Detection of preamble in the transmitter off mode initiates the **Preamble Receive 2** mode. Operation in this mode is identical to preamble receive 1 mode. Failure to detect preamble for one batch period will cause the device to switch back to the transmitter off mode. This prevents inadvertent loss of cycle synchronization due to spurious signals resembling preamble.

The **Carrier Detect** mode is identical to the carrier off mode in standard POCSAG operation. Upon first entry the transmitter off time-out is started. The receiver is enabled to receive one code-word in every 18 code-words to check for sync word and preamble. This check is performed on the last available 32 bits for every received bit.

The preamble receive mode is entered when preamble is detected. If a valid sync word is found the batch zero detect mode is entered. When neither has been detected and the time-out expires, then the long fade recovery mode is entered.

The **Long Fade Recovery** mode is intended to quickly regain synchronization in fading conditions (not caused by the transmitter switching off between transmissions) or when having been out of range, while maintaining acceptable battery economy.

Initially, the receiver is switched off until one cycle duration after the last enabling in the transmitter off mode. The receiver is then enabled for a 2 code-word period in which each contiguous group of 32 bits is tested for **any decodable** POCSAG code-word (including sync word) and preamble. Single-bit error correction is applied.

If a code-word is detected, the receiver enable period is extended by another code-word duration and the above test is repeated. This process continues while valid code-words are received.

Detection of preamble will cause the device to switch to the preamble receive mode, while sync word detection will cause the device to switch to the batch zero detect mode. When neither is detected during the 2 code-word window or any following 32-bit group, the receiver will be disabled.

If valid code-words are detected but no sync word or preamble is detected over a period of 18 code-words, the receiver is also disabled.

Data sampling, as previously described, is repeated one cycle duration after the moment the receiver was last activated.

8.15 Call termination

Call reception is terminated as follows;

- Upon reception of any address code-word (including Idle code-word but excluding the batch zero identifier in APOC-1 operation) requiring no more than single bit error correction
- In data fail mode, when a sync word is not detected at the expected batch position
- When a forced call termination command is received from an external controller.

The last method permits an external controller to stop call reception, depending on the number and type of errors which occurred in a call. After a forced call termination the decoder will enter the data fail mode.

The type of error correction as well as the call termination conditions are indicated by status bits in the message data output.

Following call termination, transfer of the data received since the previous sync word period is initiated by an interrupt to the external controller.

8.16 Call data output format

POCSAG call information is stored in the decoder SRAM in blocks of 3 bytes per code-word. Each stored call consists of a call header, followed by message data blocks and a call terminator. In the event of concatenated messages the call terminator is replaced with the call header of the next message. An alert-only call only has a call header and a call terminator.

The formats of a call header, a message data block and a call terminator are shown in Tables 5, 7 and 9.

A **Call Header** contains information on the last sync word received, the RIC which began call reception and the type of error correction performed on the address code-word.

A **Message Data** block contains the data bits from a message code-word plus the type of error correction performed. No deformatting is performed on the data bits: numeric data appear as 4-bit groups per digit, alphanumeric data has a 7-bit ASCII representation.

The **Call Terminator** contains information on the last sync word received, information on the way the call was terminated (forced call termination command, loss of sync word in data fail mode) and the type of error correction performed on the terminating code-word.

8.17 Error type indication

Table 11 shows how the different types of detected errors are encoded in the call data output format.

A message code-word containing more than a single bit error (bit E3 = 1) may appear as an address code-word (bit M1 = 0) after error correction. In this event the code-word is processed as message data and does not cause call termination.

8.18 Data transfer

Data transfer is initiated either during sync word periods or as soon as the receiver is disabled after call termination. If the SRAM buffer is full, data transfer is initiated immediately during the next code-word.

When the PCD5002 is ready to transfer received call data an external interrupt will be generated via output INT. Any message data can be read by accessing the RAM output register via the I^2C-bus interface. Bytes will be output starting from the position indicated by the RAM read pointer.

Table 5 Call header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	S3	S2	S1	R3	R2	R1	DF
2	0	S3	S2	S1	R3	R2	R1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 6 Call header bit identification

BITS (MSB to LSB)	IDENTIFICATION
S3 to S1	identifier number of sync word for current batch (7 = standard POCSAG)
R3 to R1	identifier number of user address (RIC)
DF	data fail mode indication (1 = data fail mode); note 1
F0 and F1	function bits of received address code-word (bits 20 and 21)
E3 to E1	detected error type; see Table 11; E3 = 0 in a concatenated call header

Note

1. The DF bit in the call header is set:
   a) When the sync word of the batch in which the (beginning of the) call was received, did not match the standard POCSAG or a user-programmed sync word. The sync word identifier (bits S3 to S1) will then be made 0.
   b) When any code-word of a previous call received in the same batch was uncorrectable.

Table 7 Message data format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	M2	M3	M4	M5	M6	M7	M8	M9
2	M10	M11	M12	M13	M14	M15	M16	M17
3	M18	M19	M20	M21	E3	E2	E1	M1

Table 8 Message data bit identification

BITS (MSB to LSB)	IDENTIFICATION
M2 to M21	message code-word data bits
E3 to E1	detected error type; see Table 11
M1	message code-word flag

Table 9 Call terminator format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	FT	S3	S2	S1	0	0	0	DF
2	FT	S3	S2	S1	0	0	0	X
3	X	X	X	X	E3	E2	E1	0

Table 10 Call terminator bit identification

BITS (MSB to LSB)	IDENTIFICATION
FT	forced call termination (1 = yes)
S3 to S1	identifier number of last sync word
DF	data fail mode indication (1 = data fail mode); note 1
F0 and F1	function bits of received address code-word (bits 20 and 21)
E3 to E1	detected error type; see Table 11; E3 = 0 in a call terminator

Note

1. The DF bit in the call terminator is set:
   a) When any call data code-word in the terminating batch was uncorrectable, while in data receive mode.
   b) When the sync word at the start of the terminating batch did not match the standard POCSAG or a user-programmed sync word, while in data fail mode.

Table 11 Error type identification (note 1)

E3	E2	E1	ERROR TYPE	NUMBER OF ERRORS
0	0	0	no errors - correct code-word	0
0	0	1	parity bit in error	1
0	1	0	single bit error	1 + parity
0	1	1	single bit error and parity error	1
1	0	0	not used	–
1	0	1	4-bit burst error and parity error	3 (e.g.1101)
1	1	0	2-bit random error	2
1	1	1	uncorrectable code-word	3 or more

Note

1. The POCSAG code does not permit detection of more than 3 bit errors per code-word. Therefore, the number of errors may be larger than indicated.

Successful call termination occurs on reception of a valid address code-word with less than 2 bit errors.
Unsuccessful termination occurs when a sync word is not detected while in the data fail mode.

It is generally possible to distinguish these two conditions using the sync word identifier number (bits S3 to S1); the identifier number will be non-zero for correct termination, and zero for sync word failure.

Only when a call is received in the data fail mode and the call is terminated before the end of the batch, is it not possible to distinguish unsuccessful from successful termination.

Reception of message data can be terminated at any time by transmitting a forced call termination command to the status register via the I^2C-bus. Any call received will then be terminated immediately and the data fail mode will be entered.

8.19 Continuous data decoding

Apart from transmissions in the POCSAG or APOC-1 format, the PCD5002 is also capable of decoding continuous transmissions with the same code-word structure. Any user-programmable sync word (UPSW) may be designated to enable continuous data decoding.

When a Continuous Data Decoding (CDD) sync word is detected at any sync word position, the receiver remains enabled from then on. Status bits D1 and D0 show the CDD mode to be active.

All code-words are decoded and their data fields are stored in SRAM. The usual error information is appended. No distinction is made between address and message code-words: code-word bit 0 is treated as a data bit and is stored in bit M1 of the 3-byte output format.

Code-words received at the expected sync word positions (POCSAG batch size) are matched against standard POCSAG sync word, all enabled UPSWs and preamble.

Data output to an external controller is initiated by an interrupt at the next sync word position, after reception of 16 code-words.

The call header preceding the data has a different structure from normal POCSAG or APOC-1 data. The data header format is shown in Table 12.

Continuous data decoding continues until one of the following conditions occur;

- The decoder is switched to the OFF state
- A Forced Call Termination (FCT) command is received via the I²C-bus
- Preamble is detected at the sync word position
- Standard POCSAG sync word or an enabled non-CDD sync word is detected.

Only a forced call termination command will be indicated in the SRAM data by a call terminator. In the other events continuous data decoding will stop without notification.

Upon forced termination the fade recovery mode is entered. Detection of preamble causes the device to switch to the preamble receive mode. Detection of a standard sync word or any enabled non-continuous UPSW will cause the device to switch to the data receive mode.

Continuous data decoding will continue in the next batch if any enabled CDD sync word is detected or no enabled sync word is detected.

8.20 Receiver and oscillator control

A paging receiver and an RF oscillator circuit can be controlled independently via enable outputs RXE and ROE respectively. Their operating periods are optimized according to the synchronization mode of the decoder. Each enable signal has its own programmable establishment time (see Table 14).

8.21 External receiver control and monitoring

An external controller may enable the receiver control outputs continuously via an I²C-bus command, overruling the normal enable pattern. Data reception continues normally. This mode can be exited by means of a reset or an I²C-bus command.

External monitoring of the receiver control output RXE is possible via bit D6 in the status register, when enabled via the control register (D2 = 1). Each change of state of output RXE will generate an external interrupt at output INT.

Table 12 Continuous data header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	X	X	X	C3	C2	C1	0
2	0	C3	C2	C1	C3	C2	C1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 13 Data header bit identification

BITS (MSB to LSB)	IDENTIFICATION
C3 to C1	identifier number of continuous data decoding sync word
F0 and F1	function bits of received address code-word (bits 20 and 21)
E3 to E1	detected error type (see Table 11); E3 = 0 in a concatenated call header

8.22 Battery condition input

A logic signal from an external sense circuit, signalling battery condition, can be applied to the BAT input. This input is sampled each time the receiver is disabled (RXE ↓ 0).

When enabled via the control register (D2 = 0), the condition of input BAT is reflected in bit D6 of the status register. Each change of state of bit D6 causes an external interrupt at output INT.

When using the UAA2080 pager receiver a battery-low condition corresponds to a logic HIGH level. With a different sense circuit the reverse polarity can be used as well, because every change of state is signalled to an external controller.

After a reset the initial condition of the battery-low indicator in the status register is zero.

Table 14 Receiver and oscillator establishment times (note 1)

CONTROL OUTPUT	ESTABLISHMENT TIME				UNIT
RXE	5	10	15	30	ms
ROE	20	30	40	50	ms

Note

1. The exact values may differ slightly from the above values, depending on the bit rate (see Table 25).

8.23 Synthesizer control

Control of an external frequency synthesizer is possible via a dedicated 3-line serial interface (outputs ZSD, ZSC and ZLE). This interface is common to a number of available synthesizers. The synthesizer is enabled using the oscillator enable output ROE.

The frequency parameters must be programmed in EEPROM. Two blocks of maximum 24 bits each can be stored. Any unused bits must be programmed at the beginning of a block: only the last bits are used by the synthesizer.

When the function is selected by SPF programming (SPF byte 01, bit D6), data is transferred to the synthesizer each time the PCD5002 is switched from the OFF to the ON status. Transfer takes place serially in two blocks, starting with bit 0 (MSB) of block 1 (see Table 28).

Data bits on ZSD change on the falling edges of ZSC. After clocking all bits into the synthesizer, a latch enable pulse copies the data to the internal divider registers. A timing diagram is illustrated in Fig.6.

The data output timing is synchronous, but has a pause in the bitstream of each block. This pause occurs in the 13th bit while ZSC is LOW. The nominal pause duration t_p depends on the programmed bit rate for data reception and is shown in Table 16. The total duration of the 13th bit is given by $t_{ZCL} + t_p$.

A similar pause occurs between the first and the second data block. The delay between the first latch enable pulse and the second data block is given by $t_{ZDL2} + t_p$.
The complete start-up timing of the synthesizer interface is illustrated in Fig.13.

Table 15 Synthesizer programming pause

BIT RATE (bit/s)	t_p (clocks)	t_p (μs)
512	119	1549
1200	33	430
2400	1	13

8.24 Serial microcontroller interface

The PCD5002 has an I²C-bus serial microcontroller interface capable of operating at 400 kbits/s.
The PCD5002 is a slave transceiver with a 7-bit I²C-bus address 39 (bits A6 to A0 = 0100111).

Data transmission requires 2 lines: SDA (data) and SCL (clock), each with an external pull-up resistor. The clock signal (SCL) for any data transmission must be generated by the external controlling device.

A transmission is initiated by a START condition (S: SCL = 1, SDA = ↓) and terminated by a STOP condition (P: SCL = 1, SDA = ↑).

Data bits must be stable when SCL is HIGH. If there are multiple transmissions, the STOP condition can be replaced with a new START condition.

Data is transferred on a byte basis, starting with a device address and a read/write indicator. Each transmitted byte must be followed by an acknowledge bit A (active LOW). If a receiving device is not ready to accept the next complete byte, it can force a bus wait state by holding SCL LOW.

The general I²C-bus transmission format is illustrated in Fig.7. Formats for master/slave communication are illustrated in Fig.8.

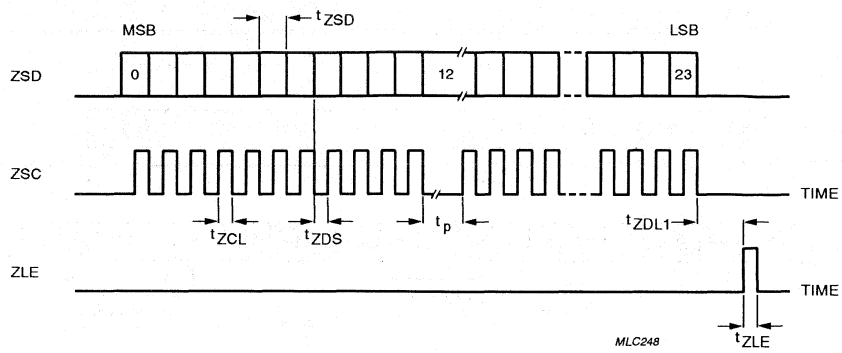


Fig.6 Synthesizer interface timing.

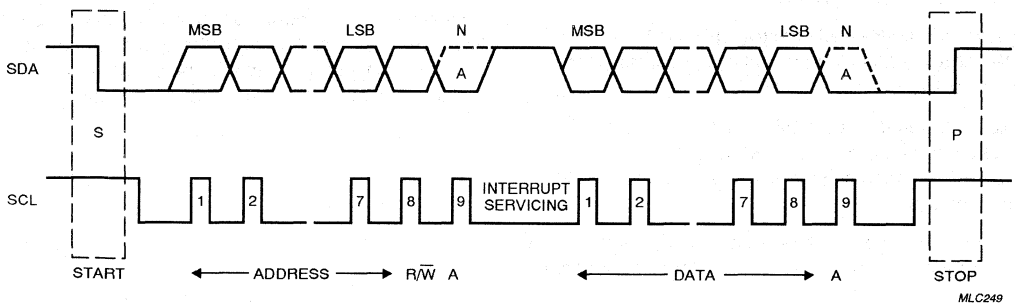
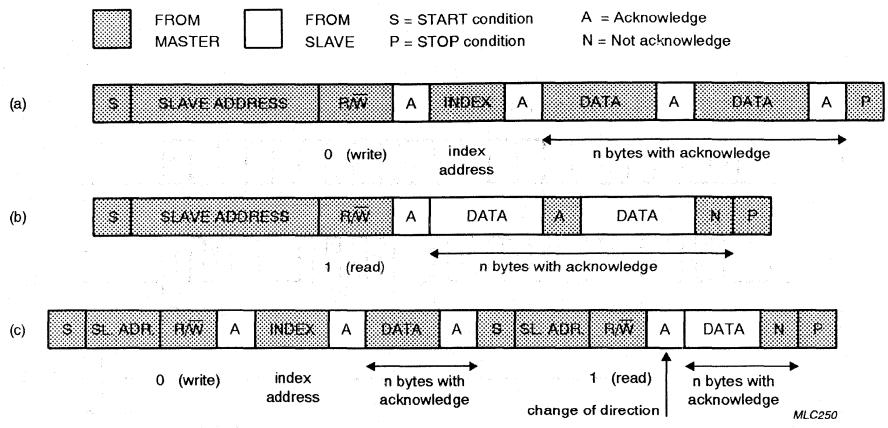


Fig.7 I²C-bus message format.



(a) Master writes to slave.
(b) Master reads from slave.
(c) Combined format (shown: write plus read).

Fig.8 Message types.

8.25 Decoder I²C-bus access

All internal access to the PCD5002 takes place via the I²C-bus interface. For this purpose the internal registers, SRAM and EEPROM have been memory mapped and are accessed via an **index register**. Table 16 shows the index addresses of all internal blocks.

Registers are addressed directly, while RAM and EEPROM are addressed indirectly via address pointers and I/O registers.

It should be noted that the EEPROM memory map is non-contiguous and is organized as a matrix.
The EEPROM address pointer contains both row and column indicators.

Data written to read-only bits will be ignored. Values read from write-only bits are undefined and must be ignored.

Each I²C-bus write message to the PCD5002 must start with its slave address, followed by the index address of the memory element to be accessed. An I²C-bus read message uses the last written index address as a data source. The different I²C-bus message types are shown in Fig.8.

As a slave the PCD5002 cannot initiate bus transfers by itself. To prevent an external controller from having to monitor the operating status of the decoder, all important events generate an external interrupt on output INT.

Table 16 Index register

ADDRESS(1)	REGISTER FUNCTION	ACCESS
00H	status	R
00H	control	W
01H	real time clock: seconds	R/$\overline{W}$
02H	real time clock: $^1/_{100}$ second	R/$\overline{W}$
03H	alert cadence	W
04H	alert set-up	W
05H	periodic interrupt modulus	W
05H	periodic interrupt counter	R
06H	RAM write address pointer	R
07H	EEPROM address pointer	R/$\overline{W}$
08H	RAM read address pointer	R/$\overline{W}$
09H	RAM data output	R
0AH	EEPROM data input/output	R/$\overline{W}$
0BH to 0FH	unused	note 2

Notes

1. The index register only uses the least significant nibble, the upper 4 bits are ignored.
2. Writing to registers 0B to 0F has no effect, reading produces meaningless data.

8.26 External interrupt

The PCD5002 can signal events to an external controller via an interrupt signal at output INT. The interrupt polarity is programmable via SPF programming. The interrupt source is shown in the status register.

Interrupts are generated by the following events (more than one event is possible);

- Call data available for output (bit D2)
- SRAM pointers becoming equal (bit D3)
- Expiry of periodic time-out (bit D7)
- Expiry of alert time-out (bit D4)
- Change of state in out-of-range indicator (bit D5)
- Change of state in battery-low indicator or in receiver control output RXE (bit D6).

Immediate interrupts are generated by status bits D3, D4, D6 (RXE monitoring) and D7. Bits D2, D5 and D6 (BAT monitoring) generate interrupts as soon as the receiver is disabled (RXE = 0).

When call data is available (D2 = 1) but the receiver remains switched on, an interrupt is generated at the next sync word position.

The interrupt output INT is reset after completion of a status read operation.

8.27 Status/Control register

The status/control register consists of two independent registers, one for reading (status) and one for writing (control).

The status register shows the current operating condition of the decoder and the cause(s) of an external interrupt. The control register activates/deactivates certain functions. Tables 17 and 18 show the bit allocations of both registers.

All status bits will be reset after a status read operation except for the out-of-range, battery-low and receiver enable indicator bits (see note 1 to Table 17).

Table 17 Status register (00H; read)

BIT[1]	VALUE	DESCRIPTION
D1 and D0	0 0	no new call data
	0 1	new call received (POCSAG or APOC-1)
	1 0	continuous decoding data available
	1 1	batch zero data available (APOC-1)
D3 and D2	0 0	no data to be read (default after reset)
	0 1	RAM read/write pointers different; data to be read
	1 0	RAM read/write pointers equal; no more data to read
	1 1	RAM buffer full or overflow
D4	1	alert timeout expired
D5	1	out-of-range
D6	1	BAT input HIGH or RXE output active (selected by control bit D2)
D7	1	periodic timer interrupt

Note

1. After a status read operation bits D3, D4 and D7 are always reset, bits D1 and D0 only when no second call is pending. D2 is reset when the RAM is empty (read and write pointers equal).

Table 18 Control register (00H; write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	1	forced call termination (automatically reset after termination)
D1	1	EEPROM programming enable
D2	0	BAT input selected for monitoring (status bit D6)
	1	RXE output selected for monitoring (status bit D6)
D3	1	receiver continuously enabled (RXE = 1, ROE = 1)
D4	0	decoder in OFF status (while DON = 0)
	1	decoder in ON status
D5 to D7	X	not used: ignored when written

8.28 Pending interrupts

A secondary status register is used for storing status bits of pending interrupts. This occurs;

- When a new call is received while the previous one was not yet acknowledged by reading the status register
- When an interrupt occurs during a status read operation.

After completion of the status read the primary register is loaded with the contents of the secondary register, which is then reset. An immediate interrupt is then generated, output INT becoming active 1 decoder clock cycle after it was reset following the status read.

It should be noted that in the event of multiple pending calls, only the status bits of the last call are retained.

8.29 Out-of-range indication

The out-of-range condition occurs when entering the fade recovery or carrier-off mode in POCSAG, or transmitter off or carrier detect mode in APOC-1. This condition is reflected in bit D5 of the status register. The out-of-range condition is reset when either preamble or a valid sync word is detected.

The out-of-range bit (D5) in the status register is updated each time the receiver is disabled (RXE $\downarrow$ 0). Every change of state in bit D5 generates an interrupt.

8.30 Real time clock

The PCD5002 provides a periodic reference pulse at output REF. The frequency of this signal can be selected by SPF programming;

- 32768 Hz
- 50 Hz (square-wave)
- 2 Hz
- $1/60$ Hz.

The 32768 Hz signal does not have a fixed period, it consists of 32 pulses distributed over 75 main oscillator cycles at 76.8 kHz. The timing is illustrated in Fig.14.

When programmed for $1/60$ Hz (1 pulse per minute) the pulse at output REF is held off while the receiver is enabled.

Except for the 50 Hz frequency the pulse width t_{RFP} is equal to one decoder clock period.

The real time clock counter runs continuously irrespective of the operating condition of the PCD5002. It contains a **seconds register** (maximum 59) and a **$1/100$ second register** (maximum 99), which can be read from or written to via the I²C-bus. The bit allocation of both registers is shown in Tables 19 and 20.

Table 19 Real time clock; seconds register (01H; read/write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	–	1 s
D1	–	2 s
D2	–	4 s
D3	–	8 s
D4	–	16 s
D5	–	32 s
D6	X	not used: ignored when written, undetermined when read
D7	X	not used: ignored when written, undetermined when read

Table 20 Real time clock; $1/100$ second register (02H; read/write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	–	0 01 s
D1	–	0.02 s
D2	–	0.04 s
D3	–	0.08 s
D4	–	0.16 s
D5	–	0.32 s
D6	–	0.64 s
D7	X	not used: ignored when written, undetermined when read

8.31 Periodic interrupt

A periodic interrupt can be realised with the periodic interrupt counter. This 8-bit counter is incremented every $1/100$ s and produces an interrupt when it reaches the value stored in the periodic interrupt modulus register. The counter register is then reset and counting continues.

Operation is started by writing a non-zero value to the modulus register. Writing a zero will stop interrupt generation immediately and will halt the periodic interrupt counter after 2.55 s.

The modulus register is write-only, the counter register is read only. Both registers have the same index address (05H).

8.32 Received call delay

Call reception (detection of an enabled RIC) causes both the periodic interrupt modulus and the counter register to be reset.

Since the periodic interrupt counter runs for another 2.55 s after a reset, the received call delay (in $1/100$ s units) can be determined by reading the counter register.

Table 21 Alert set-up register (04H; write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	0	call alert via cadence register
	1	POCSAG call alert (pattern selected by D7 and D6)
D1	0	LOW level acoustic alert (ATL), pulsed vibrator alert (25 Hz)
	1	HIGH level acoustic alert (ATL + ATH), continuous vibrator alert
D2	0	normal alerts (acoustic and LED)
	1	warbled alerts: 16 Hz (LED: on/off, ATL/ATH: alternate f_{AWH}, f_{AWL})
D3	1	acoustic alerts enable (ATL, ATH)
D4	1	vibrator alert enabled (VIB)
D5	1	LED alert enabled (LED)
D7 and D6[1]	0 0	POCSAG alert pattern FC = 00, see Fig.9 (a)
	0 1	POCSAG alert pattern FC = 01, see Fig.9 (b)
	1 0	POCSAG alert pattern FC = 10, see Fig.9 (c)
	1 1	POCSAG alert pattern FC = 11, see Fig.9 (d)

Note

1. Bits D7 and D6 correspond to function bits 20 and 21 respectively in the address code-word, which designate the POCSAG call type as shown in Table 1.

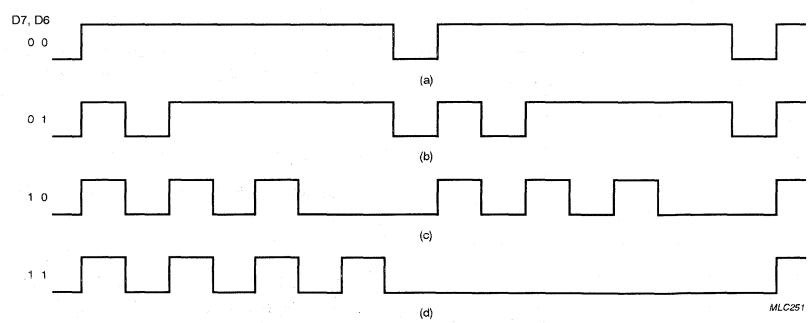


Fig.9 POCSAG alert patterns.

8.33 Alert generation

The PCD5002 is capable of controlling 3 different alert transducers, acoustic beeper (HIGH and LOW level), LED and vibrator motor. The associated outputs are ATH/ATL, LED and VIB respectively. ATL is an open-drain output capable of directly driving an acoustic alerter via a resistor. The other outputs require external transistors.

Each alert output can be individually enabled via the alert set-up register. Alert level and warble can be separately selected. The alert pattern can either be standard POCSAG or determined via the alert cadence register. Direct alert control is possible via input ALC.

The alert set-up register is shown in Table 21.

Standard POCSAG alerts can be selected by setting bit D0 in the alert set-up register, bits D6 and D7 determining the alert pattern used.

8.34 Alert cadence register (03H; write)

When not programmed for POCSAG alerts (alert set-up register bit D0 = 0), the 8-bit alert cadence register determines the alert pattern. Each bit represents a 62.5 ms time slot, a logic 1 activating the enabled alert transducers. The bit pattern is rotated with the MSB (bit D7) being output first and the LSB (bit D0) last.

When the last time slot (bit D0) is initiated an interrupt is generated to allow loading of a new pattern. When the pattern is not changed it will be repeated. Writing a zero to the alert cadence register will halt alert generation within 62.5 ms.

8.35 Acoustic alert

Acoustic alerts are generated via outputs ATL and ATH. For LOW level alerts only ATL is active, while for HIGH level alerts ATH is also active. ATL is driven in counter phase with ATH.

The alert level is controlled by bit D1 in the alert set-up register.

When D1 is reset, for standard POCSAG alerts (D0 = 1) a LOW level acoustic alert is generated during the first 4 s (ATL), followed by 12 s at HIGH level (ATL + ATH). When D1 is set, the full 16 s are at HIGH level. An interrupt is generated after the full alert time has elapsed (indicated by bit D4 in the status register).

When using the alert cadence register, D1 would normally be updated by external control when the alert time-out interrupt occurs at the start of the 8th cadence time slot. Since D1 acts immediately on the alert level, it is advisable to reset the last bit of the previous pattern to prevent unwanted audible level changes.

8.36 Vibrator alert

The vibrator output (VIB) is activated continuously during a standard POCSAG alert or whenever the alert cadence register is non-zero.

Two alert levels are supported, LOW level (25 Hz square-wave) and HIGH level (continuous). The vibrator level is controlled by bit D1 in the alert set-up register.

8.37 LED alert

The LED output pattern corresponds either to the selected POCSAG alert or to the contents of the alert cadence register. No equivalent exists for HIGH/LOW level alerts.

8.38 Warbled alert

When enabled, by setting bit D2 in the alert set-up register, the signals on outputs ATL, ATH and LED are warbled with a 16 Hz modulation frequency. Output LED is switched on and off at the modulation rate, while outputs ATL and ATH switch between f_{AWH} and f_{AWL} alerter frequencies.

8.39 Direct alert control

A direct alert control input (ALC) is available for generating user alarm signals (e.g. battery-low warning). A HIGH level on input ALC activates all enabled alert outputs, overruling any ongoing alert patterns.

8.40 Alert priority

Generation of a standard POCSAG alert (D0 = 1) overrides any alert pattern in the alert cadence register. After completion of the standard alert, the original cadence is restarted from its last position. The alert set-up register will now contain the settings for the standard alert.

The highest priority has been assigned to the alert control input (ALC). All enabled alert outputs will be activated while ALC is set. Outputs are activated/deactivated in synchrony with the decoder clock. Activation requires an extra delay of 1 clock when no alerts are being generated.

When input ALC is reset, acoustic alerting does not cease until the current output frequency cycle has been completed.

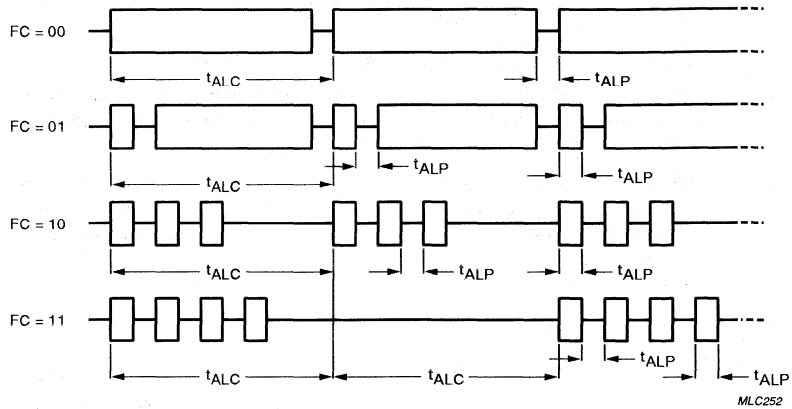


Fig.10 POCSAG alert timing.

8.41 Cancelling alerts

Standard POCSAG alerts (manual or automatic) are cancelled by resetting bit D0 in the alert set-up register. User defined alerts are cancelled by writing a zero to the alert cadence register. Any ongoing alert is cancelled when a reset pulse is applied to input RST.

8.42 Automatic POCSAG alerts

Standard alert patterns have been defined for each POCSAG call type, as indicated by the function bits in the address code-word (see Table 1). The timing of these alert patterns is shown in Fig.10. After completion of the full 16 s alert period an interrupt is generated by status bit D4.

When enabled by SPF programming (SPF byte 03, bit D2) standard POCSAG alerts will be automatically generated at outputs ATL, ATH, LED and VIB upon call reception. The alert pattern matches the call type as indicated by the function bits in the received address code-word.

The original settings of the alert set-up register will be lost. Bit D0 is reset after completion of the alert.

8.43 SRAM access

The on-chip SRAM can hold up to 96 bytes of call data. Each call consists of a call header (3 bytes), message data blocks (3 bytes per code-word) and a call terminator (3 bytes).

The RAM is filled by the decoder and can be read via the I^2C-bus interface. The RAM is accessed indirectly by a read address pointer and a data output register. A write address pointer indicates the position of the last message byte stored.

Status register bit D2 is set when the read and write pointers are different. It is reset only when the SRAM pointers become equal during reading, i.e. when the RAM becomes empty.

Status bit D3 is set when the read and write pointers become equal. This can be due to a RAM empty or a RAM full condition. It is reset after a status read operation.

Interrupts are generated as follows;

- When status bit D2 is set and the receiver is disabled (RXE = 0); data is available for reading
- Immediately when status bit D3 is set: RAM is either empty (status bit D2 = 0) or full (status bit D2 = 1).

To avoid loss of data due to RAM overflow at least 3 bytes of data must be read during reception of the code-word following the 'RAM full' interrupt.

8.44 RAM write address pointer (06H; read)

The RAM write address pointer is automatically incremented during call reception, because the decoder writes each data byte to RAM. The RAM write address pointer can only be read. Values range from 00H to 5FH. Bit D7 (MSB) is not used and its value is undefined when read. When a call data byte is written to location 5FH, the write address pointer wraps around to 00H. This does not necessarily imply a RAM full condition.

8.45 RAM read address pointer (08H; read/write)

The RAM read address pointer is automatically incremented after reading a data byte via the RAM output register.

The RAM read address pointer can be accessed for reading and writing.

The values range from 00H to 5FH. When at 5FH a read operation will cause wrapping around to 00H. Bit D7 (MSB) is not used; it is ignored when written to and undefined when read from.

8.46 RAM data output register (09H; read)

The RAM data output register contains the byte addressed by the RAM read address pointer and can only be read. Each read operation causes an increment of the RAM read address pointer.

8.47 EEPROM access

The EEPROM is intended for storage of user addresses (RICs), sync words and special programmed function (SPF) bits representing the decoder configuration.

The EEPROM can store 48 bytes of information and is organized as a matrix of 8 rows by 6 columns.
The EEPROM is accessed indirectly via an address pointer and a data I/O register.

The EEPROM is protected against inadvertent writing by means of the programming enable bit in the control register (bit D1).

The EEPROM memory map is non-contiguous. Figure 11 shows both the EEPROM organization and the access method.

Identifier locations contain RICs or sync words. A total of 20 unassigned bytes are available for general purpose storage.

8.48 EEPROM address pointer (07H; read/write)

An EEPROM location is addressed via the EEPROM address pointer. It is incremented automatically each time a byte is read from or written to via the EEPROM data I/O register.

The EEPROM address pointer contains two counters for the row and the column number. Bits D2 to D0 contain the column number (0 to 5) and bits D5 to D3 the row number (0 to 7). Bits D7 and D6 of the address pointer are not used. Data written to these bits will be ignored, while their values are undefined when read.

The column and row counters are connected in series. Upon overflow of the column counter (column = 5) the row counter is automatically incremented and the column counter wraps to 0. On overflow the row counter wraps from 7 to 0.

8.49 EEPROM data I/O register (0AH; read/write)

The byte addressed by the EEPROM address pointer can be written to or read from via the EEPROM data I/O register. Each access automatically increments the EEPROM address pointer.

8.50 EEPROM access limitations

Since the EEPROM address pointer is used during data decoding, the EEPROM may not be accessed while the receiver is active (RXE = 1). It is advisable to switch to the OFF state before accessing the EEPROM.

The EEPROM cannot be written to unless the EEPROM programming enable bit (bit D1) in the control register is set.

For writing a minimum programmed supply voltage (V_{PG}) is required (2.5 V typ.). The programmed supply current (I_{PG}) required during writing is approximately 500 μA.

8.51 EEPROM read operation

EEPROM read operations must start at a valid address in the non-contiguous memory map. Single byte or block reads are permitted.

8.52 EEPROM write operation

EEPROM write operations must always take place in blocks of 6 bytes, starting at the beginning of a row. Programming a single byte will reset the other bytes in the same row. Modifying a single byte in a row requires re-writing the unchanged bytes with their old contents.

After writing each block a pause of 7.5 ms (max.) is required to complete the internal programming operation. During this time the external microcontroller may generate an I²C-bus STOP condition. If another I²C-bus transfer is initiated the decoder will pull SCL LOW during this pause.

After writing the EEPROM programming enable bit (D1) in, the control register must be reset.

8.53 Invalid write address

When an invalid write address is used, the column counter bits (D2 to D0) are forced to zero before being loaded into the address pointer. The row counter bits are used normally.

8.54 Incomplete programming sequence

A programming sequence may be aborted by an I²C-bus STOP condition. The EEPROM programming enable bit (D1) in the control register must then be reset.

Any bytes received from the last 6-byte block will be ignored and the contents of this (incomplete) EEPROM block will remain unchanged.

8.55 Unused EEPROM locations

A total of 20 EEPROM bytes are available for general purpose storage (see Table 22).

Table 22 Unused EEPROM addresses

ROW	HEX
0	04 and 05(1)
5	28 to 2D
6	30 to 35
7	38 to 3D

Note

1. When using bytes 04H and 05H, care must be taken to preserve the SPF information stored in bytes 00H to 03H.

8.56 Special programmed function allocation

The SPF bit allocation in the EEPROM is shown in Tables 23 to 27. The SPF bits are located in row 0 of the EEPROM and occupy 4 bytes.

Bytes 04H and 05H are not used and are available for general purpose storage.

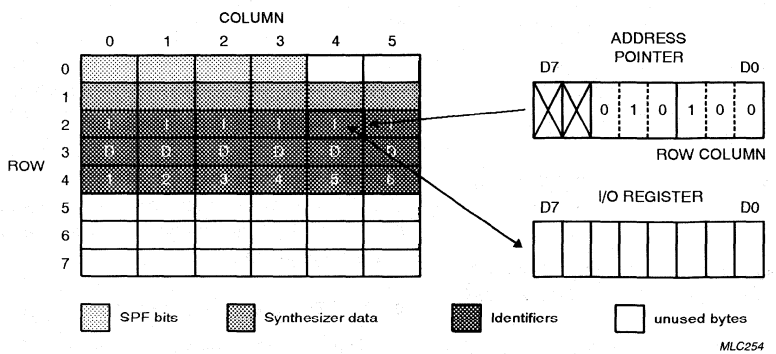


Fig.11 EEPROM organization and access.

Table 23 Special programmed functions (EEPROM address 00H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	0	POCSAG decoding enabled
	1	APOC-1 decoding enabled
D1	0	cycle length: 5 batches
	1	cycle length: 15 batches
D5 to D2 (MSB: D5)	0 to 4	batch number (D1 = 0, MSB is ignored)
	0 to 14	batch number (D1 = 1)
D6	1	continuous data decoding enabled
D7	1	received data inversion enabled

Table 24 Special programmed functions (EEPROM address 01H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	5 ms receiver establishment time (nominal); note 1
	0 1	10 ms
	1 0	15 ms
	1 1	30 ms
D3 and D2	0 0	20 ms oscillator establishment time (nominal); note 1
	0 1	30 ms
	1 0	40 ms
	1 1	50 ms
D5 and D4	0 0	512 bits/s received bit rate
	0 1	1024 bits/s (not used in POCSAG)
	1 0	1200 bits/s
	1 1	2400 bits/s
D6	1	synthesizer interface enabled (programming at switch-on)
D7	1	voltage converter enabled

Note

1. Since the exact establishment time is related to the programmed bit rate, Table 25 shows the values for the various bit rates.

Table 25 Establishment time as a function of bit rate

NOMINAL ESTABLISHMENT TIME	ACTUAL ESTABLISHMENT TIME			
	512 (bits/s)	1024 (bits/s)	1200 (bits/s)	2400 (bits/s)
5 ms	5.9 ms (3 bits)	5.9 ms (6 bits)	5 ms (6 bits)	5 ms (12 bits)
10 ms	11.7 ms (6 bits)	11.7 ms (12 bits)	10 ms (12 bits)	10 ms (24 bits)
15 ms	15.6 ms (8 bits)	15.6 ms (16 bits)	16.7 ms (20 bits)	16.7 ms (40 bits)
20 ms	23.4 ms (12 bits)	23.4 ms (24 bits)	20 ms (24 bits)	20 ms (48 bits)
30 ms	31.2 ms (16 bits)	31.2 ms (32 bits)	26.7 ms (32 bits)	26.7 ms (64 bits)
40 ms	39.1 ms (20 bits)	39.1 ms (40 bits)	40 ms (48 bits)	40 ms (96 bits)
50 ms	46.9 ms (24 bits)	46.9 ms (48 bits)	53.3 ms (64 bits)	53.3 ms (128 bits)

Table 26 Special programmed functions (EEPROM address 02H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	not used
D1	X	not used
D3 and D2	0 0	32768 Hz real time clock reference
	0 1	50 Hz square wave
	1 0	2 Hz
	1 1	$1/60$ Hz
D4	1	signal test mode enabled (REF and INT outputs)
D5	0	burst error correction enabled
D7 and D6	00	30 s (+ 0.5 s max.) transmitter off timeout
	01	60 s (+ 1 s max.)
	10	120 s (+ 2 s max.)
	11	240 s (+ 4 s max.)

Table 27 Special programmed functions (EEPROM address 03H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	2048 Hz acoustic alerter frequency
	0 1	2731 Hz
	1 0	4096 Hz
	1 1	3200 Hz
D2	1	automatic POCSAG alert generation enabled
D3	X	not used
D4	X	not used
D5	X	not used
D6	0	INT output polarity: active LOW
	1	INT output polarity: active HIGH
D7	X	not used

8.57 Synthesizer programming data

Data for programming a PLL synthesizer via pins ZSD, ZSC and ZLE can be stored in row 1 of the EEPROM. Six bytes are available starting with address 08H.

Data is transferred in two serial blocks of 24 bits each, starting with bit 0 (MSB) of block 1. Any unused bits must be programmed at the beginning of a block.

Table 28 Synthesizer programming data (EEPROM address 08H to 0DH)

ADDRESS (HEX)	BIT (MSB: D7)	DESCRIPTION
08	D7 to D0	bits 0 to 7 of data block 1 (bit 0 is MSB)
09	D7 to D0	bits 8 to 15
0A	D7 to D0	bits 16 to 23
0B	D7 to D0	bits 0 to 7 of data block 2 (bit 0 is MSB)
0C	D7 to D0	bits 8 to 15
0D	D7 to D0	bits 16 to 23

8.58 Identifier storage allocation

Up to 6 different identifiers can be stored in EEPROM for matching with incoming data. The PCD5002 can distinguish two types of identifiers;

- User addresses (RIC)
- User Programmable Sync Words (UPSW)
- Batch zero identifiers
- Continuous data decoding (CDD) sync words.

Identifiers are stored in EEPROM rows 2, 3 and 4. Each identifier location consists of 3 bytes in the same column. The identifier number is equal to the column number + 1.

Each identifier can be individually enabled. The standard POCSAG sync word is always enabled and has identifier number 7.

The identifier type is determined by bits D2 and D0 of identifier byte 3, as shown in Table 31.

Identifiers 1 and 2 always represent RICs or batch zero identifiers. The last 4 identifiers (numbers 3 to 6) can represent any identifier type.

A UPSW represents an unused address and must differ by more than 6 bits from preamble to guarantee detection.

A batch zero identifier marks the start of a new cycle in the APOC-1 protocol. It is only recognized when APOC-1 decoding has been enabled (SPF byte 00, bit D0).

Reception of a CDD sync word initiates continuous data decoding. CDD sync words are only recognized when continuous data decoding has been enabled (SPF byte 00, bit 6).

Table 29 shows the memory locations of the 6 identifiers. The bit allocation per identifier is given in Table 30.

Table 29 Identifier storage allocation (EEPROM address 10H to 25H)

ADDRESS (HEX)	BYTE	DESCRIPTION
10 to 15	1	identifier number 1 to 6
18 to 1D	2	identifier number 1 to 6
20 to 25	3	identifier number 1 to 6

Table 30 Identifier bit allocation

BYTE	BIT (MSB: D7)	DESCRIPTION
1	D7 to D0	bits 2 to 9 of POCSAG code-word (RIC or UPSW); notes 1 and 2
2	D7 to D0	bits 10 to 17
3	D7 and D6	bits 18 and 19
	D5	frame number bit FR3 (RIC); note 3
	D4	frame number bit FR2 (RIC)
	D3	frame number bit FR1 (RIC)
	D2	identifier type selection (0 = UPSW, 1 = RIC); note 4
	D1	identifier enable (1 = enabled)
	D0	batch zero ID/continuous decoding (1 = enabled)

Notes

1. The bit numbering corresponds with the numbering in a POCSAG code-word; bit 1 is the flag bit (0 = address, 1 = message).
2. A UPSW needs 18 bits to be matched for successful identification. Bit 1 (MSB) must be logic 0. Bits 2 to 19 contain the identifier bit pattern, they are followed by 2 predetermined random (function) bits and the UPSW is completed by 10 CRC error correction bits and an even-parity bit.
3. Bits FR3 to FR1 (MSB: FR3) contain the 3 least significant bits of the 21-bit RIC.
4. Identifiers 1 and 2 (RIC only) will be disabled by programming bit D2 as logic 0.

Table 31 Identifier types

BYTE 3, BIT D2	BYTE 3, BIT D0	DESCRIPTION
0	0	user programmable sync word (UPSW)
0	1	continuous data decoding (CDD) sync word
1	0	normal user address (RIC)
1	1	batch zero identifier

8.59 Voltage doubler

An on-chip voltage doubler provides an unregulated DC output for supplying an LCD or a low power microcontroller at output V_{PO}. An external ceramic capacitor of 100 nF (typ.) is required between pins CCN and CCP. The voltage doubler is enabled via SPF programming.

8.60 Level-shifted interface

All interface lines are suited for communication with a microcontroller operating from a higher supply voltage. The external device must have a common reference at V_{SS} of the PCD5002.

The reference voltage for the level-shifted interface must be applied to input V_{PR}. If required this could be the on-chip voltage doubler output V_{PO}. When the microcontroller has a separate (regulated) supply it should be connected to V_{PR}.

The level-shifted interface lines are RST, DON, ALC, REF and INT.

The I^2C-bus interface lines SDA and SCL can be level-shifted independently of V_{PR} by the standard external pull-up resistors.

8.61 Signal test mode

A special signal test mode is available for monitoring the performance of a receiver circuit together with the front-end of the PCD5002.

For this purpose the output of the digital noise filter and the recovered bit clock are made available at outputs REF and INT respectively. All synchronization and decoding functions are normally active.

The signal test mode is activated/deactivated by SPF programming.

9 OPERATING INSTRUCTIONS

9.1 Reset conditions

When the PCD5002 is reset by applying a HIGH level to input RST, the condition of the decoder is as follows;

- OFF status (irrespective of DON input level)
- REF output frequency 32768 Hz
- All internal counters reset
- Status/control register reset
- INT output at LOW level
- No alert transducers selected
- LED, VIB and ATH outputs at LOW level
- ATL output high-impedance
- SDA and SCL inputs high-impedance
- Voltage converter disabled.

The programmed functions are activated within t_{RSU} after release of the reset condition (RST LOW). The settings affecting the external operation of the PCD5002 are as follows;

- REF output frequency
- Voltage converter
- INT output polarity
- Signal test mode.

When input DON is HIGH, the decoder starts operating in ON status immediately following t_{RSU}.

9.2 Power-on reset circuit

Input RST has an internal high-ohmic pull-down resistor (nominal 2 MΩ at 2.5 V supply). This can be used together with an external capacitor connected to V_{PR} to create a power-on reset signal.

Since this pull-down resistor varies considerably with processing and supply voltage, a more accurate reset duration can be realised with an additional external resistor connected to V_{SS}.

9.3 Reset timing

The start-up time for the crystal oscillator may exceed 1 s (typ. 800 ms). It is advisable to apply a reset condition, at least during the first part of this period. The minimum reset pulse duration t_{RST} is 50 μs.

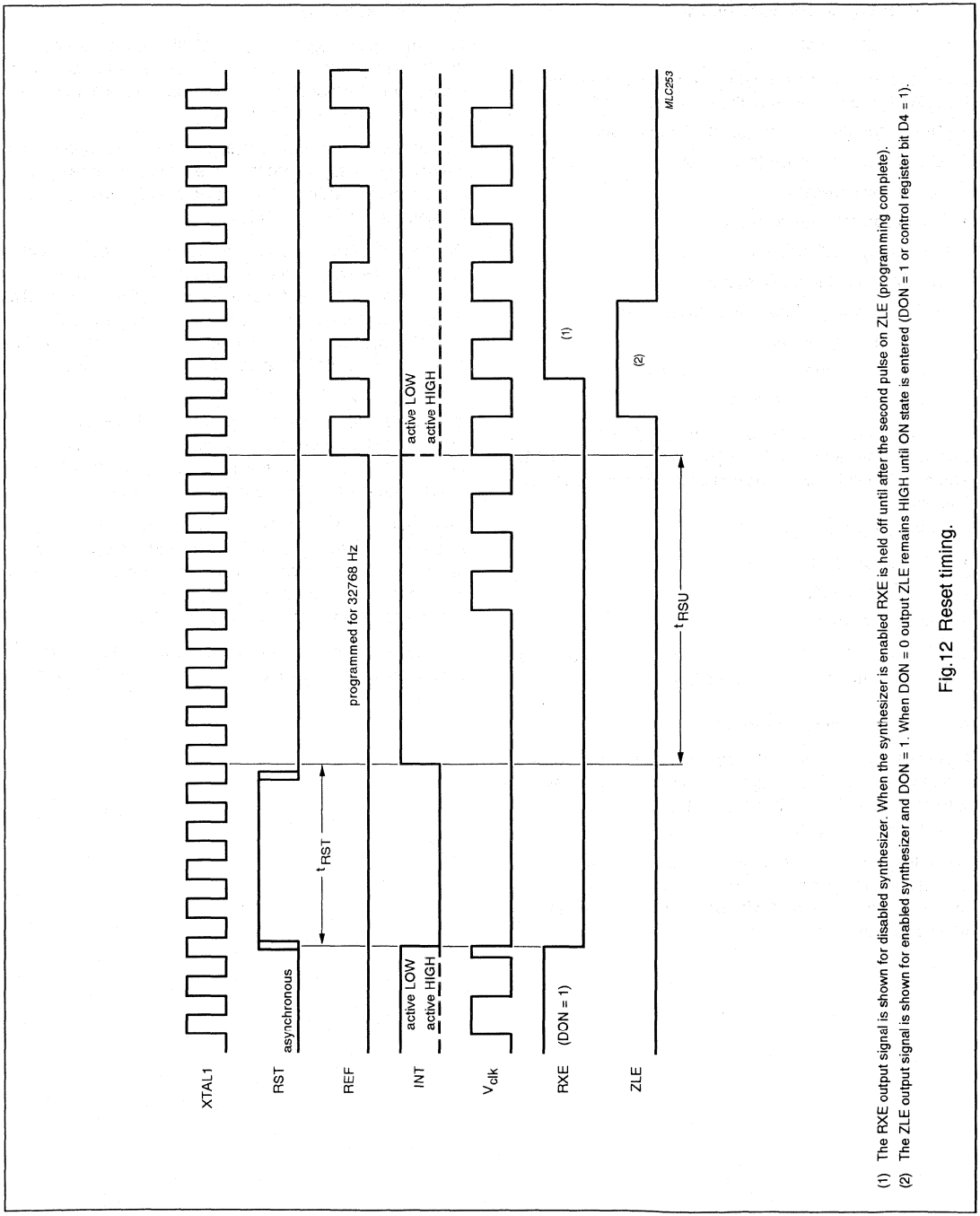
During reset the oscillator is active, but clock signals are inhibited internally. Once the reset condition is released the end of the oscillator start-up period can be detected by a rising edge on output INT.

During a reset the voltage converter clock (V_{clk}) is held at zero. The resulting output voltage drop may cause problems when the external resetting device is powered by the internal voltage doubler. A sufficiently large buffer capacitor connected between output V_{PO} and V_{SS} must be provided to supply the microcontroller during reset. The voltage at V_{PO} will not drop below V_{DD} – 0.7 V.

Immediately after a reset all programmable internal functions will start operating according to a programmed value of 0. During the first 8 full clock cycles (t_{RSU}) all programmed values are loaded from EEPROM.

After reset the receiver outputs RXE and ROE become active immediately, if DON is HIGH and the synthesizer is disabled. When the synthesizer is enabled, RXE and ROE will only become active after the second pulse on ZLE completes the loading of synthesizer data.

The full reset timing is illustrated in Fig.12. The start-up timing including synthesizer programming is illustrated in Fig.13.



(1) The RXE output signal is shown for disabled synthesizer. When the synthesizer is enabled RXE is held off until after the second pulse on ZLE (programming complete).
(2) The ZLE output signal is shown for enabled synthesizer and DON = 1. When DON = 0 output ZLE remains HIGH until ON state is entered (DON = 1 or control register bit D4 = 1).

Fig.12 Reset timing.

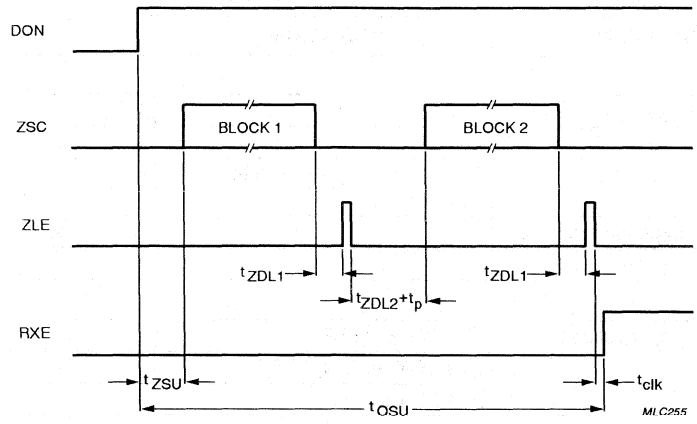


Fig.13 Start-up timing including synthesizer programming.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+7.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	−0.5	+7.0	V
V_n	voltage on pins ALC, DON, RST, SDA and SCL	$V_n \leq 7.0$ V	$V_{SS} - 0.8$	$V_{PR} + 0.8$	V
V_{n1}	input voltage on any other pin	$V_{n1} \leq 7.0$ V	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
P_{tot}	total power dissipation		−	250	mW
P_O	power dissipation per output		−	100	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_{stg}	storage temperature		−55	+125	°C

11 DC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; except where indicated T_{nom} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		1.5	2.7	6.0	V
I_{DD0}	supply current (OFF)	note 1	–	25	40	μA
I_{DD1}	supply current (ON)	DON = V_{DD}; RXE/ROE outputs LOW; note 1	–	50	80	μA
V_{PG}	programming supply voltage		2.5	–	–	V
I_{PG}	programming supply current		–	–	800	μA
Inputs						
V_{IL}	LOW level input voltage	pins RDI and BAT	–	–	$0.3V_{DD}$	V
		pins DON, ALC and RST	–	–	$0.3V_{PR}$	V
		pins SDA and SCL	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	pins RDI and BAT	$0.7V_{DD}$	–	–	V
		pins DON, ALC and RST	$0.7V_{PR}$	–	–	V
		pins SDA and SCL	$0.7V_{DD}$	–	–	V
I_{IL}	LOW level input current	pins RDI, BAT, TS1, TS2, DON, ALC and RST; V_I = V_{SS}; T_{nom}	0	–	−0.5	μA
I_{IH}	HIGH level input current	pins TS1 and TS2; V_i = V_{DD}; T_{nom}	6	–	20	μA
		pins RDI and BAT; V_i = V_{DD}; T_{nom}; RXE = 0	6	–	20	μA
		pins RDI and BAT; V_i = V_{DD}; T_{nom}; RXE = 1	0	–	0.5	μA
		pins DON, ALC and RST; V_i = V_{DD}; T_{nom}	250	500	850	nA
Outputs						
I_{OL}	LOW level output current	pins VIB and LED; V_{OL} = 0.3 V; T_{nom}	80	–	–	μA
		pin ATH; V_{OL} = 0.3 V; T_{nom}	250	–	–	μA
		pins INT and REF; V_{OL} = 0.3 V; T_{nom}	80	–	–	μA
		pins ZSD, ZSC and ZLE; V_{OL} = 0.3 V; T_{nom}	70	–	–	μA
		pin ATL; V_{OL} = 1.2 V; T_{nom}; note 2	13	27	55	mA
		pins ROE and RXE; V_{OL} = 0.3 V; T_{nom}	80	–	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{OH}	HIGH level output current	pins VIB and LED; V_{OH} = 0.7 V; T_{nom}	−0.6	–	−2.4	mA
		pin ATH; V_{OH} = 0.7 V; T_{nom}	−3.0	–	−11.0	mA
		pins INT and REF; V_{OH} = 2.4 V; T_{nom}	−80	–	–	μA
		pins ZSD, ZSC and ZLE; V_{OH} = 2.4 V; T_{nom}	−60	–	–	μA
		pin ATL high-impedance; note 3	–	–	−0.5	μA
		pins ROE and RXE; V_{OH} = 2.4 V; T_{nom}	−600	–	–	μA

Notes

1. Inputs: SDA and SCL pulled up to V_{DD}; all other inputs connected to V_{SS}.
   Outputs: RXE and ROE logic 0; REF: $f_{ref} = 1/60$ Hz; all other outputs open-circuit.
   Oscillator: no crystal; external clock f_{osc} = 76800 Hz; amplitude: V_{SS} to V_{DD}.
   Voltage convertor disabled (SPF byte 01, bit D7 = 0; see Table 24).
2. Maximum output current is subject to absolute maximum ratings per output (see Chapter "Limiting values").
3. When ATL (open-drain output) is not activated it is high impedance.

12 DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 2.7 V; V_{SS} = 0 V; $V_{PR} = V_{PO}$; T_{amb} = −25 to +70 °C; C_s = 100 nF; voltage converter enabled.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.5	–	3.0	V
$V_{PO(0)}$	output voltage; no load	V_{DD} = 2.7; I_{PO} = 0	–	5.4	–	V
V_{PO}	output voltage	V_{DD} = 2 V; I_{PO} = −250 μA	3.0	3.5	–	V
I_{PO}	output current	V_{DD} = 2 V; V_{PO} = 2.7 V	−400	−650	–	μA
		V_{DD} = 3 V; V_{PO} = 4.5 V	−650	−900	–	μA

13 OSCILLATOR CHARACTERISTICS

Quartz crystal type: MX-1V or equivalent.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 35 kΩ; C_L = 8 pF; C_0 = 1.4 pF; C_1 = 1.5 fF; TC = -35×10^{-6}/K.
Maximum overall tolerance: $\pm 200 \times 10^{-6}$ (includes: cutting, temperature, aging) for POCSAG, $\pm 55 \times 10^{-6}$ for APOC-1 (transmitter off mode).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{XO}	output capacitance XTAL2		–	10	–	pF
g_m	oscillator transconductance	V_{DD} = 1.5 V	6	12	–	μA/V

14 AC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = 2.7 V; T_{amb} = 25 °C;. f_{osc} = 76800 Hz.

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock						
T_{clk}	system clock period	f_{osc} = 76800 Hz	–	13.02	–	µs
Call alert frequencies						
f_{AL}	alerter frequency (SPF byte 03H)	D1 = 0; D0 = 0	–	2048	–	Hz
		D1 = 0; D0 = 1	–	2731	–	Hz
		D1 = 1; D0 = 0	–	3200	–	Hz
		D1 = 1; D0 = 1	–	4096	–	Hz
f_{AW}	warbled alert; modulation frequency	alert set-up bit D2 = 1; outputs ATL, ATH and LED	–	16	–	Hz
f_{AWH}	warbled alert; high acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL and ATH	–	f_{AL}	–	Hz
f_{AWL}	warbled alert; low acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL and ATH	–	$\frac{1}{2}f_{AL}$	–	Hz
f_{VBP}	pulsed vibrator frequency (square wave)	low level alert	–	25	–	Hz
Call alert duration						
t_{ALT}	alert timeout period		–	16	–	s
t_{ALL}	ATL output timeout period	low level alert	–	4	–	s
t_{ALH}	ATH output timeout period	high level alert	–	12	–	s
t_{VBL}	VIB output timeout period	low level alert	–	4	–	s
t_{VBH}	VIB output timeout period	high level alert	–	12	–	s
t_{ALC}	alert cycle period		–	1	–	s
t_{ALP}	alert pulse duration		–	125	–	ms
Real time clock reference						
f_{ref}	real time clock reference frequency (SPF byte 02H)	D3 = 0; D2 = 0; note 1	–	32768	–	Hz
		D3 = 0; D2 = 1; note 2	–	50	–	Hz
		D3 =1; D2 = 0	–	2	–	Hz
		D3 = 1; D2 = 1	–	$\frac{1}{60}$	–	Hz
t_{RFP}	real time clock reference pulse duration	all reference frequencies except 50 Hz (square wave)	–	13.02	–	µs

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver control						
t_{RXT}	RXE and ROE transition time	C_L = 5 pF	–	100	–	ns
t_{RXON}	RXE establishment time (nominal values: actual duration is bit rate dependent); see Table 21 (SPF byte 01H)	D1 = 0; D0 = 0	–	5	–	ms
		D1 = 0; D0 = 1	–	10	–	ms
		D1 = 1; D0 = 0	–	15	–	ms
		D1 = 1; D0 = 1	–	30	–	ms
t_{ROON}	ROE establishment time (nominal values: actual duration is bit rate dependent), see Table 21 (SPF byte 01H)	D3 = 0; D2 = 0	–	20	–	ms
		D3 = 0; D2 = 1	–	30	–	ms
		D3 =1; D2 = 0	–	40	–	ms
		D3 = 1; D2 = 1	–	50	–	ms
I²C-bus interface						
f_{SCL}	SCL clock frequency		0	–	100	kHz
t_{LOW}	SCL clock low period		4.7	–	–	µs
t_{HIGH}	SCL clock HIGH period		4.0	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		500	–	–	ns
t_r	SDA and SCL rise time		–	–	1000	ns
t_f	SDA and SCL fall time		–	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs
Reset						
t_{RST}	external reset duration		50	–	–	µs
t_{RSU}	set-up time after reset	oscillator running	–	–	105	µs
t_{OSU}	set-up time after switch-on	oscillator running	–	–	4	ms
Data input						
t_{TDI}	data input transition time		–	–	100	µs
t_{DI1}	data input logic 1 duration		infinite			
t_{DI0}	data input logic 0 duration		infinite			
POCSAG data timing (512 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 0; D4 = 0	–	512	–	bits/s
t_{BIT}	bit duration		–	1.9531	–	ms
t_{CW}	code-word duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POCSAG data timing (1200 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 1; D4 = 0	–	1200	–	bits/s
t_{BIT}	bit duration		–	833.3	–	µs
t_{CW}	code-word duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
POCSAG data timing (2400 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 1; D4 = 1	–	2400	–	bits/s
t_{BIT}	bit duration		–	416.6	–	µs
t_{CW}	code-word duration		–	13.3	–	ms
t_{PA}	preamble duration		240	–	–	ms
t_{BAT}	batch duration		–	226.6	–	ms
APOC-1 batch timing						
t_{SB}	cycle duration	SPF byte 00H; bit D2 = 0 (5 batches)	–	2720	–	bits
		SPF byte 00H; bit D2 = 0 (15 batches)	–	8160	–	bits
Synthesizer control						
t_{ZSU}	synthesizer set-up duration	oscillator running; note 3	1	–	2	bits
f_{ZSC}	output clock frequency	note 4	–	38400	–	Hz
t_{ZCL}	clock pulse duration		–	13.02	–	µs
t_{ZSD}	data bit duration	note 4	–	26.04	–	µs
t_{ZDS}	data bit set-up time		–	13.02	–	µs
t_{ZDL1}	data load enable delay		–	91.15	–	µs
t_{ZLE}	load enable pulse duration		–	13.02	–	µs
t_{ZDL2}	inter block delay		–	117.19	–	µs

Notes

1. 32768 Hz reference signal; 32 pulses per 75 clock cycles, alternately separated by 1 or 2 pulse periods (pulse duration: t_{RFP}). The timing is shown in Fig.14.
2. 50 Hz reference signal: square wave.
3. Duration depends on programmed bit rate; after reset t_{ZSU} = 1.5 bits.
4. Nominal values; pause in 12th data bit (see Table 11).

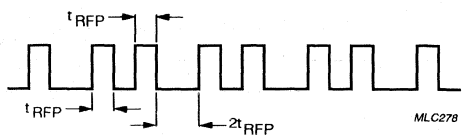


Fig.14 Timing of the 32768 Hz reference signal.

15 APPLICATION INFORMATION

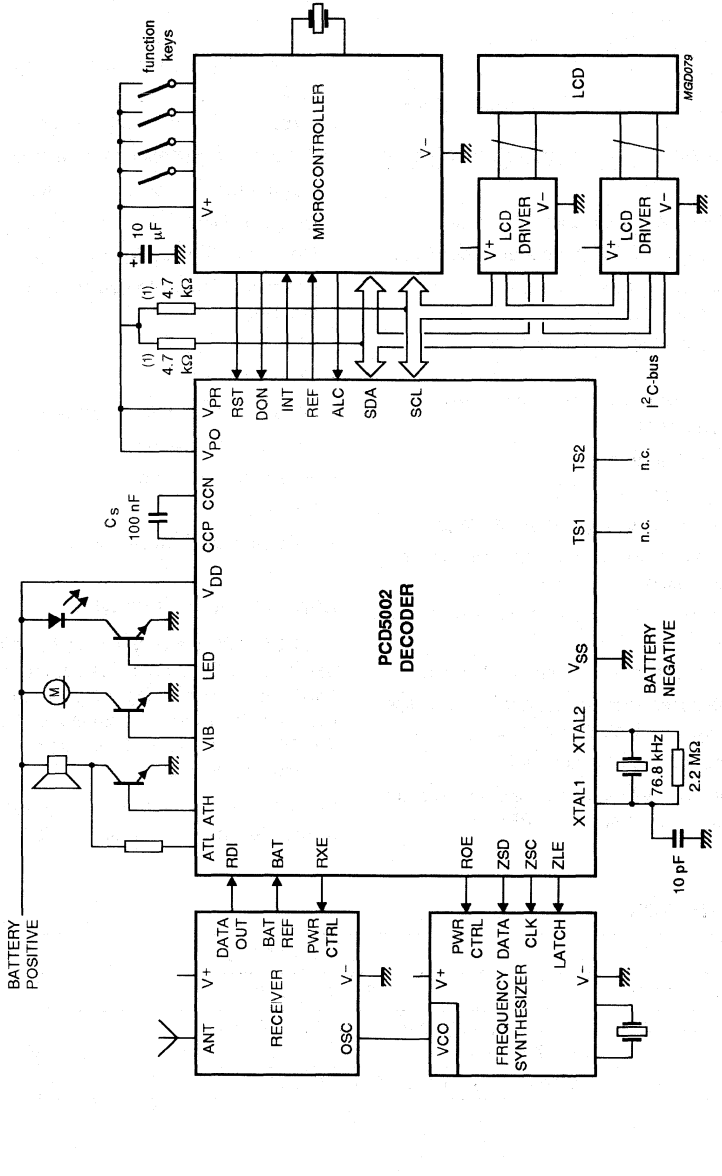


Fig.15 Typical application example (display pager).

(1) Value depends on number of devices attached.

Advanced POCSAG paging decoder PCD5003

FEATURES

- Wide operating supply voltage range: 1.5 to 6.0 V
- Low operating current: 50 μA typ. (ON), 25 μA typ. (OFF)
- Temperature range: −25 to +70 °C
- *"CCIR Radio paging Code No. 1"* (POCSAG) compatible
- 512, 1200 and 2400 bits/s data rates using 76.8 kHz crystal
- Built-in data filter (16-times oversampling) and bit clock recovery
- Advanced ACCESS synchronization algorithm
- 2-bit random and (optional) 4-bit burst error correction
- Up to 6 user addresses (RICs), each with 4 functions/alert cadences
- Up to 6 user address frames, independently programmable
- Standard POCSAG sync word, plus up to 4 user programmable sync words
- Received data inversion (optional)
- Call alert via beeper, vibrator or LED
- 2-level acoustic alert using single external transistor
- Alert control: automatic (POCSAG type), via cadence register or alert input pin
- Separate power control of receiver and RF-oscillator for battery economy
- Synthesizer set-up and control interface (3-line serial)
- On-chip EEPROM for storage of user addresses (RICs), pager configuration and synthesizer data
- On-chip SRAM buffer for message data
- Slave I²C-bus interface to microcontroller for transfer of message data, status/control and EEPROM programming
- Wake-up interrupt for microcontroller, programmable polarity
- Direct and I²C-bus control of operating status (ON/OFF)
- Battery-low indication (external detector)
- Out-of-range condition indication
- Real time clock reference output
- On-chip voltage doubler
- Interfaces directly to UAA2080 and UAA2082 paging receivers.

APPLICATIONS

- Display pagers, basic alert-only pagers
- Information services
- Personal organizers
- Telepoint
- Telemetry/data transmission.

GENERAL DESCRIPTION

The PCD5003 is a very low power POCSAG decoder and pager controller. It supports data rates of 512, 1200 and 2400 bits/s using a single 76.8 kHz crystal. On-chip EEPROM is programmable at 2.5 V minimum supply. The PCD5003 is fast I²C-bus compatible (maximum 400 kbits/s).

The PCD5003 is available in a LQFP32 package and as naked die. The pinning for LQFP32 package is shown in Fig.2.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5003H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
PCD5003U/10	–	film-frame carrier (naked die) 32 pads	–

BLOCK DIAGRAM

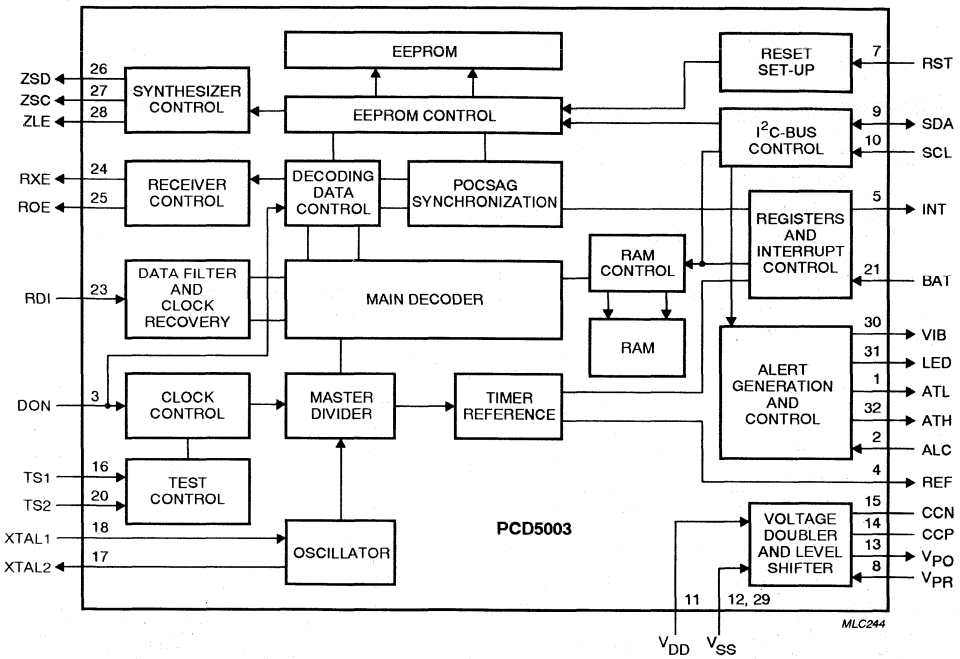


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ATL	1	alert LOW level output
ALC	2	alert control input (normally LOW by internal pull-down)
DON	3	direct ON/OFF input (normally LOW by internal pull-down)
REF	4	real time clock frequency reference output
INT	5	interrupt output
n.c.	6	not connected
RST	7	reset input (normally LOW by internal pull-down)
V_{PR}	8	external positive voltage reference input
SDA	9	I^2C-bus serial data input/output
SCL	10	I^2C-bus serial clock input
V_{DD}	11	main positive supply voltage
V_{SS}	12	main negative supply voltage
V_{PO}	13	voltage converter positive output
CCP	14	voltage converter shunt capacitor (positive side)
CCN	15	voltage converter shunt capacitor (negative side)
TS1	16	test input 1 (normally LOW by internal pull-down)
XTAL2	17	decoder crystal oscillator output
XTAL1	18	decoder crystal oscillator input
n.c.	19	not connected
TS2	20	test input 2 (normally LOW by internal pull-down)
BAT	21	battery sense input
n.c.	22	not connected
RDI	23	received POCSAG data input
RXE	24	receiver circuit enable output
ROE	25	receiver oscillator enable output
ZSD	26	synthesizer serial data output
ZSC	27	synthesizer serial clock output
ZLE	28	synthesizer latch enable output
V_{SS}	29	main negative supply voltage
VIB	30	vibrator motor drive output
LED	31	LED drive output
ATH	32	alert HIGH level output

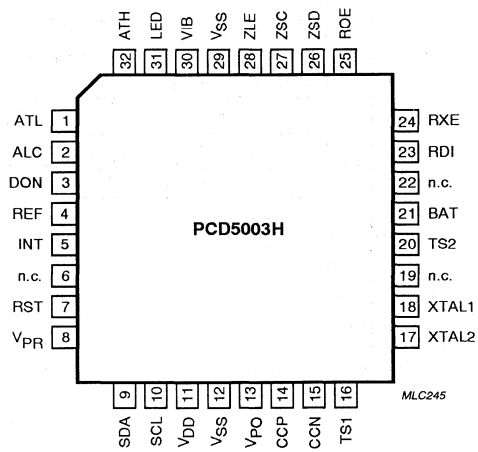


Fig.2 Pin configuration for SOT358-1 (LQFP32).

FUNCTIONAL DESCRIPTION

Introduction

The PCD5003 is a very low power decoder and pager controller specifically designed for use in new generation radio pagers. The architecture of the PCD5003 allows for flexible application in a wide variety of radio pager designs.

The PCD5003 is fully compatible with *"CCIR Radio paging Code No. 1"* (also known as the POCSAG code) operating at data rates of 512, 1200 and 2400 bits/s using a single oscillator crystal of 76.8 kHz.

In addition to the standard POCSAG sync word the PCD5003 is also capable of recognizing up to 4 User Programmable Sync Words (UPSWs). This permits the reception of both private services and POCSAG transmissions via the same radio channel.

Used together with the Philips UAA2080 or UAA2082 paging receiver, the PCD5003 offers a highly sophisticated, miniature solution for the radio paging market. Control of an RF synthesizer circuit is also provided to ease alignment and channel selection.

On-chip EEPROM provides storage for user addresses (Receiver Identity Codes or RICs) and Special Programmed Functions (SPFs), which eliminates the need for external storage devices and interconnection. For other non-volatile storage 20 bytes of general purpose EEPROM are available. The low EEPROM programming voltage makes the PCD5003 well- suited for 'over-the-air' programming/reprogramming.

On request from an external controlling device or automatically (by SPF programming), the PCD5003 will provide standard POCSAG alert cadences by driving a standard acoustic 'beeper'. Non-standard alert cadences may be generated via a cadence register or a dedicated control input.

Via external bipolar transistors the PCD5003 can also produce a HIGH level acoustic alert as well as drive an LED indicator and a vibrator motor.

The PCD5003 contains a low-power, high-efficiency voltage converter (doubler) designed to provide a higher voltage supply to LCD drivers or microcontrollers. In addition, an independent level shifted interface is provided allowing communication to a microcontroller operating at a higher voltage than the PCD5003.

Interface to such an external device is provided by an I^2C-bus which allows received call identity and message data, data for the programming of the internal EEPROM, alert control and pager status information to be transferred between the devices. Pager status includes features provided by the PCD5003 such as battery-low and out-of-range indications.

A selectable low frequency timing reference is provided for use in real time clock functions.

Data synchronization is achieved by the Philips patented ACCESS® algorithm ensuring that maximum advantage is made of the POCSAG code structure particularly in fading radio signal conditions. The algorithm allows for data synchronization without preamble detection whilst minimizing battery power consumption.

Random and (optional) burst error correction techniques are applied to the received data to optimize on call success rate without increasing falsing rate beyond specified POCSAG levels.

When the PCD5003 is used in combination with a microcontroller, communication takes place via an I^2C-bus interface. A dedicated interrupt line minimizes the required microcontroller activity.

The POCSAG paging code

A transmission using the *"CCIR Radio paging Code No. 1"* (POCSAG code) is constructed in accordance with the following rules (see Fig.3).

The transmission is started by sending a **preamble**, consisting of at least 576 continuously alternating bits (10101010...). The preamble is followed by an arbitrary number of batch blocks. Only complete batches are transmitted.

Each **batch** comprises 17 code-words of 32 bits each. The first code-word is a synchronization code-word with a fixed pattern. The **sync** word is followed by 8 frames (0 to 7) of 2 code-words each, containing message information. A code-word in a frame can either be an address, message or idle code-word.

Idle code-words also have a fixed pattern and are used to fill empty frames or to separate messages.

Address code-words are identified by an MSB of logic 0 and are coded as shown in Fig.3. A user address or RIC consists of 21 bits. Only the upper 18 bits are encoded in the address code-word (bits 2 to 19).
The lower 3 bits designate the frame number in which the address is transmitted.

Four different **call types** can be distinguished on each user address. The call type is determined by two function bits in the address code-word (bits 20 and 21), as shown in Table 1.

Alert-only calls only consist of a single address code-word. Numeric and alphanumeric calls have message code-words following the address.

Message code-words are identified by an MSB of logic 1 and are coded as shown in Fig.3. The message information is stored in a 20-bit field (bits 2 to 21). The data format is determined by the call type: 4 bits per digit for numeric messages and 7 bits per (ASCII) character for alphanumeric messages.

Each code-word is protected against transmission errors by 10 CRC check bits (bits 22 to 31) and an even-parity bit (bit 32). This permits correction of maximum 2 random errors or up to 3 errors in a burst of 4 bits (a 4-bit burst error) per code-word.

The POCSAG standard recommends the use of combinations of data formats and function bits, as given in Table 1. Other (non-standard) combinations will be received normally by the PCD5003. Message data is not deformatted.

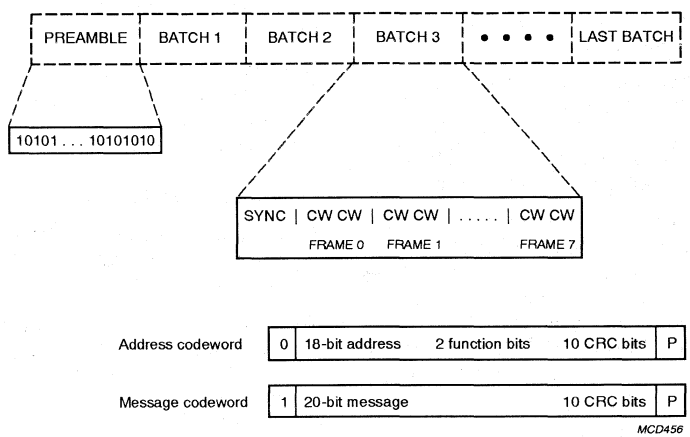


Fig.3 POCSAG code structure.

Table 1 POCSAG call types and function bits

BIT 20 (MSB)	BIT 21 (LSB)	CALL TYPE	DATA FORMAT
0	0	numeric	4-bits per digit
0	1	alert only	–
1	0	alert only	–
1	1	alphanumeric	7-bits per ASCII character

Error correction

Table 2 Error correction

ITEM	DESCRIPTION
Preamble	4 random errors in 31 bits
Synchronization code-word	2 random errors in 32 bits
Address code-word	2 random errors, plus: 4-bit burst errors (optional)
Message code-word	2 random errors, plus: 4-bit burst errors (optional)

In the PCD5003 error correction methods have been implemented as shown in Table 2.

Random error correction is default for both address and message code-words. In addition, burst error correction can be enabled by SPF programming. Up to 3 erroneous bits in a 4-bit burst can be corrected.

The error correction method used is identified in the message data output to the microcontroller, allowing rejection of calls with too many errors.

Operating states

The PCD5003 has 2 operating states:

- ON status
- OFF status.

The operating state is determined by a Direct Control input (DON) and bit D4 in the control register (see Table 3).

Table 3 Truth table for decoder operating status

DON INPUT	CONTROL BIT D4	OPERATING STATUS
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

ON STATUS

In ON status the decoder pulses the receiver and oscillator enable outputs (respectively RXE and ROE) according to the code structure and the synchronization algorithm. Data received serially at the data input (RDI) is processed for call receipt. Reception of a valid paging call is signalled to the microcontroller by means of an interrupt signal. The received address and message data can then be read via the I²C-bus interface.

OFF STATUS

In OFF status the decoder will neither activate the receiver or oscillator enable outputs, nor process any data at the data input. The crystal oscillator remains active to permit communication with the microcontroller.

In both operating states an accurate timing reference is available via the REF output. By SPF programming the signal periodicity may be selected as 32.768 kHz, 50 Hz, 2 Hz or $1/60$ Hz.

BATTERY SAVING

Current consumption is reduced by switching off internal decoder sections whenever the receiver is not enabled.

To further increase battery efficiency, reception and decoding of an address code-word is stopped as soon as the uncorrected address field differs by more than 3 bits from the enabled RICs. If the next code-word must be received again, the receiver is re-enabled thus observing the programmed establishment times t_{RXE} and t_{RDE}.

The current consumption of the complete pager can be minimized by separately activating the RF oscillator circuit (at output ROE) before activating the rest of the receiver. This is possible with the UAA2082 receiver which has external biasing for the oscillator circuit.

Reset

The decoder can be reset by applying a positive pulse on input pin RST. A power-on reset circuit consisting of an RC network can be connected to this input as well. Conditions during and after a reset are described in Chapter "Operating instructions".

Bit rates

The PCD5003 can be configured for data rates of 512, 1200 or 2400 bit/s by SPF programming. These data rates are derived from a single 76.8 kHz oscillator frequency.

Oscillator

The oscillator circuit is designed to operate at 76.8 kHz. Typically, a tuning fork crystal will be used as a frequency source. Alternatively, an external clock signal can be applied to pin XTAL1 (amplitude = V_{DD} to V_{SS}), but a slightly higher oscillator current is consumed. A 2.2 MΩ feedback resistor connected between XTAL1 and XTAL2 is required for proper operation.

To allow easy oscillator adjustment (e.g. by means of a variable capacitor) a 32.768 kHz reference frequency can be selected at output REF by SPF programming.

Input data processing

Data input is binary and fully asynchronous. Input bit rates of 512, 1200 and 2400 bits/s are supported. As a programmable option, the polarity of the received data can be inverted before further processing.

The input data is noise filtered by means of a digital filter. Data is sampled at 16 times the data rate and averaged by majority decision.

The filtered data is used to synchronize an internal clock generator by monitoring transitions. The recovered clock phase can be adjusted in steps of $1/8$ or $1/32$ bit period per received bit.

The larger step size is used when bit synchronization has not been achieved, the smaller when a valid data sequence has been detected (e.g. preamble or sync word).

Synchronization strategy

In ON status the PCD5003 synchronizes to the POCSAG data stream by means of the Philips ACCESS® algorithm. A flow diagram is shown in Fig.4. Where 'sync word' is used, this implies both the standard POCSAG sync word and any enabled User Programmable Sync Word (UPSW).

Several modes of operation can be distinguished depending on the synchronization state. Each mode uses a different method to obtain or retain data synchronization. The receiver and oscillator enable outputs (respectively RXE and ROE) are switched accordingly, with the appropriate establishment times (respectively t_{RXON} and t_{ROON}).

Before comparing received data with preamble, an enabled sync word or programmed user addresses, the appropriate error correction is applied.

Initially, after switching to ON status, the decoder is in **Switch-on** mode. Here the receiver will be enabled for a period up to 3 batches, testing for preamble and sync word. Failure to detect preamble or sync word will cause switching to carrier-off mode.

Detection of preamble switches to **Preamble Receive** mode, in which sync word is looked for. The receiver will remain enabled while preamble is detected. When neither sync word nor preamble is found within 1 batch duration carrier-off mode is entered.

Upon detection of a sync word the **Data Receive** mode is entered. The receiver is activated only during enabled user address frames and sync word periods. When an enabled user address has been detected, the receiver will be kept enabled for message code-word reception until the call termination criteria are met.

During call reception data bytes are stored in an internal SRAM buffer, capable of storing 2 batches of message data.

Messages are transmitted contiguously, only interrupted by sync words at the beginning of each batch. When a message extends beyond the end of a batch, no testing for sync takes place. Instead, a message data transfer will be initiated by an interrupt to the external controller. Data reception continues normally after a period corresponding to the sync word duration.

If any message code-word is found to be uncorrectable, data-fail mode is entered and no data transfer will be attempted at the next sync word position. Instead, a test for sync word will be carried out.

In the **Data Fail** mode message reception continues normally for 1 batch duration. Upon detection of sync word at the expected position the decoder returns to data receive mode. If sync word again fails to appear, batch synchronization is deemed lost. Call reception is then terminated and fade recovery mode is entered.

Fade Recovery mode is intended to scan for sync word and preamble over an extended window (nominal position ±8 bits). This is done for a period of up to 15 batches, allowing recovery of synchronization from long fades in the radio signal. Detection of preamble switches to preamble receive mode, while sync word detection switches to data receive mode. When neither is found within a period of 15 batches, the radio signal is considered lost and carrier-off mode is entered.

The purpose of **Carrier-Off** mode is to detect a valid radio transmission and synchronize to it quickly and efficiently. Because transmissions may start at random, the decoder enables the receiver for 1 code-word in every 18 code-words looking for preamble or sync word. By using a buffer containing 32 bits (n bits from the current scan, 32 – n from the previous scan) effectively every batch bit position can be tested within a continuous transmission of at least 18 batches. Detection of preamble switches to preamble receive mode, while sync word detection switches to data receive mode.

Call termination

Call reception is terminated:

- Upon reception of any address code-word (including Idle code-word) requiring no more than single bit error correction
- In data fail mode, when a sync word is not found at the expected batch position
- When a forced call termination command is received from an external controller.

The last method permits an external controller to stop call reception depending on the number and type of errors which occurred in a call. After a forced call termination the decoder will enter data fail mode.

The type of error correction as well as the call termination conditions are indicated by status bits in the message data output.

Following call termination, transfer of the data received since the previous sync word period is initiated by means of an interrupt to the external controller.

Call data output format

POCSAG call information is stored in the decoder SRAM in blocks of 3 bytes per code-word. Each stored call consists of a call header, followed by message data blocks and concluded by a call terminator. In the event of concatenated messages the call terminator is replaced with the call header of the next message. An alert-only call only has a call header and a call terminator.

The formats of a call header, a message data block and a call terminator are shown in Tables 4, 6 and 8.

A **Call Header** contains information on the last sync word received, the RIC which began call reception and the type of error correction performed on the address code-word.

A **Message Data** block contains the data bits from a message code-word plus the type of error correction performed. No deformatting is done on the data bits: numeric data appear as 4-bit groups per digit, alphanumeric data have a 7-bit ASCII representation.

The **Call Terminator** contains information on the last sync word received, information on the way the call was terminated (forced call termination command, loss of sync word in data fail mode) and the type of error correction performed on the terminating code-word.

Sync word indication

The sync word recognized by the PCD5003 is shown in the call header (bits S3 to S1). The decimal value represents the identifier number in the EEPROM of the UPSW in question. A value of 7 indicates the standard POCSAG sync word.

Error type indication

Table 10 shows how the different types of detected errors are encoded in the call data output format.

A message code-word containing more than a single bit error (bit E3 = 1) may appear as an address code-word (bit M1 = 0) after error correction. In this event the code-word is processed as message data and does not cause call termination.

Data transfer

Data transfer is initiated either during sync word periods or as soon as the receiver is disabled after call termination. If the SRAM buffer is full, data transfer is initiated immediately during the next code-word.

When the PCD5003 is ready to transfer received call data an external interrupt will be generated via output INT. Any message data can be read by accessing the RAM output register via the I^2C-bus interface. Bytes will be output starting from the position indicated by the RAM read pointer.

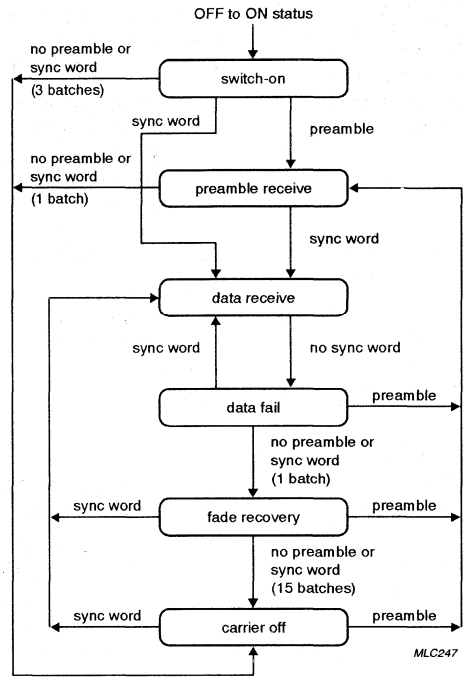


Fig.4 ACCESS® synchronization algorithm.

Table 4 Call Header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	S3	S2	S1	R3	R2	R1	DF
2	0	S3	S2	S1	R3	R2	R1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 5 Call Header bit identification

BITS (MSB to LSB)	IDENTIFICATION
S3 to S1	identifier number of sync word for current batch (7 = standard POCSAG)
R3 to R1	identifier number of user address (RIC)
DF	data fail mode indication (1 = data fail mode); note 1
F0 and F1	function bits of received address code-word (bits 20, 21)
E3 to E1	detected error type; see Table 10; E3 = 0 in a concatenated call header

Note

1. The DF bit in the call header is set:
   a) When the sync word of the batch in which the (beginning of the) call was received, did not match the standard POCSAG or a user-programmed sync word. The sync word identifier (bits S3 to S1) will then be made 0.
   b) When any code-word of a previous call received in the same batch was uncorrectable.

Table 6 Message Data format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	M2	M3	M4	M5	M6	M7	M8	M9
2	M10	M11	M12	M13	M14	M15	M16	M17
3	M18	M19	M20	M21	E3	E2	E1	M1

Table 7 Message Data bit identification

BITS (MSB to LSB)	IDENTIFICATION
M2 to M21	message code-word data bits
E3 to E1	detected error type; see Table 10
M1	message code-word flag

Table 8 Call Terminator format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	FT	S3	S2	S1	0	0	0	DF
2	FT	S3	S2	S1	0	0	0	X
3	X	X	X	X	E3	E2	E1	0

Table 9 Call Terminator bit identification

BITS (MSB to LSB)	IDENTIFICATION
FT	forced call termination (1 = yes)
S3 to S1	identifier number of last sync word
DF	data fail mode indication (1 = data fail mode); note 1
E3 to E1	detected error type; see Table 10; E3 = 0 in a call terminator

Note

1. The DF bit in the call terminator is set:
   a) When any call data code-word in the terminating batch was uncorrectable, while in data receive mode.
   b) When the sync word at the start of the terminating batch did not match the standard POCSAG or a user-programmed sync word, while in data fail mode.

Successful call termination occurs by reception of a valid address code-word with less than 2 bit errors. Unsuccessful termination occurs when sync word is not detected while in data fail mode.

It is generally possible to distinguish these two conditions using the sync word identifier number (bits S3 to S1); the identifier number will be non-zero for correct termination, and zero for sync word failure.

Only when a call is received in data fail mode and the call is terminated before the end of the batch, is it not possible to distinguish unsuccessful from correct termination.

Reception of message data can be terminated at any time by transmitting a forced call termination command to the control register via the I²C-bus. Any call received will then be terminated immediately and data fail mode will be entered.

Receiver and oscillator control

A paging receiver and an RF oscillator circuit can be controlled independently via enable outputs RXE and ROE respectively. Their operating periods are optimized according to the synchronization mode of the decoder. Each enable signal has its own programmable establishment time (see Table 11).

External receiver control and monitoring

An external controller may enable the receiver control outputs continuously via an I²C-bus command, overruling the normal enable pattern. Data reception continues normally. This mode can be left by means of a reset or an I²C-bus command.

External monitoring of the receiver control output RXE is possible via bit D6 in the status register, when enabled via the control register (D2 = 1). Each change of state of output RXE will generate an external interrupt at output INT.

Battery condition input

A logic signal from an external sense circuit signalling battery condition can be applied to the BAT input. This input is sampled each time the receiver is disabled (RXE ↓ 0).

When enabled via the control register (D2 = 0), the condition of input BAT is reflected in bit D6 of the status register. Each change of state of bit D6 causes an external interrupt at output INT.

When using the UAA2080 pager receiver a battery-low condition corresponds to a logic HIGH-level. With a different sense circuit the reverse polarity can be used as well, because every change of state is signalled to an external controller.

After a reset the initial condition of the battery-low indicator in the status register is zero.

Table 10 Error type identification

E3	E2	E1	ERROR TYPE	NUMBER OF ERRORS
0	0	0	no errors - correct code-word	0
0	0	1	parity bit in error	1
0	1	0	single bit error	1 + parity
0	1	1	single bit error and parity error	1
1	0	0	not used	
1	0	1	4-bit burst error and parity error	3 (e.g.1101)
1	1	0	2-bit random error	2
1	1	1	uncorrectable code-word	3 or more

Table 11 Receiver and oscillator establishment times (note 1)

CONTROL OUTPUT	ESTABLISHMENT TIME				UNIT
RXE	5	10	15	30	ms
ROE	20	30	40	50	ms

Note

1. The exact values may differ slightly from the above values, depending on the bit rate (see Table 22).

Synthesizer control

Control of an external frequency synthesizer is possible via a dedicated 3-line serial interface (outputs ZSD, ZSC and ZLE). This interface is common to a number of available synthesizers. The synthesizer is enabled using the oscillator enable output ROE.

The frequency parameters must be programmed in EEPROM. Two blocks of maximum 24 bits each can be stored. Any unused bits must be programmed at the beginning of a block: only the last bits are used by the synthesizer.

When the function is selected by SPF programming (SPF byte 01, bit D6), data is transferred to the synthesizer each time the PCD5003 is switched from OFF to ON status. Transfer takes place serially in two blocks, starting with bit 0 (MSB) of block 1 (see Table 25).

Data bits on ZSD change on the falling flanks of ZSC. After clocking all bits into the synthesizer, a latch enable pulse copies the data to the internal divider registers. A timing diagram is given in Fig.5.

The data output timing is synchronous, but has a pause in the bit stream of each block. This pause occurs in the 13th bit while ZSC is LOW. The nominal pause duration t_p depends on the programmed bit rate for data reception and is shown in Table 12. The total duration of the 13th bit is given by $t_{ZCL} + t_p$.

A similar pause occurs between the first and the second data block. The delay between the first latch enable pulse and the second data block is given by $t_{ZDL2} + t_p$. The complete start-up timing of the synthesizer interface is given in Fig.12.

Table 12 Synthesizer programming pause

BIT RATE (bit/s)	t_p (clocks)	t_p (μs)
512	119	1549
1200	33	430
2400	1	13

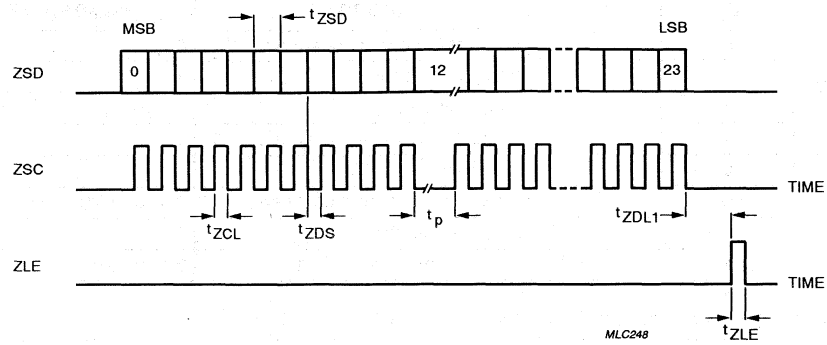


Fig.5 Synthesizer interface timing.

Serial microcontroller interface

The PCD5003 has an I²C-bus serial microcontroller interface capable of operating at 400 kbits/s. The PCD5003 is a slave transceiver with a 7-bit I²C-bus address 39 (bits A6 to A0 = 0100111). Together with the R/$\overline{W}$ bit the first byte of an I²C-bus message then becomes 4EH (write) or 4FH (read).

Data transmission requires 2 lines: SDA (data) and SCL (clock), each with an external pull-up resistor. The clock signal (SCL) for any data transmission must be generated by the external controlling device.

A transmission is initiated by a start condition (S: SCL = 1, SDA = ↓) and terminated by a stop condition (P: SCL = 1, SDA = ↑).

Data bits must be stable when SCL is HIGH. If there are multiple transmissions, the stop condition can be replaced with a new start condition.

Data is transferred on a byte basis, starting with a device address and a read/write indicator. Each transmitted byte must be followed by an acknowledge bit ACK (active LOW). If a receiving device is not ready to accept the next complete byte, it can force a bus wait state by holding SCL LOW. The general I²C-bus transmission format is shown in Fig.6. Formats for master/slave communication are shown in Fig.7.

Decoder I²C-bus access

All internal access to the PCD5003 takes place via I²C-bus interface. For this purpose the internal registers, SRAM and EEPROM have been memory mapped and are accessed via an **index register**. Table 13 shows the index addresses of all internal blocks.

Registers are addressed directly, while RAM and EEPROM are addressed indirectly via address pointers and I/O registers.

Remark: The EEPROM memory map is non-contiguous and organized as a matrix. The EEPROM address pointer contains both row and column indicators.

Data written to read-only bits will be ignored. Values read from write-only bits are undefined and must be ignored.

Each I²C write message to the PCD5003 must start with its slave address, followed by the index address of the memory element to be accessed. An I²C read message uses the last written index address as a data source. The different I²C-bus message types are shown in Fig.7.

As a slave the PCD5003 cannot initiate bus transfers by itself. To prevent an external controller from having to monitor the operating status of the decoder, all important events generate an external interrupt on output INT.

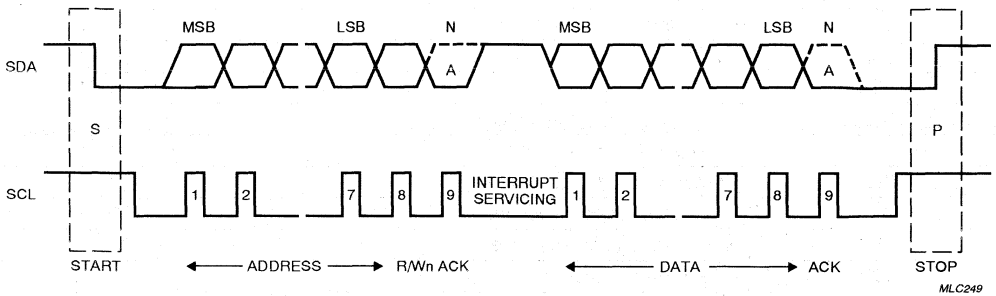
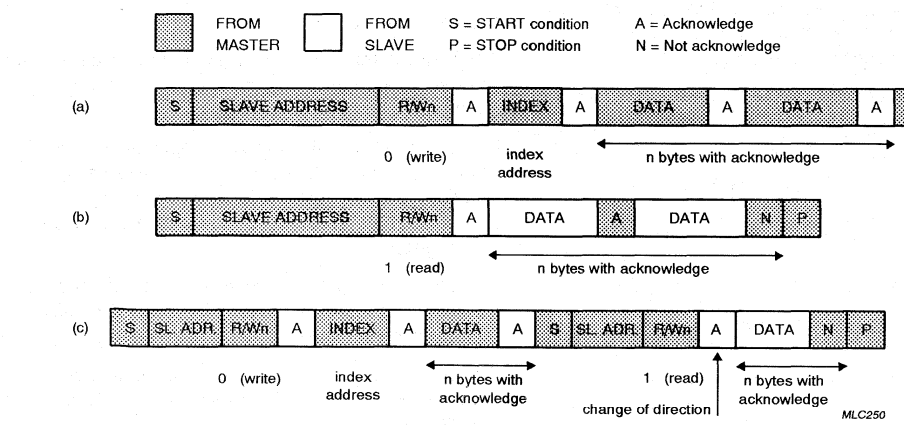


Fig.6 I²C-bus message format.



(a) Master writes to slave.
(b) Master reads from slave.
(c) Combined format (shown: write plus read).

Fig.7 Message types.

Table 13 Index register

ADDRESS[1]	REGISTER FUNCTION	ACCESS
00H	status	R
00H	control	W
01H	real time clock: seconds	R/W
02H	real time clock: $^1/_{100}$ second	R/W
03H	alert cadence	W
04H	alert set-up	W
05H	periodic interrupt modulus	W
05H	periodic interrupt counter	R
06H	RAM write address pointer	R
07H	EEPROM address pointer	R/W
08H	RAM read address pointer	R/W
09H	RAM data output	R
0AH	EEPROM data input/output	R/W
0BH to 0FH	unused	note 2

Notes

1. The index register only uses the least significant nibble, the upper 4 bits are ignored.
2. Writing to registers 0B to 0F has no effect, reading produces meaningless data.

External interrupt

The PCD5003 can signal events to an external controller via an interrupt signal on output INT. The interrupt polarity is programmable via SPF programming. The interrupt source is shown in the status register.

Interrupts are generated by the following events (more than one event possible):

- Call data available for output (bit D2)
- SRAM pointers becoming equal (bit D3)
- Expiry of periodic time-out (bit D7)
- Expiry of alert time-out (bit D4)
- Change of state in out-of-range indicator (bit D5)
- Change of state in battery-low indicator or in receiver control output RXE (bit D6).

Immediate interrupts are generated by status bits D3, D4, D6 (RXE monitoring) and D7. Bits D2, D5 and D6 (BAT monitoring) generate interrupts as soon as the receiver is disabled (RXE = 0).

When call data is available (D2 = 1) but the receiver remains switched on, an interrupt is generated at the next sync word position.

The interrupt output INT is reset after completion of a status read operation.

Status/Control register

The status/control register consists of two independent registers, one for reading (status) and one for writing (control).

The status register shows the current operating condition of the decoder and the cause(s) of an external interrupt. The control register activates/deactivates certain functions. Tables 14 and 15 show the bit allocations of both registers.

All status bits will be reset after a status read operation except for the out-of-range, battery-low and receiver enable indicator bits (see note 1 to Table 14).

Status bit D0 is set when call reception is started by detection of an enabled RIC (user address). This does not generate an interrupt.

Table 14 Status register (00H; read)

BIT[1]	VALUE	DESCRIPTION
D1 and D0	0 0	no new call data
	0 1	call data available
	1 0	reserved for future use
	1 1	reserved for future use
D3 and D2	0 0	no data to be read (default after reset)
	0 1	RAM read/write pointers different: data to be read
	1 0	RAM read/write pointers equal: no more data to read
	1 1	RAM buffer full or overflow
D4	1	alert time-out expired
D5	1	out-of-range
D6	1	BAT input HIGH or RXE output active (selected by control bit D2)
D7	1	periodic timer interrupt

Note

1. After a status read operation bits D3, D4 and D7 are always reset, bits D1 and D0 only when no second call is pending. D2 is reset when the RAM is empty (read and write pointers equal).

Table 15 Control register (00H; write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	1	forced call termination (automatically reset after termination)
D1	1	EEPROM programming enable
D2	0	BAT input selected for monitoring (status bit D6)
	1	RXE output selected for monitoring (status bit D6)
D3	1	receiver continuously enabled (RXE = 1, ROE = 1)
D4	0	decoder in OFF status (while DON = 0)
	1	decoder in ON status
D5 to D7	X	not used: ignored when written

Pending interrupts

A secondary status register is used for storing status bits of pending interrupts. This occurs:

- When a new call is received while the previous one was not yet acknowledged by reading the status register.
- When an interrupt occurs during a status read operation.

After completion of the status read the primary register is loaded with the contents of the secondary register, which is then reset. Next, an immediate interrupt is generated, output INT becoming active 1 decoder clock cycle after it was reset following the status read.

Remark: In the event of multiple pending calls, only the status bits of the last call are retained.

Out-of-Range Indication

The out-of-range condition occurs when entering fade recovery or carrier-off mode. This condition is reflected in bit D5 of the status register. The out-of-range condition is reset when either preamble or a valid sync word is detected.

The out-of-range bit (D5) in the status register is updated each time the receiver is disabled (RXE ↓ 0). Every change of state in bit D5 generates an interrupt.

Real time clock

The PCD5003 provides a periodic reference pulse at output REF. The frequency of this signal can be selected by SPF programming:

- 32768 Hz
- 50 Hz (square-wave)
- 2 Hz
- $1/60$ Hz.

The 32768 Hz signal does not have a fixed period: it consists of 32 pulses distributed over 75 main oscillator cycles at 76.8 kHz. The timing is shown in Fig.13.

When programmed for $1/60$ Hz (1 pulse per minute) the pulse at output REF is held off while the receiver is enabled.

Except for the 50 Hz frequency the pulse width t_{RFP} is equal to one decoder clock period.

The real time clock counter runs continuously irrespective of the operating condition of the PCD5003. It contains a **seconds register** (maximum 59) and a $1/100$ **second register** (maximum 99), which can be read or written via the I^2C-bus. The bit allocation of both registers is shown in Tables 16 and 17.

Table 16 Real time clock: seconds register (01H; read/write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	–	1 second
D1	–	2 seconds
D2	–	4 seconds
D3	–	8 seconds
D4	–	16 seconds
D5	–	32 seconds
D6	X	not used: ignored when written, undetermined when read
D7	X	not used: ignored when written, undetermined when read

Table 17 Real time clock: $1/100$ second register (02H; read/write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	–	0 01 second
D1	–	0.02 second
D2	–	0.04 second
D3	–	0.08 second
D4	–	0.16 second
D5	–	0.32 second
D6	–	0.64 second
D7	X	not used: ignored when written, undetermined when read

Table 18 Alert set-up register (04H; write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	0	call alert via cadence register
	1	POCSAG call alert (pattern selected by D7, D6)
D1	0	LOW level acoustic alert (ATL), pulsed vibrator alert (25 Hz)
	1	HIGH level acoustic alert (ATL + ATH), continuous vibrator alert
D2	0	normal alerts (acoustic and LED)
	1	warbled alerts: 16 Hz (LED: on/off, ATL/ATH: alternate f_{AWH}, f_{AWL})
D3	1	acoustic alerts enable (ATL, ATH)
D4	1	vibrator alert enabled (VIB)
D5	1	LED alert enabled (LED)
D7 and D6[1]	0 0	POCSAG alert pattern FC = 00, see Fig.8(a)
	0 1	POCSAG alert pattern FC = 01, see Fig.8(b)
	1 0	POCSAG alert pattern FC = 10, see Fig.8(c)
	1 1	POCSAG alert pattern FC = 11, see Fig.8(d)

Note

1. Bits D7 and D6 correspond to function bits 20 and 21 respectively in the address code-word, which designate the POCSAG call type as shown in Table 1.

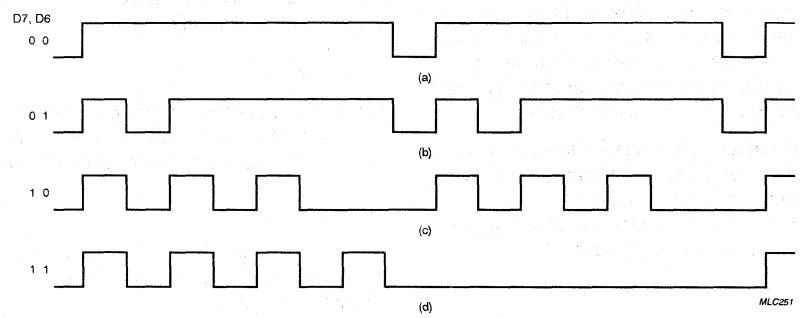


Fig.8 POCSAG alert patterns.

Periodic interrupt

A periodic interrupt can be realised with the Periodic Interrupt Counter. This 8-bit counter is incremented every $^1/_{100}$ second and produces an interrupt when it reaches the value stored in the Periodic Interrupt Modulus register. The Counter register is then reset and counting continues.

Operation is started by writing a non-zero value to the Modulus register. Writing a zero will stop interrupt generation immediately and will halt the Periodic Interrupt Counter after 2.55 seconds.

The Modulus register is write-only, the Counter register can only be read. Both registers have the same index address (05H).

Received call delay

Call reception causes both the Periodic Interrupt Modulus and the Counter register to be reset.

Since the Periodic Interrupt Counter runs for another 2.55 seconds after a reset, the received call delay (in $^1/_{100}$ second units) can be determined by reading the Counter register.

Alert generation

The PCD5003 is capable of controlling 3 different alert transducers: acoustic beeper (HIGH and LOW level), LED and vibrator motor. The associated outputs are ATH/ATL, LED and VIB respectively. ATL is an open drain output capable of directly driving an acoustic alerter via a resistor. The other outputs require external transistors.

Each alert output can be individually enabled via the alert set-up register. Alert level and warble can be separately selected. The alert pattern can either be standard POCSAG or determined via the alert cadence register. Direct alert control is possible via input ALC.

The alert set-up register is shown in Table 18.

Standard POCSAG alerts can be selected by setting bit D0 in the alert set-up register, bits D6 and D7 determining the alert pattern used.

Automatic generation via all alert outputs of the POCSAG alert pattern matching the received call type can be enabled by SPF programming (SPF byte 03, bit D2).

ALERT CADENCE REGISTER (03H; WRITE)

When not programmed for POCSAG alerts (alert set-up register bit D0 = 0), the 8-bit alert cadence register determines the alert pattern. Each bit represents a 62.5 ms time slot, a logic 1 activating the enabled alert transducers. The bit pattern is rotated with the MSB (bit D7) being output first and the LSB (bit D0) last.

When the last time slot (bit D0) is started an interrupt is generated to allow loading of a new pattern. When the pattern is not changed it will be repeated. Writing a zero to the alert cadence register will halt alert generation.

ACOUSTIC ALERT

Acoustic alerts are generated via outputs ATL and ATH. For LOW level alerts only ATL is active, while for HIGH level alerts ATH is also active. ATL is driven in counter phase with ATH.

The alert level is controlled by bit D1 of the alert set-up register.

When D1 is reset, for standard POCSAG alerts (D0 = 1) a LOW level acoustic alert is generated during the first 4 seconds (ATL), followed by 12 seconds at HIGH level (ATL + ATH). When D1 is set, the full 16 seconds are at HIGH level. An interrupt is generated upon expiry of the full alert time.

When using the alert cadence register, D1 would normally be updated by external control when the alert time-out interrupt occurs at the start of the 8th cadence time slot. Since D1 acts immediately on the alert level, it is advised to reset the last bit of the previous pattern to prevent unwanted audible level changes.

LED ALERT

The LED output pattern corresponds either to the selected POCSAG alert or to the contents of the alert cadence register. No equivalent exists for HIGH/LOW level alerts.

VIBRATOR ALERT

The vibrator output (VIB) is activated continuously during a standard POCSAG alert or whenever the alert cadence register is non-zero.

Two alert levels are supported: LOW level (25 Hz square-wave) and HIGH level (continuous). The vibrator level is controlled by bit D1 in the alert set-up register.

WARBLED ALERT

When enabled by setting bit D2 in the alert set-up register, the signals on outputs ATL, ATH and LED are warbled with a 16 Hz modulation frequency. Output LED is switched on and off at the modulation rate, while outputs ATL and ATH switch between f_{AWH} and f_{AWL} alerter frequencies.

DIRECT ALERT CONTROL

A direct alert control input (ALC) is available for generating user alarm signals (e.g. battery-low warning). A HIGH level on input ALC activates all enabled alert outputs, overruling any ongoing alert patterns.

ALERT PRIORITY

Generation of a standard POCSAG alert (D0 = 1) overrides any alert pattern in the alert cadence register. After completion of the standard alert, the original cadence is restarted from the position it was left at. The alert set-up register will now contain the settings for the standard alert.

The highest priority has been assigned to the alert control input (ALC). All enabled alert outputs will be activated while ALC is set. Outputs are activated/deactivated synchronous with the decoder clock. Activation requires an extra delay of 1 clock when no alerts are being generated.

When input ALC is reset, acoustic alerting does not cease until the current output frequency cycle has been completed.

AUTOMATIC POCSAG ALERTS

Standard alert patterns have been defined for each POCSAG call type, as indicated by the function bits in the address code-word (see Table 1). The timing of these alert patterns is shown in Fig.9.

When enabled by SPF programming (SPF byte 03, bit D2) standard POCSAG alerts will automatically be generated on outputs ATL, ATH, LED and VIB upon call reception. The alert pattern matches the call type as indicated by the function bits in the received address code-word.

The original settings of the alert set-up register will be lost. Bit D0 is reset after completion of the alert.

CANCELLING ALERTS

Any ongoing alert is cancelled when a reset pulse is applied to input RST. Standard POCSAG alerts (manual or automatic) are cancelled by resetting bit D0 in the alert set-up register. User defined alerts are cancelled by writing a zero to the alert cadence register.

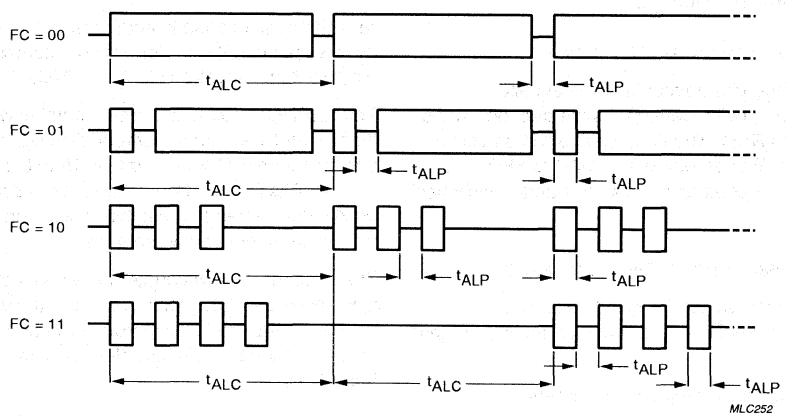


Fig.9 POCSAG alert timing.

RAM organization

SRAM ACCESS

The on-chip SRAM can hold up to 96 bytes of call data. Each call consists of a call header (3 bytes), message data blocks (3 bytes per code-word) and a call terminator (3 bytes).

The RAM is filled by the decoder and can be read via the I^2C-bus interface. The RAM is accessed indirectly by means of a read address pointer and a data output register. A write address pointer indicates the first byte after the last message byte stored.

Status register bit D2 is set when the read and write pointers are different. It is reset only when the SRAM pointers become equal during reading, i.e. when the RAM becomes empty.

Status bit D3 is set when the read and write pointers become equal. This can be due to a RAM empty or a RAM full condition. It is reset after a status read operation.

Interrupts are generated as follows:

- When status bit D2 is set and the receiver is disabled (RXE = 0): data is available for reading.
- Immediately when status bit D3 is set: RAM is either empty (status bit D2 = 0) or full (status bit D2 = 1).

To avoid loss of data due to RAM overflow at least 3 bytes of data must be read during reception of the code-word following the 'RAM full' interrupt.

RAM WRITE ADDRESS POINTER (06H; READ)

The RAM write address pointer is automatically incremented during call reception, as the decoder writes each data byte to RAM. The RAM write address pointer can only be read. Values range from 00H to 5FH.
Bit D7 (MSB) is not used and its value is undefined when read.

RAM READ ADDRESS POINTER (08H; READ/WRITE)

The RAM read address pointer is automatically incremented after reading a data byte via the RAM output register.

It can be accessed for writing as well as reading.

The values range from 00H to 5FH. When at 5FH a read operation will cause wrapping around to 00H. Bit D7 (MSB) is not used; it is ignored when written and undefined when read.

RAM DATA OUTPUT REGISTER (09H; READ)

The RAM data output register contains the byte addressed by the RAM read address pointer. It can only be read, each read operation causing an increment of the RAM read address pointer.

EEPROM organization

EEPROM ACCESS

The EEPROM is intended for storage of user addresses (RICs), sync words and special programmed function (SPF) bits representing the decoder configuration.

The EEPROM can store 48 bytes of information and is organized as a matrix of 8 rows by 6 columns. The EEPROM is accessed indirectly via an address pointer and a data I/O register.

The EEPROM is protected against inadvertent writing by means of the programming enable bit in the control register (bit D1).

The EEPROM memory map is non-contiguous as can be seen in Fig.10, which shows both the EEPROM organization and the access method.

Identifier locations contain RICs or sync words. A total of 20 unassigned bytes is available for general purpose storage.

EEPROM ADDRESS POINTER (07H; READ/WRITE)

An EEPROM location is addressed via the EEPROM address pointer. It is incremented automatically each time a byte is read or written via the EEPROM data I/O register.

The EEPROM address pointer contains two counters, for the row and the column number. Bits D2 to D0 contain the column number (0 to 5) and bits D5 to D3 the row number (0 to 7). Bits D7 and D6 of the address pointer are not used. Data written to these bits will be ignored, while their values are undefined when read.

The column and row counters are connected in series. Upon overflow of the column counter (column = 5) the row counter is automatically incremented and the column counter wraps to 0. On overflow the row counter wraps from 7 to 0.

EEPROM DATA I/O REGISTER (0A HEX, READ/WRITE)

The byte addressed by the EEPROM address pointer can be written or read via the EEPROM Data I/O register. Each access automatically increments the EEPROM address pointer.

EEPROM ACCESS LIMITATIONS

Since the EEPROM address pointer is used during data decoding, the EEPROM may not be accessed while the receiver is active (RXE = 1). It is advised to switch to OFF state before accessing the EEPROM.

The EEPROM cannot be written unless the EEPROM programming enable bit (bit D1) in the control register is set.

For writing a minimum supply voltage V_{PG} is required (2.5 V typ.). The supply current needed during writing (I_{PG}) will be ≈500 μA.

Any modified SPF settings (bytes 0 to 3) only take effect after a decoder reset. Modified identifiers are active immediately.

EEPROM READ OPERATION

EEPROM read operations must start at a valid address in the non-contiguous memory map. Single-byte or block reads are permitted.

EEPROM WRITE OPERATION

EEPROM write operations must always take place in blocks of 6 bytes, starting at the beginning of a row. Programming a single byte will reset the other bytes in the same row. Modifying a single byte in a row requires re-writing the unchanged bytes with their old contents.

After writing each block a pause of maximum 7.5 ms is required to complete the programming operation internally. During this time the external microcontroller may generate an I²C-bus stop condition. If another I²C-bus transfer is started the decoder will pull SCL LOW during this pause.

After writing the EEPROM programming enable bit (D1) in the control register must be reset.

INVALID WRITE ADDRESS

When an invalid write address is used, the column counter bits (D2 to D0) are forced to zero before being loaded into the address pointer. The row counter bits are used normally.

INCOMPLETE PROGRAMMING SEQUENCE

A programming sequence may be aborted by an I²C-bus stop condition. Next, the EEPROM programming enable bit (D1) in the control register must be reset.

Any bytes received of the last 6-byte block will be ignored and the contents of this (incomplete) EEPROM block will remain unchanged.

UNUSED EEPROM LOCATIONS

A total of 20 EEPROM bytes is available for general purpose storage (see Table 19).

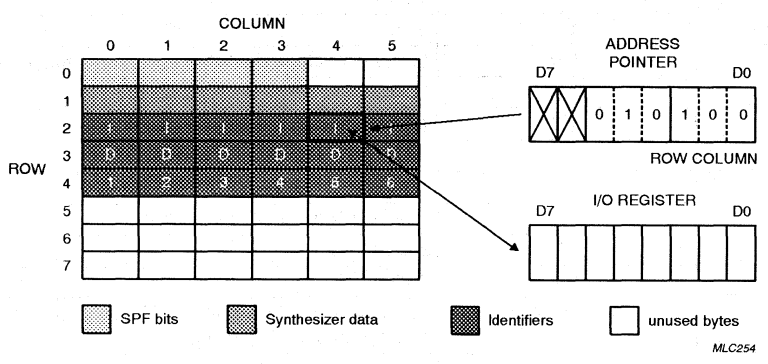


Fig.10 EEPROM organization and access.

Table 19 Unused EEPROM addresses

ROW	HEX
0	04 and 05[1]
5	28 to 2D
6	30 to 35
7	38 to 3D

Note

1. When using bytes 04H and 05H, care must be taken to preserve the SPF information stored in bytes 00H to 03H.

SPECIAL PROGRAMMED FUNCTION ALLOCATION

The SPF bit allocation in the EEPROM is shown in Tables 20 to 24. The SPF bits are located in row 0 of the EEPROM and occupy 4 bytes.

Bytes 04H and 05H are not used and are available for general purpose storage.

The contents of SPF (bytes 0 to 3) are read into the associated logic only when the decoder is reset (HIGH level in input RST).

Table 20 Special Programmed Functions (EEPROM address 00H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	reserved for future use; logic 0 when read
D1	X	reserved for future use
D2	X	reserved for future use
D3	X	reserved for future use
D4	X	reserved for future use
D5	X	reserved for future use
D6	X	reserved for future use; logic 0 when read
D7	1	received data inversion enabled

Table 21 Special Programmed Functions (EEPROM address 01H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	5 ms receiver establishment time (nominal); note 1
	0 1	10 ms
	1 0	15 ms
	1 1	30 ms
D3 and D2	0 0	20 ms oscillator establishment time (nominal); note 1
	0 1	30 ms
	1 0	40 ms
	1 1	50 ms
D5 and D4	0 0	512 bits/s received bit rate
	0 1	1024 bits/s (not used in POCSAG)
	1 0	1200 bits/s
	1 1	2400 bits/s
D6	1	synthesizer interface enabled (data is output via ZSD, ZSC and ZLE at decoder switch-on)
D7	1	voltage converter enabled

Note

1. Since the exact establishment time is related to the programmed bit rate, Table 22 shows the values for the various bit rates.

Table 22 Establishment time as a function of bit rate

NOMINAL ESTABLISHMENT TIME	ACTUAL ESTABLISHMENT TIME (bits)			
	512 bits/s	1024 bits/s	1200 bits/s	2400 bits/s
5 ms	5.9 ms (3)	5.9 ms (6)	5.0 ms (6)	5.0 ms (12)
10 ms	11.7 ms (6)	11.7 ms (12)	10.0 ms (12)	10.0 ms (24)
15 ms	15.6 ms (8)	15.6 ms (16)	16.7 ms (20)	16.7 ms (40)
20 ms	23.4 ms (12)	23.4 ms (24)	20.0 ms (24)	20.0 ms (48)
30 ms	31.2 ms (16)	31.2 ms (32)	26.7 ms (32)	26.7 ms (64)
40 ms	39.1 ms (20)	39.1 ms (40)	40.0 ms (48)	40.0 ms (96)
50 ms	46.9 ms (24)	46.9 ms (48)	53.3 ms (64)	53.3 ms (128)

Table 23 Special Programmed Functions (EEPROM address 02H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	not used
D1	X	not used
D3 and D2	0 0	32768 Hz real time clock reference
	0 1	50 Hz square-wave
	1 0	2 Hz
	1 1	$^1/_{60}$ Hz
D4	1	signal test mode enabled (REF and INT outputs)
D5	0	burst error correction enabled
D7 and D6	X X	reserved for future use

Table 24 Special Programmed Functions (EEPROM address 03H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	2048 Hz acoustic alerter frequency
	0 1	2731 Hz
	1 0	4096 Hz
	1 1	3200 Hz
D2	1	automatic POCSAG alert generation enabled
D3	X	not used
D4	X	not used
D5	X	not used
D6	0	INT output polarity: active LOW
	1	INT output polarity: active HIGH
D7	X	not used

SYNTHESIZER PROGRAMMING DATA

Data for programming a PLL synthesizer via pins ZSD, ZSC and ZLE can be stored in row 1 of the EEPROM. Six bytes are available starting from address 08H.

Data is transferred in two serial blocks of 24 bits each, starting with bit 0 (MSB) of block 1. Any unused bits must be programmed at the beginning of a block.

IDENTIFIER STORAGE ALLOCATION

Up to 6 different identifiers can be stored in EEPROM for matching with incoming data. The PCD5003 can distinguish two types of identifiers:

- User addresses (RIC)
- User Programmable Sync Words (UPSW).

Identifiers are stored in EEPROM rows 2, 3 and 4. Each identifier location consists of 3 bytes in the same column. The identifier number is equal to the column number + 1.

Only the last 4 identifiers (numbers 3 to 6) can be programmed as a UPSW. Identifiers 1 and 2 always represent RICs. A UPSW represents an unused address and must differ by more than 6 bits from preamble to guarantee detection.

The standard POCSAG sync word is always enabled and has identifier number 7.

Table 26 shows the memory locations of the 6 identifiers. The bit allocation per identifier is given in Table 27.

Table 25 Synthesizer programming data (EEPROM address 08H to 0DH)

ADDRESS (HEX)	BIT (MSB: D7)	DESCRIPTION
08	D7 to D0	bits 0 to 7 of data block 1 (bit 0 is MSB)
09	D7 to D0	bits 8 to 15
0A	D7 to D0	bits 16 to 23
0B	D7 to D0	bits 0 to 7 of data block 2 (bit 0 is MSB)
0C	D7 to D0	bits 8 to 15
0D	D7 to D0	bits 16 to 23

Table 26 Identifier storage allocation (EEPROM address 10H to 25 H)

ADDRESS (HEX)	BYTE	DESCRIPTION
10 to 15	1	identifier number 1 to 6
18 to 1D	2	identifier number 1 to 6
20 to 25	3	identifier number 1 to 6

Table 27 Identifier bit allocation

BYTE	BIT (MSB: D7)	DESCRIPTION
1	D7 to D0	bits 2 to 9 of POCSAG code-word (RIC or UPSW); notes 1 and 2
2	D7 to D0	bits 10 to 17
3	D7 and D6	bits 18 and 19
	D5	frame number bit FR3 (RIC); note 3
	D4	frame number bit FR2 (RIC)
	D3	frame number bit FR1 (RIC)
	D2	identifier type selection (0 = UPSW, 1 = RIC); note 4
	D1	identifier enable (1 = enabled)
	D0	reserved for future use, logic 0 when read

Notes

1. The bit numbering corresponds with the numbering in a POCSAG code-word: bit 1 is the flag bit (0 = address, 1 = message).
2. A UPSW needs 18 bits to be matched for successful identification. Bit 1 (MSB) must be logic 0; bits 2 to 19 contain the identifier bit pattern; they are followed by 2 predetermined random (function) bits and the UPSW is completed by 10 CRC error correction bits and an even-parity bit.
3. Bits FR3 to FR1 (MSB: FR3) contain the 3 least significant bits of the 21-bit RIC.
4. Identifiers 1 and 2 (RIC only) will be disabled by programming bit D2 as logic 0.

Voltage doubler

An on-chip voltage doubler provides an unregulated DC output for supplying an LCD or a low power microcontroller on output V_{PO}. An external ceramic capacitor of typical 100 nF is required between pins CCN and CCP. The voltage doubler is enabled via SPF programming.

Level-shifted interface

All interface lines are suited for communication with a microcontroller operating from a higher supply voltage. The external device must have a common reference at V_{SS} of the PCD5003.

The reference voltage for the level-shifted interface must be applied to input V_{PR}. This could be the on-chip voltage doubler output V_{PO} if required. When the microcontroller has a separate (regulated) supply this separate supply voltage should be connected to V_{PR}.

The level-shifted interface lines are: RST, DON, ALC, REF, INT.

The I^2C-bus interface lines SDA and SCL can be level-shifted independently of V_{PR} by means of the standard external pull-up resistors.

Signal test mode

A special signal test mode is available for monitoring the performance of a receiver circuit together with the front-end of the PCD5003.

For this purpose the output of the digital noise filter and the recovered bit clock are made available at outputs REF and INT respectively. All synchronization and decoding functions are normally active.

Signal test mode is activated/deactivated by SPF programming.

OPERATING INSTRUCTIONS

Reset conditions

When the PCD5003 is reset by applying a HIGH-level on input RST, the condition of the decoder is as follows:

- OFF status (irrespective of DON input level)
- REF output frequency 32768 Hz
- All internal counters reset
- Status/control register reset
- INT output at LOW-level
- No alert transducers selected
- LED, VIB and ATH outputs at LOW level
- ATL output high impedance
- SDA, SCL inputs high impedance
- Voltage converter disabled.

Within t_{RSU} after release of the reset condition (RST LOW) the programmed functions are activated. The settings affecting the external operation of the PCD5003 are as follows:

- REF output frequency
- Voltage converter
- INT output polarity
- Signal test mode.

When input DON is HIGH, the decoder starts operating in ON status immediately following t_{RSU}.

Power-on reset circuit

Input RST has an internal high-ohmic pull-down resistor (nominal 2 MΩ at 2.5 V supply). This can be used together with an external capacitor to V_{PR} to make a power-on reset signal.

Since this pull-down varies considerably with processing and supply voltage, a more accurate reset duration can be realised with an additional external resistor to V_{SS}.

Reset timing

The start-up time for the crystal oscillator may exceed 1 second (typ. 800 ms). It is advised to apply a reset condition at least during the first part of this period. The minimum reset pulse duration t_{RST} is 50 μs.

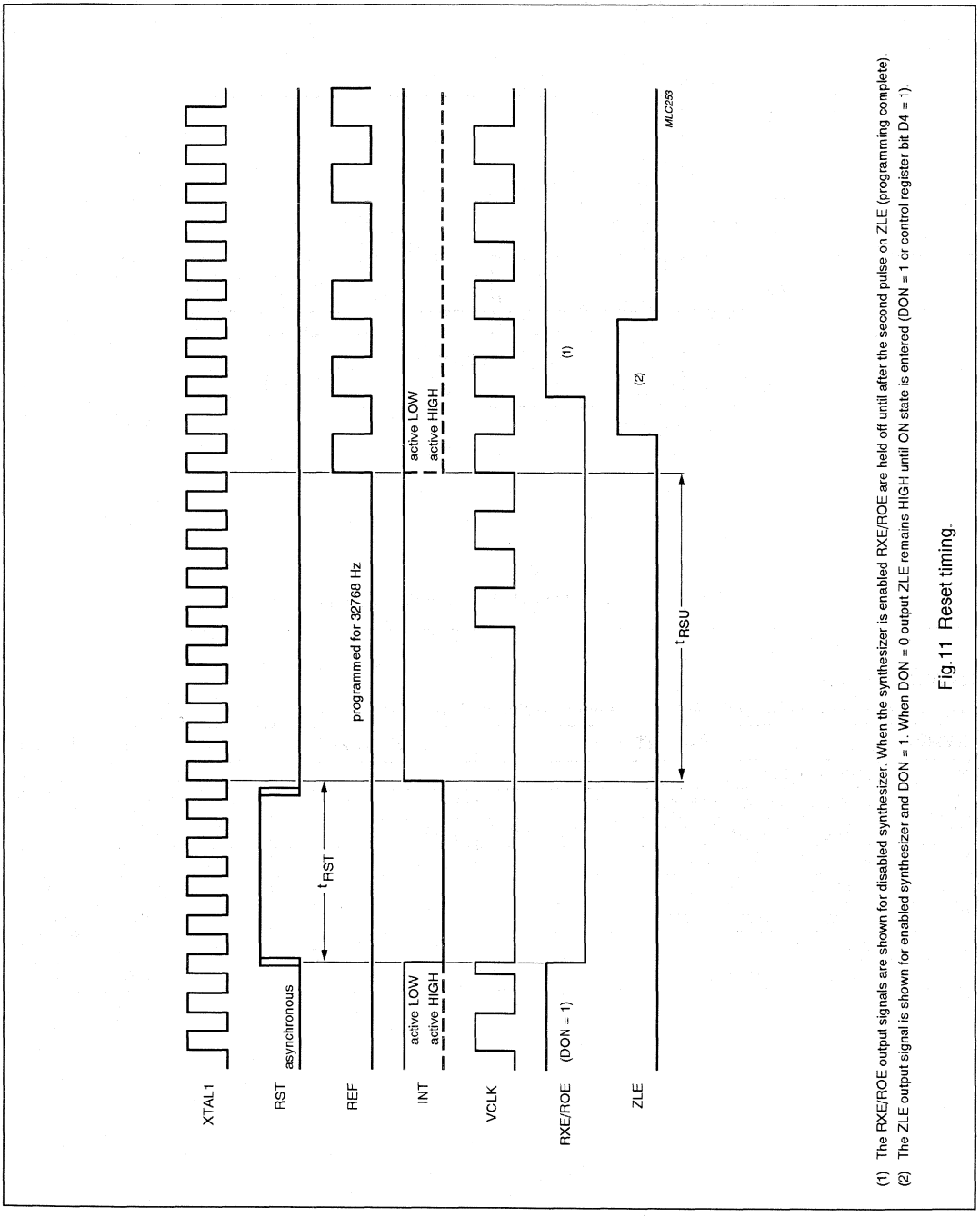
During reset the oscillator is active, but clock signals are inhibited internally. Once the reset condition is released the end of the oscillator start-up period can be detected by a rising edge on output INT.

During a reset the voltage converter clock (V_{clk}) is held at zero. The resulting output voltage drop may cause problems when the external resetting device is powered by the internal voltage doubler. A sufficiently large buffer capacitor between output V_{PO} and V_{SS} must be provided to supply the microcontroller during reset. The voltage at V_{PO} will not drop below V_{DD} – 0.7 V.

Immediately after a reset all programmable internal functions will start operating according to a programmed value of 0. During the first 8 full clock cycles (t_{RSU}) all programmed values are loaded from EEPROM.

After reset the receiver outputs RXE and ROE become active immediately, if DON is HIGH and the synthesizer is disabled. When the synthesizer is enabled, RXE and ROE will only become active after the second pulse on ZLE completes the loading of synthesizer data.

The full reset timing is shown in Fig.11. The start-up timing including synthesizer programming is given in Fig.12.



(1) The RXE/ROE output signals are shown for disabled synthesizer. When the synthesizer is enabled RXE/ROE are held off until after the second pulse on ZLE (programming complete).
(2) The ZLE output signal is shown for enabled synthesizer and DON = 1. When DON = 0 output ZLE remains HIGH until ON state is entered (DON = 1 or control register bit D4 = 1).

Fig.11 Reset timing.

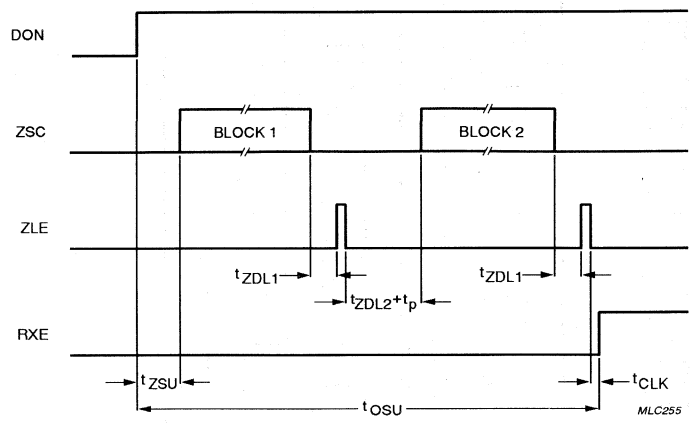


Fig.12 Start-up timing including synthesizer programming.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+7.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	−0.5	+7.0	V
V_n	voltage on pins ALC, DON, RST, SDA and SCL	$V_n \leq 7.0$ V	$V_{SS} - 0.8$	$V_{PR} + 0.8$	V
V_{n1}	voltage on any other pin	$V_{n1} \leq 7.0$ V	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
P_{tot}	total power dissipation		–	250	mW
P_O	power dissipation per output		–	100	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_{stg}	storage temperature		−55	+125	°C

DC CHARACTERISTICS

V_{DD} = 2.7 V; V_{PR} = 2.7 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		1.5	2.7	6.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	1.5	2.7	6.0	V
I_{DD0}	supply current (OFF)	note 1	–	25.0	40.0	μA
I_{DD1}	supply current (ON)	note 1; DON = V_{DD}	–	50.0	80.0	μA
V_{PG}	programming supply voltage		2.5	–	–	V
I_{PG}	programming supply current		–	–	800	μA
Inputs						
V_{IL}	LOW level input voltage					
	RDI, BAT		V_{SS}	–	$0.3V_{DD}$	V
	DON, ALC, RST		V_{SS}	–	$0.3V_{PR}$	V
	SDA, SCL		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage					
	RDI, BAT		$0.7V_{DD}$	–	V_{DD}	V
	DON, ALC, RST		$0.7V_{PR}$	–	V_{PR}	V
	SDA, SCL		$0.7V_{DD}$	–	V_{PR}	V
I_{IL}	LOW level input current pins RDI, BAT,TS1, TS2, DON, ALC and RST	T_{amb} = 25 °C; $V_I = V_{SS}$	0	–	−0.5	μA
I_{IH}	HIGH level input current	T_{amb} = 25 °C				
	TS1, TS2	$V_I = V_{DD}$	6	–	20	μA
	RDI, BAT	$V_I = V_{DD}$; RXE = 0	6	–	20	μA
	RDI, BAT	$V_I = V_{DD}$; RXE = 1	0	–	0.5	μA
	DON, ALC, RST	$V_I = V_{PR}$	250	500	850	nA
Outputs						
I_{OL}	LOW level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OL} = 0.3 V	80	–	–	μA
	ATH	V_{OL} = 0.3 V	250	–	–	μA
	INT, REF	V_{OL} = 0.3 V	80	–	–	μA
	ZSD, ZSC, ZLE	V_{OL} = 0.3 V	70	–	–	μA
	ATL	V_{OL} = 1.2 V; note 2	13	27	55	mA
	ROE, RXE	V_{OL} = 0.3 V	80	–	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{OH}	HIGH level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OH} = 0.7 V	−0.6	–	−2.4	mA
	ATH	V_{OH} = 0.7 V	−3.0	–	−11.0	mA
	INT, REF	V_{OH} = 2.4 V	−80	–	–	µA
	ZSD, ZSC, ZLE	V_{OH} = 2.4 V	−60	–	–	µA
	ATL	ATL high-impedance; note 3	–	–	−0.5	µA
	ROE, RXE	V_{OH} = 2.4 V	−600	–	–	µA

Notes

1. Inputs: SDA and SCL pulled up to V_{DD}; all other inputs connected to V_{SS}.
   Outputs: RXE and ROE logic 0; REF: f_{ref} = 1/60 Hz; all other outputs open-circuit.
   Oscillator: no crystal; external clock f_{osc} = 76800 Hz; amplitude: V_{SS} to V_{DD}.
   Voltage convertor disabled (SPF byte 01, bit D7 = 0; see Table 21).
2. Maximum output current is subject to absolute maximum ratings per output (see Chapter "Limiting values").
3. When ATL (open drain output) is not activated it is high impedance.

DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = V_{PO}; T_{amb} = −25 to +70 °C; C_s = 100 nF; voltage converter enabled.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.5	–	3.0	V
$V_{PO(0)}$	output voltage; no load	V_{DD} = 2.7; I_{PO} = 0	–	5.4	–	V
V_{PO}	output voltage	V_{DD} = 2.0 V; I_{PO} = −250 µA	3.0	3.5	–	V
I_{PO}	output current	V_{DD} = 2.0 V; V_{PO} = 2.7 V	−400	−650	–	µA
		V_{DD} = 3.0 V; V_{PO} = 4.5 V	−650	−900	–	µA

OSCILLATOR CHARACTERISTICS

Quartz crystal type: MX-1V or equivalent.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 35 kΩ; C_L = 8 pF; C_0 = 1.4 pF; C_1 = 1.5 fF; TC = −35 × 10^{-6}/K.
Maximum overall tolerance: ±200 × 10^{-6} (includes: cutting, temperature, aging).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{XO}	output capacitance XTAL2		–	10	–	pF
g_m	oscillator transconductance	V_{DD} = 1.5 V	6	12	–	µS

EEPROM CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
N_{EW}	erase/write cycles		1000	10000	–	
t_{DR}	data retention time	T_{amb} = +70 °C; note 1	10	–	–	years

Note

1. Retention cannot be guaranteed for naked dies (PCD5003U/10).

AC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = 2.7 V; T_{amb} = 25 °C;. f_{osc} = 76800 Hz.

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock						
T_{CLK}	system clock period	f_{osc} = 76800 Hz	–	13.02	–	µs
Call alert frequencies						
f_{AL}	alert frequency	SPF byte 03H; bits:				
		D1, D0 = 0 0	–	2048	–	Hz
		D1, D0 = 0 1	–	2731	–	Hz
		D1, D0 = 1 0	–	3200	–	Hz
		D1, D0 = 1 1	–	4096	–	Hz
f_{AW}	warbled alert; modulation frequency	alert setup bit D2 = 1; outputs ATL, ATH, LED	–	16	–	Hz
f_{AWH}	warbled alert; high acoustic alert frequency	alert setup bit D2 = 1; outputs ATL, ATH	–	f_{AL}	–	Hz
f_{AWL}	warbled alert; low acoustic alert frequency	alert setup bit D2 = 1; outputs ATL, ATH	–	$\frac{1}{2}f_{AL}$	–	Hz
f_{VBP}	pulsed vibrator frequency (square-wave)	low-level alert	–	25	–	Hz
Call alert duration						
t_{ALT}	alert time-out period		–	16	–	s
t_{ALL}	ATL output time-out period	low level alert	–	4	–	s
t_{ALH}	ATH output time-out period	high level alert	–	12	–	s
t_{VBL}	VIB output time-out period	low level alert	–	4	–	s
t_{VBH}	VIB output time-out period	high level alert	–	12	–	s
t_{ALC}	alert cycle period		–	1	–	s
t_{ALP}	alert pulse duration		–	125	–	ms
Real time clock reference						
f_{ref}	real time clock reference frequency	SPF byte 02H; bits:				
		D3, D2 = 0 0; note 1	–	32768	–	Hz
		D3, D2 = 0 1; note 2	–	50	–	Hz
		D3, D2 = 1 0	–	2	–	Hz
		D3, D2 = 1 1	–	$\frac{1}{60}$	–	Hz
t_{RFP}	real time clock reference pulse duration	all reference frequencies except 50 Hz (square-wave)	–	13.02	–	µs

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver control						
t_{RXT}	RXE, ROE transition time	C_L = 5 pF	–	100	–	ns
t_{RXON}	RXE establishment time (nominal values: actual duration is bit rate dependent, see Table 22)	SPF byte 01H; bits:				
		D1, D0 = 0 0	–	5	–	ms
		D1, D0 = 0 1	–	10	–	ms
		D1, D0 = 1 0	–	15	–	ms
		D1, D0 = 1 1	–	30	–	ms
t_{ROON}	ROE establishment time (nominal values: actual duration is bit rate dependent, see Table 22)	SPF byte 01H; bits:				
		D3, D2 = 0 0	–	20	–	ms
		D3, D2 = 0 1	–	30	–	ms
		D3, D2 = 1 0	–	40	–	ms
		D3, D2 = 1 1	–	50	–	ms
I²C-bus interface						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	µs
t_{HIGH}	SCL clock HIGH period		0.6	–	–	µs
t_{SUDAT}	data set-up time		100	–	–	ns
t_{HDDAT}	data hold time		0	–	–	ns
t_r	SDA, SCL rise time		–	–	300	ns
t_f	SDA, SCL fall time		note 3	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
t_{SUSTA}	start condition set-up time		0.6	–	–	µs
t_{HDSTA}	start condition hold time		0.6	–	–	µs
t_{SUSTO}	stop condition set-up time		0.6	–	–	µs
Reset						
t_{RST}	external reset duration		50	–	–	µs
t_{RSU}	set-up time after reset	oscillator running	–	–	105	µs
t_{OSU}	set-up time after switch-on	oscillator running	–	–	4	ms
Data input						
t_{TDI}	data input transition time		–	–	100	µs
t_{DI1}	data input logic 1 duration			infinite		
t_{DI0}	data input logic 0 duration			infinite		
POCSAG data timing (512 bits/s)						
f_{DI}	data input rate	SPF byte 01H; bits D5, D4 = 0 0	–	512	–	bits/s
t_{BIT}	bit duration		–	1.9531	–	ms
t_{CW}	code-word duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POCSAG data timing (1200 bits/s)						
f_{DI}	data input rate	SPF byte 01H; bits D5, D4 = 1 0	–	1200	–	bits/s
t_{BIT}	bit duration		–	833.3	–	µs
t_{CW}	code-word duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
POCSAG data timing (2400 bits/s)						
f_{DI}	data input rate	SPF byte 01H; bits D5, D4 = 1 1	–	2400	–	bits/s
t_{BIT}	bit duration		–	416.6	–	µs
t_{CW}	code-word duration		–	13.3	–	ms
t_{PA}	preamble duration		240	–	–	ms
t_{BAT}	batch duration		–	226.6	–	ms
Synthesizer control						
t_{ZSU}	synthesizer set-up duration	oscillator running; note 4	1	–	2	bits
f_{ZSC}	output clock frequency	note 5	–	38400	–	Hz
t_{ZCL}	clock pulse duration		–	13.02	–	µs
t_{ZSD}	data bit duration	note 5	–	26.04	–	µs
t_{ZDS}	data bit set-up time		–	13.02	–	µs
t_{ZDL1}	data load enable delay		–	91.15	–	µs
t_{ZLE}	load enable pulse duration		–	13.02	–	µs
t_{ZDL2}	inter block delay		–	117.19	–	µs

Notes

1. 32768 Hz reference signal: 32 pulses per 75 clock cycles, alternately separated by 1 or 2 pulse periods (pulse duration: t_{RFP}). The timing is shown in Fig.13.
2. 50 Hz reference signal: square-wave.
3. The fall time may be faster than prescribed in the I^2C-bus specification for very low load capacitance values. To increase the fall time external capacitance is required.
4. Duration depends on programmed bit rate; after reset t_{ZSU} = 1.5 bits.
5. Nominal values; pause in 12th data bit (see Table 12).

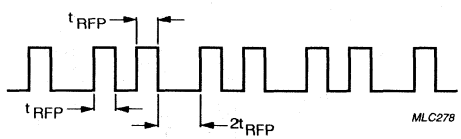
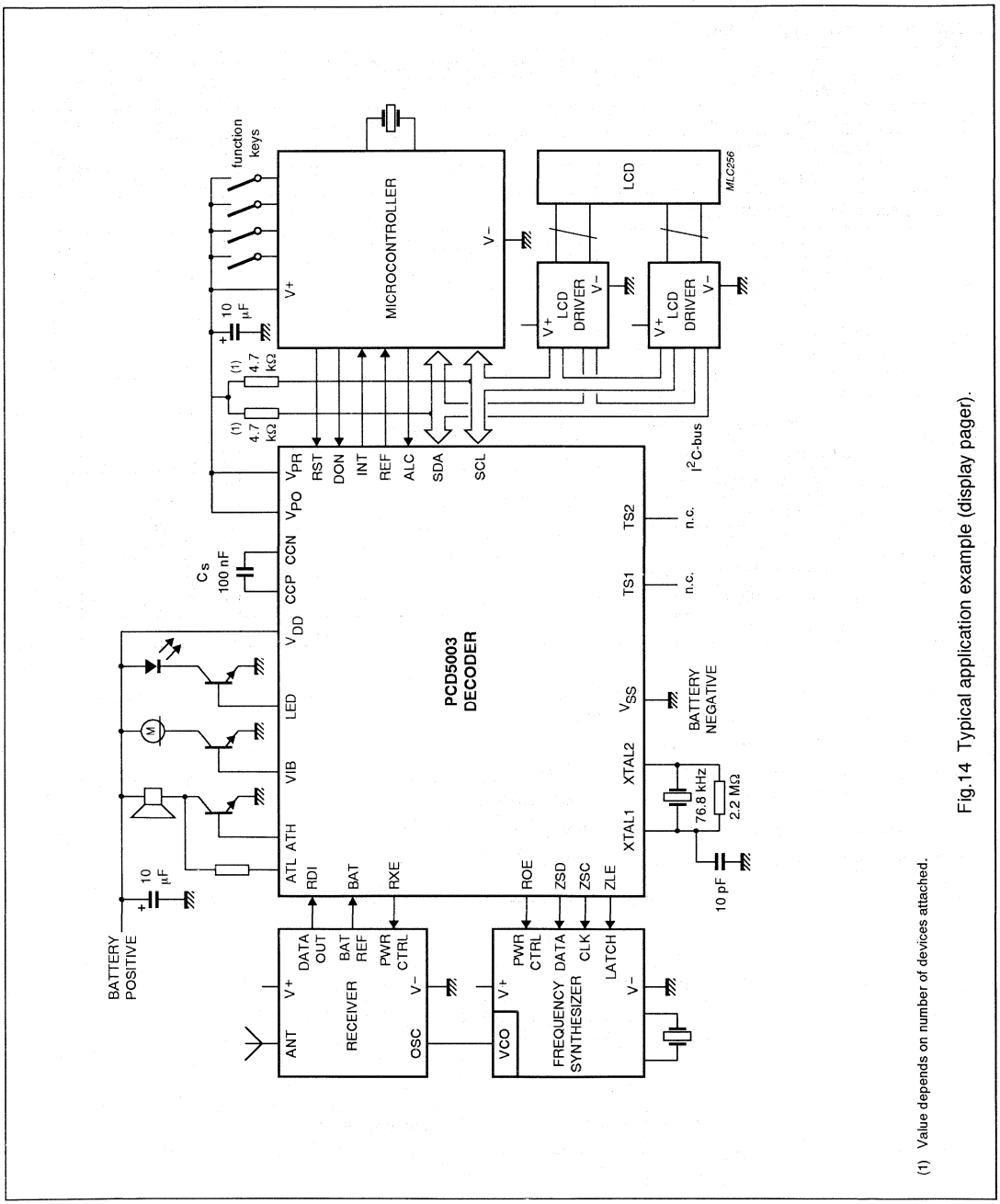


Fig.13 Timing of the 32768 Hz reference signal.

APPLICATION INFORMATION



(1) Value depends on number of devices attached.

Fig.14 Typical application example (display pager).

ADPCM codec for digital cordless telephone PCD5032

The PCD5032 is a CMOS device designed for use in Digital European Cordless Telephone systems (DECT) but it is also suited for other cordless telephony applications (e.g., CT2). The PCD5032 performs A/D and D/A conversion, ADPCM encoding and decoding compliant to CCITT recommendation G.721 (blue book 1988). The PCD5032 allows direct connection to external microphone and earpiece. The device can be used in both handset and base–station designs.

This objective specification contains advance information and is subject to change without notice.

FEATURES

- G.721 compliant ADPCM encoding and decoding
- 'Bitstream' A/D and D/A conversion
- On–chip receive and transmit filter
- On–chip ringer and tone generator
- Programmable gain of receive and transmit path
- Serial ADPCM interface with independent timing for maximum flexibility
- Linear PCM data accessible for digital echo cancelling
- Programmable via I^2C interface
- Fast receiver mute input via pin
- On–chip voltage reference
- On–chip symmetrical supply for electret microphone
- Few external components; direct connection to microphone and earpiece
- Low power consumption in standby mode
- Low supply voltage (single supply 2.7 V up to 5.5 V)
- CMOS technology
- Minimized EMC on digital outputs

APPLICATIONS

- Digital European Cordless Telephony (DECT)
- CT2 cordless
- Speech compression

PACKAGE OUTLINE

S028 (SOT136A) QFP44S14 (SOT205AG)

1.0 BLOCK DIAGRAM

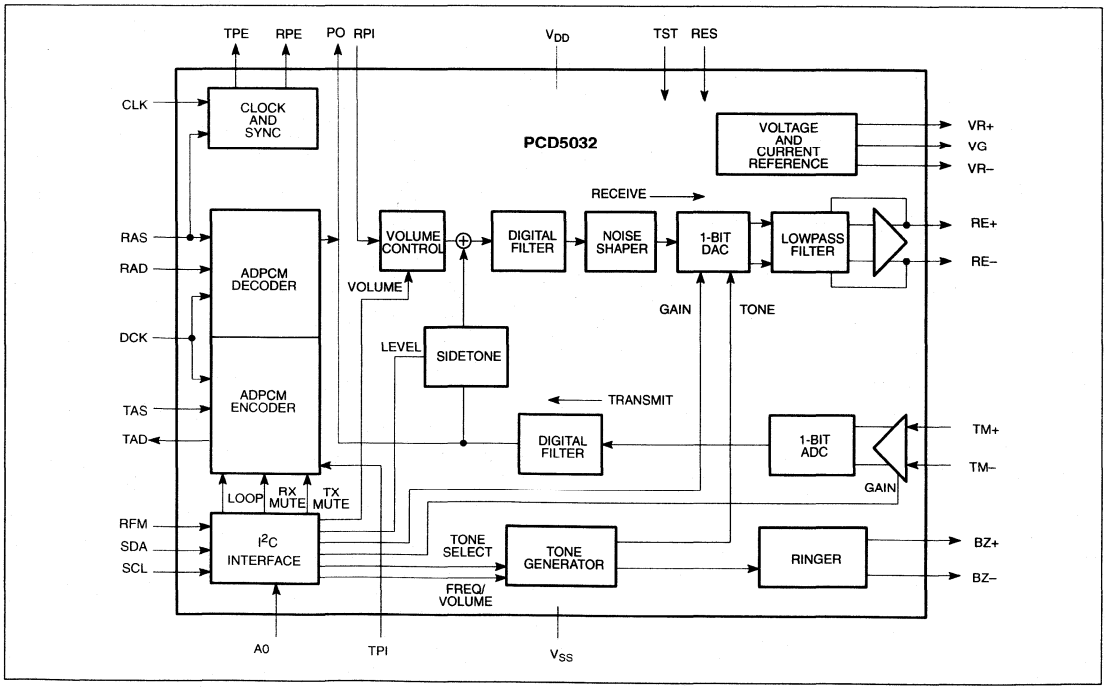


Figure 1. Block Diagram

2.0 PINNING

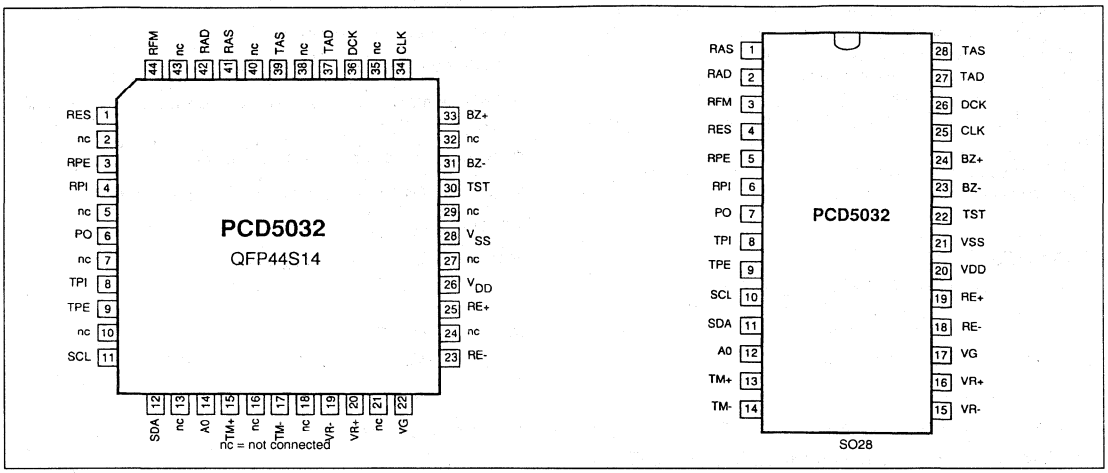


Figure 2. Pin Configuration

2.1 Pin Description

Pin	Name	I/O	Description
General			
26	V_{DD}	–	Positive power supply (2.7V – 5.5V)
28	V_{SS}	–	Negative power supply (0V)
22	VG	O	Analog signal ground
20	VR+	O	Positive reference voltage (1)
19	VR–	O	Negative reference voltage (1)
Digital			
34	CLK	I	Clock input
36	DCK	I	Data clock (ADPCM)
41	RAS	I	Receiver ADPCM sync (2)
42	RAD	I	Receiver ADPCM data input (2)
4	RPI	I	ReceiverPCM input (2)
3	RPE	O	Receiver PCM output enable (2)
44	RFM	I	Receiver fast mute (2)
39	TAS	I	TransmitterADPCM sync (2)
37	TAD	O	Transmitter ADPCM data output (2)
8	TPI	I	Transmitter PCM input (2)
9	TPE	O	Transmitter PCM output enable (2)
6	PO	O	PCM data output
12	SDA	I/O	I^2C serial data input / acknowledge
11	SCL	I	I^2C clock input
14	A0	I	I^2C address select pin
1	RES	I	Reset input (active high)
30	TST	I	Test mode (3)
Analog			
33	BZ+	O	Ringer output
31	BZ–	O	Ringer output
15	TM+	I	Transmitter audio input (microphone)
17	TM–	I	Transmitter audio input (microphone)
25	RE+	O	Receiveraudio output (earpiece)
23	RE–	O	Receiver audio output (earpiece)

NOTES:
1. Internally generated, intended for electret microphone supply.
2. Definition: Receiver= direction from ADPCM interface to earpiece; Transmitter = direction from microphone to ADPCM interface.
3. To be connected to Vss in normal application.

3.0 FUNCTIONAL DESCRIPTION

3.1 Digital interfaces (see Fig.1 Block diagram)

3.1.1 ADPCM interface

The ADPCM interface pins (RAD, TAD) carry 4 bits of serial data. Transmit and receiver data both are controlled by separate synchronization pins (RAS, TAS).

Upon detection of a high RAS signal (with rising DCK edge), the receiver will read 4 ADPCM bits on the next 4 high–to–low transitions of the DCK data clock. Likewise, upon reception of a high TAS signal, the transmitter will output 4 ADPCM bits on the next 4 low–to–high transitions of DCK. Figure 5 shows the timing diagram. During the time that the ADPCM data output (TAD) is not activated, it will be in a high impedance state, enabling a bus structure to be used in multi–line base stations. Input RAD has an internal pull–down resistor.

The minimum frequency on the DCK input is $f_{CLK}/54$. the maximum value equals the clock frequency, and any frequency in between may be chosen. The RAS signal controls the start of each conversion in a frame at an 8 kHz rate. The master clock 'CLK' must be locked to the frequency of 'RAS', with a ratio $f_{CLK} = 432 \times f_{RAS}$.

3.1.2 PCM Interface

To enable additional data processing in a base station both transmit and receive linear PCM data paths are accessible.

For the receive direction the PCM data is output on pin PO and read from pin RPI. For the transmit direction the PCM data is output on pin PO and read from pin TPI. To enable bus structures to be used in base stations the PCM output PO is in high impedance state when not active. Inputs TPI/RPI have internal pull–down.

In a typical (handset) application pin PO is directly connected to RPI and TPI. If additional data processing is required (e.g., echo cancellation in a base–station), then a data processing unit may be placed between PO and RPI or PO and TPI.

The data format is serial, 2's complement, MSB first. PO outputs 16 bits (14 data bits followed by 2 zeroes). TPI/RPI read 14 data bits. The bit frequency is 3456 kHz (CLK). Data output PO changes on the falling edge of CLK. Data inputs TPI/RPI are read on the rising edge of CLK (Figures 7,8).

For interfacing to digital signal processors signals TPE and RPE (both active low) mark the position of the transmit and receive PCM data on pin PO (Figure 6). TPE/RPE change on the rising edge of CLK.

Outputs RPE and TPE have low impedance only from half a CLK cycle before to half a CLK cycle after the active state. The rest of the time they are in high impedance state. Thus a wired–OR configuration can be made when only one DSP serial input port is used for reading both transmit and receive data. An external pull–up is required.

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In a typical (handset) application pin PO is directly connected to RPI and TPI. If additional data processing is required (e.g., echo cancellation in a base–station), then a data processing unit may be placed between PO and RPI or PO and TPI.

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For interfacing to digital signal processors signals TPE and RPE (both active low) mark the position of the transmit and receive pcm data on pin PO (Figure 6). TPE/RPE change on the rising edge of CLK.

Outputs RPE and TPE have low impedance only from half a CLK cycle before to half a CLK cycle after the active state. The rest of the time they are in high impedance state. Thus a wired–OR configuration can be made when only one DSP serial input port is used for reading both transmit and receive data. An external pull–up is required.

3.1.3 I²C Interface

The Philips I2C interface is used for programming gain and mode of operation.

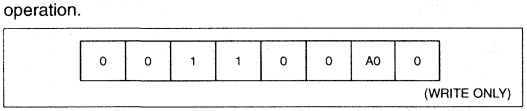


Figure 3. I²C Address

With the address select pin A0 it is possible to have two independently programmed ADPCM codecs in a base station (two outside lines). If more codecs are used in one base station then the address pin can be used as a 'select' signal. For timing of the I²C bus, see Philips Semiconductors' brochure "The I²C–bus and How to Use It".

Each function can be accessed by writing one 8–bit data word to the ADPCM codec. For this reason the 8–bit word is divided into two fields:

bit7, bit6 : function

bit5 to bit0 : value/setting.

Table 1. Overview of the I²C Programming Possibilities

Function	b7	b6	b5	b4	b3	b2	b1	b0
Operation Mode	0	0	–	–	TONE	PON	T1	T0
Receiver Control	0	1	RV2	RV1	RV0	RG2	RG1	RG0
Transmitter Control	1	0	ST1	ST0	MUTE	TG2	TG1	TG0
Ringer	1	1	BF2	BF1	BF0	BV2	BV1	BV0

Definitions

TONE : 'tone/ringer' section for tone generator output; tones can be sent to ringer or receiver DAC
PON : power-on (active)
T1-T0 : test loops
RG2-RG0 : receiver gain
TG2-TG0 : transmitter gain
RV2-RV0 : receiver volume
BV2-BV0 : tone volume
BF2-BF0 : tone frequency
ST1-ST0 : sidetone level

Programming the ADPCM codec is possible in active mode as well as in standby mode. A reset clears all I²C registers.

3.1.4 Fast Mute

The RFM (Receiver Fast Mute) pin enables fast muting of the received signal if erroneous data is present on the ADPCM interface.

Muting is done in the same manner as the receiver mute via I²C bus. The input data of the ADPCM decoder is blanked, so that the ADPCM decoder output signal goes to zero. To ensure immediate silence on the analog outputs RE+/RE–, the linear PCM input data of the receive filter is set to zero as well.

If the mute signal is switched off again, then the ADPCM decoder output settles gradually from zero to the appropriate PCM signal level. No audible clicks will occur.

The sidetone level is not affected by the mute function.

3.2 Analog Parts and I²C Programming

3.2.1 Input/Output

The analog input pins (TM+, TM–) can be connected directly to a microphone. For electret microphones capacitive coupling is required (Figure 11). The earpiece must be a low ohmic device (>100Ω differential).

The microphone and earpiece amplifiers have the possibility of gain control via the I²C interface. Further the sending and receiving direction can be muted separately. Analog gain control for the receive path can be set in steps of 1 dB. Digital volume control can be set in 6 dB steps. The following table gives an overview of the programming possibilities.

Table 2. Overview of Gain Control Options

Function	I²C-code	Description	Note
Receiver gain (relative)	01xxx101	-3dB	
	01xxx110	-2dB	
	01xxx111	-1dB	
	01xxx000	0dB	default
	01xxx001	+1dB	
	01xxx010	+2dB	
	01xxx011	+3dB	
	01xxx100	+4dB	
Receiver volume	01000xxx	0dB	defaults
	01001xxx	-6dB	
	01010xxx	-12dB	
	01011xxx	-18dB	
	01100xxx	-24dB	
	01101xxx	-30dB	
	01110xxx	-36dB	
	01111xxx	RX MUTE	
Transmitter gain (relative)	10xxx101	-3dB	
	10xxx110	-2dB	
	10xxx111	-1dB	
	10xxx000	0dB	default
	10xxx001	+1dB	
	10xxx010	+2dB	
	10xxx011	+3dB	
	10xxx100	+4dB	
Transmitter mute	10xx1xxx	TX MUTE	default off

3.2.2 Sidetone

With the I²C interface the (local) sidetone Level can be set to –12, –18, –24 dB, or switched off. See Table 3. The sidetone level is independent of the receiver volume control setting.

Table 3. Sidetone Level Options

Function	I²C-code	Description	Note
Sidetone	1000xxxx	No local sidetone	default
	1001xxxx	Level = -12 dB	
	1010xxxx	Level = -18 dB	
	1011xxxx	Level = -24 dB	

3.2.3 Tone Generator and Ringer

The PCD5032 contains a programmable tone generator which can be used for generating ringer tones (BZ+, BZ–) or local information tones in the receive path (RE+, RE–).

By setting the TONE bit (b3) in the operation mode register the tone output will be directed to the receiver DAC, otherwise the tones will be sent to the ringer output stage. Table 4 shows the possible frequency and volume settings.

Table 4. Tone Output Frequency/Volume Options

Function	I²C-code	Description	Note
Volume (rel)	11xxx000	Signal off	default
	11xxx001	-29 dB	sine wave
	11xxx010	-23 dB	sine wave
	11xxx011	-17 dB	sine wave
	11xxx100	-11 dB	sine wave
	11xxx101	-5 dB	sine wave
	11xxx110	0 dB	sine wave
	11xxx111	+4 dB	squarewave
Frequency	11000xxx	400 Hz	
	11001xxx	421 Hz	
	11010xxx	444 Hz	
	11011xxx	800 Hz	
	11100xxx	1000 Hz	
	11101xxx	1067 Hz	
	11110xxx	1333 Hz	
	11111xxx	2000Hz	

The ringer output (BZ) is differential and is intended for low ohmic devices. If the ringer is switched off then both outputs are low. The output signal is a pulse density modulated block wave (on a 32 kHz basic pulse rate) to generate a sinewave–like output signal, see Figure 4. Volume is controlled by changing the pulse width of each pulse. In the square wave mode a full square wave is generated and results in the maximum volume. The volume settings (in dB) are given for the first harmonic signal component.

3.3 Modes of Operation

The ADPCM codec has three modes of operation, a normal mode and two loop modes. See the table below for details on setting these modes. Also the standby and active mode are set via the I²C bus.

Table 5. Modes of Operation

Function	I²C-code	Description	Note
Standby mode	00xxx0xx	Power down	default
Active mode	00xxx1xx	Active	
Set Normal mode	00xxxx01	Normal operation	default
Set Loop 1	00xxxx01	Loopback on ADPCM side and on PCM side without using ADPCM transcoder	
Set Loop 2	00xxxx10	Loopback on TM+/TM– to RE+/RE– through ADPCM transcoder	

3.3.1 Standby Mode

After a reset the ADPCM codec will by default be in standby mode. All I²C settings will be cleared. PON=O sets the codec in standby

mode. In standby mode all circuits are switched off, except for the I^2C interface. Before going to standby mode the PCD5032 performs a reset of the ADPCM transcoder, digital filters and auxiliary logic functions. The I^2C interface registers are not cleared.

3.3.2 Active Mode

PON=1 in the operation mode register sets the codec in active mode. In active mode the ADPCM codec can be operated either in normal mode or one of the two test loops may be selected.

3.3.3 Test Loops

Both test loops can be used for test or evaluation purposes.

Loop 1 is intended for testing the audio path and A/D, D/A converters, the ADPCM transcoder is not addressed in this mode. The ADPCM data is directly looped back towards the radio interface. The PCM data is looped from transmit filter output to receive filter input.

Loop 2 is intended for testing the complete audio path including ADPCM encoding and decoding.

3.3.4 Reset (input RES)

After an external reset pulse the circuit will perform an internal reset procedure. The reset pulse must be active during at least 10 CLK cycles. 125 µs (one 8kHz period) after RES has gone low, the internal reset is completed and the PCD5032 goes into standby mode. At that moment the ADPCM codec is ready to be programmed.

A reset clears all I^2C registers and resets the ADPCM transcoder, digital filters and auxiliary logic functions.

4.0 CHARACTERISTICS

4.1 MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	RATING	UNITS
Supply voltage $V_{DD} - V_{SS}$	-0.5 to +6.5	V
Voltage at any pin except V_{DD}	V_{SS} -0.5 to V_{DD} +0.5	V
DC current through pin: V_{DD}, V_{SS} BZ+, BZ–, RE+, RE– other pins	 150 150 50 10	mA
Total power dissipation	500	mW
Operating ambient temperature	–25 to +70	°C
Storage temperature	–65 to +150	°C

Handling

Inputs and outputs are protected against electrostatic discharge in normal handling. ESD protection according to Human Body Model is guaranteed up to 800 V. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see'Handling MOS Devices').

4.2 ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 V, CLK = 3456 kHz

PARAMETER	LIMITS			UNITS
	MIN	TYP	MAX	
General				
Operating temperature	-25	25	70	°C
Supply voltage	2.7	3.0	5.5	V
Supply current (T_{amb} = 25°C)[1] Active (no load) Standby	 – –	 7 20	 14 100	 mA µA
Leakage current inputs	–	–	1	µA
Analog ground	0.48	0.5	0.52	xV_{DD}
Reference voltage VR+[2]	0.8	1.0	1.2	V
Reference voltage VR–[2]	–0.8	–1.0	–1.2	V
Digital I/O				
V_{IH}[3]	0.7	–	1.0	xV_{DD}
V_{IL}[3]	0	–	0.3	xV_{DD}
V_{OL}[3]	–	–	0.4	V
V_{OH}[3]	V_{DD} – 0.4		V_{DD}	V
Pull-down resistor[3]	–	150	–	kΩ
DCK frequency[4]	f_{CLK}/54 = 64	–	f_{CLK}	kHz
RAS, TAS frequency[4]	–	8	–	kHz
I²C Bus Timing				
SCL clock frequency	–	–	100	kHz
Tolerable spike width	–	–	50	ns
Bus free time	4.7	–	–	µs
Start condition set–up time	4.7	–	–	µs
Start condition hold time	4.0	–	–	µs
SCL LOW time	4.7	–	–	µs
SCL H IGH time	4.0	–	–	µs
SCL and SDA rise time	–	–	1.0	µs
SCL and SDA fall time	–	–	0.3	µs
Data set–up time	250	–	–	ns
Data hold time	0	–	–	ns
Stop condition set–up time	4.0	–	–	µs
Analog Inputs[5]				
TM+ / TM– input impedance[6]	–	125	–	kΩ
Nominal input level[7]	–	12	–	mV_{RMS}
Maximum input signal[8]	–	56	–	mV_{RMS}
Min. voltage gain	–4	–3	–2	dB
Max. voltage gain	+3	+4	+5	dB
Stepsize voltage gain	–	1	–	dB
TX harmonic distortion[9]	–	–	–40	dB

ELECTRICAL CHARACTERISTICS (conitnued)

PARAMETER	LIMITS			UNITS
	MIN	TYP	MAX	
Analog Outputs				
Receiver audio output:				
output impedance[6]		10		Ω
signal level at 0 dBm0[10]		550		mV_{RMS}
signal level at 3.14 dBm0[11]		1250		mV_{RMS}
min. gain	–4	–3	–2	dB
max. gain	+3	+4	+5	dB
gain step size	–	1	–	dB
volume control range	–36	–	0	dB
volume stepsize	–	6.0	–	dB
RX harmonic distortion[12]	–	–	–40	dB
Ringer output:[5,13]				
output impedance	–	14	29	Ω
volume control range	–29	–	+4	dB

FILTER CHARACTERISTICS

PARAMETER	LIMITS			UNITS
	MIN	TYP	MAX	
Transmitter				
Passband ripple (300–3000Hz)	–	–	0.5	dB
Frequency response				
f = 50 Hz	–35			
f = 3400 Hz			–2	dB
f = 4600 Hz	–35			
f = 8000 Hz	–60			
Analog-to-Digital Converter				
Signal-to-noise ratio (Figure 12)[6,14]		35		dB
Digital-to-Analog Converter				
Signal-to-noise ratio (Figure 12)[6,14]		35		dB
Group Delay				
Transmitter[15]			400	µs
Receiver[15]			525	µs
Group Delay Distortion				
See Figure 9				

NOTES: +3.14 dBm0 is the maximum signal level on the PCM interface. Specifications are valid in active mode (except standby current).

1. I_{DD} active measured with all inputs to V_{SS}, except CLK, DCK connected to 3.456 MHz, and RAS, TAS connected to 8 kHz. I_{DD} standby measured with all inputs connected to V_{SS}, except TMP, TMM left open. All outputs left open for both cases.
2. The ref. voltage is available on VR+ and VR– and is measured with respect to VG. The voltage outputs are intended for electret microphone supply, and can deliver 400 µA.
3. Digital inputs and outputs are CMOS–levels compatible. The outputs can sink or source 1 mA. Pull–down resistors are present at pins RPI, TPI, TST, RAD.
4. Any frequency between min and max is allowed for DCK. The signals CLK and RAS/TAS must be frequency–locked. and wilt have a ratio $f_{CLK} / f_{RAS} = 432$.
5. All analog input/output voltages and impedances are measured differentially. The circuit is designed for use with an electret microphone.
6. Frequency band is 300 Hz – 3400 Hz. Maximum load capacitance = 100 pF differentially, or 200 pF each pin.
7. Nominal signal level gives –10 dBm0 on the PCM interface (G.71 1/G.712). Value given for TX gain setting 0 dB.
8. Maximum signal level gives +3.14 dBm0 on the PCM interface, with larger input signals the digital output signal will be saturated. Value given for TX gain setting 0dB.
9. TX gain setting = 0 dB and input signal level 40 mV_{RMS} (will generate 0 dBm0 signal level on PCM interface according to G.711).
10. PCM signal level is 0 dBm0 and RX gain setting 0 dB. With a load of 300 Ω between RE+ and RE– the given signal level results in an output power of 1 mW. The maximum output current is 10 mA.
11. PCM signal level is +3.14 dBm0 and RX gain setting +4 dB. The maximum output current is 10 mA.
12. PCM signal level is 0dBm0 (G.711).
13. For maximum output power the load resistance should equal the typical output impedance (specified at I_{LOAD} – 20 mA). The minimum load resistance is limited by the "Maximum Ratings".
14. Measured with psophometric filter (CCITT G.223). Only fulfilled at V_{DD} noise level smaller than 40 mV_P (0 – 20 kHz). Measured on sample basis at V_{DD} = 3.0 V, temperature = 25°C, compliant with G.712. Signal level is –40 dBm0 on PCM interface (0.4 mV_{RMS} on analog input). Gain setting is 0 dB.
15. Group delay includes ADPCM / PCM conversion; signal frequency = 1.5 kHz. Figure is given for RAS/TAS signals at the same moment.

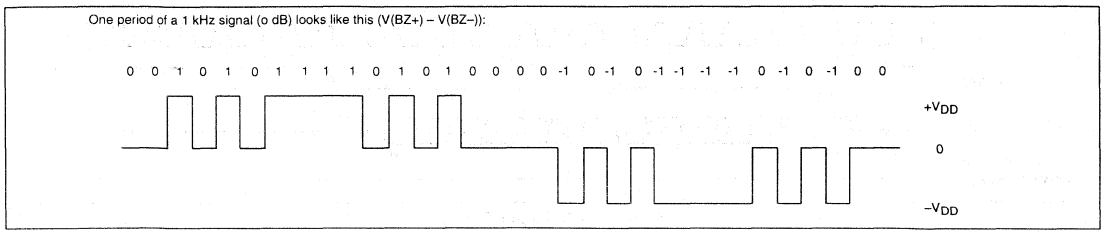


Figure 4. Tone Output Example

TIMING DIAGRAMS

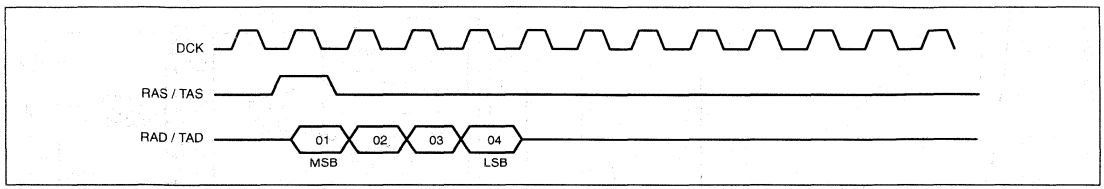


Figure 5. ADPCM Timing

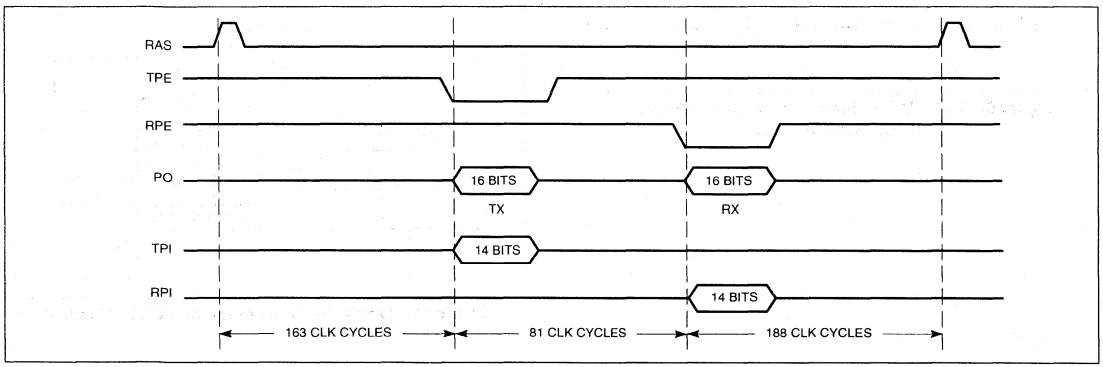


Figure 6. PCM Timing

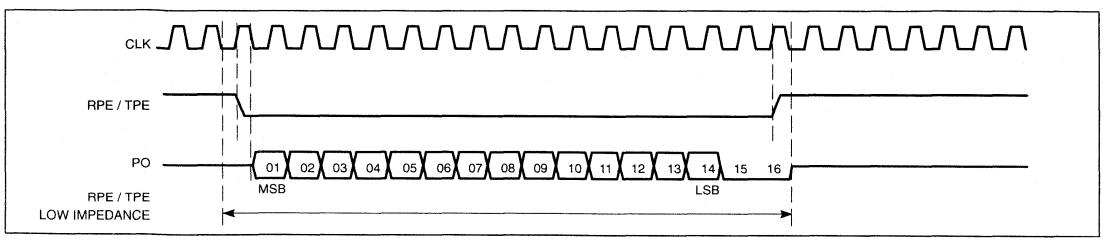


Figure 7. PCM Output Timing

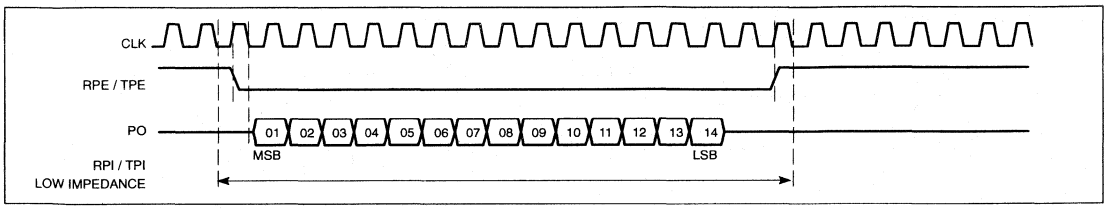


Figure 8. PCM Input Timing

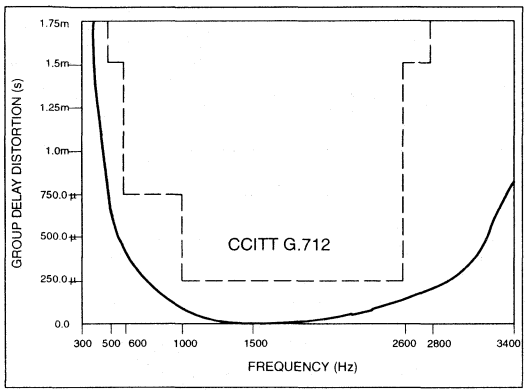


Figure 9. Group Delay Distortion Transmit + Receive (Loop Measurement)

APPLICATION INFORMATION

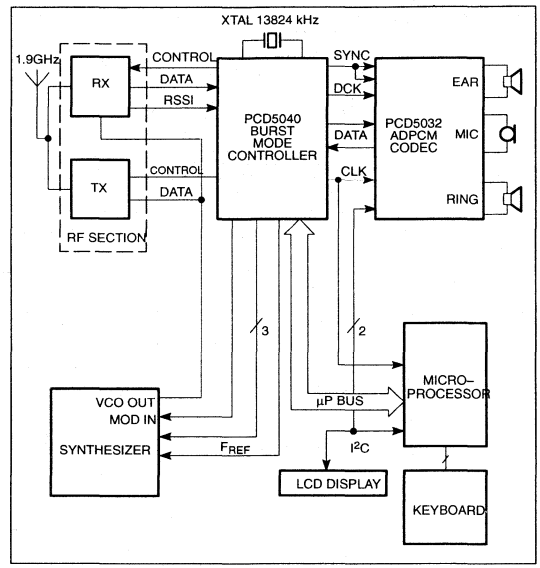


Figure 10. Typical Block Diagram for a DECT Handset

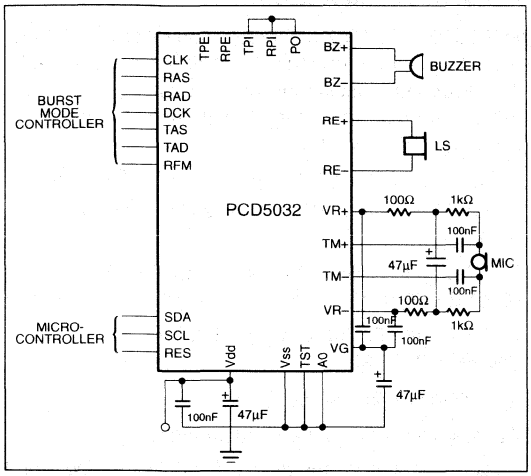


Figure 11. Typical Handset Application Diagram for the PCD5032

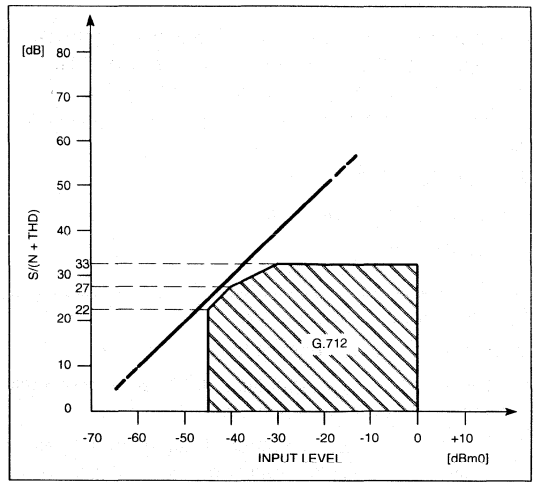


Figure 12. Typical Performance of AD and DA in Cascade (Loop 1)

DECT burst mode controller PCD5041

1 FEATURES

- On-chip pre-programmed Communication Controller with embedded firmware for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning, and control of the device's other functional units.
- Portable Part (PP) modes
- TDMA frame (de)multiplexing
- Encryption
- Scrambling
- CRC generation and checking
- Beacon transmission control (by P00 packets)
- On-chip comparator for receive data slicer function (only available in the LQFP80 package)
- Switches up to12 active speech channels from speech interface to 1152 kbit/s. radio interface, and vice versa
- Dual channel speech/data capability
- Received Signal Strength Indication (RSSI) measurement, with on-chip 6-bits peak/hold detector
- Quality control report
- Digital Phase Locked Loop (DPLL)
- Synchronization (handset to active bearer, base station to cluster of RFPs)
- Seamless handover procedure
- Fast (hardware) and slow (software) mute function
- 1 kbyte extended RAM memory
- On-chip crystal oscillator (13.824 MHz)
- Programmable microcontroller clock frequency
- Programmable interrupts
- Watchdog with two programmable time-outs
- Low power consumption in standby mode
- Low supply voltage (2.7 to 5.5 V)
- SACMOS technology.

2 GENERAL DESCRIPTION

The PCD5041 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT Physical Layer and MAC Layer time-critical functions, for use in DECT handset products which comply with the following standards (and updates):

- DECT CI part 2: Physical layer (DE/RES 3001-2)
- DECT CI part 3 : Medium Access Control layer (DE/RES 3001-3)
- DECT CI part 7: Security features for DECT (DE/RES 3001-7)
- DECT CI part 9: Public Access Profile (DE/RES 3001-9).

The PCD5041 has interfaces to:

- ADPCM CODECs in the handset mode
- A radio transceiver; the interface is fully decoded, and includes power-down signals
- An external microcontroller.

The PCD5041 is designed to be connected to an ADPCM CODEC (Philips' PCD5032, for example) and an 80C51-type microcontroller. Other microcontrollers (e.g. 68000) and CODECs can also be supported.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5041H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2
PCD5041HZ	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4 BLOCK DIAGRAM

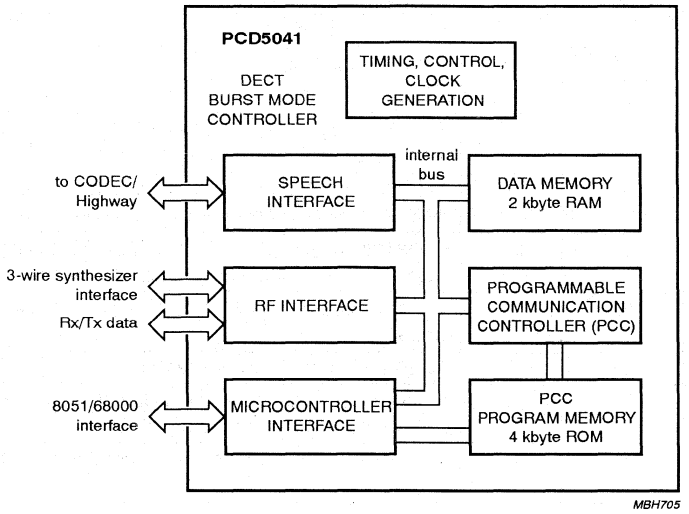


Fig.1 Block diagram.

5 PINNING (see Figs 2 and 3)

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
AD0 to AD7	1 to 8	80, 1, and 3 to 7	I/O	address/Data bus
ALE	9	9	I	address latch enable
$\overline{CS}$	10	11	I	chip select (active LOW)
A8 to A10	13 to 11	14 to 12	I	address bus
V_{DD1}	14	15	P	positive supply 1
PROC_CLK	15	16	O	microcontroller clock; programmable from $f_{CLK}/64$ to f_{CLK}, where f_{CLK} is the crystal oscillator frequency
V_{SS1}	16	17	P	negative supply 1
XTAL1	17	20	I	crystal oscillator input
XTAL2	18	21	O	crystal oscillator output
V_{SS2}	19	22	P	negative supply
RESET_OUT	20	23	O	watchdog timer output; intended to reset the external microcontroller when expired
$\overline{RD}$	21	24	I	read (active LOW)
$\overline{WR}$	22	25	I	write (active LOW)
$\overline{RDY}$	23	26	O	ready signal (active LOW), to initiate wait states in the microcontroller (open drain)

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
$\overline{INT}$	24	27	O	interrupt (active LOW)
CLK100	25	29	O	100 Hz frame timer
V_{SS3}	26	31	P	negative supply 3
DO	27	32	O	3-state data output on the speech interface
FS3	–	33	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS1	28	34	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS4	–	35	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS2	29	36	O	8 kHz framing signal to ADPCM CODEC 2 in the base station mode
DI	30	37	I	data input on the speech interface
DCK	31	38	O	simple base + handset; 1152 kHz data clock (output), otherwise 2048 kHz data clock (input) signal
CLK3	32	39	O	3.456 MHz clock (nominal value, used to adjust system timing)
ANT_SW	33	40	O	selects one of two antennas
$\overline{T\_ENABLE}$	34	41	O	Transmitter Enable (active LOW)
T_POWER_RMP	35	43	O	Transmitter Power Ramp control
RMT_STAT	36	44	I	serial 8-bit data can be read in for each slot; REMote radio
SYNTH_LOCK	37	45	I	lock indication from synthesizer
V_{SS4}	38	46	P	negative supply 4
REF_CLK	39	47	O	reference frequency for the synthesizer, i.e. the crystal oscillator clock f_{CLK}
V_{DD2}	40	48	P	positive supply 2
S_ENABLE	41	49	O	synthesizer enable
S_CLK	42	51	O	clock signal, to be used with S_DATA
S_DATA	43	52	O	serial data to the synthesizer
S_POWER_DWN	44	53	O	synthesizer power-down control
VCO_BND_SW	45	54	O	VCO bandswitch control signal
1200 HZ	46	55	O	control signal for dual synthesizer schemes
T_DATA	47	56	O	serial output data to transmitter
SET_OFF_IN	48	57	I	switches off the crystal oscillator, and prevents all RF signals from becoming active
TEST1	49	58	I	selects various test modes.; normal operation set to 0
RSSI_AN	50	60	I	analog signal (for basic DECT systems), peak signal strength measured after a lowpass filter
TEST2	51	–	I	selects various test modes; normal operation set to 0
TEST3	52	61	I	selects various test modes; normal operation set to 0
R_DATA	53	63	I	receive data

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
$\overline{R\_ENABLE}$	54	64	O	receiver enable (active LOW)
R_POWER_DWN	55	65	O	receiver power-down
$\overline{COMP\_NE}$	–	66	I	digital input comparator not_enable (active LOW)
SLICE_CTR	56	67	O	slice time constant control
COMP_OUT	–	68	O	digital comparator output
V_{DD3}	57	69	P	positive supply 3
V_{SS5}	58	70	P	negative supply 5
COMP_INM	–	71	I	analog comparator input negative
V_{REF}	59	72	I	reference input for the A/D converter
COMP_INP	–	73	I	analog input positive
$V_{DD(RAM)}$	60	74	P	power supply for data RAM
SYNCPORT	61	76	I/O	in the base station the signal is the SYNCPORT
RESET	62	77	I	BMC master reset signal
MEM_SEL	63	78	I	selects PCC program memory at microcontroller interface
EN_WATCHDOG	64	79	I	enable watchdog input; when HIGH, the watchdog timer of the BMC is enabled

Notes

1. Un-referenced pins for the LQFP80 package are not connected. FS3, FS4 and the comparator signals are only available in the LQFP80 package.
2. **All** signals which are input or I/O, and which can be floating, need to be pulled up to V_{DD} or down to V_{SS} in order to protect the device against cross-currents. Exceptions are VREF and RSSI_AN, which do not have to be protected.

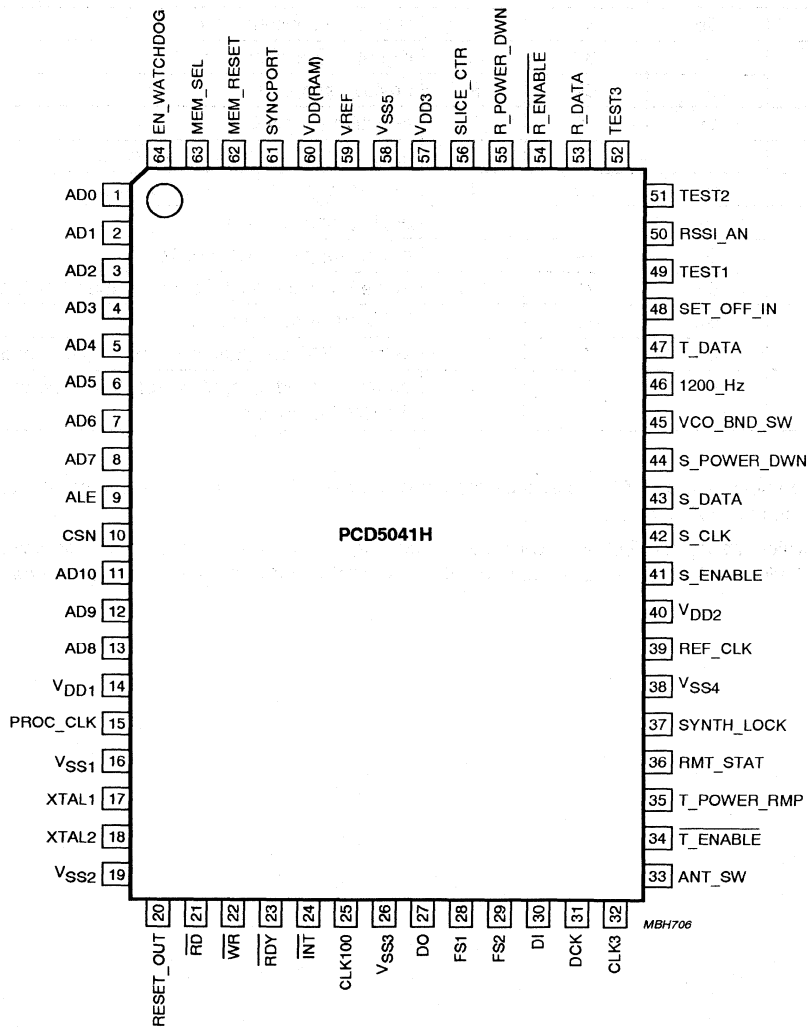


Fig.2 Pin configuration, PCD5041H (QFP64 package).

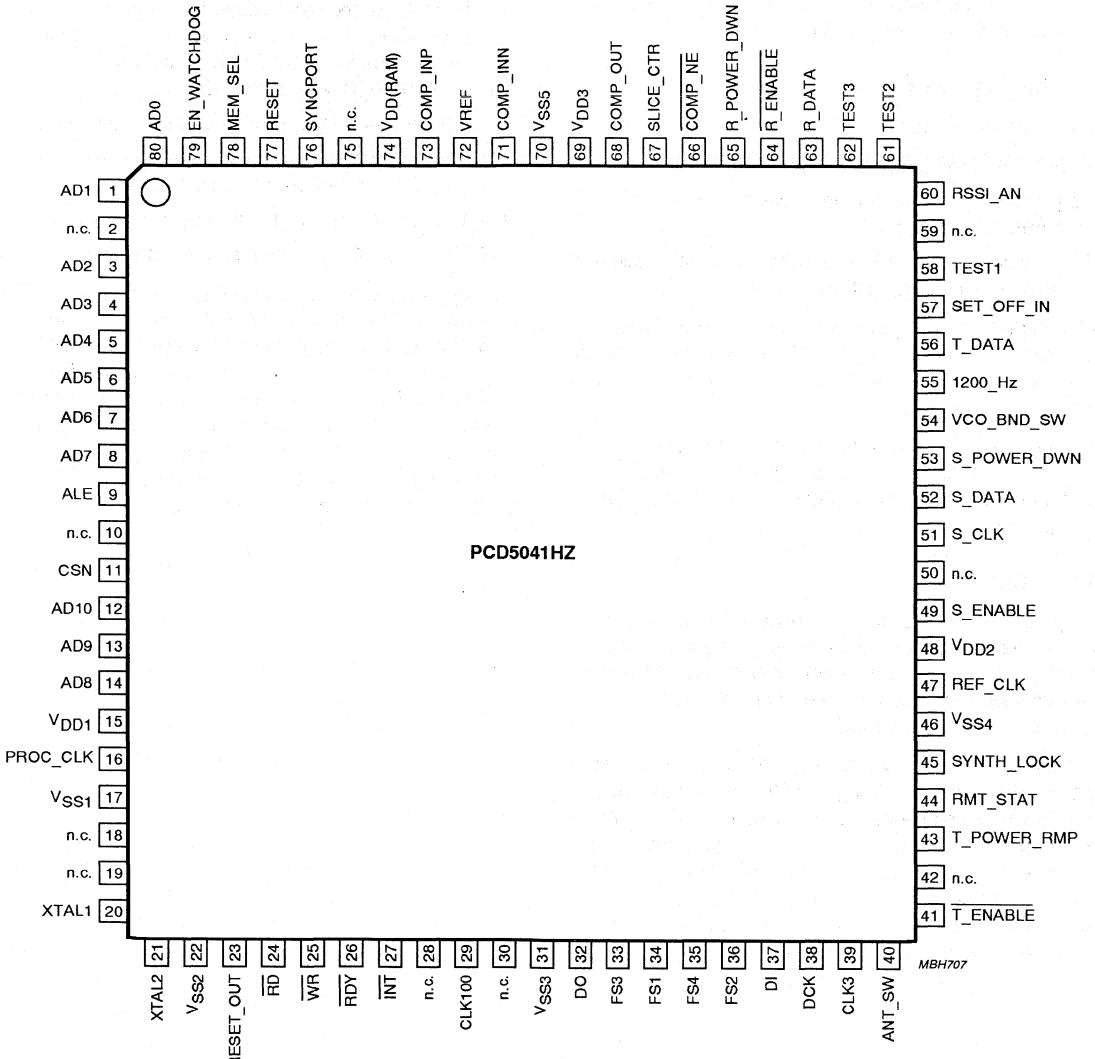


Fig.3 Pin configuration, PCD5041HZ (LQFP80 package).

6 FUNCTIONAL DESCRIPTION (see Fig.1)

The PCD5041 has dedicated hardware blocks containing logic for time-critical functions requiring bit or byte-time accuracy. Other functions requiring only slot-time accuracy are performed by software in the Programmable Communication Controller (PCC). This approach offers maximum flexibility during prototyping.

6.1 Internal bus and data memory

6.1.1 INTERNAL BUS

The function of the internal bus is:

- To provide access for all functional blocks to the common data memory
- To provide access for the microcontroller-interface and the PCC to all other functional blocks.

All functional blocks (speech-interface, RF-interface, microcontroller-interface and PCC) can autonomously use the internal bus to communicate with the common data memory.

A bus controller is used to handle the bus priority mechanism. When several blocks request access simultaneously, the request with the highest priority is handled first.

6.1.2 DATA MEMORY

A large part of the data memory is used for the bit rate adaptation between the DECT radio interface and the speech interface. The data memory also acts as the main communication interface between the external microprocessor and the PCC.

In a handset, the device uses only 1 kbyte of the common data memory. The remaining 1 kbyte can be used by the microcontroller as an extended data memory for the higher layer software. The microcontroller is not aware of the fact that it is sharing the memory with the PCD5041. From the microcontroller's point of view, the PCD5041's microcontroller-interface plus the common data memory behave as a standard RAM device.

6.2 Clock generation and correction (see Fig.4)

The device has an on-chip 13.824 MHz crystal oscillator. From this source, a few frequencies are derived for internal and external use. Frequencies generated for external use are:

- 13.824 MHz for the synthesizer reference (pin REF_CLK). This output is only provided if the synthesizer power-down control (output on pin S_POWER_DWN) is not selected.
- 0.144 to 13.824 MHz for the microcontroller clock (pin PROC_CLK)
- 3.456 MHz for the ADPCM CODEC (pin CLK3)
- 1200 Hz (pin 1200_HZ) for dual synthesizer switching
- 100 Hz (pin CLK100) indicates start of frame.

Nominally, the frequency on pin CLK3 is 3.456 MHz. This frequency is obtained by dividing the crystal frequency by 4. Sometimes, the crystal frequency will be divided by 3 or by 5, to synchronize the combination of the ADPCM CODEC and the device to an external source. For the handset application, the PCD5041 can be synchronized to the incoming radio channel, using the 'slot synchronization' event of one active channel, so the handset is locked to one base station.

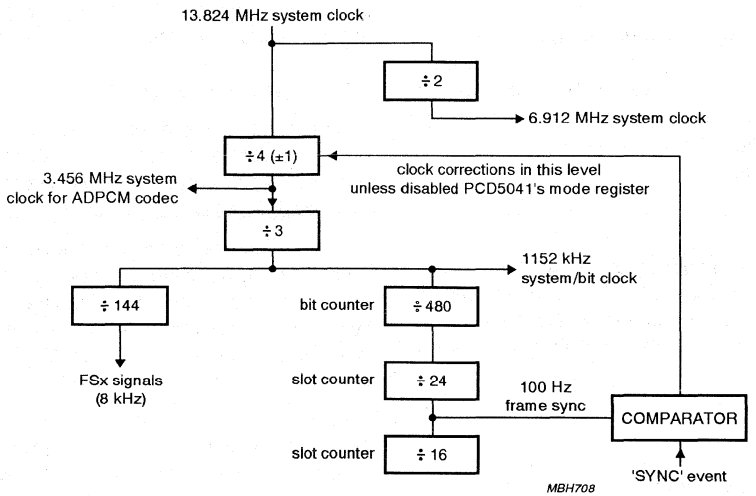


Fig.4 Internal clocking scheme of the PCD5041.

6.3 Programmable communication controller and program memory

6.3.1 PCC

The PCC is a RISC-type controller and is used to control functions which are slot-time accurate. It is well suited for bit manipulation, and runs at a clock frequency of 6.912 MHz (equivalent to 3.4Mips). After finishing a task, it switches to a power saving state, from which it returns after a pre-programmed time.

6.3.2 PCC FUNCTIONS

The most important functions of the PCC are to:

- Perform the appropriate actions on received messages: PMID and FMID checking, RFPI checking, TBC handling
- Prepare A-field messages for transmission
- Prepare the RF-interface for the coming slot
- Perform the procedures for RSSI and set-up scan, maintain scan counters and timers, assemble the RSSI field in the common data memory
- Filter events and indicate them to the microcontroller by interrupt.

6.4 Speech interface

The speech interface block performs the following functions:

- Connection to a 1 152 kbit/s interface in a handset and a simple base station in the so called '12 slot mode'
- Autonomous storing/fetching of ADPCM speech data in/from the PCD5041's common data memory, using internal addressing logic
- Muting of speech data
- Local call.

6.4.1 12-SLOT MODE

This is the normal operating mode for the PCD5041. The 12-slot mode is selected if up to 4 ADPCM CODECs are connected to the PCD5041, where the PCD5041 is the master of these CODECs. In a handset, or in a simple base stations which is connected with up to 4 analog lines to the public network, the PCD5041 is master of the CODECs. Each CODEC is connected with a separate framing reference signal (FS1 to FS4) to the PCD5041. In the QFP64 package, 2 framing signals FS1 and FS2 are available, whereas in the LQFP80 package 4 framing signals can be used (FS1 to FS4). When more CODECs

are to be connected, the FS5 to FS12 signals have to be generated externally. When using the framing signals FS1 to FS4, no interface logic is required when using the PCD5032 ADPCM CODEC.

A speech-slot control table is used to determine where to store/fetch speech data for transmission and reception. The hardware speech-interface is capable of addressing the right speech buffer for the relevant speech slot, and will maintain a counter carrying the offset to the correct stored/fetched address.

6.4.2 MUTING

Due to various reasons the quality of the incoming speech data may be degraded significantly. By muting the speech data, these disturbances are not audible (or are less audible) to the user. The PCD5041 performs two types of muting:

- Fast muting
- Slow muting.

Fast muting, which is performed by the PCD5041 automatically, is nothing more than a repetition of the previously received frame (80 speech samples) to the ADPCM CODEC. It is issued if no Sync word was detected. Slow muting is issued by the microcontroller, after having detected a degradation of quality. A slow mute is implemented as a continuous '0000' nibble transmission to the ADPCM CODEC, until slow mute is released.

6.4.3 LOCAL CALL

A local call option is implemented, in order to loopback data from one CODEC to another CODEC, and vice versa, see Fig.5.

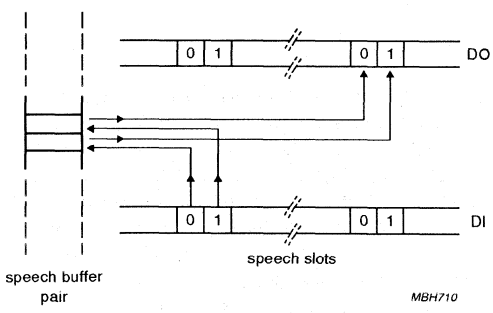


Fig.5 Local call switching on speech interface.

6.5 RF interface

Most of the functions performed by the RF interface are under control of the PCC. Specifically, the processing of non-speech data and the programming of functions and registers is done via the PCC.

6.5.1 SERIAL TRANSMITTER

The serial receiver processes the data, which comes from the RF section, and which is already filtered by the synchronization part. The data is latched, using the recovered data clock.

The serial receiver will collect the complete A-field and B-field and store it in the common data memory. Before the A-field is received, the A-field start address is programmed by the PCC. Upon reception of A-field nibbles, the address is updated by the serial receiver. Meanwhile, the PCC will program the B-field start address.

In Fig.6 the data flow in the serial receiver is shown. Note that almost no decoding of messages is required. Only the header of the A-field needs to be decoded to check if a ciphered message is being received or transmitted, which requires the ciphering to be switched on in the A-field also.

6.5.2 SERIAL RECEIVER

The serial transmitter performs the reverse of the receiver functions. Several blocks used in the receiver are also used in the transmitter. Amongst these are the CRC-generators, the scrambler, and the address registers. Figure 7 shows the serial transmitter structure.

By transmitting the X-CRC twice, the Z-field is transmitted. The handling of the address registers is the same for the transmitter. Transmission of the synchronization sequence (S-field) is done using the same method as the A-field and B-field. The S-field is stored in the common data memory and will be fetched by the transmitter, just before transmission.

Two additional functions are not shown in Fig.7:

- In the handset the data in the serial transmitter may be advanced by a programmable number of bit periods. This is done to compensate for the delay in the RF section
- The transmitted data can be inverted (using a switch in the PCD5041 mode register), in order to connect the PCD5041 to VCOs requiring negative modulation.

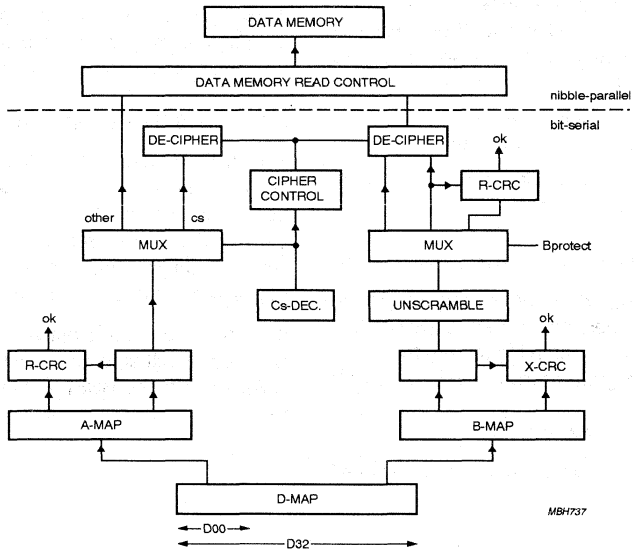


Fig.6 Serial receiver structure.

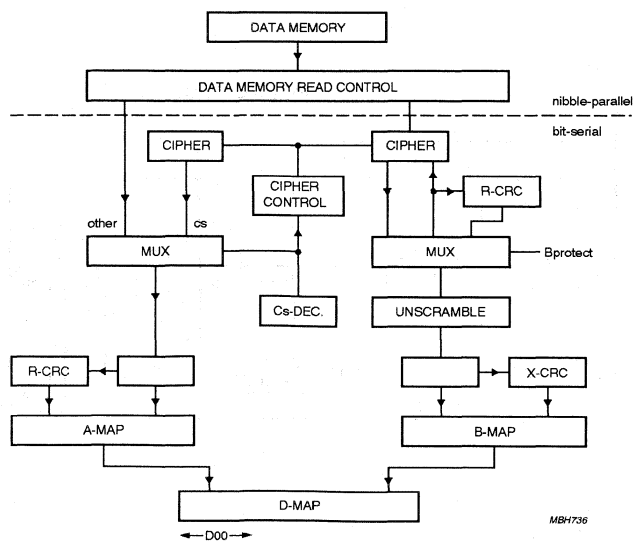


Fig.7 Serial transmitter structure.

6.5.3 SEAMLESS HANDOVER

Seamless handover guarantees that when speech information is switched from one slot to another, no speech samples are lost, added or displaced. Seamless handover is achieved in the RF interface by:

- Using a look-up table containing the correct start addresses of the B-fields in the data memory
- The RF receive and transmit blocks move data to/from the data memory block in 4-bit nibbles.

6.5.4 RF CONTROL SIGNALS

The timing of the control signals to the RF section is fixed, but such that an RF delay between 1.5 and 7 μs can be tolerated. Only the transmitter ramp signal and the synthesizer enable are programmable within certain limits.

6.5.5 SYNTHESIZER PROGRAMMING

To program a synthesizer, a 3-wire serial interface is used. The signals on this interface are:

- S_ENABLE (enable)
- S_CLK (clock)
- S_DATA (data).

To program various types of synthesizers, a 3-byte shift register is present. Three data formats are supported: 8, 16 or 24 bit words can be selected. The transfer of data from a frequency table in the common data memory to the shift register is under control of the PCC.

6.5.6 RSSI MEASUREMENT (see Fig.8)

The RSSI measurement in the PCD5041 RF-interface block is done in 3 parts: a peak/hold detector, a 6-bit A/D converter, and an RSSI control unit, which controls the peak/hold detector and the A/D converter. Once per slot time, a sample is fetched by the PCC and saved in the appropriate area of the common data memory.

If the radio receiver is active in a particular time slot, the RSSI value will automatically be measured in that slot. Adjustment to the RSSI_AN input level can be made with VREF.

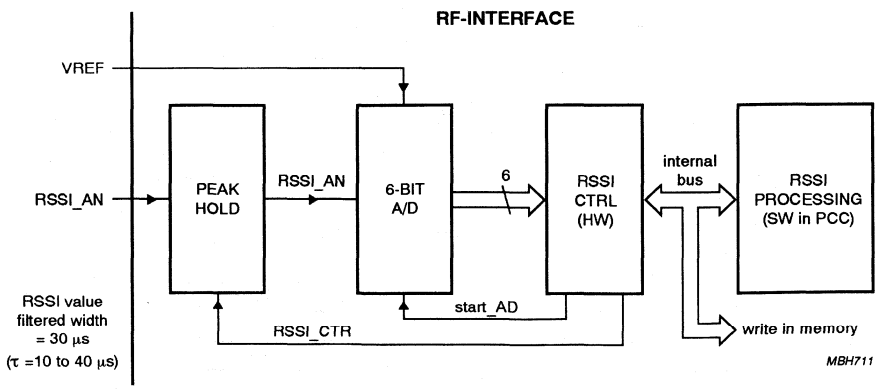


Fig.8 RSSI measurement path.

6.5.7 LOCAL CALL SWITCHING (see Fig.9)

The PCD5041 provides a local call switching function in the base station. It stores incoming speech nibbles in the common data memory, in the area reserved for that particular receive slot. Then, during the transmit phase, it passes the start pointer of the same data memory area to the transmit block. Thus, the speech data is echoed to the other user. To handle quality degradation for local calls, a mute can be performed at the RF side of the speech buffer.

6.5.8 DATA SYNCHRONIZATION (see Fig.10)

The data synchronization is done in 2 phases:

- Bit synchronization
- Sync word detection.

Bit synchronization is done using a Digital PLL (DPLL), with an oversampling factor of 12, i.e. the DPLL is running at 12 times the data rate. The output from the DPLL is a receive clock signal (RxC), which acts as the enable for a 20-bit shift register.

Sync word detection is achieved by checking the incoming data pattern with the expected synchronization field pattern, using a correlator.
The correlator has a programmable threshold, so it can accept bit errors in the sync field pattern up to the threshold level. Furthermore, the correlator window is programmable. This means that 'SlotSync', which indicates the slot synchronization event, can be detected only during a certain period (the time window).

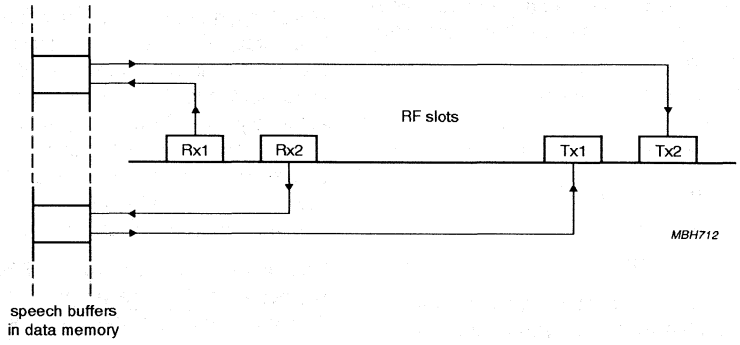


Fig.9 Local call switching on the RF-side.

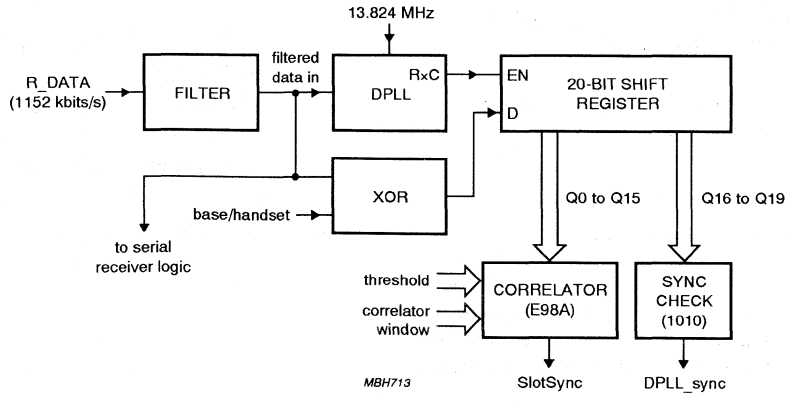


Fig.10 Schematic of the receiver synchronization part.

The 'DPLL_sync' indication should only be used, when 'SlotSync' is active. It indicates that the last 4 bits of the pre-amble field (the training sequence) are received correctly, and thus indicates that the DPLL was in lock (synchronized) in time. If the 'SlotSync' is active, and the 'DPLL_sync' is not, then a sliding interferer might have been detected.

If 'SlotSync' is not detected, effectively no data is received in that slot. This implies a 'fast mute' because speech data received in the previous frame is not destroyed.

6.5.9 CIPHERING MACHINE

The description of the cipher machine is subject to confidentiality. The specification of its algorithms are delivered by ETSI under the terms of a Non-Disclosure Agreement.

The cipher machine is under control of the TBC, which is implemented in the PCC. The cipher machine generates 2 fields of ciphering bits:

- A_cipher (40 bits) for A-field messages (ciphers tail only)
- B_cipher (320 bits) for speech in B-field.

The transmitted ciphered bits are then:

- A_ciphered: = A XOR A_cipher
- B_ciphered: = B XOR B_cipher.

On reception by the peer end point, deciphering consists of the same operation thanks to the synchronous generation of A_cipher and B_cipher.

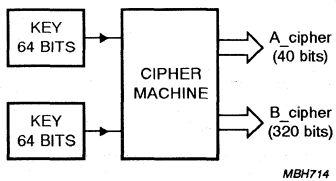


Fig.11 Cipher machine and its sources.

The cipher machine is time-multiplexed on a slot basis. Initially, the Initialisation Vector (IV) and the key must be loaded into the cipher machine. Transfer of the IV and key from the common data area to the cipher machine is done automatically by the cipher machine. The contents of the memory space where IV and key are found, are the responsibility of the PCC, and the external microprocessor.

6.5.10 COMPARATOR/DATA SLICER ON PCD5041HZ

The PCD5041HZ contains a comparator/data slicer. The comparator is a stand-alone circuit. No connections other than power supply are made internally. The comparator can be used as a data slicer for the receiver input. The delay requirements listed in Chapter 8 were derived from this application. Another use of the comparator is in a successive approximation A/D converter to indicate battery low-voltage condition, or in a power-on-reset circuit.

When the signal $\overline{\text{COMP\_NE}}$ is LOW the comparator is enabled. When $\overline{\text{COMP\_NE}}$ is HIGH the comparator is disabled, and the circuit consumes no power. If the comparator is used as a data slicer for the receiver input, the R_DATA is connected to COMP_OUT, the $\overline{\text{COMP\_NE}}$ is connected to $\overline{\text{R\_ENABLE}}$, both connection are done externally. The pin COMP_INP is connected to the RF mixer. A proper bias voltage (from the slicer time constant control circuit) is connected to COMP_INM. Another use of the comparator is in a successive approximation A/D converter for battery voltage detection.

The pins are protected against ESD damaging, with a protection diode to the positive and negative supply rail. The input pin $\overline{\text{COMP\_NE}}$ has a pull-up resistor which keeps the comparator in power-down mode by default.

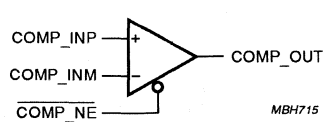


Fig.12 Circuit schematic of the comparator/data slicer.

6.6 Microcontroller Interface

6.6.1 Function of the microcontroller interface

The microcontroller interface will provide the following services.

- Direct interface to processors which have an INTEL-8051 compatible interface
- General interface to processors that can handle 'wait states' e.g. 68000-family; in this case glue logic is required
- Processor clock signal of which the frequency is programmable in order to adjust instantaneously processor performance to processor work load
- A programmable interrupt register
- A watchdog timer with time-out periods of 1.25 or 82 seconds, depending on the programming.

The microcontroller can address the PCD5041 as any other RAM memory connected to the microcontroller bus. By writing the 'Interface-Mode Register', the microcontroller can select the interface mode and its own clock frequency.

6.6.2 Microcontroller interrupts

The function of microcontroller Interrupts is to make optimal use of the microcontroller's processing power, and to achieve optimal cooperation between time-critical tasks and less time-critical tasks both executed in software. Three registers are available to handle interrupts. These are:

- Interrupt Event Register
- Interrupt Enable Register
- Interrupt Reset Register.

These registers are to be regarded together. Corresponding bits in these registers relate to one and the same event. Bits in the Interrupt Event Register are set by the PCC and are to be reset by the external processor by writing '1's in the corresponding bits in the Interrupt Reset Register. The mask in the Interrupt Enable Register enables the interrupt if corresponding events do occur.

6.6.3 Watchdog

The PCD5041 is equipped with a watchdog timer, which generates a reset towards an external device (e.g. a microcontroller) after time-out. Two (fixed) time-out periods can be programmed; 1.25 s and 82 s.
The watchdog function can be disabled by using the EN_WATCHDOG input pin.

6.6.4 Power-down

The PCC may switch off the 6.912 MHz internal clock, to enter a power saving mode. All blocks, running on this clock are then switched off (i.e. RF-interface, cipher block, speech interface, PCC). This is called the power-down state, and is only used in the handset mode.

The 13.824 MHz clock is never switched off. The Timing Control, microcontroller interface, and Bus Controller keep running, in order to remain synchronous with a base station, and to keep the wake-up circuitry active. During power-down the external microcontroller has still access to the common data area.

6.7 Survey of registers

For a survey of all addresses occupied refer to Tables 1 and 2. Some of the address locations are used differently for read and write. The addresses 000 to 7DF are occupied by RAM memory, while the upper 32 bytes are assigned to the hardware registers. A part of the RAM memory is allocated for use by the RF block, cipher block, and the speech interface.

Table 1 Hardware register addresses

ADDRESS	WRITE	READ
7E0	–	–
7E1	S-DATA1	–
7E2	S-DATA2	–
7E3	S-DATA3	RMT-STAT
7E4	–	RF-STATUS
7E5	B-field-shift	–
7E6	B-field-loc.	–
7E7	A-field-loc.	–
7E8	window-wide-off	–
7E9	window-wide-on	–
7EA	window-narrow-off	–
7EB	window-narrow-on	–
7EC	T-power-rmp-on	–
7ED	synth-off	–
7EE	RF-control-port	sync-status
7EF	slot-cnt-off	slot-counter-copy
7F0	frame-cnt-ref	RSSI
7F1	sync-ref-preset	bit-counter-copy 1
7F2	bit-counter-preset	bit-counter-copy 2
7F3	frame-counter	frame-counter
7F4	slot-counter	slot-counter
7F5	sync-control	sync-control
7F6	BMC-mode	BMC-mode
7F7	correlator-threshold	measure
7F8	watchdog-1	–
7F9	watchdog-2	–
7FA	–	–
7FB	–	–
7FC	interrupt-event	interrupt-event
7FD	interrupt-enable	interrupt-enable
7FE	interrupt-reset	–
7FF	controller mode	controller mode

Table 2 Fixed RAM locations

ADDRESS	ENTRY
740 to 747	cipher key vector #0
748 to 74F	cipher key vector #1
750 to 757	cipher key vector #2
758 to 75F	cipher key vector #3
760 to 767	cipher key vector #4
768 to 76F	cipher key vector #5
770 to 777	cipher key vector #6
778 to 77F	cipher key vector #7
780 to 787	cipher key vector #8
788 to 78F	cipher key vector #9
790 to 797	cipher key vector #10
798 to 79F	cipher key vector #11
7A0 to 7A7	cipher init vector
7A8 to 7AA	not used
7AB	XZ field buffer
7AC to 7AF	S-field buffer
7B0 to 7BB	cipher-slot-control-table
7BC to 7BF	not used
7C0 to 7DF	speech-slot-control-table

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	+500	mW
P_O	power dissipation per output	−	30	mW
I_{DD}	supply current	−100	+130	mA
I_{SS}	ground current	−100	+130	mA
T_{stg}	storage temperature range	−55	+100	°C
T_j	operating junction temperature	−	90	°C

8 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
T_{amb}	operating ambient temperature		−25	−	+70	°C
V_{DD}	supply voltage		2.7	−	5.5	V
$V_{DD(ret)}$	RAM retention voltage		1.0	−	V_{DD}	V
I_{DD}	operating supply current	note 1	−	6	12	mA
$I_{DD(stb)}$	standby supply current	note 2	−	1	3	mA
	clock input duty cycle	All inputs LOW except WRN; XTAL1 running at 14 MHz	45	−	55	%
Digital I/O						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
V_{OL}	LOW level output voltage		0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
V_{OH}	HIGH level output voltage		$0.7V_{DD}$	−	V_{DD}	V
I_{LI}	input leakage current				1.0	µA
$I_{O(source)}$	output source current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{O(sink)}$	output sink current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{RDYN(sink)}$	RDYN output sink current	V_{DD} = 3.6 V; V_O = 0.4 V	2.0	5.0	−	mA
		V_{DD} = 5.0 V; V_O = 0.4 V	−	6.0	−	mA
f_{DCK}	DCK input frequency	n = 1 to 32	−	n × 64	−	kHz
f_{FS1}	FS1 input frequency		−	8	−	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator (inputs XTAL1 and XTAL2)						
g_m	transconductance	V_{DD} = 2.7 V	0.6	–	–	mS
		V_{DD} = 3.6 V	–	1.6	–	mS
R_F	feedback resistance		200	500	–	kΩ
RSSI Peak detector (6-bit linear A-D converter, for RSSI measurement on input RSSI_AN)						
$V_{i(RSSI\_AN)}$	input level		0	–	V_{DD}	V
$V_{conv(RSSI\_AN)}$	voltage conversion range		0	–	V_{REF}	V
$V_{i(VREF)}$	V_{REF} input voltage		1.0	3.0	V_{DD}	V
$Z_{i(VREF)}$	V_{REF} input impedance	during power-down high impedance	–	50	–	kΩ
t_{conv}	conversion time		18.4	–	–	µs
	integral non-linearity		–	–	4	LSB
	differential non-linearity	note 3	–	0.2	1.5	LSB
$Z_{i(RSSI\_AN)}$	input impedance RSSI_AN		–	1	–	MΩ
PCD5041HZ comparator characteristics						
$I_{DD(stb)(comp)}$	supply current (standby)	note 4	–	10	–	µA
$I_{DD(idle)(comp)}$	supply current (idle)	V_{DD} = 3.0 V; note 4	–	135	–	µA
$I_{DD(1MHz)}$	supply current (1 MHz)	V_{DD} = 3.0 V; note 4	–	350	–	µA
$I_{LI(comp)}$	input leakage current	note 5	–	–	1	µA
C_i	input capacitance	note 5	–	10	–	pF
R_{pu}	pullup resistance	note 6	–	200	–	kΩ
V_{cm}	input common mode range	note 7	1.0	–	V_{DD} – 0.5	V
V_{os}	max. input offset voltage	note 8	–	5	–	mV
t_{pd}	propagation delay	note 9	–	100	200	ns
Δt_{pd}	delay difference	note 8 and 9	–	10	–	ns
$V_{OL(comp)}$	output level LOW	I_O = 2 mA	–	–	0.4	V
$V_{OH(comp)}$	output level HIGH	I_O = 2 mA	V_{DD} – 0.4	–	–	V
t_r	output rise time	C_L = 50 pF	–	15	–	ns
t_f	output fall time	C_L = 50 pF	–	15	–	ns
t_{en}	enable time		–	–	8	µs

Notes to the characteristics

1. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; one speech link active (under typical conditions).
2. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; after reset.
3. Maximum differential non-linearity at supply voltage 5.5 V and V_{REF} = 1 V.
4. Supply current $I_{DD(stb)(comp)}$ flows when $\overline{COMP\_NE}$ is HIGH.
   Supply current $I_{DD(idle)(comp)}$ flows when the comparator is in active mode ($\overline{COMP\_NE}$ is LOW). It is the DC current of the comparator when it is not switching, and V(COMP_INP) < V(COMP_INM).
   The active mode supply current $I_{DD(1MHz)}$ includes the output pulse rate of 1 MHz.
5. For input pins COMP_INP, COMP_INM, $\overline{COMP\_NE}$.
6. For input pin $\overline{COMP\_NE}$.
7. The minimum input common mode voltage will be measured at DC levels with, COMP_INM at 1 V DC ±30 mV. The same goes for the maximum input common mode voltage at (V_{DD} – 0.5V).
8. These values are not tested in production, and are based upon theoretical estimates and laboratory tests.
9. The propagation delay t_{pd} is measured from the time the differential input voltage equals the offset voltage, to the 50% point of the output transition. The initial differential input voltage is 100 mV and the propagation delay is specified for an input overdrive of 30 mV, and a load capacitance of 50 pF. t_{pd} is valid for both the positive and negative going output transition. The maximum value is valid for the total ranges of temperature, supply voltage and common mode input voltage. The worst case operation conditions are at the minimum supply voltage, the lowest operating temperature and the minimum input common mode voltage. The delay difference Δt_{pd} gives the difference between t_{pd} for the rising output transition and t_{pd} for the falling output transition and is valid for all operating conditions. The test method to check the maximum delay difference is by measuring the RMS voltage of the output signal.

DECT burst mode controller PCD5042

1 FEATURES

- On-chip pre-programmed Communication Controller with embedded firmware for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning, and control of the device's other functional units.
- Fixed Part (FP) modes
- TDMA frame (de)multiplexing
- Encryption
- Scrambling
- CRC generation and checking
- Beacon transmission control (by P00 packets)
- On-chip comparator for receive data slicer function (only available in the LQFP80 package)
- Switches up to12 active speech channels from speech interface to 1152 kbits/s. radio interface, and vice versa
- Dual channel speech/data capability
- RSSI measurement, with on-chip 6-bits peak/hold detector
- Local call switching for up to 6 internal calls on RF side/local call switching on speech side.
- Quality control report
- Digital Phase Locked Loop (DPLL)
- Synchronization (handset to active bearer, base station to cluster of RFPs)
- Seamless handover procedure
- Fast (hardware) and slow (software) mute function
- 1 kbyte extended RAM memory
- On-chip crystal oscillator (13.824 MHz)
- Programmable microcontroller clock frequency
- Programmable interrupts
- Watchdog with two programmable time-outs
- Low power consumption in standby mode
- Low supply voltage (2.7 to 5.5 V)
- SACMOS technology.

2 GENERAL DESCRIPTION

The PCD5042 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT Physical Layer and MAC Layer time-critical functions, for use in DECT base station products which comply with the following standards:

- DECT CI part 2: Physical layer (DE/RES 3001-2)
- DECT CI part 3 : Medium Access Control layer (DE/RES 3001-3)
- DECT CI part 7: Security features for DECT (DE/RES 3001-7)
- DECT CI part 9: Public Access Profile (DE/RES 3001-9).

The PCD5042 has interfaces to:

- Up to 4 ADPCM CODECs in a simple base station (with up to 4 analogue lines) without glue logic
- n x 64 kbits/s highway, where n = 1 to 32, for systems requiring more than 4 connections to the network
- A radio transceiver; the interface is fully decoded, and includes power-down signals
- An external microcontroller.

The PCD5042 is designed to be connected to an ADPCM CODEC (Philips' PCD5032, for example) and an 80C51-type microcontroller. Other microcontrollers (e.g. 68000) and CODECs can also be supported.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5042H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2
PCD5042HZ	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4 BLOCK DIAGRAM

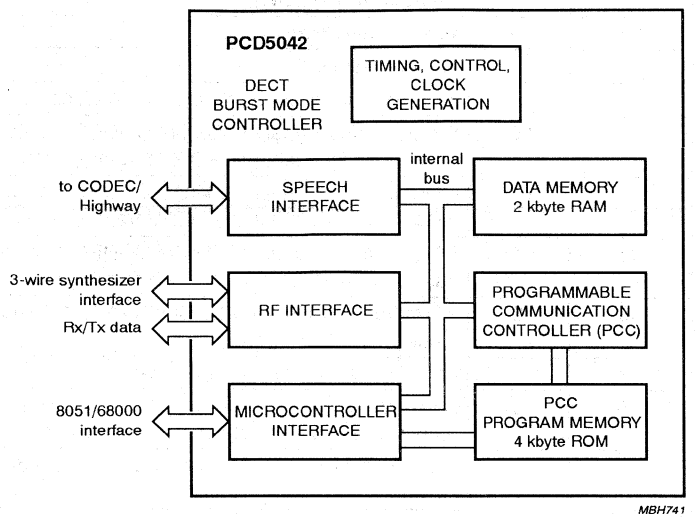


Fig.1 Block diagram.

5 PINNING (see Figs 2 and 3)

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
AD0 to AD7	1 to 8	80, 1, and 3 to 7	I/O	address/Data bus
ALE	9	9	I	address latch enable
$\overline{CS}$	10	11	I	chip select (active LOW)
A8 to A10	13 to 11	14 to 12	I	address bus
V_{DD1}	14	15	P	positive supply 1
PROC_CLK	15	16	O	microcontroller clock; programmable from $f_{CLK}/64$ to f_{CLK}, where f_{CLK} is the crystal oscillator frequency
V_{SS1}	16	17	P	negative supply 1
XTAL1	17	20	I	crystal oscillator input
XTAL2	18	21	O	crystal oscillator output
V_{SS2}	19	22	P	negative supply
RESET_OUT	20	23	O	watchdog timer output; intended to reset the external microcontroller when expired
$\overline{RD}$	21	24	I	read (active LOW)
$\overline{WR}$	22	25	I	write (active LOW)
$\overline{RDY}$	23	26	O	ready signal (active LOW), to initiate wait states in the microcontroller (open drain)

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
$\overline{INT}$	24	27	O	interrupt (active LOW)
CLK100	25	29	O	100 Hz frame timer
V_{SS3}	26	31	P	negative supply 3
DO	27	32	O	3-state data output on the speech interface
FS3	–	33	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS1	28	34	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS4	–	35	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS2	29	36	O	8 kHz framing signal to ADPCM CODEC 2 in the base station mode
DI	30	37	I	data input on the speech interface
DCK	31	38	O	simple base + handset; 1152 kHz data clock (output), otherwise 2048 kHz data clock (input) signal
CLK3	32	39	O	3.456 MHz clock (nominal value, used to adjust system timing)
ANT_SW	33	40	O	selects one of two antennas
$\overline{T\_ENABLE}$	34	41	O	Transmitter Enable (active LOW)
T_POWER_RMP	35	43	O	Transmitter Power Ramp control
RMT_STAT	36	44	I	serial 8-bit data can be read in for each slot; REMote radio
SYNTH_LOCK	37	45	I	lock indication from synthesizer
V_{SS4}	38	46	P	negative supply 4
REF_CLK	39	47	O	reference frequency for the synthesizer, i.e. the crystal oscillator clock f_{CLK}
V_{DD2}	40	48	P	positive supply 2
S_ENABLE	41	49	O	synthesizer enable
S_CLK	42	51	O	clock signal, to be used with S_DATA
S_DATA	43	52	O	serial data to the synthesizer
S_POWER_DWN	44	53	O	synthesizer power-down control
VCO_BND_SW	45	54	O	VCO bandswitch control signal
1200 HZ	46	55	O	control signal for dual synthesizer schemes
T_DATA	47	56	O	serial output data to transmitter
SET_OFF_IN	48	57	I	switches off the crystal oscillator, and prevents all RF signals from becoming active
TEST1	49	58	I	selects various test modes.; normal operation set to 0
RSSI_AN	50	60	I	analog signal (for basic DECT systems), peak signal strength measured after a lowpass filter
TEST2	51	–	I	selects various test modes; normal operation set to 0
TEST3	52	61	I	selects various test modes; normal operation set to 0
R_DATA	53	63	I	receive data

SYMBOL	PIN		TYPE[2]	DESCRIPTION
	QFP64	LQFP80[1]		
$\overline{R\_ENABLE}$	54	64	O	receiver enable (active LOW)
R_POWER_DWN	55	65	O	receiver power-down
$\overline{COMP\_NE}$	–	66	I	digital input comparator not_enable (active LOW)
SLICE_CTR	56	67	O	slice time constant control
COMP_OUT	–	68	O	digital comparator output
V_{DD3}	57	69	P	positive supply 3
V_{SS5}	58	70	P	negative supply 5
COMP_INM	–	71	I	analog comparator input negative
V_{REF}	59	72	I	reference input for the A/D converter
COMP_INP	–	73	I	analog input positive
$V_{DD(RAM)}$	60	74	P	power supply for data RAM
SYNCPORT	61	76	I/O	in the base station the signal is the SYNCPORT
RESET	62	77	I	BMC master reset signal
MEM_SEL	63	78	I	selects PCC program memory at microcontroller interface
EN_WATCHDOG	64	79	I	enable watchdog input; when HIGH, the watchdog timer of the BMC is enabled

Notes

1. Un-referenced pins for the LQFP80 package are not connected. FS3, FS4 and the comparator signals are only available in the LQFP80 package.
2. **All** signals which are input or I/O, and which can be floating, need to be pulled up to V_{DD} or down to V_{SS} in order to protect the device against cross-currents. Exceptions are VREF and RSSI_AN, which do not have to be protected.

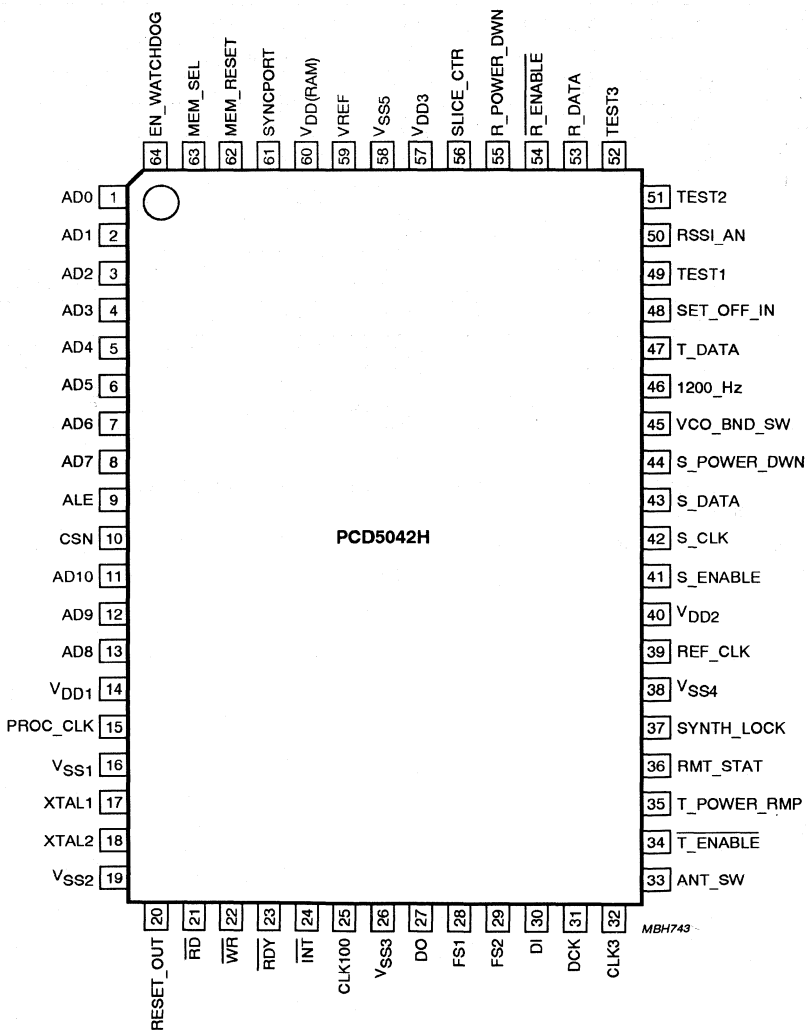


Fig.2 Pin configuration, PCD5042H (QFP64 package).

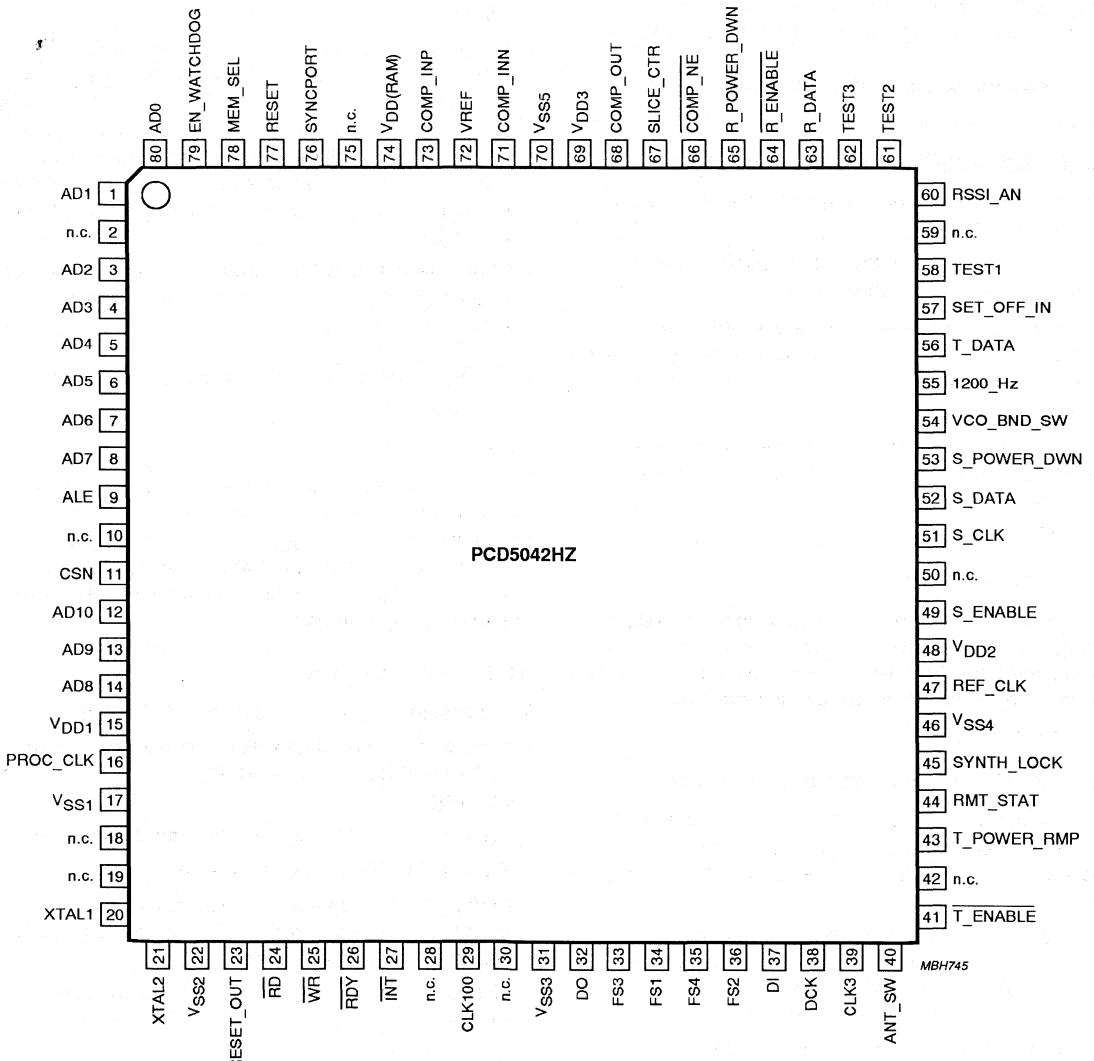


Fig.3 Pin configuration, PCD5042HZ (LQFP80 package).

6 FUNCTIONAL DESCRIPTION (see Fig.1)

The PCD5042 has dedicated hardware blocks containing logic for time-critical functions requiring bit or byte-time accuracy. Other functions requiring only slot-time accuracy are performed by software in the Preprogrammed Communication Controller (PCC). This approach offers maximum flexibility during prototyping.

6.1 Internal bus and data memory

6.1.1 INTERNAL BUS

The function of the internal bus is:

- To provide access for all functional blocks to the common data memory
- To provide access for the microcontroller-interface and the PCC to all other functional blocks.

All functional blocks (speech-interface, RF-interface, microcontroller-interface and PCC) can autonomously use the internal bus to communicate with the common data memory.

A bus controller is used to handle the bus priority mechanism. When several blocks request access simultaneously, the request with the highest priority is handled first.

6.1.2 DATA MEMORY

A large part of the data memory is used for the bit rate adaptation between the DECT radio interface and the speech interface. The data memory also acts as the main communication interface between the external microprocessor and the PCC.

6.2 Clock generation and correction (see Fig.4)

The device has an on-chip 13.824 MHz crystal oscillator. From this source, a few frequencies are derived for internal and external use. Frequencies generated for external use are:

- 13.824 MHz for the synthesizer reference (pin REF_CLK). This output is only provided if the synthesizer power-down control (output on pin S_POWER_DWN) is not selected.
- 0.144 to 13.824 MHz for the microcontroller clock (pin PROC_CLK)
- 3.456 MHz for the ADPCM CODEC (pin CLK3)
- 1200 Hz (pin 1200_HZ) for dual synthesizer switching
- 100 Hz (pin CLK100) indicates start of frame.

Nominally, the frequency on pin CLK3 is 3.456 MHz. This frequency is obtained by dividing the crystal frequency by 4. Sometimes, the crystal frequency will be divided by 3 or by 5, to synchronize the combination of the ADPCM CODEC and the device to an external source. External synchronization for base station applications is achieved as follows:

- **Master base station**. The master base station provides a 100 Hz signal to slave base stations on pin SYNCPORT. If the PCD5042 is connected to a digital interface (32-slot mode speech interface), the external synchronization will be done on the incoming 8 kHz signal. If it is connected to an analog line (12-slot mode speech interface), it will use its own crystal oscillator as reference.
- **Slave base station**. The slave base station will use the incoming SYNCPORT signal as synchronization reference.

6.3 Programmable communication controller and program memory

6.3.1 PCC

The PCC is a RISC-type controller and is used to control functions which are slot-time accurate. It is well suited for bit manipulation, and runs at a clock frequency of 6.912 MHz (equivalent to 3.4 Mips). After finishing a task, it switches to a power saving state, from which it returns after a pre-programmed time.

6.3.2 PCC FUNCTIONS

The most important functions of the PCC are to:

- Perform the appropriate actions on received messages: PMID and FMID checking, RFPI checking, TBC handling
- Prepare A-field messages for transmission
- Prepare the RF-interface for the coming slot
- Perform the procedures for RSSI and set-up scan, maintain scan counters and timers, assemble the RSSI field in the common data memory
- Filter events and indicate them to the microcontroller by interrupt.

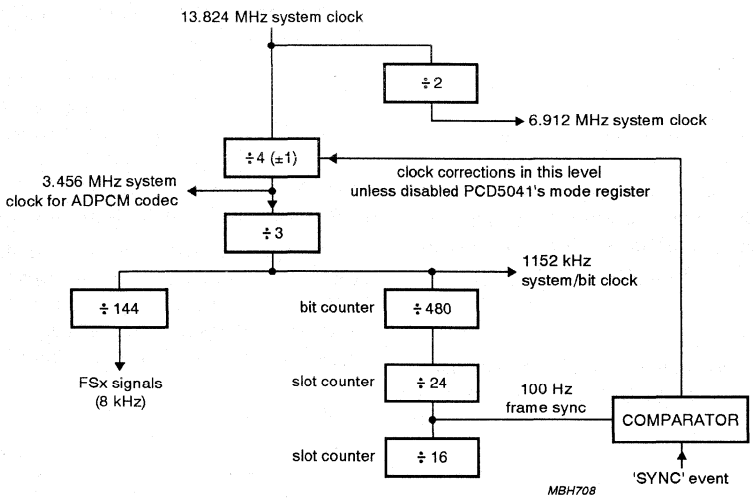


Fig.4 Internal clocking scheme of the PCD5042.

6.4 Speech interface

The speech interface block performs the following functions:

- Connection to a 1152 kbits/s interface in a handset and a simple base station in the so called '12 slot mode'
- Connection to a n x 64 kbits/s interface in base stations in the so called '32 slot mode'
- Autonomous storing/fetching of ADPCM speech data in/from the PCD5042's common data memory, using internal addressing logic
- Muting of speech data
- Local call.

6.4.1 12-SLOT MODE

The 12-slot mode is selected if up to 4 ADPCM CODECs are connected to the PCD5042, where the PCD5042 is the master of these CODECs. In a handset, or in a simple base stations which is connected with up to 4 analog lines to the public network, the PCD5042 is master of the CODECs. Each CODEC is connected with a separate framing reference signal (FS1 to FS4) to the PCD5042. In the QFP64 package, 2 framing signals FS1 and FS2 are available, whereas in the LQFP80 package 4 framing signals can be used (FS1 to FS4). When more CODECs are to be connected, the FS5 to FS12 signals have to be generated externally. When using the framing signals FS1 to FS4, no interface logic is required when using the PCD5032 ADPCM CODEC.

A speech-slot control table is used to determine where to store/fetch speech data for transmission and reception. The hardware speech-interface is capable of addressing the right speech buffer for the relevant speech slot, and will maintain a counter carrying the offset to the correct stored/fetched address.

6.4.2 32-SLOT MODE

The 32-slot mode is used to connect the PCD5042 to a digital interface with a data rate of n x 64 kbits/s; where n = 1 to 32 is the number of speech slots. This equates to data rates from 64 kbits/s to 2048 kbits/s.
Up to 12 of the 32 speech slots can be used simultaneously. The same kind of speech-slot control table used in the 12-slot mode is used for the 32-slot mode.

6.4.3 MUTING

Due to various reasons the quality of the incoming speech data may be degraded significantly. By muting the speech

data, these disturbances are not audible (or are less audible) to the user. The PCD5042 performs two types of muting:

- Fast muting
- Slow muting.

Fast muting, which is performed by the PCD5042 automatically, is nothing more than a repetition of the previously received frame (80 speech samples) to the ADPCM CODEC. It is issued if no Sync word was detected. Slow muting is issued by the microcontroller, after having detected a degradation of quality. A slow mute is implemented as a continuous '0000' nibble transmission to the ADPCM CODEC, until slow mute is released.

6.4.4 LOCAL CALL

A local call option is implemented, in order to loopback data from one CODEC to another CODEC, and vice versa, see Fig.5.

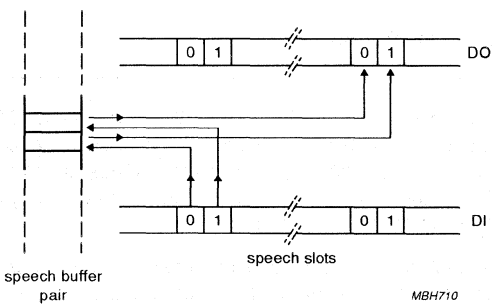


Fig.5 Local call switching on speech interface.

6.5 RF interface

Most of the functions performed by the RF interface are under control of the PCC. Specifically, the processing of non-speech data and the programming of functions and registers is done via the PCC.

6.5.1 SERIAL RECEIVER

The serial receiver processes the data, which comes from the RF section, and which is already filtered by the synchronization part. The data is latched, using the recovered data clock.

The serial receiver will collect the complete A-field and B-field and store it in the common data memory. Before the A-field is received, the A-field start address is programmed by the PCC. Upon reception of A-field nibbles, the address is updated by the serial receiver. Meanwhile, the PCC will program the B-field start address.

In Fig.6 the data flow in the serial receiver is shown. Note that almost no decoding of messages is required. Only the header of the A-field needs to be decoded to check if a ciphered message is being received or transmitted, which requires the ciphering to be switched on in the A-field also.

6.5.2 SERIAL TRANSMITTER

The serial transmitter performs the reverse of the receiver functions. Several blocks used in the receiver are also used in the transmitter. Amongst these are the CRC-generators, the scrambler, and the address registers. Figure 7 shows the serial transmitter structure.

By transmitting the X-CRC twice, the Z-field is transmitted. The handling of the address registers is the same for the transmitter. Transmission of the synchronization sequence (S-field) is done using the same method as the A-field and B-field. The S-field is stored in the common data memory and will be fetched by the transmitter, just before transmission.

Two additional functions are not shown in Fig.7:

- In the handset the data in the serial transmitter may be advanced by a programmable number of bit periods. This is done to compensate for the delay in the RF section
- The transmitted data can be inverted (using a switch in the PCD5042 mode register), in order to connect the PCD5042 to VCOs requiring negative modulation.

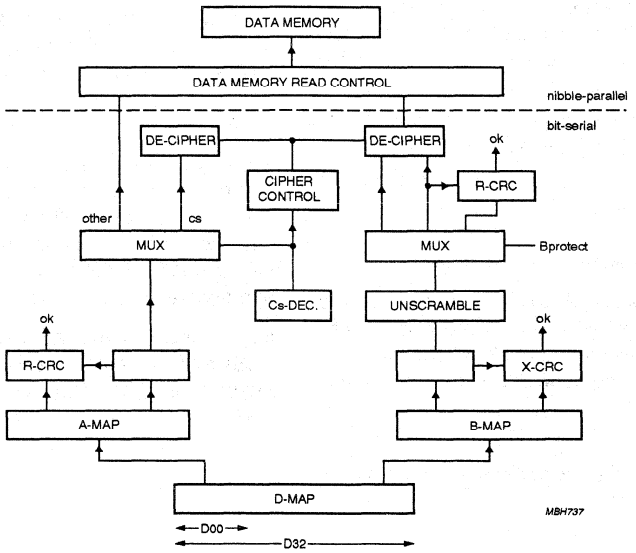


Fig.6 Serial receiver structure.

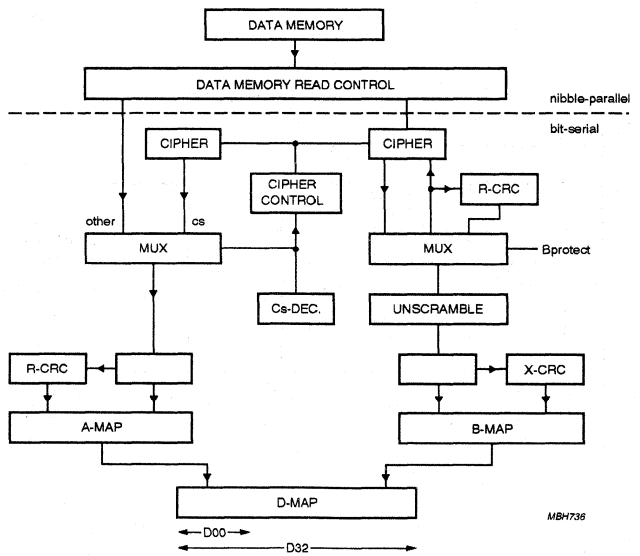


Fig.7 Serial transmitter structure.

6.5.3 SEAMLESS HANDOVER

Seamless handover guarantees that when speech information is switched from one slot to another, no speech samples are lost, added or displaced. Seamless handover is achieved in the RF interface by:

- Using a look-up table containing the correct start addresses of the B-fields in the data memory
- The RF receive and transmit blocks move data to/from the data memory block in 4-bit nibbles.

6.5.4 RF CONTROL SIGNALS

The timing of the control signals to the RF section is fixed, but such that an RF delay between 1.5 and 7 μs can be tolerated. Only the transmitter ramp signal and the synthesizer enable are programmable within certain limits.

6.5.5 SYNTHESIZER PROGRAMMING

To program a synthesizer, a 3-wire serial interface is used. The signals on this interface are:

- S_ENABLE (enable)
- S_CLK (clock)
- S_DATA (data).

To program various types of synthesizers, a 3-byte shift register is present. Three data formats are supported: 8, 16 or 24 bit words can be selected. The transfer of data from a frequency table in the common data memory to the shift register is under control of the PCC.

6.5.6 RSSI MEASUREMENT (see Fig.8)

The RSSI measurement in the PCD5042 RF-interface block is done in 3 parts: a peak/hold detector, a 6-bit A/D converter, and an RSSI control unit, which controls the peak/hold detector and the A/D converter. Once per slot time, a sample is fetched by the PCC and saved in the appropriate area of the common data memory.

If the radio receiver is active in a particular time slot, the RSSI value will automatically be measured in that slot. Adjustment to the RSSI_AN input level can be made with VREF.

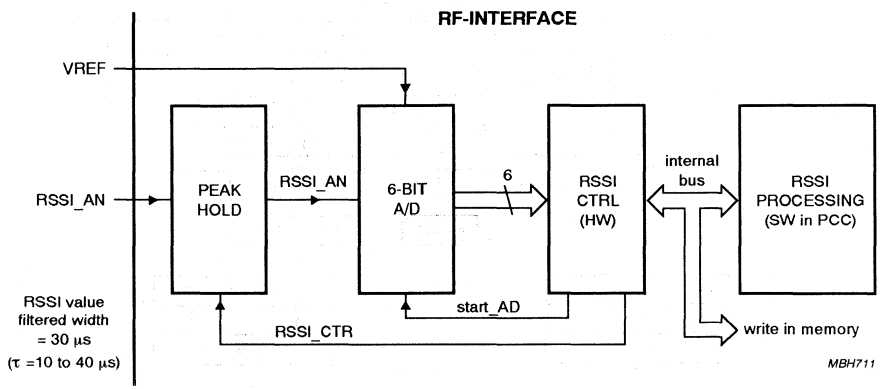


Fig.8 RSSI measurement path.

6.5.7 LOCAL CALL SWITCHING (see Fig.9)

The PCD5042 provides a local call switching function in the base station. It will store incoming speech nibbles in the common data memory, in the area reserved for that particular receive slot. Then, during the transmit phase, it passes the start pointer of the same data memory area to the transmit block. Thus, the speech data is echoed to the other user. To handle quality degradation for local calls, a mute can be performed at the RF side of the speech buffer.

6.5.8 DATA SYNCHRONIZATION (see Fig.10)

The data synchronization is done in 2 phases:

- Bit synchronization
- Sync word detection.

Bit synchronization is done using a Digital PLL (DPLL), with an oversampling factor of 12, i.e. the DPLL is running at 12 times the data rate. The output from the DPLL is a receive clock signal (RxC), which acts as the enable for a 20-bit shift register.

Sync word detection is achieved by checking the incoming data pattern with the expected synchronization field pattern, using a correlator.
The correlator has a programmable threshold, so it can accept bit errors in the sync field pattern up to the threshold level. Furthermore, the correlator window is programmable. This means that 'SlotSync', which indicates the slot synchronization event, can be detected only during a certain period (the time window).

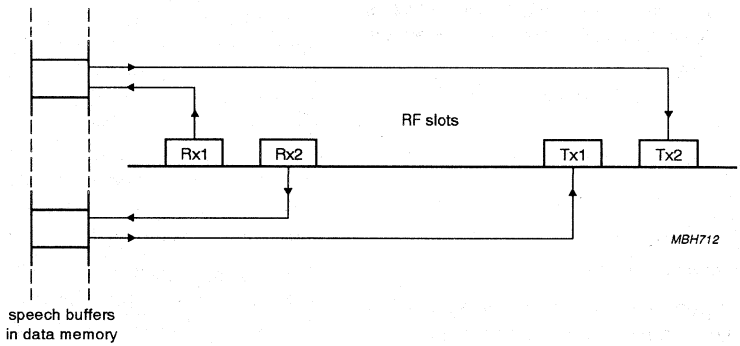


Fig.9 Local call switching on the RF-side.

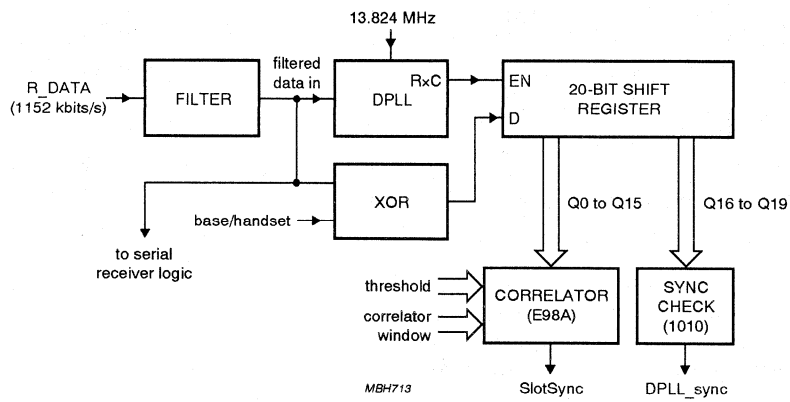


Fig.10 Schematic of the receiver synchronization part.

The 'DPLL_sync' indication should only be used, when 'SlotSync' is active. It indicates that the last 4 bits of the pre-amble field (the training sequence) are received correctly, and thus indicates that the DPLL was in lock (synchronized) in time. If the 'SlotSync' is active, and the 'DPLL_sync' is not, then a sliding interferer might have been detected.

If 'SlotSync' is not detected, effectively no data is received in that slot. This implies a 'fast mute' because speech data received in the previous frame is not destroyed.

6.5.9 CIPHERING MACHINE

The description of the cipher machine is subject to confidentiality. The specification of its algorithms are delivered by ETSI under the terms of a Non-Disclosure Agreement.

The cipher machine is under control of the TBC, which is implemented in the PCC. The cipher machine generates 2 fields of ciphering bits:

- A_cipher (40 bits) for A-field messages (ciphers tail only)
- B_cipher (320 bits) for speech in B-field.

The transmitted ciphered bits are then:

- A_ciphered: = A XOR A_cipher
- B_ciphered: = B XOR B_cipher.

On reception by the peer end point, deciphering consists of the same operation thanks to the synchronous generation of A_cipher and B_cipher.

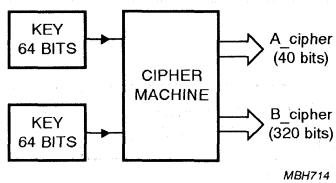


Fig.11 Cipher machine and its sources.

The cipher machine is time-multiplexed on a slot basis. Initially, the Initialisation Vector (IV) and the key must be loaded into the cipher machine. Transfer of the IV and key from the common data area to the cipher machine is done automatically by the cipher machine. The contents of the memory space where IV and key are found, are the responsibility of the PCC, and the external microprocessor.

6.5.10 COMPARATOR/DATA SLICER ON PCD5042HZ

The PCD5042HZ contains a comparator/data slicer. The comparator is a stand-alone circuit. No connections other than power supply are made internally.
The comparator can be used as a data slicer for the receiver input. The delay requirements listed in Chapter 8 were derived from this application. Another use of the comparator is in a successive approximation A/D converter to indicate battery low-voltage condition, or in a power-on-reset circuit.

When the signal $\overline{\text{COMP\_NE}}$ is LOW the comparator is enabled. When $\overline{\text{COMP\_NE}}$ is HIGH the comparator is disabled, and the circuit consumes no power. If the comparator is used as a data slicer for the receiver input, the R_DATA is connected to COMP_OUT, the $\overline{\text{COMP\_NE}}$ is connected to $\overline{\text{R\_ENABLE}}$, both connection are done externally. The pin COMP_INP is connected to the RF mixer. A proper bias voltage (from the slicer time constant control circuit) is connected to COMP_INM. Another use of the comparator is in a successive approximation A/D converter for battery voltage detection.

The pins are protected against ESD damaging, with a protection diode to the positive and negative supply rail. The input pin $\overline{\text{COMP\_NE}}$ has a pull-up resistor which keeps the comparator in power-down mode by default.

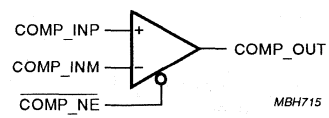


Fig.12 Circuit schematic of the comparator/data slicer.

6.6 Microcontroller Interface

6.6.1 Function of the microcontroller interface

The microcontroller Interface will provide the following services.

- Direct interface to processors which have an INTEL-8051 compatible interface
- General interface to processors that can handle 'wait states' e.g. 68000-family; in this case glue logic is required
- Processor clock signal of which the frequency is programmable in order to adjust instantaneously processor performance to processor work load
- A programmable interrupt register
- A watchdog timer with time-out periods of 1.25 or 82 seconds, depending on the programming.

The microcontroller can address the PCD5042 as any other RAM memory connected to the microcontroller bus. By writing the 'Interface-Mode Register', the microcontroller can select the interface mode and its own clock frequency.

6.6.2 Microcontroller interrupts

The function of microcontroller Interrupts is to make optimal use of the microcontroller's processing power, and to achieve optimal cooperation between time-critical tasks and less time-critical tasks both executed in software. Three registers are available to handle interrupts. These are:

- Interrupt Event Register
- Interrupt Enable Register
- Interrupt Reset Register.

These registers are to be regarded together. Corresponding bits in these registers relate to one and the same event. Bits in the Interrupt Event Register are set by the PCC and are to be reset by the external processor by writing '1's in the corresponding bits in the Interrupt Reset Register. The mask in the Interrupt Enable Register enables the interrupt if corresponding events do occur.

6.6.3 Watchdog

The PCD5042 is equipped with a watchdog timer, which generates a reset towards an external device (e.g. a μC) after time-out. Two (fixed) time-out periods can be programmed; 1.25 s and 82 s. The watchdog function can be disabled by using the EN_WATCHDOG input pin.

6.6.4 Power-down

The PCC may switch off the 6.912 MHz internal clock, to enter a power saving mode. All blocks, running on this clock are then switched off (i.e. RF-interface, cipher block, speech interface, PCC). This is called the power-down state, and is only used in the handset mode.

The 13.824 MHz clock is never switched off. The Timing Control, microcontroller interface, and Bus Controller keep running, in order to remain synchronous with a base station, and to keep the wake-up circuitry active. During power-down the external microcontroller has still access to the common data area.

6.7 Survey of registers

For a survey of all addresses occupied refer to Tables 1 and 2. Some of the address locations are used differently for read and write. The addresses 000 to 7DF are occupied by RAM memory, while the upper 32 bytes are assigned to the hardware registers. A part of the RAM memory is allocated for use by the RF block, cipher block, and the speech interface.

Table 1 Hardware register addresses

ADDRESS	WRITE	READ
7E0	–	–
7E1	S-DATA1	–
7E2	S-DATA2	–
7E3	S-DATA3	RMT-STAT
7E4	–	RF-STATUS
7E5	B-field-shift	–
7E6	B-field-loc.	–
7E7	A-field-loc.	–
7E8	window-wide-off	–
7E9	window-wide-on	–
7EA	window-narrow-off	–
7EB	window-narrow-on	–
7EC	T-power-rmp-on	–
7ED	synth-off	–
7EE	RF-control-port	sync-status
7EF	slot-cnt-off	slot-counter-copy
7F0	frame-cnt-ref	RSSI
7F1	sync-ref-preset	bit-counter-copy1
7F2	bit-counter-preset	bit-counter-copy2
7F3	frame-counter	frame-counter
7F4	slot-counter	slot-counter
7F5	sync-control	sync-control
7F6	BMC-mode	BMC-mode
7F7	correlator-threshold	measure
7F8	watchdog-1	–
7F9	watchdog-2	–
7FA	–	–
7FB	–	–
7FC	interrupt-event	interrupt-event
7FD	interrupt-enable	interrupt-enable
7FE	interrupt-reset	–
7FF	controller mode	controller mode

Table 2 Fixed RAM locations

ADDRESS	ENTRY
740 to 747	cipher key vector #0
748 to 74F	cipher key vector #1
750 to 757	cipher key vector #2
758 to 75F	cipher key vector #3
760 to 767	cipher key vector #4
768 to 76F	cipher key vector #5
770 to 777	cipher key vector #6
778 to 77F	cipher key vector #7
780 to 787	cipher key vector #8
788 to 78F	cipher key vector #9
790 to 797	cipher key vector #10
798 to 79F	cipher key vector #11
7A0 to 7A7	cipher init vector
7A8 to 7AA	not used
7AB	XZ field buffer
7AC to 7AF	S-field buffer
7B0 to 7BB	cipher-slot-control-table
7BC to 7BF	not used
7C0 to 7DF	speech-slot-control-table

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_i	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	+500	mW
P_O	power dissipation per output	−	30	mW
I_{DD}	supply current	−100	+130	mA
I_{SS}	ground current	−100	+130	mA
T_{stg}	storage temperature range	−55	+100	°C
T_j	operating junction temperature	−	90	°C

8 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
T_{amb}	operating ambient temperature		−25	−	+70	°C
V_{DD}	supply voltage		2.7	−	5.5	V
$V_{DD(ret)}$	RAM retention voltage		1.0	−	V_{DD}	V
I_{DD}	operating supply current	note 1	−	6	12	mA
$I_{DD(stb)}$	standby supply current	note 2	−	1	3	mA
	clock input duty cycle	All inputs LOW except WRN; XTAL1 running at 14 MHz	45	−	55	%
Digital I/O						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
V_{OL}	LOW level output voltage		0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
V_{OH}	HIGH level output voltage		$0.7V_{DD}$	−	V_{DD}	V
I_{LI}	input leakage current				1.0	µA
$I_{O(source)}$	output source current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{O(sink)}$	output sink current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{RDYN(sink)}$	RDYN output sink current	V_{DD} = 3.6 V; V_O = 0.4 V	2.0	5.0	−	mA
		V_{DD} = 5.0 V; V_O = 0.4 V	−	6.0	−	mA
f_{DCK}	DCK input frequency	n = 1 to 32	−	n × 64	−	kHz
f_{FS1}	FS1 input frequency		−	8	−	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator (inputs XTAL1 and XTAL2)						
g_m	transconductance	V_{DD} = 2.7 V	0.6	–	–	mS
		V_{DD} = 3.6 V	–	1.6	–	mS
R_F	feedback resistance		200	500		kΩ
RSSI Peak detector (6-bit linear A-D converter, for RSSI measurement on input RSSI_AN)						
$V_{i(RSSI\_AN)}$	input level		0	–	V_{DD}	V
$V_{conv(RSSI\_AN)}$	voltage conversion range		0	–	V_{REF}	V
$V_{i(VREF)}$	V_{REF} input voltage		1.0	3.0	V_{DD}	V
$Z_{i(VREF)}$	V_{REF} input impedance	during power-down high impedance	–	50	–	kΩ
t_{conv}	conversion time		18.4	–	–	µs
	integral non-linearity		–	–	4	LSB
	differential non-linearity	note 3	–	0.2	1.5	LSB
$Z_{i(RSSI\_AN)}$	input impedance RSSI_AN		–	1	–	MΩ
PCD5042HZ comparator characteristics						
$I_{DD(stb)(comp)}$	supply current (standby)	note 4	–	10	–	µA
$I_{DD(idle)(comp)}$	supply current (idle)	V_{DD} = 3.0 V; note 4	–	135	–	µA
$I_{DD(1MHz)}$	supply current (1 MHz)	V_{DD} = 3.0 V; note 4	–	350	–	µA
$I_{LI(comp)}$	input leakage current	note 5	–	–	1	µA
C_i	input capacitance	note 5	–	10	–	pF
R_{pu}	pullup resistance	note 6	–	200	–	kΩ
V_{cm}	input common mode range	note 7	1.0	–	V_{DD} – 0.5	V
V_{os}	max. input offset voltage	note 8	–	5	–	mV
t_{pd}	propagation delay	note 9	–	100	200	ns
Δt_{pd}	delay difference	note 8 and 9	–	10	–	ns
$V_{OL(comp)}$	output level LOW	I_O = 2 mA	–	–	0.4	V
$V_{OH(comp)}$	output level HIGH	I_O = 2 mA	V_{DD} – 0.4	–	–	V
t_r	output rise time	C_L = 50 pF	–	15	–	ns
t_f	output fall time	C_L = 50 pF	–	15	–	ns
t_{en}	enable time		–	–	8	µs

Notes to the characteristics

1. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; one speech link active (under typical conditions).
2. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; after reset.
3. Maximum differential non-linearity at supply voltage 5.5 V and V_{REF} = 1 V.
4. Supply current $I_{DD(stb)(comp)}$ flows when $\overline{COMP\_NE}$ is HIGH.
   Supply current $I_{DD(idle)(comp)}$ flows when the comparator is in active mode ($\overline{COMP\_NE}$ is LOW). It is the DC current of the comparator when it is not switching, and V(COMP_INP) < V(COMP_INM).
   The active mode supply current $I_{DD(1MHz)}$ includes the output pulse rate of 1 MHz.
5. For input pins COMP_INP, COMP_INM, $\overline{COMP\_NE}$.
6. For input pin $\overline{COMP\_NE}$.
7. The minimum input common mode voltage will be measured at DC levels with, COMP_INM at 1 V DC ±30 mV. The same goes for the maximum input common mode voltage at (V_{DD} – 0.5V).
8. These values are not tested in production, and are based upon theoretical estimates and laboratory tests.
9. The propagation delay t_{pd} is measured from the time the differential input voltage equals the offset voltage, to the 50% point of the output transition. The initial differential input voltage is 100 mV and the propagation delay is specified for an input overdrive of 30 mV, and a load capacitance of 50 pF. t_{pd} is valid for both the positive and negative going output transition. The maximum value is valid for the total ranges of temperature, supply voltage and common mode input voltage. The worst case operation conditions are at the minimum supply voltage, the lowest operating temperature and the minimum input common mode voltage. The delay difference Δt_{pd} gives the difference between t_{pd} for the rising output transition and t_{pd} for the falling output transition and is valid for all operating conditions. The test method to check the maximum delay difference is by measuring the RMS voltage of the output signal.

DECT burst mode controller PCD5043

1 FEATURES

- On-chip pre-programmed Communication Controller with embedded firmware for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning, and control of the device's other functional units.
- Fixed Part (FP) modes
- TDMA frame (de)multiplexing
- Encryption
- Scrambling
- CRC generation and checking
- Beacon transmission control (by P00 packets)
- Switches up to12 active speech channels from speech interface to 1152 kbits/s. radio interface, and vice versa
- Dual channel speech/data capability
- RSSI measurement, with on-chip 6-bits peak/hold detector
- Local call switching for up to 6 internal calls on RF side/local call switching on speech side
- Quality control report
- Digital Phase Locked Loop (DPLL)
- Synchronization (handset to active bearer, base station to cluster of RFPs)
- Seamless handover procedure
- Fast (hardware) and slow (software) mute function
- 1 kbyte extended RAM memory
- On-chip crystal oscillator (13.824 MHz)
- Programmable microcontroller clock frequency
- Programmable interrupts
- Watchdog with two programmable time-outs
- Low power consumption in standby mode
- Low supply voltage (2.7 to 5.5 V)
- SACMOS technology.

2 GENERAL DESCRIPTION

The PCD5043 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT Physical Layer and MAC Layer time-critical functions, for use in DECT remote radio transceiver (PABX) products which comply with the following standards:

- DECT CI part 2: Physical layer (DE/RES 3001-2)
- DECT CI part 3 : Medium Access Control layer (DE/RES 3001-3)
- DECT CI part 7: Security features for DECT (DE/RES 3001-7)
- DECT CI part 9: Public Access Profile (DE/RES 3001-9).

The PCD5043 has interfaces to:

- Up to 4 ADPCM CODECs in a simple base station (with up to 4 analogue lines) without glue logic
- n x 64 kbits/s highway, where n = 1 to 32, for systems requiring more than 4 connections to the network
- A radio transceiver; the interface is fully decoded, and includes power-down signals
- An external microcontroller.

The PCD5043 is designed to be connected to an ADPCM CODEC (Philips' PCD5032, for example) and an 80C51-type microcontroller. Other microcontrollers (e.g. 68000) and CODECs can also be supported.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5043H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm	SOT319-2

4 BLOCK DIAGRAM

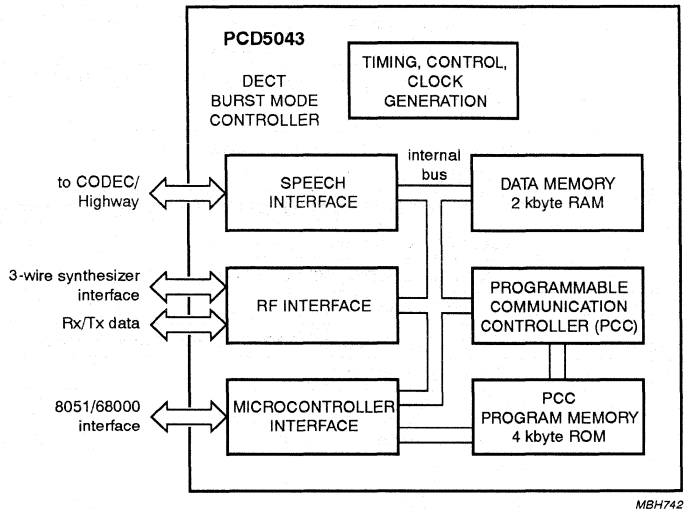


Fig.1 Block diagram.

5 PINNING (see Fig.2)

SYMBOL	PIN	TYPE[1]	DESCRIPTION
AD0 to AD7	1 to 8	I/O	address/Data bus
ALE	9	I	address latch enable
$\overline{CS}$	10	I	chip select (active LOW)
A8 to A10	13 to 11	I	address bus
V_{DD1}	14	P	positive supply 1
PROC_CLK	15	O	microcontroller clock; programmable from $f_{CLK}/64$ to f_{CLK}, where f_{CLK} is the crystal oscillator frequency
V_{SS1}	16	P	negative supply 1
XTAL1	17	I	crystal oscillator input
XTAL2	18	O	crystal oscillator output
V_{SS2}	19	P	negative supply
RESET_OUT	20	O	watchdog timer output; intended to reset the external microcontroller when expired
$\overline{RD}$	21	I	read (active LOW)
$\overline{WR}$	22	I	write (active LOW)
$\overline{RDY}$	23	O	ready signal (active LOW), to initiate wait states in the microcontroller (open drain)
$\overline{INT}$	24	O	interrupt (active LOW)
CLK100	25	O	100 Hz frame timer

SYMBOL	PIN	TYPE[1]	DESCRIPTION
V_{SS3}	26	P	negative supply 3
DO	27	O	3-state data output on the speech interface
FS1	28	I/O	8 kHz framing signal to ADPCM CODEC 1 output, for simple base + handset, otherwise 8 kHz framing input
FS2	29	O	8 kHz framing signal to ADPCM CODEC 2 in the base station mode
DI	30	I	data input on the speech interface
DCK	31	O	simple base + handset; 1152 kHz data clock (output), otherwise 2048 kHz data clock (input) signal
CLK3	32	O	3.456 MHz clock (nominal value, used to adjust system timing)
ANT_SW	33	O	selects one of two antennas
$\overline{\text{T\_ENABLE}}$	34	O	Transmitter Enable (active LOW)
T_POWER_RMP	35	O	Transmitter Power Ramp control
RMT_STAT	36	I	serial 8-bit data can be read in for each slot; REMote radio
SYNTH_LOCK	37	I	lock indication from synthesizer
V_{SS4}	38	P	negative supply 4
REF_CLK	39	O	reference frequency for the synthesizer, i.e. the crystal oscillator clock f_{CLK}
V_{DD2}	40	P	positive supply 2
S_ENABLE	41	O	synthesizer enable
S_CLK	42	O	clock signal, to be used with S_DATA
S_DATA	43	O	serial data to the synthesizer
S_POWER_DWN	44	O	synthesizer power-down control
VCO_BND_SW	45	O	VCO bandswitch control signal
1200 HZ	46	O	control signal for dual synthesizer schemes
T_DATA	47	O	serial output data to transmitter
SET_OFF_IN	48	I	switches off the crystal oscillator, and prevents all RF signals from becoming active
TEST1	49	I	selects various test modes.; normal operation set to 0
RSSI_AN	50	I	analog signal (for basic DECT systems), peak signal strength measured after a lowpass filter
TEST2	51	I	selects various test modes; normal operation set to 0
TEST3	52	I	selects various test modes; normal operation set to 0
R_DATA	53	I	receive data
$\overline{\text{R\_ENABLE}}$	54	O	receiver enable (active LOW)
R_POWER_DWN	55	O	receiver power-down
SLICE_CTR	56	O	slice time constant control
V_{DD3}	57	P	positive supply 3
V_{SS5}	58	P	negative supply 5
V_{REF}	59	I	reference input for the A/D converter
$V_{DD(RAM)}$	60	P	power supply for data RAM
SYNCPORT	61	I/O	in the base station the signal is the SYNCPORT

SYMBOL	PIN	TYPE[1]	DESCRIPTION
RESET	62	I	BMC master reset signal
MEM_SEL	63	I	selects PCC program memory at microcontroller interface
EN_WATCHDOG	64	I	enable watchdog input; when HIGH, the watchdog timer of the BMC is enabled

Note

1. **All** signals which are input or I/O, and which can be floating, need to be pulled up to V_{DD} or down to V_{SS} in order to protect the device against cross-currents. Exceptions are VREF and RSSI_AN, which do not have to be protected.

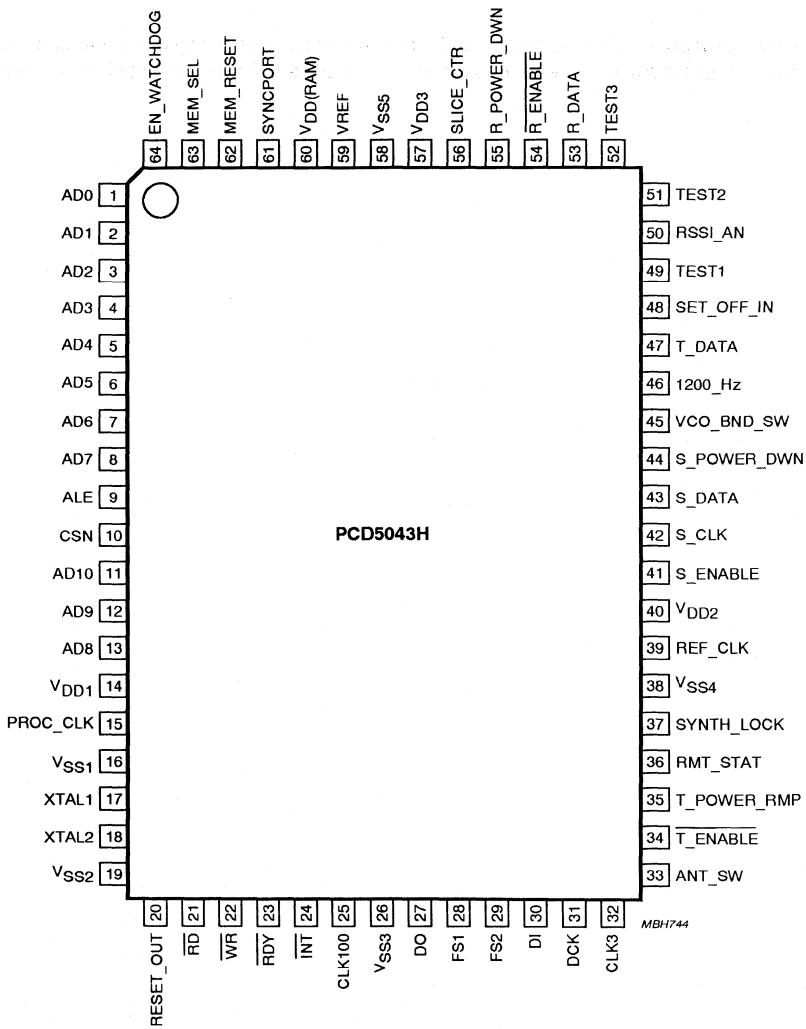


Fig.2 Pin configuration, PCD5043H.

6 FUNCTIONAL DESCRIPTION (see Fig.1)

The PCD5043 has dedicated hardware blocks containing logic for time-critical functions requiring bit or byte-time accuracy. Other functions requiring only slot-time accuracy are performed by software in the Preprogrammed Communication Controller (PCC). This approach offers maximum flexibility during prototyping.

6.1 Internal bus and data memory

6.1.1 INTERNAL BUS

The function of the internal bus is:

- To provide access for all functional blocks to the common data memory
- To provide access for the microcontroller-interface and the PCC to all other functional blocks.

All functional blocks (speech-interface, RF-interface, microcontroller-interface and PCC) can autonomously use the internal bus to communicate with the common data memory.

A bus controller is used to handle the bus priority mechanism. When several blocks request access simultaneously, the request with the highest priority is handled first.

6.1.2 DATA MEMORY

A large part of the data memory is used for the bit rate adaptation between the DECT radio interface and the speech interface. The data memory also acts as the main communication interface between the external microprocessor and the PCC.

6.2 Clock generation and correction (see Fig.3)

The device has an on-chip 13.824 MHz crystal oscillator. From this source, a few frequencies are derived for internal and external use. Frequencies generated for external use are:

- 13.824 MHz for the synthesizer reference (pin REF_CLK). This output is only provided if the synthesizer power-down control (output on pin S_POWER_DWN) is not selected.
- 0.144 to 13.824 MHz for the microcontroller clock (pin PROC_CLK)
- 3.456 MHz for the ADPCM codec (pin CLK3)
- 1200 Hz (pin 1200_HZ) for dual synthesizer switching
- 100 Hz (pin CLK100) indicates start of frame.

Nominally, the frequency on pin CLK3 is 3.456 MHz. This frequency is obtained by dividing the crystal frequency by 4. Sometimes, the crystal frequency will be divided by 3 or by 5, to synchronize the combination of the ADPCM codec and the device to an external source. External synchronization for base station applications is achieved as follows:

- **Master base station**. The master base station provides a 100 Hz signal to slave base stations on pin SYNCPORT. If the PCD5043 is connected to a digital interface (32-slot mode speech interface), the external synchronization will be done on the incoming 8 kHz signal. If it is connected to an analog line (12-slot mode speech interface), it will use its own crystal oscillator as reference.
- **Slave base station**. The slave base station will use the incoming SYNCPORT signal as synchronization reference.

6.3 Programmable communication controller and program memory

6.3.1 PCC

The PCC is a RISC-type controller and is used to control functions which are slot-time accurate. It is well suited for bit manipulation, and runs at a clock frequency of 6.912 MHz (equivalent to 3.4 Mips). After finishing a task, it switches to a power saving state, from which it returns after a pre-programmed time.

6.3.2 PCC FUNCTIONS

The most important functions of the PCC are to:

- Perform the appropriate actions on received messages: PMID and FMID checking, RFPI checking, TBC handling
- Prepare A-field messages for transmission
- Prepare the RF-interface for the coming slot
- Perform the procedures for RSSI and set-up scan, maintain scan counters and timers, assemble the RSSI field in the common data memory
- Filter events and indicate them to the microcontroller by interrupt.

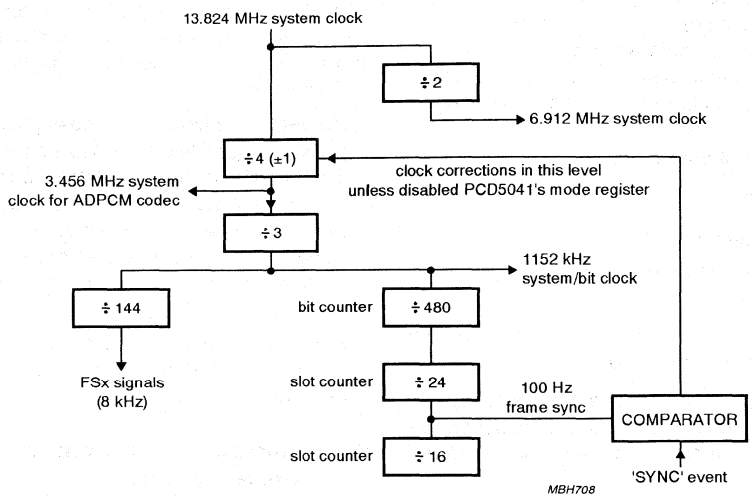


Fig.3 Internal clocking scheme of the PCD5043.

6.4 Speech interface

The speech interface block performs the following functions:

- Connection to a 1152 kbits/s interface in a handset and a simple base station in the so called '12 slot mode'
- Connection to a n x 64 kbits/s interface in base stations in the so called '32 slot mode'
- Autonomous storing/fetching of ADPCM speech data in/from the PCD5043's common data memory, using internal addressing logic
- Muting of speech data
- Local call.

6.4.1 12-SLOT MODE

The 12-slot mode is selected if up to 4 ADPCM codecs are connected to the PCD5043, where the PCD5043 is the master of these codecs. In a handset, or in a simple base stations which is connected with up to 4 analog lines to the public network, the PCD5043 is master of the codecs. Each codec is connected with a separate framing reference signal (FS1 to FS4) to the PCD5043. In the QFP64 package, 2 framing signals FS1 and FS2 are available, whereas in the LQFP80 package 4 framing signals can be used (FS1 to FS4). When more codecs are to be connected, the FS5 to FS12 signals have to be generated externally. When using the framing signals FS1 to FS4, no interface logic is required when using the PCD5032 ADPCM codec.

A speech-slot control table is used to determine where to store/fetch speech data for transmission and reception. The hardware speech-interface is capable of addressing the right speech buffer for the relevant speech slot, and will maintain a counter carrying the offset to the correct stored/fetched address.

6.4.2 32-SLOT MODE

The 32-slot mode is used to connect the PCD5043 to a digital interface with a data rate of n x 64 kbits/s; where n = 1 to 32 is the number of speech slots. This equates to data rates from 64 kbits/s to 2048 kbits/s.
Up to 12 of the 32 speech slots can be used simultaneously. The same kind of speech-slot control table used in the 12-slot mode is used for the 32-slot mode.

6.4.3 MUTING

Due to various reasons the quality of the incoming speech data may be degraded significantly. By muting the speech

data, these disturbances are not audible (or are less audible) to the user. The PCD5043 performs two types of muting:

- Fast muting
- Slow muting.

Fast muting, which is performed by the PCD5043 automatically, is nothing more than a repetition of the previously received frame (80 speech samples) to the ADPCM codec. It is issued if no Sync word was detected. Slow muting is issued by the microcontroller, after having detected a degradation of quality. A slow mute is implemented as a continuous '0000' nibble transmission to the ADPCM codec, until slow mute is released.

6.4.4 LOCAL CALL

A local call option is implemented, in order to loopback data from one codec to another codec, and vice versa, see Fig.4.

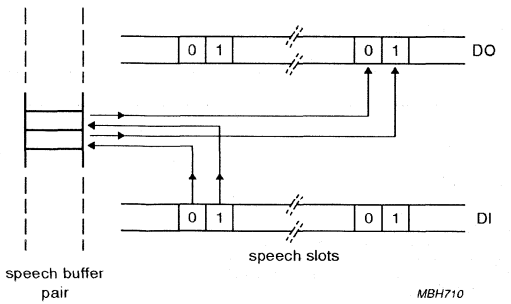


Fig.4 Local call switching on speech interface.

6.5 RF interface

Most of the functions performed by the RF interface are under control of the PCC. Specifically, the processing of non-speech data and the programming of functions and registers is done via the PCC.

6.5.1 SERIAL RECEIVER

The serial receiver processes the data, which comes from the RF section, and which is already filtered by the synchronization part. The data is latched, using the recovered data clock.

The serial receiver will collect the complete A-field and B-field and store it in the common data memory. Before the A-field is received, the A-field start address is programmed by the PCC. Upon reception of A-field nibbles, the address is updated by the serial receiver. Meanwhile, the PCC will program the B-field start address.

In Fig.5 the data flow in the serial receiver is shown. Note that almost no decoding of messages is required. Only the header of the A-field needs to be decoded to check if a ciphered message is being received or transmitted, which requires the ciphering to be switched on in the A-field also.

6.5.2 SERIAL TRANSMITTER

The serial transmitter performs the reverse of the receiver functions. Several blocks used in the receiver are also used in the transmitter. Amongst these are the CRC-generators, the scrambler, and the address registers. Figure 6 shows the serial transmitter structure.

By transmitting the X-CRC twice, the Z-field is transmitted. The handling of the address registers is the same for the transmitter. Transmission of the synchronization sequence (S-field) is done using the same method as the A-field and B-field. The S-field is stored in the common data memory and will be fetched by the transmitter, just before transmission.

Two additional functions are not shown in Fig.6:

- In the handset the data in the serial transmitter may be advanced by a programmable number of bit periods. This is done to compensate for the delay in the RF section
- The transmitted data can be inverted (using a switch in the PCD5043 mode register), in order to connect the PCD5043 to VCOs requiring negative modulation.

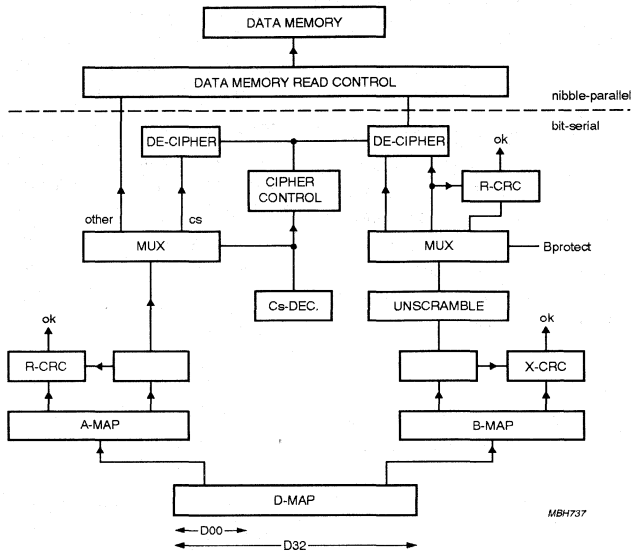


Fig.5 Serial receiver structure.

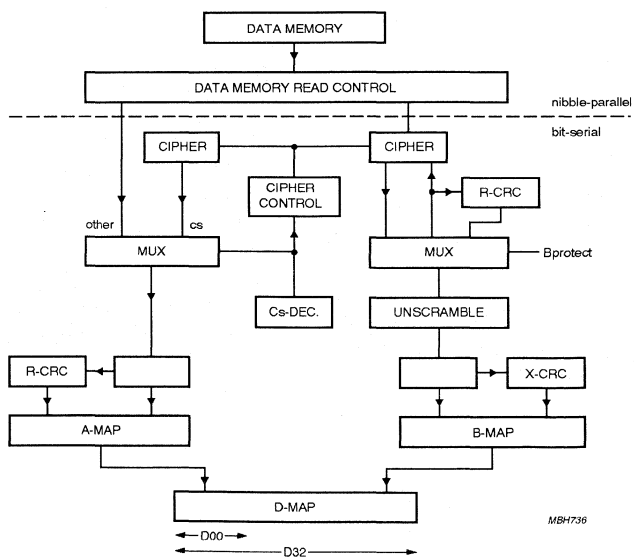


Fig.6 Serial transmitter structure.

6.5.3 SEAMLESS HANDOVER

Seamless handover guarantees that when speech information is switched from one slot to another, no speech samples are lost, added or displaced. Seamless handover is achieved in the RF interface by:

- Using a look-up table containing the correct start addresses of the B-fields in the data memory
- The RF receive and transmit blocks move data to/from the data memory block in 4-bit nibbles.

6.5.4 RF CONTROL SIGNALS

The timing of the control signals to the RF section is fixed, but such that an RF delay between 1.5 and 7 μs can be tolerated. Only the transmitter ramp signal and the synthesizer enable are programmable within certain limits.

6.5.5 SYNTHESIZER PROGRAMMING

To program a synthesizer, a 3-wire serial interface is used. The signals on this interface are:

- S_ENABLE (enable)
- S_CLK (clock)
- S_DATA (data).

To program various types of synthesizers, a 3-byte shift register is present. Three data formats are supported: 8, 16 or 24 bit words can be selected. The transfer of data from a frequency table in the common data memory to the shift register is under control of the PCC.

6.5.6 RSSI MEASUREMENT

The RSSI measurement in the PCD5043 RF-interface block is done in 3 parts: a peak/hold detector, a 6-bit A/D converter, and an RSSI control unit, which controls the peak/hold detector and the A/D converter. Once per slot time, a sample is fetched by the PCC and saved in the appropriate area of the common data memory.

If the radio receiver is active in a particular time slot, the RSSI value will automatically be measured in that slot. Adjustment to the RSSI_AN input level can be made with VREF.

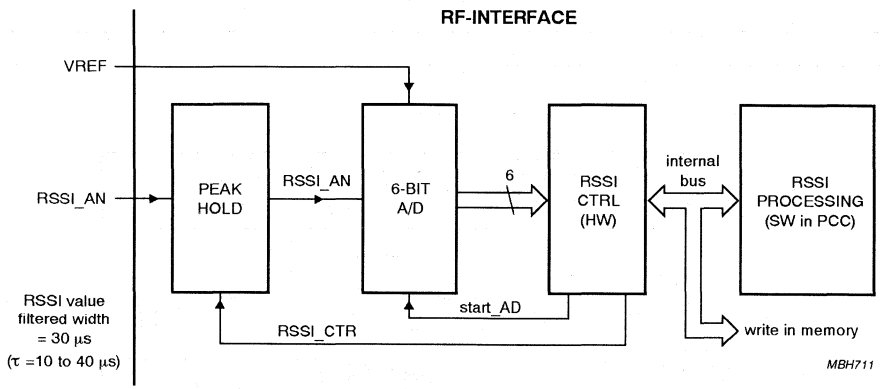


Fig.7 RSSI measurement path.

6.5.7 LOCAL CALL SWITCHING (see Fig.8)

The PCD5043 provides a local call switching function in the base station. It will store incoming speech nibbles in the common data memory, in the area reserved for that particular receive slot. Then, during the transmit phase, it passes the start pointer of the same data memory area to the transmit block. Thus, the speech data is echoed to the other user. To handle quality degradation for local calls, a mute can be performed at the RF side of the speech buffer.

6.5.8 DATA SYNCHRONIZATION (see Fig.9)

The data synchronization is done in 2 phases:

- Bit synchronization
- Sync word detection.

Bit synchronization is done using a Digital PLL (DPLL), with an oversampling factor of 12, i.e. the DPLL is running at 12 times the data rate. The output from the DPLL is a receive clock signal (RxC), which acts as the enable for a 20-bit shift register.

Sync word detection is achieved by checking the incoming data pattern with the expected synchronization field pattern, using a correlator.
The correlator has a programmable threshold, so it can accept bit errors in the sync field pattern up to the threshold level. Furthermore, the correlator window is programmable. This means that 'SlotSync', which indicates the slot synchronization event, can be detected only during a certain period (the time window).

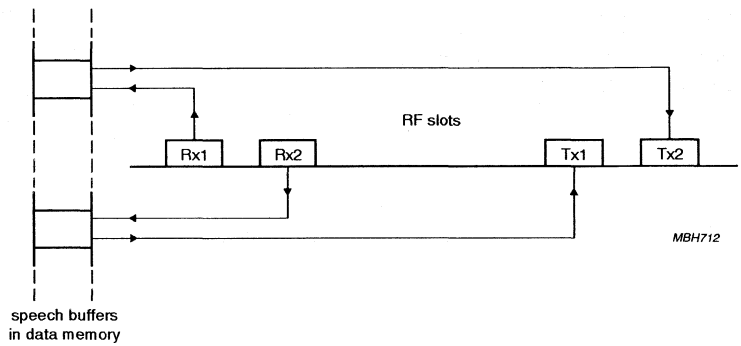


Fig.8 Local call switching on the RF-side.

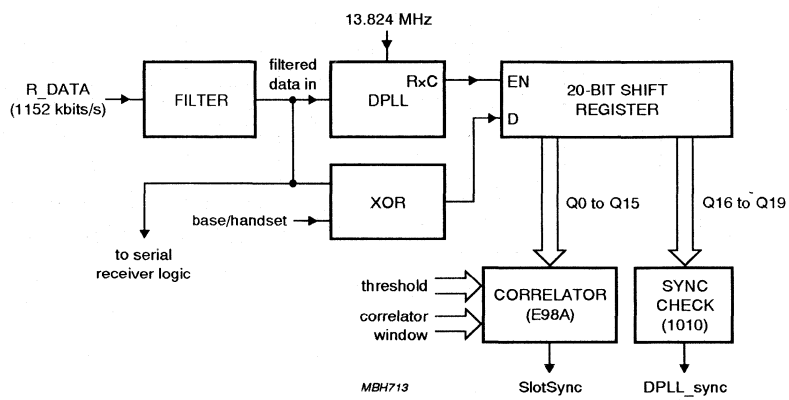


Fig.9 Schematic of the receiver synchronization part.

The 'DPLL_sync' indication should only be used, when 'SlotSync' is active. It indicates that the last 4 bits of the pre-amble field (the training sequence) are received correctly, and thus indicates that the DPLL was in lock (synchronized) in time. If the 'SlotSync' is active, and the 'DPLL_sync' is not, then a sliding interferer might have been detected.

If 'SlotSync' is not detected, effectively no data is received in that slot. This implies a 'fast mute' because speech data received in the previous frame is not destroyed.

6.5.9 CIPHERING MACHINE

The description of the cipher machine is subject to confidentiality. The specification of its algorithms are delivered by ETSI under the terms of a Non-Disclosure Agreement.

The cipher machine is under control of the TBC, which is implemented in the PCC. The cipher machine generates 2 fields of ciphering bits:

- A_cipher (40 bits) for A-field messages (ciphers tail only)
- B_cipher (320 bits) for speech in B-field.

The transmitted ciphered bits are then:

- A_ciphered: = A XOR A_cipher
- B_ciphered: = B XOR B_cipher.

On reception by the peer end point, deciphering consists of the same operation thanks to the synchronous generation of A_cipher and B_cipher.

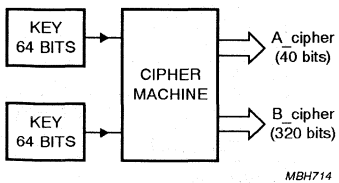


Fig.10 Cipher machine and its sources.

The cipher machine is time-multiplexed on a slot basis. Initially, the Initialisation Vector (IV) and the key must be loaded into the cipher machine. Transfer of the IV and key from the common data area to the cipher machine is done automatically by the cipher machine. The contents of the memory space where IV and key are found, are the responsibility of the PCC, and the external microprocessor.

6.6 Microcontroller Interface

6.6.1 FUNCTION OF THE MICROCONTROLLER INTERFACE

The microcontroller Interface will provide the following services.

- Direct interface to processors which have an INTEL-8051 compatible interface
- General interface to processors that can handle 'wait states' e.g. 68000-family; in this case glue logic is required
- Processor clock signal of which the frequency is programmable in order to adjust instantaneously processor performance to processor work load
- A programmable interrupt register
- A watchdog timer with time-out periods of 1.25 or 82 seconds, depending on the programming.

The microcontroller can address the PCD5043 as any other RAM memory connected to the microcontroller bus. By writing the 'Interface-Mode Register', the microcontroller can select the interface mode and its own clock frequency.

6.6.2 MICROCONTROLLER INTERRUPTS

The function of microcontroller Interrupts is to make optimal use of the microcontroller's processing power, and to achieve optimal cooperation between time-critical tasks and less time-critical tasks both executed in software. Three registers are available to handle interrupts. These are:

- Interrupt Event Register
- Interrupt Enable Register
- Interrupt Reset Register.

These registers are to be regarded together. Corresponding bits in these registers relate to one and the same event. Bits in the Interrupt Event Register are set by the PCC and are to be reset by the external processor by writing '1's in the corresponding bits in the Interrupt Reset Register. The mask in the Interrupt Enable Register enables the interrupt if corresponding events do occur.

6.6.3 WATCHDOG

The PCD5043 is equipped with a watchdog timer, which generates a reset towards an external device (e.g. a μC) after time-out. Two (fixed) time-out periods can be programmed; 1.25 s and 82 s. The watchdog function can be disabled by using the EN_WATCHDOG input pin.

6.6.4 POWER-DOWN

The PCC may switch off the 6.912 MHz internal clock, to enter a power saving mode. All blocks, running on this clock are then switched off (i.e. RF-interface, cipher block, speech interface, PCC). This is called the power-down state, and is only used in the handset mode.

The 13.824 MHz clock is never switched off. The Timing Control, microcontroller interface, and Bus Controller keep running, in order to remain synchronous with a base station, and to keep the wake-up circuitry active. During power-down the external microcontroller has still access to the common data area.

6.7 Survey of registers

For a survey of all addresses occupied refer to Tables 1 and 2. Some of the address locations are used differently for read and write. The addresses 000 to 7DF are occupied by RAM memory, while the upper 32 bytes are assigned to the hardware registers. A part of the RAM memory is allocated for use by the RF block, cipher block, and the speech interface.

Table 1 Hardware register addresses

ADDRESS	WRITE	READ
7E0	–	–
7E1	S-DATA1	–
7E2	S-DATA2	–
7E3	S-DATA3	RMT-STAT
7E4	–	RF-STATUS
7E5	B-field-shift	–
7E6	B-field-loc.	–
7E7	A-field-loc.	–
7E8	window-wide-off	–
7E9	window-wide-on	–
7EA	window-narrow-off	–
7EB	window-narrow-on	–
7EC	T-power-rmp-on	–
7ED	synth-off	–
7EE	RF-control-port	sync-status
7EF	slot-cnt-off	slot-counter-copy
7F0	frame-cnt-ref	RSSI
7F1	sync-ref-preset	bit-counter-copy1
7F2	bit-counter-preset	bit-counter-copy2
7F3	frame-counter	frame-counter
7F4	slot-counter	slot-counter
7F5	sync-control	sync-control
7F6	BMC-mode	BMC-mode
7F7	correlator-threshold	measure
7F8	watchdog-1	–
7F9	watchdog-2	–
7FA	–	–
7FB	–	–
7FC	interrupt-event	interrupt-event
7FD	interrupt-enable	interrupt-enable
7FE	interrupt-reset	–
7FF	controller mode	controller mode

8 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{amb}	operating ambient temperature		−25	−	+70	°C
V_{DD}	supply voltage		2.7	−	5.5	V
$V_{DD(ret)}$	RAM retention voltage		1.0	−	V_{DD}	V
I_{DD}	operating supply current	note 1	−	6	12	mA
$I_{DD(stb)}$	standby supply current	note 2	−	1	3	mA
	clock input duty cycle	All inputs LOW except WRN; XTAL1 running at 14 MHz	45	−	55	%
Digital I/O						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
V_{OL}	LOW level output voltage		0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
V_{OH}	HIGH level output voltage		$0.7V_{DD}$	−	V_{DD}	V
I_{LI}	input leakage current				1.0	μA
$I_{O(source)}$	output source current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{O(sink)}$	output sink current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	−	mA
$I_{RDYN(sink)}$	RDYN output sink current	V_{DD} = 3.6 V; V_O = 0.4 V	2.0	5.0	−	mA
		V_{DD} = 5.0 V; V_O = 0.4 V	−	6.0	−	mA
f_{DCK}	DCK input frequency	n = 1 to 32	−	n × 64	−	kHz
f_{FS1}	FS1 input frequency		−	8	−	kHz
Oscillator (inputs XTAL1 and XTAL2)						
g_m	transconductance	V_{DD} = 2.7 V	0.6	−	−	mS
		V_{DD} = 3.6 V	−	1.6	−	mS
R_F	feedback resistance		200	500		kΩ
RSSI Peak detector (6-bit linear A-D converter, for RSSI measurement on input RSSI_AN)						
$V_{i(RSSI\_AN)}$	input level		0	−	V_{DD}	V
$V_{conv(RSSI\_AN)}$	voltage conversion range		0	−	V_{REF}	V
$V_{i(VREF)}$	V_{REF} input voltage		1.0	3.0	V_{DD}	V
$Z_{i(VREF)}$	V_{REF} input impedance	during power-down high impedance	−	50	−	kΩ
t_{conv}	conversion time		18.4	−	−	μs
	integral non-linearity		−	−	4	LSB
	differential non-linearity	note 3	−	0.2	1.5	LSB
$Z_{i(RSSI\_AN)}$	input impedance RSSI_AN		−	1	−	MΩ

Notes to the characteristics

1. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; one speech link active (under typical conditions).
2. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; after reset.
3. Maximum differential non-linearity at supply voltage 5.5 V and V_{REF} = 1 V.

Table 2 Fixed RAM locations

ADDRESS	ENTRY
740 to 747	cipher key vector #0
748 to 74F	cipher key vector #1
750 to 757	cipher key vector #2
758 to 75F	cipher key vector #3
760 to 767	cipher key vector #4
768 to 76F	cipher key vector #5
770 to 777	cipher key vector #6
778 to 77F	cipher key vector #7
780 to 787	cipher key vector #8
788 to 78F	cipher key vector #9
790 to 797	cipher key vector #10
798 to 79F	cipher key vector #11
7A0 to 7A7	cipher init vector
7A8 to 7AA	not used
7AB	XZ field buffer
7AC to 7AF	S-field buffer
7B0 to 7BB	cipher-slot-control-table
7BC to 7BF	not used
7C0 to 7DF	speech-slot-control-table

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_i	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	–	+500	mW
P_O	power dissipation per output	–	30	mW
I_{DD}	supply current	−100	+130	mA
I_{SS}	ground current	−100	+130	mA
T_{stg}	storage temperature range	−55	+100	°C
T_j	operating junction temperature	–	90	°C

8 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{amb}	operating ambient temperature		−25	–	+70	°C
V_{DD}	supply voltage		2.7	–	5.5	V
$V_{DD(ret)}$	RAM retention voltage		1.0	–	V_{DD}	V
I_{DD}	operating supply current	note 1	–	6	12	mA
$I_{DD(stb)}$	standby supply current	note 2	–	1	3	mA
	clock input duty cycle	All inputs LOW except WRN; XTAL1 running at 14 MHz	45	–	55	%
Digital I/O						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{OL}	LOW level output voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
V_{OH}	HIGH level output voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current				1.0	µA
$I_{O(source)}$	output source current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	–	mA
$I_{O(sink)}$	output sink current	V_{DD} = 3.6 V; 0.4 V ≤ V_O ≤ V_{DD} − 0.4 V	2.0	5.0	–	mA
$I_{RDYN(sink)}$	RDYN output sink current	V_{DD} = 3.6 V; V_O = 0.4 V	2.0	5.0	–	mA
		V_{DD} = 5.0 V; V_O = 0.4 V	–	6.0	–	mA
f_{DCK}	DCK input frequency	n = 1 to 32	–	n × 64	–	kHz
f_{FS1}	FS1 input frequency		–	8	–	kHz
Oscillator (inputs XTAL1 and XTAL2)						
g_m	transconductance	V_{DD} = 2.7 V	0.6	–	–	mS
		V_{DD} = 3.6 V	–	1.6	–	mS
R_F	feedback resistance		200	500		kΩ
RSSI Peak detector (6-bit linear A-D converter, for RSSI measurement on input RSSI_AN)						
$V_{i(RSSI\_AN)}$	input level		0	–	V_{DD}	V
$V_{conv(RSSI\_AN)}$	voltage conversion range		0	–	V_{REF}	V
$V_{i(VREF)}$	V_{REF} input voltage		1.0	3.0	V_{DD}	V
$Z_{i(VREF)}$	V_{REF} input impedance	during power-down high impedance	–	50	–	kΩ
t_{conv}	conversion time		18.4	–	–	µs
	integral non-linearity		–	–	4	LSB
	differential non-linearity	note 3	–	0.2	1.5	LSB
$Z_{i(RSSI\_AN)}$	input impedance RSSI_AN		–	1	–	MΩ

Notes to the characteristics

1. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; one speech link active (under typical conditions).
2. V_{DD} = 3.0 V; f_{clk} =13.824 MHz; no external load; after reset.
3. Maximum differential non-linearity at supply voltage 5.5 V and V_{REF} = 1 V.

FEATURES

- CMOS low-voltage, low-power
- Can be used in burst mode with power-down
- Three-wire serial bus interface with the bus available in power-down mode
- On-chip ramp generator for 256 different power levels
- Extendable dynamic range
- Two programmable regulator start conditions, V_{KICK} and V_{HOME}
- Programmable analog output voltage limitation
- Ramping speed depending on the 13 MHz system frequency clock for Global System for Mobile communications (GSM) and Personnel Communications Network (PCN)
- Low swing input buffer for the 13 MHz master clock
- Compatible to a large number of different RF power modules
- Programmable temperature matching
- Quick restart option.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	2.7	5.0	5.5	V
V_{DDA}	analog supply voltage	2.7	5.0	5.5	V
$I_{DD(tot)}$	total supply current	–	9	15	mA
T_{amb}	operating ambient temperature	–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5075	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266

BLOCK DIAGRAM

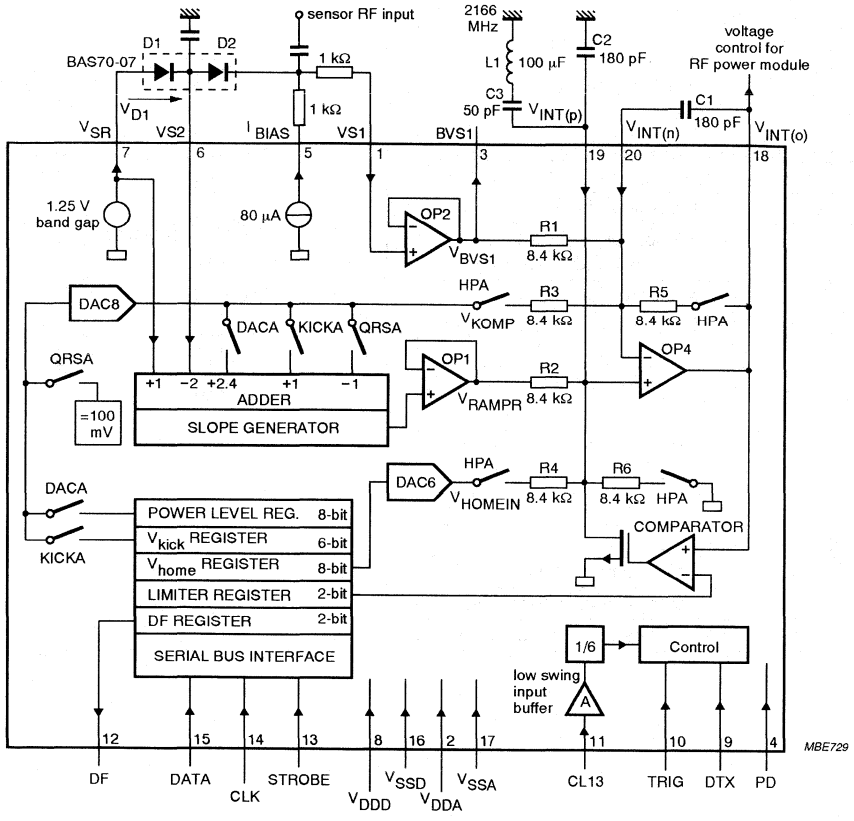


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VS1	1	sensor signal input 1
V_{DDA}	2	analog supply voltage
BVS1	3	buffered sensor output signal
PD	4	power-down input
I_{BIAS}	5	bias current output for external rectifier
VS2	6	sensor signal input 2
V_{SR}	7	bias voltage output for sensor
V_{DDD}	8	digital supply voltage
DTX	9	test, disable or stop TX burst (has to be connected to V_{SSD})
TRIG	10	trigger signal input
CL13	11	13 MHz master clock pulse input (LOW swing input)
DF	12	programmable 3-state output
STROBE	13	serial bus strobe input signal
CLK	14	serial bus clock input signal
DATA	15	serial bus data input signal
V_{SSD}	16	digital ground
V_{SSA}	17	analog ground
$V_{INT(o)}$	18	integrator output voltage
$V_{INT(p)}$	19	integrator positive input voltage
$V_{INT(n)}$	20	integrator negative input voltage

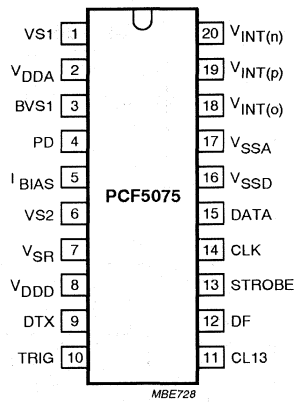


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

This CMOS device integrates operational amplifiers, two digital-to-analog converters and a serial interface to implement an 'Integrating-Controller'. It is designed to control both the power level and the up and down-ramping of GSM-transmit bursts.

The GSM/PCN power-up power-down ramping curves are generated on-chip, using an internal clock frequency of 2.166 MHz ($T_{cy} = 1/f_{clk}$), that is generated internally by dividing the external 13 MHz clock by six.

Generally, the power amplifier is ramped-up after a rising edge on TRIG (pin 10) and ramped-down after a falling edge. When TRIG goes LOW for less than two clock periods ($2T_{cy}$), a special function for base station applications is activated (see Chapter "Appendix A: base station features").

When DTX (pin 9) becomes active during a ramp-up, ramping is stopped and a normal ramp-down is executed thereby turning the power module off. To restart the ramp generator, DTX and TRIG have to go LOW (TRIG has to stay LOW for more than two clock periods). The next LOW-to-HIGH transition will cause a ramp-up again.

The contents of the power-level register (PL7-to-PL0) determines which of 256 possible values the top of the clock period burst will have.

To match the controller to different power modules and sensors several parameters must be adapted:

1. The typical value of the external capacitors C1 and C2; C1 determines the maximum bandwidth of the power control loop, depending on the highest steepness of the control curve of the power module and on the sensor attenuation (see Fig.4).
2. The upper voltage limit of $V_{O(INT)}$ (pin 18) to protect the power module; the output of $V_{O(INT)}$ can be limited to 4.0 V, 3.4 V or 2.7 V, depending on the contents of the limiter register (lim1-to-lim0). The fourth limiter register word can be used to switch the limiter option off. This limiting results in a ringing at $V_{O(INT)}$ (200 mV (p-p) typ.) but, because the power module is in saturation, it will not transfer the ringing to the antenna.
3. The HOME $V_{O(INT)}$ position; the integrator output voltage at home position, (PD and TRIG LOW) must be programmed with the V_{HOME} register. Bits Vh5-to-Vh0 are fed into a 6-bit DAC that generates a part of V_{HOME}.
4. The temperature behaviour of the home position; bits Dvh1 and Dvh0 must be used to add 0, 1 or 2 internally generated diode voltages to V_{HOME}. In this manner it is possible to compensate for a possible temperature dependence (–2 mV/°C or –4 mV/°C) of the control curves of the power module.
5. The KICK voltage; the 6 bits of the KICK voltage register (Vk5-to-Vk0) determine the differential integrator input voltage just after a ramp-up starting signal is detected.

The register information is written via a three-wire serial bus (see Sections "Serial bus programming" and "Data format").

The DF output (pin 12) is a general purpose pin which can have three different states, LOW, HIGH and 3-state, depending on the values of DF0 and DF1 in the serial register.

Separate power supply pins are provided for the analog and digital blocks.

Primary start condition

When the power supply is first switched on, the PCF5075 is in an undefined state because the chip has neither a power-on-reset nor a reset pin. Consequently, a first initialisation of the digital part is necessary.

The easiest way of doing this is to perform a short dummy ramp-up/ramp-down sequence, apply the 13 MHz master clock, make PD LOW and then toggle TRIG LOW-HIGH-LOW for more than two clock periods in the HIGH state. The chip will stay initialized as long as the supplies are on. After this, recognition of the 13 MHz master clock and TRIG will be influenced by PD.

PD LOW

The serial bus is operating, e.g. all registers can be programmed but no effect will be seen on any pin. The contents of these registers are passed to the rest of the circuit only during power-up and with the 13 MHz master clock applied.

Also, because the LOW-input swing buffer at pin CL13 is switched off, neither the adder nor the slope generator will function. This means that after the chip is powered-up, the outputs have to settle again to the programmed register values. The settling time is dominated by the slow power-up of the band gap of typically 250 μs.

If the chip is used in the burst mode, it is important to switch on the PCF5075 before the power module or the

RF-power. Otherwise it is possible that a positive spike at $V_{O(INT)}$ will open the power module.

A save value is t_{ON} = 400 μs between the PCF5075 and the power module respectively the next TRIG pulse (see Fig.3).

PD HIGH

The whole chip is active. Pin CL13 clocks the internal state machine as well as the adder and slope generator. Every change at TRIG is recognized if the master clock is running. The contents of the serial bus registers are processed. If the master clock is switched off during power-up, the state machine is stopped and the output of the adder/slope generator becomes undefined. Nevertheless, by reactivating the master clock, the output of the adder/slope generator will settle to the old values again.

The analog integrating controller

The analog integrating controller consists of three operational amplifiers (OP1, OP2 and OP4) and one comparator. OP1 and OP2 are only used for buffering purposes, OP 4 is used to form a differential integrator. The comparator is used to limit the integrator output voltage to the value selected by the 'lim'-bits in the serial register.

A two (Schottky) diode external rectifier is connected to pins V_{SR}, VS2, I_{BIAS} and VS1.

The SC-Adder block basically generates the voltage $V_{SR} - 2V_{D1} + V_{PL}$.The differential integrator then integrates the difference of this voltage and the voltage $V_{SR} - 2V_{D1} + V_{RFIN}$. The integrator output voltage $V_{O(INT)}$ is used to control the power amplifier module.

Table 1 Definition of some voltages (see Fig.1)

SYMBOL	DESCRIPTION
V_{SR}	band gap voltage, typically 1.25 V
V_{D1}	voltage over the (external) Schottky diode D1
V_{PL}	voltage determining the power level; it is generated in the SC-Adder block if switch DACA is closed (i.e. if the signal DACA is HIGH); equals 2.4 times the DAC8 output
V_{RFIN}	voltage difference at pin VS1 when RF is rectified at the sensor diode D2
V_{BVS1}	buffered voltage from pin VS1
V_{KICK}	kick voltage; if KICKA is HIGH, DAC8 outputs this voltage
V_{KOMP}	voltage at R3 if the circuit is switched to the home position by HPA; V_{KOMP} compensates V_{KICK} at R2
V_{RAMPR}	buffered output voltage of the slope generator; steady state limits of some succeeding filtered voltage steps (not 1:1 visible at pin $V_{INT(p)}$) HPA/KICKA active: $V_{SR} - 2V_{D1} + V_{KICK}$ DACA active: $V_{SR} - 2V_{D1} + V_{PL}$ QRSA active: $V_{SR} - 2V_{D1} - V_{QRS}$
V_{HOMEIN}	if HPA is active, DAC6 outputs the value of the V_{HOME} register which is directly visible only at pin 18; V_{HOMEIN} also contains the diode forward voltages nV_F (with n = 0,1 or 2; $V_F \approx 700$ mV at T_{amb} = 27 °C)
V_{QRS}	0 or 100 mV; 0 V only if a 'Quick Restart' condition is detected; otherwise, if QRSA is active, DAC8 outputs 100 mV; this voltage is inverted by the adder and causes a ramp-down with a shortened tail

Ramp generation (see Fig.3)

The circuit is activated with the PD signal going LOW before time mask 'AS' and deactivated after ramping-down, e.g. at 'GS' to 'HS'. For this usual "power-down burst mode" application in GSM/PCN mobile stations the RF input power at the power module must be activated between 'AS' and 'BS' (when the home position at $V_{O(INT)}$ has already reached its stable value) and deactivated between 'GS' and 'HS'.This is necessary for many types of power modules to meet the –70 dB margin. For quick restart after ramping-down see Chapter "Appendix A: base station features".

A ramp-up is started by a positive edge on TRIG. To be able to detect a quick restart (base station applications only) the TRIG signal is internally delayed by two clock periods. Because of this, all other internal signals are delayed by two clock periods with respect to the signal at pin TRIG.

The timing diagram shows a possible relationship between the chip timing ('B' to 'G') relative to the GSM-mask ('AS' to 'HS'). However, the user is free to choose t_1 and t_2 independently so that the mask is not violated.

Description of the signals starting at a stable home position of $V_{O(INT)}$ at time B – $2T_{cy}$.

The integrator output voltage is regulated to the value defined in the V_{HOME} register. The output of the slope generator is $V_{SR} - 2V_{D1} + V_{KICK}$ and is connected to the positive input $V_{INT(p)}$ of operational amplifier OP4 (V_{KICK} is defined by the 'V_k'-bits in the V_{KICK} register). Two clock periods after a positive edge on TRIG the integrator start condition circuitry is turned off and OP4 is switched into an integrator configuration ('B'). Now the HPA switches are open. Due to the positive differential input voltage V_{KICK}, the integrator output will start to rise. After $18T_{cy}$ ('C') the output of DAC8 is connected to the adder and slope generator block. The input of the 8-bit DAC comes from PL7 to PL0 of the power level register. The slope generator will generate a smooth curve between the former and the new output value of the adder block. The voltage V_{RAMPR} at the end is $V_{SR} - 2V_{D1} + VPL$, thus the power amplifier is ramped-up via the integrator in approximately $22T_{cy}$.

This condition is stable providing TRIG remains HIGH. Two clock periods after a negative edge at TRIG the ramp-down is started ('E').The adder output voltage will change to $V_{SR} - 2V_{d1} - V_{QRS}$ (V_{QRS} = 100 mV typ.), because DACA becomes inactive and QRSA active. This additional subtraction of 100 mV causes a ramp-down with a shortened tail.The slope generator again generates a smooth curve between the new adder output voltage and the old adder output voltage. The slope generator must have reached its final value $38T_{cy}$ after the recognized falling edge of TRIG because the signal HPA is activated again and by that turning the integrator into its 'home position' ('G').The integrator output voltage will be regulated once more to the value defined in the V_{HOME} register. The adder output voltage is $V_{SR} - 2V_{D1} + V_{KICK}$. The voltage V_{KICK} is subtracted at $V_{INT(n)}$ by V_{KOMP} while the home position is active (see Fig.1). Thus the resulting voltage at $V_{O(INT)}$ has the programmed value V_{HOME}.

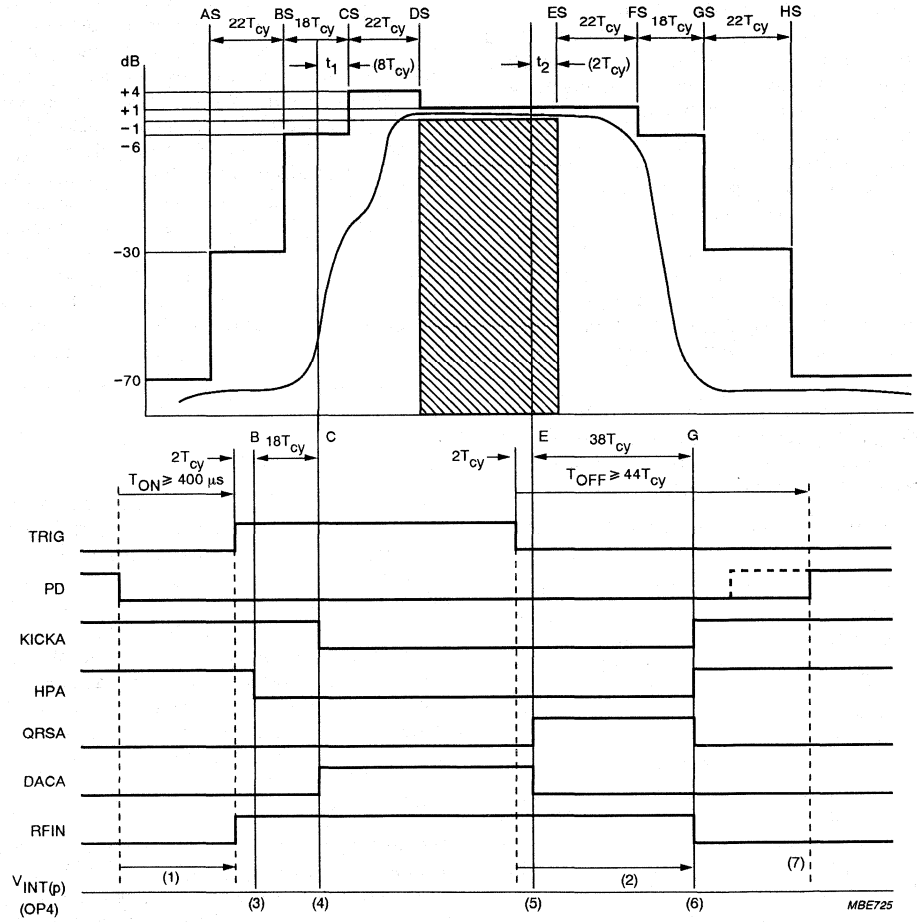
Figs 4, 5 and 6 show measurements of the circuit in application.

STABILITY

Figure 6 shows the result of a special test. A static power level was chosen where the steepness of the control curve of a worst case power module sample has the highest value. This value usually is approximately 6 to 10 dB less than the maximum possible power. Capacitors C1 and C2 are now reduced to the point where the loop is close to the limit of stability. A gain peaking at the critical frequency occurs and noise increases. By this easy procedure the critical frequency and the critical value for C1 = C2 can be found. These capacitances must now be increased by a factor of 2 to 4 for sufficient stability reserve.

CLOCK INFLUENCE

The resulting loop band width must be smaller than the internal clock frequency f_{clk} = 2.166 MHz. A gain peaking effect at f_{clk} must be avoided, low pass filters between pin $V_{O(INT)}$ and the input of the power module will reduce the stability margin and this can cause an unwanted gain at f_{clk}. As shown in the block diagram (see Fig.1) an uncritical serial resonant circuit at pin $V_{INT(p)}$ is recommended.



(1) $t_{RFON} = t_{ON} - 12T_{cy}$ to $t_{ON} + 2T_{cy}$.
(2) $t_{RFOFF} = 44T_{cy}$ to $66T_{cy}$.
(3) $V_{SR} - 2V_{d1} + V_{kick}$ (start integrator).
(4) $V_{SR} - 2V_{d1} + V_{PL}$.
(5) $V_{SR} - 2V_{d1} - V_{qrs}$.
(6) $(V_{SR} - 2V_{d1} + V_{kick} + V_{HOMEIN})/3$.
(7) This timing to the RF input power of the power module ensures that the −70 dB margin, even if the isolation of the power module is bad, is met.

Fig.3 Timing of a typical ramp-up/ramp-down curve.

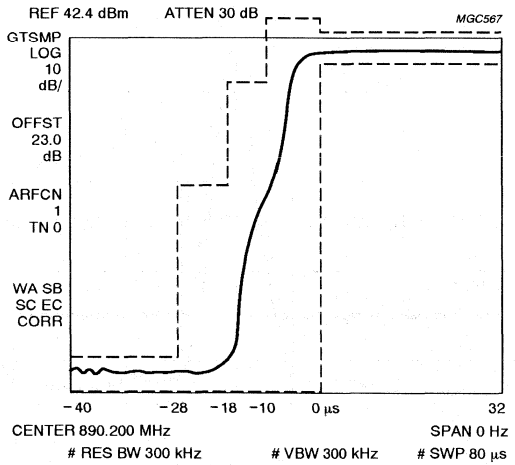


Fig.4 Ramp-up.

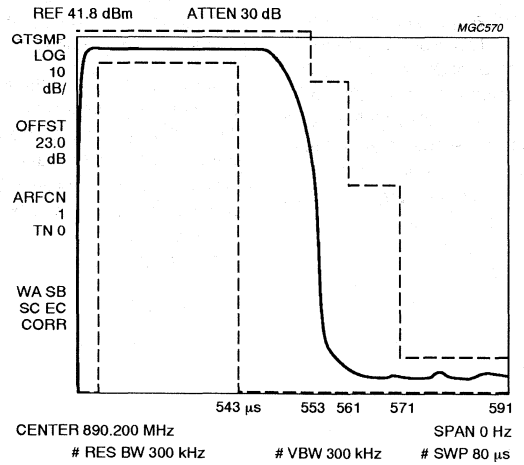


Fig.5 Ramp-down.

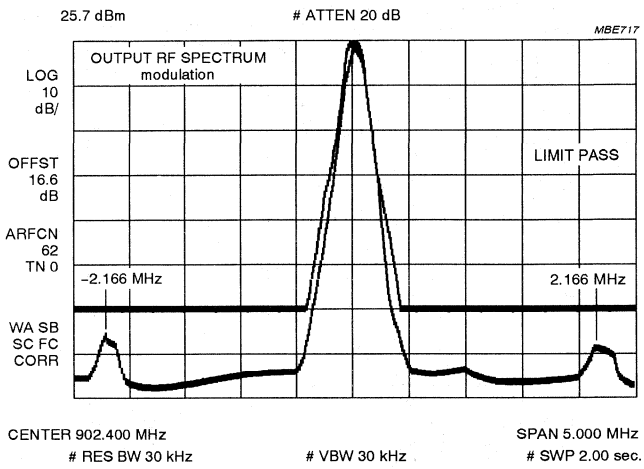


Fig.6 Modulation spectrum.

Serial bus programming

A simple 3-wire unidirectional serial bus is used to program the circuit. The 3 wires are Data, Clock and Strobe. The data sent to the device is loaded in bursts framed by Strobe. Programming clock edges and their appropriate data bits are ignored until Strobe goes active LOW. The programmed information is loaded into the addressed latch when Strobe returns inactive HIGH. Only the last 16 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. The bus is also programmable during power-down.

Data format

Data is entered with the most significant bit (MSB) first. The leading bits make up the data field, while the trailing four bits are an address field. The PCF5075 uses only one of the available addresses. The format is given in Table 2.

The trailing address bits are decoded upon the inactive Strobe edge. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous circuit operation, the strobe pulse is not allowed during internal data reads by the rest of the circuit. This condition is guaranteed by respecting a minimum Strobe pulse width after data transfer (see Chapter "Timing characteristics").

Table 2 Programming register bit usage

DATA BITS				SUBADDRESS		DEVICE ADDRESS			
MSB			LSB						
p15	pxx	p7	p6	p5	p4	p3	p2	p1	p0
data9	datax	data1	data0	Sadd1	Sadd0	add3	add2	add1	add0

The correspondence between data and address fields is given in Table 3.

Table 3 Register bit allocation

DATA FIELD (D9 TO D0)										SUB ADDRESS		DEVICE ADDRESS			
MSB									LSB						
p15	p14	p13	p12	p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	0
Vk5	Vk4	Vk3	Vk2	Vk1	Vk0	Lim1	Lim0	nu(1)	nu(1)	0	0	1	0	1	0
Vh5	Vh4	Vh3	Vh2	Vh1	Vh0	DVh1	DVh0	nu(1)	nu(1)	0	1	1	0	1	0
PL7(2)	PL6(2)	PL5(2)	PL4(2)	PL3(2)	PL2(2)	PL1(2)	PL0(2)	DF1(4)	DF0(3)	1	1	1	0	1	0

Notes

1. nu = not used.
2. PL = power level.
3. DF0 = data on DF output.
4. DF1 = enable of this output for DF1 = 0 pin DF is in 3-state mode.

Table 4 Limiter voltage

LIM1	LIM0	LIMITER VOLTAGE	TOLERANCE AT T_{amb} = 27 °C	TOLERANCE AT T_{amb} = 85 °C
1	1	limiter off	–	–
0	0	2.7 V	±250 mV	±450 mV
0	1	3.4 V	±250 mV	±450 mV
1	0	4.0 V	±250 mV	+250 to −750 mV

Table 5 DVh diode offset for V_{HOME}

DVH1	DVH0	V_{HOME}(1)(2)
0	0	Vh
0	1	Vh+ VF
1	0	Vh + 2VF
1	1	V_{DD}

Notes

1. Vh = voltage programmed into Vh5 to Vh0 generated by DAC6 (max. 2 V at V_{SR} = 1.25 V).
2. VF = an internally generated diode voltage drop with 0.7 V ±50 mV at T_{amb} = 25 °C or 0.7 V +50 to −100 mV at T_{amb} = 85 °C ($T_C \approx -2$ mV/°C).

Vk BITS

The Vk bits control the kick voltage in 64 steps of 4.8 mV per step.

Vh BITS

The Vh bits control the home position voltage in 64 steps of 32 mV per step.

PL BITS

The PL bits control the ramp-up top level voltage (equal to power level) in 256 steps of 11.7 mV per step.

LIMITING VALUES

$V_{DD} = V_{DDD} = V_{DDA}$; $V_{SS} = V_{SSD} = V_{SSA}$; in accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	7.0	V
V_i	DC input voltage on all pins	−0.5	7.0	V
I_i	DC current into any signal pin	−10	+10	mA
P_{tot}	total power dissipation	−	83	mW
T_{stg}	storage temperature	−65	150	°C
T_{amb}	operating ambient temperature	−40	85	°C

OPERATING CHARACTERISTICS

T_{amb} = −40 to 85 °C; $V_{DD} = V_{DDA} = V_{DDD}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operational amplifier (OP1)						
V_{DD}	supply voltage		2.7	−	5.5	V
B_G	gain bandwidth	at −3 dB	−	4	−	MHz
SR(p)	positive slew rate		−	0.3	−	V/μs
SR(n)	negative slew rate		−	0.3	−	V/μs
Operational amplifiers (OP2 and OP4)						
V_{DD}	supply voltage		2.7		5.5	V
B_G	gain bandwidth	at −3 dB; unity gain; C_L = 220 pF; note 1	4	−	−	MHz
CMRR	common mode rejection ratio		−	45	−	dB
PSRR	power supply ripple rejection	for unity gain	50	−	−	dB
SR(p)	positive slew rate	for unity gain; note 2	4.5	−	−	V/μs
SR(n)	negative slew rate	for unity gain; note 2	4.5	−	−	V/μs
V_{os}	voltage offset	no load at output	−7	0	+7	mV
CM_{il}	common mode input low limit	± 5% tolerance; note 3	−	−	0.5	V
CM_{ih}	common mode input high limit	± 5% tolerance; notes 3 and 4	$0.9V_{DD}$	−	−	V

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
$V_{o(min)}$	minimum output voltage	for unity gain	–	–	0.3	V
$V_{o(max)}$	maximum output voltage	for unity gain; note 4	$0.85V_{DDD}$	–	–	V
R_O	small signal output resistance	I_{load} = 2 mA at 1.9 V	–	5	10	Ω
Resistors R1 and R2						
R1	value of R1	T_{amb} = 25 °C	6.7	8.4	10	kΩ
R2	value of R2	T_{amb} = 25 °C	6.7	8.4	10	kΩ
R_{match}	matching between R1 and R2		–	2	–	%
T_C	temperature coefficient		–	0.13	–	%/°C
Programmability and accuracy of V_{PL}						
INLE	integral non-linearity error		–	–	±10	LSB
DNLE	differential non-linearity error		–	–	±1	LSB
$V_{o(min)}$	minimum output voltage	note 5	–	11.5	–	mV
$V_{o(max)}$	maximum output voltage	notes 5 and 6	–	$2.4V_{SR}$	–	V
Programmability and accuracy of V_{KICK}						
INLE	integral non-linearity error		–	–	±10	LSB
DNLE	differential non-linearity error		–	–	±1	LSB
$V_{o(min)}$	minimum output voltage	note 5	–	4.8	–	mV
$V_{o(max)}$	maximum output voltage	note 5	–	312	–	mV
Programmability and accuracy of V_{HOME}						
INLE	integral non-linearity error		–	–	±10	LSB
DNLE	differential non-linearity error		–	–	±1	LSB
$V_{o(min)}$	minimum output voltage	V_{SR} = 1.25 V; Dvh1 = 0; Dvh0 = 0; note 5	–	32	–	mV
$V_{o(max)}$	maximum output voltage	V_{SR} = 1.25 V; Dvh1 = 0; Dvh0 = 0; note 5	–	2	–	V

Notes

1. Minimum specified frequency at T_{amb} = 27 °C; for T_{amb} = 85 °C a typical value of 4 MHz is specified.
2. Slew rates are measured between 10% and 90% of output voltage interval with a load of approximately 40 pF to ground.
3. The tolerance band for the input range is defined as the interval where the output follows the input with ±5% tolerance of the actual input value.
4. These values at T_{amb} = 25 °C are supply voltage and temperature dependent (T_C = 3 mV/°C).
5. The value is dependent on V_{SR}, for tolerance of V_{SR} (see Chapter "DC characteristics").
6. The maximum output is limited to $V_{PL(max)} = 0.85V_{DD}$.

DC CHARACTERISTICS

T_{amb} = −40 to 85 °C; $V_{DD} = V_{DDD} = V_{DDA}$; $V_{SS} = V_{SSD} = V_{SSA}$ = 0 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.7	5.0	5.5	V
$I_{DD(op)}$	total operating current	f_i = 13 MHz	–	9	15	mA
$I_{DD(idle)}$	total idle current	PD = HIGH	–	–	10	μA
Logic I/O's (pins 4, 9, 10, 12 to 15)						
I_{IL}	LOW level input leakage current	V_{IL} = 0.8 V	−5	–	5	μA
I_{LH}	HIGH input leakage current	V_{IH} = 2 V	−5	–	5	μA
C_i	input capacitance		–	10	–	pF
CL13, low-swing master clock input (pin 11)						
I_{PD}	input pull-down current in power-down	V_i = 1 V; T_{amb} = 25 °C; T_C = −0.5%/°C; note 1	–	–	25	μA
C_I	input capacitance		–	10	–	pF
$\|Z_i\|$	input impedance	f_i = 13 MHz; note 1	–	5	–	kΩ
$V_{i(p-p)}$	input voltage (peak-to-peak value)	AC coupling = 33 pF	0.5	–	V_{DD}	V
Sensor DC reference input voltage VS1 and VS2 (pins 1 and 6); note 2						
V_{VS2}	input voltage		0	–	V_{SR}	V
V_{VS1}	input voltage		–	–	$0.9V_{DD}$	
Bias current source I_{BIAS} (pin 5)						
I_{BIAS}	bias current source for D1 and D2	V_i = 1 V; T_{amb} = 25 °C; T_C = −0.22μA/°C	60	80	100	μA
V_{CM}	voltage range	note 3	0.3	–	$0.9V_{DD}$	V
Band gap voltage V_{SR} (pin 7)						
V_{SR}	bandgap voltage	T_{amb} = 25 °C	1.16	1.25	1.34	V
T_C	temperature coefficient for V_{SR}		–	−0.175	–	mV/°C
T_{pu}	power-up time band gap	note 4	–	250	–	μs
Other analog I/O's (pins 3, 18, 19 and 20)						
I_{IL}	input leakage current	V_i = 1 V	−15	–	15	μA
C_I	input capacitance		–	10	–	pF

Notes

1. In power down mode this input is inactive and switched to ground with more than 40 kΩ. An AC coupling with 33 pF is recommended.
2. The voltage at pin VS2 is VS2 = $V_{SR} - V_{d1}$ with the forward voltage V_{d1} ~ 250 mV of the DC reference diode D1 of the RF sensor. V_{d1} must not be influenced by RF because a voltage change at pin VS2 moves the input voltage of the adder and slope generator.
3. Two 1 kΩ resistors close to the RF sensor diode D2 in the block diagram are necessary for RF decoupling.
4. The necessary start-up time T_{ON} = 400 μs (see Fig.3) between PD and TRIG is more than T_{pd}.

TIMING CHARACTERISTICS

T_{amb} = −40 to +85 °C; $V_{DD} = V_{DDA} = V_{DDD}$; $V_{SS} = V_{SSA} = V_{SSD}$ = 0 V; unless otherwise specified.
For timing see Fig.3; $T_{cy} = {}^{6}/_{13}$ µs.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Controller timing					
t_{qrs}	negative pulse width on TRIG for quick restart recognition	0.077	–	0.769	µs
t_{noqrs}	negative pulse width on TRIG for no quick restart recognition	1.0	–	–	µs
$t_{d(TRIG-B)}$	delay from positive TRIG edge to point B = ${}^{13}/_{6}T_{cy}$	–	1.0	–	µs
$t_{d(B-C)}$	delay from point B to point C = $18T_{cy}$	–	8.31	–	µs
$t_{d(TRIG-E)}$	delay from negative TRIG edge to point E = ${}^{13}/_{6}T_{cy}$	–	1.0	–	µs
$t_{d(E-G)}$	delay from point E to point G = $38T_{cy}$	–	17.54	–	µs
Serial bus timing					
SERIAL PROGRAMMING CLOCK (PIN 14)					
t_r	rise time	–	10	–	ns
t_f	fall time	–	10	–	ns
T_{cy}	clock period	100	–	–	ns
ENABLE PROGRAMMING (PIN 13); note 1					
t_{start}	strobe set-up time to first clock edge	40	–	–	ns
t_{end}	strobe hold time from first clock edge	20	–	–	ns
REGISTER SERIAL INPUT DATA (PIN 15)					
t_{su}	input data to CLK set-up time	20	–	–	ns
t_h	input data to CLK hold time	20	–	–	ns

Note

1. After rising edge of STROBE one more active CLK edge (LOW-to-HIGH transition) completes the transfer.

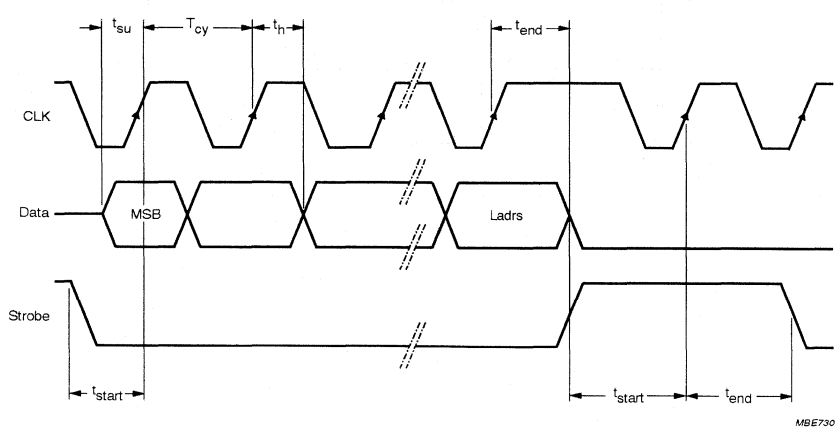


Fig.7 Serial bus timing diagram.

APPLICATION INFORMATION

Switching the dynamic range

For GSM phase 2 and PCN, some very low power levels are needed. The control voltage V_{PL} can be as low as 30 mV, which is approximately 3 LSB of the power level register and therefore not accurate enough. Nevertheless it is possible to use this chip. The DF pin (pin 12) can be used to switch a 13 dB attenuator, right after the sensor, into the antenna path.

This has the advantage of not changing the behaviour of the loop, however, the disadvantage is introducing a certain amount of attenuation when switched off. As shown in the application diagram (see Fig.8) another approach is to switch a gain stage at the sensor. By doing this the loop gain and the bandwidth of the loop will be switched. Consequently, at least a 13 dB stability margin is needed if the switchable gain stage has a range of 13 dB.

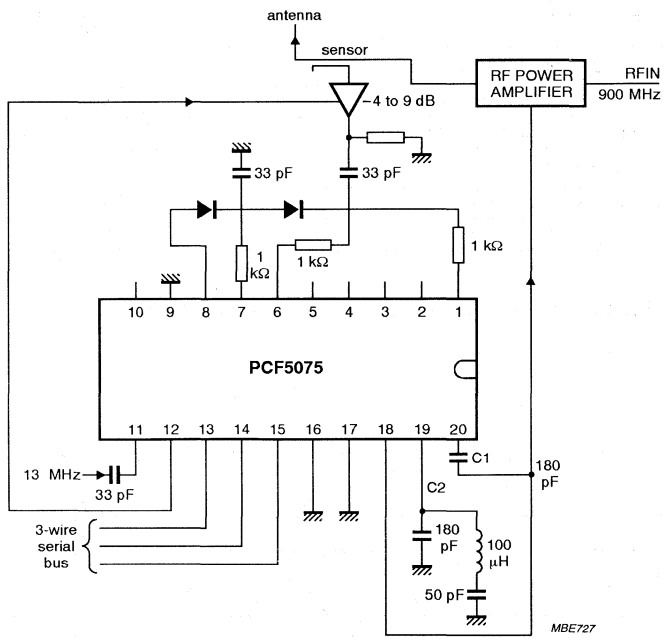


Fig.8 Application diagram for mobile stations.

Additional application information

An evaluation kit with software and demonstration boards is available for the PCF5075 together with the power modules BGY20x. Additionally, a package of PSPICE models with several plots and descriptions is also available which will provide help for applications.

Very little bus traffic is required for the PCF5075 because the ramping curves are generated on-chip. V_{KICK} and V_{HOME} define the start conditions for up-ramping. V_{PL} determines the power levels. TRIG is the trigger for up and down-ramping.

The non-linear behaviour of the control curves of the power modules have a big influence on the loop. Start conditions in the flat area of the control curve are critical and need some attention. Initially $V_{O(INT)}$ will be at the home position. The switches HPA release the regulator. The integrator now must be moved into the active part of the control curve. This is achieved by integrating V_{KICK}. When $V_{O(INT)}$ has reached the active region of the control curve the loop is closed and the circuit is able to follow the ramping function generated by a voltage step to the slope generator. The step height V_{PL} determines the power of the transmit burst. Down-ramping is started at the slope generator input by a voltage step from V_{PL} back to −100 mV. The loop follows the leading function for down-ramping until the RF sensor measures zero. The sensor signal is not able to go to −100 mV because this would represent a negative power. The reason for the −100 mV in the leading function is to shorten the tail of the slope.

For V_{KICK} a value of 60 mV is recommended, matched to a kick power that is 8 dB below −13 dBm (see Fig.9). Usually V_{KICK} has a constant value for all power levels.

One of the highlights of the PCF5075 is that for matching of the start behaviour only one parameter must be adapted to the individual sample of the power module. This parameter is the home position of $V_{O(INT)}$ that is set by V_{HOMEIN}. An optimized value must be chosen in production for the life of the device. This value can be stored in an EPROM. Software may help to adapt V_{HOMEIN} to different temperatures. The $V_{O(INT)}$ home position that has to be programmed must be matched to the middle of the two curves illustrated in Fig.9.

V_{HOMEIN} is the sum of V_{HOME} and of the diode forward voltages with a typical negative temperature behaviour. Two diodes are necessary for matching the behaviour of the power module BGY20x. But if two diodes are chosen (see Table 5), the absolute value of $V_{O(INT)}$ is so high that there is not enough room for matching the start behaviour. Therefore, only one diode is recommended for the modules BGY20x. The fine temperature matching must be done by software. Details about this matching are shown in plot 3 of the PSPICE package.

Curve 1 in Fig.9 shows what happens if the home position of $V_{O(INT)}$ has the highest usable value. This behaviour is matched to meet the −6 dB margin and the −30 dB margin at the power level −13 dBm. The −70 dB margin will be met by optimizing the time where the RF input power of the power module is activated.

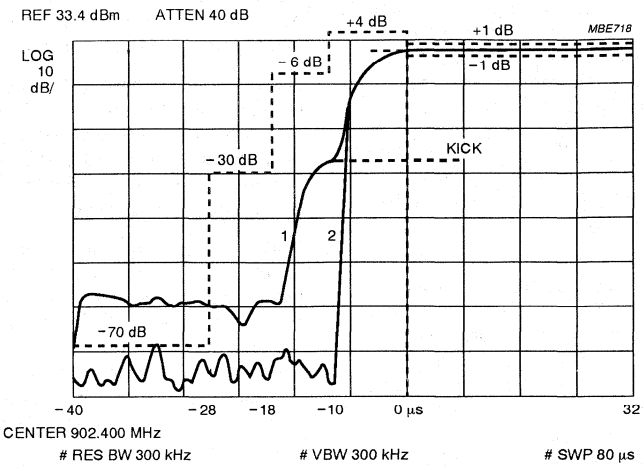
Curve 2 in Fig.9 results if the home position has the lowest usable value. Here the ramping curve seems to be optimal, but the switching spectrum is at the limit. This behaviour occurs when the regulator, which is integrating V_{KICK}, has not yet reached the active part of the power module control curve and thus the step of the slope generator has the highest steepness. In this situation the power ramps-up with a delay and with increased steepness as can be seen in the curve.

For the power level −13 dBm the TRIG time may be shifted a little by software. At all other power levels TRIG can be kept constant.

THEORETICAL LIMIT FOR CORRECT DOWN-RAMPING

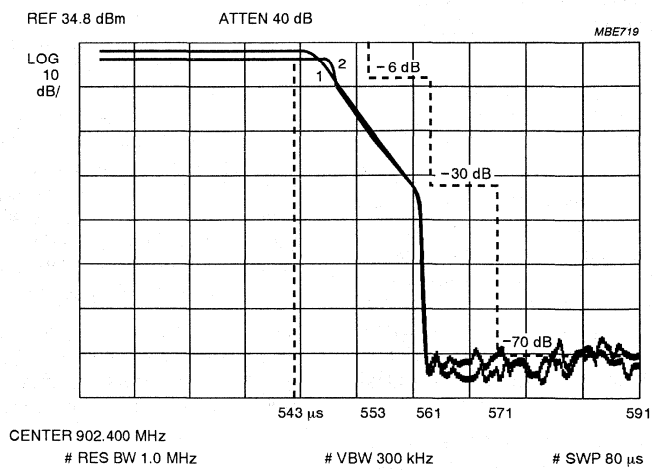
No loop is able to follow a leading value which is beyond a physical limit. The power limit of any power module depends on RF input power, transmit frequency, supply voltage and load impedance. The maximum V_{PL} must be matched to the worst case output power and reduced by 1 dB. A distance of 1 dB is necessary because the steepness of the control curve of the power module decreases for higher output power. A wrong behaviour is shown in Fig.10. Curve 1 works fine, but the module is at the power limit. If the supply voltage is reduced now, the theoretical principle of a loop design is violated. Thus the down-ramping in curve 2 starts with a delay followed by an increased steepness. The GSM margin for the switching spectrum will only be met if the maximum value of V_{PL} is matched to the possibilities of the loop.

The programmable $V_{O(INT)}$ limiter (see Table 4) is foreseen to protect the power module during error conditions such as, for example, wrong antenna connection and not to avoid the down-ramping behaviour of curve 2.



(1) Curve 1: highest usable value.
(2) Curve 2: lowest usable value.

Fig.9 Power as a function of time; rising edge (behaviour at different worst case home positions of $V_{O(INT)}$).



(1) Curve 1: correct behaviour.
(2) Curve 2: unusable behaviour with wrong V_{PL} value.

Fig.10 Power as a function of time, falling edge.

GSM signal processing IC PCF5083

1 FEATURES

- Fabricated in a 0.5 µm CMOS process with 3-layer metal
- LQFP128 package (SOT420AA-2)
- 3.3 V operation
- Low power
- Embedded DSP core for all GSM specific signal processing tasks:
  - 16-bit fixed point DSP
  - 19.5 MHz or external clock operation
  - Flexible power-down modes
  - 5 kbyte on-chip program or data RAM
  - 2 kbyte on-chip data ROM
  - 16 kbyte on-chip program ROM
  - Fully pre-programmed modules for GSM baseband tasks including all data channels
  - Dedicated GSM signal processor with application specific hardware for: equalisation, channel encoding/decoding for all traffic and control channels and encryption/decryption (A5/1 and A5/2 algorithms)
  - Tone and side-tone generation
- GSM Hardware Timer and Interface core:
  - Power saving Sleep mode for GSM mobiles
  - Programmable TDMA timing and power-down signals with 0.25 bit resolution
  - Three wire serial control bus for fast programming of RF ICs and synthesizers
  - IOM®-2 interface for external accessories, host software download and support of the Digital Audio Interface (DAI)
  - RS232 interface for the man machine interface controller
  - Man machine interface power-down control
  - Power supply control logic with Watchdog Timer
  - Real time clock and calendar running on 32.768 kHz
  - 6-bit general purpose I/O port
- Reduced swing 13 MHz main clock input
- On-chip PLL to derive the DSP and microcontroller clock
- 8-bit, 68000 compatible host interface with three interrupt lines
- Boundary scan interface in accordance with *"IEEE Standard 1149.1-1990"*.

2 GENERAL DESCRIPTION

The PCF5083 GSM Signal Processing IC is a dedicated VLSI circuit; fabricated in a 0.5 µm CMOS process. It has been designed for baseband signal processing tasks for the Pan European Global System for Mobile telecommunication (GSM). The PCF5083 is part of the second generation Philips Semiconductors GSM chip set.

The PCF5083 consists of an embedded 16-bit DSP core for all GSM specific signal processing tasks and a Timer and Interface core which contains many peripheral functions to simplify the system design.

3 APPLICATIONS

The PCF5083 is suitable for use in GSM mobile stations or hand-helds.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5083H/F2	LQFP128	plastic low profile quad flat package; 128 leads; (PCF5083-2B)	SOT420-1
PCF5083H/001/F2	LQFP128	plastic low profile quad flat package; 128 leads; (PCF5083-2C)	SOT420-1
PCF5083H/5V2/F3	LQFP128	plastic low profile quad flat package; 128 leads; (PCF5083-3A)	SOT420-1

5 BLOCK DIAGRAM

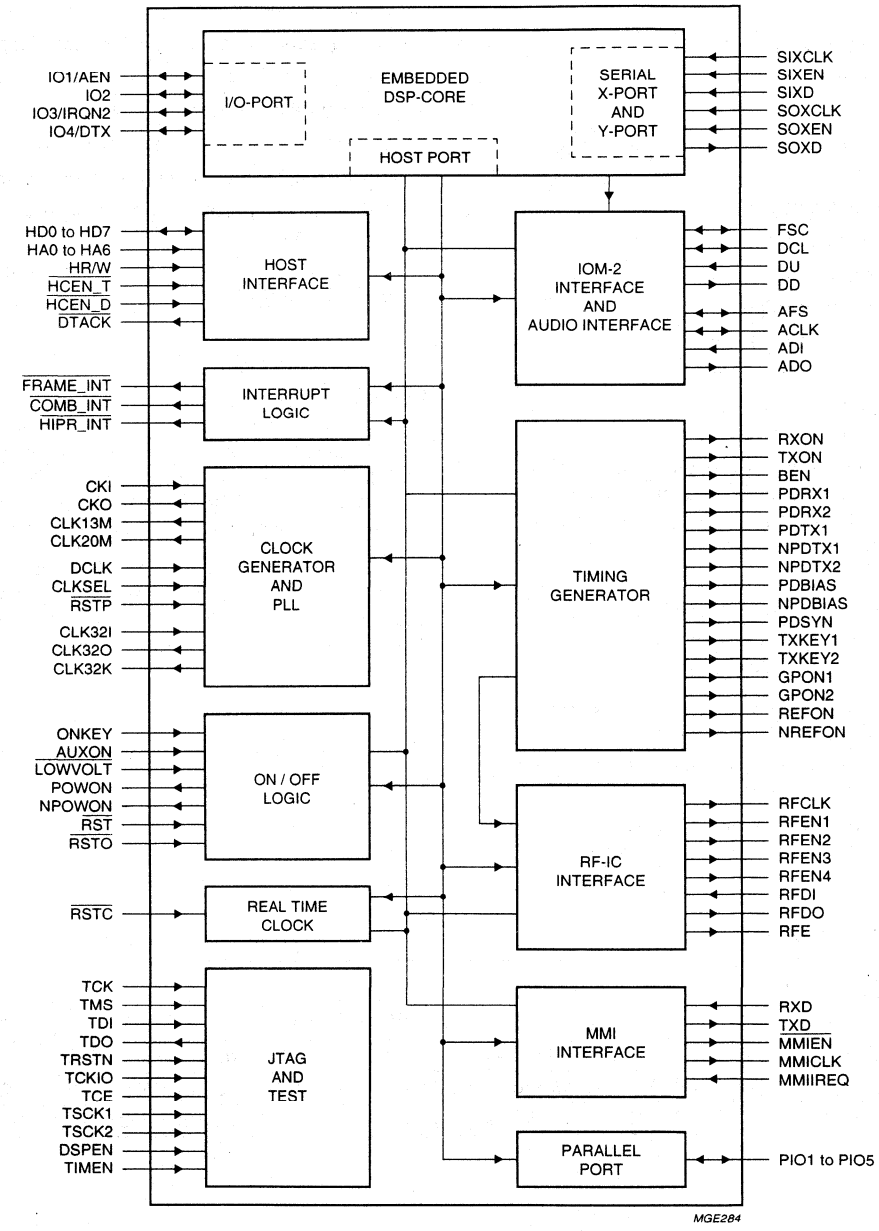


Fig.1 Block diagram.

6 PINNING INFORMATION

6.1 Pinning

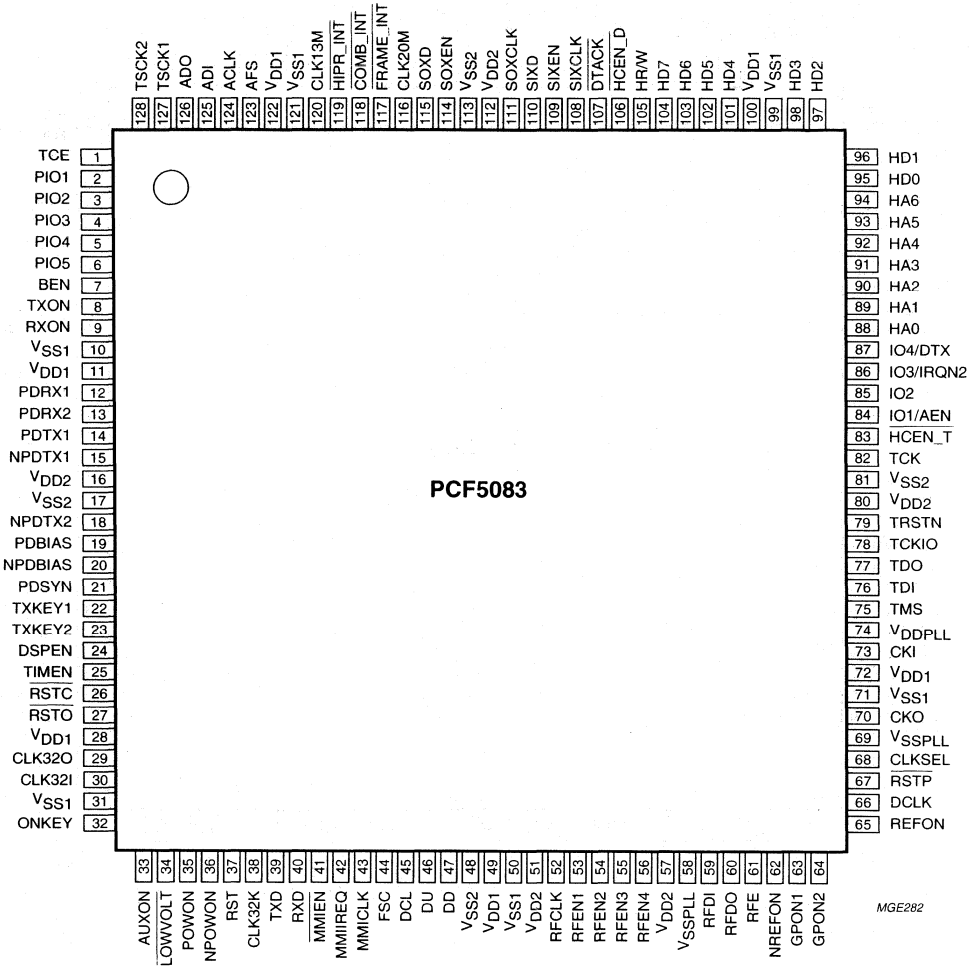


Fig.2 Pin configuration - PCF5083-2B and PCF5083-2C.

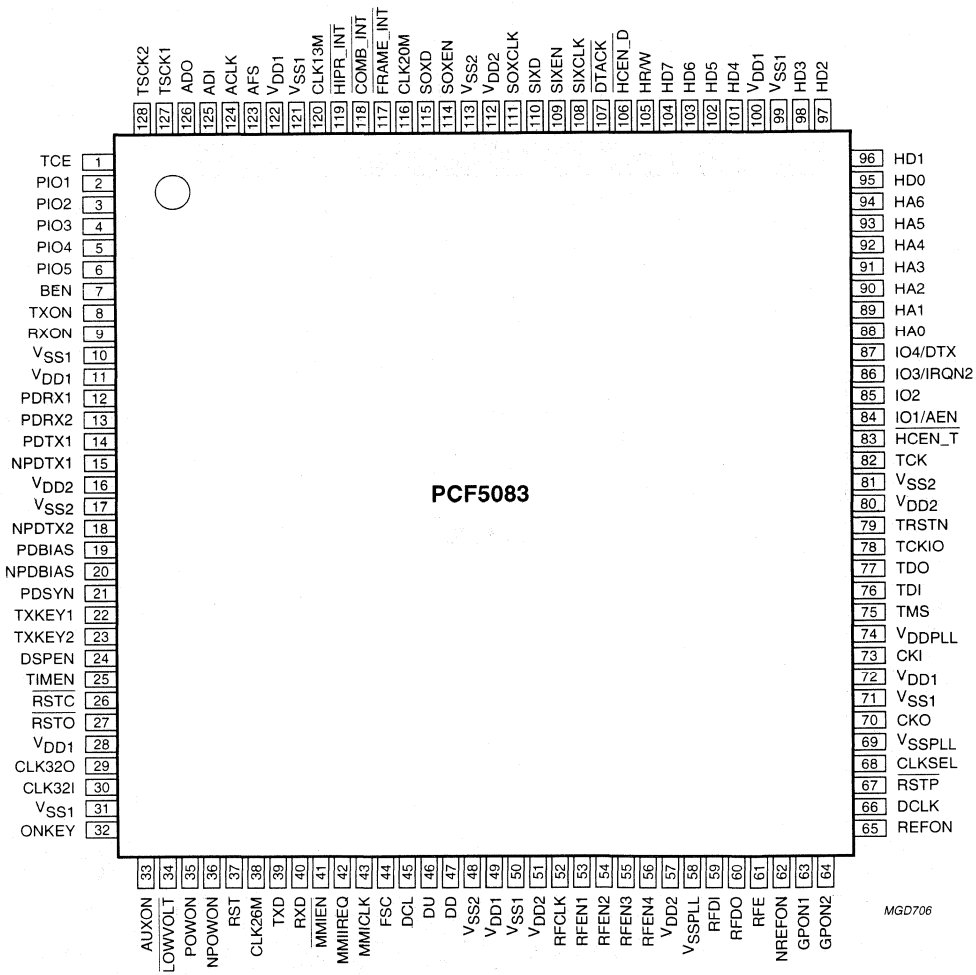


Fig.3 Pin configuration - PCF5083-3A.

6.2 Pinning description

SYMBOL	PIN	I/O	DESCRIPTION
TCE	1	I	Test Clock Enable (active HIGH); tied to V_{SS} during normal operation.
PIO1 to PIO5	2 to 6	I/O	General purpose parallel port (3-state output).
BEN	7	O	Baseband Port Enable (active HIGH, 3-state).
TXON	8	O	Modulator window enable (active HIGH, 3-state).
RXON	9	O	Receiver window enable (active HIGH, 3-state).
V_{SS1}	10		Ground I/O pin.
V_{DD1}	11		Supply I/O pin.
PDRX1	12	O	Receiver Power-down 1 (active HIGH, 3-state).
PDRX2	13	O	Receiver Power-down 2 (active HIGH, 3-state).
PDTX1	14	O	Transmitter Power-down 1 (active HIGH, 3-state).
NPDTX1	15	O	Inverted output of PDTX1 (active LOW, 3-state).
V_{DD2}	16		Supply core.
V_{SS2}	17		Ground core.
NPDTX2	18	O	Transmitter Power-down 2 (active LOW, 3-state).
PDBIAS	19	O	Transmitter power supply Power-down (active HIGH, 3-state).
NPDBIAS	20	O	Inverted output of PDBIAS (active LOW, 3-state).
PDSYN	21	O	Synthesizer Power-down (active HIGH, 3-state).
TXKEY1	22	O	Power ramping control (active HIGH, 3-state).
TXKEY2	23	O	Power module control (active HIGH, 3-state).
DSPEN	24	I	DSP Test Mode Enable (active HIGH). PCF5083-2B includes an internal pull-down resistor. PCF5083-2C does not include an internal pull-down resistor.
TIMEN	25	I	Timer Test Mode Enable (active HIGH). PCF5083-2B includes an internal pull-down resistor. PCF5083-2C does not include an internal pull-down resistor.
$\overline{\text{RSTC}}$	26	I	Asynchronous Reset - real time clock (active LOW, CMOS level Schmitt trigger input).
$\overline{\text{RSTO}}$	27	I	Asynchronous Reset - ON/OFF logic (active LOW, CMOS level Schmitt trigger input).
V_{DD1}	28		Supply I/O pin.
CLK32O	29	O	32.768 kHz crystal oscillator output.
CLK32I	30	I	32.768 kHz crystal oscillator input.
V_{SS1}	31		Ground I/O pin.
ONKEY	32	I	ON/OFF Key input (active HIGH, CMOS level Schmitt trigger input with internal pull-down resistor).

SYMBOL	PIN	I/O	DESCRIPTION
AUXON	33	I	Auxiliary Switch on input (active HIGH, CMOS level Schmitt trigger input).
$\overline{\text{LOWVOLT}}$	34	I	Low battery indication (active LOW, CMOS level Schmitt trigger input).
POWON	35	O	Power Regulator on (active HIGH).
NPOWON	36	O	Power Regulator on (active LOW).
$\overline{\text{RST}}$	37	I	Asynchronous Reset for timer section (active LOW, CMOS level Schmitt trigger input).
CLK32K	38	O	The 32.768 kHz CMOS level output for PCF5083-2B and PCF5083-2C.
CLK26M			The 26 MHz CMOS level output for PCF5083-3.
TXD	39	O	RS232 transmit data output (open-drain output).
RXD	40	I	RS232 receive data input.
$\overline{\text{MMIEN}}$	41	O	RS232 input buffer full indication (active LOW, open-drain output).
MMIREQ	42	I	MMI clock request (active HIGH, CMOS level Schmitt trigger input).
MMICLK	43	O	MMI clock 13 MHz.
FSC	44	I/O	IOM®-2 frame pulse (3-state).
DCL	45	I/O	IOM®-2 clock (3-state).
DU	46	I	IOM®-2 data input (CMOS level Schmitt trigger input).
DD	47	O	IOM®-2 data output (open drain output).
V_{SS2}	48		Ground core.
V_{DD1}	49		Supply I/O pin.
V_{SS1}	50		Ground I/O pin.
V_{DD2}	51		Supply core.
RFCLK	52	O	RF–IC interface shift clock (3-state).
RFEN1	53	O	RF–IC Interface Enable 1(active LOW, 3-state).
RFEN2	54	O	RF–IC Interface Enable 2 (active LOW, 3-state).
RFEN3	55	O	RF–IC Interface Enable 3 (active LOW, 3-state).
RFEN4	56	O	RF–IC Interface Enable 4 (active LOW, 3-state).
V_{DD2}	57		Supply core.
V_{SSPLL}	58		Ground for PLL.
RFDI	59	I	RF–IC Interface data in.
RFDO	60	O	RF–IC Interface data out (3-state).
RFE	61	O	RF–IC Interface Enable (active HIGH, 3-state).
NREFON	62	O	Reference oscillator power-down (active LOW, 3-state).

SYMBOL	PIN	I/O	DESCRIPTION
GPON1	63	O	Sleep mode power-down 1 (active HIGH, 3-state).
GPON2	64	O	Sleep mode power-down 2 (active HIGH, open-drain output).
REFON	65	O	Sleep mode power-down 3 (active HIGH, 3-state).
DCLK	66	I	External DSP clock input.
$\overline{RSTP}$	67	I	PLL reset (active LOW with internal pull-down resistor).
CLKSEL	68	I	Timer clock source select.
V_{SSPLL}	69		Ground for PLL.
CKO	70	O	Low swing input buffer output.
V_{SS1}	71		Ground I/O pin.
V_{DD1}	72		Supply I/O pin.
CKI	73	I	Reference clock input, low swing input 13 kHz.
V_{DDPLL}	74		Supply for PLL.
TMS	75	I	JTAG port mode select (with internal pull-down resistor).
TDI	76	I	JTAG port data input (with internal pull-down resistor).
TDO	77	O	JTAG port data output.
TCKIO	78	I	Auxiliary test signal - tied to V_{SS} during operation.
TRSTN	79	I	JTAG port reset (with internal pull-down resistor).
V_{DD2}	80		Supply core.
V_{SS2}	81		Ground core.
TCK	82	I	JTAG port clock input (with internal pull-down resistor).
$\overline{HCEN\_T}$	83	I	Host Interface Enable - Timer core (active LOW).
IO1/AEN	84	I/O	DSP general purpose I/O used for voice port control (CMOS level I/O). The PCF5083-3 has its own internal pull-up resistor however, both the PCF5083-2B and PCF5083-2C require a pull-up resistor.
IO2	85	I/O	DSP general purpose I/O used for voice port control (CMOS level I/O). The PCF5083-3 has its own internal pull-up resistor however, both the PCF5083-2B and PCF5083-2C require a pull-up resistor.
IO3/IRQN2	86	I/O	DSP general purpose I/O or Interrupt Request Input 2 (CMOS level I/O). The PCF5083-3 has its own internal pull-up resistor however, both the PCF5083-2B and PCF5083-2C require a pull-up resistor.
IO4/DTX	87	I/O	DSP general purpose I/O (CMOS level I/O, external pull-up resistor required).
HA0 to HA6	88 to 94	I	Host Interface Address.
HD0 to HD3	95 to 98	I/O	Host Interface Data (3-state).

SYMBOL	PIN	I/O	DESCRIPTION
V_{SS1}	99		Ground I/O pin.
V_{DD1}	100		Supply I/O pin.
HD4 to HD7	101 to 104	I/O	Host Interface data (3-state).
HR/W	105	I	Host Interface Write Enable.
$\overline{\text{HCEN\_D}}$	106	I	Host Interface Enable - DSP core (active LOW).
$\overline{\text{DTACK}}$	107	O	Host port acknowledge - used as DTACK from DSP core (active LOW, open-drain output).
SIXCLK	108	I	DSP serial input port X clock (CMOS level Schmitt trigger input).
SIXEN	109	I	DSP serial input port X enable.
SIXD	110	I	DSP serial input port X data.
SOXCLK	111	I	DSP serial output port X clock (CMOS level Schmitt trigger input).
V_{DD2}	112		Supply core.
V_{SS2}	113		Ground core.
SOXEN	114	I	DSP serial output port X enable.
SOXD	115	O	DSP serial output port X data (3-state).
CLK20M	116	O	19.5 MHz CMOS level output.
$\overline{\text{FRAME\_INT}}$	117	O	TDMA frame interrupt (active LOW, open drain output).
$\overline{\text{COMB\_INT}}$	118	O	Combined interrupt (active LOW, open drain output).
$\overline{\text{HIPR\_INT}}$	119	O	High Priority Interrupt (active LOW, open drain output).
CLK13M	120	O	13 MHz CMOS level output.
V_{SS1}	121		Ground I/O pin.
V_{DD1}	122		Supply I/O pin.
AFS	123	I/O	Audio Interface frame sync signal (3-state).
ACLK	124	I/O	Audio Interface Clock (3-state).
ADI	125	I	Audio Interface Data In, RS232 clock if enabled.
ADO	126	O	Audio Interface Data Out (3-state).
TSCK1	127	I	Test Clock 1 - tied to V_{SS} during normal operation.
TSCK2	128	I	Test Clock 2 - tied to V_{DD2} during normal operation.

7 OVERVIEW OF THE GSM CHIP SET

7.1 General

The chip set's high-level architectural modularity ensures that it can be easily adapted to meet various market requirements in terms of hardware and software. Figure 4 is a simplified block diagram of a GSM terminal using the Philips Semiconductors chip set.

The receiver converts the antenna input signal from 890 to 915 MHz down into a complex baseband signal consisting of an in-phase (I) and a quadrature component (Q). In order to deal with the high dynamic range from −104 to −10 dBm, the receiver provides an AGC input controlled by the layer 1 software in the System Controller. The complex baseband signal is connected to the input of the PCF5072 baseband interface IC. This IC samples the I and Q components at the GSM bit clock (270 kHz) with an accuracy of approximately 2 × 13 bits.

The equalizer is responsible for the following tasks:

- Channel impulse response estimation and bit synchronization by means of the training sequence
- Adaptive channel equalization with a modified Maximum Likelihood Sequence Estimation (MLSE) approach that produces a bit-by-bit soft decision information (Channel Measurement Information (CMI)
- Channel impulse response adaption and frequency offset estimation.

After decryption the channel decoder performs convolutional and block decoding. Depending on the logical channel in use, there are decoding schemes for TCH/F (FACCH/F), SACCH and SDCCH.

The speech decoder synthesises the audio signal from the received bit stream. Updating of comfort noise parameters occurs each time a valid Silence Descriptor (SID) is received. Comfort noise is inserted during periods of speech pauses. Substitution and muting of lost or bad frames is implemented.

The full rate speech encoder collects speech samples of 13-bit uniform PCM format (104 kbits/s) and compresses them to 13 kbits/s according to the linear predictive coding, long term prediction, Regular Pulse Excitation (RPE-LTP). Discontinuous Transmission (DTX) is available (voice activity detection, background acoustic noise).

To protect the data from transmission errors, block and convolutional coders form the channel encoder. The encoding modules relates to the logical channels (e.g. RACH, TCH/F (FACCH/F), SDCCH/SACCH).

After encryption the burst builder generates either Normal Bursts (NB) or Access Bursts (AB). The bit-stream is then modulated with a GMSK modulator (Gaussian Minimum Shift Keying) and upconverted in a quadrature mixer to 890 to 915 MHz.

The on-chip GSM timer generates all power-down and control signals for the receiver, the transmitter, the P90CL301 System Controller and the PCF5072 baseband interface IC.

The System Controller (P90CL301) services all HW interfaces and performs the signalling software contained in the GSM layer stack (with L1, L2, L3, O&M, UAP, SIMAP etc).

The voiceband ADCs and DACs of the PCF5072 perform the conversion between the analog audio signals and the digital domain.

7.2 The role of the PCF5083

The PCF5083 is a dedicated VLSI circuit offering baseband signal processing tasks for the Pan European Global System for Mobile telecommunication (GSM). The PCF5083 can be applied in GSM mobile stations or hand-helds. The embedded DSP core is optimized for GSM baseband functions and contains an on-chip program ROM featuring the following tasks:

- Full rate speech coding/decoding including VAD/DTX (*"GSM 06 series"*)
- Encryption/decryption according to both A5/1 and A5/2 algorithms (*"GSM Rec. 3.20, 3.21"*)
- Burst building supporting access burst and normal burst (*"GSM Rec. 5.02"*)
- Frequency Correction Burst (FCB) detection and evaluation
- Synchronization burst (SCH) detection
- BCCH monitoring of neighbouring cells
- Channel coding/decoding and interleaving/de-interleaving (*"GSM Rec. 5.03"*) for:
  - Broadcast Channels (BCH): SCH, BCCH
  - Common Control Channels (CCCH): PCH, RACH, AGCH
  - Dedicated Control Channels (DCH): SDCCH, SACCH
  - Traffic Channels (TCH): TCH/FS, TCH/F2.4, TCH/F4.8, TCH/F9.6, TCH/H4.8 and TCH/H2.4
  - Associated Control Channels (ACCH): FACCH and SACCH

- Equalization for normal and synchronization bursts
- Power measurement of serving and neighbouring cells
- Tone and side-tone generation.

2.5 kbytes of RAM are free for downloading of additional software modules e.g. rate adaptation, handsfree, voice recognition.

The DSP communicates via two serial ports to the baseband interface IC and to the IOM®-2 Interface and Voice Port for speech and data transmission. For command and data transfer it is connected to a microcontroller via its 8-bit Host Port and the 68000 compatible Host Interface. The I/O port of the DSP core provides four general purpose I/O lines. Some of the port lines are used as dedicated control signals.

The Timer and Interface functions include a GSM specific hardware timer and a couple of interface functions which simplify system design and keep the chip count to a minimum.

The Timing Generator provides the TDMA burst timing and power on/off signals for the RF transmitter, RF receiver, synthesizer, DSP and baseband interface IC. The timing signals can be programmed with an accuracy of a quarterbit ($1/500$ TDMA frame). Their output polarity is programmable.

The RF-IC Interface is used to program the RF ICs and the synthesizer. It is compatible with the Philips 'Three Wire Bus' and other standards. The bus consists of clock, data and several enable lines to transfer data between the PCF5083 and the connected devices. ICs of one family share the same enable line. Their unique address is a part of the data stream. ICs of different families use separate enable lines.

The PCF5083 includes an IOM®-2 Interface to connect external accessories e.g. a handsfree set. It may be used as a software download interface and provides access for the Digital Audio Interface during Type Approval.

The Audio Interface provides the connection between a local codec, the IOM®-2 Bus and the DSP.

The ON/OFF Logic performs the basic power-up and power-down switching function for the whole mobile. It controls the supply voltage switches for the terminal. The on/off conditions are controlled via the operators keyboard, a low voltage battery indication circuit, the Watchdog Timer or an auxiliary switch on input for general purpose use.

The man-machine interface section includes a dedicated RS232 interface and generates a 13 MHz clock for the keyboard and card reader controller. If this controller is inactive, the clock is stopped to save power. If the controller requests service, the clock is switched on again.

The PCF5083 includes a 6-bit general purpose parallel port to control system functions. One bit of the port is used on-chip to provide a reset signal for the DSP core.

The PCF5083 is accessed via its 8-bit, 68000 compatible Host Interface. Separate chip enable lines for the DSP and the Timer core are available. The DSP core provides a signal to be used as DTACK for maximum speed operation. Three interrupt lines are provided for the microcontroller.

The PCF5083 requires two clock signals. The 13 MHz main clock is used internally to generate the TDMA timing and as a reference clock for the on-chip PLL. A second clock of 32.768 kHz is used for a real time clock/calendar, a Watchdog Timer and to provide timing in a power reducing Sleep mode. During this mode TDMA timing is maintained with slow running, high accuracy counters, while all timing signals are kept inactive to save power.

The on-chip PLL generates three clocks (13, 39 and 52 MHz) which are manipulated to generate the internal DSP clock (19.5 MHz), a 19.5 MHz output (CLK20M) and a 26 MHz output (CLK26M, only version 3) used by the microcontroller and other system components. The 13 MHz PLL output is used by the Timing Generator in addition to being fed back to the PLL. The nominal duty cycle of the PLL outputs is 50%, independent of the reference clock characteristics. The PLL clock outputs may be used for all system components requiring a symmetric input clock therefore leading to reduced tolerance requirements for the duty cycle of the reference clock.

Other ICs of the Philips second generation GSM chipset are:

- P90CL301: 16-bit 68000 compatible microcontroller
- TDA8005: SIM/MMI-Controller
- PCF5072: Baseband Interface and Audio Codec
- SA1638: IF processing IC
- SA1620: RF processing IC (900 MHz)
- UMA1019: Synthesizer
- PCF5075: Power amplifier controller
- BGY20x: UHF Power Amplifier Module family.

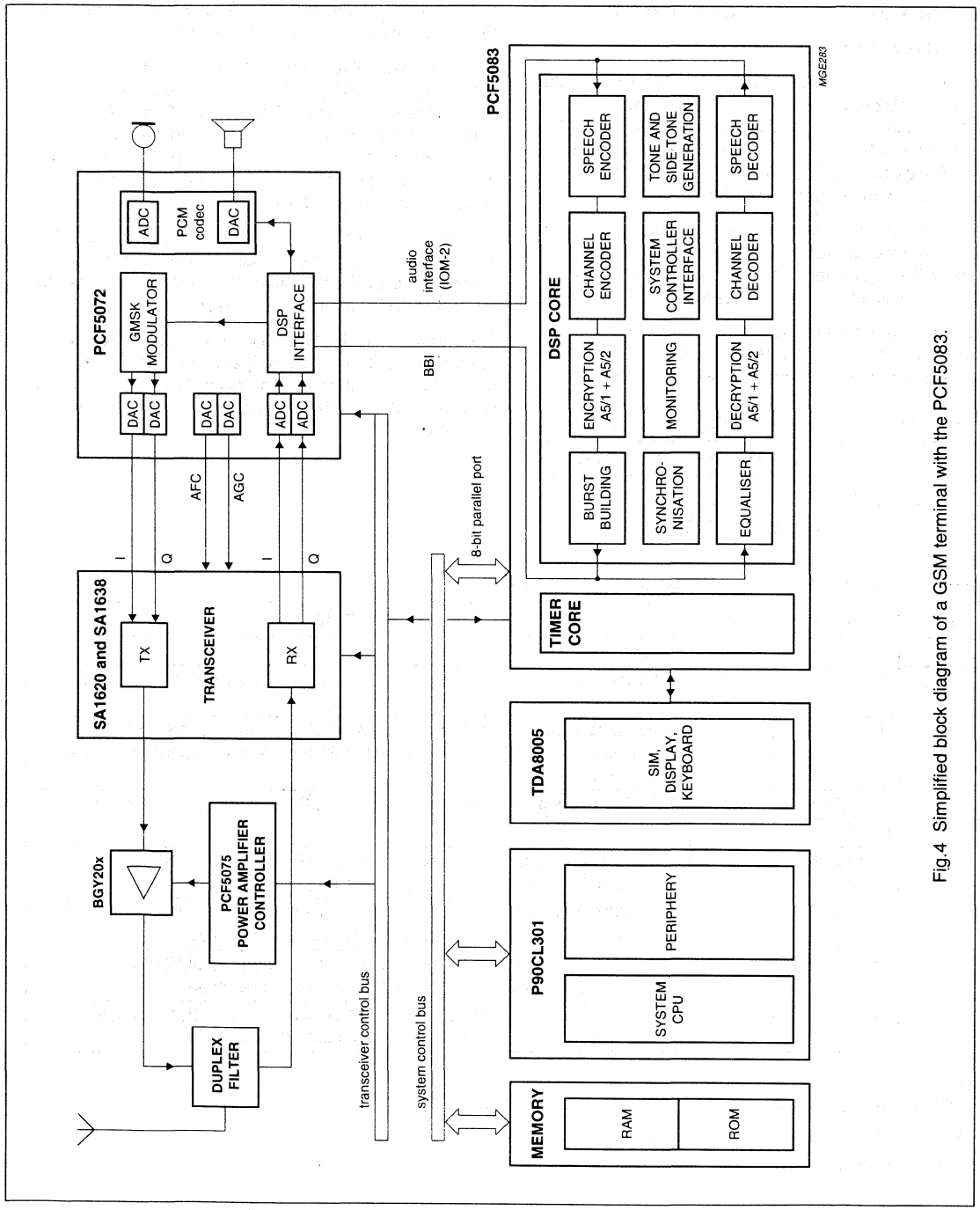


Fig.4 Simplified block diagram of a GSM terminal with the PCF5083.

8 FUNCTIONAL DESCRIPTION TIMER CORE

8.1 Clock generator

The Clock Generator consists of a low swing input buffer for the 13 MHz reference clock, a PLL as frequency multiplier and a 32.768 kHz crystal oscillator. The PLL generates 13 MHz, 39 MHz and 52 MHz from the 13 MHz reference clock. The PLL reset input $\overline{RSTP}$ is used to bring the PLL into a low-power state when set to a LOW level.

The 13 MHz reference clock is AC coupled to input CKI. CKI is a reduced swing input which requires a signal in the range of 0.7 $V_{(p-p)}$ (worst case) for operation. The clock signal is amplified and used as the input clock for the PLL.

The Timer core is either clocked with the 13 MHz reference clock or the 13 MHz PLL output. The clock source is selected with input CLKSEL as shown in Table 1.

Table 1 Timer Core clock selection

CLKSEL	TIMER CORE CLOCK
0	PLL output
1	buffered CKI input

Using the PLL output reduces the tolerance requirements for the duty cycle of the reference clock.

The DSP core will function with the 39 MHz PLL clock or the clock supplied from DCLK. The clock source is selected with the flags in SYSCON_REG; see Tables 2 and 3. Within the DSP core the selected clock is first halved before use. The 52 MHz PLL is register selectable for future applications but should not be used in the current implementation of this device

The inverting buffer stage between CLK32I and CLK32O, together with an external crystal network generates a 32.768 kHz clock for the Timer Core. This clock is used for the real time clock, the ON/OFF logic etc.

The internal 13 MHz, 19.5 MHz and 2b/2c: 32.768 kHz/ 3: 26 MHz clocks are externally available for other system components, e.g. the microcontroller. All clock outputs can be disabled if they are not used to reduce the power consumption.

Table 2 System Configuration Register (SYSCON); note 1

BIT	FLAG	R/W	DESCRIPTION
7	–	–	Reserved
6	LOCK	R	**PLL lock select.** If LOCK = 0; then PLL in lock. If LOCK = 1; then PLL out of lock.
5	RS232_CLK	W	**RS232 interface clock source.** If RS232_CLK = 0; then the 13 MHz Timer clock is used. If RS232_CLK = 1; then the RS232 clock is supplied via the ADI pin (pin 125).
4	DSP_CLK1	W	**DSP clock select.** This two bits select the DSP clock frequency; see Table 3.
3	DSP_CLK0	W	
2	CLK32K[2]	W	**CLK32K output enable/disable.** If CLK32K = 0; then the CLK32K output is enabled. If CLK32K = 1; then the CLK32K output is disabled.
	CLK26M[3]		**CLK26M output enable/disable.** If CLK26M = 0; then the CLK26M output is enabled. If CLK26M = 1; then the CLK26M output is disabled.
1	CLK20M	W	**CLK20M output enable/disable.** If CLK20M = 0; then the CLK20M output is enabled. If CLK20M = 1; then the CLK20M output is disabled.
0	CLK13M	W	**CLK13M output enable/disable.** If CLK13M = 0; then the CLK13M output is enabled. If CLK13M = 1; then the CLK13M output is disabled.

Note

1. Default value after reset 0X00 0000b (x: LOCK is undefined).
2. Versions PCF5083-2b and PCF5083-2c only.
3. PCF5083-3 only.

Table 3 Selection of the DSP clock

DSP_CLK1	DSP_CLK0	DSP CLOCK
0	0	DCLK/2
0	1	26 MHz
1	0	19.5 MHz
1	1	Reserved

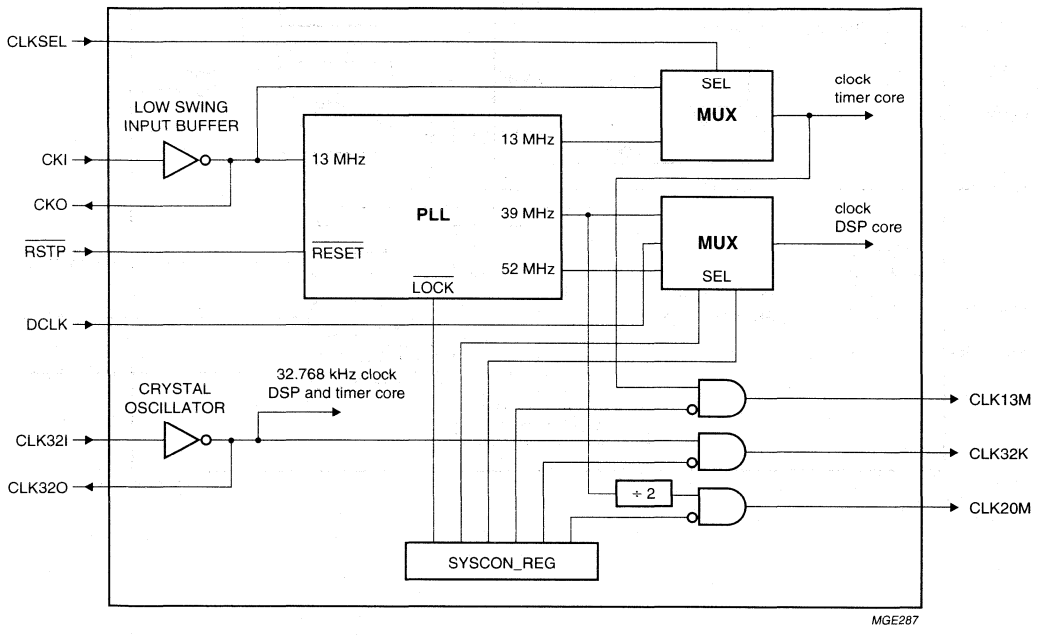


Fig.5 Clock generator block diagram.

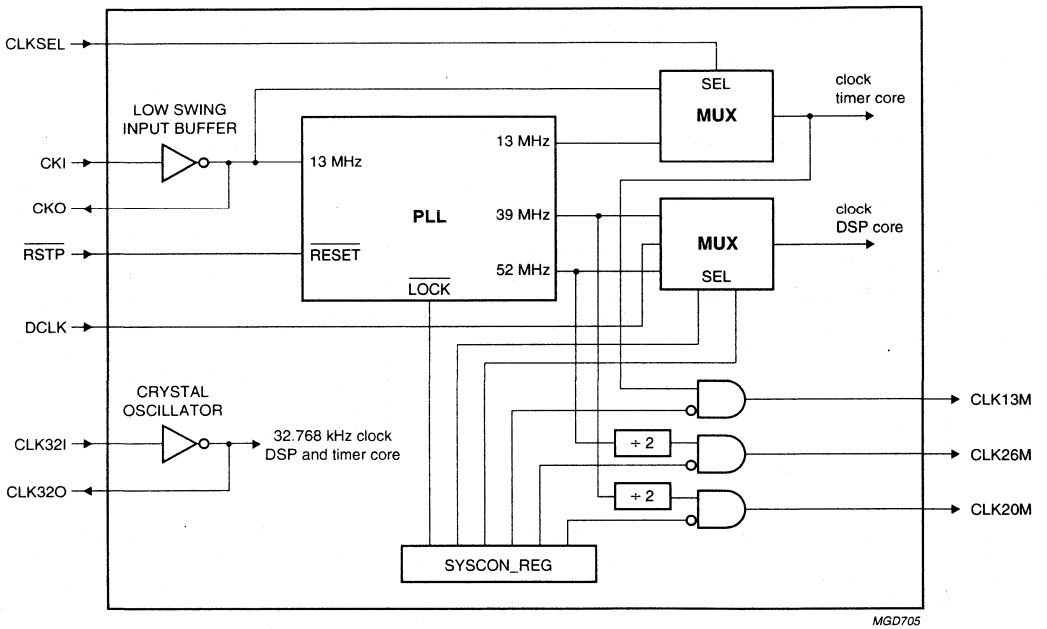


Fig.6 Clock generator block diagram.

8.2 ON/OFF Logic

The ON/OFF logic performs the main power on and off switching function for the whole mobile. The on/off conditions are controlled via an operators keyboard, a low voltage battery indication circuit, a hardware Watchdog Timer or an auxiliary switch on input for general purpose use.

The hardware control interrupt HWCTRL_INT, signalled via the $\overline{\text{COMB\_INT}}$ output (refer to Section 10.2), is used to signal the status of the ON/OFF Logic. The inputs DSPEN and TIMEN are used to control the Watchdog function. $\overline{\text{RST}}$ and $\overline{\text{RSTO}}$ are asynchronous reset lines. The inputs ONKEY, AUXON and $\overline{\text{LOWVOLT}}$ are debounced with a time constant of 62.5 ms. The minimum pulse width for the safe detection of a signal transition is therefore $2 \times 62.5 = 125$ ms on any of these lines. The ON/OFF Logic signals are specified in Table 4.

Table 4 ON/OFF Logic signals

SIGNAL	DESCRIPTION
ONKEY	Input (active HIGH) to be connected to the ON/OFF switch of the operators keyboard.
AUXON	Input (edge sensitive) for general purpose use, e.g. used as battery charger connect indication or ignition sense in mobile applications.
$\overline{\text{LOWVOLT}}$	Input (active LOW) to be connected to an external low battery indication circuit.
POWON	Output (active HIGH) to be connected to the ON terminal of the supply voltage switch.
NPOWON	Inverted output signal of POWON.

8.2.1 Mobile switch-on procedure

Switching on the mobile is initiated via the PCF5083 according to Table 5.

If one of the three conditions ONKEY, AUXON or Alarm time match become true, a corresponding flag is set in register HWCTRL_REG. As soon as one of these flags is set, signal POWON is set and NPOWON is reset. At the same time the HWCTRL_INT interrupt is activated. The interrupt condition is signalled via the $\overline{\text{COMB\_INT}}$ line to the System Controller if the relevant bit is set in the COMBINT_REG register (refer to Section 10.2).

The hardware reset $\overline{\text{RST}}$ clears the enable bits for the $\overline{\text{COMB\_INT}}$ interrupt lines.

The interrupt flags in register HWCTRL_REG must be cleared by the System Controller to deactivate the interrupt condition. A flag is cleared by writing a logic 1 to its bit location.

The POWON output is the main power control signal. As soon as POWON goes HIGH, all ICs in the mobile are powered via the supply voltage switch. The $\overline{\text{LOWVOLT}}$ input asserted LOW, indicating a low voltage situation, or $\overline{\text{RSTO}}$ asserted LOW inhibits the mobile to be switched on.

If the PCF5083 was switched on via AUXON (HWCTRL_REG[AUXON_LH] = 1) and the AUXON signal remains HIGH, the flag HWCTRL_REG[AUXON_LH] must be cleared, before the PCF5083 enters the Power-down mode.

Table 5 Mobile switch-on conditions

$\overline{\text{RST0}}$	$\overline{\text{LOWVOLT}}$	ONKEY	AUXON	ALARM TIME MATCHES CURRENT TIME	POWON	$\overline{\text{COMB\_INT}}$
L	X	X	X	X	L	3-state
H	L	X	X	X	L	3-state
H	H	L → H	X	X	L → H	H → L
H	H	X	L → H	X	L → H	H → L
H	H	X	X	yes	L → H	H → L

8.2.2 MOBILE SWITCH-OFF PROCEDURE

The switch-off request to the System Controller is initiated via a LOW-to-HIGH transition and hold of pin ONKEY for longer than 1 second or a LOW level on pin $\overline{\text{LOWVOLT}}$. The HWCTRL_INT interrupt is activated if one of these conditions has set it's corresponding flag in register HWCTRL_REG.

The next step is to deactivate the POWON signal. Therefore the flag HWCTRL_REG[SWOFF] has to be set. If the SWOFF flag is not set within 8 seconds (see Section 8.2.3) and the Watchdog Timer expires, POWON is deactivated without any further interaction. The SWOFF flag is automatically cleared when the mobile is switched on again.

The PCF5083 is immediately and under all conditions forced into the off state with $\overline{\text{RSTO}}$ asserted LOW.

Table 6 Mobile switch-off request conditions

ONKEY	$\overline{\text{LOWVOLT}}$	$\overline{\text{COMB\_INT}}$
H	H	H
L → H	X	H → L
X	H → L	H → L

It should be noted that:

- If POWON is LOW (switch-off state), all outputs of the PCF5083 except POWON and NPOWON are in their high-impedance state.
- The hardware control interrupt (HWCTRL_INT) is not asserted externally but stays internally pending during Sleep mode. The timing generator unit is forced into wake-up state if the hardware control interrupt is asserted internally.
- Other interrupt conditions, caused by the MMI power-down unit and the real time clock unit, are also indicated with the hardware control interrupt. These conditions are mentioned in the appropriate sections.
- The interrupt flags in register HWCTRL_REG have to be cleared by the System Controller to deactivate the interrupt condition. A flag is cleared by writing a logic 1 to its bit location.

Table 7 Mobile switch-off conditions

HWCTRL_REG[SWOFF]	OFF/WATCHDOG TIMER EXPIRES	$\overline{\text{RSTO}}$	POWON
L	no	H	H
L → H	no	H	H → L
L	yes	H	H → L
X	X	L	H → L

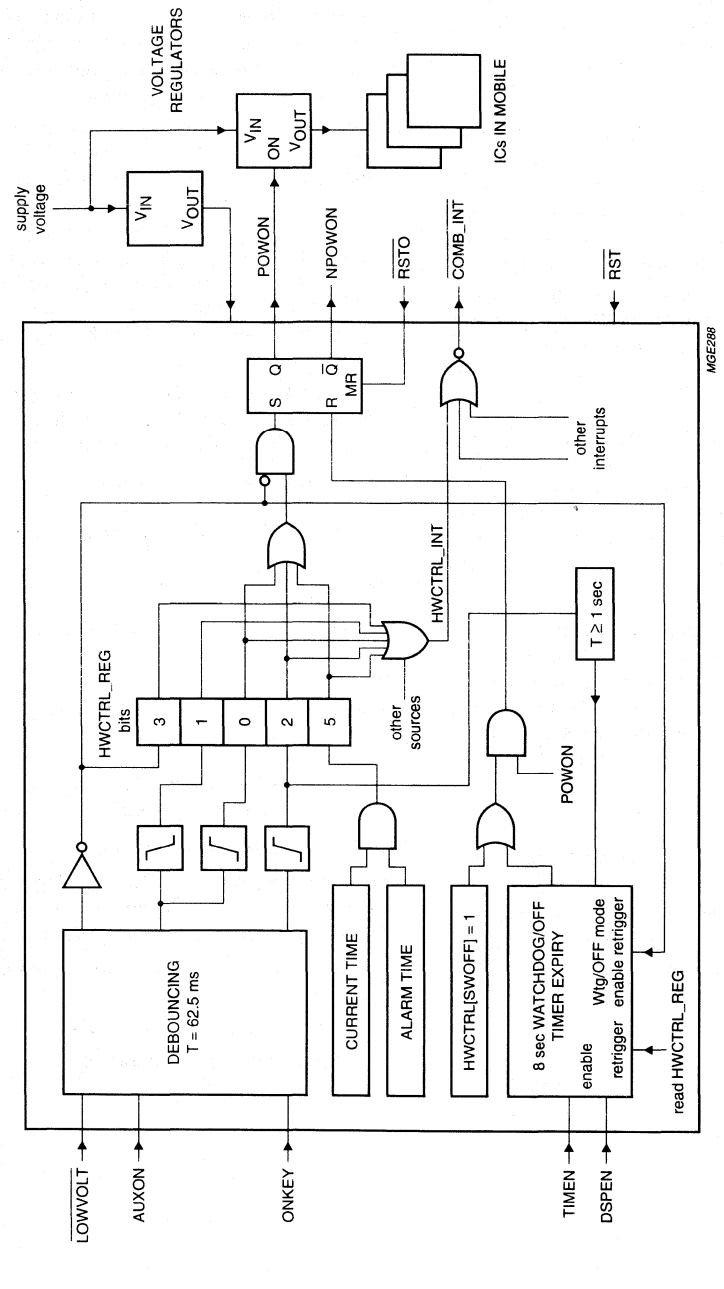


Fig.7 ON/OFF logic functional diagram.

8.2.3 OFF TIMER AND WATCHDOG TIMER

The hardware switch-off and Watchdog Timer are used to power-down the mobile if the System Controller has lost control for more than 8 seconds.

8.2.3.1 Watchdog Timer

After the reset signal $\overline{RST}$ is deactivated, the Watchdog Timer starts to count. If the timer expires after 8 seconds, the POWON output is set LOW. To prevent this occurring, the System Controller must restart the timer periodically, reading register HWCTRL_REG within 8 seconds after the previous read operation. The Watchdog function is enabled if DSPEN = TIMEN = LOW. The configuration DSPEN = TIMEN = HIGH disables the Watchdog Timer. All other settings are for debugging purposes.

8.2.3.2 OFF Timer

After the switch-off request (HWCTRL_INT activated via $\overline{LOWVOLT}$ or ONKEY conditions), the OFF-Timer starts to count. If the timer expires after 8 seconds, or if the System Controller sets HWCTRL_REG[SWOFF] to a logic 1, the POWON output is set LOW. The OFF-Timer cannot be restarted with a read access to register HWCTRL_REG.

For some special purposes, e.g. if the battery charging control is handled from the System Controller, the OFF-Timer can be stopped after it was activated from ONKEY or $\overline{LOWVOLT}$. It then resumes its watchdog function. The OFF-Timer is stopped with a write access to register STOP_REG. The data value written to this register has to be A5H. Other data values do not stop the OFF-Timer.

It should be noted that:

- The OFF/Watchdog Timer is not restarted after a stop operation
- If either the ONKEY or $\overline{LOWVOLT}$ line stays active after a stop operation, it is again recognized after its 1 second switch-off time-out or 62.5 ms debouncing period, respectively.

8.3 Timing Generator

The Timing Generator provides TDMA timing and power-down signals for the RF transmitter, RF receiver, synthesizer and baseband interface IC.

The Timing Generator has three modes of operation to control the mobile:

1. **Normal mode:** in this mode the mobile is fully active. All ICs receive their operating voltage, the power consumption is reduced by switching the ICs on and off with their power-down inputs.
2. **Sleep or Idle mode:** in this mode the mobile is switched on, but no call is active. The mobile will be fully activated if a mobile originated call is requested via the keyboard. Otherwise parts of the mobile are activated from time to time to monitor incoming calls. Outside these intervals all ICs can be switched off under control of the PCF5083. In this mode the main 13 MHz clock is switched off. To maintain TDMA timing alignment, the PCF5083 is running temporarily on a slower clock frequency.
3. **Reduced Sleep mode:** this mode is equal to the Sleep mode, except that the TDMA timing alignment is maintained by the main 13 MHz clock.

In this chapter the following definitions are used:

- 1 bit (Bit) = $48 \times \frac{1}{13000000}$ s = 3.692 µs ($\frac{1}{1250}$ TDMA frame)
- 1 quarterbit (QB) = $\frac{1}{4}$ Bit = 0.923 µs ($\frac{1}{5000}$ TDMA frame)
- 1 timeslot (TS) = 625 QB = 0.576 ms ($\frac{1}{8}$ TDMA frame)
- 1 Burst = 1 TS

The term frame refers to a TDMA frame throughout this section unless otherwise stated.

The Timing Generator consists of:

- The quarterbit counter (QBC) counting 5000 quarterbit steps in one TDMA frame and running on 1.0833 MHz. This clock is switched off during Sleep mode.
- The Timing Generator (TG) with output polarity and mask registers.
- The sleep quarterbit counter (SQBC).
- The Sleep mode timing generator.

8.3.1 THE QUARTERBIT COUNTER

The quarterbit counter (QBC) represents the timebase of the mobile. It consists of a 13-bit upcounter. The counter directly counts the quarterbit steps within one TDMA frame. Its range is therefore 0 to 4999.

At the beginning of every TDMA frame (quarterbit counter state 0) the signal $\overline{\text{FRAME\_INT}}$ goes LOW, generating an interrupt (frame interrupt) to the System Controller. The interrupt line is deactivated by accessing the register MODE0_REG. The frame interrupt is disabled with MODEx_REG[DISFRAMEINT] = 1.

8.3.1.1 Initial Quarterbit Counter Timing Alignment

The timing offset between a base station and a mobile station can be corrected by presetting the quarterbit counter with an estimated correction value. Therefore the register QBC_REG has to be set up with this correction value in frame N and the flag QBRCTRL_REG[SYNC] has to be set.

At the end of frame N the quarterbit counter is loaded from QBC_REG with zeros. The duration of frame N + 1 is 5000 – [QBC_REG] and the mobile will be synchronised at the beginning of frame N + 2. The frame interrupt at the beginning of frame N + 1 is disabled. The timing generation is disabled during frame N + 1. The SYNC flag is cleared after synchronization.

For the System Controller the resulting timing looks like frame N being extended and synchronization being achieved with frame N + 1.

8.3.1.2 Maintaining the Quarterbit Counter Timing Alignment

Small timing corrections can be made by inserting or extracting one quarterbit step at the beginning of a TDMA frame. Therefore the INSERT or EXTRACT flag in register QBCCTRL_REG have to be set. These flags are cleared after the timing alignment was performed.

8.3.2 NORMAL MODE

In Normal mode the Timing Generator provides the output signals specified in Table 8.

The power-down signals NPDTX2, NPDTX1 and NPDBIAS are active LOW by default. All other signals are active HIGH by default. Active HIGH in this context means that the signals are on high level during a receive or a transmit burst.

The output polarity can be changed by setting the corresponding bit in register POL_REG to a logic 1. The signals can be clamped to a level depending on their flag in POL_REG by setting the corresponding bit in register MASK_REG to a logic 0.

After a reset with $\overline{\text{RST}}$, the receiver, transmitter and synthesizer control lines are set to their inactive level.

The general MS timing is assumed to have the receive timeslot (RX) in timeslot 0, the transmit timeslot (TX) in timeslot 3 and the monitor timeslot (MON) in timeslot 6 within a TDMA frame.

Table 8 Output signals

SIGNAL	DESCRIPTION
Signals for the receiver section	
RXON	baseband interface IC receiver enable
BEN	baseband interface IC enable
PDRX1	receiver power-down 1
PDRX2	receiver power-down 2
Signals for the transmitter section	
TXON	baseband interface IC transmitter enable
BEN	baseband interface IC enable
TXKEY1	power amplifier power-down
TXKEY2	power ramping controller trigger signal
PDTX1	transmitter power-down 1
NPDTX1	inverted output of PDTX1
NPDTX2	transmitter power-down 2
PDPIAS	power amplifier bias voltage power-down
NPDBIAS	inverted output of PDBIAS
Signal for the synthesizer	
PDSYN	synthesizer power-down

8.3.2.1 Receiver Timing

The Receiver Timing is characterized in Table 9. The start and duration times are defined by loading the mentioned registers.

Table 9 Receiver Timing (note 1)

BURST TYPE SIGNAL	START (QB)[2]	DURATION (BIT)
Rx burst[3][4]		
RXON	RXSTART_REG + 929 = (0 to 127) + 929	RXLENGTHx_REG = (1 to 255)
BEN	RXSTART_REG + 928 = (0 to 127) + 928	RXLENGTHx_REG + 4 = (1 to 255) + 4
PDRX1[5]	RXSTART_REG + 1024 − PDRX1_REG × 32 = (0 to 127) + 1024 − (0 to 31) × 32	to end of RXON
PDRX2	RXSTART_REG + 1024 − PDRX2_REG × 32 = (0 to 127) + 1024 − (0 to 31) × 32	to end of RXON
PDSYN	RXSTART_REG + 1024 − PDSYN_REG × 32 = (0 to 127) + 1024 − (0 to 31) × 32	to end of RXON
MON burst[6][7][8]		
RXON	MONSTART_REG + 929 = (0 to 4999) + 929	RXLENGTHx_REG = (1 to 255)
BEN	MONSTART_REG + 928 = (0 to 4999) + 928	RXLENGTHx_REG + 4 = (1 to 255) + 4
PDRX1[5]	MONSTART_REG + 1024 − PDRX1_REG × 32 = (0 to 4999) + 1024 − (0 to 31) × 32	to end of RXON
PDRX2	MONSTART_REG + 1024 − PDRX2_REG × 32 = (0 to 4999) + 1024 − (0 to 31) × 32	to end of RXON
PDSYN	MONSTART_REG + 1024 − PDSYN_REG × 32 = (0 to 4999) + 1024 − (0 to 31) × 32	to end of RXON

Notes

1. A minimum delay of 948 quarterbit periods must be programmed between the end of a monitor burst and the start of the next monitor burst, measured from the falling edge of RXON to the next rising edge of RXON.
2. If (MONSTART_REG + 929) > 5000 then the monitor burst ends in the next TDMA timeslot at (MONSTART_REG + 929) − 5000.
3. MODEx_REG[RECRX] enable the generation of Rx burst timing.
4. RXBURSTx_REG (x = 0 to 2) is selected with 2 flags in register MODEx_REG.
5. PDRX1 is not activated during a monitor burst if the MODEx_REG[RXCAL] flag is set.
6. For the three level measurement mode, a second monitor burst can be generated during the TX timeslot. The start position of this burst is then controlled with register TXSTART_REG. Its duration is given from the same register as for the actual monitor burst.
7. If (MONSTART_REG + 929 +RXBURSTx_REG) > 5000 then the monitor burst ends in the next TDMA timeslot at (MONSTART_REG + 929 + RXBURSTx_REG) − 5000.
8. MODEx_REG[RECMON] enable/disable the generation of monitor burst timing.

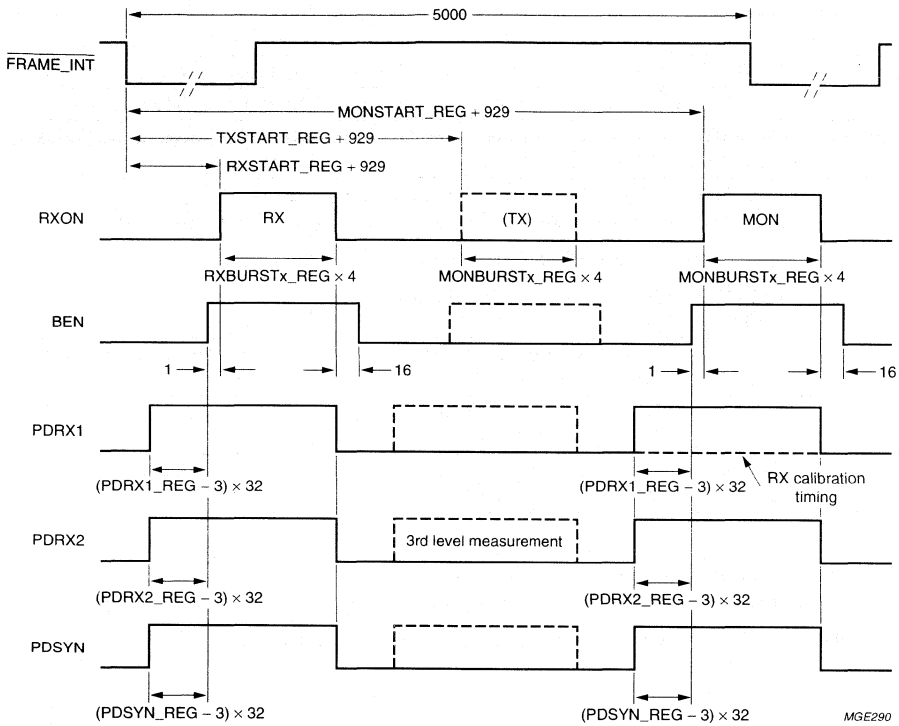


Fig.8 Receiver timing.

8.3.2.2 Transmitter Timing

The transmitter timing is shown in Table 10. The start and duration times are defined by loading the named registers.

Table 10 Transmitter Timing

BURST TYPE SIGNAL	START (QB)[1]	DURATION (QB)[2]
TX burst		
TXON	TXSTART_REG + 929 = (0 to 2047) + 929	TXLENGTHx_REG = (1 to 255)
BEN	TXSTART_REG + 928 = (0 to 2047) + 928	to end of TXON + 16
(N)PDTX1,2	TXSTART_REG + 1024 − PDRX1,2_REG × 32 = (0 to 2047) + 1024 − (0 to 31) × 32	to end of TXKEY + PDDELAY_REG (1 to 63)
(N)PDBIAS	TXSTART_REG + 1024 − PDBIAS_REG × 32 = (0 to 2047) + 1024 − (0 to 31) × 32 or if PDBIAS_REG < PDTX1_REG + 4 (note 3): TXSTART_REG + 1024 − (PDTX1_REG + 4) × 32 = (0 to 2047) + 1024 − (0 to 31) × 32	to end of TXKEY + PDDELAY_REG + 32 (1 to 63)
TXKEY1	TXSTART_REG + 929 + KEYON1_REG = (0 to 2047) + 929 + (1 to 511) × 32	TXKEYx_REG = (1 to 1023)
TXKEY2	TXSTART_REG + 929 + KEYON2_REG = (0 to 2047) + 929 + (1 to 511) × 32	to end of TXKEYx + KEYOFF_REG (1 to 63)
PDSYN	TXSTART_REG + 1024 − PDSYN_REG × 32 = (0 to 2047) + 1024 − (1 to 31) × 32	to end of TXKEYx + PDDELAY_REG (1 to 63)

Notes

1. The timing advance is adjusted with the value of TXSTART_REG.
2. TXBURSTx_REG and TXKEYx_REG (x = 0 or 1) is selected with a flag in register MODEx_REG.
3. Therefore (N)PDBIAS will always be active at least 4 × 32 QB prior to PDTX1.

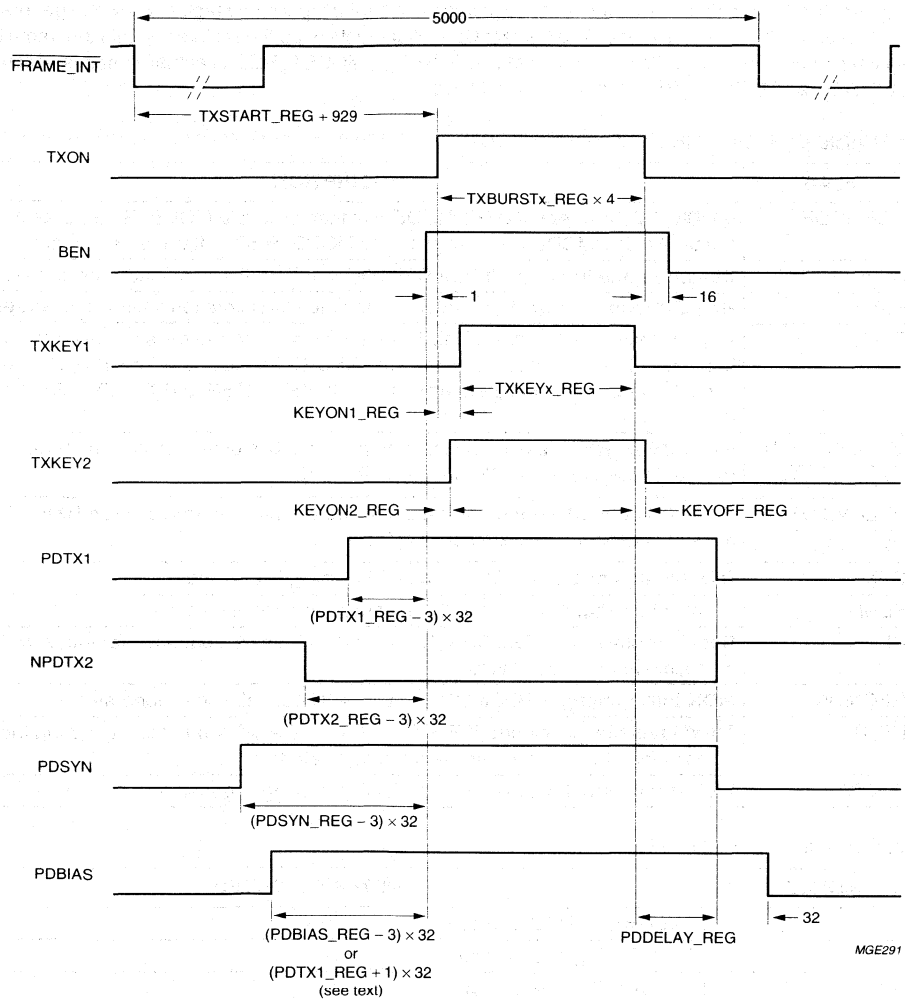


Fig.9 Transmit burst timing.

8.3.2.3 Timing Generation

To generate all burst types required to fulfil the GSM timing, it is necessary to combine and/or modify the basic receive and transmit burst sequences. For this purpose two registers MODE0_REG and MODE1_REG exist, containing some flags to control the burst timing. Both mode registers and the registers RXSTART_REG, TXSTART_REG and MONSTART_REG have an additional pipeline stage.The first register stage can be read or written by the SC.

The second stage is used for timing generation. The pipelining operation is performed at QBC = 0 (together with the frame interrupt generation). Some flags inside the mode registers have a third pipelining stage to allow the generation of a MON burst which overlaps into the next frame. The System Controller must set up the registers within the frame before the programmed timing becomes active. Which register MODE0_REG or MODE1_REG is actually used is described in Table 11. MODE0_REG and MODE1_REG contain identical flags.

Table 11 Mode Registers (MODE0_REG and MODE1_REG)

BIT	FLAG	DESCRIPTION
13	USEMODE	**MODE_REGx select.** If USERMODE = 0; then switch to MODE_REG0 after the next frame. If USERMODE = 1; then switch to MODE_REG1 after the next frame.
12	DISFRAMENT	**Disable frame interrupt.** If DISFRAMENT = 1; then the frame interrupt is disabled.
11	RXCAL	**RX calibration timing.** If RXCAL = 1; then the RX calibration timing is generated.
10	TXLENGTH	**Register select.** The state of this bit determines which registers are used for the TX burst. If TXLENGTH = 0; then registers TXBURST0_REG and TXKEY0_REG are used. If TXLENGTH = 1; then registers TXBURST1_REG and TXKEY1_REG are used.
9	MONLENGTH1	**RXBURSTx_REG select.** The state of these two bits determine which RXBURST register is used for the MON burst; see Table 12.
8	MONLENGTH0	
7	RXLENGTH1	**RXBURSTx_REG select.** The state of these two bits determine which RXBURST register is used for the Rx burst; see Table 13.
6	RXLENGTH0	
5	DTX	**DTX timing enable.** If DTX = 1; then DTX timing is enabled.
4	SEND	**TX burst timing.** If SEND = 1; the TX burst timing is generated.
3	RECON	**Receiver start-up.** If RECON = 1, the receiver start-up sequence for the MON burst in the idle frame is generated.
2	RECMON	**MON burst timing.** If RECMON = 1; the MON burst timing is generated.
1	RECTX	**Third level measurement.** If RECTX = 1; then the MON burst timing during the TX timeslot for a third level measurements generated.
0	RECRX	**Rx burst timing.** If RECRX = 1; the Rx burst timing is generated.

Table 12 Register selection for the MON burst

MONLENGTH1	MONLENGTH0	REGISTER SELECTED
0	0	RXBURST0_REG is used.
0	1	RXBURST1_REG is used.
1	0	RXBURST2_REG is used.
1	1	Undefined during a MON burst.

Table 13 Register selection for the Rx burst

RXLENGTH1	RXLENGTH0	REGISTER SELECTED
0	0	RXBURST0_REG is used.
0	1	RXBURST1_REG is used.
1	0	RXBURST2_REG is used.
1	1	Undefined during a RX burst.

8.3.2.4 MON burst during idle frame

This burst is a special case of the MON burst. It is used for FCB search and for monitoring during the idle frame. If RECON is set, a timing equivalent to the MON burst timing is generated, with the exception that all output lines (BEN, RXON, PDRXx etc.) are kept active at the end of the burst. The output lines are set inactive again during the first frame with RECMON set at the time, they normally would be deactivated at the end of a MON burst. During the frames in between, either RECON = 1, or RECRX = RECTX = RECMON = RECON = SEND = 0 must be programmed.

8.3.2.5 Register mode switching

Which of the registers MODE0_REG or MODE1_REG is used for timing generation is determined using the following two rules:

1. After any write access to MODE0_REG, MODE0_REG is active during the next frame.
2. After every frame the USEMODE flag of the currently active register determines which register is used during the next frame, unless there was a write access to MODE0_REG during the current frame.
   e.g. MODE0_REG: USEMODE = 1 and MODE1_REG: USEMODE = 0 is programmed during frame N.

   This causes the following timing:

   a) MODE0_REG is active during frame N + 1
   b) MODE1_REG is active during frame N + 2
   c) MODE0_REG is active during frame N + 3 and so on, until MODE0_REG is being written again.

8.3.2.6 DTX Mode Processing

DTX mode (Discontinuous Transmission) is enabled with MODEx_REG[DTX] = 1. In DTX mode, the DSP makes the decision whether a TX burst should be generated or not. The DTX condition is signalled via IO4 (generate transmit burst: IO4 = 0, no transmit burst: IO4 = 1). If no TX burst is to be generated, the power-down lines TXKEY1/2, (N)PDTX1/2 and PDSYN are kept inactive or if already asserted, they are set inactive again. (N)PDBIAS become inactive with their default delay of 8 bit after (N)PDTX1/2 respective PDSYN if they were already asserted, otherwise they also remain inactive. TXON and BEN are not affected from DTX mode.

8.3.2.7 Interface to the RF-IC Bus

The Timing Generator provides trigger signals for the frequency and gain control channels of the RF-IC interface when the quarterbit counter matches either RXSTART_REG, TXSTART_REG or MONSTART_REG. Further trigger signals are generated for the gain control channel after every receive burst to send the contents of register DACOFF_REG and prior to a receive burst if the quarterbit counter matches xxSTART_REG + 1024 − AGCSTART_REG × 32 (xx = RX, TX or MON) to send the contents of register DACON_REG (refer to Section 8.4).

Note, if the generation of a trigger signal falls into an active burst, the trigger signal is delayed until the end of the current burst.

8.3.2.8 Timing modes Application Examples

Table 14 Timing mode applications

FRAME	4	3	2	1	0	BIT ASSIGNMENT; REGISTER MODE_REG
	SEND	RECON	RECMON	RECTX	RECRX	ACTION
						BCCH Detection
N	0	1	0	0	0	Receiver on at the start of timeslot 0 (MONSTART_REG = 0) in TDMA frame N + 1. Receiver on.
N + 1 to N + M	0	0	0	0	0	Keep receiver on.
N + 1 + M	0	0	1	0	0	Receiver off after number of samples defined by MONSTART_REG, RXLENGTHx_REG and number of TDMA frames M.
						Frequency Estimation
X	0	0	0	0	1	Receive during TS0.
						Frame with RX, TX, MON
X	1	0	1	0	1	Receive during RX, MON, transmit during TX.
						Frame before idle frame (monitoring)
I-1	1	1	0	0	1	Receive during RX, transmit during TX, receiver on defined by MONSTART_REG.
						Idle frame (monitoring)
I	0	0	1	0	0	Receiver off defined by MONSTART_REG and RXLENGTHx_REG.
						Frame with RX, TX, MON
I-1	1	0	1	0	1	Receive during RX, MON, transmit during T.
or[1]						
I-1	1	0	0	0	1	Receive during RX, transmit during TX.
						Idle frame (SYNC burst reading)
I	0	0	0	0	0	No operation.
or[1]						
I	0	0	1	0	0	Receive during MON.
						Three level measurements
X	0	0	1	1	1	Receive during RX, TX and MON slot.
						Send access burst
X	1	0	0	0	0	Transmit during TX.

Note

1. The SYNC burst location is defined by MONSTART_REG. If a timing is required with s = MONSTART_REG ≥ 5000, MONSTART_REG is programmed with s mod 5000 and the second alternative is used.

During the three level measurement mode the burst length of the receive burst during the TX slot is defined by the same register RXBURSTx_REG as used for the MON burst. The receive frequency must be set by programming the TX channel of the RF_IC interface.

For a certain operation mode in frame N, the Timing Generator has to be programmed with all necessary parameters in frame N – 1. For this purpose the registers RXSTART_REG, TXSTART_REG, MONSTART_REG and MODEx_REG have an additional pipelining stage. The pipelining takes place at the beginning of every TDMA frame with the frame interrupt generation.

8.3.3 SLEEP MODE

The Sleep mode circuitry is used to reduce the power consumption during the Idle mode. During Sleep mode, the mobile is switched on, but no call is active. The mobile is only activated to read the paging blocks and for neighbour cell monitoring. Outside these intervals, all ICs can be switched off to save power.

In this mode also the main 13 MHz oscillator may be switched off. To maintain TDMA timing alignment, the PCF5083 is running temporarily on a slower clock frequency, derived from the 32.768 kHz real time clock oscillator. This clock is called Sleep Clock (SLCLK). During the Sleep mode the PCF5083 controls the signals specified in Table 15, the timing for these signals is detailed in Table 16.

Sleep mode is activated with QBCCTRL_REG[SLEEP] = 1 and QBCCTRL_REG[SLEEPRED] = 0 (the SLEEPRED flag is used for reduced Sleep mode, see below). The register SLEEPCNT_REG has to be programmed with the number of TDMA frames the mobile wants to sleep minus one. Register FRAMECNT_REG is automatically cleared when the Sleep mode is entered and counts the number of TDMA frames actually slept. The 9-bit registers SLEEPCNT_REG and FRAMECNT_REG allow a maximum Sleep mode period of 512 frames. Refer to Fig.11 for the signal flow.

Table 15 Signals controlled by the PCF5083 during Sleep mode

SIGNAL	DESCRIPTION
REFON	Reference oscillator on. Active HIGH output.
NREFON	Inverted REFON output.
DSPON	DSP power-down (connected on chip).
GPON1	General purpose power-down and radio part interface 3-state enable. Active HIGH output.
GPON2	General purpose power-down. Active HIGH output.

Table 16 Sleep mode signal timing

SIGNAL	FRAME NUMBER	ACTIVATION OF SIGNAL IF SLEEPCNT_REG EQUALS
(N)REFON	In frame N + 1 on the third positive SLCLK edge	REFON_REG (notes 1 and 2)
DSPON	In frame N + 1 on the second positive SLCLK edge	KISSON_REG (note 2)
GPON1	In frame N + 1 on the second positive SLCLK edge	GPON1_REG (note 2)
GPON2	In frame N + 1 on the third positive SLCLK edge	GPON2_REG (note 2)

Notes

1. (N)REFON is not deactivated if the Sleep mode is initiated while the sleep clock calibration procedure is running (see Section 8.3.3.3), while the IOM®-2 interface is enabled or the MMICLK flag in register HWCTRL_REG is set, indicating that the MMI controller requires the 13 MHz clock.
2. Maximum 295 ms before Sleep mode terminates with 4.6 ms resolution {[(0 to 63) + 1] × 4.6 ms}.

A power-down line is only deactivated during Sleep mode if the corresponding activation register is programmed with a higher value than register SLEEPCNT_REG. Otherwise the power-down line stays active during Sleep mode. The output polarity of the power-down lines can be changed by setting their corresponding bit in register POL_REG to a logic 1. The signals can be clamped to a level depending on their flag in POL_REG by setting the corresponding bit in register MASK_REG to a logic 0.

Because the 13 MHz clock is also internally disabled during Sleep mode, the PCF5083 cannot be accessed with the host port.

During Sleep mode, burst timing and frame interrupt generation is stopped and the registers MODE0_REG and MODE1_REG are cleared.

8.3.3.1 Transceiver control lines

The timing generator signals RXON, TXON, BEN, PDRX1, PDRX2, PDTX1, NPDTX1, NPDTX2, PDBIAS, NPDBIAS, PDSYN, TXKEY1, TXKEY2 and the RF device control bus signals RFCLK, RFDO, RFEN1 to RFEN4, RFE and the Voice Port signals ASF, ACLK and ADO are 3-stated as long as the signal GPON1 is inactive during Sleep mode.

The signals are driven into their high-impedance state independently of the actual polarity to which GPON1 is programmed, unless MASK_REG[GPON1] = 0. In this case the outputs are driven during Sleep mode.

8.3.3.2 The Sleep Quarterbit Counter

In Sleep mode, the 13 MHz reference oscillator is switched off to reduce the power consumption. The TDMA timing is maintained using the sleep quarterbit counter (SQBC), which is driven from the sleep clock (SLCLK). The sleep clock is derived from the 32.768 kHz real time clock. Upon entering Sleep mode, the contents of the quarterbit counter are copied to the sleep quarterbit counter. After the end of a Sleep mode period, the sleep quarterbit counter is copied back to the quarterbit counter and normal timing is performed again.

To maintain the correct timing over hundreds of TDMA frames, the sleep quarterbit counter is incremented with the value SQBC_INC equal to the clock ratio between the quarterbit clock and the sleep clock. This value must be very accurate and can be derived using the calibration method described in Section 8.3.3.3.

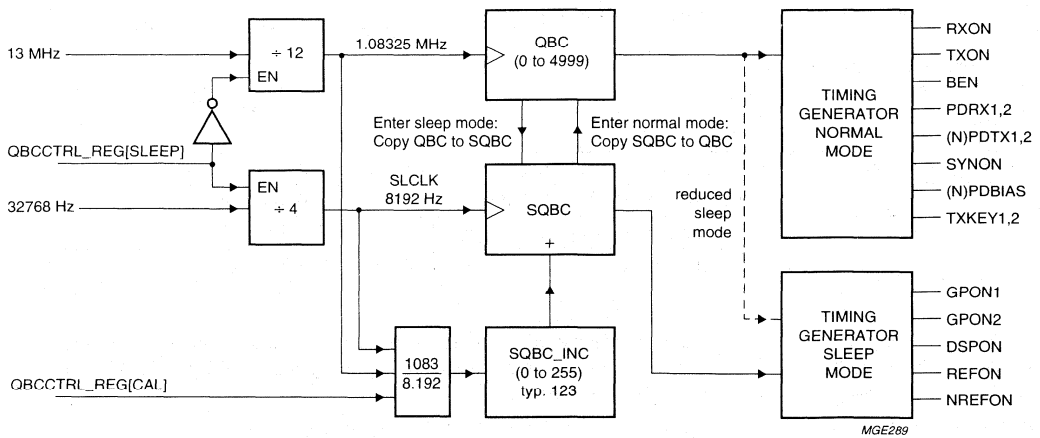


Fig.10 Quarterbit counters for normal and Sleep mode.

8.3.3.3 *Sleep Clock Calibration*

Since the ratio between the quarterbit clock and the sleep clock may vary, an accurate value for the increment SQBC_INC can be obtained with the following procedure:

1. Set QBCCTRL_REG[CAL] = 1 to enable the calibration mode.
2. The calibration procedure lasts for 8 seconds.
3. After calibration, the CAL flag in QBCCTRL_REG is automatically cleared. After 1 ms the register SQBCINC_REG holds the lower 8 bits of the increment value and can be used to verify the calibration process. The maximum allowed frequency deviation is −23.8 kHz to +25.4 kHz at 13 MHz and −63.6 Hz to +60.3 Hz at 32.768 kHz.

During the calibration procedure, the 13 MHz master clock may not be switched off. Therefore, REFON stays active even if the Sleep mode is enabled.

The calibration procedure has to be repeated from time to time, because the exact frequency of the 13 MHz as well as the 32 kHz clock may change.

After power up, the calibration procedure must be performed before the Sleep mode can be activated.

8.3.3.4 *Reduced Sleep mode*

During reduced Sleep mode the mobile timing is maintained with the quarterbit counter. The sleep quarterbit counter is not used. For the System Controller all timings are as in Sleep mode. The signal REFON is always active. All other Sleep mode signals (GPON1 etc.) are activated as during Sleep mode. The reduced Sleep mode is invoked with QBCCTRL_REG[SLEEP] = 1 and QBCCTRL_REG[SLEEPRED] = 1.

8.3.3.5 *From Sleep mode to Normal mode*

The PCF5083 is forced into a wake-up state if the hardware control interrupt HWCTRL_INT is asserted internally (caused by the ON/OFF monitor, MMI power-down unit or real time clock). The interrupt line $\overline{\text{COMB\_INT}}$ is not asserted but the interrupt stays pending internally until Sleep mode is finished.

If the PCF5083 enters the wake-up state and SLEEPCNT_REG is less than or equal to REFON_REG, the Sleep mode terminates normally. Otherwise, if SLEEPCNT_REG is greater than REFON_REG, REFON_REG is copied to SLEEPCNT_REG instead of SLEEPCNT_REG being decremented at the next frame boundary and the Sleep mode terminates with reduced duration. The maximum delay from any wake-up request to the end of the wake-up procedure depends on the setting of REFON_REG and is 64 × 4.6 ms = 294.4 ms.

After entering the normal mode again FRAMECNT_REG shows the number of actually slept frames. If the Sleep mode terminated normally, this number equals the number SLEEPCNT_REG previously was programmed with.

The System Controller now has to set up the timing generator mode for the next frame. With the beginning of the next frame the PCF5083 enters the normal operation again.

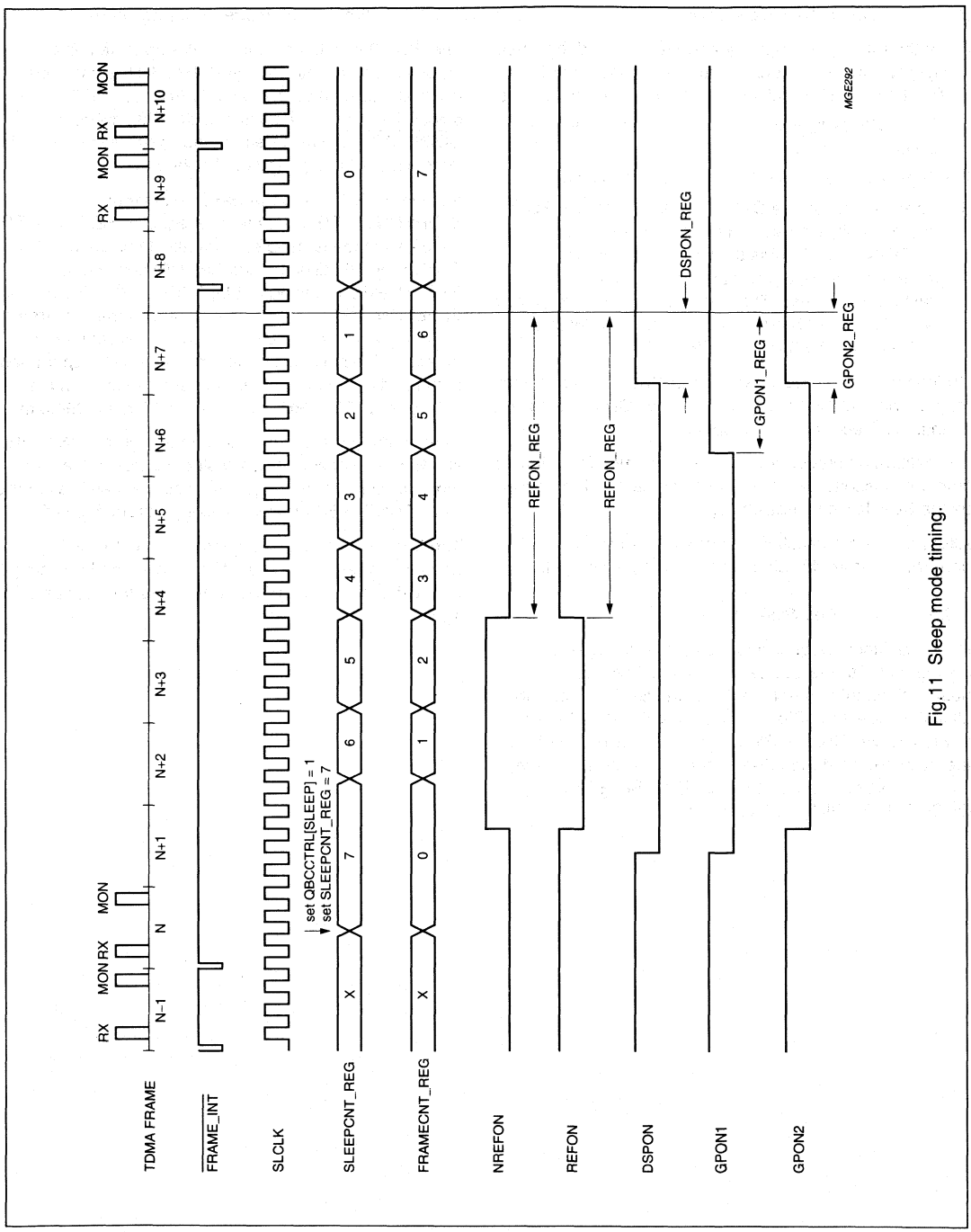


Fig.11 Sleep mode timing.

8.4 RF-IC Interface Bus

This block provides a serial interface to control the RF devices like synthesizer, baseband interface IC etc. The interface is upward compatible with the 'Philips Three Wire Bus'. Compared with the Philips bus it is extended for bidirectional data transfer and additional timing modes are implemented. The interface consists of a clock (RFCLK), a data output (RFDO), a data input (RFDI) and enable lines (RFEN1 to RFEN4 and RFE). The interface is subdivided into three logical channels as described below.

8.4.1 Frequency Setting Channel

The registers RX_REG, TX_REG and MON_REG are set up during frame N – 1 with the frequency information for the RX, TX or MON burst of frame N. Therefore these three registers have a pipeline stage. The pipelining takes place at the beginning of every TDMA frame together with the frame interrupt generation. The transmission of the three registers is controlled from the timing generator as described in Section 8.3.2.7. The register TX_REG is also used for a monitor burst during the TX timeslot. The register RFCTRL0_REG contains four address bits (A0 to A3) which are transmitted with either of the three data registers. The data structure and the function of the mode (M0 to M2) and select (SEL0, SEL1) flags contained in RFCTRL0_REG is described in Section 8.4.4.

8.4.2 Gain Control Channel

The registers RXGAIN_REG, TXGAIN_REG and MONGAIN_REG are set up during frame N – 1 with the gain control information for the RX burst or MON burst of frame N. Therefore these three registers have a pipeline stage. The pipelining takes place at the beginning of every TDMA frame together with the frame interrupt generation. The transmission of the three registers is controlled from the timing generator as described in Section 8.3.2.7. No gain information is sent prior to a TX-burst. The register TXGAIN_REG is used for a monitor burst during the TX timeslot. The DAC bit of these registers is not transmitted but used to select between the registers DAC0_REG and DAC1_REG. The register RFCTRL1_REG contains four address bits (A0 to A3) which are transmitted with either of the three data registers. The data structure and the function of the mode (M0 to M2) and select (SEL0 and SEL1) flags contained in RFCTRL1_REG is described in Section 8.4.4.

The DAC flag in xxGAIN_REG selects either DAC0_REG or DAC1_REG to be transmitted immediately after xxGAIN_REG. These two registers hold static data and do not have an additional frame pipeline stage like the xx_REG or xxGAIN_REG. The contents of register RFCTRL2_REG functionally corresponds to the contents of RFCTRL1_REG.

Two further registers, DACON_REG and DACOFF_REG exist. They are used to power-up or power-down a gain setting DAC. These two registers also hold static data like DACx_REG. The transmission of the three registers is controlled from the timing generator as described in Section 8.3.2.7. The contents of RFCTRL3_REG register functionally corresponds to the contents of RFCTRL1_REG or RFCTRL2_REG.

The MSB (bit 16) of the registers DAC0_REG, DAC1_REG, DACON_REG and DACOFF_REG is located in register MSB_REG, because of the limited address space.

8.4.3 Immediate Control Channel

The Immediate Control Channel (IMC) consists of the registers IMCOUT_REG for the output direction and IMCIN_REG for the input direction. The contents of IMCOUT_REG are transmitted every time a new data word is written to it. The flag SIINT_REG[IMC_OBE] is set after the contents of IMCOUT_REG was copied to the shift register. If the corresponding mask flag SIMASK_REG[IMC_OBE_MASK] is set, the serial interface interrupt SI_INT is activated. Together with IMCOUT_REG being transmitted, the data at RFDI is read into register IMCIN_REG. The flag SIINT_REG[IMC_IBF] is set at the end of the shift operation. The interrupt handling corresponds to the IMC_OBE flag. The interrupt flags are cleared when their corresponding register is written respectively read.

The mode flags in IMCOUT_REG have the same function as the flags in RFCTRLx_REG. The four select flags (SEL0 to SEL3) correspond to the enable lines RFEN1 to RFEN4. Each enable line is activated if their corresponding select flag is set. Therefore it is possible to activate more than one line at a time.

Table 17 Select flags in register IMCOUT_REG

SEL0	SEL1	SEL2	SEL3	ACTIVE ENABLE LINE
1	X	X	X	RFSEN1
X	1	X	X	RFSEN2
X	x	1	X	RFSEN3
X	X	X	1	RFSEN4

The inhibit flag (INH) in IMCOUT_REG controls whether the IMC operation is inhibited during a receive or transmit burst indicated with PDRX2 or NPDTX2 active. If the INH flag is set the IMC operation is delayed until PDRX2 and NPDTX2 become inactive. If the INH flag is reset the two lines are don't care.

8.4.4 Operation Modes and Control Registers

The characteristics of each channel are controlled using the contents of the registers RFCTRL0_REG to RFCTRL3_REG.

The interface is programmable, one of three timing modes can be selected for every data transfer. For the exact timing see Chapter 16. In Mode 3 the transmission of the data registers associated with the control register is disabled.

If there is a conflict between the different data channels, data transmission is scheduled according to Table 22.

Table 18 RC-IF Interface Bus Control Registers

BIT	FLAG	OPERATION
7	M1	These two bits select the timing mode, see Table 19.
6	M0	
5	SEL1	These two bits are used to assert the enable lines RFEN1 to RFEN1, see Table 21.
4	SEL0	
3	A3	These four bits form the address field.
2	A2	
1	A1	
0	A0	

Table 19 Selection of the RC-IF Interface timing modes

MODE	M1	M0	BITS TRANSFERRED	RFE ASSERTED
0	0	0	21	no
1	0	1	21	no
2	1	0	16	yes
3	1	1	Transmission of the corresponding data registers is disabled.	

Note

1. The 16 or 21 data bits are transmitted MSB first according to Table 20.

Table 20 RF-IC Interface data structure

MODE	BITS TRANSFERRED	1ST BIT	LAST BIT
0 and 1	21[1]	D17	A0
IMC channel	21	D20	D0
2	16	D15	D0

Note

1. The 21 bits consist of D17 to D0 and A2 to A0.

Table 21 Selection of enable lines RFEN1 to RFEN4

SEL1	SEL0	ENABLE LINE ASSERTED
0	0	RFEN1
0	1	RFEN2
1	0	RFEN3
1	1	RFEN4

Table 22 Order of priority

PRIORITY	TRANSMISSION
Highest	frequency setting
	gain control DACOFF_REG
	gain control DACON_REG
	gain control xxGAIN_REG then DACx_REG
Lowest	Immediate Control Channel

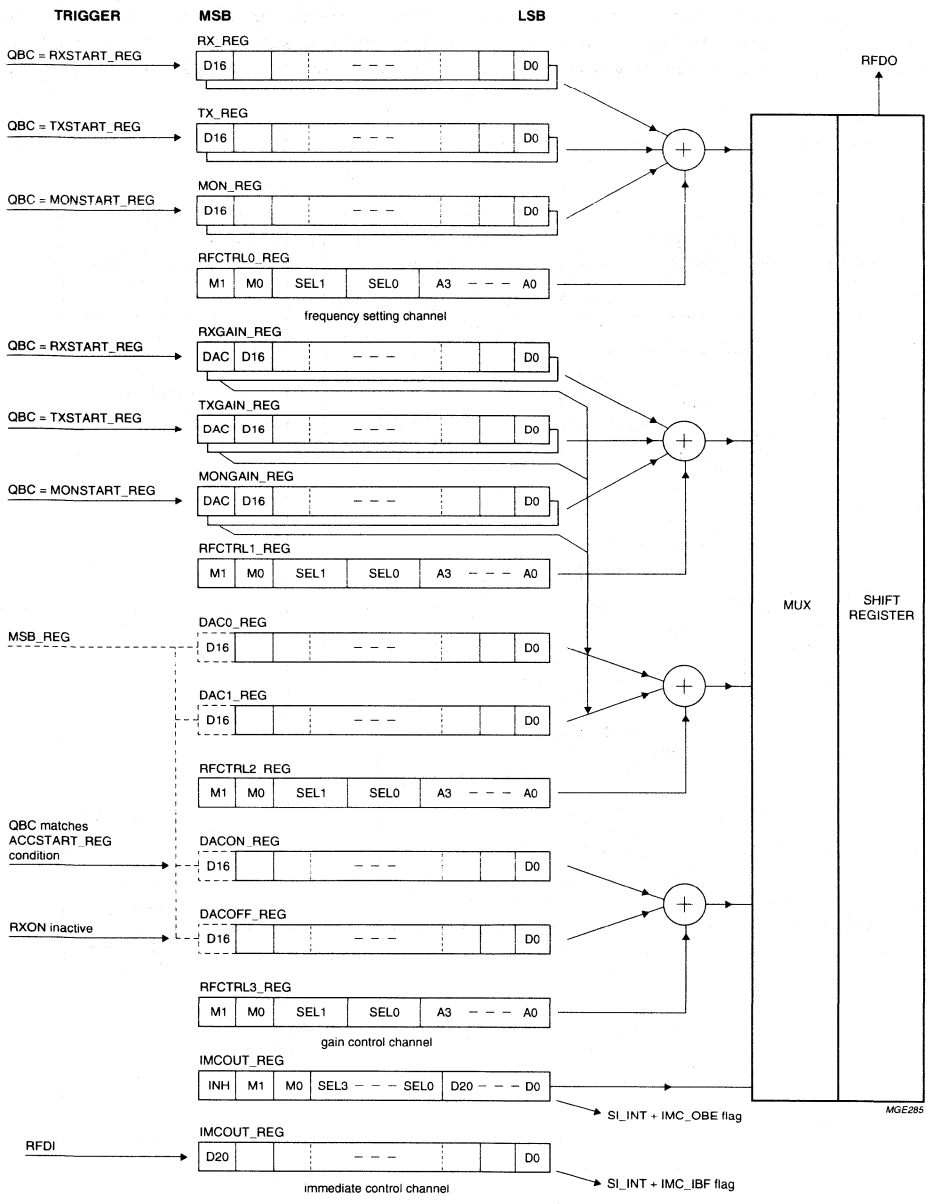


Fig.12 RF-IC interface register set.

8.5 IOM®-2 Interface

The PCF5083 includes a type of PCM Highway like digital Data and Voice interface which is also available for external devices. It can be configured to be compatible to the IOM®-2 standard. The blocks connected to this bus inside the IC are the Y-Port of the DSP core, the IOM®-2 master and the Audio Interface. The clock and frame synchronization signals (DCL, FSC) are either generated internally or provided externally. Figure 13 shows the general structure of the IOM®-2 interface.

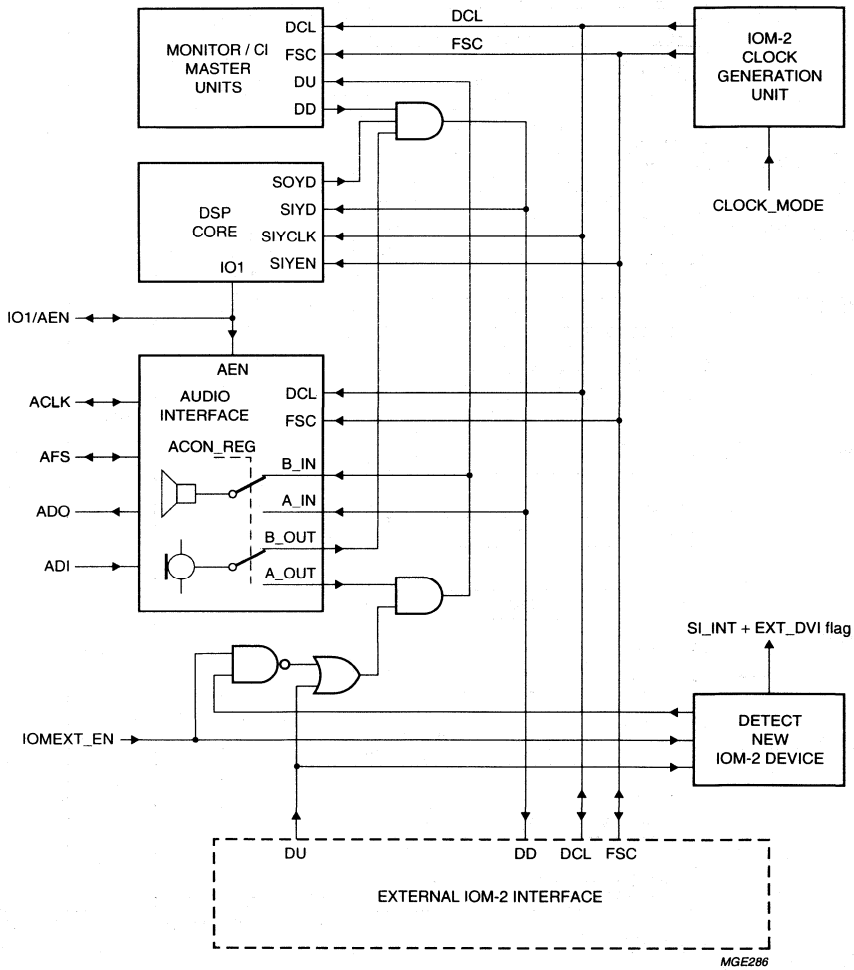


Fig.13 IOM®-2 Interface structure.

8.5.1 IOM®-2 Clock Generation

If the IOM®-2 clock and frame synchronization signals are generated internally from the 13 MHz reference clock, the basis clock runs at 1.536 MHz as illustrated in Fig.14. One 125 µs FSC period consists of 192 DCL periods (0 to 191). The DCL periods 12, 25, 38, 51, 64, 77, 90, 103, 116, 129, 142, 155, 168 and 181 are 8T wide (high time = low time = 4T), where T is the 13 MHz clock period (T = 77 ns). All other DCL periods are 8.5T wide (high time = 4.5T, low time = 4T).

It is possible to extend or to reduce 12 consecutive IOM®-2 frame periods by 1T each. This results in a total reduction or extension of one quarterbit (12T = 923 ns), which is required in case of timing alignment. This adjustment is performed by setting either the FSCEXT flag for extension, or the FSCRED flag for reduction. Both these flags reside in QCCTRL_REG. The flags are automatically reset after the adjustment.

The length of the frame synchronization pulse (FSC) is chosen to $29 \times 8.5T + 2 \times 8T + 6T = 268.5T$.

The whole IOM®-2 signal generation is disabled in Clock mode 0 (see Table 23, default after reset).

In Sleep mode the REFON output stays active to keep the 13 MHz oscillator running as long as the IOM®-2 interface is not disabled (Clock mode 0).

Other clock modes are derived from this mode by subdividing the 1.536 MHz DCL clock by 2, 3, 4, 6, or 12. The FSC period is not changed.

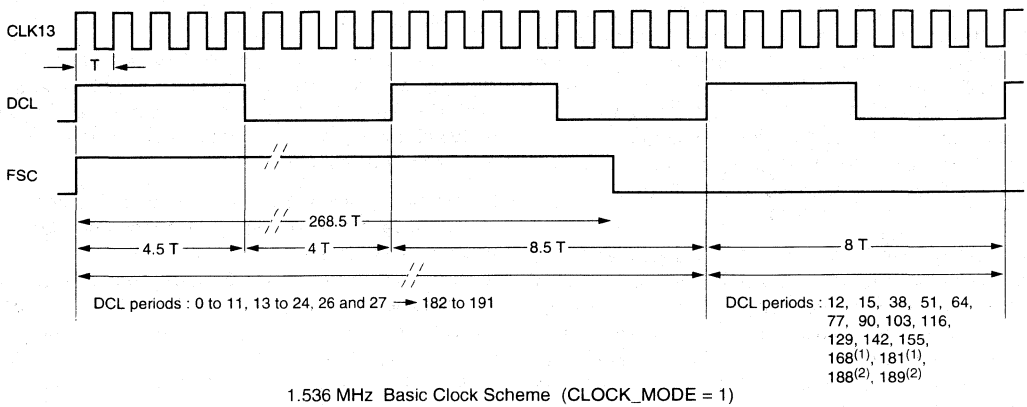
In external clock mode the IOM®-2 clock and frame synchronization signal are provided via the DCL and FSC pins. The DCL clock in this mode is a multiple of 128 kHz or 256 kHz with a maximum frequency of 2.048 MHz or 4.096 MHz respectively.

In both internal and external clock modes, it is possible to select between a double clock cycle mode per data bit or a single clock cycle mode per data bit with the IOMCON_REG[DATA_MODE] flag. In double clock cycle mode the data output gets valid with the first rising edge of DCL and the data input is sampled with the second negative edge of DCL within a bit period. In single clock cycle mode the data output gets valid with the rising edge of DCL and the data input is sampled with the falling edge of DCL within a bit period. Data is organized in 16-bit timeslots. The maximum number of timeslots supported is 12 in internal and 16 in external clock mode.

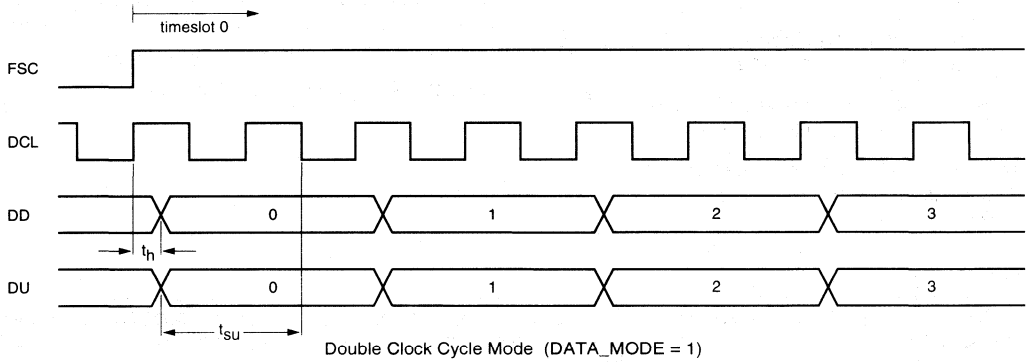
Table 23 lists all possible clock modes.

Table 23 IOM®-2 Clock Modes

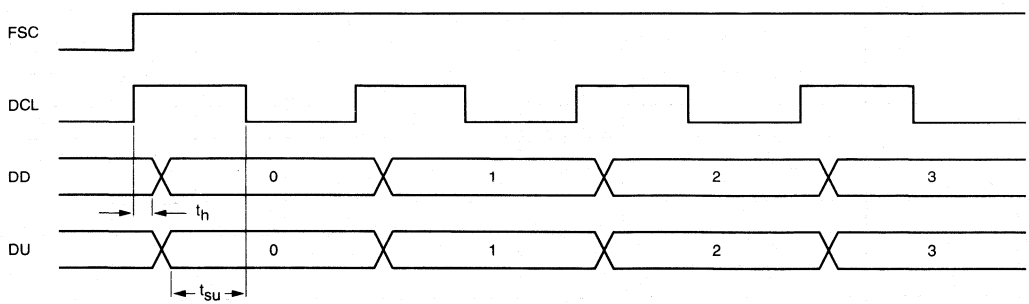
DCL FREQUENCY	SINGLE(1)/DOUBLE(2) CLOCK CYCLE MODE	NUMBER OF 16-BIT TIMESLOTS	DIVISION RATIO	CLOCK_MODE FLAGS (DEC.)	DATA_MODE FLAG
IOM®-2 interface off	–	–	–	0	x
1.536 MHz	2	6	1	1	1
1.536 MHz	1	12	1	1	0
768 kHz	1	6	2	2	0
768 kHz	2	3	2	2	1
512 kHz	2	2	3	3	1
512 kHz	1	4	3	3	0
384 kHz	1	3	4	4	0
256 kHz	2	1	6	5	1
256 kHz	1	2	6	5	0
128 kHz	1	1	12	6	0
external clock n × 128 kHz (2.084 MHz max.)	1	n (n ≤ 16)	–	7	0
external clock n × 256 kHz (4.096 MHz max.)	2	n (n ≤ 16)	–	7	1



1.536 MHz Basic Clock Scheme (CLOCK_MODE = 1)



Double Clock Cycle Mode (DATA_MODE = 1)



Single Clock Cycle Mode (DATA_MODE = 0)

MGE293

Fig.14 IOM®-2 Interface timing diagrams.

8.5.2 IOM®-2 Master Unit

The IOM®-2 master unit implements two monitor channels and C/I channel masters. All handshake protocols are implemented in accordance with the IOM®-2 standard with the exception of the constraints mentioned below. The data structure of a 16-bit monitor and C/I timeslot is also implemented according to the IOM®-2 standard with the exception that the timeslot location is not fixed within a IOM®-2 frame.

As data is structured in 16-bit timeslots (see Table 24) the timeslot a master works on, can be selected with the flags IOMCON_REG[MASTERx_TS0 to MASTERx_TS3]. These bits binary encode the timeslot number (0 to 5), with timeslot 0 being indicated with the rising edge of FSC.

Both monitor masters can be independently enabled with the flags IOMCON_REG[MASTERx_EN].

For every serviced channel a data register (MON0_REG, MON1_REG, CI0_REG and CI1_REG) with input and output buffer stage and a state machine for receive and transmit direction exists. For every register IOMFLAG_REG holds two flags to indicate the input data buffer full and the output buffer empty condition. The flags are xxx_IBF (input buffer full) and xxx_OBE (output buffer empty) with xxx equal to the register name. If one of these flags together with the corresponding enable flag in IOMEN_REG is set the IOM®-2 interrupt is activated (refer to Section 10.2). The flags are reset with read respectively write operations to their corresponding data register.

8.5.3 Monitor Channel Transmitter Protocol

- After IOMCON_REG[MASTERx_EN] is set to a logic 1, the transmitter state machine is in an idle state. The pattern FFH is sent and the output buffer empty flag MONx_OBE (x = 1 or 2) is set. The MX flag is sent as a logic 1 in accordance with the IOM®-2 specifications.
- To initiate a message transmission the System Controller has to program MONx_REG with the first byte of the message. The MONx_OBE flag is cleared with the data write access.
- A full handshake is implemented in accordance with the IOM®-2 specifications. The transmitter may delay the data transmission in case the System Controller does not provide new data in time. MX = 0 is maintained until MONx_REG is programmed with new data. The MONx_OBE flag is cleared with the data write access. The receiver delays the data transmission if it sends no data acknowledge. In this case MX = 0 is maintained and the data byte is repeated in subsequent frames.
- To request new data from the controller the MONx_OBE flag may be set as soon as the data acknowledge (MR = 1) from the receiver is detected except for the first byte reception. Here the MR transition HIGH-to-LOW has to be detected. This leaves the controller approximately 250 µs to program the MONx_REG with the next byte without delay within the handshake procedure except for the first byte.
- An end of transmission is sent if the TEOMx flag in IOMCTRL_REG is set when MONx_OBE = 1 after the last byte transmission. The end of transmission is sent (MX = 1 in at least two subsequent frames) after the acknowledge of the last byte is completely received. After the end of transmission is sent the transmitter state machine is in the idle state.
- The TEOMx flags are also used to initialize the transmitter state machine. If the flag is set the state machine may get from any state into the idle state.
- The TEOMx flag is automatically cleared.
- If an abort request is received, the transmitter in accordance with the specifications, sends the end of transmission sequence and enters the idle state. The MONx_OBE flag is set. The abort request is indicated with the RABORTx flag set in IOMCTRL_REG. RABORTx = 1 also asserts the IOM®-2 interrupt (MONx_OBE_EN is used as enable bit) to indicate the abort to the System Controller. The flag is reset with the MONx_OBE flag.

Table 24 Data structure of a 16-bit IOM®-2 monitor and C/I master timeslot

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MONX								C/IX						MR	MX

8.5.4 Monitor Channel Receiver Protocol

- After IOMCON_REG[MASTERx_EN] is set to a logic 1, the receiver state machine is in an idle state and waits for the first byte transmission. The input buffer full flag MONx_IBF is cleared. The MR flag is sent as a logic 1 in accordance with the IOM®-2 specification.
- After the reception of a data byte the MONx_IBF flag is set and the System Controller may read the data from MONx_REG.
- A full handshake is implemented in accordance with IOM®-2 specification. The receiver may delay the data transmission if the input buffer is full and the System Controller does not read the buffer in time. In this case MR = 0 is maintained until MONx_REG is read. The MONx_IBF flag is cleared with the data read access. The transmitter may delay the data transmission if it delays the next byte valid indication. In this case MR = 0 is maintained in subsequent frames.
- If an end of transmission is detected the receiver state machine gets into the idle state. The REOMx flag in IOMCTRL_REG is set. REOMx = 1 also asserts the IOM®-2 interrupt (IOMx_IBF_EN is used as enable bit) to indicate the end of transmission to the System Controller. The REOMx flag is cleared with a dummy read of MONx_REG.
- To send an abort request the TABORTx flag in IOMCTRL_REG is set. The receiver state machine enters the idle state. The TABORTx flag is reset after the procedure.

Time-outs are not detected. Collision detection and the maximum speed case is not supported.

8.5.5 Command/Indication Channel Transmitter

All data words are sent at least in two subsequent frames. If the transmitter runs out of data the last data word is repeated. The flags CI0(1)_IBF and CI0(1)_OBE are provided to indicate the input/output register status.

8.5.6 Command/Indication Channel Receiver

If the received data is different from the data input buffer the new data pattern is loaded into the data input buffer. The CI0(1)_IBF flag is cleared if it is set. If during the next frame the received data is identical to the data stored in the data input buffer the buffer contents is considered valid and the CI0(1)_IBF flag is set. The System Controller now has to fetch the data within the next 125 µs, otherwise data might be lost.

8.5.7 Audio Interface

The Audio Interface provides the translation of one 16-bit IOM®-2 timeslot into a timing according to Chapter 16 for the receive and transmit direction. The operation of the interface is configurable with the flags of register ACON_REG. The Audio Interface is enabled or disabled under control of the DSP core with IO1/AEN = 1. Otherwise the data word 00H is sent in both directions.

With ACON_REG[TRANS_EN] = 1, a transparent mode is selected. In this mode the internal IOM®-2 signals FSC and DCL are directly connected to ACLK and AFS. ADI is directly connected to A_OUT or B_OUT and ADO to A_IN or B_IN.

The following should be noted:

- The flags in register ACON_REG should only be changed when the Audio Interface is disabled with IO1/AEN = 0
- The Audio Interface can only operate in the transparent mode if a timing mode is selected which results in only one 16-bit timeslot on the IOM®-2 side
- The frequency of ACLK must be chosen such that the complete transmission of a 16-bit word via the Audio Interface does not exceed the duration of N-1 timeslots, with N equal to the number of 16-bit timeslots on the IOM®-2 side
- Jitter is not allowed on AFS and ACLK as audio data might get corrupted.

Table 25 Audio Interface configuration register (ACON_REG)

BIT	FLAG	OPERATION (if bit is set)
0	TX_EN	Enable transmit direction (ADI to IOM®-2).
1	TX_DEST	Select output to IOM®-2. A logic 0 selects A_OUT; a logic 1 selects B_OUT.
2	RX_EN	Enable receive direction (IOM®-2 to ADO).
3	RX_SOURCE	Select input from IOM®-2. A logic 0 selects A_IN; a logic 1 selects B_IN.
4 to 7	TX_SLOT0 to TX_SLOT3	IOM®-2 timeslot translated from the transmit section (0 to 15).
8 to 11	RX_SLOT0 to RX_SLOT3	IOM®-2 timeslot translated from the receive section (0 to 15).
12	TRANS_EN	Enable transparent mode.

8.5.8 External IOM®-2 interface

This block provides an IOM®-2 interface for external devices and accessories e.g. digital handsfree equipment data and fax interfaces etc. It is used as an interface to the system simulator during type approval.

The external IOM®-2 interface (DCL, FSC, DU and DD) is only enabled if the flag IOMCON_REG[IOMEXT_EN] is set. Otherwise, unless in external clock mode, the outputs DCL, FSC and DD are in their high-impedance state and the input DU is don't care (default after reset). In external clock mode the flag IOMCON_REG[IOMEXT_EN] flag only controls the data lines DU and DD. DCL and FSC are inputs in this mode independently from the state of the flag. If the flag IOMCON_REG[IOMEXT_INV] is set, all I/Os of the external IOM®-2 interface are inverted to allow the use of an external inverting driver circuit.

If the external IOM®-2 interface is disabled with IOMCON_REG[IOMEXT_EN] = 0, the DU input is externally pulled-up and will be monitored for a LOW level. An external device has to pull-down this line to register itself. If a LOW on DU was detected, the SI_INT interrupt is activated with flag SIINT_REG[EXT_IOM] set. The flag and therefore the interrupt condition is automatically cleared after IOMCON_REG[IOMEXT_EN] was set.

8.6 MMI Interface

The PCF5083 provides a RS232 and a Power-down interface to fully support the MMI controller TDA8005.

8.6.1 RS232 interface

This block provides a full RS232 interface with a fixed 8E1 protocol configuration.

The shift clock is derived from the 1 MHz clock for normal operation. For test purposes a clock applied at input ADI is used if SYSCON_REG[RS232_CLK] is set. The clock is divided by $12 \times 3 \times 16$ to derive the shift clock. This results in a baud rate of 22569.44 Baud at 13 MHz. The receiver works with an oversampling of 16.

8.6.1.1 Transmit

After writing to the register TXD_REG, the register content is serially clocked out. The SIINT_REG[TXD_OBE] flag is set and the SI_INT interrupt is generated (refer to Section 10.2). The flag and therefore the interrupt condition is cleared after writing the next data byte to register TXD_REG.

8.6.1.2 Receive

The incoming serial data stream is clocked into register RXD_REG. SIINT_REG[RXD_IBF] is set after a data byte was received and the SI_INT interrupt is generated. The state of the RXD_IBF flag is available on the $\overline{\text{MMIEN}}$ output and is used to implement a hardware handshake to the TDA8005. The SIINT_REG[PAR_ERR] flag signals a parity error and will be updated when the RXD_IBF flag goes active. The RXD_IBF flag and therefore the interrupt condition is cleared automatically after reading the register RXD_REG.

Both interrupt conditions can be disabled with the corresponding mask flags in SIMASK_REG. The flag handling remains the same as described.

The output $\overline{\text{MMIEN}}$ is set to a logic 1 as long as HWCTRL_REG[MMICLK] = 0.

Note that PAR_ERR is not used as an interrupt condition.

8.6.2 MMI power-down interface

The MMI power-down interface controls the power consumption of the MMI controller (MMIC) TDA8005 by halting its main 13 MHz clock. The following signals are used:

- MMICLK: 13 MHz clock output, main clock for the MMIC
- MMIREQ: MMI clock request input.

The MMI wake-up and power-down procedures are:

1. Force MMIC into power-down mode:
   Set HWCTRL_REG[MMICLK] = 0 to stop the 13 MHz MMI clock. The MMICLK output is held LOW and the output $\overline{\text{MMIEN}}$ of the RS232 interface is set HIGH.
2. Wake-up MMIC via System Controller:
   Set HWCTRL_REG[MMICLK] = 1 to activate MMICLK.
3. Wake-up MMIC after keyboard or SIM card reader activity:
   In this case the MMIC generates a LOW-to-HIGH transition on pin MMIREQ. The flags MMIREQ and MMICLK in register HWCTRL_REG will be set and the MMICLK output is activated. If the timing generator unit (SGU) is in Sleep mode, a wake-up request is issued to force the SGU into the wake-up state. In the wake-up state HWCTRL_INT and MMICLK are activated. The MMIREQ flag has to be explicitly cleared by the System Controller.

It should be noted that:

- A LOW-to-HIGH transition of MMIREQ is detected independent of HWCTRL_REG[MMICLK] respectively.
- As long as HWCTRL_REG[MMICLK] = 1, the REFON output stays active even if the SGU enters Sleep mode.

During power-up reset indicated with $\overline{RST}$ active LOW, HWCTRL_REG[MMICLK] is set and MMICLK is activated.

8.7 General purpose parallel I/O port

The PCF5083 includes a 6-bit general purpose parallel I/O port. Every I/O line, except PIO0, has a corresponding data bit in PORTDATA_REG and a data direction bit in PORTDDIR_REG. The bits in PORTDATA_REG directly represent the state of the I/O pins if the port is configured as an input. Otherwise if the port is configured as output, the data written to PORTDATA_REG directly represents the state of the port line. A logic 1 in PORTDDIR_REG configures the port line as an output, a logic 0 as an input.

PIO0 is configured as output only. It is used internally to drive the reset input of the DSP core.

8.8 Real Time Clock

A real time/alarm time clock unit is included in the timer core. The clock unit is driven from the 32.768 kHz crystal oscillator. A leap year function is included. The clock function utilizes the registers/counters specified in Table 26.

Table 26 Clock function registers/counters

REGISTERS/ COUNTERS	CLOCK FUNCTION
SEC_REG	seconds, 00 to 59, two 4-bit digits BCD encoded
MIN_REG	minutes, 00 to 59, two 4-bit digits BCD encoded
HOUR_REG	hours, 00 to 23, two 4-bit digits BCD encoded
DAY_REG	day, 0 to 6, 0 = Monday to 6 = Sunday
DATE_REG	date, 0 to 31, two 4-bit digits BCD encoded
MONTH_REG	month, 01 to 12, two 4-bit digits BCD encoded
YEAR_REG	year, 00 to 99, two 4-bit digits BCD encoded

If the flag HWCTRL_REG[SECINT] is reset, the hardware control interrupt (HWCTRL_INT, refer to Section 10.2) is asserted with the HWCTRL_REG[CLOCK] flag set every time MIN_REG is incremented. Otherwise if the flag is set, the interrupt is asserted every time SEC_REG is incremented.

8.8.1 Setting the real time clock

To set the real time clock, the SETCLOCK bit in HWCTRL_REG must be set to a logic 1. The flag is then polled until it is read as a logic 1 again. This action may last up to 0.5 s. After SETCLOCK = 1 is detected, the clock registers can be written. After the write operation SETCLOCK has to be reset again. If the register setting takes place immediately after the hardware control interrupt was asserted, the clock registers may be written without polling of the SETCLOCK flag (SETCLOCK still has to be set prior and reset after the register write operation).

The following should be noted:

- If the Sleep mode is invoked, a wake-up request is generated every time the hardware control interrupt is asserted. To increase performance it is not recommended to use the interrupt facility at a rate of one second during Sleep mode.

An alarm function is implemented using the registers SEC_A_REG, MIN_A_REG, HOUR_A_REG, DAY_A_REG, DATE_A_REG, MONTH_A_REG and YEAR_A_REG. If the contents of these registers equals the corresponding counters, the hardware control interrupt is asserted with the flag HWCTRL_REG[ALARM] set. If all bits are set to one in one of the registers (07H in case of the DAY_A_REG) it is don't care for the comparison. If the alarm function is activated while the MS is switched off, the MS is powered up as described in Section 8.2.1.

If $\overline{RSTC}$ is activated the clock counters are reset to 00H, except date and month which are set to 01H. MONTH_A_REG is set to 00H to avoid an alarm condition. The other alarm registers are undefined.

9 DESCRIPTION OF THE DSP CORE

9.1 Interface description

9.1.1 Baseband Digitizer Interface

The PCF5083 serial input port SIX is used for the reception of off-air data from the baseband digitizer PCF5072 (BBD).

The port consists of:

- Serial Input Data signal (SIXD), containing 16I and 16Q data bits, MSB first
- Serial Input Clock signal (SIXCLK), running at 13 MHz
- Serial Input Enable signal (SIXEN), active LOW.

Regularly spaced I and Q samples are sent to the DSP with a periodicity of 1/(2 270.833 kHz); (twice the GSM bit period). The number of incoming samples expected by the DSP depends upon the current status in which the DSP is operating (see Table 27).

The column START OF SAMPLING indicates in which time slot (1 time slot = 1/8 TDMA frame = 577 µs) the sampling of the I and Q pairs has to start.

Time slots are numbered from 0 to 7, whereby slot 0 is defined as the receive time slot of the mobile station (see Section 8.3.2.1).

Each I/Q component pair is represented by two 16-bit two's complement numbers, as shown in Table 28, with one sign bit (I15 and Q15) and 15 fractional bits. The range for the I and Q components is specified below.

Range: $-1.0 \leq I,Q < +1.0$

It should be noted that due to the limited SNR of the PCF5072 of 66 dB, only the 11 MSBs of I and Q contain meaningful data.

The I and Q components are defined as follows:

$I = f(A) \times \cos \Phi$

$Q = f(A) \times \sin \Phi$

where A is the magnitude and Φ is the phase of the antenna input signal. The function f(A) describes the characteristic of the AGC applied (see Fig.16).

Table 27 Time window for BBD output data

OPERATION STATUS	START OF SAMPLING	NUMBER OF I AND Q PAIRS
Reception of a normal burst	TS 0	149
Reception of a synchronization burst	–	167
Reception of a normal burst	TS 0	167
Level measurement of neighbouring BCCH	TS 5	80
DC offset measurement	TS 5	128
FCB search	TS 6	1404[1] (9 × 156)

Note

1. The value 1404 for FCB search is the default value after reset. It can be changed by the FB_search_fcb_init procedure.

Table 28 I and Q component format

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
O	O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0

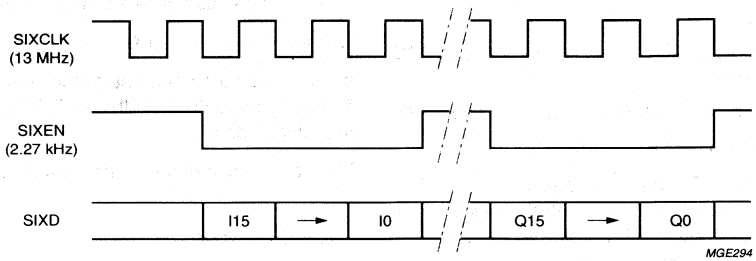


Fig.15 Baseband RX Timing diagram.

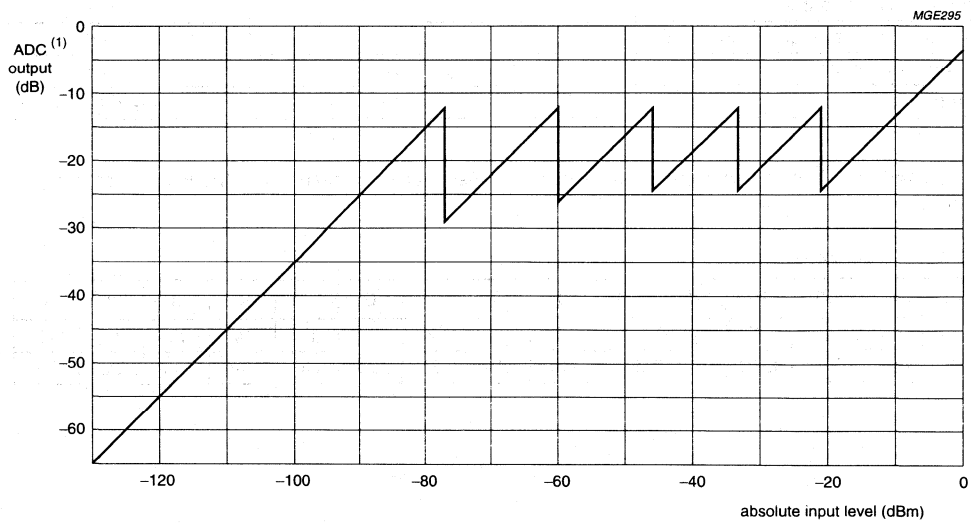


Fig.16 AGC characteristic.

9.1.2 GMSK Modulator Interface

The PCF5083 serial output port SOX is used to transmit the coded, interleaved and formatted bits to the GMSK modulator in the PCF5072 baseband interface IC.

The SOX port consists of:

- Serial Output Data signal (SOXD)
- Serial Output Clock signal (SOXCLK), running at 270.83 kHz
- Serial Output Enable signal (SOXEN), active LOW.

The GSM bit clock is directly used as the external shift clock, therefore no external buffering of transmission data is necessary.

The PCF5083 general purpose I/O pin IO4 is used to enable or disable the transmitter during DTX. If IO4 = 0, the transmitter is enabled. If IO4 = 1, the transmitter is disabled. It is sampled by the TDMA timer at the beginning of the transmit burst period.

9.1.2.1 Burst format

Tables 29 and 30 show the format of the normal and access burst produced by the DSP. The period of the 8 leading bits allows the power amplifier to ramp-down and ramp-up.

Table 29 Normal burst format

BITS	NUMBER OF BITS	DESCRIPTION
0 to 7	8	dummy bits (set to logic 1)
8 to 155	148	BN0 to BN147 in accordance with *"GSM Rec. 05.02"*

Table 30 Access burst format

BITS	NUMBER OF BITS	DESCRIPTION
0 to 7	8	dummy bits (set to logic 1)
8 to 95	88	BN0 to BN87 in accordance with *"GSM Rec. 05.02"*
96 to 155	60	dummy bits (set to logic 1)

9.1.3 Audio and Data Interface

The PCF5083 serial port Y is connected on-chip to the IOM®-2 interface of the Timer Core. It is used for connection to the following devices:

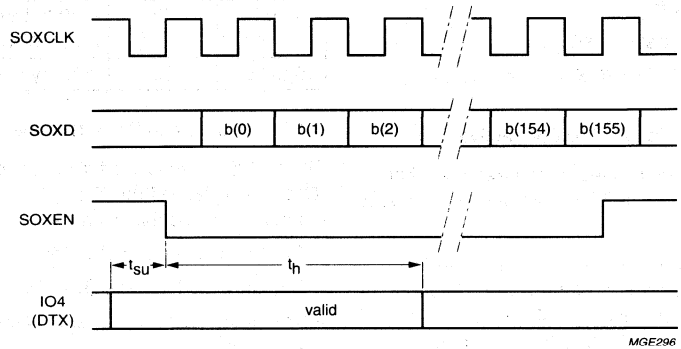
- PCM codec in the PCF5072
- Digital Audio Interface (DAI), used during type approval
- Terminal adaptor for data services
- External digital answering machine.

The physical transfer order on the IOM®-2 bus is 16-bit, MSB first. The following signals are used:

- Serial data input SIYD
- Serial data output SOYD
- Serial shift clock SIYCLK
- Frame synchronization input SIYEN.

The DSP by default reads and writes the first 16-bit timeslot of the IOM®-2 interface. This may be changed with the appropriate software command to any 16-bit timeslot.

Input and output from/to the IOM®-2 bus is performed via two FIFOs named audio input and audio output FIFO. These FIFOs are implemented by firmware. Each FIFO is able to store up to 297 16-bit samples.



DTX setup time: $t_{su} > 0$
DTX hold time: $t_h > 124 \times 3.69\ \mu s$

Fig.17 GMSK modulator timing diagram.

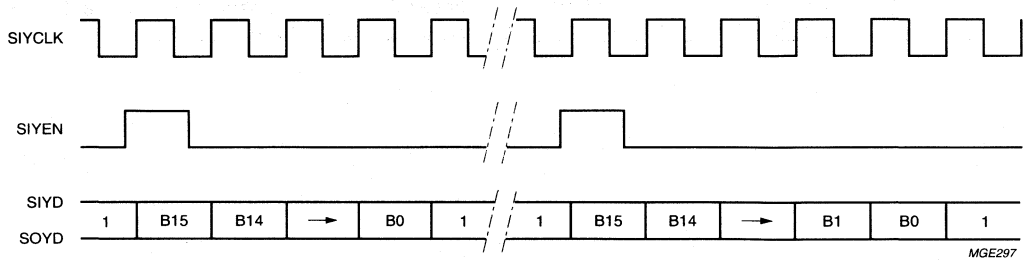


Fig.18 Audio and Interface timing (default).

9.1.4 AUDIO INTERFACE

9.1.4.1 Downlink speech frame format

Every 20 ms the speech decoder in the DSP outputs a speech frame consisting of 160 16-bit words. These speech frames are transmitted to the PCM codec. The speech frame format is described in Table 32.

Table 31 Field descriptions

FIELD	DESCRIPTION
SAMPLE	This field contains the 13-bit linear PCM audio samples in two's complement (MSB = sign bit) representation as defined by the *"GSM recommendation 06.01"*.
PARM	Whenever the speech decoder is active the PARM field is used to transfer the speech parameters (D1 to D260) together with some frame classification information (see Table 99) and the currently selected test mode (see Table 34) out of the DSP. The terms SP (speech flag), SID (silence descriptor) and MUF (muting flag) are defined in *"GSM Rec. 06.31"* (DTX for full-rate speech TCH). The HF bit indicates, whether the speech codec is operating in handsfree mode (HF = 1) or not. The bits TM2 to TM0 are intended to be evaluated by an external Digital Audio Interface (DAI). They determine the currently selected test mode during type approval as described in *"GSM Rec. 11.10, Section III.1.2.4.7"*. TM2 to TM0 are passed in the TMODE file of the operation_mode parameter of the speech decoder procedure. Refer to Section 9.3.1 for more information.
SYNC	Synchronization signal for external (test) equipment. Marks the 20 ms speech frames. Each falling edge of SYNC marks the beginning of a new output speech frame and with a constant offset due to internal module processing time the rising edge of SYNC marks a new input speech frame. As soon as audio output data are available this bit always reflects the internal speech frame timing independently of other processing tasks of the DSP.

Table 32 Downlink speech frame format

OFFSET	SAMPLE FIELD													PARM FIELD		SYNC FIELD
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	audio sample 0													TM1	TM0	0
1	audio sample 1													HF	TM2	0
2	audio sample 2													0	0	.
3 to 27	audio samples 3 to 27													not used		.
28	audio sample 28													SID	0	0
29	audio sample 29													MUF	SP	.
30	audio sample 30													D2	D1	.
31	audio sample 31													D4	D3	.
32 to 157	audio samples 32 to 157													.	.	.
158	audio sample 158													D258	D257	.
159	audio sample 159													D260	D259	1

Table 33 Frame classification

FRAME TYPE	SP	SID2	MUF
Speech frame	1	0	0
Transmitted SID	0	1	0
Repeated SID	0	0	0
Silence frame	1	0	1
Reserved	all other codes		

Table 34 Test mode selection

DESCRIPTION	TM2	TM1	TM0
Normal operation (no tested divide via DAI)	0	0	0
Test of speech decoder/DTX functions (downlink)	0	0	1
Test of speech encoder/DTX functions (uplink)	0	1	0
Test of acoustic devices and ADCs and DACs	1	0	0
Reserved	all other codes		

9.1.4.2 Uplink Speech Frame Format

Every 20 ms the speech encoder in the DSP requires a speech frame consisting of 160 16-bit words. The speech frame format is described in Table 36. Each word consists of three fields as shown in Table 35.

Table 35 Field descriptions

FIELD	DESCRIPTION
SAMPLE	This field contains the 13-bit linear PCM audio samples in two's complement (MSB = sign bit) representation as defined by the *"GSM recommendation 06.01"*.
PARM	If the bypass_flag in SP_encoder_TCHFS procedure (see Section 9.3.1) is set to 1, the speech encoder is bypassed and the bits D1 to D260 are used as the coded speech frame. If bypass_flag is set to 2, the speech encoder is only bypassed, if the control flag BM0 is set to 1 and BM1 is set to 0. The SP_R flag indicates, either a speech frame (SP_R = 1) or a silence frame (SP_R = 0) is transmitted. Before the external device could send meaningful information, it has to synchronize to the rising edge of the SYNC bit (see Table 43).
RESD, RESE	RESet Decoder, RESet Encoder. In test mode (see Section 9.3.1 speech coding procedures) these bits behave as a reset signal for the speech decoder/encoder on a LOW-to-HIGH transition, RESD/RESE must remain set for at least 40 ms.

Table 36 Uplink speech frame format

OFFSET	SAMPLE FIELD													PARM FIELD		RESD FIELD
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	audio sample 0													RESE	not used	RESD
1	audio sample 1													not used		.
2 to 27	audio samples 2 to 27															.
28	audio sample 28													BM1	BM0	.
29	audio sample 29													–	SP_R	.
30	audio sample 30													D2	D1	.
31	audio sample 31													D4	D3	.
32 to 157	audio samples 32 to 157													.	.	.
158	audio sample 158													D258	D257	.
159	audio sample 159													D260	D259	RESD

9.1.5 TERMINAL ADAPTOR INTERFACE FOR DATA SERVICES

9.1.5.1 General description

In Fig.19 the block diagram of the data service architecture using the PCF5083 is shown. The GSM terminal is connected to an external terminal adaptor via the IOM®-2 interface (serial port Y) of the PCF5083. Channel coding in accordance with *"GSM recommendation 05.03"* is done by the DSP, rate adaptation and e.g. Hayes command handling is done by the terminal adaptor.

There are two types of information that have to be exchanged between the terminal adaptor and the GSM terminal:

1. User data that has to be transmitted via the air interface. This is the input and output of the channel codec in the PCF5083
2. Control data which has to be exchanged between the System Controller and the terminal adaptor.

Data transfer via the IOM®-2 is done in form of data frames. Each data frame contains 160 16-bit samples (20 ms) and consists of a user data block containing user data to/from the channel codec and a control data block containing control data to/from the System Controller. The DSP firmware (the procedures MP_read_data_frame and MP_write_data_frame, see Section 9.3.1) performs multiplexing and demultiplexing of user and control data. Control data is forwarded to the System Controller or to the terminal adaptor, respectively without modification or interpretation by the DSP.

A fully integrated solution for the architecture of GSM data services is in preparation, at which rate adaptation is realised as an additional DSP software module, Hayes command interpretation is part of the P90CL301 software and data communications are done via the RS-232 port of the P90CL301.

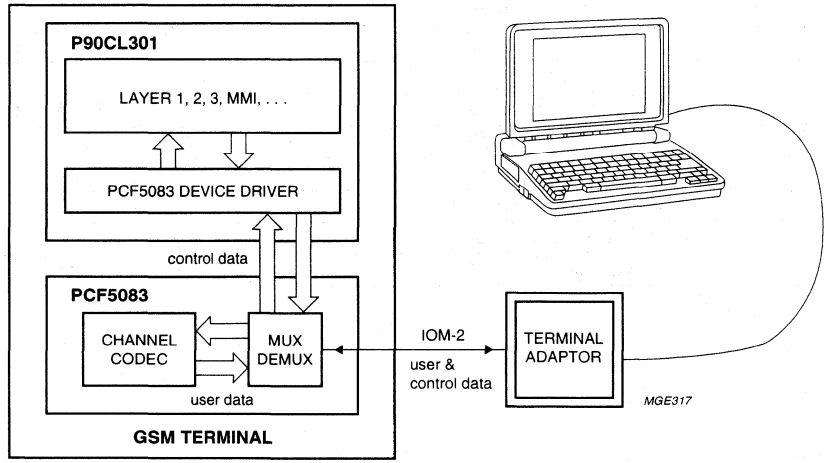


Fig.19 Block diagram of the GSM Data Services with the PCF5083.

9.1.5.2 Format of downlink data frames

The downlink data frame format is described in Table 40. Each word consists of four fields; these are described in Table 37.

Table 37 Field descriptions

FIELD	DESCRIPTION
DATA	Depending on the contents of the CMD field (see Table 38), this field contains a data byte belonging to a user or a control data block or auxiliary control information for the terminal adaptor.
CMD	This field classifies the 16-bit samples as described in the Table 38.
SYNC	Synchronization signal for external (test) equipment. Marks the 20 ms speech frames. Each falling edge of SYNC marks the beginning of a new output speech frame and with a constant offset due to internal module processing time the rising edge of SYNC marks a new input speech frame. As soon as audio output data are available this bit always reflects the internal speech frame timing independently of other processing tasks of the DSP.
INFO	This field may be used by external devices to distinguish between audio and data frames. The INFO field of word#2 contains the so called frame identification (FID); see Table 39.

Table 38 Classification of the 16-bit samples

CMD FIELD					DESCRIPTION
7	6	5	4	3	
0	0	0	0	1	The data field contains a valid data byte belonging to either a user or a control data block.
0	0	0	1	0	The data field contains auxiliary control information that may be used by the terminal adaptor for synchronization purposes.
1	1	1	1	1	Indicates that the data field contains invalid data, which should be ignored.
Other combinations					Reserved for future expansion. Not used by the DSP.

Table 39 Valid values for FID

FID[1]	FRAME TYPE
00	audio frame
01	data frame
1X	reserved

Note

1. Binary value; X = don't care.

Table 40 Downlink data frame format

OFFSET	DATA FIELD								CMD FIELD					INFO FIELD		SYNC FIELD	DESCRIPTION
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0XFF								1	1	1	1	1	0	1	0	Header: to be used by the terminal adaptor for synchronization purposes
1	0XFF								1	1	1	1	1	0	1	0	
2	0XFF								1	1	1	1	1	FID = 01		0	
3 to 21	0XFF								1	1	1	1	1	0	1	0	
22	0X01								0	0	0	1	0	0	1	0	
23	0XFF								1	1	1	1	1	0	1	0	
24	0XFF								1	1	1	1	1	0	1	0	
25	0X00								0	0	0	1	0	0	1	0	
26	0XFF								1	1	1	1	1	1	1	1	User data block. LU is the block length. Valid range: $0 \leq LU \leq 36$.
27	0XFF								1	1	1	1	1	1	1	1	
28	0XFF								1	1	1	1	1	1	1	1	
29	LU								0	0	0	0	1	0	0	1	
30	0XFF								1	1	1	1	1	1	1	1	
	0XFF								1	1	1	1	1	1	1	1	
	U[1]								0	0	0	0	1	1	1	1	
	0XFF								1	1	1	1	1	1	1	1	
	0XFF								1	1	1	1	1	1	1	1	
	U[2]								0	0	0	0	1	0	0	1	
	0XFF								1	1	1	1	1	1	1	1	
	U(LU – 1)								0	0	0	0	1	0	0	1	
	0XFF								1	1	1	1	1	1	1	1	
	0XFF								1	1	1	1	1	1	1	1	
	U(LU)								0	0	0	0	1	0	0	1	
	0XFF								1	1	1	1	1	1	1	1	
	0XFF								1	1	1	1	1	1	1	1	
	LC								0	0	0	0	1	0	0	1	Control data block; LC is the block length. Valid range: $0 \leq LC \leq 8$.
	0XFF								1	1	1	1	1	1	1	1	
	0XFF								1	1	1	1	1	1	1	1	
	C[0]								0	0	0	0	1	0	0	1	
	0XFF								1	1	1	1	1	1	1	1	
	0XFF								1	1	1	1	1	1	1	1	
	C[1]								0	0	0	0	1	0	0	1	
	0XFF								1	1	1	1	1	1	1	1	
	C(LC – 2)								0	0	0	0	1	0	0	1	
	0XFF								1	1	1	1	1	1	1	1	
	0XFF								1	1	1	1	1	1	1	1	
	C(LC – 1)								0	0	0	0	1	0	0	1	
159	0XFF								1	1	1	1	1	1	1	1	

9.1.5.3 Format of uplink data frames

The uplink data frame format is described in Table 43. Each word consists of four fields; these are described in Table 41.

Table 41 Field descriptions

FIELD	DESCRIPTION
DATA	This field contains the data bytes of user data block and control data block. Only words with CMD = 00001 contain valid data fields (see Table 42).
CMD	This field classifies the 16-bit samples as described in the Table 42.
SYNC, INFO	In uplink direction, these fields are without meaning.

Table 42 Classification of the 16-bit samples

CMD FIELD					DESCRIPTION
7	6	5	4	3	
0	0	0	0	1	The data field contains a valid data byte belonging to either a user or a control data block.
0	0	0	1	0	The data field contains auxiliary control information that may be used by the terminal adaptor for synchronization purposes; note 1.
1	1	1	1	1	Indicates that the data field contains invalid data, which should be ignored.
Other combinations					Reserved for future expansion. Not used by the DSP.

Note

1. The external terminal adaptor may insert at any position an arbitrary number of fill words with CMD = 11111.

Table 43 Uplink data frame format

OFFSET	DATA FIELD(1)								CMD FIELD					INFO FIELD		SYNC FIELD	DESCRIPTION
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	X								1	1	1	1	1	X	X	X	User data block; this block contains modified CCITT frame in accordance with *"GSM Rec. 05.03"*. It is used as input data for the channel encoder. LU is the block length Valid range: 0 ≤ LU ≤ 33
	X								1	1	1	1	1	X	X	X	
	LU								0	0	0	0	1	X	X	X	
	U[0]								0	0	0	0	1	X	X	X	
	U[1]								0	0	0	0	1	X	X	X	
	U(LU – 2)								0	0	0	0	1	X	X	X	
	U(LU – 1)								0	0	0	0	1	X	X	X	
	LC								0	0	0	0	1	X	X	X	Control data block; the first byte LC is the block length. LC may also be zero. This block is forwarded to the System Controller. Valid range: 0 ≤ LC ≤ 10.
	C[0]								0	0	0	0	1	X	X	X	
	C[1]								0	0	0	0	1	X	X	X	
	C(LC – 2)								0	0	0	0	1	X	X	X	
	C(LC – 1)								0	0	0	0	1	X	X	X	
159	X								1	1	1	1	1	X	X	X	

Notes

1. X = don't care.

9.1.5.4 User data block formats

In the following sections the user data block formats for all data channels defined in *"GSM Rec. 05.03"* are explained. The formats for uplink and downlink directions are identical with the exception that three additional bytes are transmitted in the downlink direction:

- The first byte contains the facch_flag. This flag indicates whether the channel decoder has decoded a FACCH (facch_flag = 1) or not (facch_flag = 0).
- The other two bytes, rxqual_ber_low and rxqual_ber_high, indicate the estimated Bit Error Rate (BER) at the channel decoder input.

The Bit Error Rate can be calculated using the following equation:

$$BER = \frac{rxqual\_ber\_low + 256 \times rxqual\_ber\_high}{4096}$$

Tables 44 to 47 show the user data block format for full-rate and half-rate data channels running at different baud rates.

Note that the TCH/H4.8 format is used for half-rate data channels at 4.8 kbits/s. It is equivalent to the format used for TCH/F9.6 (see Table 46).

Table 44 TCH/F2.4

The following table shows the user data block for full rate data channel at 2.4 kbit/s (and less). The 2 × 36 data bits shown correspond to 2 modified CCITT V.110 36-bit frames.

DESCRIPTION	OFFSET	DOWNLINK DATA	UPLINK DATA
Block size	0	14	11
Valid flag	1	1	1
Modified CCITT frame 1	2	rb8 to rb1	rb8 to rb1
	3	rb16 to rb9	rb16 to rb9
	4	rb24 to rb17	rb24 to rb17
	5	rb32 to rb25	rb32 to rb25
	6	rb36 to rb33	rb36 to rb33
Modified CCITT frame 2	7	rb8 to rb1	rb8 to rb1
	8	rb16 to rb9	rb16 to rb9
	9	rb24 to rb17	rb24 to rb17
	10	rb32 to rb25	rb32 to rb25
	11	rb36 to rb33	rb36 to rb33
FACCH flag	12	facch_flag	–
rxqual_ber	13	rxqual_ber_low	–
	14	rxqual_ber_high	–

Table 45 TCH/F4.8

The following table shows the user block data format for full rate data channel at 4.8 kbit/s. The 2 × 60 data bits shown correspond to 2 modified CCITT V.110 60-bit frames according to *"GSM 04 21"*.

DESCRIPTION	OFFSET	DOWNLINK DATA	UPLINK DATA
Block size	0	20	17
Valid flag	1	1	1
Modified CCITT frame 1	2	rb8 to rb1	rb8 to rb1
	3	rb16 to rb9	rb16 to rb9
	4	rb24 to rb17	rb24 to rb17
	5	rb32 to rb25	rb32 to rb25
	6	rb40 to rb33	rb40 to rb33
	7	rb48 to rb41	rb48 to rb41
	8	rb56 to rb49	rb56 to rb49
	9	rb60 to rb57	rb60 to rb57
Modified CCITT frame 2	10	rb8 to rb1	rb8 to rb1
	11	rb16 to rb9	rb16 to rb9
	12	rb24 to rb17	rb24 to rb17
	13	rb32 to rb25	rb32 to rb25
	14	rb40 to rb33	rb40 to rb33
	15	rb48 to rb41	rb48 to rb41
	16	rb56 to rb49	rb56 to rb49
	17	rb60 to rb57	rb60 to rb57
FACCH flag	18	facch_flag	–
rxqual_ber	19	rxqual_ber_low	–
	20	rxqual_ber_high	–

Table 46 TCH/F9.6

The following table shows the full rate data channel at 9.6 kbit/s. The 4 × 60 data bits shown correspond to 4 modified CCITT V.110 60-bit frames in accordance with *"GSM 04.21"*. For non-transparent services those four blocks shall align with one 240-bit RLP frame. The valid_flag indicates, whether the data block contains valid data (valid_flag = 1) or not (valid_flag = 0). It is used for DTX.

DESCRIPTION	OFFSET	DOWNLINK DATA	UPLINK DATA
Block size	0	36	33
Valid flag; note	1	1	valid flag
Modified CCITT frame 1	2	rb8 to rb1	rb8 to rb1
	3	rb16 to rb9	rb16 to rb9
	4	rb24 to rb17	rb24 to rb17
	5	rb32 to rb25	rb32 to rb25
	6	rb40 to rb33	rb40 to rb33
	7	rb48 to rb41	rb48 to rb41
	8	rb56 to rb49	rb56 to rb49
	9	rb60 to rb57	rb60 to rb57
Modified CCITT frame 2	10	rb8 to rb1	rb8 to rb1
	11	rb16 to rb9	rb16 to rb9
	12	rb24 to rb17	rb24 to rb17
	13	rb32 to rb25	rb32 to rb25
	14	rb40 to rb33	rb40 to rb33
	15	rb48 to rb41	rb48 to rb41
	16	rb56 to rb49	rb56 to rb49
	17	rb60 to rb57	rb60 to rb57
Modified CCITT frame 3	18	rb8 to rb1	rb8 to rb1
	19	rb16 to rb9	rb16 to rb9
	20	rb24 to rb17	rb24 to rb17
	21	rb32 to rb25	rb32 to rb25
	22	rb40 to rb33	rb40 to rb33
	23	rb48 to rb41	rb48 to rb41
	24	rb56 to rb49	rb56 to rb49
	25	rb60 to rb57	rb60 to rb57
Modified CCITT frame 4	26	rb8 to rb1	rb8 to rb1
	27	rb16 to rb9	rb16 to rb9
	28	rb24 to rb17	rb24 to rb17
	29	rb32 to rb25	rb32 to rb25
	30	rb40 to rb33	rb40 to rb33
	31	rb48 to rb41	rb48 to rb41
	32	rb56 to rb49	rb56 to rb49
	33	rb60 to rb57	rb60 to rb57

DESCRIPTION	OFFSET	DOWNLINK DATA	UPLINK DATA
FACCH flag	34	facch_flag	–
Rxqual_ber	35	rxqual_ber_low	–
	36	rxqual_ber_high	–

Table 47 TCH/H2.4

The following table shows the user data block for half rate data channel at 2.4 kbit/s (and less). The 4 × 36 data bits shown correspond to 4 modified CCITT V.110 36-bit frames according to GSM 04 21.

DESCRIPTION	OFFSET	DOWNLINK DATA	UPLINK DATA
Block size	0	24	21
Valid flag	1	1	1
Modified CCITT frame 1	2	rb8 to rb1	rb8 to rb1
	3	rb16 to rb9	rb16 to rb9
	4	rb24 to rb17	rb24 to rb17
	5	rb32 to rb25	rb32 to rb25
	6	rb36 to rb33	rb36 to rb33
Modified CCITT frame 2	7	rb8 to rb1	rb8 to rb1
	8	rb16 to rb9	rb16 to rb9
	9	rb24 to rb17	rb24 to rb17
	10	rb32 to rb25	rb32 to rb25
	11	rb36 to rb33	rb36 to rb33
Modified CCITT frame 3	12	rb8 to rb1	rb8 to rb1
	13	rb16 to rb9	rb16 to rb9
	14	rb24 to rb17	rb24 to rb17
	15	rb32 to rb25	rb32 to rb25
	16	rb36 to rb33	rb36 to rb33
Modified CCITT frame 4	17	rb8 to rb1	rb8 to rb1
	18	rb16 to rb9	rb16 to rb9
	19	rb24 to rb17	rb24 to rb17
	20	rb32 to rb25	rb32 to rb25
	21	rb36 to rb33	rb36 to rb33
FACCH flag	22	facch_flag	–
Rxqual_ber	23	rxqual_ber_low	–
	24	rxqual_ber_high	–

9.1.6 System Controller interface

The PCF5083 parallel port is used for communication with the P90CL301 System Controller (SC) which is compatible with the 68000 family microcontrollers. Details about interfacing are described in Chapter 10.

The host port of the DSP has three internal registers:

1. PI; 16-bit parallel input register (write-only)
2. PO; 16-bit parallel output register (read-only)
3. PIOS; 5-bit parallel I/O Status/Control register (see Table 50).

The 16-bit words of registers PI and PO are transferred in two access cycles of 8-bits. The LOW byte/HIGH byte selection is controlled with HA0 and with bit 5 of the PIOS register, PLSB. For correct interrupt generation the transfer order should be HA1 and HA0 = 00; then HA1 and HA0 = 01 (see Table 48).

Table 48 Host port register addressing

PLSB	HA1	HA0	DESCRIPTION	STATUS REGISTER PIOS CHANGE
0 (1)	0	0	access PI/PO HIGH (LOW) byte	no change
0 (1)	0	1	access PI/PO LOW (HIGH) byte	PISE = 0 or POSF = 0
X	1	0	reserved	no change
X	1	1	read status register PIOS	no change

Table 49 Status/Control Register (PIOS)

7	6	5	4	3	2	1	0
–	–	–	PLSB	PORQEN	PIRQEN	POSF	PISE

Table 50 Description of PIOS bits

BIT	NAME	DIRECTION	DESCRIPTION
7	–	–	These three bits are not used.
6	–	–	
5	–	–	
4	PLSB	read	This bit controls the parallel transfer order. When PLSB = 1; the LSB is transferred first. The reset value is a logic 1.
3	PORQEN	read/write	When PORQEN = 1; PORQN is enabled. The reset value is a logic 0.
2	PIRQEN	read/write	When PIRQEN = 1; PIRQN is enabled. The reset value is a logic 0.
1	POSF	read	When POSF = 1; the Output Register (PO) is full. The reset value is a logic 0.
0	PISE	read	When PISE = 1; the Input Register (PI) is empty. The reset value is a logic 1.

The host can be used in three modes:

1. **Acknowledge mode:** in this mode the PCF5083 provides an open drain output $\overline{\text{DTACK}}$, that acknowledges data read or write accesses to the host port registers PI, PO or PIOS. This signal has to be connected to the 90CL301 $\overline{\text{DTACK}}$ input. Using the hardware handshake via $\overline{\text{DTACK}}$, the 90CL301 can write data to the PI register at any time. It is not necessary to poll the PISE bit in the status register PIOS. If the 90CL301 writes to PI and PI is still full, the write access is automatically extended until the DSP has read PI. Under worst case conditions this will last 10 µs (see formula below). Before reading a message via PO however, the System Controller has to check once if a message is available from DSP. This is done by polling the POSE flag in the PIOS register. If POSE is a logic 1 the System Controller has to read the first word of the message. After determination of the message length, the rest of the message can be read without further polling.
2. **Polling mode:** in this mode the hardware handshake via $\overline{\text{DTACK}}$ is not used. Before writing a word to PI, the 90CL301 must wait until the PISE flag in the Status Register PIOS is set. Correspondingly, the 90CL301 must wait until the POSE flag in PIOS is set, before reading PO.
3. **Interrupt mode:** in this mode the PCF5083 provides two internal interrupt request signals PIRQN and PORQN. Signal PIRQN (active LOW) corresponds to status register bit PISE (active HIGH) and PORQN (active LOW) to bit POSF (active HIGH). As soon as the status bit PISE or POSF is set, PIRQN/PORQN is going LOW, generating an interrupt at the host. The interrupt service routines should handle the two 8-bit transfers. After the first transfer PIRQN/PORQN goes HIGH, removing the interrupt source. After the second transfer a new interrupt will be generated.
   PIRQN and PORQN can be enabled by setting PIOS bit 2 for PIRQ_EN and bit 3 for PIRQ_EN to HIGH. After reset both signals are disabled. The PIRQN and $\overline{\text{PORQN}}$ interrupt condition is signalled via the $\overline{\text{HIPR\_INT}}$ interrupt line (see Section 10.2).

Command and indication messages are buffered in two queues, each of 139 words. If working in acknowledge mode the layer 1 software in the 90CL301 has to ensure that no queue overflow occurs (this will never happen during normal operation).

The times TPI and TPO required by the DSP to receive or transmit a message consisting of N words can be calculated according to the following formulas:

$TPI = 10\ \mu s + (N - 1) \times 1.5\ \mu s$

$TPO = N \times 1.5\ \mu s$

Data transfer in acknowledge mode produces the least overhead in the 90CL301 layer 1 software. It is therefore recommended to use the acknowledge mode for communication with the DSP.

9.1.7 Event Counter Clock

The event counter is used by the firmware for time-out detection.The 32.768 kHz clock is internally connected to the ECLK input of the DSP.

9.1.8 General Purpose I/O Pins

Table 51 Usage of General Purpose I/O Pins

PIN	RESET DEFAULT	DESCRIPTION
IO1	0	Audio interface of the timer core select pin. A logic 1 enables the interface; a logic 0 disables the interface.
IO2	1	used for procedure trace
IO3	1	used for procedure trace
IO4	1	DTX select pin. A logic 1 enables the transmitter; a logic 0 disables the transmitter.

Note that the IO1 pin is not changed automatically by the DSP firmware (e.g. by the procedure MP_iom2_enable). Whenever audio data should be transmitted via the audio interface, IO1 has to be set explicitly by calling the procedure DB_write_register:

DB_write_register(11, 0x0100, 1) sets the IO1 bit in register SIOC

DB_write_register(11, 0x0100, 2) resets the IO1 bit in register SIOC.

9.1.9 POWER SAVING MODES

9.1.9.1 Idle mode

When operating in Idle mode the DSP enters a dormant state and requires only a fraction of the power normally needed to supply the device in the full operating mode. The processor core is switched off whereas the I/O section of the processor is fully functional. The Idle mode is invoked by the on-chip firmware whenever the DSP is waiting for an I/O event. The DSP automatically leaves the Idle mode as soon as the input or output operation has been completed.

9.1.9.2 Power-down mode

The Power-down mode is initiated when the signal DSPON is deactivated during Sleep mode (see Section 8.3.3). The DSP will stop operation synchronously after a maximum of 3 CLKI cycles delay. All parts of the DSP which operate with the main processor clock are in static state. Only the blocks running with the serial interface clocks are not affected by the Power-down mode. For minimum power consumption the external serial shift clocks should therefore be switched off. The DSP remains in the power-down state as long as the signal DSPON is held inactive. The processor continues its operation for a maximum of 3 clock cycles after the signal DSPON is set active again.

9.2 Message Interface to the System Controller

The DSP can be controlled with commands and joining 16-bits parameters from the System Controller via the host port register PI. The first word always contains the command OPCODE and length. The second word is an arbitrary ID code which is useful for debugging purposes. The following words are command parameters. The DSP can also generate indications giving status information or requested data. These indication messages can be read (R) via host port register PO.

The DMA message is used to download data into the program/data RAM. Download is always done into the data address space. The parameters mc_before and mc_after indicate the value of the Memory Configuration Register before and after download. Thus, it is possible to switch a RAM bank into the data address space, download a program and switch it back afterwards. For more information about the MC Register and the PCF5083 memory mapping please refer to *"Information Manual Digital Signal Processors PCF508x, Philips Semiconductors, 1995"*.

Table 52 Commands/indications to/from the PCF5083

MNEMONIC	DIRECTION	OPCODE[1] bit 15 to bit 8	LENGTH bit 7 to bit 0	ID	DATA
DMA	write	0X0000		msg_id	mc_before n_words; address data [1] to data [n words]; mc_after
EXEC_PROC	write	0X01	3 + npar	msg_id	proc_id; parameter_1 to parameter_N
PROC_RETURN	read	0X11	3 + n_retvals	msg_id	proc_id; return_value 1 to return value_N
PACKET	write	0X02	2 + N (cmd_len)	msg_id	cmd_1 to cmd_N
RESET	write	0X03	3	msg_id	reset_parm
NOP	write	0X05	2 + N	msg_id	data_1 to data_N
ERROR	read	0X12	3	msg_id	error_code

Note

1. X = don't care.

9.2.1 Execution of GSM baseband procedures

The EXEC_PROC commands initiate the execution of internal procedures. The procedure specified by proc_id is executed within the DSP. The input parameters of the procedure are part of the message. The return values (if any) of the procedure and the msg_id parameter are packed to a PROC_RETURN indication.

Several commands can be combined with the PACKET command to reduce overhead especially when sending commands to the DSP in **polling mode**.

9.2.2 No Operation (NOP) command

This NOP command may be used for debugging purposes. It is ignored by the DSP. The length of the data field has to be at least one word.

9.2.3 Soft resetting the DSP

The RESET command causes the DSP to perform a soft reset. It is executed immediately after the current running procedure is completed. Depending on the reset parameter (see Table 53) the input and/or output command queues are cleared. It is possible to reset more than one FIFO or queue, by setting the appropriate bits.

Table 53 Parameter of RESET message

MNEMONIC	VALUE(1)	DESCRIPTION
RESET_ALL	0X0000	Restart main program (soft reset), clear all buffers and queues and all external memory.
OUTPUT_MESSAGE_QUEUE	0X0001	Clear the output message queue.
INPUT_MESSAGE_QUEUE	0X0002	Clear the input message queue.
BBD_IN_FIFO	0X0004	Clear the baseband digitizer input FIFO.
MOD_OUT_FIFO	0X0008	Clear the GMSK modulator output FIFO.

Note

1. X = don't care.

9.2.4 ERROR HANDLING

The ERROR indication notifies the SC that an error has occurred in previously submitted EXEC PROC commands with ID msg_id. Table 54 shows all possible error codes. After the detection of an error, the current command is aborted and the DSP continues execution of the next command in the input queue.

Table 54 Error codes

MNEMONIC	CODE	DESCRIPTION
RESET_OCCURRED	1	the DSP main program restarted
MSG_TYP_UNKNOWN	5	an undefined command was received by the DSP
WRONG_PARAMETER	10	one of the procedure parameters is not in a valid range
MSG_IN_FIFO_OVERFLOW	11	an input queue overflow occurred
MSG_OUT_FIFO_OVERFLOW	12	an output queue overflow occurred
BBD_IN_FIFO_OVERFLOW	13	a BBD FIFO overflow occurred
MOD_FIFO_FULL	14	the modulator FIFO is not empty enough to receive all data
AUDIO_IN_IFO_OVERFLOW	15	an audio input FIFO overflow occurred
AUDIO_OUT_FIFO_UNDERFLOW	16	an audio output FIFO underflow occurred
AUDIO_OUT_FIFO_FULL	17	the audio output FIFO is not empty enough to receive all data
TIMEOUT_BBD_IN_FIFO	20	a time-out occurred waiting for BBD samples
TIMEOUT_AUDIO_IN_FIFO	21	a timeout occurred waiting for audio input samples
AUDIO_SYNC_FAILED	22	the audio synchronization was not successful
AUDIO_SYNC_TIMEOUT	26	MP_audio_sync waited too long for the first BBD sample
FSC_TIMEOUT	27	MP_iom2_enable waited too long for the frame sync interrupt
AUDIO_SAMPLES_INSERTED	28(1)	MP_audio_sync inserted audio samples into the audio FIFO
AUDIO_SAMPLES_REMOVED	29(1)	MP_audio_sync removed audio samples from the audio FIFO
SPEECH_ENCODER_RESET	31(1)	a speech encoder reset occurred
SPEECH_DECODER_RESET	32(1)	a speech decoder reset occurred

Note

1. These error codes do not notify a real error; they indicate the occurrence of a special event.

9.3 GSM baseband procedures

The baseband procedures with optional input parameters can be called by the EXEC_PROC command as described in Section 9.2. Return values are packed in the PROC_RETURN indication. Every procedure deals with the following types of data:

- Input parameters which are directly supplied by the System Controller
- Return values which are automatically sent to the System Controller as soon as the procedure is completed
- Input and output data buffers located in the DSP data RAM. They are used for communication with other procedures. Most of the procedures use a common buffer SCRATCH_BUFF for their input and output data. Only a small number of procedures need specific buffer for input or output. In this case there are one or two additional parameters in_buff_id or out_buff_id which determine the buffers where input and output data are located. In Table 55 a list of all available buffers is given.

For all trailing parameters of a procedure which are not transmitted with the EXEC_PROC command a default value of zero is used.

Table 55 Data buffers for baseband procedures

MNEMONIC	ID[1]	SIZE	DESCRIPTION
VERSION_BUFF	0X8000	10	Contains the BCD coded version numbers of all software packages (order: MP, BB, CI, CM, DB, EM, FB, SP and TP). A version number 0Xmm.ss means version mm.ss.
SCRATCH_BUFF	0X8001	167	Scratch buffer for communication between arbitrary modules.
TCH_CMI_BUFF	0X8002	116	The combination of the 4 buffers; TCH_CMI_BUFF1 to TCH_CMI_BUFF4.
TCH_CMI_BUFF1	0X8003	29	Used to store the CMI values of 4 consecutive bursts belonging to one TCH block.
TCH_CMI_BUFF2	0X8004	29	
TCH_CMI_BUFF3	0X8005	29	
TCH_CMI_BUFF4	0X8006	29	
CCH_CMI_BUFF	0X8007	116	The combination of the 4 buffers; CCH_CMI_BUFF1 to CCH_CMI_BUFF4.
CCH_CMI_BUFF1	0X8008	29	Used to store the CMI values of 4 consecutive bursts belonging to one CCH block.
CCH_CMI_BUFF2	0X8009	29	
CCH_CMI_BUFF3	0X800A	29	
CCH_CMI_BUFF4	0X800B	29	
CCH_INFO_BUFF	0X800C	32	The combination of the 4 buffers; CCH_INFO_BUFF1 to CCH_INFO_BUFF4.
CCH_INFO_BUFF1	0X800D	8	Used to store the information bits 4 bursts belonging to one CCH block.
CCH_INFO_BUFF2	0X800E	8	
CCH_INFO_BUFF3	0X800F	8	
CCH_INFO_BUFF4	0X8010	8	
TCH_LOOP_BUFF	0X8011	82	Used to store four normal bursts during TCH loop-back operation. Note this buffer is also used by the speech encoder.
MP_CONTROL_BUFF	0X8013	6	Used to control several features of the firmware; see Table 56.
IQ_BUFF	0X8018	334	Used to store I and Q components from the PCF5072. This buffer is overlaid with SCRATCH_BUFF.

Notes

1. X = don't care.

The MP_CONTROL_BUFF may be used to control several features of the DSP. It consists of 4 parameter fields as given in Tables 56 and 57.

Table 56 Contents of MP_CONTROL_BUFF

OFFSET	DESCRIPTION
0	time-out_freq: ECLK input frequency divided by 10 kHz. After reset time-out_freq is set to 3 (32.768 kHz clock).
1	eclk_cycle_count: contains number of ECLK cycles spent most recently called procedure. Required for test purposes only.
2 to 4	proc_trace_buff[2]: for debugging purposes the DSP provides a procedure trace facility. The IDs of the procedures to be traced must be stored in proc_trace_buff. If any of these procedures is executing, its corresponding I/O pin (see Table 57) is set to a logic 0.

Table 57 Associated I/O pins

LOCATION	I/O PIN	DEFAULT AFTER RESET
proc_trace_buff[0]	IO2	17 CP_rx_normal_burst
proc_trace_buff[1]	IO3	00 trace errors; note 1

Note

1. If proc_trace_buff[1] is 0, then IO3 is set on errors.

9.3.1 PROCEDURE DESCRIPTION

In this section all baseband procedures offered by the DSP are listed in alphabetical order. The following naming conventions are used throughout the description:

- Value: this is a 16-bit integer parameter (call by value) or return value (e.g. training sequence code, dtx flag)
- Value [SIZE]: this is an array consisting of SIZE 16-bit words. The array is transmitted word by word between the System Controller and the DSP (e.g. FACCH msg[12])
- Parameter names ending with buff_id identify a buffer in the DSP data RAM where input or output data of the procedure is stored.

Table 58 Procedure description

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
BB_access_burst Burst building of a random access burst in accordance with "*GSM Rec. 05.02*". The burst information bits must be located in SCRATCH_BUFF. The result is returned in SCRATCH_BUFF.	1	–	–
BB_normal_burst Burst building of n_bursts normal bursts in accordance with *"GSM Rec. 05.02"*. The burst information bits must be located in the buffer determined by info_buff_id. The result is returned in buffer burst_buff_id. 'tsc' is the training sequence code (range: 0 to 7)	2	info_buff_id burst_buff_id tsc n_bursts	–
CI_decrypt (note 1) Decryption of the CMI values of n_bursts bursts stored in buffer cmi_buff_id. Note that n_bursts may be in the range from 1 to 4. If n_bursts is set to 4, cmi_buff_id **must not** be any other than TCH_CMI_BUFF or CCH_CMI_BUFF	3	cmi_buff_id n_bursts	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
CI_decrypt_init (note 1) Initialization for CI_decrypt. The decrypt_flag enables or disables decryption. decrypt_flag = 0, means no decryption. decrypt_flag = 1, decryption according to A5/1. decrypt_flag = 2, decryption according to A5/2 t1 is absolute Frame Number (FN) divisor 26 × 51 (0 to 2047,11 bits). t2 is absolute Frame Number (FN) modulo 26 (0 to 25, 5 bits) t3 is absolute Frame Number (FN) modulo 51 (0 to 50, 6 bits) key[0 to 3] contains 64 bits of the ciphering key K_c in accordance with *"GSM Rec. 03.20"*. The bits are loaded by the algorithm in LSB first order (first bit = LSB {key[0]}, last bit = MSB {key[3]}). The A8 algorithm delivers 8 bytes kc[0] to kc[7]. The mapping between kc and key is as follows: key[0] = kc[6] << 8; kc[7] key[1] = kc[4] << 8; kc[5] key[2] = kc[2] << 8; kc[3] key[3] = kc[0] << 8; kc[1]	4	decrypt_flag t1 t2 t3 key[4]	–
CI_encrypt Encryption of n_bursts normal bursts, info_buff_id determines the buffer where the information bits of the first burst are stored.	5	info_buff_id n_bursts	–
CI_encrypt_init Initialization for CI_encrypt. The encrypt_flag enables or disables encryption. decrypt_flag = 0, means no encryption. decrypt_flag = 1, encryption according to A5/1. decrypt_flag = 2, encryption according to A5/2. t1 is absolute Frame Number (FN) divisor 26 × 51 (0 to 2047,11 bits). t2 is absolute Frame Number (FN) modulo 26 (0 to 25, 5 bits) t3 is absolute Frame Number (FN) modulo 51 (0 to 50, 6 bits) Key[0 to 3] contains 64 bits of the ciphering key K_c in accordance with *"GSM Rec. 03.20"*. The bits are loaded by the algorithm in LSB first order (first bit = LSB {key[0]}, last bit = MSB {key[3]}). The A8 algorithm delivers 8 bytes kc[0] to kc[7]. The mapping between kc and key is as follows: key[0] = kc[6] << 8; kc[7] key[1] = kc[4] << 8; kc[5] key[2] = kc[2] << 8; kc[3] key[3] = kc[0] << 8; kc[1]	6	encrypt_flag t1 t2 t3 key[4]	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
CM_convert_TCHFS_data This routine is used for the TCH/FS loop-back. It converts the output data of CM_decoder_TCHFS into a format which is required for CM_encoder_TCHS. If bfi_sig_flag is set to logic 1, then the decoded speech parameters are set to zero if a bad frame has been detected.	7	bfi_sig_flag	–
CM_decoder_CCH Channel decoder for control channels. In accordance with *"GSM Rec. 05.03"* this procedure can be used for the following channels: BCCH: Broadcast Control Channel PCH: Paging Channel SACCH: Slow Associated Control Channel AGCH: Access Grant Channel SDCCH: Stand-alone Dedicated Control Channel. The four bursts containing CCH information which are stored in CCH_CMI_BUFF are decoded rxqual_ber reflects the estimated bit error rate at the input of the channel decoder (hard decision assumed) multiplied by 4096. bfi_cch bad frame indication: bfi_cch = 0; the decoded CCH message is OK bfi_cch = 1; a parity error has been detected bfi_cch = 2; a bad metric error has been detected bfi_cch = 3; both parity **and** bad metric errors have been detected. cch_msg[12] contains the CCH message consisting of 184 bits. The bits are stored in a packed format with 16-bits per word and LSB first order. Unused MSBs are set to zero.	8	–	rxqual_ber bfi_cch cch_msg[12]
CM_decoder_SCH Channel decoder synchronization channel. bfi_sch is the bad frame indication: bfi_sch = 0; the decoded SCH message is OK bfi_sch = 1; a parity error has been detected bfi_sch = 2; a bad metric error has been detected bfi_sch = 3; both parity **and** bad metric errors have been detected. sch_msg[2] contains the decoded SCH message consisting of 25 bits. The bits are stored in a packed format with 16-bits per word and LSB first order. Unused bits are set to zero.	9	–	bfi_sch sch_msg[2]

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
CM_decoder_TCHDATA Channel decoder and de-interleaver for data channels and FACCH in accordance with *"GSM Rec. 05.03"*. The CMI values located in TCH_CMI_BUFF are decoded. The decoded bits are stored in SCRATCH_BUFF. The data channel decoder is selected by the call of CM_DECODER_TCHDATA_INIT. rxqual_ber (format 16-bit integer) reflects the estimated bit error rate at the input of the channel decoder (hard decision assumed) multiplied by 4096. bfi_facch is the bad frame indication: bfi_facch = 0; the decoded FACCH message is OK bfi_facch = 1; a parity error has been detected bfi_facch = 2; a bad metric error has been detected bfi_facch = 3; both parity **and** bad metric errors have been detected. The facch_flag indications: facch_flag = 0; indicates that no FACCH message has been received. In this case facch_msg[12] contains zeros. facch_flag = 1; indicates that a FACCH message has been decoded and is returned into facch_msg[12]. The facch_msg[12] contains the 184 bits of the decoded FACCH message. The bits are stored in a packed format with 16-bits per word and LSB first order. Unused MSBs are set to zero.	72	–	rxqual_ber bfi_facch facch_flag facch_msg[12]
CM_decoder_TCHDATA_init Initialization of the CM_decoder_TCHDATA. The parameter data_service may be one of the following values: data_service = 0; full-rate = 9.6 kbits/s data_service = 1; full-rate = 4.8 kbits/s data_service = 2; full-rate ≤ 2.4 kbits/s data_service = 3; half-rate = 4.8 kbits/s data_service = 4; half-rate ≤ 2.4 kbits/s.	73	data_service	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
CM_decoder_TCHFS Channel decoder and de-interleaver for the full-rate speech traffic channel and FACCH in accordance with *"GSM Rec. 05.03"*. The CMI values located in TCH_CMI_BUFF are decoded. The decoded bits are stored in SCRATCH_BUFF. rxqual_ber (format 16-bit integer) reflects the estimated bit error rate at the input of the channel decoder (hard decision assumed) multiplied by 4096. bfi_facch is the bad frame indication: bfi_facch = 0; the decoded FACCH message is OK bfi_facch = 1; a parity error has been detected bfi_facch = 2; a bad metric error has been detected bfi_facch = 3; both parity **and** bad metric errors have been detected. The facch_flag indications: facch_flag = 0; indicates that no FACCH message has been received. In this event facch_msg[12] contains zeros facch_flag = 1; indicates that a FACCH message has been decoded and is returned into facch_msg[12]. The facch_msg[12] contains the 184 bits of the decoded FACCH message. The bits are stored in a packed format with 16-bits per word and LSB first order. Unused MSB's are set to zero.	10	–	rxqual_ber bfi_facch facch_flag facch_msg[12]
CM_decoder_TCHFS_init Initialization of CM_decoder_TCHFS.	11	–	–
CM_encoder_CCH Channel decoder for control channels. In accordance with *"GSM Rec. 05.03"* this procedure can be used for the following channels: SACCH: Slow Associated Control Channel SDCCH: Stand-alone Dedicated Control Channel. The encoded data is stored in CCH_INFO_BUFF. The cch_msg[12] contains the 184 bits of the decoded CCH message. The bits are stored in a packed format with 16-bits per word and LSB first order. Unused MSB's are set to zero.	12	cch_msg[12]	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
CM_encoder_RACH Channel encoder random access channel. The encoded RACH message is stored in SCRATCH_BUFF. bsic contains the 6 bits B(0) to B(5) of the base station identity code in accordance with *"GSM Rec. 05.03"*. B(0) is stored in the LSB (bit 0) of bsic, B(5) in bit 5 of bsic. B(0) = MSB of PLMN colour code, B(5) = LSB of BS colour code. rach_msg[1] contains the RACH message consisting out of 8 bits. The bits are stored in LSB first order. Unused MSBs are set to zero.	13	bsic rach_msg[1]	–
CM_encoder_TCHDATA Channel encoder and interleaver for data channels, FACCH and DTX uplink control. The dtx_flag determines whether discontinuous transmission (DTX) is applied: dtx_flag = 1; DTX is applied dtx_flag = 0; DTX is not applied. DTX is valid only for the encoder for full-rate 9.6 kbits/s and half-rate 4.8 kbits/s. The facch_flag indications: facch_flag = 0; indicates that no FACCH data must be encoded facch_flag = 1; indicates that a FACCH message must be encoded. The facch_msg[12] contains the 184 bits of the FACCH message. The bits are stored in a packed format with 16-bits per word and LSB first order. The return value txen is only useful if DTX is applied. It indicates whether the TCH block will be transmitted over the air interface. txen = 1; TCH block will be transmitted over the air interface txen = 0; TCH block will not be transmitted over the air interface. For data services other than full-rate 9.6 kbits/s and half-rate 4.8 kbits/s txen will be set to logic 1.	74	dtx_flag facch_flag facch_msg[12]	txen
CM_encoder_TCHDATA_init Initialization of CM_ENCODER_TCHDATA. The parameter data_service may be one of the following values: data_service = 0; full-rate = 9.6 kbits/s data_service = 1; full-rate = 4.8 kbits/s data_service = 2; full-rate ≤ 2.4 kbits/s data_service = 3; half-rate = 4.8 kbits/s data_service = 4; half-rate ≤ 2.4 kbits/s.	75	data_service	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
CM_encoder_TCHFS Channel encoder and interleaver for traffic channel full-rate speech and FACCH and DTX uplink control. The dtx_flag determines whether discontinuous transmission (DTX) is applied: dtx_flag = 1; DTX is applied dtx_flag = 0; DTX is not applied. The taf determines whether the current traffic frame is aligned with the SACCH multiframe structure as described in *"GSM Rec. 05.08"*: taf = 0; not aligned with SACCH multiframe structure taf = 1; aligned with SACCH multiframe structure. The facch_flag indications: facch_flag = 0; indicates that no FACCH message need be encoded facch_flag = 1; indicates that a FACCH message must be encoded. The facch_msg[12] contains the 184 bits of the FACCH message. The bits are stored in a packed format with 16-bits per word and LSB first order. The return value txen is only useful if DTX is applied. It indicates whether the TCH block will be transmitted over the air interface. txen = 1; TCH block will be transmitted over the air interface txen = 0; TCH block will not be transmitted over the air interface.	14	dtx_flag taf facch_flag facch_msg[12]	txen
CM_encoder_TCHFS_init Initialization of CM_encoder_TCHFS.	15	–	–
CP_audio_loop Combination of: MP_READ_AUDIO_IN_FIFO (SCRATCH_BUFF, 160, –1); MP_WRITE_AUDIO_OUT_FIFO (SCRATCH_BUFF, 160).	16	–	–
CP_freq_estim Combination of: MP_READ_BBD_IN_FIFO (IQ_BUFF, 167); FB_FREQ_ESTIM (threshold) The fb_freq_estim processes 156 I and Q samples only. 167 samples are read in order to minimize the number of different burst length	81	threshold	fb_qual fb_foi
CP_freq_estim_offset (PCF5083-3) Combination of: MP_READ_BBD_IN_FIFO_INIT (i_offset, q_offset); MP_READ_BBD_IN_INFO (IQ_BUFF, 167); FB_FREQ_ESTIM (threshold).	37	threshold i_offset q_offset	fb_qual fb_foi

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
CP_power measure Combination of: MP_READ_BBD_IN_FIFO (IQ_BUFF, 80); EM_POWER_MEASUREMENT (agc-gain1).	19	agc_gain1	power1
CP_power-measure_offset (PCF5083-3) Combination of: MP_READ_BBD_IN_FIFO (i_offset, q_offset); MP_READ_ BBD_IN_INFO (IQ_BUFF, 80) EM_POWER_MEASUREMENT (agc_gain1).	20	agc_gain1 i_offset q_offset	power1
CP_regenerate_tone_gen Combination of: MP_READ_AUDIO_IN_FIFO (SCRATCH_BUFF, 160, 0XFFFF); DB_FILL_BUFFER (SCRATCH_BUFF, 0, 0X0000, 160); TG_TONE_GEN ( ); MP_WRITE_AUDIO_OUT (SCRATCH_BUFF, 160).	64	–	–
CP_rx_normal_burst Combination of: MP_READ_BBD_IN_FIFO (SCRATCH_BUFF, 149); EM_POWER_MEASUREMENT(agc_gain); EM_NORMAL_BURST (tch_cmi_buff_id, tsc); CI_DECRYPT (tch_cmi_buff_id, 1).	17	tch_cmi_buff tsc agc_gain	power snr toi foi_re foi_im
CP_rx_normal_burst_offset (PCF5083-3) Combination of: MP_READ_BBD_IN_FIFO (i_offset, q_offset); MP_READ_BBD_IN_FIFO (SCRATCH_BUFF, 149); EM_POWER_MEASUREMENT(agc_gain); EM_NORMAL_BURST (tch_cmi_buff_id, tsc); CI_DECRYPT (tch_cmi_buff_id, 1).	38	tch_cmi_buff tsc agc_gain i_offset q_offset	power snr toi foi_re foi_im
CP_rx_SCH Combination of: MP_READ_BBD_IN_FIFO (IQ_BUFF, 167); EM_SYNC_BURST( ); CM_DECODER_SCH( ).	55	–	snr toi foi_re foi_im bfi_sch sch_msg[12]

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
CP_rx_SCH_offset (PCF5083-3) Combination of: MP_READ_BBD_IN_FIFO (i_offset, q_offset); MP_READ_BBD_IN_FIFO (IQ_BUFF, 167); EM_SYNC_BURST( ); CM_DECODER_SCH( ).	39	i_offset q_offset	snr toi foi_re foi_im bfi_sch sch_msg[12]
CP_rx_speech Combination of: CM_DECODER_TCHFS( ); TG_TONE_GEN( ); SP_DECODER_TCHFS (dtx_flag, taf, test_mode); MP_WRITE_AUDIO_OUT_FIFO (SCRATCH_BUFF, 160).	18	dtx_flag taf test_mode	rxqual_ber bfi_facch facch_flag facch_msg[12]
CP_rxlev2 (only in versions PCF5083-1 and PCF5083-2) Combination of: MP_READ_BBD_IN_FIFO (IQ_BUFF, 80); EM_POWER_MEASUREMENT(agc_gain1); MP_READ_BBD_IN_FIFO (IQ_BUFF, 80); EM_POWER_MEASUREMENT(agc_gain2).	20	agc_gain1 agc_gain2	power1 power2
CP_rxlev3 (only in versions PCF5083-1 and PCF5083-2) Combination of: MP_READ_BBD_IN_FIFO (IQ_BUFF, 80); EM_POWER_MEASUREMENT(agc_gain1); MP_READ_BBD_IN_FIFO (IQ_BUFF, 80); EM_POWER_MEASUREMENT(agc_gain2); MP_READ_BBD_IN_FIFO (IQ_BUFF, 80); EM_POWER_MEASUREMENT(agc_gain3).	21	agc_gain1 agc_gain2 agc_gain3	power1 power2 power3
CP_search_fcb_offset (PCF5083-3) Combination of: MP_READ_BBD_IN_FIFO (i_offset, q_offset); FB_search_fcb( ).	21	i_offset q_offset	fb_found fb_toi fb_index
CP_start_TCHFS Combination of: CI_ENCRYPT_INIT (enc_flag, t1, t2, t3, key[4]); CI_DECRYPT_INIT (enc_flag, t1, t2, t3, key[4]); SP_ENCODER_TCHFS_INIT( ); SP_DECODER_TCHFS_INIT( ); CM_ENCODER_TCHFS_INIT( ); CM_DECODER_TCHFS_INIT( ); CI_ENCRYPT (SCRATCH_BUFF, nb); BB_NORMAL_BURST (SCRATCH_BUFF, SCRATCH_BUFF, tsc, nb); MP_IOM2_ENABLE( ); MP_AUDIO_SYNC (tch_frame_no, slip, delta_rx_delay, delta_tx_delay); MP_WRITE_NORMAL_BURST (SCRATCH_BUFF, nb).	78	enc_flag dec_flag t1 t2 t3 key[4] nb tsc slip delta_rx_delay delta_tx_delay	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
CP_tx_CCH Combination of: CM_ENCODER_CCH (cch_msg); CI_ENCRYPT (CCH_INFO_BUFF, 4); BB_NORMAL_BURST (CCH_INFO_BUFF, SCRATCH_BUFF, tsc, 4); MP_WRITE_MOD_OUT_FIFO (SCRATCH_BUFF, 44).	23	tsc cch_msg[12]	–
CP_tx_four_normal_bursts Combination of: CI_ENCRYPT (SCRATCH_BUFF, 4); BB_NORMAL_BURST (SCRATCH_BUFF, SCRATCH_BUFF, tsc, 4); MP_WRITE_MOD_OUT_FIFO (SCRATCH_BUFF, 44).	43	tsc	–
CP_tx_normal_burst Combination of: CI_ENCRYPT (info_buff_id, 1); BB_NORMAL_BURST (SCRATCH_BUFF, SCRATCH_BUFF, tsc, 1); MP_WRITE_MOD_OUT_FIFO (SCRATCH_BUFF, 11).	24	info_buff_id tsc	–
CP_tx_RACH Combination of: CM_ENCODER_RACH (bsic, rach_msg); BB_ACCESS_BURST( ); MP_WRITE_MOD_OUT_FIFO (SCRATCH_BUFF, 11).	25	bsic rach_msg	–
CP_tx_speech Combination of: MP_READ_AUDIO_IN_FIFO (SCRATCH_BUFF, 160, 11); SP_ENCODER_TCHFS (dtx_flag, bypass_flag, test_mode); CM_ENCODER_TCHFS (dtx_flag, taf, facch_flag, facch_msg); CI_ENCRYPT (SCRATCH_BUFF, 4); BB_NORMAL_BURST (SCRATCH_BUFF, SCRATCH_BUFF, tsc, 4); MP_WRITE_MOD_OUT_FIFO (SCRATCH_BUFF, 44).	26	dtx_flag bypass_flag test_mode taf tsc facch_flag facch_msg[12]	txen
DB_call This procedure calls a procedure located at program address proc_addr.	30	proc_addr	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
DB_copy_buffer n_words words are copied within DSP data RAM	27	source_buff_id dest_buff_id source_offset dest_offset n_words	–
DB_compare_info_cmi This procedure may be used to measure bit errors in a received burst. It compares the first n_bits soft outputs (CMIs) of the equalizer located in cmi_buff to the n_bits hard bits located in buffer info_buffer_id and returns the number of errors found (n_errors).	71	info_buff_ptr cmi_buff_ptr n_bits	n_errors
DB_fill_buffer n_words words are filled with fill_value.	28	buff_id buff_offset fill_value n_words	–
DB_pio_test This procedure can be used to test data transfer between the 90CL301 and the PCF5083. With every call, **DB_pio_test** checks if the parameters in_seq[0 to 4] are equal to the following predefined sequences of numbers: in_seq[0] = k × 3 in_seq[1] = k × 5 in_seq[2] = k × 7 in_seq[3] = k × 9 in_seq[4] = k × 11. Where k indicates how often **DB_pio_test** has been previously called (e.g. k = 0 for the first call after reset). The return value n_errors indicates the number of errors found in in_seq[0 to 4] (range 0 to 4). In addition the following predefined output sequences are returned: out_seq[0] = k × 11 out_seq[1] = k × 9 out_seq[2] = k × 7 out_seq[3] = k × 5 out_seq[4] = k × 3.	70	in_seq [0 to 4]	out_seq [0 to 4] n_errors
DB_read_buffer The n_words are read from buffer buff_id starting at offset buff_offset; n_words must not be greater than 19.	29	buff_id buff_offset n_words	buff[n_words]

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
DB_read_register This function may be used to read the contents of a control or shadow register of the DSP. If reg_number is out-of-range, the function returns an error, ERROR_WRONG_PARAMETER. The registers that may be read are given in Table 59	61	reg_number	reg_contents
DB_wait Wait for cycles ECLK cycles.	56	cycles	–
DB_write_buffer n_words are written into buffer buff_id starting at offset buff_offset; n_words must not be greater than 17.	32	buff_id buff_offset n_words data[n_words]	–
DB_write_register This function may be used to write a control or shadow register of the DSP. Dependent on the input parameter action the register reg_number is written with value or the value is interpreted as a mask to set or to clear only specific bits. The procedure disables the interrupts to make sure that nobody else can change the registers. If reg_number is out-of-range or if an attempt is made to set or clear bits in a register, that is only writeable, the function returns an error (ERROR_WRONG_PARAMETER). The registers that may be changed are given in Table 60. The action parameter may be one of following values: action = 0; write register (reg = value) action = 1; set bits (reg ≠ value) action = 2; clear bits (reg ≠ ~value).	62	reg_number value action	–
EM_init This procedure sets the output mode for EM_normal_burst and EM_sync_burst. The output_mode values are defined below: output_mode = 0; the 4th return value contains the frequency offset df, in Hz. output_mode = 1 (default after reset); the 4th return value contains the imaginary part of the frequency offset df.	82	output_mode	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
EM_normal_burst Adaptive viterbi equalizer for normal bursts. The 149 I and Q pairs in IQ_BUFF are demodulated. The parameter cmi_buff_id determines the buffer where the demodulated CMI values should be stored. The following values for cmi_buff_id are allowed: TCH_CMI_BUFFx for sub-block number x of a TCH. CCH_CMI_BUFFx for sub-block number x of a CCH. The parameter tsc determines the training sequence code. Valid range: $0 \leq tsc \leq 7$. The snr is an estimation for the signal-to-noise ratio ($0 \leq snr \leq 255$). The toi denotes the measured time difference (in quarterbits) between the first information bit of the burst and the start of the sampling window. Range: $0 \leq toi \leq 28$. A toi value of 12 is the optimal position. For output_mode = 1; (see EM_init) foi_re and foi_im denote the real and imaginary part of the frequency offset information. The frequency offset df (Hz) can be calculated in accordance with equation: $f_{df} = \frac{foi\_im}{foi\_re \times 663}$ For output_mode = 0; the frequency offset df in Hz is returned instead of foi_im as the 4th return values. It should be noted that the frequency offset output (for both output modes) only contains meaningful information, if foi_re > 450.	34	cmi_buff_id tsc	snr toi foi_re foi_im df
EM_offset_measurement This procedure measures the offset of the complex baseband signal located in IQ_BUFF. The parameter n_samples is the number of complex I and Q samples to be used for averaging; n_samples must be one of the following values: 64 or 128. If n_samples is not specified, then a default value of 128 is used. The i_offset and q_offset is the time averaged value of the complex baseband signal.	79	[n_samples]	i_offset q_offset
EM_power_measurement Power measurement for RXLEV calculation of serving and neighbouring cells. The agc_gain is the gain of the current AGC range in $1/8$ dB. The parameter n_samples is the number of I and Q samples located in IQ_BUFF to be used for averaging; n_samples must be one of the following values: 80 or 144. If the parameter n_samples is not specified, then a default value of 80 is used. The power_dBm is the time averaged value of the complex baseband signal in $1/8$ dBm steps (range: –722+agc_gain to agc_gain).	35	agc_gain [n_samples]	power_dB

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
EM_ sync_burst Adaptive viterbi equalizer for synchronization bursts. The 167 I and Q pairs in IQ_BUFF are demodulated. The demodulated CMI values are also stored in SCRATCH_BUFF. snr is an estimation for the signal-to-noise ratio ($0 \leq snr \leq 255$) The toi denotes the measured time difference (in quarterbits) between the first information bit of the burst and the start of the sampling window. Range: $0 \leq toi \leq 96$. A toi value of 46 is the optimal position. The foi_re and foi_im denote the real and imaginary part of the frequency offset information. The frequency offset df (Hz) can be calculated in accordance with equation: $f_{df} = \frac{foi\_im}{foi\_re \times 663}$	36	–	snr toi foi_re foi_im
FB_freq_estim This procedure performs a frequency measurement by analysing the phase of the 156 IQ samples located in IQ_BUFF. The parameter threshold is the frequency estimation reliability threshold. If it is not specified a default value of 3 will be used. fb_qual = 0; indicates that no FCB has been detected, fb_qual > 0 means that an FCB has been found. The fb_qual may be used as reliability information. The return value fb_foi is the measured frequency offset information in Hertz. fb_foi = received frequency – frequency of local oscillator.	66	[threshold]	fb_qual fb_foi
FB_freq_estim_init This routine initialises all internal counters that are used for averaging by FB_freq_estim and FB_estim_eval. It is not necessary to call FB_freq_estim if averaging via FB_freq_estim_eval is not required.	65	–	–
FB_freq_estim_eval The procedure performs a weighted averaging over all previous results of FB_freq_estim. The parameter threshold is the frequency estimation reliability threshold (recommended value: tbf). fb_flag = 0 indicates that no FCBs have been detected. fb_flag = 1 indicates that at least one FCB has been detected. The return value fb_foi is the measured frequency offset information in Hertz. fb_foi = received frequency – frequency of local oscillator.	67	threshold	fb_flag fb_foi

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
FB_search_fcb This procedure searches for a frequency correction burst (FB) by scanning 9 or more timeslots. FB_search_fcb can be used on 26 or 51-frames multiframe structure. When serving a traffic channel (TCH) the BCCH carrier has to be scanned in the IDLE frames of the 26 multiframe structure using search windows of 9 timeslots. After initialization with FB_search_fcb_init (see below), FB_search_fcb has to be called in up to 11 consecutive IDLE frames. This time period is called an observation interval, containing at least one FB. The 51 multiframe structure is used in cell selection or IDLE mode and on an SDDCH. If search windows of 9 timeslots are used to scan the BCCh carrier, the search must be done by 15 successive calls to FB_search_fcb within the following TDMA frames (N denotes the arbitrary TDMA frame number of the first call): N, N+2, N+4, N+6, N+8, N+11, N+13, N+15, N+17, N+19, N+22, N+24, N+26, N+28, N+30. If the search window is extended to 17 timeslots, the search can be done by 7calls at the frames: N, N+3, N+6, N+9, N+12, N+15, N+18. Values of fb_found are defined below: fb_found = –1; the search has been aborted and no FCB has been found. fb_found = 0; no FB has been found up to now, FB_search_fcb should be called again in the next Idle frame. fb_found = > 0; the search has been successful. fb_found FBs have been found within n_obser_int observation intervals. The return value fb_toi is the start of the FB in bits (1 bit = 3.69 µs) relative to first complex sample of the observation window. The fb_index indicates in which of the previous calls to FB_search_fcb the FB has been actually found. If fb_index is zero, then the FB has been found by fast detection during the current search. The fb_index = –1 means that no FB has been found within the current observation interval, if this is combined with fb_found > 0 the call cannot be located and only fb_toi can be used.	39	–	fb_found fb_toi fb_index

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
FB_search_fcb_init Initialization of FB_search_fcb. This routine has to be called before a new FB search is started. The following parameters are recommended: The parameter len_obser_int indicates how many observation windows belong to an observation interval. The parameter len_obser_int must be set to 11 for a 26-frames and to 15 (or 7) for 51-frames multiframe structure. If the parameter len_obser_int is omitted or set to zero, all successive calls of FB_search_fcb perform only fast FB detection. The FB search algorithm includes a match filter for FB detection. The output of this matched filter is compared with the parameter threshold in order to decide whether an FB has been found or not. If the parameter threshold is omitted (or set to zero respectively) the recommended default value of 400 is used. The parameter hi_threshold is used to perform a fast FB detection under good channel conditions. If the matched filter output exceeds hi_threshold, the FB search is terminated immediately. If hi_threshold is not specified, a default value of 667 is used. The parameter n_samples indicates the length of a search window in bits, i.e. the number of IQ samples. If n_samples is not specified, a default value of 1404 bits is used, corresponding to 9 timeslots. The parameter n_obser_int indicates the number of observation intervals to be used. If the n_obser_int is not specified, a default value of 1 is used.	68	len_obser_int [threshold] [hi_threshold] [n_timeslots] [n_samples] [n_obser_int]	–
MP_audio_sync To start speech procedures in a regular way in full rate traffic channel mode the speech frame timing has to be locked to the TDMA frame timing. Each time a traffic channel is established or switched over (e.g. handover), a new synchronization has to be performed. MP_AUDIO_SYNC has to be started before the receive time slot. The procedure synchronises speech and TDMA frame timing by waiting for the first I and Q pair coming from the BBD and then immediately sets the pointers of audio input and output FIFOs. The parameter slip is normally set to zero indicating that an audio synchronization should be performed. If slip is not equal to zero (valid range 1 to 5), it is checked whether the audio frame timing is still locked to the TDMA frame timing. If the deviation exceeds slip audio samples (125 µs) a resynchronization is performed. The parameter tch_frame_no has to be set to (**fn mod 26**) where fn is the TDMA frame number of the first TDMA frame of the TCH block. The parameters delta_rx_delay and delta_tx_delay are normally set to zero. They may be used to increase or decrease the speech delay in receive and transmit path in 125 µs units, e.g. delta_rx_delay = 1 increases the delay in the RX path by 125 µs. Valid range for delta_rx_delay and delta_tx_delay is –10 to +10. Note that MP_iom2_enable must be called beforehand.	41	tch_frame_no slip delta_rx_delay delta_tx_delay	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
MP_convert_cmi This procedure may be used to make a loopback between equalizer output and burst builder input. It converts the 114 soft outputs (CMIs) of the equalizer located in cmi_buff_id into 114 'hard' bits. These bits are stored in buffer info_buff_id.	22	cmi_buff_id info_buff_id	–
MP_exec_reset This procedure is used to execute a reset synchronous to the input message queue. The difference to the RESET message is, that this procedure is not executed immediately after it is found in the input queue. The reset_action is the same as the one of the RESET message.	60	reset_action	–
MP_if_enough_audio_in_samples This procedure is used for conditional execution of procedures. The following n_procs procedures are executed if the audio input FIFO contains at least n_samples samples, otherwise the procedures are skipped.	42	n_samples n_procs	–
MP_iom2_disable This procedure disables the IOM®-2 interrupts of the DSP. This results in a reduced computational load of the DSP and therefore also in reduced power consumption.	44	–	–
MP_iom2_enable This procedure enables the IOM®-2 interrupts of the DSP. Sending or receiving data over the IOM®-2 interface is only possible if this procedure has been called. After reset the IOM®-2 interrupts are disabled. After the call of MP_iom2_enable the audio FIFOs are initialized as follows: The audio input FIFO contains 1 sample (value = 0xFFFD) and the audio output FIFO contains 148 samples (value = 0xFFFD). This procedure must therefore be called before the MP_AUDIO_SYNC procedure.	45	–	–
MP_offset_compensation This procedure performs offset measurement and compensation. The following function is performed: (i_offset, q_offset) = EM_offset_measurement (n_samples) MP_read_bbd_in_FIFO_init (i_offset, q_offset).	63	–	–
MP_read_audio_in_fifo n_words words from the audio data input FIFO are copied to the buffer buff_id in the DSP data memory. This FIFO collects the audio samples from the ADC converter located in the handset. The procedure waits until the FIFO contains sufficient data. The time-out is expressed in steps of 100 µs. If time-out occurs a TIMEOUT_AUDIO_IN_FIFO error message is automatically sent to the SC.	46	buff_id n_words timeout_val	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
MP_read_bbd_in_fifo ABS(n_samples) I and Q pairs are copied from the baseband digitizer (BBD) input FIFO to the buffer determined by buff_id located in the DSP data RAM. If n_samples is greater than zero the de-rotating and offset compensation is performed while copying. Otherwise no further processing is performed. The procedure waits until the FIFO contains sufficient data. In the event of time_out occurring (10 ms), an ERROR message is sent to the SC.	47	buff_id n_samples	–
MP_read_bbd_in_fifo_init Initialization of MP_read_bbd_in_fifo. The offset values i_offset and q_offset are subtracted from the I and Q components during succeeding calls of **MP_read_bbd_in_fifo**.	58	i_offset q_offset	–
MP_read_data_frame This procedure reads an uplink data frame consisting of framelength (typically 160) words from the audio input FIFO. The format of the uplink data frame is described in Section 9.1.5.3. The user data block is extracted and copied to SCRATCH_BUFF. If the control data block is not empty, the procedure returns the packed control bytes to the SC. The packing method used is most significant bytes first (big endian, 68000 compatible). The procedure waits for timeout × 100 µs for the data frame. If time-out occurs TIMEOUT_AUDIO_IN_FIFO error message is automatically sent to the SC.	76	user_buff_id framelength timeout	n_words n_user_bytes n_ctrl_bytes ctrl_bytes[ ]
MP_set_side_tone The DSP automatically adds the attenuated microphone input signal to the loudspeaker output signal, whereby the 3 LSBs remain unchanged (see Section 9.1.4). The attenuation to be used is described in Table 61.	31	att	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
MP_write_audio_out_fifo The n_words located in buffer buff_id are copied from the DSP data memory into the audio output FIFO. This FIFO collects the samples that have to be sent to the DAC. If the FIFO is not empty enough to receive all samples an ERROR message is sent to the SC.	49	buff_id n_words	–
MP_write_data_frame This procedure generates an output data frame of framelength words (typical 160) as described in Section 9.1.5.2 and writes it into the audio output FIFO. All n_ctrl_bytes control data bytes are unpacked and written to the control data block. If no control bytes are available, only the control data header is transmitted. The channel decoder output data located in buffer user_buff_id are written to the user data block. If the audio output FIFO is not empty enough for framelength samples, an ERROR message is automatically sent to the SC (AUDIO_FIFO_FULL).	77	user_buff_id framelength n_ctrl_bytes ctrl_bytes[ ]	–
MP_write_mod_out_fifo The n_words located in buffer buff_id are copied to the modulator output FIFO. This FIFO collects the samples that have to be transmitted to the GMSK modulator. If the FIFO is not empty enough to receive all samples an ERROR message is automatically sent to the SC.	50	buff_id n_words	–
MP_write_normal_bursts The n_bursts normal bursts located in buffer buff_id are copied to the modulator output FIFO. If the FIFO is not empty enough to receive all samples an ERROR message is automatically sent to the SC.	50	buff_id n_burst	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
SP_decoder_TCHFS GSM full-rate speech decoder as defined in *"GSM Rec. 06.01, 06.10, 06.11, 06.12, 06.31 and 06.32"*. The following tasks are performed: Speech decoding algorithm. Frame repetition and muting, in the event of a Bad Frame Indication (BFI) and/or bad receive quality. SID frame detection and Comfort Noise Insertion (CNI) in the event of discontinuous transmission (DTX). Integrated handsfree algorithm using a weighting balance and comfort noise insertion. The speech parameters in SCRATCH_BUFF are decoded. The audio output data (see Table 32) is returned in SCRATCH_BUFF. The three input parameters determine the operating mode of the speech decoder. The dl_dtx_flag enables DTX in down link when set. Note that the dl_dtx_flag should always be set to 1 except for test purposes. The operation_mode consists of 3 fields: TMODE, HF and ATT. These fields are shown in Table 62. The TMODE field is copied to the audio output data (bits TM0 to TM2 according to Table 36) in accordance with *"GSM recommendation 11.10, section III.1.2.4.7"*. TMODE can take the following values: TMODE = 0; normal operation. TMODE = 1; test of speech decoder. In this test mode an automatic reset of the internal state variables is performed if a rising edge of the RESD bit contained in the audio input data (defined in Table 36) is detected. TMODE = 2; test of speech encoder. TMODE = 4; test of acoustic devices. The HF fields enables (HF = 1) or disables (HF = 0) the handsfree mode of the speech codec. The ATT field has only a meaning in handsfree mode. It informs the handsfree program about the attenuation between loudspeaker an microphone in 3 dB steps. ATT = 0 means 0 dB, ATT = 7 means 21 dB. For proper operation the ATT field has to be adjusted according to the volume control of the loudspeaker. The arrangement of loudspeaker and microphone has to be such that the attenuation at maximum volume level does not exceed 0 dB. The binary taf (time alignment flag) marks with taf = 1 those traffic frames that are aligned with the SACCH multiframe structure defined in *"GSM Rec. 05.08"*.	51	dtx_flag taf operation_mode	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
SP_decoder_TCHFS_init Initialization of SP_decoder_TCHFS.	52	–	–
SP_encoder_TCHFS GSM full-rate speech encoder as defined in *"GSM Rec. 06.01, 06.10, 06.11, 06.12, 06.31 and 06.32"*. The following tasks are performed. Speech encoding algorithm. Voice Activity Detection (VAD) algorithm in the event of discontinuous transmission (DTX). Integrated handsfree algorithm using a weighting balance and comfort noise insertion. The 160 words audio input data in SCRATCH_BUFF (see Table 36) are processed. The encoded speech parameters are returned in SCRATCH_BUFF. The dtx_flag enables or disables DTX as defined below: dtx_flag = 1 enables DTX. dtx_flag = 0 disables DTX. If test_mode = 2 (test of speech encoder) then the RESE bit in SCRATCH_BUFF is checked. If a rising edge is detected, the internal state variables are cleared. If bypass flag = 1; it disables the speech encoder. In this case the parameter bits D1 to D260 (see Table 36) are directly passed to the output. If bypass flag = 2; the speech encoder is only bypassed, if the control flag BM0 (see Table 36) is set to 1 and BM1 is set to 0, otherwise the speech coder is executed. This mode is required for remote interrogation of an external answering machine.	53	dtx_flag test_mode bypass_flag	–
SP_encoder_TCHFS_init Initialization of SP_encoder_TCHFS.	54	–	–
TG_tone_gen This procedures adds a tone consisting of up to 3 sine waves to the audio signal located in SCRATCH_BUFF, whereby the 3 LSB's remain unchanged (see Section 9.1.4). For more information refer to TG_tone_gen_init.	59	–	–

DESCRIPTION	ID	PARAMETERS	RETURN VALUES
TG_tone_gen_init This routine initialises TG_tone_gen. The parameters start_att_inc_factor and start_att_factor indicate how the sine wave starts. Frequency, decay and amplitude factor for each oscillation are set. If one of the sine values is zero the state variables of this oscillation are not set. This can be used to change parameters of the oscillation during tone generation. The input signal is multiplied with the factor ampl_input. The ampl_input is represented in 16-bit fixed-point arithmetic with 14 fractional bits (0X4000 corresponds to 1.0). The parameter start_att is the factor for starting the generated tone softly. Each sample of the generated tone signal is multiplied by start_att. The start_att is multiplied by start_att_inc every sample. Both start_att and start_att_inc are represented in 16-bit fixed-point arithmetic with 14 fractional bits (0X4000 corresponds to 1.0). The parameter start_att_inc is the factor for increment of the start_att_factor and is specified below: 0X4000: start_att_factor is not changed 0X4001 to 0X7FFF: start_att_factor is incremented 0X0000 to 0X3FFF: start_att_factor is decremented. If start_att_inc_factor × start_att_factor is not greater than start_att_factor + 0.5 there is no increment because of rounding. cos_omega_1, cos_omega_2, cos_omega_3 = 32768 cos(Ω) is the value to determine the oscillation frequency of the Nth sinus oscillation $\Omega = 2 \times D \times f/f_S$, where f is the frequency of the oscillation, f_S is the sampling frequency. sin_omega_1, sin_omega_2, sin_omega_3 = 32768 sin(Ω) is the value to determine the amplitude of the oscillation. decay_N = r is the value to determine the decay of the sinus oscillation (r is the pole radius of the generating filter): 0X4000: no decay 0X0001 to 0X3FFF: decay 0X4001 to 0X7FFF: not stable. ampl_sin_1, ampl_sin_2, ampl_sin_3 are the values to determine the amplitude of the sine oscillation.	57	ampl_input start_att start_att_inc cos_omega_1 sin_omega_1 decay_1 ampl_1 cos_omega_2 sin_omega_2 decay_2 ampl_2 cos_omega_3 sin_omega_3 decay_3 ampl_3	–
TG_tone_gen_off This procedures switches off the tone generation. To restart tone generation TG_tone_gen_init has to be called again.	33	–	–

Notes

1. The on-chip firmware does not include the basic ciphering algorithms A5/1 and A5/2, which produce BLOCK1 and BLOCK2 in accordance with *"GSM recommendation 3.20"*. Therefore the firmware only works correctly, if encryption and decryption is switched-off. If ciphering is required, a corresponding software module must be downloaded into the on-chip program RAM. More information will be made available with application notes.

Table 59 Registers that may be read (see Table 58)

REGISTER	
NUMBER	**NAME**
0	pxs0
1	pxs1
2	pys0
3	pys1
4	sas
5	eas
6	dcuc
7	acuc
8	sp
9	iopc
10	iopcx
11	sioc
12	soym
13	iopf
14	eb
15	reserved
16	mc

Table 60 Registers that may be changed (see Table 58)

REGISTER	
NUMBER	**NAME**
0	pxs0
1	pxs1
2	pys0
3	pys1
4	sas
5	eas
6	dcuc
7	acuc
8	sp
9	iopc
10	iopcx
11	sioc
12	soym
13	siyc
14	soyc
15	ecb
16	mc

Table 61 Determination of the attenuation routine (see Table 58); note 1

att	DESCRIPTION
0	no side tone
1	3 dB attenuation
2	6 dB attenuation
3	9 dB attenuation
4	12 dB attenuation
5	15 dB attenuation
6	18 dB attenuation
−1	loop back test microphone to loud speaker

Note

1. After reset att is initialized with zero.

Table 62 Operation_mode fields

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
don't care									ATT			HF	TMODE		

9.3.2 Performance of GSM baseband procedures

The performance of the PCF5083 GSM baseband procedures is specified within this section.

All performances are valid for the following conditions; unless otherwise specified. However, performance figures are only preliminary or must be fixed respectively.

- AGC and quantization in accordance with Fig.16
- Receiver input noise (AWGN); −111 dBm
- IF filter with a frequency characteristic as shown in Fig.20
- Constant frequency offset (df) in baseband signal; −100 Hz ≤ df ≤ 100 Hz
- Gain mismatch in I and Q path less than 0.5 dB
- Phase error less than 2°
- Channel models in accordance with *"GSM Rec. 05.05"*.

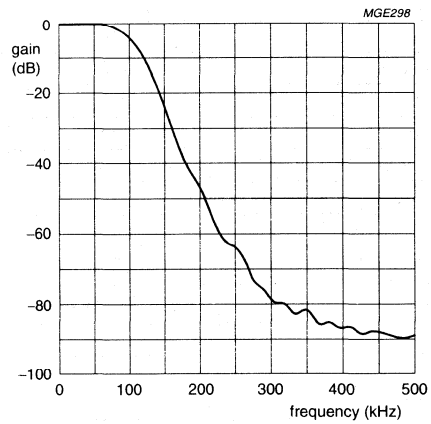


Fig.20 Frequency response of the IF filter.

9.3.2.1 Usable receiver input level range

Table 63 Usable receiver input level range

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
NER1	nominal error rate; TCH/FS class II	static; −10 dBm	2×10^{-5}	–
NER2	nominal error rate; TCH/FS class II	static; −50 dBm	2×10^{-5}	–
NER3	nominal error rate; TCH/FS class II	static; −85 dBm	2×10^{-5}	–
NER4	nominal error rate; TCH/FS class II	EQ50; −40 dBm	2.5	%
NER5	nominal error rate; TCH/FS class II	EQ50; −85 dBm	2.5	%

9.3.2.2 Sensitivity

Table 64 Equalizer and channel decoder sensitivity; note 1

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
FER1	frame erasure rate	static; ideal FH	5×10^{-4}	–
RBER6	residual bit error rate; TCH/FS class Ib	static; ideal FH	0.2	%
RBER7	residual bit error rate; TCH/FS class II	static; ideal FH	0.5	%
FER2	frame erasure rate	TU50; no FH	4.0	%
RBER3	residual bit error rate; TCH/FS class Ib	TU50; no FH	0.2	%
RBER4	residual bit error rate; TCH/FS class II	TU50; no FH	5.0	%
RBER5	residual bit error rate; TCH/FS class II	RA250; no FH	6.0	%
RBER6	residual bit error rate; TCH/FS class II	HT100; no FH	7.0	%
FER3	frame erasure rate; FACCH	TU50; no FH	6.0	%
FER4	frame erasure rate; SCH	TU50; no FH	13.0	%

Note

1. Input level: –102 dBm.

9.3.2.3 Co-channel rejection

Table 65 Equalizer and channel decoder co-channel rejection; note 1

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
FER5	frame erasure rate, TCH/FS	TU3; no FH	15.0 (2.0)	%
RBER7	residual bit error rate; TCF/FS class Ib	TU3; no FH	1.0 (0.1)	%
RBER8	residual bit error rate; TCF/FS class II	TU3; no FH	3.0 (6.0)	%
FER6	frame erasure rate; FACCH	TU3; no FH	18.0	%
FER7	frame erasure rate; SCH	TU50; no FH	14.0	%

Note

1. Signal levels:
   a) Level of wanted signal –85 dBm.
   b) Level of unwanted signal –94 dBm.

9.3.2.4 Erroneous frame indication performance

Table 66 Equalizer and channel decoder erroneous frame indication performance

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
FDR1	false detection rate of FACCH, SACCH or SDCCH	random RF input; level = –95 dBm	tbf	–
FDR2	false detection rate of TCH/FS	random RF input; level = –95 dBm	0.1	%

9.4 Software applications

This section contains examples for several basic GSM channels. For every example the procedures to be executed within the DSP are shown in the form of tables. The first column contains the TDMA frame number fn in which the EXEC_PROC messages should be sent to the DSP. The 2nd column shows the corresponding procedures with all parameters. Parameters in uppercase are constants, lowercase parameters are variables. The 3rd column contains the number words N_W to be transmitted to the DSP within frame fn (PACKET message assumed). The columns RX and MX contain the number of I and Q pairs to be sampled in the receive and monitoring timeslots of TDMA frame fn. Column TX contains the number of bits to sent to the GMSK modulator within the transmit timeslot. The tables are based upon the general rule that an EXEC_PROC message for a procedure that starts execution in TDMA frame n has to be sent in TDMA frame N – 1.

Unless otherwise noted, the corresponding PROC_RETURN message will be available at the latest at the end of TDMA frame N+1, i.e. if the messages are read by the SC at beginning of every TDMA frame, the PROC_RETURN message will be available in frame N + 2. Start and end of a TDMA frame are defined by the falling edge of the $\overline{\text{FRAME\_INT}}$ signal produced by the timer core.

9.4.1 Receiving a CCH block

Table 67 shows how to receive a CCH block and to perform monitoring of two neighbouring cells in parallel. It is assumed that the CCH block has to be received in the frames N to N + 3. Note that the TX timeslot is used for monitoring in this example.

Table 67 Procedures to be started for receiving a CCH block

fn	PROCEDURES[1]	N_W	RX	TX	MX
N – 1	CP_rx_normal_burst (CCH_CMI_BUFF1, tsc, agc_gain1); CP_power_measure (agc_gain2) CP_power_measure (agc_gain3)	15	–	–	–
N	CP_rx_normal_burst (CCH_CMI_BUFF2, tsc, agc_gain1); CP_power_measure (agc_gain2) CP_power_measure (agc_gain3)	15	149	80	80
N + 1	CP_rx_normal_burst (CCH_CMI_BUFF3, tsc, agc_gain1); CP_power_measure (agc_gain2) CP_power_measure (agc_gain3)	15	149	80	80
N + 2	CP_rx_normal_burst (CCH_CMI_BUFF4, tsc, agc_gain1); CM_decoder_CCH( ); CP_power_measure (agc_gain2) CP_power_measure (agc_gain3)	18	149	80	80
N + 3	–	–	149	80	80

Note

1. Procedures to be started via EXEC_PROC in TDMA frame FN.

9.4.2 TRANSMITTING A CCH BLOCK

This example shows how to transmit a CCH block. The transmission is performed in the TDMA frames N to N + 3. Only one message has to be sent in order to transmit a CCH block.

Table 68 Procedures to be started for transmitting a CCH block

fn	PROCEDURES[1]	N_W	RX	TX	MX
N – 1	CP_tx_CCH (tsc, cch_msg)	15	–	–	–
N	–	–	–	156	–
N + 1	–	–	–	156	–
N + 2	–	–	–	156	–
N + 3	–	–	–	156	–

Note

1. Procedures to be started via EXEC_PROC in TDMA frame FN.

9.4.3 FB SEARCH FOR TIMING SYNCHRONIZATION

This example shows how to achieve time synchronization when the mobile is in IDLE mode or is on a channel with a 51 multiframe structure.

Table 69 Procedures to be started for FB search for timing synchronization

fn	PROCEDURES[1]	N_W	RX	TX	MX
N	FB_search_fcb_init(15) FB_search_fcb( )	9	–	–	–
N+11, N+22	FB_search_fcb( )	5	–	–	–
N+1, N+12, N+23		–	–	–	1404
N+2, N+13, N+24	FB_search_fcb( )	5	–	–	
N+3, N+14, N+25		–	–	–	1404
N+4, N+15, N+26	FB_search_fcb( )	5	–	–	
N+5, N+16, N+27		–	–	–	1404
N+6, N+17, N+28	FB_search_fcb( )	5	–	–	
N+7, N+18, N+29		–	–	–	1404
N+8, N+19, N+30	FB_search_fcb( )	5	–	–	
N+9, N+20, N+31		–	–	–	1404
N+10, N+21, N+32		–	–	–	

Note

1. Procedures to be started via EXEC_PROC in TDMA frame FN.

9.4.4 PROCESSING A TCH/FS MULTIFRAME

9.4.4.1 Normal mode

Figure 21 depicts the timing diagram of the procedure execution timing for a TCH/FS multiframe. Table 70 shows the procedures to be executed within the DSP for processing of a TCH/FS multiframe in normal mode. It is assumed that an even numbered time slot is assigned.

Table 70 Procedures to be executed for processing a TCH/FS multiframe in normal mode

FN MOD 26	PROCEDURES	N_W	RX	TX	MX
0	CP_rx_normal_burst (TCH_CMI_BUFF2, tsc, agc_gain) CP_power_measure (agc_gain1) MP_audio_sync(2, 2)	17	149	156	80
4, 13, 17	CP_rx_normal_burst (TCH_CMI_BUFF2, tsc, agc_gain) CP_power_measure (agc_gain1)	12	149	156	80
8	{CM_encoder_CCH (cch_msg[12])}; note 1 CP_rx_normal_burst (TCH_CMI_BUFF2, tsc, agc_gain) CP_rx_normal_burst (CCH_INFO_BUFFi, tsc) CP_power_measure (agc_gain1)	32	149	156	80
21	CP_rx_normal_burst (TCH_CMI_BUFF2, tsc, agc_gain) CI_encrypt (SCRATCH_BUFF1); note 2 CP_power_measure (agc_gain1)	17	149	156	80
1, 5, 9, 14, 18, 22	CP_rx_normal_burst (TCH_CMI_BUFF3, tsc, agc_gain) CP_tx_speech (dtx, bpf, tm, taf, tsc, ff, fm[12]) CP_power_measure (agc_gain1)	33	149	156	80
2, 6, 10, 15, 19	CP_rx_normal_burst (TCH_CMI_BUFF4, tsc, agc_gain) CP_rx_speech (dtx_flag, taf, test_mode) CP_power_measure (agc_gain1)	18	149	156	80
3, 7, 12, 16, 20	CP_rx_normal_burst (TCH_CMI_BUFF1, tsc, agc_gain) CP_power_measure (agc_gain1)	12	149	156	80
11	CP_rx_normal_burst (CCH_CMI_BUFF1, tsc, agc_gain) [CM_decoder_CCH( )]; note 3 CP_power_measure (agc_gain1)	14	149	156	80

FN MOD 26	PROCEDURES	N_W	RX	TX	MX
23 start of FB monitoring	CP_rx_normal_burst (TCH_CMI_BUFF4, tsc, agc_gain) FB_search_FCB_INT (n_int, threshold) FB_search_FCB( ) CP_rx_speech (dtx_flag, taf, test_mode)	22	149	156	80
23 continue FB monitoring	CP_rx_normal_burst (TCH_CMI_BUFF4, tsc, agc_gain) FB_search_FCB( ) CP_rx_speech (dtx_flag, taf, test_mode)	17	149	156	80
23 decode SCh	CP_rx_normal_burst (TCH_CMI_BUFF4, tsc, agc_gain) CP_rx_speech (dtx_flag, taf, test_mode) CP_rx_SCH( )	17	149	156	80
23 level measurement	CP_rx_normal_burst (TCH_CMI_BUFF4, tsc, agc_gain) CP_rxlev3 (agc_gain1, agc_gain2, agc_gain3); note 4 CP_rx_speech (dtx_flag, taf, test_mode)	20	149	156	80
24	CI_decrypt (SCRATCH_BUFF,1); note 5	0	149	156	1404[6] or 167[7]
25	CP_rx_normal_burst (TCH_CMI_BUFF1, tsc, agc_gain) CP_power_measure (agc_gain1)	17	80 or 0	80 or 0	80 or 0

Notes

1. CM_encoder_CCH is only called, if the current multiframe contains the 1st SACCH sub-block.
2. Dummy encryption to increment TDMA frame counters (skip Idle frame).
3. CM_decoder_CCH is only called, if the current multiframe contains the 4th SACCH sub-block.
4. If the BCCh identification of the neighbouring cells is not required in a certain idle frame, then up to 3 level measurements can be performed in that frame.
5. Dummy encryption to increment TDMA frame counter (skip idle frame).
6. Monitoring of a frequency correction burst from a neighbouring cell.
7. Decoding of a synchronization burst from a neighbouring cell.

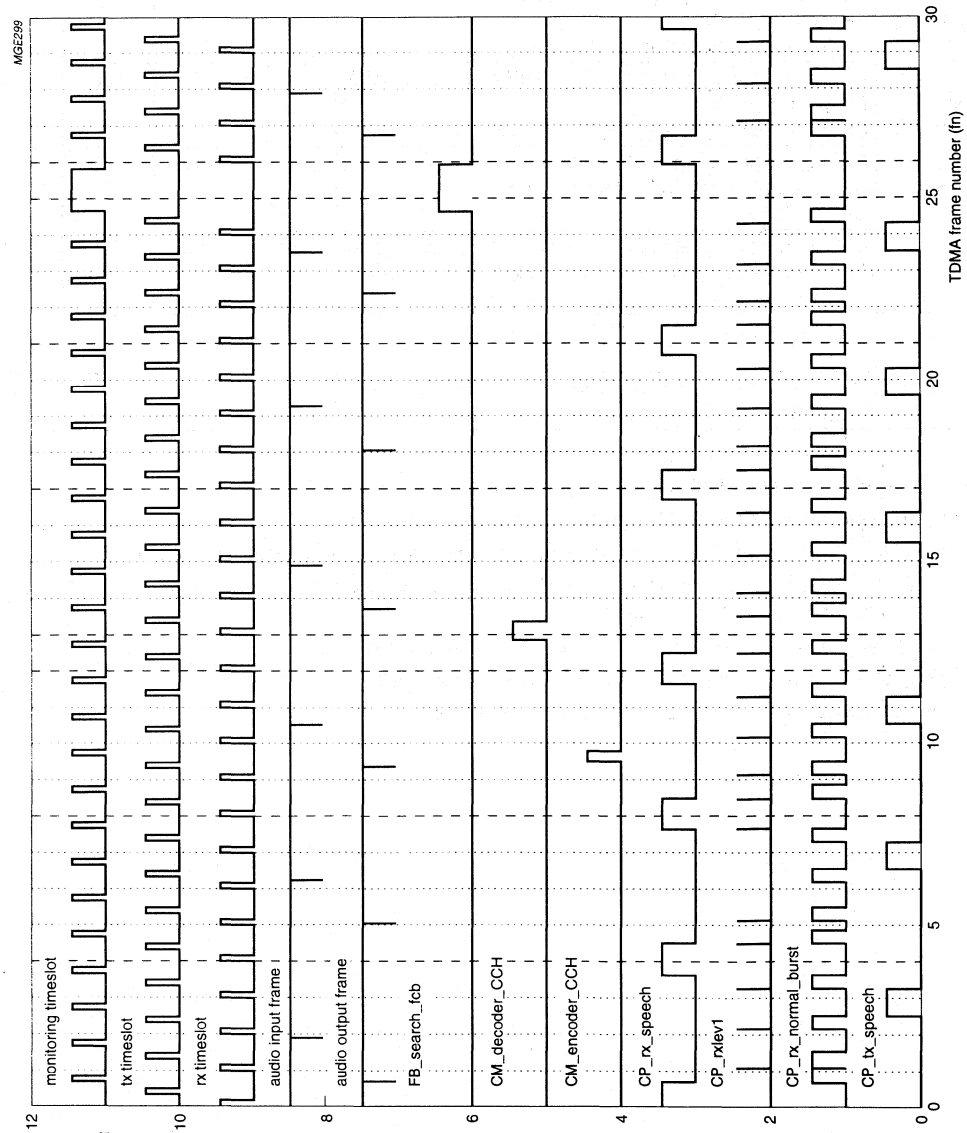


Fig.21 Procedure execution timing for TCH/FS.

9.4.4.2 *Loop-back mode*

During TCH_LOOP mode the CP_TX_SPEECH and CP_RX_SPEECH procedures have to be replaced by the following procedures:

- Replacement for CP_tx_speech:

  MP_read_audio_in_fifo (SCRATCH_BUFF, 160)

  DB_copy_buffer (TCH_LOOP_BUFF, SCRATCH_BUFF, 0, 0, 82)

  CM_convert_tchfs_data(bfi_sig_flag)

  CM_encoder_tchfs(dtx_flag, taf, facch_flag, facch_msg[12])

  CP_tx_four_normal_bursts (tsc)

- Replacement for CP_rx_speech:

  CM_decoder_tchfs( )

  DB_copy_buffer(SCRATCH_BUFF, TCH_LOOP_BUFF, 0, 0, 82)

  DB_fill_buffer(SCRATCH_BUFF, 0, 0, 160)

  MP_write_audio_out_fifo(SCRATCH_BUFF, 160).

9.4.4.3 *Initialization messages for normal mode*

Before the first TDMA frame of a TCH/FS can be processed, several initialization messages have to be sent to the DSP. Initialization is done in 2 DMA frames as shown in Table 72.

The first one or two results of CM_decoder_TCH are based on only partially observed input data, since 8 successive normal bursts are needed due to interleaving.

Table 71 Parameter nb

nb	$t2_s$						
4	0	4	8	13	17	21	25
3	1	5	9	14	18	22	10
2	2	6	–	15	19	23	–
5	3	7	12	16	20	24	–
6	11	–	–	–	–	–	–

Table 72 Initialization messages

TDMA FRAME	EXPLANATION
$FN_s - 2$	In this TDMA frame the message for initialization of speech CODEC, channel CODEC and ciphering are sent to the DSP. Furthermore the modulator out FIFO is filled with the proper number of bursts and synchronization between TDMA frame timing and speech frame timing is performed and the audio interface is enabled by setting the IO1 pin. No data is received or transmitted within this frame.
$FN_s - 1$	In this TDMA frame the EXEC_PROC messages for the procedures processing the data of frame FN_s are sent to the DSP. No data is received or transmitted within this frame.
FN_s	In this TDMA frame the normal processing of receive and transmit data takes place.

Table 73 Initialization procedures

fn	PROCEDURES[1]	N_W	RX	TX	MX
$FN_s - 2$	CP_start_TCHFS (enc_flag, dec_flag, $t1_s$, $t2_s$, $t3_s$, kc[4], nb); notes 2 and 3 DB_write_register (11, 0x0100, 1); set IO1 = 1	21	0	0	0
$FN_s - 1$	The correct value for N_W must be looked-up in Table 70	'...'	0	0	0
FN_s	The correct value for N_W must be looked up in Table 70	'...'	149	164	151

Notes

1. Procedures to be started via EXEC_PROC in TDMA frame FN (TCH/FS normal mode).
2. $t1_s = FN_s$ divided by 26×51;
   $t2_s = FN_s$ modulo 26;
   $t3_s = FN_s$ modulo 51.
3. The parameter nb determines the number of normal bursts to be written into the modulator output FIFO in the initialization frame. It depends on the frame number of the 1st processed frame in accordance with Table 71.

9.4.4.4 Handover mode

Table 74 shows the procedures to be executed within the DSP for processing of a TCH/FS multiframe in Handover mode.

Table 74 Procedures to be executed for processing a TCH/FS multiframe in handover mode

FN MOD 26	PROCEDURES	N_W	RX	TX	MX
0, 4, 13, 17	CP_tx_RACH (bsic, rach_msg) CP_rx_normal_burst (TCH_CMI_BUFF2, tsc, agc_gain) CP_power_measure (agc_gain1)	12	149	156	80
8, 21	CP_tx_RACH (bsic, rach_msg) CP_rx_normal_burst (TCH_CMI_BUFF2, tsc, agc_gain) CI_encrypt (SCRATCH_BUFF,1); note 1 CP_power_measure (agc_gain1)	12	149	156	80
1, 5, 9, 14, 18, 22	CP_tx_RACH (bsic, rach_msg) CP_rx_normal_burst (TCH_CMI_BUFF3, tsc, agc_gain) CI_encrypt (SCRATCH_BUFF, 4) MP_read_audio_in_fifo (SCRATCH_BUFF, 160) CP_power_measure (agc_gain1)	33	149	156	80
2, 6, 10, 15, 19, 23	CP_tx_RACH (bsic, rach_msg) CP_rx_normal_burst (TCH_CMI_BUFF4, tsc, agc_gain) DB_fill_buffer (SCRATCH_BUFF,0,0,160) MP_write_audio_out_fifo (SCRATCH_BUFF, 160) CM_decoder_TCH (dtx_flag, taf, test_mode) CP_power_measure (agc_gain1)	18	149	156	80
3, 7, 12, 16, 20	CP_tx_RACH (bsic, rach_msg) CP_rx_normal_burst (TCH_CMI_BUFF1, tsc, agc_gain) CP_power_measure (agc_gain1)	12	149	156	80
11	CP_tx_RACH (bsic, rach_msg) CP_rx_normal_burst (CCH_CMI_BUFFi, tsc, agc_gain) [CM_decoder_CCH( )]; note 2 CP_power_measure (agc_gain1)	14	149	156	80
24	CP_tx_RACH (bsic, rach_msg) CI_decrypt (SCRATCH_BUFF,1); note 3	15	149	156	80
25	CP_tx_RACH (bsic, rach_msg) CP_rx_normal_burst (TCH_CMI_BUFF1, tsc, agc_gain) CP_power_measure (agc_gain1)	12	–	156	–

Notes

1. Dummy encryption to increment TDMA frame counters (skip Idle + SACCH frame).
2. CM_DECODER_CCH is only called, if the current multiframe contains the 4th SACCH sub-block.
3. Dummy encryption to increment TDMA frame counters (skip Idle frame).

9.4.4.5 Initialization messages for Handover mode

Table 75 shows how a handover from TCH/FS to another TCH/FS has to be processed. 'fn_H' is the first frame transmitted on the new TCH/FS in Handover mode (handover access burst transmitted in uplink). 'fn_S' is the first frame processed in normal mode on the new TCH/FS (normal burst in up link).

Table 75 Initialization procedures for handover mode

fn	PROCEDURES[1]	N_W	RX	TX	MX
.	procedure calls for TCH/FS in normal mode; the correct value for N_W must be looked-up in Table 70.	'...'	149	156	80
.	.	.	.	.	.
.	procedure calls for TCH/FS in normal mode; the correct value for N_W must be looked-up in Table 70.	'...'	149	156	80
.	–	0	149	156	80
$fn_H - 2$	CP_start_TCHFS (enc_flag, dec_flag, $t1_s$, $t2_s$, $t3_s$, kc[4], nb); notes 2 and 3 MP_exec_reset (MOD_OUT_FIFO); DB_write_register(11, 0x0100, 1); set IO1 = 1	21	0	0	0
$fn_H - 1$	procedure calls for TCH/FS in handover mode; the correct value for $N_W$must be looked-up in Table 70.	'...'	0	0	0
fn_H	procedure calls for TCH/FS in handover mode; the correct value for N_W must be looked-up in Table 70.	'...'	149	156	80
.	procedure calls for TCH/FS in handover mode; the correct value for N_W must be looked-up in Table 70.	'...'	149	156	80
$fn_S - 2$	procedure calls for TCH/FS in handover mode BB_normal_burst (SCRATCH_BUFF,SCRATCH_BUFF, tsc, nb)MP_write_normal_bursts (SCRATCH_BUFF, nb); note 3	29	149	156	80
$fn_S - 1$	procedure calls for TCH/FS in normal mode; the correct value for N_W must be looked-up in Table 70.	'...'	149	156	80
fn_S	procedure calls for TCH/FS in normal mode; the correct value for N_W must be looked-up in Table 70.	'...'	149	156	80

Notes

1. Procedures to be started via EXEC_PROC in TDMA frame FN (TCH/FS normal mode).
2. $t1_S = FN_S$ divided by 26×51;
   $t2_S = FN_S$ modulo 26;
   $t3_S = FN_S$ modulo 51.
3. The parameter nb determines the number of normal bursts to be written into the modulator output FIFO in the initialization frame. It depends on the frame number of the 1st processed frame in accordance with Table 71.

9.5 Instruction Set

Details concerning the PCF5083 Instruction Set can be found in the *"PCF5082 Information manual"*. Some exceptions that apply to the PCF5083 are listed below:

- Moves from RAM using pointers to I/O control registers (iopc, iopcx and sioc) are not recommended due to reliability problems. Load immediate from program memory to these registers should be performed. Otherwise, access to the I/O control registers could be performed via secondary registers e.g.

  bm = *px0++ followed by sioc = bm

- All code segments using pp pointer as source must be within a disable/enable pair if interrupts are enabled e.g. disable;

  .....
  bm = *pp++;
  .....

- The instruction *px0++ is illegal. Instead, use the following sequence with consideration to the point above:

  dr = *pp++;
  *px0++ = dr;

- The instruction '.... = *pp++' may be located in any PROM bank (including the mirrored PROM07 at location XF800H to XFFFF0. However, the instruction will not work if located in any of the RAM banks mapped to program address space.

10 MICROCONTROLLER INTERFACE

The PCF5083 includes a standard 68000 compatible microcontroller interface. The interface consists of the lines specified in Table 76.

The 128-byte wide register space of the Timer core is selected if $\overline{\text{HCEN\_T}}$ is asserted. The 4 byte wide register space of the DSP core is selected if $\overline{\text{HCEN\_D}}$ is asserted. The DSP core only uses the address lines HA0 and HA1. All other address lines are don't care for the DSP core.

The Timer core accessed via $\overline{\text{HCEN\_T}}$ does not assert $\overline{\text{DTACK}}$.

Registers wider than 8-bit are aligned on word boundaries with the MSB on the lowest address and the LSB on the highest address. For registers which use only three byte addresses, a reserved address location is provided to make these registers accessible as longwords.

Reserved address locations, write only bits or registers and unused bits within registers are read as zeros and don't care for write operations.

For the DSP Core refer to Section 9.1.6.

Table 76 The Interface signal lines

SIGNAL	DESCRIPTION
HD0 to HD7	8-bit bidirectional data bus.
HA0 to HA6	7-bit unidirectional address bus.
HR/W	Read/write select line. A logic 0, writes to the PCF5083. A logic 1, reads from the PCF5083.
$\overline{\text{HCEN\_T}}$	Chip select line for the Timer core (active LOW).
$\overline{\text{HCEN\_D}}$	Chip select line for the DSP core (active LOW).
$\overline{\text{DTACK}}$	DSP core data acknowledge line (connected to the DTACK input of a 68000 compatible microcontroller.

10.1 Register Set for the Timer Core

Table 77 Register set

OFFSET	REGISTER	SIZE	R/W(1)	DESCRIPTION
00, 01	MODE0_REG	14	R/W	Mode Control Register 0; see Table 78
02, 03	MODE1_REG	14	R/W	Mode Control Register 1; see Table 78
04	RXBURST0_REG	8	W	RXON length in bit
05	RXBURST1_REG	8	W	RXON length in bit
06	RXBURST2_REG	8	W	RXON length in bit
07	TXBURST0_REG	8	W	TXON length in bit
08	TXBURST1_REG	8	W	TXON length in bit
09	TXBURST2_REG	7	W	Start of the Rx burst in QB
0A, 0B	TXSTART_REG	11	W	Start of the TX burst in QB
0C, 0D	MONSTART_REG	13	W	Start of the MON burst in QB
0E, 0F	TXKEY0_REG	10	W	TXKEY0 length in QB
10, 11	TXKEY1_REG	10	W	TXKEY1 length in QB
12	GPON1_REG	6	W	Time of GPON1 getting active in TDMA frames before the end of the Sleep mode

OFFSET	REGISTER	SIZE	R/W[1]	DESCRIPTION
13	GPON2_REG	6	W	Time of GPON2 getting active in TDMA frames before the end of the Sleep mode
14	reserved	–	–	–
15	DSPON_REG	6	W	Time of DSPON getting active in TDMA frames before the end of the Sleep mode
16	REFON_REG	6	W	Time of (N)REFON getting active in TDMA frames before the end of the Sleep mode
17	PDRX1_REG	5	W	Time of PDRX1 getting active in 32 QB before RXON active
18	PDRX2_REG	5	W	Time of PDRX2 getting active in 32 QB before RXON active
19	PDTX1_REG		W	Time of PDTX1 getting active in 32 QB before TXON active
1A	PDTX2_REG		W	Time of NPDTX2 getting active in 32 QB before TXON active
1B	PDBIAS_REG		W	Time of PDBIAS getting active in 32 QB before TXON active
1C	PDSYN_REG		W	Time of PDSYN getting active in 32 QB before RXON/TXON active
1D	AGCSTART_REG		W	Time of DACON_REG to be sent in 32 QB before RXON active
1E	PDDELAY_REG	6	W	PDTX1, NPDTX2 and PDSYN inactive to TXKEY1 inactive delay in QB
1F	KEYOFF_REG	6	W	TXKEY2 inactive to TXKEY1 inactive delay in QB
20, 21	KEYON2_REG	9	W	TXKEY2 active to TXON active delay in QB
22, 23	KEYON1_REG	9	W	TXKEY1 active to TXON active delay in QB
24, 25	POL_REG	14	R/W	Polarity of Power-Down Control Lines; see Table 79
26, 27	MASK_REG	15	R/W	Bit mask register for Power-Down Control Lines; see Table 80
28	QBCCTRL_REG	8	R/W	Quarterbit counter control register; see Table 81
29	SQBCINC_REG	8	R	Sleep quarterbit counter increment
	STOP_REG	8	W	Stop OFF-Timer with data value A5H
2A, 2B	QBC_REG	15	R	QBC access for synchronization
		13	W	R: read 15-bit quarterbit counter (1/4 QB resolution) W: write 13-bit synchronization value (1 QB resolution)
2C, 2D	SLEEPCNT_REG	9	W	Number of TDMA frames to sleep
	FRAMECNT_REG	9	R	Duration of last Sleep mode period in TDMA frames
2E, 2F	HWCTRL_REG	11	R/W	Hardware Control Register; see Table 82
30 to 3F	–	–	R/W	Real Time Clock registers; see Table 83
3E	reserved	–	–	–
3F to 41	RX_REG	17	W	RF Bus: RX frequency
42	reserved	–	–	–
43 to 45	TX_REG	17	W	RF Bus: TX frequency
46	reserved	–	–	–
47. to 49	MON_REG	17	W	RF Bus: MON frequency
4A	reserved	–	–	–
4B to 4D	RXGAIN_REG	18	W	RF Bus: RX gain
4E	reserved	–	–	–
4F to 51	TXGAIN_REG	18	W	RF Bus: Gain setting for a MON burst during the TX timeslot

OFFSET	REGISTER	SIZE	R/W[1]	DESCRIPTION
52	reserved	–	–	–
53 to 55	MONGAIN_REG	18	W	RF Bus: MON gain
56, 57	DAC0_REG	16	W	Gain DAC value 0
58, 59	DAC1_REG	16	W	Gain DAC value 1
5A, 5B	DACON_REG	16	W	Gain DAC power-up value
5C, 5D	DACOFF_REG	16	W	Gain DAC power-down value
5E	reserved	–	–	–
5E to 61	IMCIN_REG	21	R	IMC data in
	IMCOUT_REG	28	W	IMC data out
62	MSB_REG	4	R/W	Gain Control Channel MSB Register 0: DAC0_REG bit 16 1: DAC1_REG bit 16 2: DACON_REG bit 16 3: DACOFF_REG bit 16
63	RFCTRL0_REG	8	W	RF bus control register 0
64	RFCTRL1_REG	8	W	RF bus control register 1
65	RFCTRL2_REG	8	W	RF bus control register 2
66	RFCTRL3_REG	8	W	RF bus control register 3
67	COMBINT_REG	6	R/W	Combined interrupt register; see Table 84
68	HIPRINT_REG	8	R/W	High priority interrupt register; see Table 85
69	HIPRMASK_REG	8	R/W	High priority interrupt mask register; see Table 86
6A	SIINT_REG	6	R	Serial interface interrupt register; see Table 87
6B	SIMASK_REG	5	R/W	Serial interface interrupt mask register; see Table 88
6C, 6D	IOMCON_REG[2]	16	R/W	IOM®-2 interface configuration register; see Table 89
6E, 6F	ACON_REG	13	R/W	Audio Interface configuration register; see Table 90
70	RXD_REG	8	R	RS232 data input register
	TXD_REG	8	W	RS232 data output register
71	MON0_REG	8	R/W	IOM®-2 interface monitor 0 data register
72	MON1_REG	6	R/W	IOM®-2 interface monitor 1data register
73	CI0_REG	6	R/W	IOM®-2 interface C/I 0 data register
74	CI1_REG	6	R/W	IOM®-2 interface C/I 1 data register
75	IOMFLAG_REG	8	R	IOM®-2 interface interrupt flag register; see Table 91
76	IOMCTRL_REG	8	R/W	IOM®-2 interface control register; see Table 92
77	IOMEN_REG	8	R/W	IOM®-2 interface interrupt enable register, see Table 93
78	PORTDATA_REG	6	R/W	Parallel port data register; see Table 94
79	PORTDDIR_REG	6	R/W	Parallel port data direction register; see Table 95
7A	SYSCON_REG	7	R/W	System configuration register; see Table 96

Notes

1. R = read only; W = write only; R/W = read and write.
2. The flags of register IOMCON_REG should not be changed as long as the interface is enabled with CLOCK_MODE = 0 to prevent an unpredictable behaviour of the interface.

Table 78 Mode Control Registers 0 and 1

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	RECRX	Generate the Rx burst timing	0	–
1	R/W	RECTX	Generate the MON burst timing during the TX timeslot	0	–
2	R/W	RECMON	Generate the MON burst timing	0	–
3	R/W	RECON	Generate the idle frame timing	0	–
4	R/W	SEND	Generate the TX burst timing	0	–
5	R/W	DTX	Enable DTX mode	0	–
6	R/W	RXLENGTH0	Select RXLENGTHx_REG for the Rx burst	0	–
7	R/W	RXLENGTH1		0	–
8	R/W	MONLENGTH0	Select RXLENGTHx_REG for the MON burst	0	–
9	R/W	MONLENGTH1		0	–
10	R/W	TXLENGTH	Select TXLENGTHx_REG for the TX burst	0	–
11	R/W	RXCAL	Generate the RX calibration timing	0	–
12	R/W	DISFRAMEINT	Disable the frame interrupt	0	–
13	R/W	USEMODE	Select MODEx_REG for the next frame	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 79 Polarity Register (Power-Down Control Lines)

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	PDRX1	Enable line has default polarity if its corresponding bit is a logic 0. Enable line has inverse default polarity if its corresponding bit is a logic 1.	0	–
1	R/W	PDRX2		0	–
2	R/W	NPDTX2		0	–
3	R/W	PDSYN		0	–
4	R/W	TXKEY1		0	–
5	R/W	TXKEY2		0	–
6	R/W	RXON		0	–
7	R/W	TXON		0	–
8	R/W	BEN		0	–
9	R/W	GPON1		0	–
10	R/W	GPON2		0	–
11	R/W	REFON		0	–
12	R/W	DSPON		0	–
13	R/W	NREFON		0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–'denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 80 Bit mask register (Power-Down Control Lines)

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	PDRX1	A logic 1 enables the control line. A logic 0 disables the control line, output level determined with corresponding output polarity flag	1	–
1	R/W	PDRX2		1	–
2	R/W	(N)PDTX1, (N)PDBIAS		1	–
2	R/W	NPDTX2		1	–
3	R/W	PDSYN		1	–
4	R/W	TXKEY1		1	–
5	R/W	TXKEY2		1	–
6	R/W	RXON		1	–
7	R/W	TXON		1	–
8	R/W	BEN		1	–
9	R/W	GPON1		1	–
10	R/W	GPON2		1	–
11	R/W	REFON		1	–
12	R/W	DSPON		1	–
13	R/W	NREFON		1	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 81 Quarterbit Counter Control Register

Bit	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	SYNC	Enable SYNC mode	0	–
1	R/W	INSERT	Enable INSERT mode	0	–
2	R/W	EXTRACT	Enable EXTRACT mode	0	–
3	R/W	SLEEP	Enable Sleep mode	0	–
4	R/W	SLEEPRED	Enable Reduced Sleep mode	0	–
5	R/W	CAL	Start Sleep mode calibration procedure	0	–
6	R/W	FSCEXT	Enable IOM®-2 FSC period extension mode	0	–
7	R/W	FSCRED	Enable IOM®-2 FSC period reduction mode	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 82 Hardware Control Register

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	AUXON_LH[2]	HWCTRL_INT activated from LOW-to-HIGH transition of input AUXON	–	0
1	R/W	AUXON_HL[2]	HWCTRL_INT activated from HIGH-to-LOW transition of input AUXON	–	0
2	R/W	ONKEY[2]	HWCTRL_INT activated from ONKEY input	–	0
3	R/W	LOWVOLT[2]	HWCTRL_INT activated from $\overline{LOWVOLT}$ input	–	0
4	R/W	CLOCK[2]	HWCTRL_INT activated from real time clock	–	0
5	R/W	ALARM[2]	HWCTRL_INT activated from alarm time match	–	0
6	R/W	SWOFF	Set to logic 1 for mobile switch off operation	0	0
7	R/W	SECINT	Select the real time clock interrupt to appear every second or every minute	0	0
8	R/W	SETCLOCK	Set to logic 1 to enable the real time clock to be set	0	0
9	R/W	MMIREQ[2]	HWCTRL_INT activated from a MMI controller service request via input MMIREQ	–	0
10	R/W	MMICLK	A logic 1 enables the MMI controller clock output (MMICLK)	1	1

Notes

1. $\overline{RSTx}$ = 0 means reset condition if $\overline{RSTO}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.
2. To clear these interrupt flags, the corresponding location has to be written with a logic 1.

Table 83 Real Time Clock registers

OFFSET	R/W	SYMBOL	SIZE	DESCRIPTION	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
30	R/W	SEC_REG	7	RTC: seconds	–	00
31	R/W	MIN_REG	7	RTC: minutes	–	00
32	R/W	HOUR_REG	6	RTC: hours	–	00
33	R/W	DAY_REG	3	RTC: day	–	00
34	R/W	DATE_REG	6	RTC: date	–	01
35	R/W	MONTH_REG	5	RTC: month	–	01
36	R/W	YEAR_REG	8	RTC: year	–	00
37	R/W	SEC_A_REG	7	RTC alarm function: seconds	–	–
38	R/W	MIN_A_REG	7	RTC alarm function: minutes	–	–
39	R/W	HOUR_A_REG	6	RTC alarm function: hours	–	–
3A	R/W	DAY_A_REG	3	RTC alarm function: day	–	–
3B	R/W	DATE_A_REG	6	RTC alarm function: date	–	–
3C	R/W	MONTH_A_REG	5	RTC alarm function: month	–	00
3D	R/W	YEAR_A_REG	8	RTC alarm function: year	–	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 84 Combined Interrupt Register

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R	HWCTRL_INT	HWCTRL_INT interrupt was activated.	–	–
1	R	IOM_INT	IOM_INT interrupt was activated.	–	–
2	R	SI_INT	SI_INT interrupt was activated.	–	–
3	R/W	HWCTRL_MASK	Enable the HWCTRL_INT interrupt to assert the $\overline{COMB\_INT}$ interrupt line.	0	–
4	R/W	IOM_MASK	Enable the IOM_INT interrupt to assert the $\overline{COMB\_INT}$ interrupt line.	0	–
5	R/W	SI_MASK	Enable the SI_INT interrupt to assert the $\overline{COMB\_INT}$ interrupt line.	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 85 High Priority Interrupt Register

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	RX_INT[2]	Assert the $\overline{HIPR\_INT}$ interrupt line when the RX_REG is sent via the RF Bus.	0	–
1	R/W	RXTX_INT[2]	Assert the $\overline{HIPR\_INT}$ interrupt line when the TX_REG is sent via the RF Bus prior to a MON burst in the TX timeslot.	0	–
2	R/W	TX_INT[2]	Assert the $\overline{HIPR\_INT}$ interrupt line when the TX_REG is sent via the RF Bus prior to a TX burst.	0	–
3	R/W	MON_INT[2]	Assert the $\overline{HIPR\_INT}$ interrupt line when the MON_REG is sent via the RF Bus.	0	–
4	R/W	AS_INT1[2]	Assert the $\overline{HIPR\_INT}$ interrupt line when the DACOFF_REG is sent via the RF Bus.	0	–
5	R/W	FRAME_INT[2]	Assert the $\overline{HIPR\_INT}$ interrupt line at the beginning of every TDMA frame.	0	–
6	R	PIRQN_INT	Assert the $\overline{HIPR\_INT}$ interrupt line if the DSP core host port input request is active.	0	–
7	R	PORQN_INT	Assert the $\overline{HIPR\_INT}$ interrupt line if the DSP core host port output request is active.	0	–

Notes

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.
2. To clear these interrupt flags, the corresponding location has to be written with a logic 1.

Table 86 High priority interrupt mask register

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	RX_MASK	Enable the RX_INT flag to assert the $\overline{HIPR\_INT}$ interrupt line.	0	–
1	R/W	RXTX_MASK	Enable the RXTX_INT flag to assert the $\overline{HIPR\_INT}$ interrupt line.	0	–
2	R/W	TX_MASK	Enable the TX_INT flag to assert the $\overline{HIPR\_INT}$ interrupt line.	0	–
3	R/W	MON_MASK	Enable the MON_INT flag to assert the $\overline{HIPR\_INT}$ interrupt line.	0	–
4	R/W	AS_MASK	Enable the AS_INT flag to assert the $\overline{HIPR\_INT}$ interrupt line.	0	–
5	R/W	FRAME_MASK	Enable the FRAME_INT flag to assert the $\overline{HIPR\_INT}$ interrupt line.	0	–
6	R/W	PIRQN_MASK	Enable the PIRQN_INT flag to assert the $\overline{HIPR\_INT}$ interrupt line.	0	–
7	R/W	PORQN_MASK	Enable the PORQN_INT flag to assert the $\overline{HIPR\_INT}$ interrupt line.	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 87 Serial Interface Interrupt Register

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R	IMC_OBE	RF Bus IMC channel output buffer empty.	0	–
1	R	IMC_IBF	RF Bus IMC channel input buffer full.	0	–
2	R	TXD_OBE	RS232 interface output buffer empty.	0	–
3	R	RXD_IBF	RS232 interface input buffer full.	0	–
4	R	EXT_IOM	External IOM®-2 interface request.	0	–
5	R	PAR_ERR	RS232 interface parity error.	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 88 Serial Interface Interrupt Mask Register

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	IMC_OBE_MASK	Enable the IMC_OBE flag to assert the SI_INT interrupt condition.	0	–
1	R/W	IMC_IBF_MASK	Enable the IMC_IBF flag to assert the SI_INT interrupt condition.	0	–
2	R/W	TXD_OBE_MASK	Enable the TXD_OBE flag to assert the SI_INT interrupt condition.	0	–
3	R/W	RXD_IBF_MASK	Enable the RXD_IBF flag to assert the SI_INT interrupt condition.	0	–
4	R/W	EXT_IOM_MASK	Enable the EXT_IOM flag to assert the SI_INT interrupt condition.	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 89 IOM®-2 Interface Configuration Register

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	IOMEXT_EN	Set to a logic 1 to enable the external IOM®-2 interface	0	–
1	R/W	IOMEXT_INV	Set to a logic 1 to invert the external IOM®-2 lines	0	–
2	R/W	CLOCK_MODE0	Select the IOM®-2 clock mode	0	–
3	R/W	CLOCK_MODE1		0	–
4	R/W	CLOCK_MODE2		0	–
5	R/W	DATA_MODE	Select the IOM®-2 data mode.	0	–
6	R/W	MASTER0_EN	Set to a logic 1 to enable the IOM®-2 master unit 0	0	–
7	R/W	MASTER1_EN	Set to a logic 1 to enable the IOM®-2 master unit 1	0	–
8	R/W	MASTER0_TS0	Select the IOM®-2 timeslot for the IOM®-2 master unit 0	0	–
9	R/W	MASTER0_TS1		0	–
10	R/W	MASTER0_TS2		0	–
11	R/W	MASTER0_TS3		0	–
12	R/W	MASTER1_TS0	Select the IOM®-2 timeslot for the IOM®-2 master unit 1	0	–
13	R/W	MASTER1_TS1		0	–
14	R/W	MASTER1_TS2		0	–
15	R/W	MASTER1_TS3		0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 90 Audio Interface Configuration Register

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	TX_EN	Set to a logic 1 to enable the Voice Port transmit section	0	–
1	R/W	TX_DEST	Select Voice Port transmit section data port	0	–
2	R/W	RX_EN	Set to a logic 1 to enable the Voice Port receive section	0	–
3	R/W	RX_SOURCE	Select Voice Port receive section data port	0	–
4	R/W	TX_SLOT0	Select IOM®-2 timeslot for the Voice Port transmit section	0	–
5	R/W	TX_SLOT1		0	–
6	R/W	TX_SLOT2		0	–
7	R/W	TX_SLOT3		0	–
8	R/W	RX_SLOT0	Select IOM®-2 timeslot for the Voice Port receive section	0	–
9	R/W	RX_SLOT1		0	–
10	R/W	RX_SLOT2		0	–
11	R/W	RX_SLOT3		0	–
12	R/W	TRANS_EN	Set to a logic 1 to enable the Voice Port transparent mode	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 91 IOM®-2 Interface Interrupt Flag Register

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R	MON0_IBF	Monitor master 0 input buffer full	0	–
1	R	MON0_OBE[2]	Monitor master 0 output buffer empty	0(1)	–
2	R	MON1_IBF	Monitor master 1 input buffer full	0	–
3	R	MON1_OBE[2]	Monitor master 1 output buffer empty	0(1)	–
4	R	CI0_IBF	C/I channel master 0 input buffer full	0	–
5	R	CI0_OBE[2]	C/I channel master 0 output buffer empty	0(1)	–
6	R	CI1_IBF	C/I channel master 1 input buffer full	0	–
7	R	CI1_OBE[2]	C/I channel master 1 output buffer empty	0(1)	–

Notes

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.
2. These flags change from '0' to '1' after the IOM®-2 interface was enabled with CLOCK_MODE = 0 and MASTERx_EN = '0' after the state machined of the monitor/CI master units are in an initial state.

Table 92 IOM®-2 Interface Control Register

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	TABORT0	Monitor master 0 transmit abort request	0	–
1	R/W	TABORT1	Monitor master 1 transmit abort request	0	–
2	R	RABORT0	Monitor master 0 receive abort request	0	–
3	R	RABORT1	Monitor master 1 receive abort request	0	–
4	R/W	TEOM0	Monitor master 0 transmit end of message	0	–
5	R/W	TEOM1	Monitor master 1 transmit end of message	0	–
6	R	REOM0	Monitor master 0 receive end of message	0	–
7	R	REOM1	Monitor master 1 receive end of message	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 93 IOM®-2 Interface Interrupt Enable Register

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R/W	MON0_IBF_EN	Enable the MON0_IBF flag to assert the IOM_INT interrupt condition.	0	–
1	R/W	MON0_OBE_EN	Enable the MON0_OBE flag to assert the IOM_INT interrupt condition.	0	–
2	R/W	MON1_IBF_EN	Enable the MON1_IBF flag to assert the IOM_INT interrupt condition.	0	–
3	R/W	MON1_OBE_EN	Enable the MON1_OBE flag to assert the IOM_INT interrupt condition.	0	–
4	R/W	CI0_IBF_EN	Enable the CI0_IBF flag to assert the IOM_INT interrupt condition.	0	–
5	R/W	CI0_OBE_EN	Enable the CI0_OBE flag to assert the IOM_INT interrupt condition.	0	–
6	R/W	CI1_IBF_EN	Enable the CI1_IBF flag to assert the IOM_INT interrupt condition.	0	–
7	R/W	CI1_OBE_EN	Enable the CI1_OBE flag to assert the IOM_INT interrupt condition.	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 94 Parallel Port Data Register

BIT	R/W	SYMBOL	OPERATION	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0 to 5	R/W	PIO0_DATA to PIO5_DATA	PIO0 to PIO5 input or output data	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 95 Parallel Port Data Direction Register

BIT	R/W	SYMBOL	OPERATION	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	R	PIO0_DDIR	reserved	0	–
1 to 5	R/W	PIO1_DDIR to PIO5_DDIR	A logic 1 selects the port as an output. A logic 0 selects the port as an input.	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

Table 96 System Configuration Register (SYSCON)

BIT	R/W	SYMBOL	OPERATION (if bit is set)	$\overline{RST}$ = 0	$\overline{RSTx}$ = 0[1]
0	W	CLK13M	Disable the CLK13M output pin.	0	–
1	W	CLK20M	Disable the CLK20M output pin.	0	–
2	W	CLK32K	Disable the CLK32K output pin; PCF5083-2B and PCF5083-2C only.	0	–
		CLK26M	Disable the CLK26M output pin; PCF5083-3A only.	0	–
3	W	DSP_CLK0	These two bits select the DSP core input clock.	0	–
4	W	DSP_CLK1		0	–
5	W	RS232_CLK	Select the external clock for the RS232 interface	0	–
6	R	LOCK	When a logic 1, the PLL is out of lock. When a logic 0, the PLL is in lock.	0	–

Note

1. $\overline{RSTx}$ = 0 means reset condition if either $\overline{RSTO}$ or $\overline{RSTC}$ is asserted; '–' denotes not affected from reset line. During reset ($\overline{RST}$, $\overline{RSTO}$, $\overline{RSTC}$) only those registers with an explicitly given reset value are affected. All other registers are undefined and have to be set by the controller.

10.2 Interrupt Logic

The PCF5083 provides three active LOW interrupt lines: $\overline{\text{FRAME\_INT}}$, $\overline{\text{COMB\_INT}}$ and $\overline{\text{HIPR\_INT}}$ for use with the microcontroller. These interrupt lines are described in Table 97.

Table 97 Interrupt lines

INTERRUPT	DESCRIPTION
$\overline{\text{FRAME\_INT}}$	This output generates an interrupt at the beginning of every TDMA frame. The interrupt is deactivated with an access to register MODE0_REG.
$\overline{\text{COMB\_INT}}$	This output combines three different interrupts: HWCTRL_INT: indicates all interrupts from the on/off monitor, MMI power-down unit and the real time clock. All these interrupt sources are encoded in register HWCTRL_REG IOM_INT: indicates all interrupts from the IOM®-2 interface encoded in registers IOMFLAG_REG and IOMCTRL_REG. Enable flags for this interrupt source are provided in register IOMEN_REG. SI_INT: indicates all interrupts from the RF-IC bus interface and the RS232 interface encoded in register SIINT_REG. Enable flags for this interrupt source are provided in register SIMASK_REG. The register COMBINT_REG contains an interrupt flag and an enable flag for each of the three interrupts. The interrupt flags are inactive if none of their corresponding interrupt conditions is active and enabled.
$\overline{\text{HIPR\_INT}}$	This outputs combines some high priority interrupt sources derived from the RF-IC bus trigger signals generated from the timing generator, from the TDMA frame interrupt and the host port of the DSP core. The register HIPRINT_REG holds flags for each interrupt condition and the register HIPRMASK_REG the corresponding interrupt enable flags. For further details refer to Section 10.1

11 RESET

The PCF5083 has three asynchronous, active LOW reset inputs: $\overline{\text{RSTO}}$, $\overline{\text{RSTC}}$ and $\overline{\text{RST}}$.

$\overline{\text{RSTO}}$ resets the ON/OFF monitor. $\overline{\text{RSTC}}$ the real time clock unit. For a proper reset, $\overline{\text{RSTO}}$ and $\overline{\text{RSTC}}$ have to be asserted until the 32.768 kHz oscillator has stabilized.

$\overline{\text{RST}}$ controls all other parts of the PCF5083. $\overline{\text{RST}}$ is connected to the system reset. For a proper reset, $\overline{\text{RST}}$ has to be asserted for at least 62.5 ms.

After powering-up the PCF5083 all reset lines $\overline{\text{RSTO}}$, $\overline{\text{RSTC}}$ and $\overline{\text{RST}}$ must be asserted to achieve a defined state of the IC.

The DSP core reset is driven via the general purpose parallel port bit 0. After an external reset via $\overline{\text{RST}}$, this port pin is set to a logic 0. The DSP core is therefore set into the reset state.

12 JTAG TEST INTERFACE

The PCF5083 JTAG interface is used to increase testability at board level. The interface is implemented in accordance with IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture.

The interface signals are specified in Table 98 and the operations supported by the interface are given in Table 99.

Table 98 JTAG test interface signals

SIGNAL	DESCRIPTION
TRSTN	Test Reset, active LOW input. This signal resets the internal TAP controller and the state of the boundary-scan cells. It must be pulled LOW during normal operation to ensure that the boundary scan circuitry does not influence the application logic.
TCK	Test Clock input.
TMS	Test Mode Select input. This signal controls the internal state machine of the TAP controller.
TDI	Test Data Input to shift in instructions and data are applied to the boundary-scan circuitry.
TDO	Test Data Out. While shifting in data at the port TDI, data in also shifted out serially at this pin. The instruction register and the data registers are always connected between TDI and TDO.

Table 99 Operations supported by the JTAG-circuitry

INSTRUCTION	BINARY CODE	DESCRIPTION OR VALUE
EXTEST	00000	Refer to IEEE standard
ACUTEST[1]	00001	Test mode for IC production
CONTEST[1]	00010	Test mode for IC production
DCUTEST[1]	00011	Test mode for IC production
IOTEST[1][1]	00100	Test mode for IC production
FCTTEST[1]	00101	Test mode for IC production
SFTTEST[1]	00110	Test mode for IC production
FCTTESTV[1]	00111	Test mode for IC production
SAMPLE/PRELOAD	01000	Refer to IEEE standard
RESET[1]	10000	Generate a synchronous reset for the DSP core
GO[1]	10001	Restart the DSP core at 0x0000 after the RESET instruction
HIGH-Z	10010	Sets all 3-state pins in their high impedance state; TDI, TDO equal to BYPASS
CLAMP	10011	Pins like EXTEST. TDI, TDO equal to BYPASS
NMI[1]	10100	Generate a NMI to the DSP core
–	10110	Reserved
–	10111	Reserved
TESTIN[1]	11000	Select the test input register TI
TESTOUT[1]	11001	Select the test output register TO
STATUS	11010	Select the status register
IDCODE[2]	11101	0001 0101110110000110 00000010101 1 (PCF5083-1)
		0010 0101110110000110 00000010101 1 (PCF5083-2)
		0011 0101110110000110 00000010101 1 (PCF5083-3)
BYPASS[3]	Others	Refer to IEEE standard

Notes

1. For all DSP core specific instructions refer to [1].
2. This instruction is always captured in the state Capture_IR of the TAP controller.
3. This instruction is loaded into the instruction register in the state Reset of the TAP-controller.

Table 100 Boundry Scan Chain

NO.	SIGNAL	I/O	3-STATE CONTROL
TDI			
1	REFON	output	105
2	DCLK	input	
3	$\overline{\text{RSTP}}$	input	
4	CLKSEL	input	
5	CKI	input	
6	cki_enable	output	note 1
7	$\overline{\text{HCEN\_T}}$	input	
8	IO1	output	9
9	io1_enable	output	
10	IO1	input	
11	IO2	output	12
12	io2_enable	output	
13	IO2	input	
14	IO3	output	15
15	io3_enable	output	
16	IO3	input	
17	IO4	output	18
18	io4_enable	output	
19	IO4	input	
20	HA0	input	
21	HA1	input	
22	HA2	input	
23	HA3	input	
24	HA4	input	
25	HA5	input	
26	HA6	input	
27	hd_enable	output	
28	HD0	output	27
29	HD0	input	
30	HD1	output	27
31	HD1	input	
32	HD2	output	27
33	HD2	input	
34	HD3	output	27
35	HD3	input	
36	HD4	output	27
37	HD4	input	
38	HD5	output	27
39	HD5	input	
40	HD6	output	27
41	HD6	input	
42	HD7	output	27
43	HD7	input	
44	HR/W	input	
45	$\overline{\text{HCEN\_D}}$	input	
46	$\overline{\text{DTACK}}$ (_enable)	output	46; note 2
47	SIXCLK	input	
48	SIXEN	input	
49	SIXD	input	
50	SOXCLK	input	
51	SOXEN	input	
52	SOXD	output	53
53	soxd_enable	output	
54	CLK20M	output	105
55	$\overline{\text{FRAME\_INT}}$ (_enable)	output	55; note 2
56	$\overline{\text{COMB\_INT}}$ (_enable)	output	56; note 2
57	$\overline{\text{HIPR\_INT}}$ (_enable)	output	57; note 2
58	CLK13M	output	105
59	AFS	input	60
60	afs_enable	output	
61	AFS	output	
62	ACLK	output	63
63	aclk_enable	output	
64	ACLK	input	
65	ADI	input	
66	ADO	output	103
67	TSCK1	input	

NO.	SIGNAL	I/O	3-STATE CONTROL
68	TSCK2	input	
69	TCE	input	
70	PIO1	input	
71	PIO1	output	72
77	pio1_enable	output	
73	PIO2	input	
74	PIO2	output	75
75	pio2_enable	output	
76	PIO3	input	
77	PIO3	output	78
78	pio3_enable	output	
79	PIO4	input	
80	PIO4	output	81
81	pio4_enable	output	
82	PIO5	input	
83	PIO5	output	84
84	pio5_enable	output	
85	BEN	output	103
86	TXON	output	103
87	RXON	output	103
88	PDRX1	output	103
89	PDRX2	output	103
90	PDTX1	output	103
91	NPDTX1	output	103
92	NPDTX2	output	103
93	PDBIAS	output	103
94	NPDBIAS	output	103
95	PDSYN	output	103
96	TXKEY1	output	103
97	TXKEY2	output	103
98	DSPEN	input	
99	TIMEN	input	
100	$\overline{\text{RSTC}}$	input	
101	$\overline{\text{RSTO}}$	input	
102	ONKEY	input	
103	gpon1_enable	output	
104	CLK32I	input	
105	powon_enable	output	

NO.	SIGNAL	I/O	3-STATE CONTROL
106	AUXON	input	
107	$\overline{\text{LOWVOLT}}$	output	
108	POWON	output	
109	NPOWON	output	
110	$\overline{\text{RST}}$	input	
111	CLK32K; note 3	output	105
	CLK26M; note 4		
112	TXD (_enable)	output	112; note 2
113	RXD	input	
114	$\overline{\text{MMIEN}}$ (_enable)	output	114; note 2
115	MMIREQ	input	
116	MMICLK	output	105
117	FSC	input	
118	FSC	output	119
119	fsc_dcl_enable	output	
120	DCL	input	
121	DCL	output	119
122	DU	input	
123	DD (_enable)	output	123; note 2
124	RFCLK	output	103
125	RFEN1	output	103
126	RFEN2	output	103
127	RFEN3	output	103
128	RFEN4	output	103
129	RFDI	input	
130	RFDO	output	103
131	RFE	output	103
132	NREFON	output	105
133	GPON1	output	105
TDO			
134	GPON1 (_enable)	output	134; note 2

Notes

1. H: enable CKI pad to scan cell; L: CKI reads High.
2. Open-drain output.
3. PCF5083-2B and PCF5083-2C versions only.
4. PCF5083-3 only.

13 TEST AND EMULATION MODES

The PCF5083 supports two test and emulation modes which make all internal signals of the DSP or Timer core externally available. These test modes are selected with either DSPEN = 1 and TIMEN = 0, or DSPEN = 0 and TIMEN = 1.

More information on these test modes will be made available with application notes. Ask your local sales office about the status of these application notes.

14 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+5.0	V
V_I	input voltage on any pin with respect to ground (V_{SS})	−0.5	V_{DD} + 0.5V	V
I_I	sink current into any pin	−20	+20	mA
P_{tot}	total power dissipation	−	800	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C

Notes

1. Stresses above those listed under Maximum Absolute Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on 125 °C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltage larger than the rated maxima.

15 DC CHARACTERISTICS

T_{amb} = −40 to +85 °C; V_{DD} = 3.3 V ±10%.

SYMBOL	PARAMETER[1]	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		2.7	3.0	3.6	V
I_{DD}	operating supply current	all sections operating; Timer active, DSP encoding speech; note 2				
	$I_{(VDD2)}$ + $I_{(VDDPLL)}$		−	40	50	mA
	$I_{(VDD1)}$	note 3	−	8	−	mA
I_{DDtot}	$I_{(VDD2)}$ + $I_{(VDDPLL)}$ + $I_{(VDD1)}$		−	48	−	mA
$I_{DD(SLP)}$	supply current Sleep mode	Timer sleeping, DSP inactive				
	$I_{(VDD2)}$ + $I_{(VDDPLL)}$		−	250	500	µA
	$I_{(VDD1)}$	note 3	−	340	−	µA
$I_{DD(SLP)tot}$	$I_{(VDD2)}$ + $I_{(VDDPLL)}$ + $I_{(VDD1)}$		−	590	−	µA

SYMBOL	PARAMETER[1]	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(STBY)}$	supply current Standby mode	ON/OFF logic and RTC active				
	$I_{(VDD2)} + I_{(VDDPLL)}$		–	15	100	µA
	$I_{(VDD1)}$	note 3	–	245	–	µA
$I_{DD(STBY)tot}$	$I_{(VDD2)} + I_{(VDDPLL)} + I_{(VDD1)}$		–	260	–	µA
All inputs except CK32I, CKI and Schmitt trigger inputs						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	LOW level sink current without pull-down resistor	$V_{IN} = 0$	–	–	1	µA
I_{IH}	HIGH level source current with pull-down resistor	$V_{IN} = V_{DD}$	40	150	250	µA
I_{ZL}	3-state output leakage current	$V_O = 0$ to V_{DD}	–	–	1	µA
All outputs						
V_{OL}	LOW level output voltage		–	–	0.4	V
V_{OH}	HIGH level output voltage (except open-drain outputs)		$0.8V_{DD}$	–	–	V
I_{LI}	open-drain output leakage current	$V_O = 0$ to V_{DD}	–	–	1	µA
CMOS Schmitt trigger inputs						
V_{IL}	LOW level input voltage		0	–	$0.25V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.75V_{DD}$	–	V_{DD}	V
V_{HYS}	Hysteresis		–	0.7	–	V
CK32I						
I_{IL}	LOW level sink current	$V_{IN} = 0$; CK32O open	–	–	1	µA
I_{IH}	HIGH level source current	$V_{IN} = V_{DD}$; CK32O open	–	–	1	µA
C_{in}	input capacitance		–	20	–	pF
g_m	32 kHz oscillator transconductance	CK32I = CK32O = $0.6V_{DD}$	5	–	25	µS
CKI						
V_{IN}	input voltage swing	DC bias = $0.35V_{DD}$ (internally generated)	0.7	–	$V_{DD} - V_{SS}$	V

Notes

1. V_{DD1} = pad ring power supply; V_{DD2} = core power supply and V_{DDPLL} = analog PLL power supply.
2. Current consumption during active speech encoding is measured and then derated by 0.8 to reflect activity level during one cycle.
3. I_{DD1} is estimated with a 30 pF load on each output.

16 AC CHARACTERISTICS

T_{amb} = −40 to +85 °C; V_{DD} = 3.3 V ±10%; see notes 1 to 4.

NO	PARAMETER	MIN.	TYP.	MAX.	UNIT
13 MHz clock timing (see Figs 22 and 24; note 5)					
1	CKI HIGH time	20	–	–	ns
2	CKI LOW time	20	–	–	ns
3	CKI frequency ($1/t_{13}$)	–	13	–	MHz
4	CLK13M HIGH to CKI HIGH delay	–	30	–	ns
5	CLK13M LOW to CKI LOW delay	–	30	–	ns
6	MMICLK HIGH to CKI HIGH delay	–	30	–	ns
7	MMICLK LOW to CKI LOW delay	–	30	–	ns
–	PLL lock time with respect to $\overline{\text{RSTP}}$ HIGH	–	–	50	µs
32 kHz clock timing (see Figs 25 and 26; note 6)					
3	CLK32K frequency	–	32.768	–	kHz
26 MHz clock timing (see Fig.23; notes 5 and 7)					
1	CLK26M HIGH time	5	–	–	ns
2	CLK26M LOW time	5	–	–	ns
3	CLK26M frequency	–	26	–	MHz
DSP and RS232 clock timing (see Figs 27 and 28; note 6)					
1	DCLK frequency; note 8	–	–	39	MHz
2	DCLK HIGH time	10	–	–	ns
3	DCLK LOW time	10	–	–	ns
4	External RS232 Interface clock frequency - 19200 Baud (provided via ADI and selected with SYSCON_REG[RS232_CLK] = 1)	–	11.0592	–	MHz
5	External RS232 Interface clock HIGH time	–	90.4	–	ns
6	External RS232 Interface clock LOW time	–	90.4	–	ns

NO	PARAMETER	MIN.	TYP.	MAX.	UNIT
Host Interface timing (see Figs 29 and 30)					
1	HR/W setup time to $\overline{\text{HCEN}}$ LOW	5	–	–	ns
2	HA0 to HA6 setup time to $\overline{\text{HCEN}}$ LOW	5	–	–	ns
3a	HD0 to HD7 setup time ($\overline{\text{HCEN\_T}}$)	t_{13}	–	–	ns
3b	HD0 to HD7 setup time ($\overline{\text{HCEN\_D}}$)	10	–	–	ns
4	HD0 to HD7 hold time after $\overline{\text{HCEN}}$ HIGH	10	–	–	ns
5	HR/W hold time after $\overline{\text{HCEN}}$ HIGH	5	–	–	ns
6	HA0 to HA6 hold time after $\overline{\text{HCEN}}$ HIGH	10	–	–	ns
7a	$\overline{\text{HCEN}}$ pulse width ($\overline{\text{HCEN\_T}}$)	$3t_{13}$	–	–	ns
7b	$\overline{\text{HCEN}}$ pulse width ($\overline{\text{HCEN\_D}}$)	$2t_{dclkout} + 20$	–	–	ns
8[9]	$\overline{\text{DTACK}}$ LOW delay time, DSP write cycle	–	30	–	ns
9	$\overline{\text{DTACK}}$ HIGH delay time, DSP read cycle; note 3	–	40	–	ns
10[10]	$\overline{\text{DTACK}}$ LOW delay time, DSP read cycle	–	30	–	ns
11	$\overline{\text{DTACK}}$ LOW to data valid; note 11	–	35	50	ns
12	$\overline{\text{DTACK}}$ HIGH delay time, DSP read cycle; note 3	–	40	–	ns
13a	HD0 to HD7 valid after $\overline{\text{HCEN}}$ LOW ($\overline{\text{HCEN\_T}}$)	–	–	$3t_{13}$	ns
13b	HD0 to HD7 valid after $\overline{\text{HCEN}}$ LOW ($\overline{\text{HCEN\_T}}$)	–	–	45	ns
14	HD0 to HD7 3-state after $\overline{\text{HCEN}}$ HIGH	–	–	30	ns
RF Device Control Bus timing - Mode 0 (see Fig.31; note 12)					
1	RFEN1 to RFEN4 setup time to RFCLK LOW	–	$4t_{13}$	–	ns
2	RFEN1 to RFEN4 hold time after RFCLK HIGH	–	$2t_{13}$	–	ns
3	RFCLK HIGH time	–	$6t_{13}$	–	ns
4	RFCLK LOW time	–	$6t_{13}$	–	ns
5	RFDO setup time to RFCLK HIGH	–	$10t_{13}$	–	ns
6	RFDO hold time after RFCLK HIGH	–	$2t_{13}$	–	ns
7[7]	RFDI setup time to RFCLK HIGH	70	–	–	ns
RF Device Control Bus timing - Mode 1 (see Fig.32; note 12)					
1	RFEN1 to RFEN4 setup time to RFCLK HIGH	–	$4t_{13}$	–	ns
2	RFEN1 to RFEN4 hold time after RFCLK LOW	–	$2t_{13}$	–	ns
3	RFCLK LOW time	–	$6t_{13}$	–	ns
4	RFCLK HIGH time	–	$6t_{13}$	–	ns
5	RFDO setup time to RFCLK HIGH	–	$4t_{13}$	–	ns
6	RFDO hold time after RFCLK LOW	–	$2t_{13}$	–	ns
7[7]	RFDI setup time to RFCLK LOW	70	–	–	ns

NO	PARAMETER	MIN.	TYP.	MAX.	UNIT
RF Device Control Bus timing - Mode 2 (see Fig.33; note 12)					
1	RFEN1 to RFEN4 setup time to RFCLK HIGH	–	$4t_{13}$	–	ns
2	RFEN1 to RFEN4 hold time after RFCLK LOW	–	$14t_{13}$	–	ns
3	RFCLK LOW time	–	$6t_{13}$	–	ns
4	RFCLK HIGH time	–	$6t_{13}$	–	ns
5	RFDO setup time to RFCLK HIGH	–	$4t_{13}$	–	ns
6	RFDO hold time after RFCLK LOW	–	$2t_{13}$	–	ns
7(7)	RFDI setup time to RFCLK LOW	70	–	–	ns
8	RFE setup time to RFEN1 to RFEN4 LOW	–	$6t_{13}$	–	ns
Baseband Interface timing (DSP Core X_Port) (see Fig.34)					
1	SIXEN setup to SIXCLK HIGH	5	–	–	ns
2	SIXD setup to SIXCLK HIGH	5	–	–	ns
3	SIXD hold time after SIXCLK HIGH	10	–	–	ns
4	SIXEN hold time after SIXCLK HIGH	10	–	–	ns
5	SIXCLK frequency	–	13	–	MHz
6	SIXCLK LOW time	20	–	–	ns
7	SIXCLK HIGH time	20	–	–	ns
8	SOXEN setup time to SOXCLK LOW	20	–	–	ns
10	SOXD hold time after SOXCLK LOW	–	–	40	ns
11	SOXEN hold time after SOXCLK LOW	10	–	–	ns
12	SOXD 3-state after SOXEN HIGH	–	–	20	ns
13	SOXCLK frequency	–	0.27	13	MHz
14	SOXCLK LOW time	20	1800	–	ns
15	SOXCLK HIGH time	20	1800	–	ns
IOM -2 Interface timing (see Figs 35 and 36)					
1(7)	DD hold time after DCL HIGH	–30	–	30	ns
2a(13)	DCL cycle time	–	$8.5t_{13}$	–	ns
2b(13)	DCL cycle time	–	$8t_{13}$	–	ns
2c(13)	DCL frequency	–	4.096	–	MHz
3(7)	FSC hold time after DCL HIGH	–30	–	30	ns
4(7)	DU setup time to DCL LOW	50	–	–	ns
5(7)	DU hold time after DCL LOW	50	–	–	ns
6(13)(7)	DCL HIGH time	75	–	–	ns
7(13)(7)	DCL LOW time	75	–	–	ns

NO	PARAMETER	MIN.	TYP.	MAX.	UNIT
Voice Port timing - non-transparent mode (see Fig.37 and note 14)					
1[7]	AFS setup time to ACLK HIGH	200	–	–	ns
2[7]	AFS hold time after ACLK LOW	10	–	–	ns
3[7]	ADO hold time after ACLK HIGH		–	30	ns
4[7]	ADI setup time to ACLK LOW	30	–	–	ns
5[7]	ADI hold time to ACLK LOW	40	–	–	ns
6[7]	ACLK frequency	–	–	1	MHz
7[7]	ACLK HIGH time	400	–	–	ns
8[7]	ACLK LOW time	400	–	–	ns
JTAG Port timing (see Fig.38)					
1	TCK LOW time	35	–	–	ns
2	TCK HIGH time	25	–	–	ns
3	TCK cycle time	–	–	10	ns
4	TMS setup time to TCK HIGH	10	–	–	ns
5	TMS hold time after TCK HIGH	30	–	–	ns
6	TDI setup time to TCK HIGH	5	–	–	ns
7	TDI hold time after TCK HIGH	30	–	–	ns
8	TDO asserted after TCK LOW	–	–	60	ns
9	TDO hold time after TCK LOW	–	–	60	ns
10	TDO 3-state after TCK LOW	–	–	30	ns
11	TRSTN pulse width	100	–	–	ns
General purpose parallel port (see Fig.39)					
1	PIO data valid after CLK13M rising edge (output)	–	70	–	ns
2	PIO data setup time	–	10	–	ns
3	PIO data valid after CLK13M rising edge (input)	–	70	–	ns
All outputs					
t_r[7]	rise time	–	–	20	ns
t_f[7]	fall time	–	–	20	ns

Notes to the AC characteristics

1. Parameters are valid over the specified temperature range.
2. All voltages are measured with respect to ground (V_{SS}). For testing all inputs swing between 0 V and V_{DD} with a transition time of 4 ns. All time measurements are made with input voltages of 0 V and V_{DD} and output voltages of $0.2V_{DD}$ and $0.8V_{DD}$ as appropriate.
3. Test conditions for outputs: C_L = 40 pF, except open-drain outputs. Test conditions for open-drain outputs: C_L = 40 pF; I_L = 1.8 mA at V_{DD}.
4. All timing diagrams should only be referred to in regard to the edge-to-edge measurements of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to the functional description and related timing diagrams for device operation. All setup and hold times are specified with respect to V_{IH} and V_{IL}. All delay times with respect to $0.5V_{DD}$. Times with only typical values are not tested during IC production
5. For testing the AC characteristics, the low swing input CKI is driven with a square wave signal of the specified minimum peak-to-peak input voltage swing. The typical values for additional components are: C1 = 4.7 nF, C_2 = 100 pF and R_1 = 10 kΩ.
6. For testing the AC characteristics, the input CLK32I is driven with a standard test signal (see note 2). A typical application for crystal operation is: R = 10 MΩ, fQ = 32.768 kHz, C_1 = 15 pF, C_T = 15 pF (for crystal C_L = 12.5 pF).
7. These times are guaranteed by design and are not tested during IC production.
8. DCLK internally divided-by-two to drive the DSP; $t_{DCLKOUT} = {}^1/_{DCLK}$.
9. This time specified is when PI is empty.
10. This time specified is when PO is full.
11. Not tested in production.
12. Mode 0 and 1, or Mode 2 are selected by register settings. Refer to the functional specification.
13. The output DCL has two different cycle times depending on the DCL period number. Refer to the functional description. The table lists the cycle times for the 1.536 MHz internal clock mode and the maximum clock frequency in external clock mode. The minimum cycle times correspond to the 4.096 MHz external clock mode and therefore apply to all the external clock modes.
14. The Audio Interface timing is given for the non-transparent mode. In transparent mode the IOM®-2 Interface timing applies to the Audio Interface accordingly, refer to functional description.

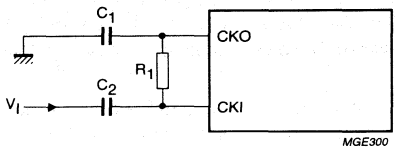


Fig.22 13 MHz Clock circuit.

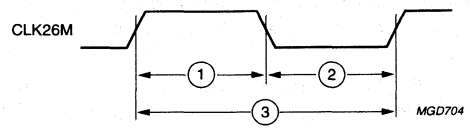


Fig.23 CLK26M Clock timing.

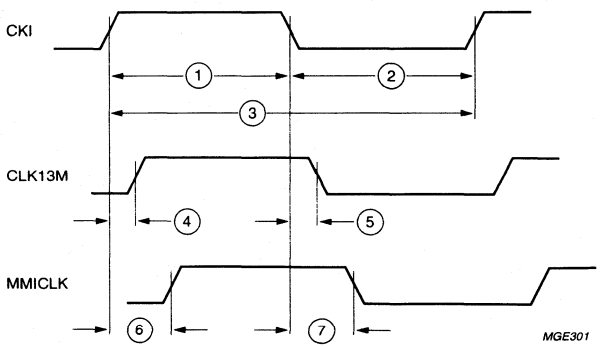


Fig.24 13 MHz Clock timing.

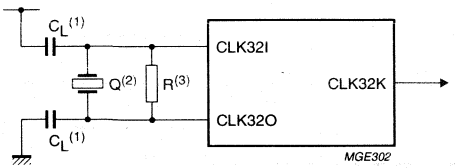


Fig.25 32.768 kHz Clock circuit.

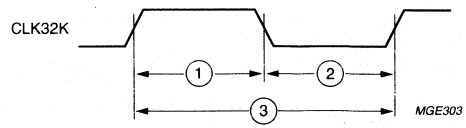


Fig.26 32.768 kHz Clock timing.

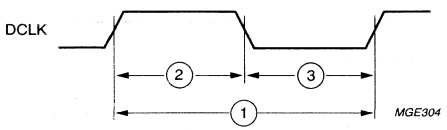


Fig.27 DSP Clock timing.

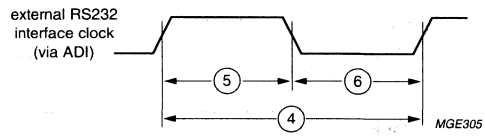


Fig.28 RS232 Clock timing.

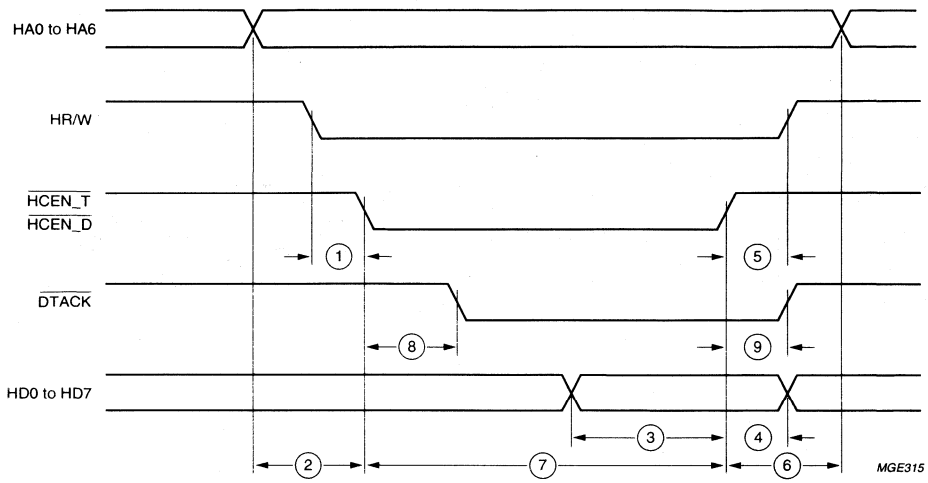


Fig.29 Host Interface Write timing.

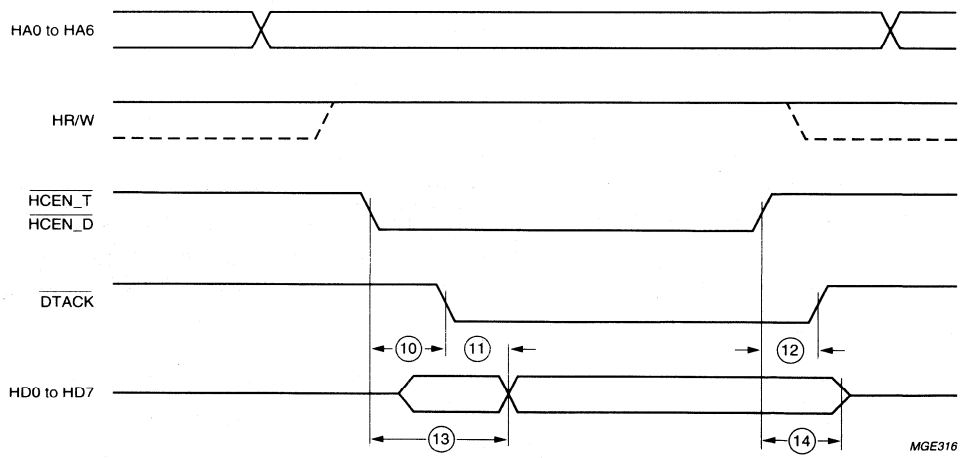


Fig.30 Host Interface Read timing.

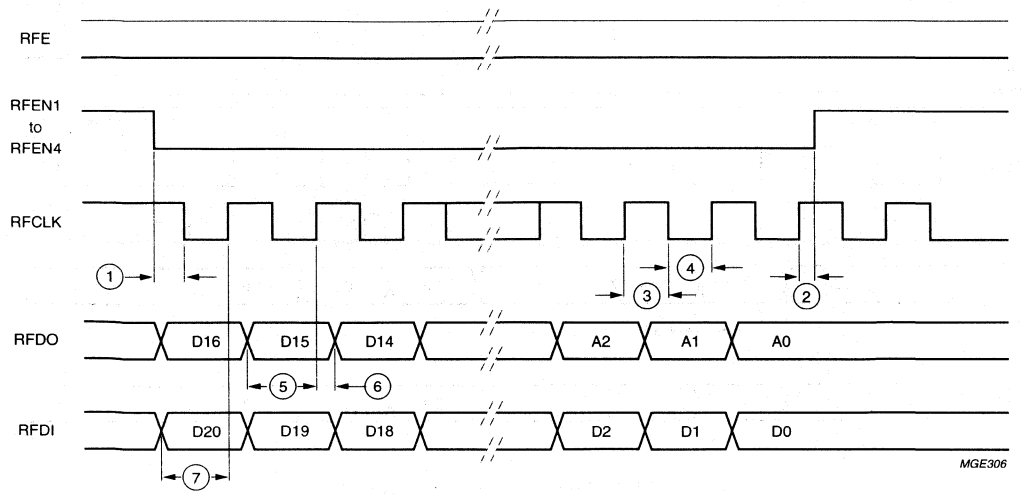


Fig.31 RF-IC Control Bus timing – Mode 0.

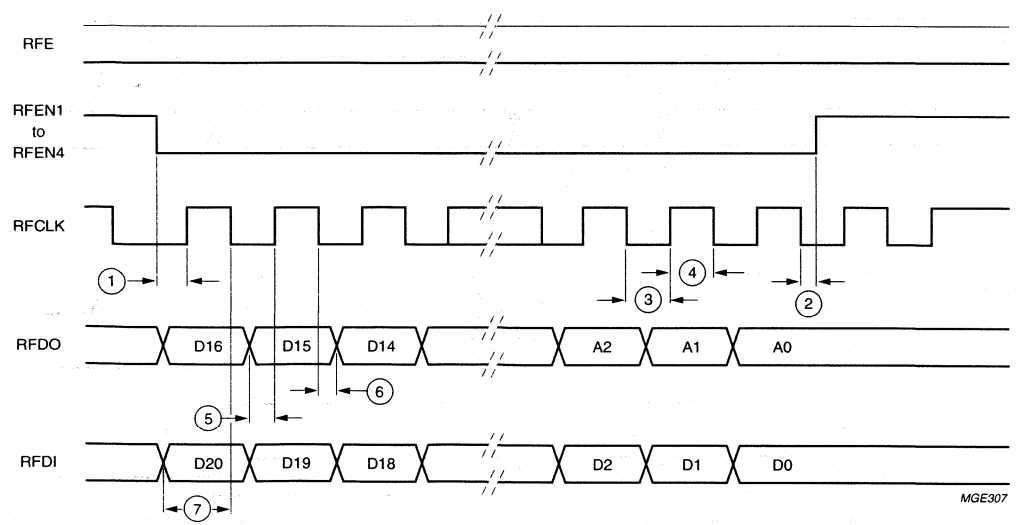


Fig.32 RF-IC Control Bus timing – Mode 1.

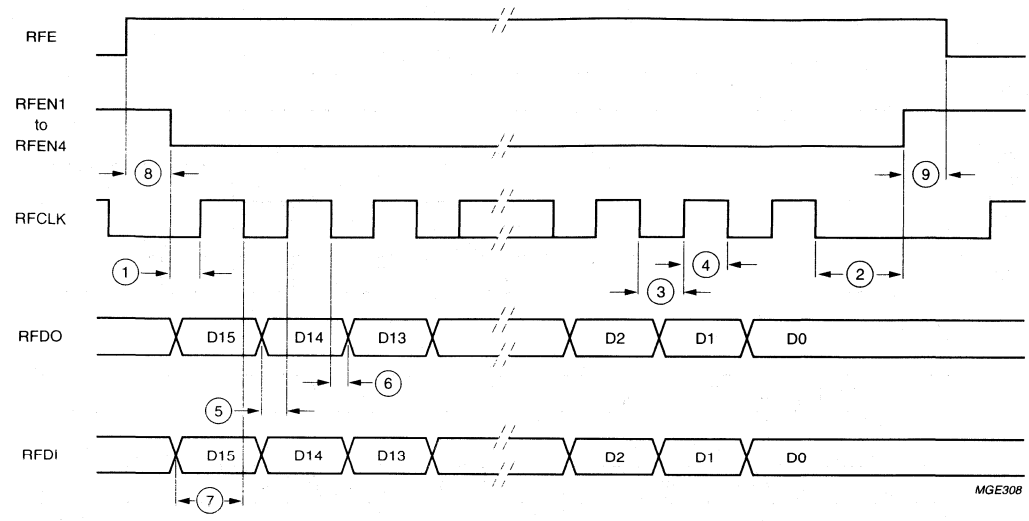


Fig.33 RF-IC Control Bus timing – Mode 2.

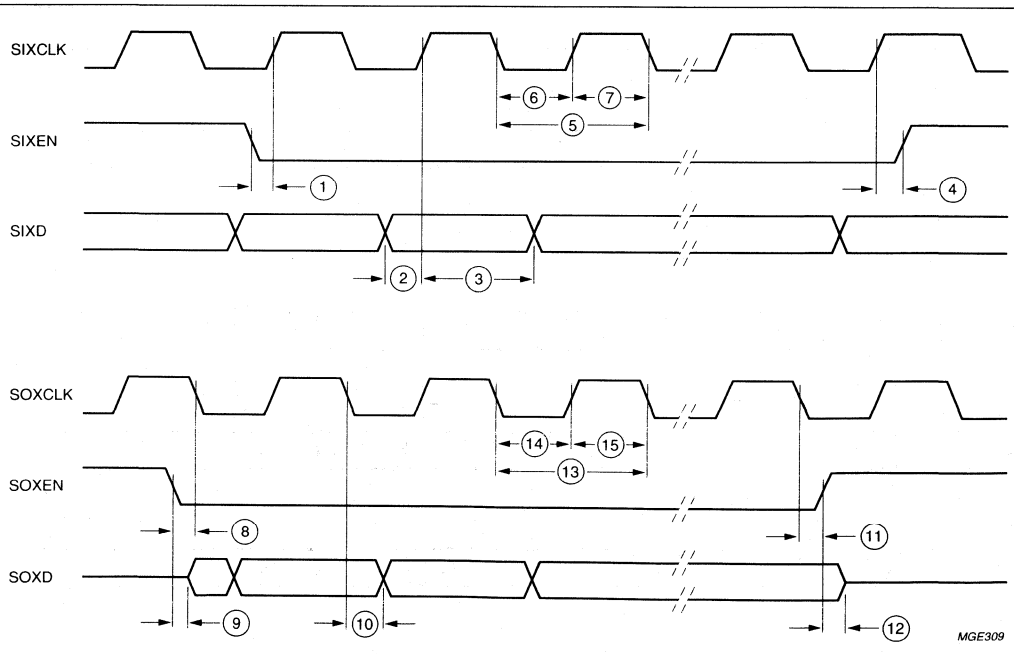


Fig.34 Baseband Interface timing (DSP Core x-Port).

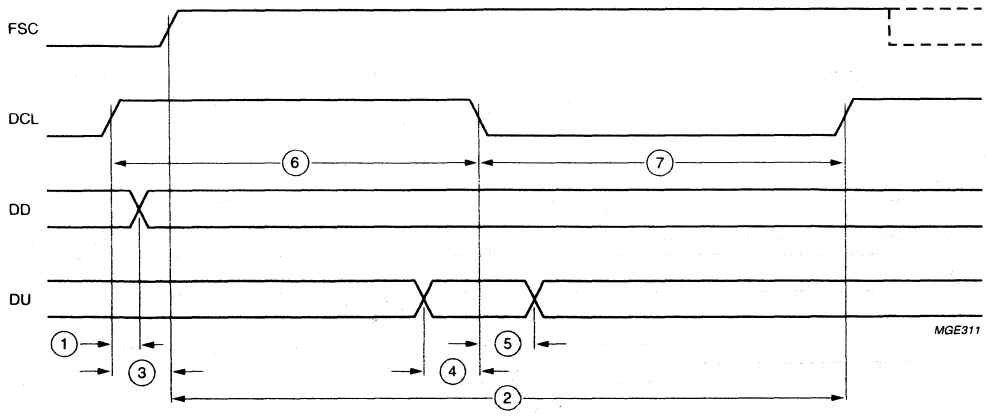


Fig.35 IOM®-2 Interface timing - Single Clock cycle mode.

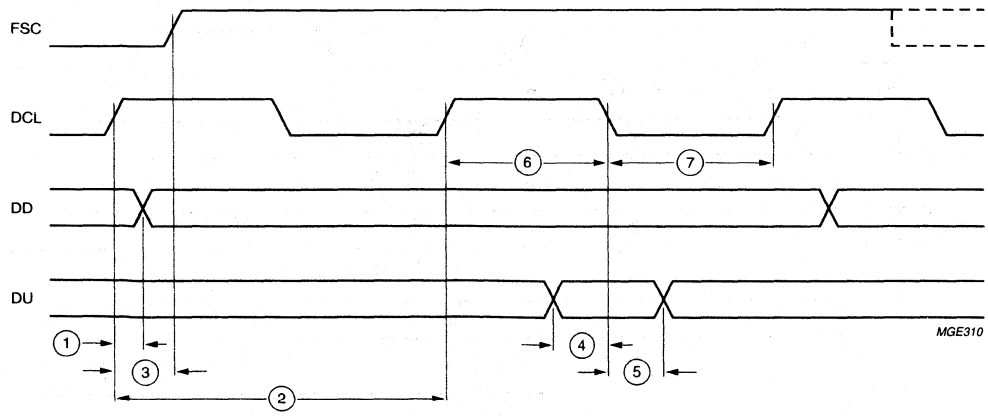


Fig.36 IOM®-2 Interface timing - Double Clock cycle mode.

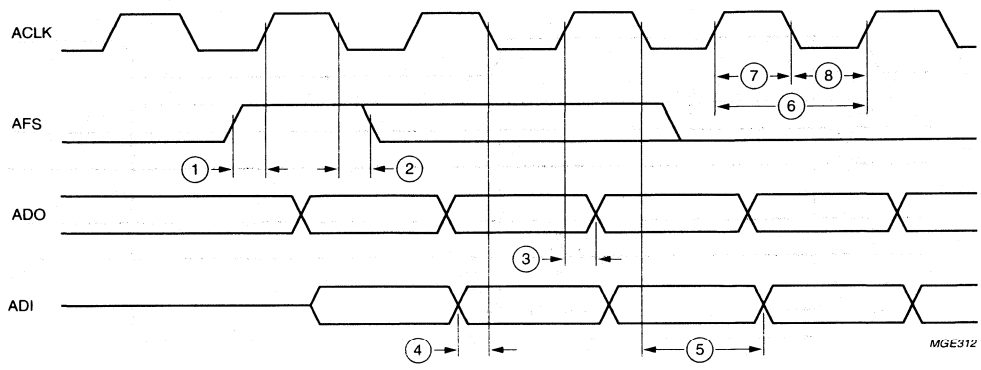


Fig.37 Audio Interface timing (non-transparent mode).

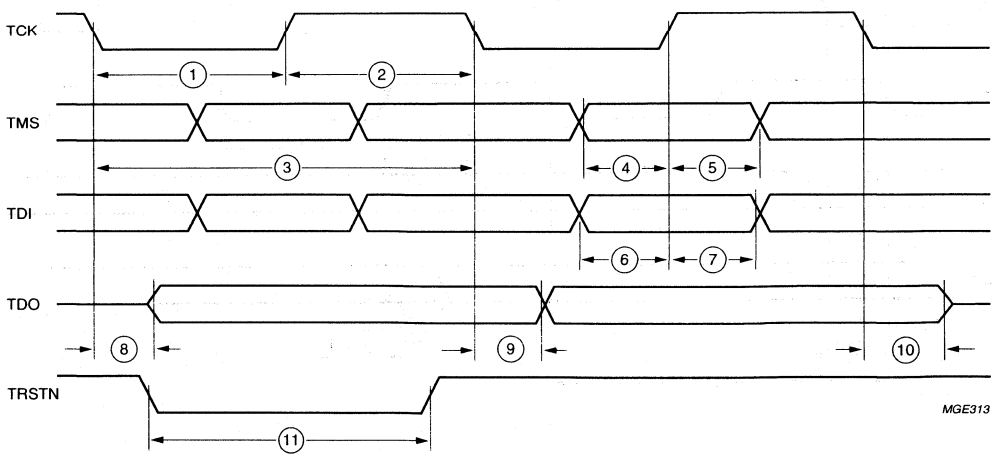


Fig.38 JTAG port timing.

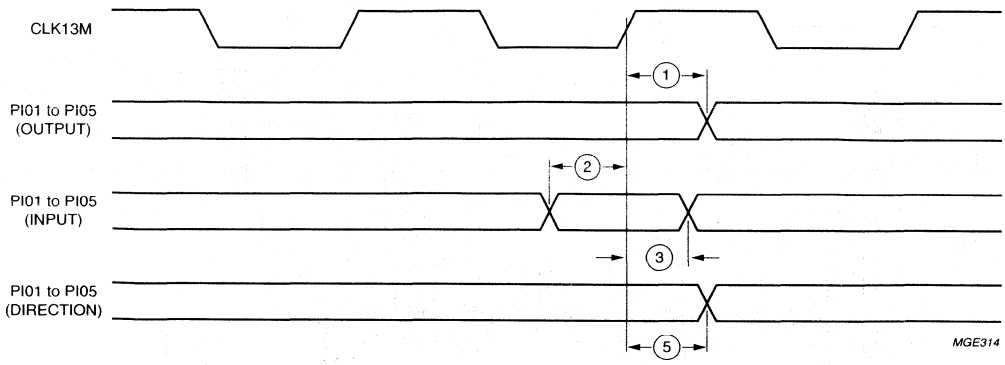


Fig.39 General purpose parallel port.

17 APPLICATION INFORMATION

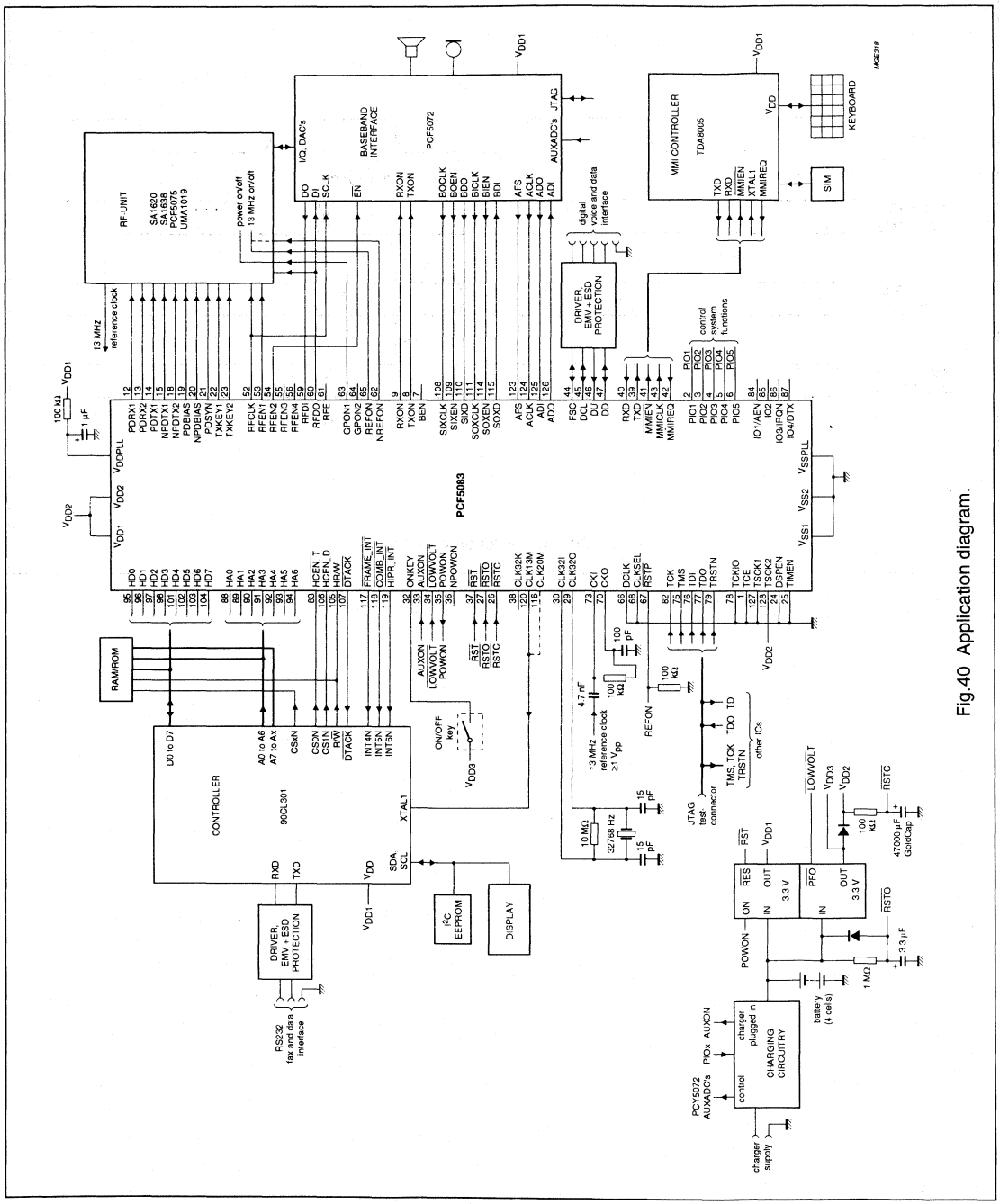


Fig.40 Application diagram.

NOTES

DECT baseband controllers PCD5090; PCA5097

INTRODUCTION

This data sheet details the specific features of the:

PCD5090/xxx; DSP-ROM, with external ROM

PCA5097/xxx; DSP-ROM, with Field Electronically Erasable Programmable Read Only Memory (FEEPROM).

FEATURES

General

- The PCx509x is designed for GAP-compliant handsets and simple base stations
- Embedded 80C51 microcontroller with twice the performance of the classic architecture, up to 128 kbytes external memory or 64 kbytes FEEPROM program memory and 3 kbytes of data memory on chip. In addition there is 1 kbyte of on-chip data memory that is shared with on-chip Burst Mode Logic (BML) and DSP, the System Data RAM (SDR).
- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I²C-bus, interrupt sources and/or external memory. External program memory is addressable up to 128 kbytes (PCD5090/xxx and PCA5097/xxx).
- Portable Part (PP) and Fixed Part (FP) modes
- TDMA frame (de)multiplexing; transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation, protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three-channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement and battery voltage measurement. One channel available for other purposes.
- On-chip 8-bit DAC for frequency adjustment of 13.824 MHz on-chip crystal oscillator
- Phase error measurement and phase error correction by hardware
- Digital-to-Analog Converters (DACs) and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032)
- IOM-2interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable timing of radio-control signals
- Programmable polarity of radio-control signals
- Easy interfacing with radio circuits, operating at other supply voltage
- Programmable GMSK pulse shaper
- On-chip comparator for use as bit-slicer
- Power-on reset
- Low supply voltage (2.7 to 5.5 V)
- SACMOS technology.

DSP software features

- ADPCM encoding and decoding complying with G.721
- Speech filters
- Programmable gain in speech paths
- Side tone and soft mute
- Ringer and tone (DTMF) generator
- Dial tone detection
- Echo cancellation
- Automatic gain control
- Telephone Answering Machine (TAM) switch
- Conference call (PCD5090/400)
- Hands-free operation (PCD5090/311).

For each DSP software version a separate manual is available, in which detailed information is provided on how parameters must be set.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5090H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2
PCA5097H			
PCD5090HZ	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

BLOCK DIAGRAM

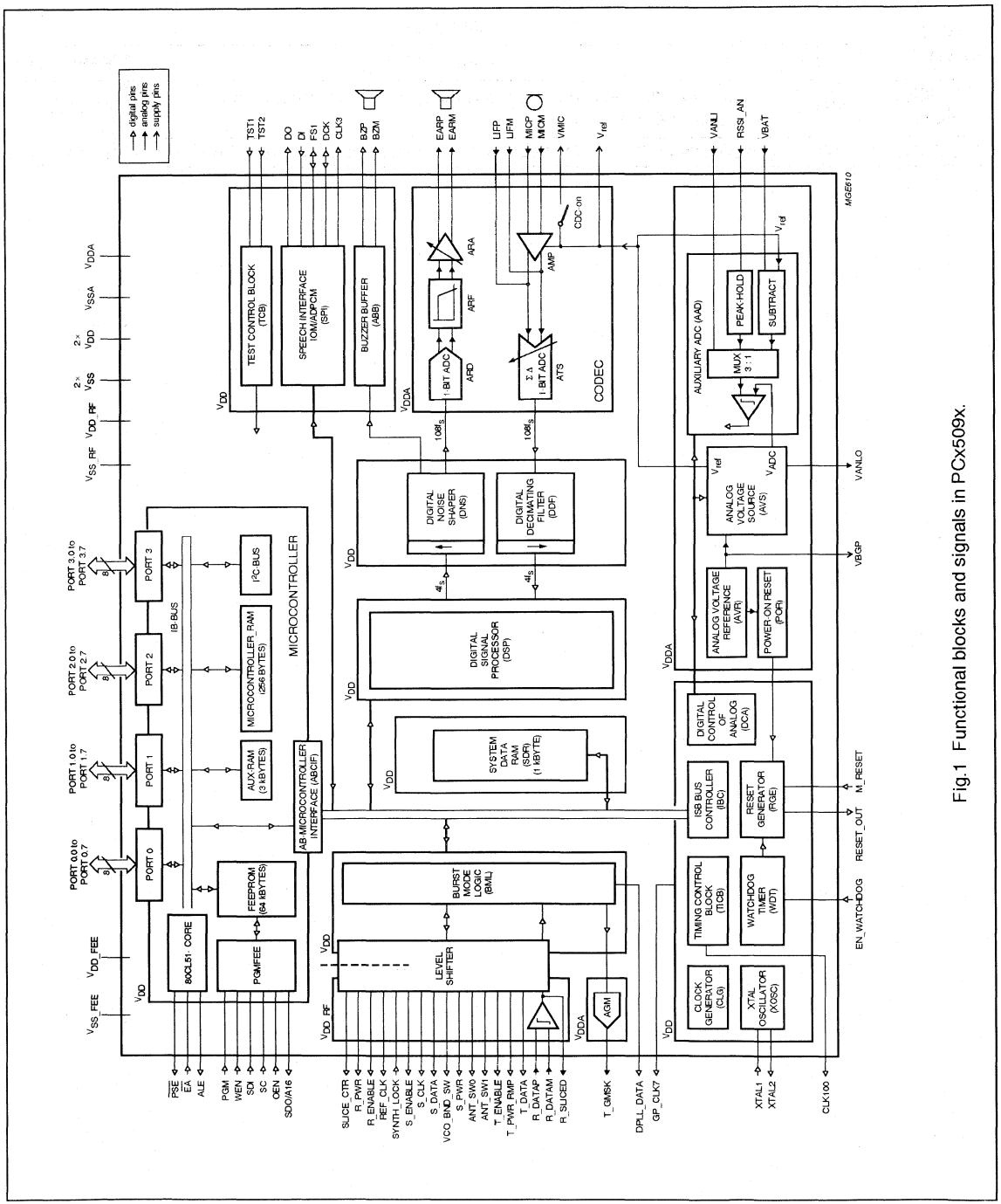


Fig.1 Functional blocks and signals in PCx509x.

PINNING

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
ANT_SW1	1	99	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	100	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	1	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	2	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	3	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	4	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	5	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	6	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	7	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	8	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	9	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	10	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	11	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	12	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS_RF}	15	13	–	–	supply	negative supply voltage for RF interface level shifters
V_{DD_RF}	16	14	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD_FEE}	17	15	–	–	supply	positive supply voltage for FEEPROM program memory
SLICE_CTR	18	16	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	17	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	18	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	19	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	20	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	21	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	22	I	–	ANAIOD1	analog input to A/D converter
VBAT	25	23	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	24	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec
DCK	27	25	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	26	I	–	DIPP0PES	ADPCM or IOM data input

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
FS1	29	27	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	28	O	off	ISI8DPES	ADPCM or IOM data output
XTAL2	31	29	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	30	I	–	ANAIOD1	crystal oscillator input
VANLO	33	31	O	1.0 V	ANAIOD1	analog output from D/A converter
TST2	34	32	I	–	DIDP0PES	test input 2
TST1	35	33	I	–	DIDP0PES	test input 1
LIFM	36	34	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	35	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	36	–	–	supply	negative supply voltage for analog circuits
MICM	39	37	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	38	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	39	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	40	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	41	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	42	–	–	supply	positive supply voltage for analog circuits
EARM	45	43	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	44	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	45	I	–	DIUP0PES	watchdog enable input
P1.0	48	46	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	47	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	49	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	50	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	51	O	L	ISP2DPES	R_DATA comparator output
PGM	54	52	I	–	DIDP0PES	FEEPROM programming mode; can be left open-circuit for PCA5090 and PCD5090/xxx
P1.3	55	53	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	54	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.5	57	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
P1.6	58	56	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	57	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD2}	60	58	–	–	supply	positive supply voltage
BZM	61	59	O	L	ANAIOD2	negative buzzer output
BZP	62	60	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	61	–	–	supply	negative supply voltage
V_{SS_FEE}	64	62	–	–	supply	negative supply voltage
P3.0	65	63	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	64	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.6	71	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.2	75	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
SDO/A16	76	74	O	H or L L	ISP4DPES	PCA5090,PCA5097: FEEPROM shift data output PCD5090/xxx, PCA5097/xxx: FEEPROM shift data out/address bit 16 for 128 kbytes external program memory
OEN	77	75	I	–	DIDP0PES	FEEPROM output enable; tie to V_{DD} for PCA5090, PCD5090/xxx
SC	78	76	I	–	DIDP0PES	FEEPROM shift clock; can be left open-circuit for PCA5090, PCD5090/xxx
SDI	79	77	I	–	DIDP0PES	FEEPROM shift data input; can be left open-circuit for PCA5090, PCD5090/xxx
WEN	80	78	I	–	DIUP0PES	FEEPROM Write enable; can be left open-circuit for PCA5090, PCD5090/xxx
P2.3	81	79	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	80	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
P2.5	83	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	84	O	H	ISQ2CPES	program store enable (80C51)
ALE	87	85	O	H	ISQ4CPES	address latch enable (80C51)
$\overline{EA}$	88	86	I	–	ISF2DPES	external access enable (80C51)
V_{SS1}	89	87	–	–	supply	negative supply voltage
V_{DD1}	90	88	–	–	supply	positive supply voltage
P0.7	91	89	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	90	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	97	I	–	DIDP0PES	master reset input (Schmitt-trigger)
RESET_OUT	100	98	O	H	ISF2DPES	reset output

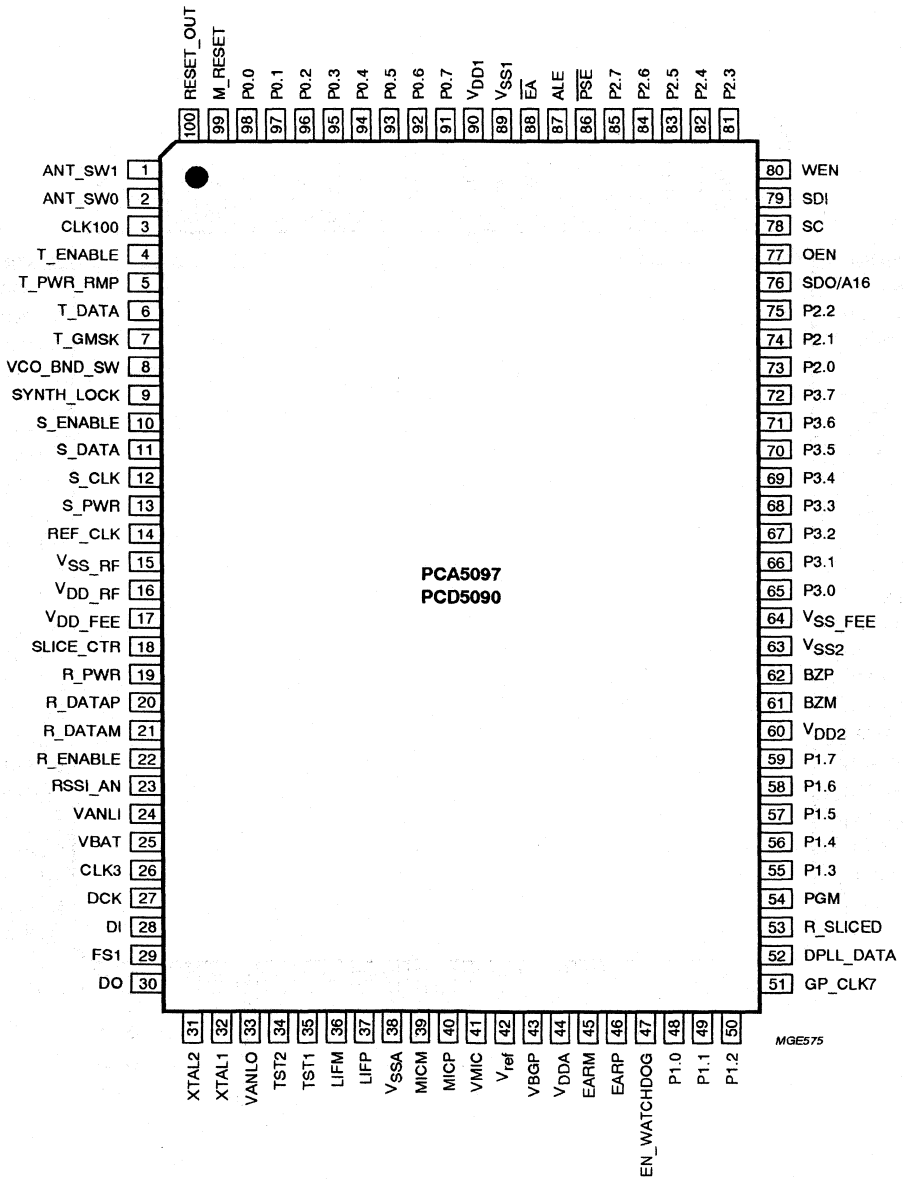


Fig.2 Pin configuration of PCX509x (QFP100).

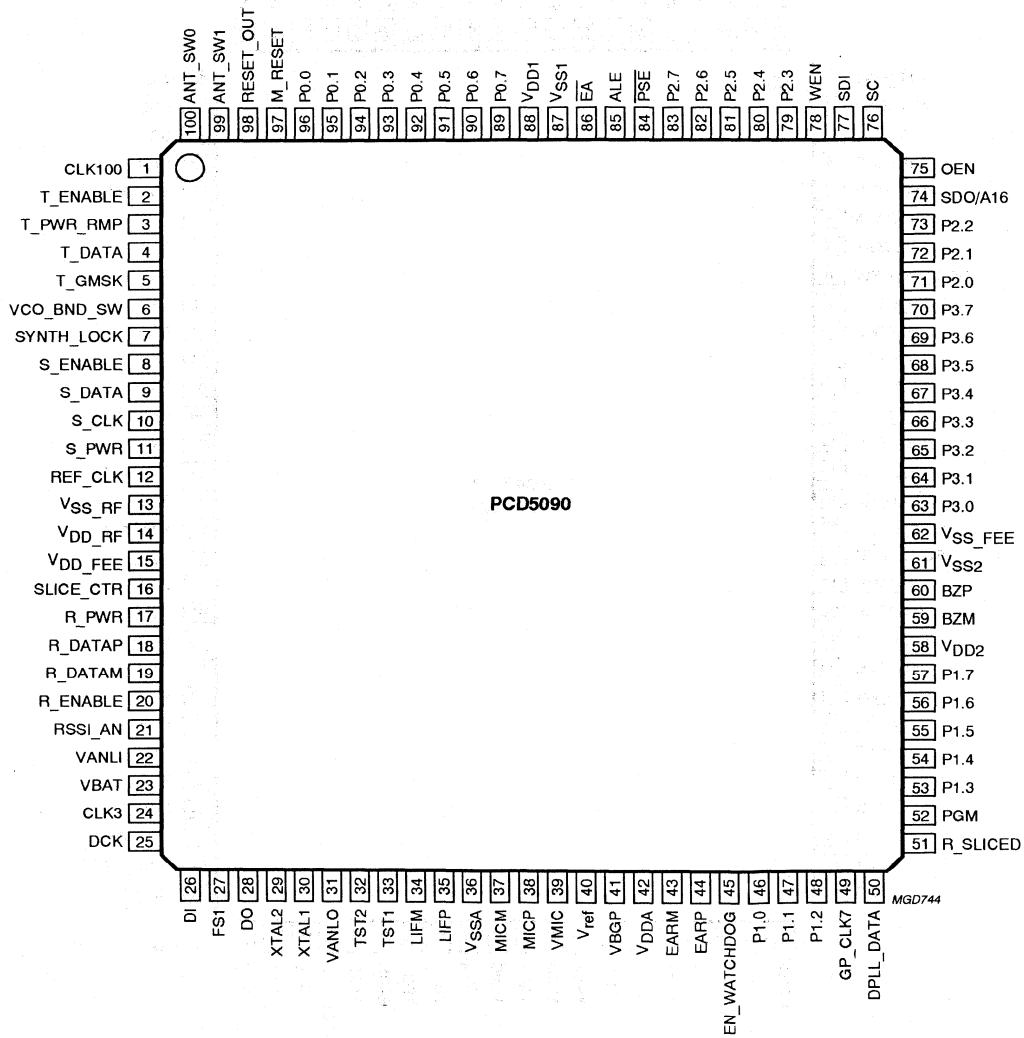


Fig.3 Pin configuration of PCD5090/xxx only (LQFP100).

FUNCTIONAL DESCRIPTION

DECT controller system description

The PCX509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications (DECT) systems. The family is designed for minimal component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I²C-bus. The Philips DECT RF-Interface is implemented. The Burst Mode Logic performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.

Power-on reset logic and power management functions further reduce power consumption and external components. The chip is intended to support stand-alone systems only. There are no provisions to build clusters of base stations. There are no provisions for external controllers to exert control over the embedded 80C51 or to have direct access to the on-chip data memories.

The DECT controller consists of a number of functional blocks that operate more or less autonomously and communicate with each other via the System Data RAM (SDR). Blocks have access to SDR via the Internal System Bus (ISB). The ISB consists of an 8-bit data, a 10-bit address bus and a number of bus-request/bus-grant signals. Access to the ISB is controlled by ISB bus Controller (IBC). The IBC acknowledges bus requests on the basis of a priority scheme.

The embedded controller 80C51 is to be programmed by the user. It must contain DECT software from Man-Machine-Interface (MMI) to the DECT protocols TBC, CBC and DBC (refer to figures 10, 11, 12 and 13 in *"prETS 300 175-2:1992 section 6"*).
All software is available from Philips Semiconductors.

Hardware state machines in the Burst Mode Logic (BML) and the Speech Interface (SPI) execute the lower blocks in the TBC, CBC and DBC. The 80C51 has control over the BML and the SPI via tables in SDR. The BML saves serial data, received via R_DATAP/M, in buffer areas in SDR. The position of buffers in SDR is fixed by the 80C51 software by means of tables previously mentioned.

A-fields and B-fields are stored in separate buffers. In this way, two traffic bearers, each with their private A-fields, can share the same B-field buffer as is required in case of bearer hand-over or local call.

The blocks DSP and CODEC support speech processing functions such as A/D- and D/A conversion, filtering, ADPCM encoding and decoding, 8-bit A-law PCM to 14-bit linear PCM conversion and its reverse, echo cancelling, tone generation, etc.

PCA5097

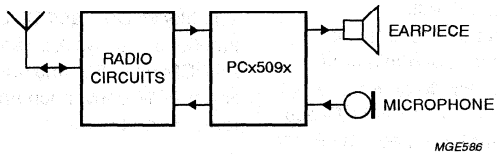
This chip is intended for program development. It contains 64 kbytes of internal program memory (FEEPROM) for the 80C51 and DSP program RAM.

PCD5090/xxx

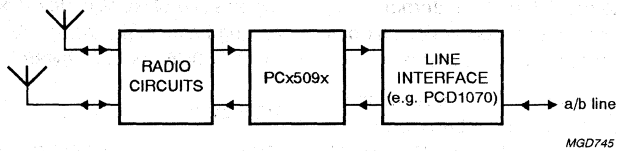
This chip is intended for handset and base station applications. The DSP program is now fixed in a ROM, for which several ROM codes (/xxx) are available (handset, analog base, digital base). An external program memory for the 80C51 of 128 kbytes ROM can be handled.

PCA5097/xxx

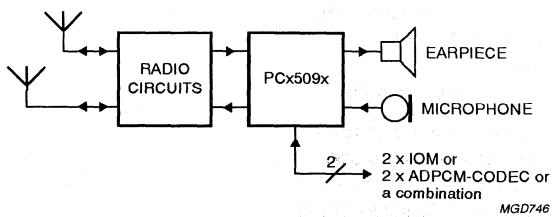
This is the same as PCD5090/xxx, but there is 64 kbytes internal program memory (FEEPROM) for the 80C51. The DSP program is preprogrammed in ROM.
This chip is meant for development purpose only.



a. Handset.



b. Base with analog interface and echo cancellation; up to 6 portables can be handled.



c. Base with digital interface and analog handset connected; up to 6 portables can be handled.

Fig.4 Block diagrams of DECT systems with PCx509x.

DECT baseband controllers PCD5091; PCD5092

FEATURES

- The PCD509x is designed for GAP-compliant handsets and base stations
- Embedded 80C51 microcontroller with twice the performance of the classic architecture, 64 kbytes of PROM program memory and 3 kbytes of data memory on chip. In addition there is 1 kbyte of on-chip data memory that is shared with on-chip Burst Mode Logic (BML) and DSP, the System Data RAM (SDR).
- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, I²C-bus, interrupt sources and/or external memory. External program memory is addressable up to 128 kbytes (PCD509x/xxx).
- +5 V port (P0 to P3) interface
- Portable Part (PP) and Fixed Part (FP) modes
- TDMA frame (de)multiplexing. Transmission or reception can be programmed for any slot.
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three-channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for frequency adjustment of 13.824 MHz on-chip crystal oscillator
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable timing of radio-control signals
- Programmable polarity of radio-control signals
- Easy interfacing with radio circuits, operating at other supply voltage (RF supply pin with level shifter for RF signals)
- GMSK pulse shaper
- On-chip comparator for use as bit-slicer
- Power-on reset
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

DSP software features

- ADPCM encoding and decoding complying with G.721
- Speech filters
- Programmable gain in speech paths
- Side tone and soft mute
- Ringer and tone (DTMF) generator
- Dial tone detection
- Echo cancellation
- Automatic gain control
- Telephone Answering Machine (TAM) switch
- Hands-free operation (PCD5091 and PCD5093)
- Conference call (PCD5094).

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set.

For further information please contact Philips Semiconductors.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5091HZ	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
PCD5091H PCD5092H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

BLOCK DIAGRAM

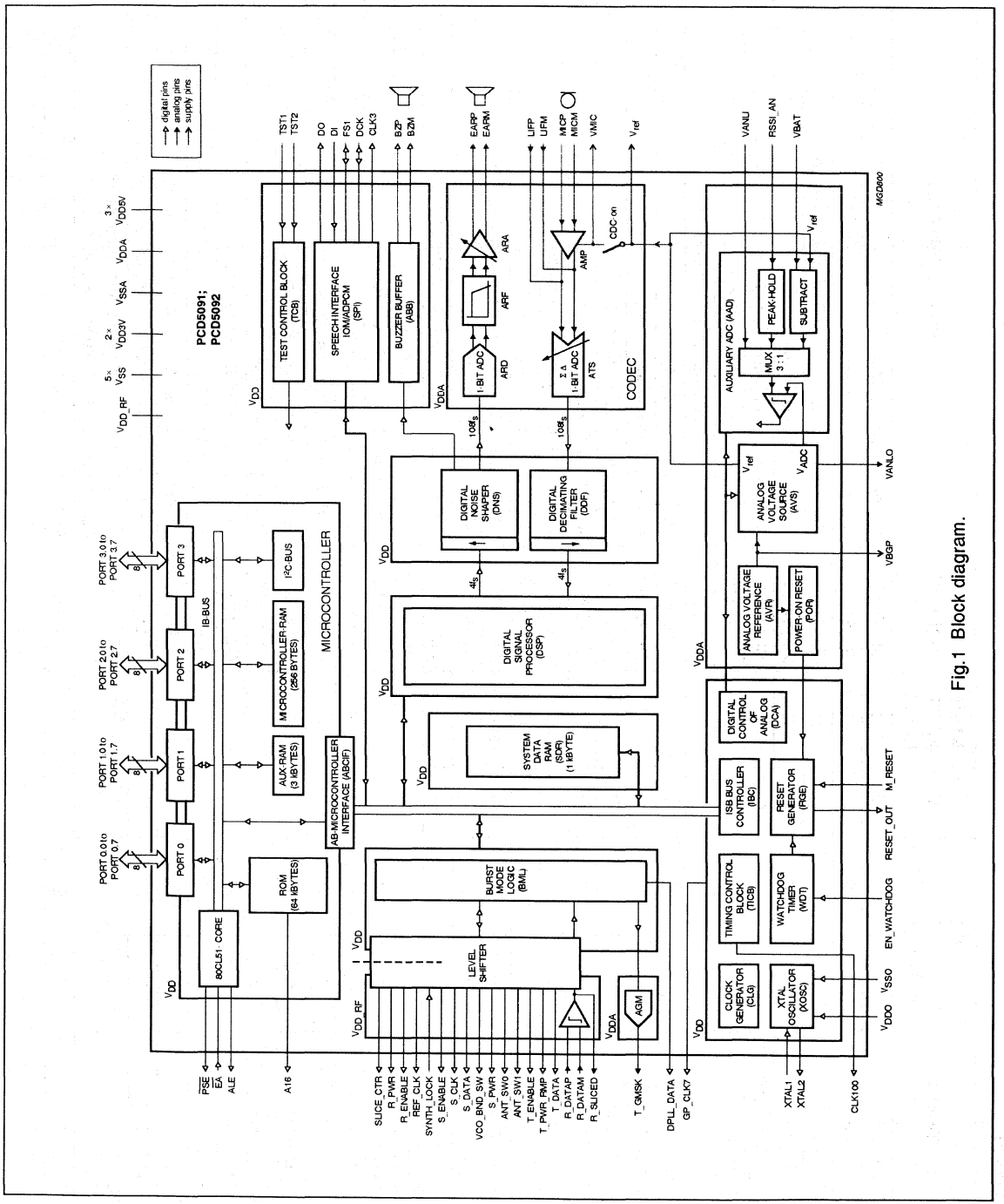


Fig.1 Block diagram.

PINNING

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
ANT_SW1	1	99	O	H	ISP2DRF3	antenna switch 1 output
ANT_SW0	2	100	O	H	ISP2DRF3	antenna switch 0 output
CLK100	3	1	O	H	ISP2DPES	100 Hz signal related to DECT frame timing output
T_ENABLE	4	2	O	H	ISP2DRF3	enable transmitter output
T_PWR_RMP	5	3	O	L	ISP2DRF3	switch transmitter power output
T_DATA	6	4	O	off	ISF2DRF3	unmodulated transmitter data output
T_GMSK	7	5	O	L	ANAIOD1	GMSK modulated transmitter data output
VCO_BND_SW	8	6	O	L	ISP2DRF3	VCO band switch output
SYNTH_LOCK	9	7	I	–	DIPP0RF3	synthesizer lock input
S_ENABLE	10	8	O	L	ISP2DRF3	synthesizer enable output
S_DATA	11	9	O	L	ISP2DRF3	serial synthesizer data output
S_CLK	12	10	O	L	ISP2DRF3	clock for serial synthesizer interface output
S_PWR	13	11	O	H	ISP2DRF3	switch synthesizer power output
REF_CLK	14	12	O	running	ISP4DRF3	13.824 MHz reference clock for synthesizer output
V_{SS1}	15	13	–	–	supply	negative supply voltage 1
V_{DD_RF}	16	14	–	–	supply	positive supply voltage for RF interface level shifters
V_{DD3V_1}	17	15	–	–	supply	positive supply voltage 1 (+3 V)
SLICE_CTR	18	16	O	L	ISP2DRF3	switch slicer time constant output
R_PWR	19	17	O	H	ISP2DRF3	switch receiver power output
R_DATAP	20	18	I	–	ANAIOD2	positive input for receiver data
R_DATAM	21	19	I	–	ANAIOD2	negative input for receiver data
R_ENABLE	22	20	O	H	ISP2DRF3	enable receiver output
RSSI_AN	23	21	I	–	ANAIOD1	analog input for RSSI measurement
VANLI	24	22	I	–	ANAIOD1	analog input to ADC
VBAT	25	23	I	–	ANAIOD1	analog input for battery voltage measurement
CLK3	26	24	O	L	ISP2DPES	3.456 MHz clock output for external ADPCM codec
DCK	27	25	I/O	input	ISF2DPES ISF2UPES	ADPCM output or IOM data clock input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DI	28	26	I	–	DIPP0PES	ADPCM or IOM data input

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
FS1	29	27	I/O	input	ISF2DPES ISF2UPES	8 kHz framing input/output (ISF2UPES in PCD5090/xxx, PCA5097/xxx)
DO	30	28	O	off	ISI8DPES	ADPCM or IOM data output
XTAL2	31	29	O	running	ANAIOD1	crystal oscillator output
XTAL1	32	30	I	–	ANAIOD1	crystal oscillator input
VANLO	33	31	O	1.0 V	ANAIOD1	analog output from D/A converter
V_{SSO}	34	32	I	–	supply	negative supply voltage for the oscillator
V_{DDO}	35	33	I	–	supply	positive supply voltage for the oscillator
LIFM	36	34	I	0.7 V	ANAIOD1	negative input from line interface
LIFP	37	35	I	0.7 V	ANAIOD1	positive input from line interface
V_{SSA}	38	36	–	–	supply	negative supply voltage for analog circuits
MICM	39	37	I	0.7 V	ANAIOR1	negative input from microphone
MICP	40	38	I	0.7 V	ANAIOR1	positive input from microphone
VMIC	41	39	O	off	ANAIOD1	positive microphone supply voltage (+2 V)
V_{ref}	42	40	O	2.0 V	ANAIOD1	reference voltage (+2 V)
VBGP	43	41	O	1.25 V	ANAIOR1	bandgap output voltage (+1.25 V)
V_{DDA}	44	42	–	–	supply	positive supply voltage for analog circuits
EARM	45	43	O	1.4 V	ANAIOD1	negative output to earpiece
EARP	46	44	O	1.4 V	ANAIOD1	positive output to earpiece
EN_WATCHDOG	47	45	I	–	DIUP0PES	watchdog enable input
P1.0	48	46	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.1	49	47	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.2	50	48	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
GP_CLK7	51	49	O	L	ISP2DPES	general purpose 6.912 MHz output
DPLL_DATA	52	50	O	L	ISP2DPES	data after clock recovery network
R_SLICED	53	51	O	L	ISP2DPES	R_DATA comparator output
V_{DD5V_1}	54	52	I	–	supply	positive supply voltage 1 for the +5 V interface
P1.3	55	53	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.4	56	54	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P1.5	57	55	I/O	H	ISQ2CPES	bidirectional 80C51 port pin

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
P1.6	58	56	I/O	off	ISI8DPES	bidirectional 80C51 port pin
P1.7	59	57	I/O	off	ISI8DPES	bidirectional 80C51 port pin
V_{DD3V_2}	60	58	–	–	supply	positive supply voltage 2 (+3 V)
BZM	61	59	O	L	ANAIOD2	negative buzzer output
BZP	62	60	O	L	ANAIOD2	positive buzzer output
V_{SS2}	63	61	–	–	supply	negative supply voltage 2
V_{SS3}	64	62	–	–	supply	negative supply voltage 3
P3.0	65	63	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.1	66	64	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.2	67	65	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.3	68	66	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.4	69	67	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.5	70	68	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.6	71	69	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P3.7	72	70	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.0	73	71	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.1	74	72	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.2	75	73	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
A16	76	74	O	L	ISP4DPES	address bit 16 for 128 kbytes external program memory
V_{DD5V_2}	77	75	I	–	supply	positive supply voltage 2 for the +5 V interface
V_{SS4}	78	76	I	–	supply	negative supply voltage 4
TST1	79	77	I	–	DIDP0PES	test input 1
TST2	80	78	I	–	DIDP0PES	test input 2
P2.3	81	79	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.4	82	80	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.5	83	81	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.6	84	82	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
P2.7	85	83	I/O	H	ISQ2CPES	bidirectional 80C51 port pin
$\overline{PSE}$	86	84	O	H	ISQ2CPES	program store enable (80C51); active LOW
ALE	87	85	O	H	ISQ4CPES	address latch enable (80C51)

SYMBOL	PIN		I/O	STATE AFTER RESET	PIN TYPE	PIN DESCRIPTION
	QFP100	LQFP100				
$\overline{EA}$	88	86	I	–	ISF2DPES	external access enable (80C51); active LOW
V_{SS5}	89	87	–	–	supply	negative supply voltage 5
V_{DD5V_3}	90	88	–	–	supply	positive supply voltage 3 for the +5 V interface
P0.7	91	89	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.6	92	90	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.5	93	91	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.4	94	92	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.3	95	93	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.2	96	94	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.1	97	95	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
P0.0	98	96	I/O	off H	ISP2DPES ISQ2CPES	bidirectional 80C51 port pin (ISQ2CPES in PCD5090/xxx, PCA5097/xxx)
M_RESET	99	97	I	–	DIDP0PES	master reset input (Schmitt-trigger)
RESET_OUT	100	98	O	H	ISF2DPES	reset output

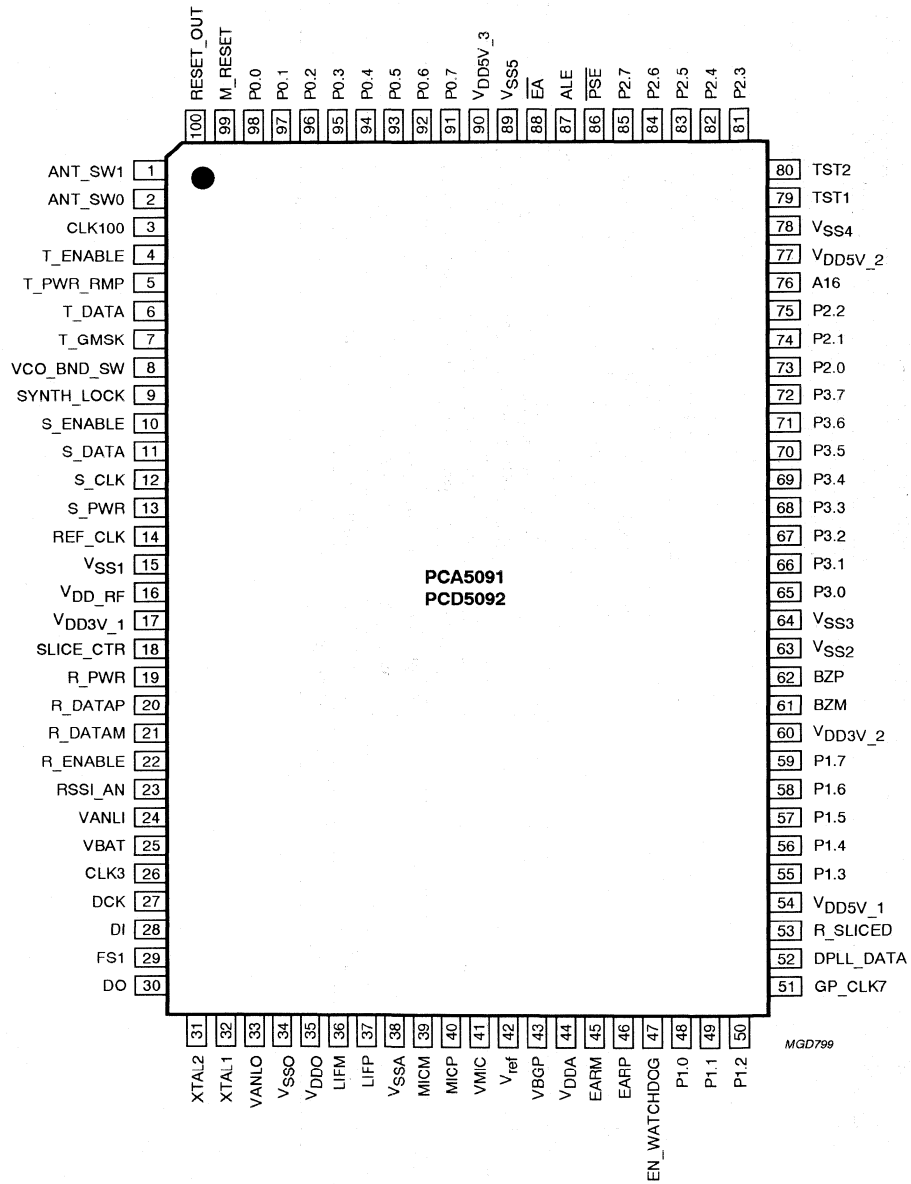


Fig.2 Pin configuration (QFP100).

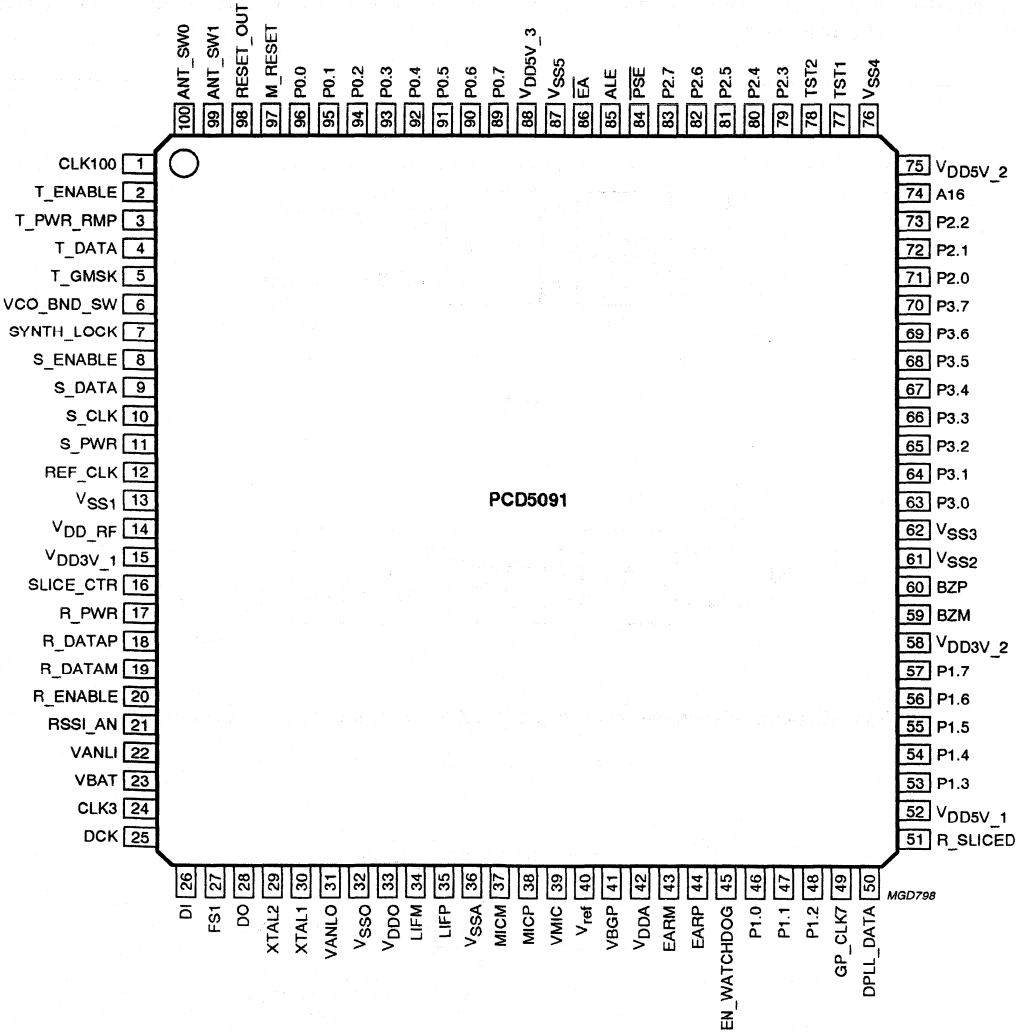
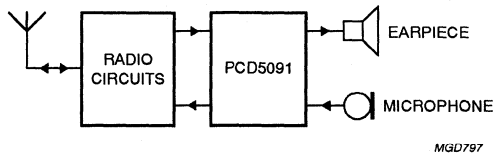


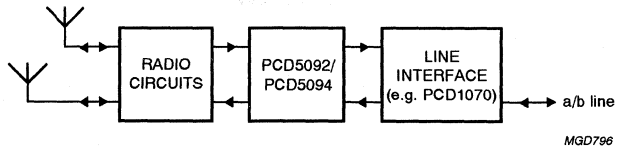
Fig.3 Pin configuration (LQFP100).

FUNCTIONAL DESCRIPTION

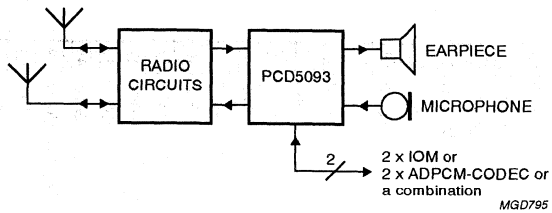
The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and I²C-bus. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.



a. Handset.



b. Base with analog interface and echo cancellation; up to 6 portables can be handled.



c. Base with digital interface and analog handset connected; up to 6 portables can be handled.

Fig.4 Block diagrams of DECT systems with PCX509x.

IC card interface | TDA8002

FEATURES

- Single supply voltage interface (3.3 or 5 V environment)
- Low-power (sleep) mode
- Three specific protected half-duplex bidirectional buffered I/O lines
- V_{CC} regulation (5 V ±5%, I_{CC} < 65 mA at V_{DD} = 5 V, with controlled rise and fall times
- Thermal and short-circuit protections with current limitations
- Automatic ISO 7816 activation and deactivation sequences
- Clock generation for the card up to 12 MHz with synchronous frequency changes
- Clock generation up to 20 MHz (auxiliary clock)
- Synchronous and asynchronous cards (Memory and smart cards)
- ISO 7816, GSM11.11 compatibility and EMV (Europay, Mastercard, Visa) compliant
- Step-up converter for V_{CC} generation
- Supply supervisor for spikes elimination and emergency deactivation.

APPLICATIONS

- IC card readers for:
  - GSM applications
  - banking
  - electronic payment
  - identification
  - Pay TV
  - road tolling.

GENERAL DESCRIPTION

The TDA8002 is a complete low-power, analog interface for asynchronous and synchronous cards. It can be placed between the card and the microcontroller. It performs all supply, protection and control functions. It is directly compatible with ISO 7816, GSM11.11 and EMV specifications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage						
V_{DDA}	analog supply voltage		3.0	5	6.5	V
I_{DD}	supply current	low-power mode	–	–	150	µA
		idle mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 5 V	–	–	5	mA
		active mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 5 V	–	–	9	mA
		active mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 3 V	–	–	12	mA
Card supply voltage						
$V_{CC(stat)}$	output voltage	DC load <65 mA	4.75	–	5.25	V
$I_{CC(lim)}$	output current	V_{CC} short-circuited to GND	–	–	65	mA
General						
f_{clk}	card clock frequency		0	–	12	MHz
t_{de}	deactivation cycle time		60	80	100	µs
P_{tot}	continuous total power dissipation					
	TDA8002AT; TDA8002BT	T_{amb} = −25 to +85 °C	–	–	0.56	W
	TDA8002G	T_{amb} = −25 to +85 °C	–	–	0.46	W
T_{amb}	operating ambient temperature		−25	–	+85	°C

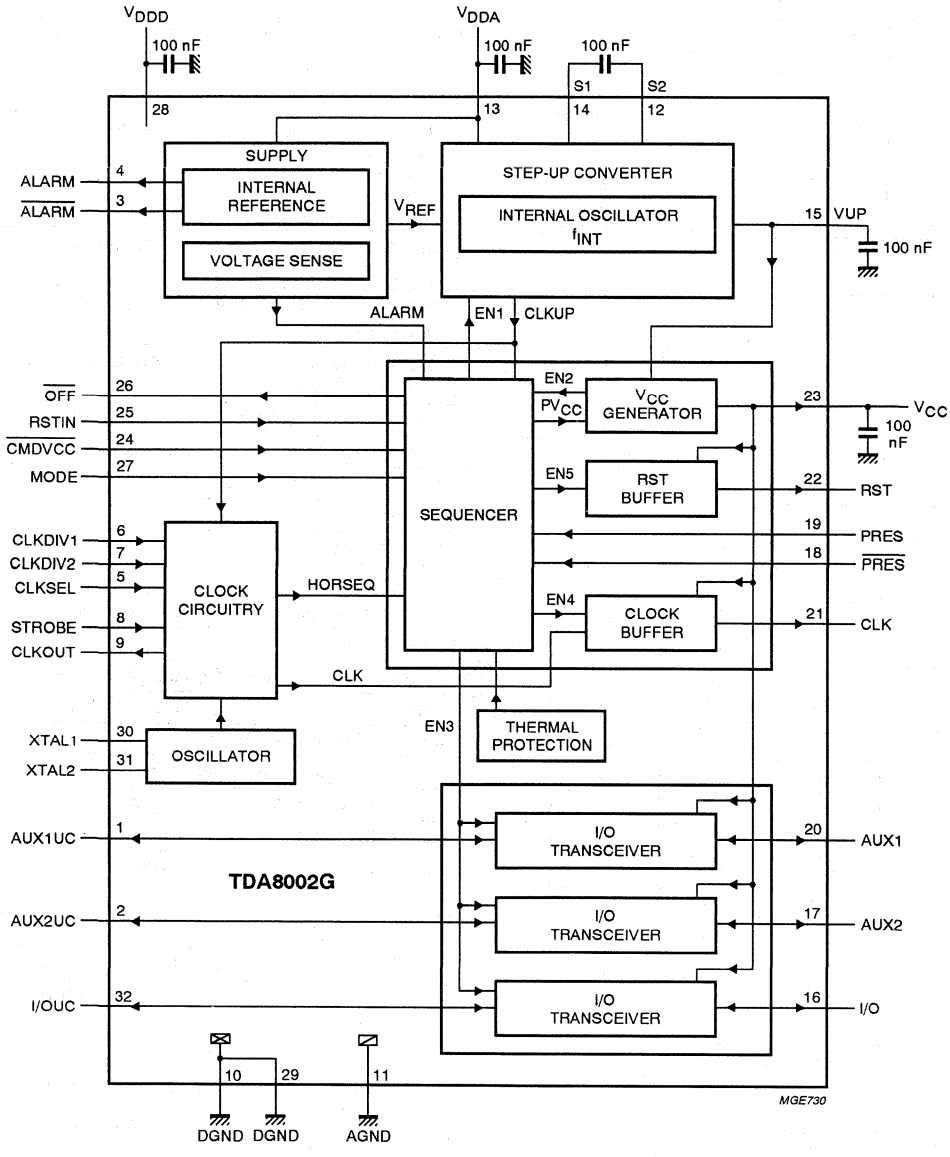
ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE			
	MARKING	NAME	DESCRIPTION	VERSION
TDA8002AT/3/C1[2]	TDA8002AT/3	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-AH4
TDA8002AT/5/C1[3]	TDA8002AT/5	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-AH4
TDA8002BT/3/C1[2]	TDA8002BT/3	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-AH4
TDA8002BT/5/C1[3]	TDA8002BT/5	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-AH4
TDA8002G/3/C1[2]	80023	LQFP32	plastic low profile quad flat pack; 32 leads; body width 5.0 mm	SOT401-BA2
TDA8002G/5/C1[3]	80025	LQFP32	plastic low profile quad flat pack; 32 leads; body width 5.0 mm	SOT401-BA2
TDA8002U/3/C1[2]	–	–	wafer	–
TDA8002U/5/C1[3]	–	–	wafer	–

Note

1. **The /3 or /5 suffix indicates the voltage supervisor option.**
2. The /3 version can be used with a 3 V or 5 V power supply environment (see Chapter "Functional description").
3. The /5 version can be used with a 5 V power supply environment.

BLOCK DIAGRAM



ALL CAPACITORS ARE MANDATORY.

Fig.1 Block diagram (TDA8002G).

PINNING

SYMBOL	PIN			I/O	DESCRIPTION
	TYPE A	TYPE B	TYPE G		
XTAL1	1	1	30	I/O	crystal connection or input for external clock
XTAL2	2	2	31	I/O	crystal connection
I/OUC	3	3	32	I/O	data I/O line to and from microcontroller
AUX1UC	4	4	1	I/O	auxiliary line to and from microcontroller for synchronous applications
AUX2UC	5	–	2	I/O	auxiliary line to and from microcontroller for synchronous applications
$\overline{\text{ALARM}}$	–	5	3	O	open drain NMOS reset for microcontroller (active LOW)
ALARM	6	6	4	O	open drain PMOS reset for microcontroller (active HIGH)
CLKSEL	7	7	5	I	control signal for CLK (LOW = XTAL oscillator; HIGH = STROBE input)
CLKDIV1	8	8	6	I	control with CLKDIV2 for choosing CLK frequency
CLKDIV2	9	9	7	I	control with CLKDIV1 for choosing CLK frequency
STROBE	10	10	8	I	external clock input for synchronous applications
CLKOUT	11	11	9	O	clock output (see Table 1)
DGND	12	12	10	supply	digital ground
AGND	13	13	11	supply	analog ground
S2	14	14	12	I/O	capacitance connection for voltage doubler
V_{DDA}	15	15	13	supply	positive supply voltage
S1	16	16	14	I/O	capacitance connection for voltage doubler
VUP	17	17	15	I/O	output of voltage doubler (connect to 100 nF)
I/O	18	18	16	I/O	data I/O line to and from card
AUX2	19	–	17	I/O	auxiliary I/O line to and from card
$\overline{\text{PRES}}$	20	19	18	I	active LOW card presence contact
PRES	–	20	19	I	active HIGH card presence contact
AUX1	21	21	20	I/O	auxiliary I/O line to and from card
CLK	22	22	21	O	clock to card (C3) (see Table 1)
RST	23	23	22	O	card reset (C2)
V_{CC}	24	24	23	O	supply for card (C1) (decouple with 100 nF)
$\overline{\text{CMDVCC}}$	25	25	24	I	active LOW start activation sequence from microcontroller
RSTIN	26	26	25	I	card reset from microcontroller
$\overline{\text{OFF}}$	27	27	26	O	open drain NMOS interrupt to microcontroller (active LOW)
MODE	28	28	27	I	operating mode selection (HIGH = normal; LOW = low-power)
V_{DDD}	–	–	28	supply	positive supply voltage
DGND	–	–	29	supply	digital ground

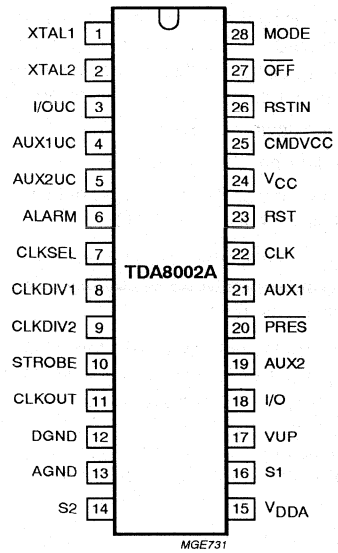


Fig.2 Pin configuration (TDA8002A).

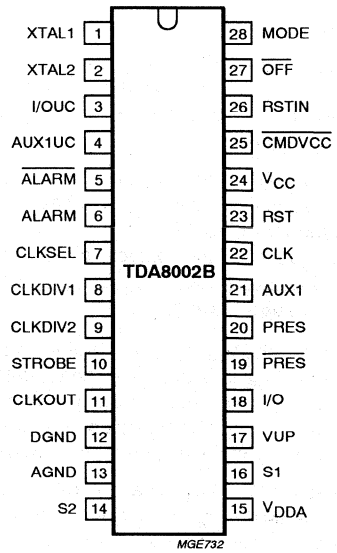


Fig.3 Pin configuration (TDA8002B).

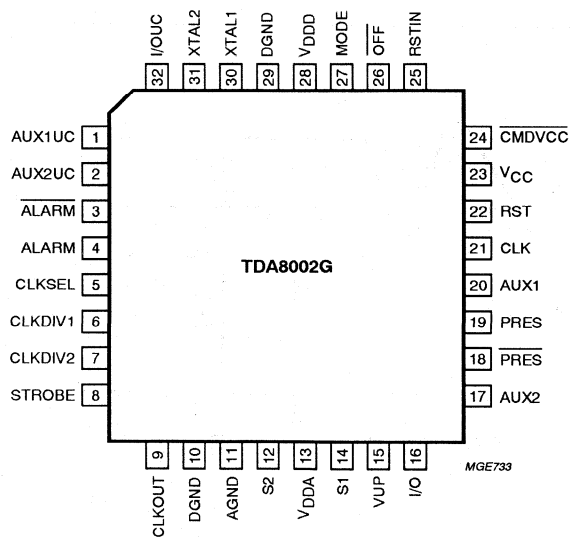


Fig.4 Pin configuration (TDA8002G).

FUNCTIONAL DESCRIPTION

Power supply

The supply pins for the chip are V_{DDA}, V_{DDD}, AGND and DGND. V_{DDA} and V_{DDD} (i.e. V_{DD}) should be in the range of 3.0 to 6.5 V. All card contacts remain inactive during power-up or power-down.

On power-up, the logic is reset by an internal signal. The sequencer is not activated until V_{DD} reaches $V_{th2} + V_{hys2}$ (see Fig.5). When V_{DD} falls below V_{th2}, an automatic deactivation sequence of the contacts is performed.

Supply voltage supervisor (V_{DD})

This block surveys the V_{DD} supply. A defined reset pulse of 10 ms minimum (t_W) is retriggerable and is delivered on the ALARM outputs during power-up or power-down of V_{DD} (see Fig.5). This signal is also used for eliminating the spikes on card contacts during power-up or power-down.

When V_{DD} reaches $V_{th2} + V_{hys2}$, an internal delay is started. The ALARM outputs are active until this delay has expired. When V_{DD} falls below V_{th2}, ALARM is activated and a deactivation sequence of the contacts is performed.

For 3 V supply, the supervisor option must be chosen at 3 V. For 5 V supply, both options (3 or 5 V) may be chosen depending on the application.

Clock circuitry

The TDA8002 supports both synchronous and asynchronous cards (I^2C-bus memories requiring an acknowledge signal from the master are not supported). There are three methods to clock the circuitry:

1. apply a clock signal to pin STROBE
2. use of an internal RC oscillator
3. or use of a quartz oscillator which should be connected between pins XTAL1 and XTAL2.

When CLKSEL is HIGH, the clock should be applied on the STROBE pin, and when CLKSEL is LOW, one of the internal oscillators is used.

When an internal clock is used, the clock output is available on pin CLKOUT. The RC oscillator is selected by making CLKDIV1 HIGH and CLKDIV2 LOW. The clock output to the card is available on pin CLK. The frequency of the card clock can be the input frequency divided by 2 or 4, STOP LOW or 1.25 MHz, depending on the states of CLKDIV1 or CLKDIV2 (see Table 1).

Do not change CLKSEL during activation. When in low-power (sleep) mode, the internal oscillator frequency which is available on pin CLKOUT is lowered to approximately 16 kHz for power-economy purposes.

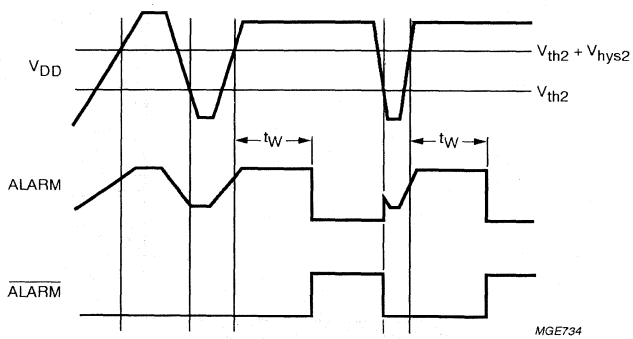


Fig.5 Alarm as a function of V_{DD} (pulse width 10 ms).

Table 1 Clock circuitry definition; note 1

MODE	CLKSEL	CLKDIV1	CLKDIV2	FREQUENCY OF CLK	FREQUENCY OF CLKOUT
HIGH	LOW	HIGH	LOW	$^1/_2f_{INT}$	$^1/_2f_{INT}$
HIGH	LOW	LOW	LOW	$^1/_4f_{XTAL}$	f_{XTAL}
HIGH	LOW	LOW	HIGH	$^1/_2f_{XTAL}$	f_{XTAL}
HIGH	LOW	HIGH	HIGH	STOP LOW	f_{XTAL}
HIGH	HIGH	X	X	STROBE	f_{XTAL}
LOW(2)	X	X	X	STOP LOW	$^1/_2f_{INT}$(2)

Notes

1. X = don't care.
2. In low-power mode.

I/O Circuitry

The three I/O lines are identical. The idle state is HIGH for all I/O (i.e. I/O, I/OUC, AUX1, AUX1UC, AUX2, AUX2UC). I/O is referenced to V_{CC}, I/OUC to V_{DD}, ensuring proper operation in case $V_{CC} \neq V_{DD}$.

The first side on which a falling edge is detected becomes a master (input). An anti-latch circuitry first disables the detection of the falling edge on the other side, which becomes slave (output).

After a delay time t_d (about 50 ns), the LOW level signal present on the master side is transferred to the slave side.

When the input returns to HIGH level, a current booster is activated at the output side during delay t_d. Now both sides return to their idle state, ready to detect another LOW level signal on any side.

In case of a conflict, both lines may remain LOW until the software enables the lines to be HIGH. The anti-latch circuitry ensures that the lines do not remain LOW if both sides return HIGH, regardless of the prior conditions. The maximum frequency on the lines is approximately 1 MHz.

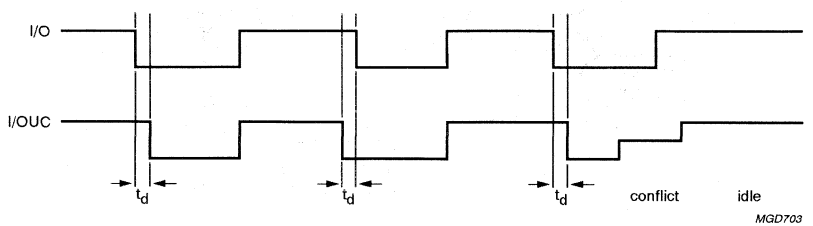


Fig.6 Master and slave signals.

Logic circuitry

After power-up, the circuit has seven possible states of operation. Figure 7 shows the sequence of these states.

IDLE MODE

After reset, the circuit enters the idle mode.
A minimum number of functions in the circuit are active while waiting for the microcontroller to start a session:

- All card contacts are inactive
- I/OUC, AUX1UC and AUX2UC are high impedance
- Oscillator XTAL runs, delivering CLKOUT
- Voltage supervisor is active.

LOW-POWER (SLEEP) MODE

When pin MODE goes LOW, the circuit enters the low-power (sleep) mode. As long as pin MODE is LOW, no activation is possible.

If pin MODE goes LOW in the active mode, a normal deactivation sequence is performed before entering low-power mode. When pin MODE goes HIGH, the circuit enters normal operation after a delay of at least 6 ms (96 cycles of CLKOUT). During this time CLKOUT remains at 16 kHz.

- All card contacts are inactive
- Oscillator XTAL does not run
- The V_{DD} supervisor, ALARM output, card presence detection and $\overline{OFF}$ output remain functional
- Internal oscillator is slowed to 32 kHz, CLKOUT providing 16 kHz.

ACTIVE MODE

When the activation sequence is completed, the TDA8002 will be in the active mode. Data is exchanged between the card and the microcontroller via the I/O lines.

State diagram

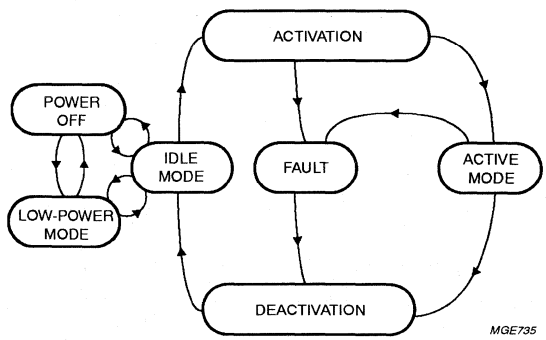


Fig.7 State Diagram.

ACTIVATION SEQUENCE

From idle mode, the circuit enters the activation mode when the microcontroller sets the $\overline{\text{CMDVCC}}$ line LOW or sets the MODE line HIGH when the $\overline{\text{CMDVCC}}$ line is already LOW. The internal circuitry is then activated, the internal clock is activated and an activation sequence is performed. When RST is enabled, RST becomes the inverse of RSTIN.

- Step-up converter is started ($t_1 \sim t_0$)
- V_{CC} rises from 0 to 5 V ($t_2 = t_1 + 1\frac{1}{2}T$)
- I/O, AUX1, AUX2 are enabled and CLK is enabled ($t_3 = t_1 + 4T$); a special circuitry ensures that I/O remains below V_{CC} during falling slope of V_{CC}
- CLK is sent by setting RSTIN to HIGH (t_4)
- RST is enabled ($t_5 = t_1 + 7T$); after t_5, RSTIN has no further action on CLK, but is only controlling RST.

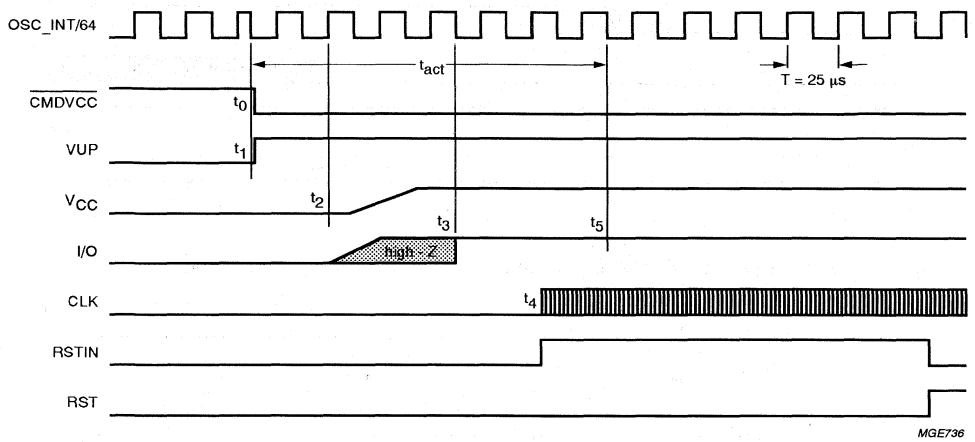


Fig.8 Activation sequence using RSTIN and $\overline{\text{CMDVCC}}$.

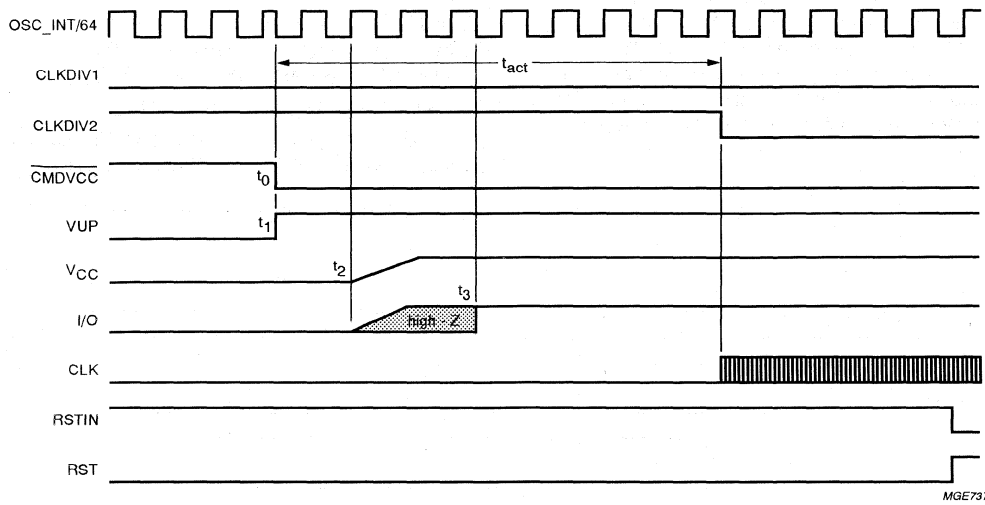


Fig.9 Activation sequence using $\overline{\text{CMDVCC}}$, CLKDIV1 and CLKDIV2 signals to enable CLK.

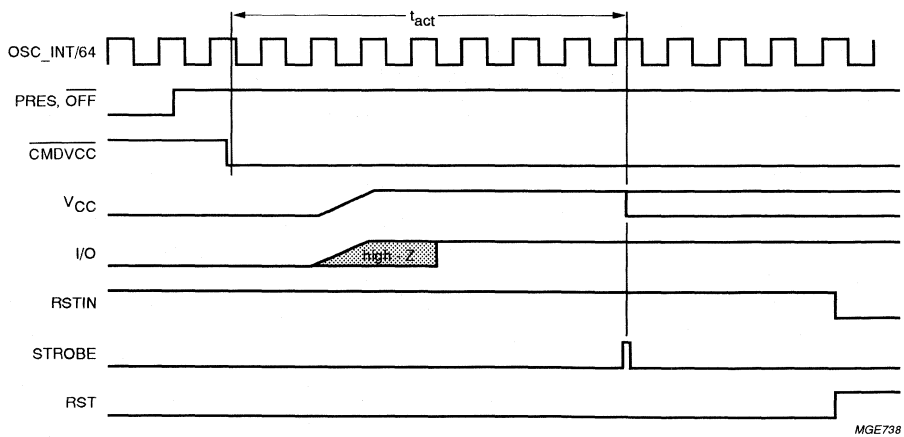


Fig.10 Activation sequence for synchronous application.

DEACTIVATION SEQUENCE

When a session is completed, the microcontroller sets the $\overline{\text{CMDVCC}}$ line to HIGH state or MODE line to LOW state. The circuit then executes an automatic deactivation sequence by counting the sequencer back and ends in idle mode.

- RST goes LOW ($t_{11} = t_{10}$)
- CLK is stopped ($t_{12} = t_{11} + \frac{1}{2}T$)
- I/O, AUX1, AUX2 are outputs into high-impedance state ($t_{13} = t_{11} + T$)
- V_{CC} falls to zero ($t_{14} = t_{11} + 1\frac{1}{2}T$); a special circuitry ensures that I/O remains below V_{CC} during falling slope of V_{CC}
- VUP falls ($t_{15} = t_{11} + 5T$).

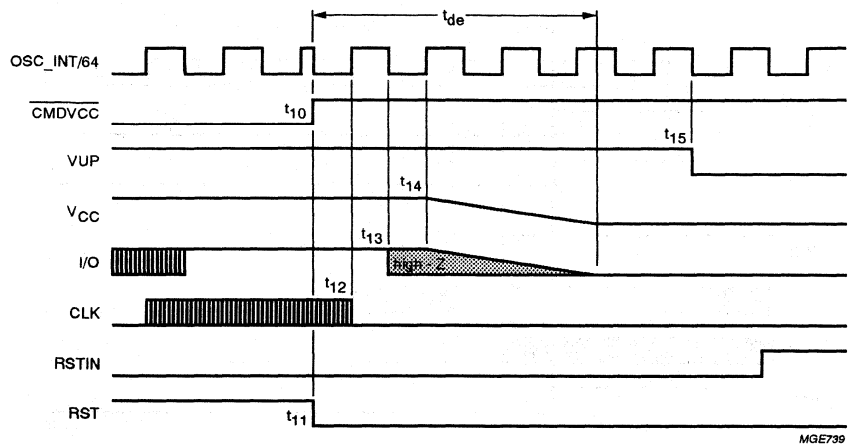


Fig.11 Deactivation sequence.

Fault detection

The following fault conditions are monitored by the circuit:

- Short-circuit or high current on V_{CC}
- Removing card during transaction
- V_{DD} dropping
- Overheating.

When any one of these faults are detected, the circuit pulls the interrupt line $\overline{OFF}$ to its active LOW state and a deactivation sequence is initiated. After completion of the deactivation sequence, $\overline{OFF}$ is set to HIGH when the microcontroller has reset the $\overline{CMDVCC}$ line HIGH if the card is present. If the card is not present then $\overline{OFF}$ remains LOW.

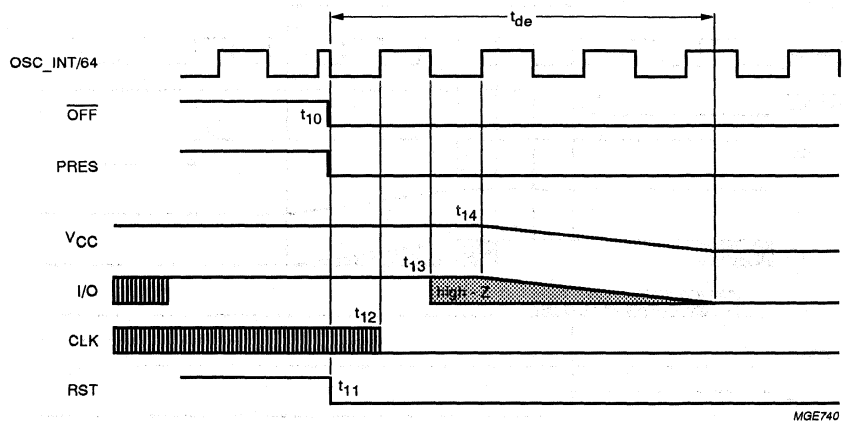


Fig.12 Emergency deactivation sequence.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+6.5	V
VX1	voltage on CMOS pins: XTAL1, XTAL2, ALARM, $\overline{ALARM}$, MODE, RSTIN, CLKSEL, AUX2UC, AUX1UC, CLKDIV1, CLKDIV2, CLKOUT, STROBE, $\overline{CMDVCC}$, $\overline{OFF}$, DELAY		−0.3	+6.5	V
VX2	voltage on card contact pins		−0.3	+6.5	V
V_{es}	electrostatic voltage				
	on pins: I/O, RST, V_{CC}, CLK, AUX1, AUX2, PRES, $\overline{PRES}$		−6	+6	kV
	on all other pins		−2	+2	kV
T_{stg}	storage temperature		−55	+125	°C
P_{tot}	continuous total power dissipation				
	TDA8002T	T_{amb} = −25 to +85 °C	−	0.56	W
	TDA8002G	T_{amb} = −25 to +85 °C	−	0.46	W
T_j	junction temperature		−	+150	°C

Note

1. Stress beyond these levels may cause permanent damage to the device. This is a stress rating only and functional operation of the device under this condition is not implied.

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses positive and 3 pulses negative on each pin referenced to ground.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT136-1	70	K/W
	SOT401-1	91	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; f_{XTAL} = 10 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Temperature						
T_{amb}	operating ambient temperature		−25	−	+85	°C
Supply						
V_{DD}	positive supply voltage		3.0	5	6.5	V
I_{DD}	supply current	low-power mode; V_{DD} = 5 V	−	−	150	μA
		idle mode; V_{DD} = 5 V; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz	−	−	5	mA
		active mode; V_{DD} = 5 V; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz	−	−	9	mA
		active mode; V_{DD} = 3 V; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz	−	−	12	mA
V_{th2}	threshold voltage on V_{DD} (falling) for voltage supervisor	option 5 V power supply (TDA8002XX/5)	4.3	4.4	4.5	V
		option 3.3 V or 5 V power supply (TDA8002XX/3)	2.5	−	2.6	V
V_{hys2}	hysteresis on V_{th2}		30	50	70	mV
CARD SUPPLY VOLTAGE (V_{CC})						
V_{CC}	output voltage	idle mode	−	−	0.4	V
		active mode; I_{CC} < 20 mA: DC load with 3 V < V_{DD} < 3.3 V	4.75	−	5.25	V
		active mode; I_{CC} < 65 mA: DC load with 3.3 V < V_{DD} < 6.5 V	4.75	−	5.25	V
		active mode; I_{CC} = 40 nA; AC load	4.6	−	5.4	V
I_{CC}	output current	from 0 to 5 V	−	−	65	mA
		V_{CC} short-circuited to ground	−	−	100	mA
SR	slew rate	up and down; note 1	0.1	0.14	0.18	V/μs
Crystal connections (XTAL1 and XTAL2)						
C_{ext}	external capacitors	note 2	−	15	−	pF
f_{XTAL}	resonance frequency	note 3	2	−	24	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data lines (I/O, I/OUC, AUX1, AUX2, AUX1UC, AUX2UC)						
V_{OH}	HIGH level output voltage on I/O	I_{OH} = −20 μA	V_{CC} − 0.5	−	V_{CC} + 0.1	V
		I_{OH} = −100 μA	3.5	−	−	V
V_{OL}	LOW level output voltage on I/O	$I_{I/O}$ = 1 mA	−	−	300	mV
V_{OH}	HIGH level output voltage on I/OUC	I_{OH} = −20 μA	V_{DD} − 0.5	−	V_{DD} + 0.2	V
V_{OL}	LOW level output voltage on I/OUC	$I_{I/OUC}$ = 1 mA	−	−	300	mV
V_{IH}	HIGH level output voltage on I/O		0.65V_{CC}	−	V_{CC}	V
V_{IL}	LOW level input voltage on I/O		0	−	1.5	V
V_{IH}	HIGH level input voltage on I/OUC	option 5 V power supply (TDA8002XX/5)	3.5	−	V_{DD}	V
		option 3.3 V or 5 V power supply (TDA8002XX/3)	2.2	−	V_{DD}	V
V_{IL}	LOW level input voltage on I/OUC	option 5 V power supply (TDA8002XX/5)	0	−	1.5	V
		option 3.3 V or 5 V power supply (TDA8002XX/3)	0	−	0.8	V
$V_{I/O(idle)}$	voltage on I/O outside a session	idle mode	−	−	0.4	V
$Z_{I/OUC(idle)}$	impedance on I/OUC outside a session	idle mode	10	−	−	MΩ
R_{pu}	internal pull-up resistance between I/O and V_{CC}		8	10	12	kΩ
I_{edge}	current from I/O when active pull-up is active		−	1	−	mA
t_{edge}	delay between falling edge on I/O and I/OUC		−	100	−	ns
	delay between falling edge on I/OUC and I/O		−	100	−	ns
I_{IL}	LOW level current on I/O	V_{IL} = 0.4 V	−	−	−600	μA
I_{IH}	HIGH level current on I/O	V_{IH} = V_{CC}	−	−	10	μA
t_r, t_f	rise and fall times	C_i = C_o = 30 pF	−	−	0.5	μs
ALARM, $\overline{\text{ALARM}}$, $\overline{\text{OFF}}$ (open-drain outputs) when connected						
I_{OH}	HIGH level output current on pin $\overline{\text{ALARM}}$	V_{OH} = 5 V	−	−	5	μA
V_{OL}	LOW level output voltage on pin $\overline{\text{ALARM}}$	I_{OL} = 2 mA	−	−	0.4	V
I_{OH}	HIGH level output current on pin $\overline{\text{OFF}}$	V_{OH} = 5 V	−	−	5	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OL}	LOW level output voltage on pin $\overline{OFF}$	I_{OL} = 2 mA	–	–	0.4	V
I_{OL}	LOW level output current on pin ALARM	V_{OL} = 0 V	–	–	−5	μA
V_{OH}	HIGH level output voltage on pin ALARM	I_{OH} = −2 mA	V_{DD} − 1	–	–	V
t_W	ALARM pulse width		7	–	12	ms
Clock output (CLKOUT) (powered from V_{DD})						
f_{CLKOUT}	frequency on CLKOUT		0	–	20	MHz
		LOW power	–	16	–	kHz
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = −1 mA	V_{DD} − 0.5	–	–	V
t_r, t_f	rise and fall times	C_L = 15 pF; notes 4 and 5	–	–	8	ns
δ	duty factor	C_L = 15 pF; note 4	40	–	60	%
Internal oscillator						
f_{INT}	frequency of internal oscillator	active mode	2	–	3	MHz
		low-power mode	–	32	–	kHz
Reset output to the card (RST)						
$V_{O(idle)}$	output voltage	idle mode	0	–	0.3	V
t_{rst}	delay between RSTIN and RST	RST enabled	–	–	100	ns
V_{OL}	LOW level output voltage	I_{OL} = 200 μA	0	–	0.3	V
V_{OH}	HIGH level output voltage	I_{OH} = −200 μA	4.3	–	V_{CC}	V
		I_{OH} = −50 μA	V_{CC} − 0.5	–	V_{CC}	V
Clock output to the card (CLK)						
$V_{O(idle)}$	output voltage	idle mode	0	–	0.3	V
V_{OL}	LOW level output voltage	I_{OL} = 200 μA	0	–	0.3	V
V_{OH}	HIGH level output voltage	I_{OH} = −50 μA	V_{CC} − 0.5	–	V_{CC}	V
t_r	rise time	C_L = 30 pF; note 4	–	–	8	ns
t_f	fall time	C_L = 30 pF; note 4	–	–	8	ns
δ	duty factor	C_L = 30 pF; note 4	45	–	55	%
SR	slew rate (rise and fall)		0.2	–	–	V/ns
Strobe input (STROBE)						
f_{STROBE}	frequency on STROBE		0	–	20	MHz
V_{IL}	LOW level input voltage	option 5 V power supply (TDA8002XX/5)	0	–	1.5	V
		option 3.3 V or 5 V power supply (TDA8002XX/3)	0	–	0.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH level input voltage	option 5 V power supply (TDA8002XX/5)	3.5	–	V_{DD}	V
		option 3.3 V or 5 V power supply (TDA8002XX/3)	2.2	–	V_{DD}	V
Logic inputs (CLKSEL, CLKDIV1, CLKDIV2, PRES, $\overline{\text{PRES}}$, MODE, $\overline{\text{CMDVCC}}$ and RSTIN); note 6						
V_{IL}	LOW level input voltage	option 5 V power supply (TDA8002XX/5)	0	–	1.5	V
		option 3.3 V or 5 V power supply (TDA8002XX/3)	0	–	0.8	V
V_{IH}	HIGH level input voltage	option 5 V power supply (TDA8002XX/5)	3.5	–	V_{DD}	V
		option 3.3 V or 5 V power supply (TDA8002XX/3)	2.2	–	V_{DD}	V
$I_{IL(PRES)}$	LOW level input voltage on pin PRES	V_{OL} = 0 V	–	–	−10	μA
$I_{IH(PRES)}$	HIGH level input voltage on pin PRES		–	–	10	μA
Protections						
T_{sd}	shut-down local temperature		–	135	–	°C
$I_{CC(sd)}$	shut-down current at V_{CC}		–	–	90	mA
Timing						
t_{act}	activation sequence duration	see Fig.9; guaranteed by design	–	180	220	μs
t_{de}	deactivation sequence duration	see Fig.11; guaranteed by design	60	80	100	μs
t_3	start of the window for sending CLK to the card		–	–	130	μs
t_5	end of the window for sending CLK to the card		150	–	–	μs

Notes

1. The tests for dynamic response of V_{CC} are done at 1 Hz, 10 kHz, 100 kHz and 1 MHz, with a capacitive load of 100 nF.
2. It may be necessary to put capacitors from XTAL1 and XTAL2 to ground depending on the choice of crystal or resonator.
3. When the oscillator is stopped in mode 1, XTAL1 is set to HIGH.
4. The transition time and duty cycle definitions are shown in Fig.13; $\delta = \frac{t_1}{t_1 + t_2}$.
5. CLKOUT transition time and duty cycle do not need to be tested.
6. $\overline{\text{PRES}}$ and $\overline{\text{CMDVCC}}$ are active LOW; RSTIN and PRES are active HIGH.

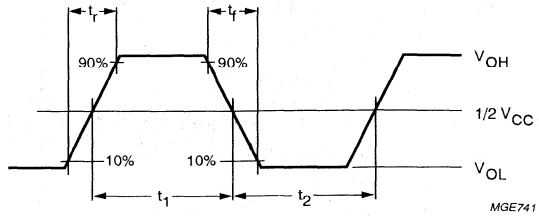


Fig.13 Definition of transition times.

APPLICATION INFORMATION

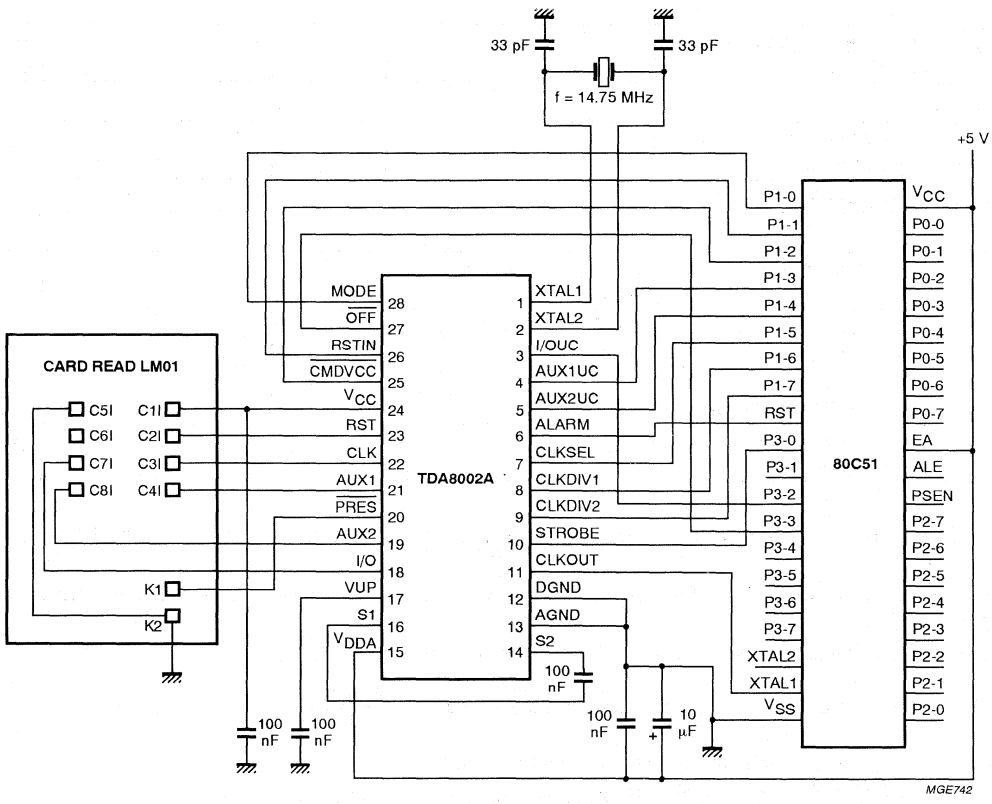


Fig.14 Application diagram (for more details, consult Application Note *"AN96096"*).

Low-power smart card coupler TDA8005

FEATURES

- V_{CC} generation (5 V ±5%, 20 mA maximum with controlled rise and fall times)
- Clock generation (up to 8 MHz), with two times synchronous frequency doubling
- Clock STOP HIGH, clock STOP LOW or 1.25 MHz (from internal oscillator) for cards power-down mode
- Specific UART on I/O for automatic direct/inverse convention settings and error management at character level
- Automatic activation and deactivation sequences through an independent sequencer
- Supports the protocol T = 0 in accordance with ISO 7816, GSM11.11 requirements (Global System for Mobile communication); and EMV banking specification approved for Final GSM11.11 Test Approval (FTA)
- Several analog options are available for different applications (doubler or tripler DC/DC converter, card presence, active HIGH or LOW, threshold voltage supervisor, etc.
- Overloads and take-off protections
- Current limitations in the event of short-circuit
- Special circuitry for killing spikes during power-on or off
- Supply supervisor
- Step-up converter (supply voltage from 2.5 to 6 V)
- Power-down and sleep mode for low-power consumption
- Enhanced ESD protections on card side (6 kV minimum)
- Control and communication through a standard RS232 full duplex interface
- Optional additional I/O ports for:
  - keyboard
  - LEDs
  - display
  - etc.
- 80CL51 microcontroller core with 4 kbytes ROM and 256-byte RAM.

APPLICATIONS

- Portable smart card readers for protocol T = 0
- GSM mobile phones.

GENERAL DESCRIPTION

The TDA8005 is a low cost card interface for portable smart card readers. Controlled through a standard serial interface, it takes care of all ISO 7816 and GSM11-11 requirements. It gives the card and the set a very high level of security, due to its special hardware against ESD, short-circuiting, power failure, etc. Its integrated step-up converter allows operation within a supply voltage range of 2.5 to 6 V.

The very low-power consumption in Power-down and sleep modes saves battery power. A special version where the internal connections to the controller are fed outside through pins allows easy development and evaluation, together with a standard 80CL51 microcontroller.

Development tools, application report and support (hardware and software) are available.

The device can be supplied either as a masked chip with standard software handling all communication between smart card and a master controller in order to make the application easier, or as a maskable device.

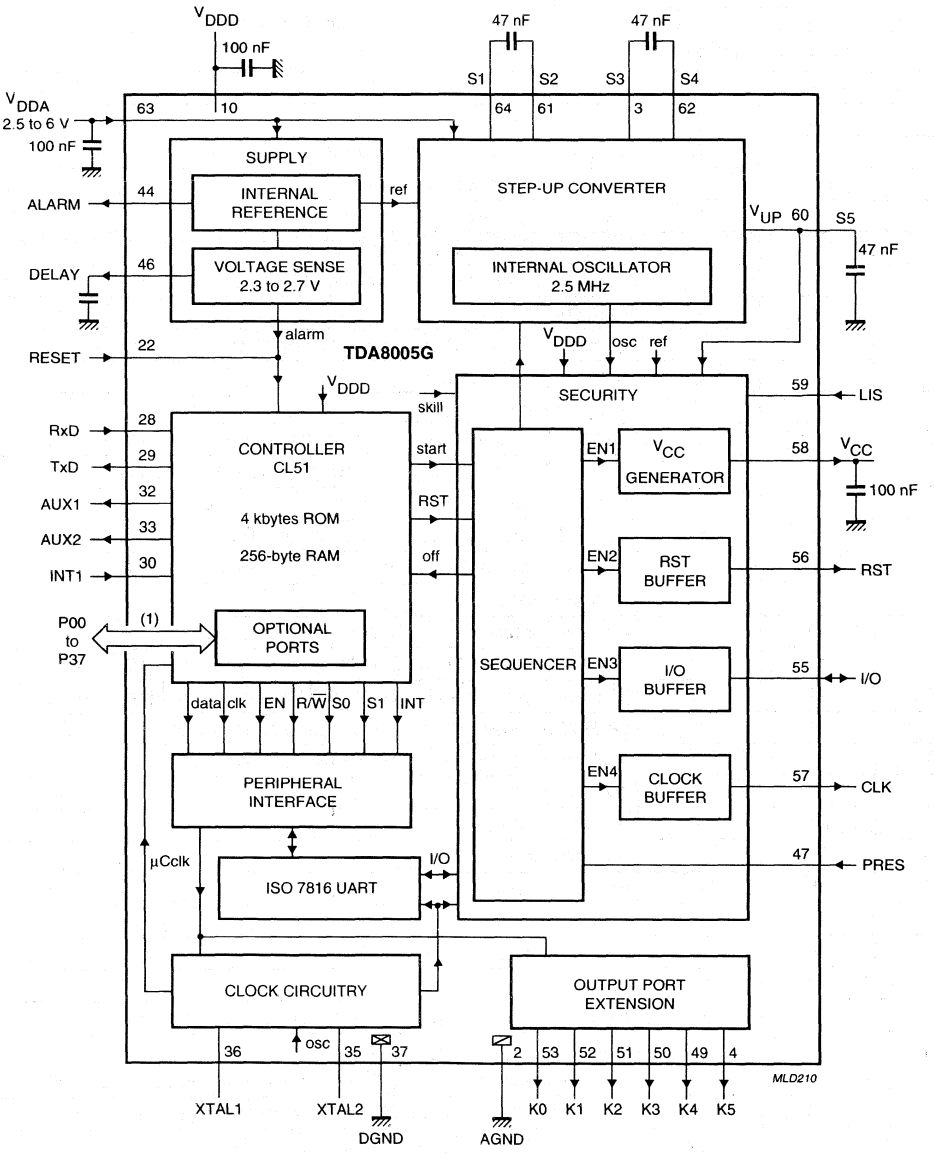
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	doubler and tripler option	2.5	–	6.0	V
$I_{DD(pd)}$	supply current in power-down mode	V_{DD} = 5 V; card inactive	–	–	100	µA
$I_{DD(sm)}$	supply current in sleep mode doubler	card powered but clock stopped	–	–	500	µA
$I_{DD(sm)}$	supply current in sleep mode tripler	card powered but clock stopped	–	–	500	µA
$I_{DD(om)}$	supply current in operating mode	unloaded; f_{xtal} = 13 MHz; $f_{\mu C}$ = 6.5 MHz; f_{card} = 3.25 MHz	–	–	5.5	mA
V_{CC}	card supply voltage	including static and dynamic loads on 100 nF capacitor	4.75	5.0	5.25	V
I_{CC}	card supply current	operating	–	–	20	mA
		limitation	–	–	30	mA
SR	slew rate on V_{CC} (rise and fall)	maximum load capacitor 150 nF (including typical 100 nF decoupling)	0.05	0.1	0.15	V/µs
t_{de}	deactivation cycle duration		–	–	100	µs
t_{act}	activation cycle duration		–	–	100	µs
f_{xtal}	crystal frequency		2	–	16	MHz
T_{amb}	operating ambient temperature		–25	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8005G	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
TDA8005H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM



(1) For details see Chapter "Pinning".

Fig.1 Block diagram (LQFP64; SOT314-2).

PINNING

SYMBOL	PIN		DESCRIPTION
	LQFP64 SOT314-2	QFP44 SOT307-2	
n.c.	1	–	not connected
AGND	2	1	analog ground
S3	3	2	contact 3 for the step-up converter
K5	4	–	output port from port extension
P03	5	3	general purpose I/O port (connected to P03)
P02	6	4	general purpose I/O port (connected to P02)
P01	7	5	general purpose I/O port (connected to P01)
n.c.	8	–	not connected
P00	9	6	general purpose I/O port (connected to P00)
V_{DDD}	10	7	digital supply voltage
n.c.	11	–	not connected
TEST1	12	8	test pin 1 (connected to P10; must be left open-circuit in the application)
P11	13	9	general purpose I/O port or interrupt (connected to P11)
P12	14	10	general purpose I/O port or interrupt (connected to P12)
P13	15	11	general purpose I/O port or interrupt (connected to P13)
P14	16	12	general purpose I/O port or interrupt (connected to P14)
n.c.	17	–	not connected
P15	18	13	general purpose I/O port or interrupt (connected to P15)
P16	19	14	general purpose I/O port or interrupt (connected to P16)
TEST2	20	15	test pin 2 (connected to PSEN; must be left open-circuit in the application)
P17	21	16	general purpose I/O port or interrupt (connected to P17)
RESET	22	17	input for resetting the microcontroller (active HIGH)
n.c.	23	–	not connected
n.c.	24	–	not connected
n.c.	25	–	not connected
n.c.	26	–	not connected
n.c.	27	–	not connected
RxD	28	18	serial interface receive line
TxD	29	19	serial interface transmit line
INT1	30	20	general purpose I/O port or interrupt (connected to P33)
T0	31	21	general purpose I/O port (connected to P34)
AUX1	32	22	push-pull auxiliary output (±5 mA; connected to timer T1 e.g. P35)
AUX2	33	23	push-pull auxiliary output (±5 mA; connected to timer P36)
P37	34	24	general purpose I/O port (connected to P37)
XTAL2	35	25	crystal connection
XTAL1	36	26	crystal connection or external clock input
DGND	37	27	digital ground
n.c.	38	–	not connected

SYMBOL	PIN		DESCRIPTION
	LQFP64 SOT314-2	QFP44 SOT307-2	
n.c.	39	–	not connected
P20	40	28	general purpose I/O port (connected to P20)
P21	41	–	general purpose I/O port (connected to P21)
P22	42	29	general purpose I/O port (connected to P22)
P23	43	30	general purpose I/O port (connected to P23)
ALARM	44	–	open-drain output for Power-On Reset (active HIGH or LOW by mask option)
n.c.	45	–	not connected
DELAY	46	31	external capacitor connection for delayed reset signal
PRES	47	32	card presence contact input (active HIGH or LOW by mask option)
TEST3	48	33	test pin 3 (must be left open-circuit in the application)
K4	49	–	output port from port extension
K3	50	–	output port from port extension
K2	51	–	output port from port extension
K1	52	–	output port from port extension
K0	53	–	output port from port extension
TEST4	54	34	test pin 4 (must be left open-circuit in the application)
I/O	55	35	data line to/from the card (ISO C7 contact)
RST	56	36	card reset output (ISO C2 contact)
CLK	57	37	clock output to the card (ISO C3 contact)
V_{CC}	58	38	card supply output voltage (ISO C1 contact)
LIS	59	39	supply for low-impedance on cards contacts
S5	60	40	contact 5 for the step-up converter
S2	61	41	contact 2 for the step-up converter
S4	62	42	contact 4 for the step-up converter
V_{DDA}	63	43	analog supply voltage
S1	64	44	contact 1 for the step-up converter

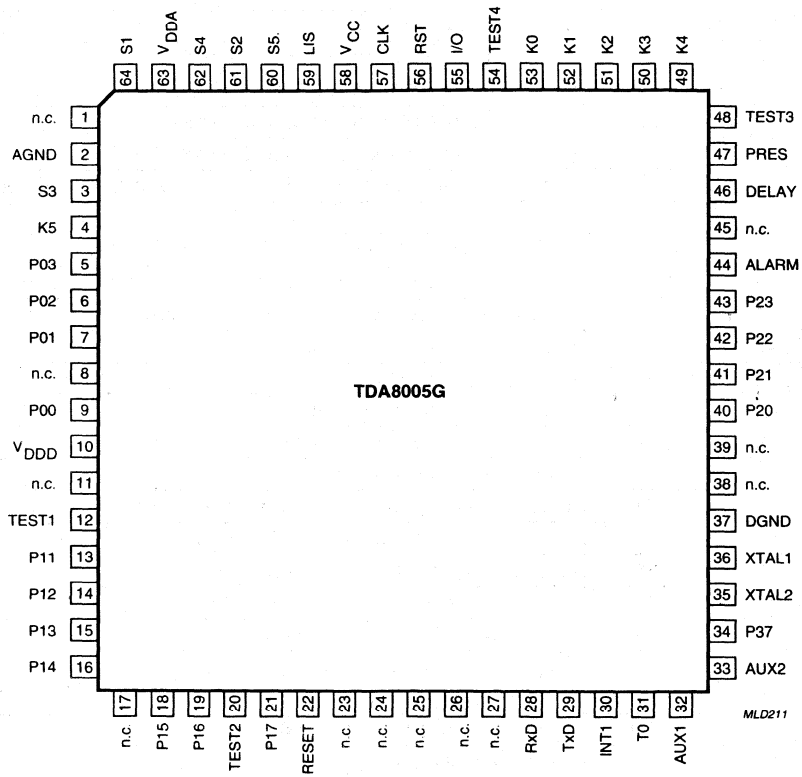


Fig.2 Pin configuration (LQFP64; SOT314-2).

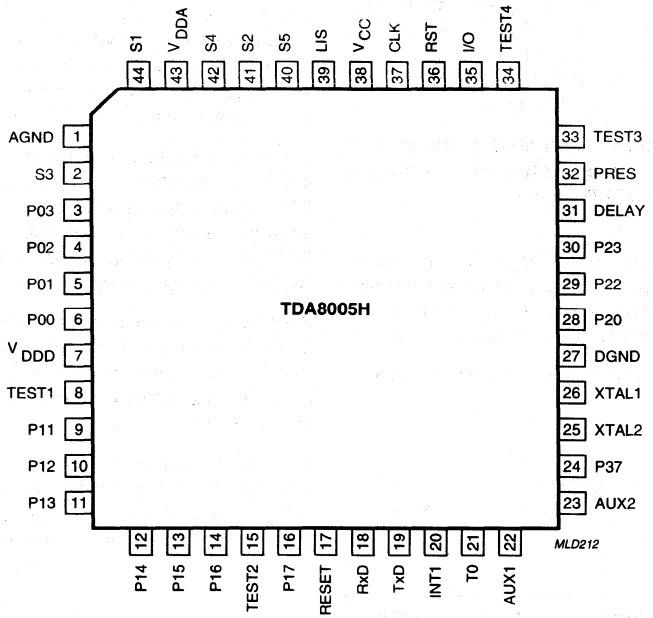


Fig.3 Pin configuration (QFP44; SOT307-2).

FUNCTIONAL DESCRIPTION

Microcontroller

The microcontroller is an 80CL51 with 256 bytes of RAM instead of 128. The baud rate of the UART has been multiplied by four in modes 1, 2 and 3 (which means that the division factor of 32 in the formula is replaced by 8 in both reception and transmission, and that in the reception modes, only four samples per bit are taken with decision on the majority of samples 2, 3 and 4) and the delay counter has been reduced from 1536 to 24.

Remark: this has an impact when getting out of PDOWN mode. It is recommended to switch to internal clock before entering PDOWN mode (see *"application report"*).

All the other functions remain unchanged. Please, refer to the published specification of the 80CL51 for any further information. Pins INT0, P10, P04 to P07 and P24 to P27 are used internally for controlling the smart card interface.

Mode 0 is unchanged. The baud rate for modes 1 and 3 is:

$$\frac{2^{SMOD}}{8} \times \frac{f_{clk}}{12 \times (256 - TH1)}$$

The baud rate for mode 2 is: $\frac{2^{SMOD}}{16} \times f_{clk}$

Table 1 Mode 3 timing

BAUD RATE	f_{clk} = 6.5 MHz; V_{DD} = 5 V		f_{clk} = 3.25 MHz; V_{DD} = 5 or 3 V	
	SMOD	TH1	SMOD	TH1
135416	1	255	–	–
67708	0	255	1	255
45139	1	253	–	–
33854	0	254	0	255
27083	1	251	–	–
22569	0	253	1	253
16927	–	–	0	254
13542	–	–	1	251
11285	0	250	0	253

Supply

The circuit operates within a supply voltage range of 2.5 to 6 V. The supply pins are V_{DDD}, DGND and AGND. Pins V_{DDA} and AGND supply the analog drivers to the card and have to be externally decoupled because of the large current spikes that the card and the step-up converter can create. An integrated spike killer ensures the contacts to the card remain inactive during power-up or power-down. An internal voltage reference is generated which is used within the step-up converter, the voltage supervisor, and the V_{CC} generator.

The voltage supervisor generates an alarm pulse, whose length is defined by an external capacitor tied to the DELAY pin, when V_{DDD} is too low to ensure proper operation (1 ms per 1 nF typical). This pulse is used as a RESET pulse by the controller, in parallel with an external RESET input, which can be tied to the system controller.

It is also used in order to either block any spurious card contacts during controllers reset, or to force an automatic deactivation of the contacts in the event of supply drop-out [see Sections "Activation sequence" and "Deactivation sequence (see Fig.10)"].

In the 64 pin version, this reset pulse is output to the open drain ALARM pin, which may be selected active HIGH or active LOW by mask option and may be used as a reset pulse for other devices within the application.

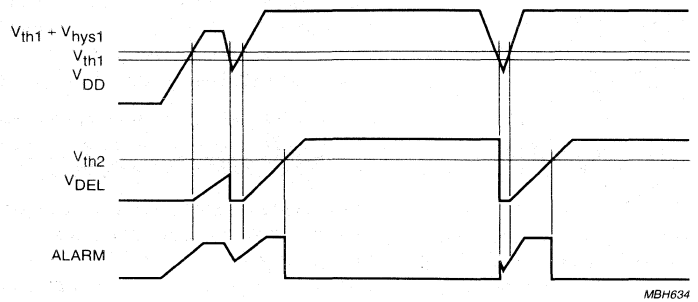


Fig.4 Supply supervisor.

Low impedance supply (pin LIS)

For some applications, it is mandatory that the contacts to the card (V_{CC}, RST, CLK and I/O) are low impedance while the card is inactive and also when the coupler is not powered. An auxiliary supply voltage on pin LIS ensures this condition where I_{LIS} = <5 µA for V_{LIS} = 5 V. This low impedance situation is disabled when V_{CC} starts rising during activation, and re-enabled when the step-up converter is stopped during deactivation. If this feature is not required, the LIS pin must be tied to V_{DD}.

Step-up converter

Except for the V_{CC} generator, and the other cards contacts buffers, the whole circuit is powered by V_{DDD} and V_{DDA}. If the supply voltage is 3 V or 5 V, then a higher voltage is needed for the ISO contacts supply. When a card session is requested by the controller, the sequencer first starts the step-up converter, which is a switched capacitors type, clocked by an internal oscillator at a frequency approximately 2.5 MHz. The output voltage, V_{UP}, is regulated at approximately 6,5 V and then fed to the V_{CC} generator. V_{CC} and GND are used as a reference for all other cards contacts. The step-up converter may be chosen as a doubler or a tripler by mask option, depending on the voltage and the current needed on the card.

ISO 7816 security

The correct sequence during activation and deactivation of the card is ensured through a specific sequencer, clocked by a division ratio of the internal oscillator.

Activation (START signal P05) is only possible if the card is present (PRES HIGH or LOW according to mask option), and if the supply voltage is correct (ALARM signal inactive), CLK and RST are controlled by RSTIN (P04), allowing the correct count of CLK pulses during Answer-to-Reset from the card.

The presence of the card is signalled to the controller by the OFF signal (P10).

During a session, the sequencer performs an automatic emergency deactivation in the event of card take-off, supply voltage drop, or hardware problems. The OFF signal falls thereby warning the controller.

Clock circuitry

The clock to the microcontroller and the clock to the card are derived from the main clock signal (XTAL from 2 to 16 MHz, or an external clock signal).

Microcontroller clock (f_{clk}) after reset, and during power reduction modes, the microcontroller is clocked with $f_{INT}/8$, which is always present because it is derived from the internal oscillator and gives the lowest power consumption. When required, (for card session, serial communication or anything else) the microcontroller may choose to clock itself with $\frac{1}{2}f_{xtal}$, $\frac{1}{4}f_{xtal}$ or $\frac{1}{2}f_{INT}$. All frequency changes are synchronous, thereby ensuring no hang-up due to short spikes etc.

Cards clock: the microcontroller may select to send the card $\frac{1}{2}f_{xtal}$, $\frac{1}{4}f_{xtal}$, $\frac{1}{8}f_{xtal}$ or $\frac{1}{2}f_{INT}$ (≈1.25 MHz), or to stop the clock HIGH or LOW. All transition are synchronous, ensuring correct pulse length during start or change in accordance with ISO 7816.

After power on, CLK is set at STOP LOW, and f_{clk} is set at $\frac{1}{8}f_{INT}$.

Power-down and sleep modes

The TDA8005 offers a large flexibility for defining power reduction modes by software. Some configurations are described below.

In the power-down mode, the microcontroller is in power-down and the supply and the internal oscillator are active. The card is not active; this is the smallest power consumption mode. Any change on P1 ports or on PRES will wake-up the circuit (for example, a key pressed on the keyboard, the card inserted or taken off).

In the sleep mode, the card is powered, but configured in the Idle or sleep mode. The step-up converter will only be active when it is necessary to reactivate V_{UP}. When the microcontroller is in Power-down mode any change on P1 ports or on PRES will wake up the circuit.

In both power reduction modes the sequencer is active, allowing automatic emergency deactivation in the event of card take-off, hardware problems, or supply drop-out.

The TDA8005 is set into Power-down or sleep mode by software. There are several ways to return to normal mode, Introduction or extraction of the card, detection of a change on P1 (which can be a key pressed) or a command from the system microcontroller. For example, if the system monitors the clock on XTAL1, it may stop this clock after setting the device into power-down mode and then wake it up when sending the clock again. In this situation, the internal clock should have been chosen before the f_{clk}.

Peripheral interface

This block allows synchronous serial communication with the three peripherals (ISO UART, CLOCK CIRCUITRY and OUTPUT PORTS EXTENSION).

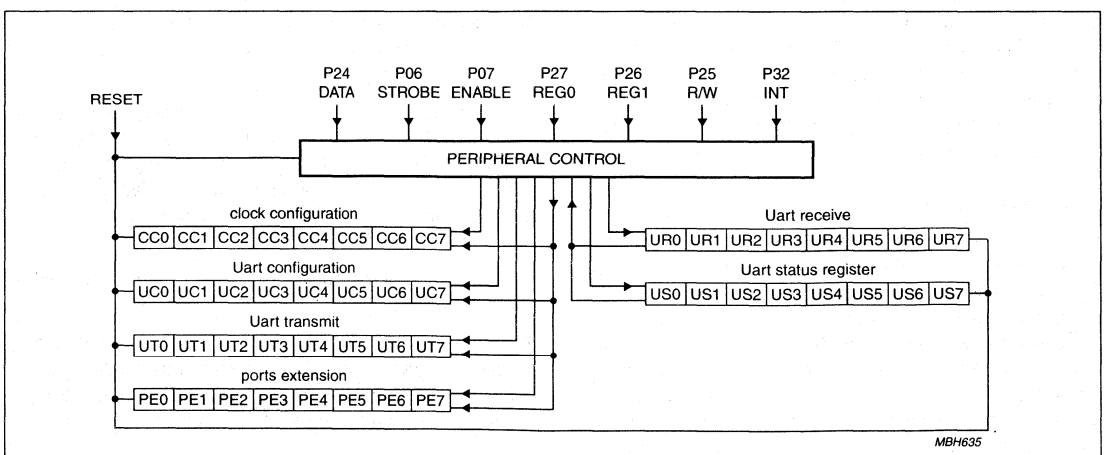


Fig.5 Peripheral interface diagram.

Table 2 Description of Fig.5

BIT NAME	DESCRIPTION
REG0 = 0, REG1 = 0, R/W = 0; CLOCK CONFIGURATION (Configuration after reset is cards clock STOP LOW, $f_{clk} = 1/8 f_{INT}$)	
CC0	cards clock = $1/2 f_{xtal}$
CC1	cards clock = $1/4 f_{xtal}$
CC2	cards clock = $1/8 f_{xtal}$
CC3	cards clock = $1/2 f_{INT}$
CC4	cards clock = STOP HIGH
CC5	$f_{clk} = 1/2 f_{xtal}$
CC6	$f_{clk} = 1/4 f_{xtal}$
CC7	$f_{clk} = 1/2 f_{INT}$
REG0 = 1, REG1 = 0, R/W = 0; UART CONFIGURATION (after reset all bits are cleared)	
UC0	ISO UART RESET
UC1	START SESSION
UC2	LCT (Last Character to Transmit)
UC3	TRANSMIT/RECEIVE
UC4 to UC7	not used
REG0 = 0, REG1 = 1, R/W = 0; UART TRANSMIT	
UT0 to UT7	LSB to MSB of the character to be transmitted to the card
REG0 = 1, REG1 = 1, R/W = 0; PORTS EXTENSION (after reset all bits are cleared)	
PE0 to PE5	PE0 to PE5 is the inverse of the value to be written on K0 to K5
PE6, PE7	not used
REG0 = 0, REG1 = 0, R/W = 1; UART RECEIVE	
UR0 to UR7	LSB to MSB of the character received from the card
REG0 = 1, REG1 = 0, R/W = 1; UART STATUS REGISTER (after reset all bits are cleared)	
US0	UART TRANSMIT buffer empty
US1	UART RECEIVE buffer full
US2	first start bit detected
US3	parity error detected during reception of a character (the UART has asked the card to repeat the character)
US4	parity error detected during transmission of a character. The controller must write the previous character in UART TRANSMIT, or abort the session.
US5 to US7	not used

USE OF PERIPHERAL INTERFACE

Write operation:

Select the correct register with R/W, REG0, REG1.

Write the word in the peripheral shift register (PSR) with DATA and STROBE. DATA is shifted on the rising edge of STROBE. 8 shifts are necessary.

Give a negative pulse on ENABLE. The data is parallel loaded in the register on the falling edge of ENABLE.

Read operation:

Select the correct register with R/W, REG0 and REG1.

Give a first negative pulse on ENABLE. The word is parallel loaded in the peripheral shift register on the rising edge of ENABLE.

Give a second negative pulse on ENABLE for configuring the PSR in shift right mode.

Read the word from PSR with DATA and STROBE. DATA is shifted on the rising edge of STROBE. 7 shifts are necessary.

Table 3 Example of peripheral interface

CHANGE OF CLOCK CONFIGURATION(1)		**READ CHARACTER ARRIVED IN UART RECEIVE**(2)	
	CLR REG0		CLR REG0
	CLR REG1		CLR REG1
	CLR R/W		SET R/W
	MOV R2, #8		CLR ENABLE
LOOP	RRC A		SET ENABLE
	MOV DATA C		CLR ENABLE
	CLR STROBE		SET ENABLE
	SET STROBE		MOV R2, #8
	DJNZ R2, LOOP	LOOP	MOV C, DATA
	CLR ENABLE		RRC A
	SET ENABLE		CLR STROBE
	SET DATA		SET STROBE
	RET		DJNZ R2, LOOP
			SET DATA
			RET

Notes

1. The new configuration is supposed to be in the accumulator.
2. The character will be in the accumulator.

ISO UART

The ISO UART handles all the specific requirements defined in ISO T = 0 protocol type. It is clocked with the cards clock, which gives the $f_{clk}/31$ sampling rate for start bit detection (the start bit is detected at the first LOW level on I/O) and the $f_{clk}/372$ frequency for ETU timing (in the reception mode the bit is sampled at $\frac{1}{2}$ETU). It also allows the cards clock frequency changes without interfering with the baud rate.

This hardware UART allows operating of the microcontroller at low frequency, thus lowering EM radiations and power consumption. It also frees the microcontroller of fastidious conversions and real time jobs thereby allowing the control of higher level tasks.

The following occurs in the reception mode (see Fig.6):

- Detection of the inverse or direct convention at the begin of ATR.
- Automatic convention setting, so the microcontroller only receives characters in direct convention.
- Parity checking and automatic request for character repetition in case of error (reception is possible at 12 ETU).

In the transmission mode (see Fig.7):

- Transmission according to the convention detected during ATR, consequently the microcontroller only has to send characters in direct convention. Transmission of the next character may start at 12 ETU in the event of no error or 13 ETU in case of error.
- Parity calculation and detection of repetition request from the card in the event of error.
- The bit LCT (Last Character to Transmit) allows fast reconfiguration for receiving the answer 12 ETU after the start bit of the last transmitted character.

The ISO UART status register can inform which event has caused an interrupt. (Buffer full, buffer empty, parity error detected etc.) cf Peripheral Interface.

This register is reset when the microcontroller reads the status out of it.

The ISO UART configuration register enables the microcontroller to configure the ISO UART. cf Peripheral Interface.

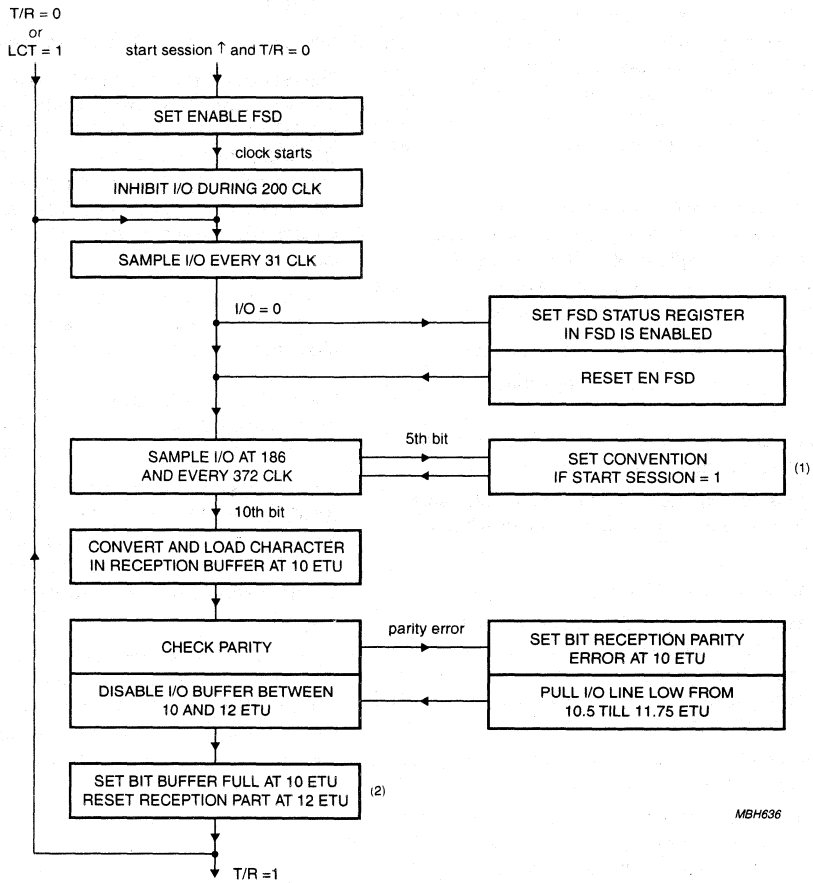
After power-on, all ISO UART registers are reset.

The ISO UART is configured in the reception mode. When the microcontroller wants to start a session, it sets the bits START SESSION and RESET ISO UART in UART CONFIGURATION and then sets START LOW. When the first start bit on I/O is detected (sampling rate $f_{clk}/31$), the UART sets the bit US2 (First Start Detect) in the status register which gives an interrupt on INT0 one CLK pulse later.

The convention is recognized on the first character of the ATR and the UART configures itself in order to exchange direct data without parity processing with the microcontroller whatever the convention of the card is. The bit START SESSION must be reset by software. At the end of every character, the UART tests the parity and resets what is necessary for receiving another character.

If no parity error is detected, the UART sets the bit US1 (BUFFER FULL) in the STATUS REGISTER which warns the microcontroller it has to read the character before the reception of the next one has been completed. The STATUS REGISTER is reset when read from the controller.

If a parity error has been detected, the UART pulls the I/O line LOW between 10.5 and 12 ETU. It also sets the bits BUFFER FULL and US3 (parity error during reception) in the STATUS REGISTER which warns the microcontroller that an error has occurred. The card is supposed to repeat the previous character.



(1) The start session is reset by software.

(2) The software may load the received character in the peripheral control at any time without any action on the ISO UART.

Fig.6 ISO UART reception flow chart.

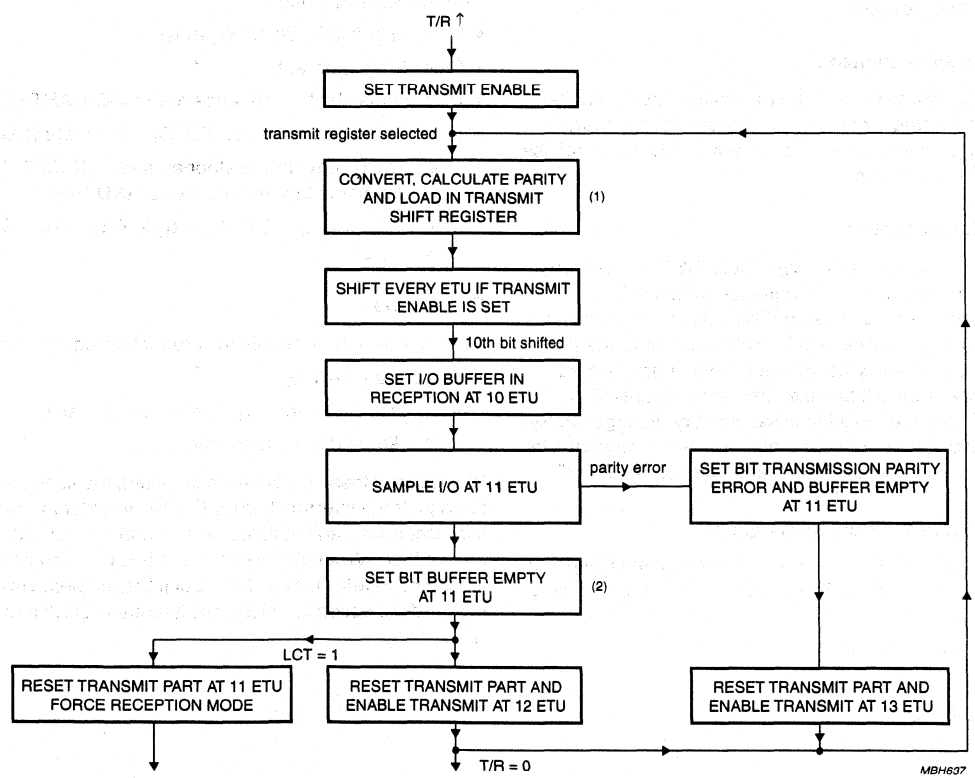
When the controller needs to transmit data to the card, it first sets the bit UC3 in the UART CONFIGURATION which configures the UART in the transmission mode. As soon as a character has been written in the UART TRANSMIT register, the UART makes the conversion, calculates the parity and starts the transmission on the rising edge of ENABLE. When the character has been transmitted, it surveys the I/O line at 11 ETU in order to know if an error has been detected by the card.

If no error has occurred, the UART sets the bit US0 (BUFFER EMPTY) in the STATUS REGISTER and waits for the next character. If the next character has been written before 12 ETU, the transmission will start at 12 ETU. If it was written after 12 ETU it will start on the rising edge of ENABLE.

If an error has occurred, it sets the bits BUFFER EMPTY and US4 (parity error during transmission) which warns the microcontroller to rewrite the previous character in the UART TRANSMIT register. If the character has been rewritten before 13 ETU, the transmission will start at 13 ETU. If it has been written after 13 ETU it will start on the rising edge of ENABLE.

When the transmission is completed, the microcontroller may set the bit LCT (Last Character to Transmit) so that the UART will force the reception mode into ready to get the reply from the card at 12 ETU. This bit must be reset before the end of the first reception. The bit T/R must be reset to enable the reception of the following characters.

When the session is completed, the microcontroller re-initializes the whole UART by resetting the bit RESET ISO UART.



(1) The transmit register may be loaded just after reading from the status register.
(2) The software must reset the last character but before completion of the first received character.

Fig.7 ISO UART transmission flow chart.

I/O buffer modes (see Fig.8)

The following are the I/O buffer modes:

1. I/O buffer disabled by ENIO.
2. I/O buffer in input, 20 kΩ pull-up resister connected between I/O and V_{CC}, I/O masked till 200 clock pulses.
3. I/O buffer in input, 20 kΩ pull-up resister connected between I/O and V_{CC}, I/O is sampled every 31 clock pulses.
4. I/O buffer in output, 20 kΩ pull-up resister connected between I/O and V_{CC}.
5. I/O buffer in output, I/O is pulled LOW by the N transistor of the buffer.
6. I/O buffer in output, I/O is strongly HIGH or LOW by the P or N transistor.

Output ports extension

In the LQFP64 version, 6 auxiliary output ports may be used for low frequency tasks (for example, keyboard scanning). These ports are push-pull output types (cf use in software document).

Activation sequence

When the card is inactive, V_{CC}, CLK, RST and I/O are LOW, with low impedance with respect to GND. The step-up converter is stopped. The I/O is configured in the reception mode with a high impedance path to the ISO UART, subsequently no spurious pulse from the card during power-up will be taken into account until I/O is enabled. When everything is satisfactory (voltage supply, card present, no hardware problems), the microcontroller may initiate an activation sequence by setting START LOW (t_0):

- The step-up converter is started (t_1)
- LIS signal is disabled by ENLI, and V_{CC} starts rising from 0 to 5 V with a controlled rise time of 0.1 V/µs typically (t_2)
- I/O buffer is enabled (t_3)
- Clock is sent to the card (t_4)
- RST buffer is enabled (t_5).

In order to allow a precise count of clock pulses during ATR, a defined time window (t_3; t_5) is opened where the clock may be sent to the card by means of RSTIN. Beyond this window, RSTIN has no more action on clock, and only monitors the cards RST contact (RST is the inverse of RSTIN).

The sequencer is clocked by $f_{INT}/64$ which leads to a time interval T of 25 µs typical. Thus $t_1 = 0$ to $1/64T$, $t_2 = t_1 + 1/2 3T$, $t_3 = t_1 + 4T$, $t_4 = t_3$ to t_5 and $t_5 = t_1 + 7T$ (see Fig.9).

Deactivation sequence (see Fig.10)

When the session is completed, the microcontroller sets START HIGH. The circuit then executes an automatic deactivation sequence:

- Card reset (RST falls LOW) at t_{10}
- Clock is stopped at t_{11}
- I/O becomes high impedance to the ISO UART (t_{12})
- V_{CC} falls to 0 V with typical 0.1 V/µs slew rate (t_{13})
- The step-up converter is stopped and CLK, RST, V_{CC} and I/O become low impedance to GND (t_{14}).
- $t_{10} < 1/64T$; $t_{11} = t_{10} + 1/2T$; $t_{12} = t_{10} + T$; $t_{13} = t_{10} + 1/2 3T$; $t_{14} = t_{10} + 5T$.

Protections

Main hardware fault conditions are monitored by the circuit

- Overcurrent on V_{CC}
- Short circuits between V_{CC} and other contacts
- Card take-off during transaction.

When one of these problems is detected, the security logic block pulls the interrupt line OFF LOW, in order to warn the microcontroller, and initiates an automatic deactivation of the contacts. When the deactivation has been completed, the OFF line returns HIGH, except if the problem was due to a card extraction in which case it remains LOW till a card is inserted.

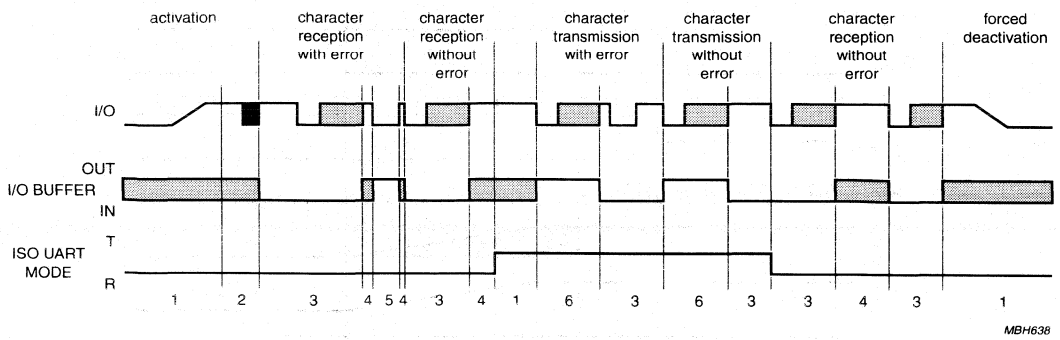


Fig.8 I/O buffer modes.

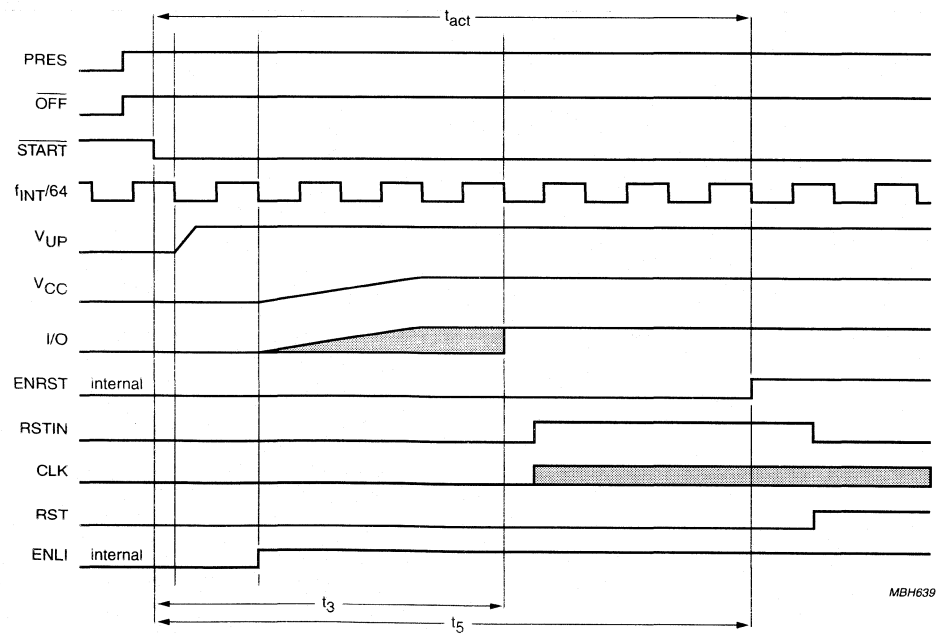


Fig.9 Activation sequence.

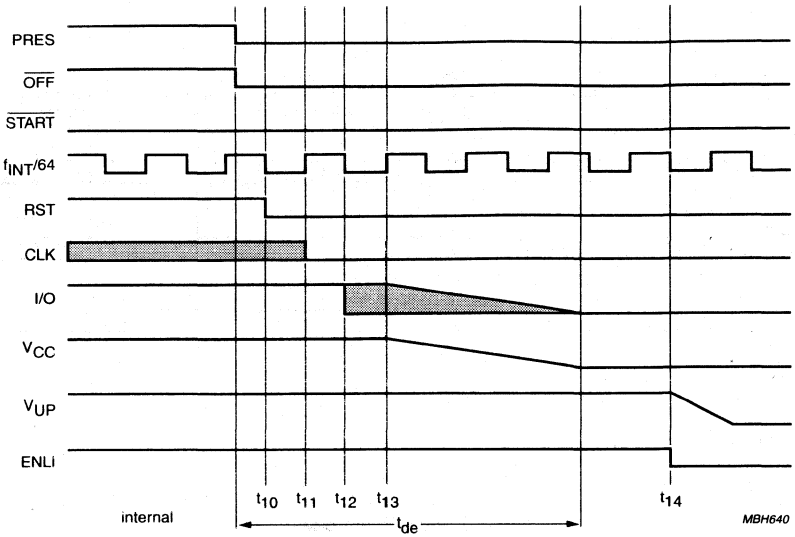


Fig.10 Emergency deactivation sequence after a card take-off.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		−0	6.5	V
V_{DDD}	digital supply voltage		−0	6.5	V
V_n	all input voltages		−0	V_{DD} + 0.5	V
I_{n1}	DC current into XTAL1, XTAL2, RX, TX, RESET, INT1, P34, P37, P00 to P03, P11 to P17, P20 to P23 and TEST1 to TEST4		−	5	mA
I_{n2}	DC current from or to AUX1, AUX2		−10	+10	mA
I_{n3}	DC current from or to S1 to S5		−30	+30	mA
I_{n4}	DC current into DELAY		−5	+10	mA
I_{n5}	DC current from or to PRES		−5	+5	mA
I_{n6}	DC current from and to K0 to K5		−5	+5	mA
I_{n7}	DC current from or into ALARM (according to option choice)		−5	+5	mA
P_{tot}	continuous total power dissipation	T_{amb} = −20 to +85°C	−	500	mW
T_{stg}	IC storage temperature		−55	+150	°C
V_{es}	electrostatic discharge	on pins I/O, V_{CC}, RST, CLK and PRES	−6	+6	kV
		on other pins	−2	+2	kV
T_j	Operating Junction Temp.	−	−	125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air		
	LQFP64	70	K/W
	QFP44	60	K/W

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; for general purpose I/O ports see 80CL51 data sheet; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	Option dependant	2.5	–	6.0	V
$I_{DD(pd)}$	supply current power-down mode	V_{DD} = 5 V; card inactive V_{DD} = 3V; " "	–	90	–	µA
$I_{DD(sm)}$	supply current sleep mode	card powered, but with clock stopped	–	500	–	µA
$I_{DD(om)}$	supply current operating mode	unloaded; f_{xtal} = 13 MHz; f_{clk} = 6.5 MHz; f_{card} = 3.25 MHz	–	5.5	–	mA
		V_{DD} = 3 V; f_{xtal} = 13 MHz; f_{clk} = 3.25 MHz; f_{card} = 3.25 MHz	–	3	–	mA
V_{th1}	threshold voltage on V_{DD} (falling)	supervisor option	2	–	2.3	V
			2.45	–	3	V
			3.8	–	4.5	V
V_{hys1}	hysteresis on V_{th1}		40	–	350	mV
V_{th2}	threshold voltage on DELAY		–	1.38	–	V
V_{DEL}	voltage on pin DELAY		4.6	–	V_{DD}	V
I_{DEL}	output current at DELAY	pin grounded (charge)	–1.5	–1	–0.4	µA
		V_{DEL} = V_{DD} (discharge)	4	6.8	10	mA
t_W	ALARM pulse width	C_{DEL} = 10 nF	–	10	–	ms
ALARM (open drain active HIGH or LOW output)						
I_{OH}	HIGH level output current	active LOW option; V_{OH} = 5 V	–	–	10	µA
V_{OL}	LOW level output voltage	active LOW option; I_{OL} = 2 mA	–	–	0.4	V
I_{OL}	LOW level output current	active HIGH option, V_{OL} = 0 V	–	–	–10	µA
V_{OH}	HIGH level output voltage	active HIGH option, I_{OH} = –2 mA	V_{DD} – 1	–	–	V
Crystal oscillator (note 1)						
f_{xtal}	crystal frequency		2	–	16	MHz
f_{EXT}	external frequency applied on XTAL1		0	–	16	MHz
Step-up converter						
f_{INT}	oscillation frequency		2	–	3	MHz
V_{UP}	voltage on S5		–	6.5	–	V
Low impedance supply (LIS)						
V_{LIS}	voltage on LIS		0	–	V_{DD}	V
I_{LIS}	current at LIS		–	–	7	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset output to the card (RST)						
$V_{inactive}$	output voltage	when inactive	−0.3	−	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	−0.3	−	0.4	V
$I_{inactive}$	current from RST when inactive and pin grounded		−	−	−1	mA
V_{OL}	LOW level output voltage	I_{OL} = 200 µA	−0.25	−	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} <−200 µA	4	−	V_{CC} + 0.3	V
t_r	rise time	C_L = 30 pF	−	−	1	µs
t_f	fall time	C_L = 30 pF	−	−	1	µs
Clock output to the card (CLK)						
$V_{inactive}$	output voltage	when inactive	−0.3	−	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	−0.3	−	0.4	V
$I_{inactive}$	current from CLK when inactive and pin grounded		−	−	−1	mA
V_{OL}	LOW level output voltage	I_{OL} = 200 µA	−0.25	−	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} <−200 µA	V_{CC}−0.5	−	V_{CC}+0.25	V
t_r	rise time	C_L = 30 pF	−	−	15	ns
t_f	fall time	C_L = 30 pF	−	−	15	ns
f_{clk}	clock frequency	1 MHz Idle configuration	1	−	1.5	MHz
		low operating speed	−	−	2	MHz
		middle operating speed	−	−	4	MHz
		high operating speed	−	−	8	MHz
δ	duty cycle	C_L = 30 pF	45	−	55	%
Card supply voltage (V_{CC})						
$V_{inactive}$	output voltage	when inactive	−0.3	−	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	−0.3	−	0.4	V
$I_{inactive}$	current from VCC when inactive and pin grounded		−	−	−1	mA
V_{cc}	output voltage in active mode with 100 nF capacitor; static load (up to 20 mA) dynamic current of 40 nA	I_{max} = 200 mA, f_{max} = 5 MHz, and duration <400 ns	− 4.75 4.5	−	− 5.25 5.5	V
I_{CC}	output current	V_{CC} = 5V	−	−	−20	mA
		V_{CC} shorted to GND	−	−	−40	mA
SR	slew rate	up or down (max capacitance is 150 nF)	0.04	0.1	0.16	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data line (I/O)						
$V_{inactive}$	output voltage	when inactive	−0.3	–	0.4	V
		when LIS is used; $I_{inactive}$ = 1 mA	−0.3	–	0.4	V
$I_{inactive}$	current from I/O when inactive and pin grounded		–	–	−1	mA
V_{OL}	LOW level output voltage (I/O configured as an output)	I_{OL} = 1 mA	−0.25	–	0.3	V
V_{OH}	HIGH level output voltage (I/O configured as an output)	I_{OH} <−100 μA	V_{CC}+0.8	–	V_{CC}+0.25	V
V_{IL}	input voltage LOW (I/O configured as an input)	I_{IL} = 1 mA	0	–	0.5	V
V_{IH}	input voltage HIGH (I/O configured as an input)	I_{IL} = 100 μA	V_{CC}+0.6	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	1	μs
t_f	fall time	C_L = 30 pF	–	–	1	μs
R_{pu}	pull-up resistor connected to V_{CC} when I/O is input	see Table 4 for options	–	–	–	
Protections						
$I_{CC(sd)}$	shutdown current at V_{CC}		–	−30	–	mA
Timing						
t_{act}	activation sequence duration		–	–	225	μs
t_{de}	deactivation sequence duration		–	–	150	μs
$t_{3(start)}$	start of the window for sending clock to the card		–	–	130	μs
$t_{5(end)}$	end of the window for sending clock to the card		140	–	–	μs
Auxiliary outputs (AUX1, AUX2)						
V_{OL}	LOW level output voltage	I_{OL} = 5 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −5 mA	V_{DD} − 1	–	–	V
Output ports from extension (K0 to Kn)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −2 mA	V_{DD} − 1	–	–	V
Card presence input (PRES)						
V_{IL}	LOW level input voltage	I_{IL} = −1 mA	–	–	0.6	V
V_{IH}	HIGH level input voltage	I_{IH} = 100 μA	0.7V_{DD}	–	–	V
I_{IH}	HIGH level input current	V_{IH}=+5V	0.2	–	3	μA

Note

1. The crystal oscillator is the same as OPTION 3 of the 80CL51.

APPLICATION INFORMATION

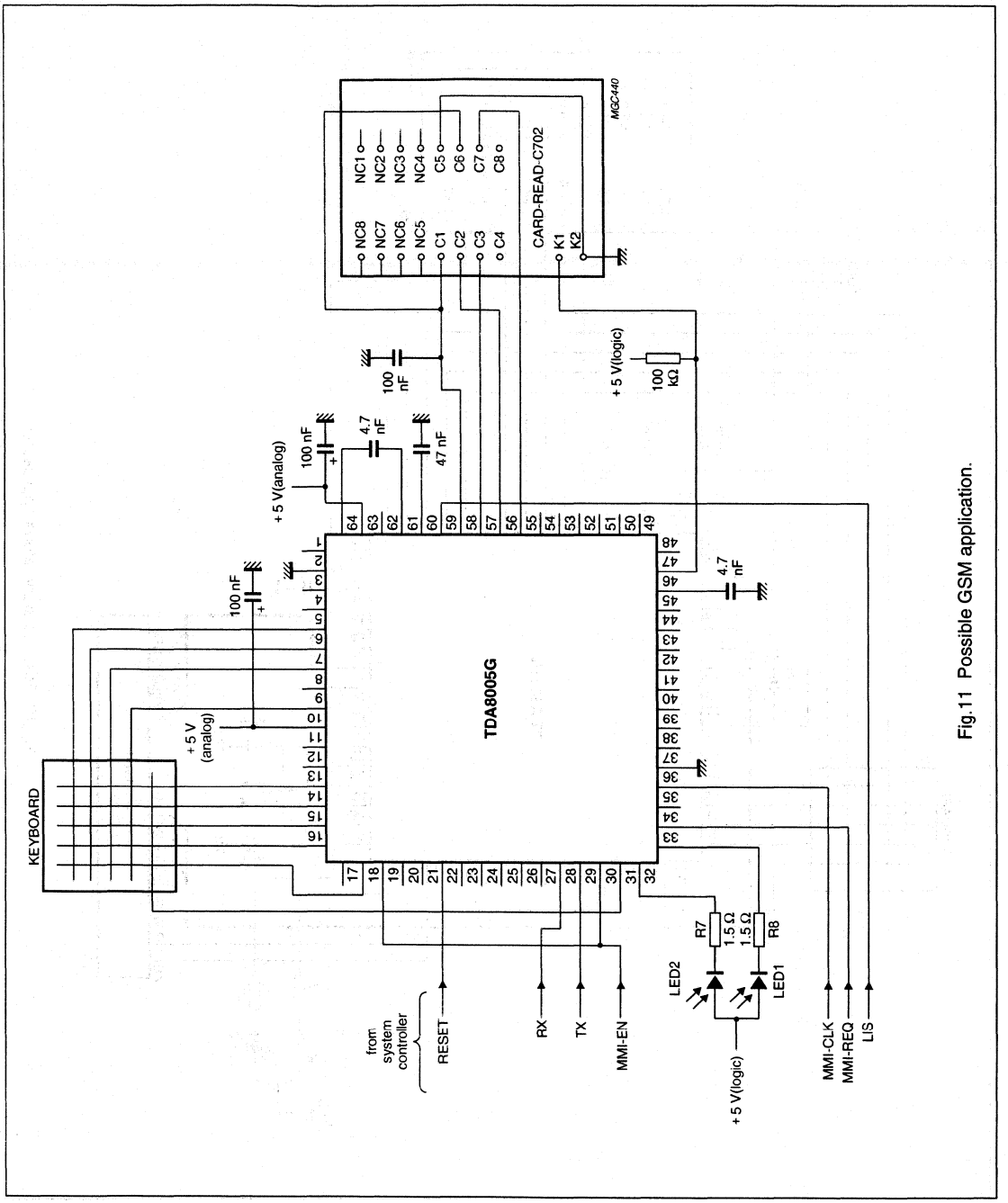


Fig.11 Possible GSM application.

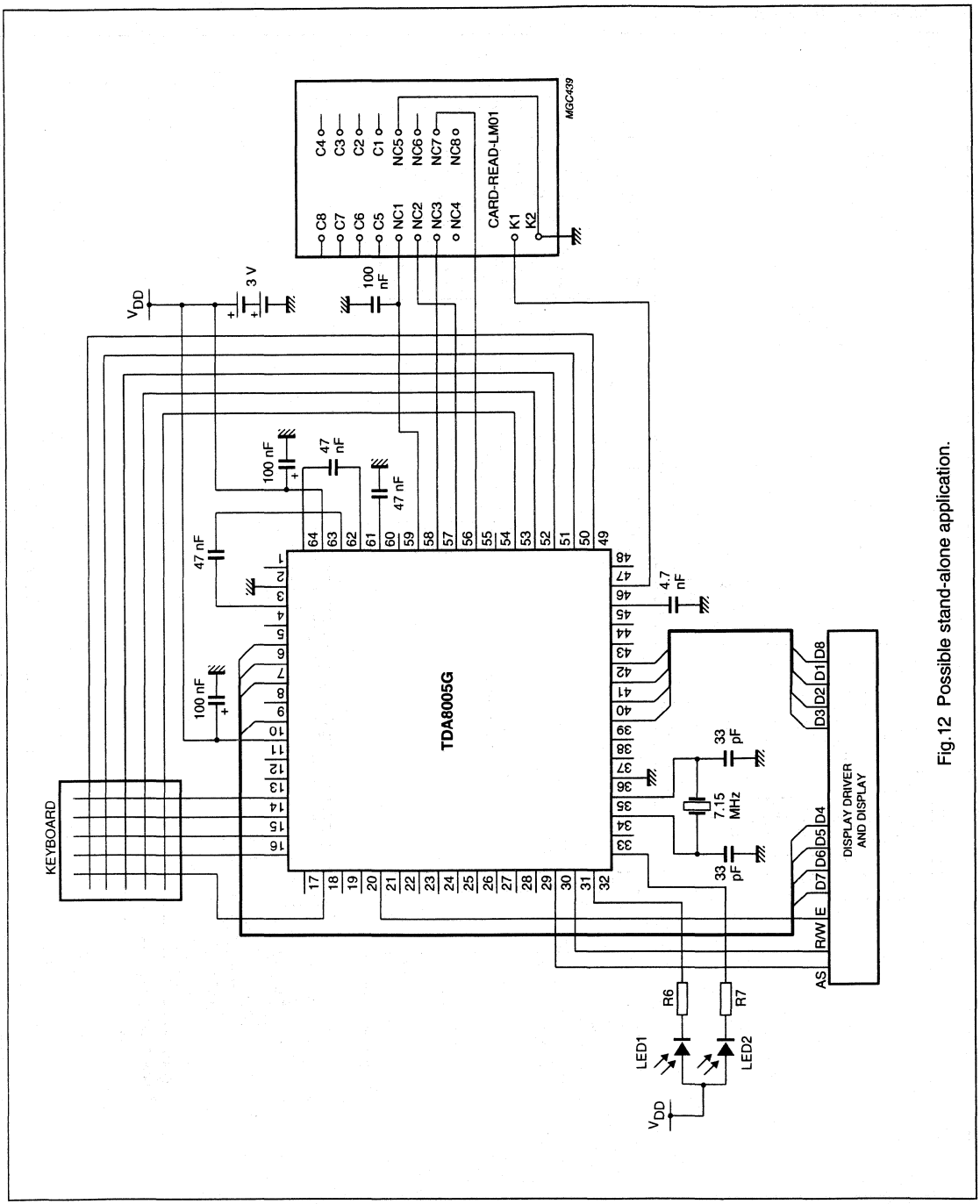


Fig.12 Possible stand-alone application.

Table 4 TDA8005 option choice form

FUNCTION	DESCRIPTION	OPTION
Ports		
P00		
P01		
P02		
P03		
P04	RSTIN (fixed)	3 S
P05	START (fixed)	3 S
P06	STR (fixed)	3 S
P07	EN (fixed)	3 S
P10	OFF (fixed)	2 S
P11		
P12		
P13		
P14		
P15		
P16		
P17		
P20		
P21		
P22		
P23		
P24	DATA (fixed)	1 S
P25	R/W (fixed)	3 S
P26	REG1 (fixed)	3 S
P27	REG0 (fixed)	3 S
P30		
P31		
P32	INT (fixed)	1 S
P33		
P34		
P35	AUXI (fixed)	3 S
P36	AUX2 (fixed)	3 S
P37		

FUNCTION	DESCRIPTION	OPTION
Analog options		
Step-up	doubler (updo) or tripler (uptri)	
Supervisor	2.3 (supervb, 3 (supervtr) or 4.5 (superVCI)	
I/O	low impedance (UARTI) or high impedance (UARTZ)	
I/O pull-up	10, 20 or 30 kΩ	
R_CLK	0, 50, 100, 150 or 200 Ω	
R_RST	0, 50, 80, 130 or 180 Ω	
ALARM	active HIGH (alarmbufp) or active LOW (alarmbufn)	
PRES	active HIGH (prestopp) or active LOW (prestopn)	

Hands free IC TEA1094; TEA1094A

FEATURES

- Low power consumption
- Power-down function (TEA1094A only)
- Microphone channel with:
  - externally adjustable gain
  - microphone mute function.
- Loudspeaker channel with:
  - externally adjustable gain
  - dynamic limiter to prevent distortion
  - rail-to-rail output stage for single-ended load drive
  - logarithmic volume control via linear potentiometer
  - loudspeaker mute function.
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:
    - externally adjustable sensitivity
    - externally adjustable signal envelope time constant
    - externally adjustable noise envelope time constant
  - decision logic with:
    - externally adjustable switch-over timing
    - externally adjustable idle mode timing
    - externally adjustable dial tone detector in receive channel
  - voice switch control with:
    - adjustable switching range
    - constant sum of gain during switching
    - constant sum of gain at different volume settings.

APPLICATIONS

- Mains, battery or line-powered telephone sets with hands-free/listening-in functions
- Cordless telephones
- Answering machines
- Fax machines.

GENERAL DESCRIPTION

The TEA1094 and TEA1094A are bipolar circuits intended for use in mains, battery or line-powered telephone sets, cordless telephones, answering machines and Fax machines. In conjunction with a member of the TEA106X, TEA111X families of transmission circuits, the devices offer a hands-free function. They incorporate a microphone amplifier, a loudspeaker amplifier and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1094	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1094A	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
TEA1094T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TEA1094AT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TEA1094AM	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

QUICK REFERENCE DATA

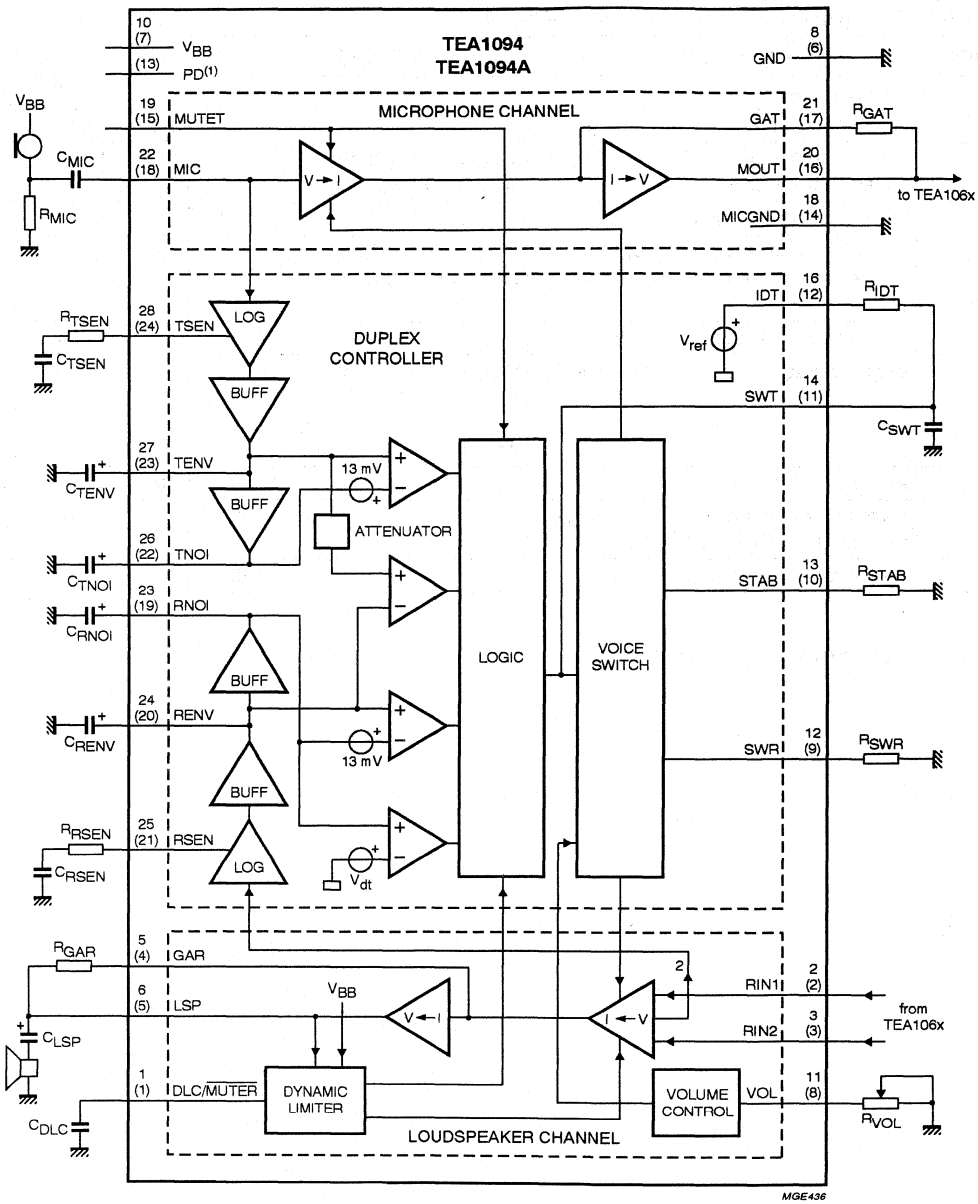
V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTET = LOW; PD = LOW (TEA1094A only); R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BB}	supply voltage		3.3	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	3.1	4.4	mA
G_{vtx}	voltage gain from pin MIC to pin MOUT in transmit mode	V_{MIC} = 1 mV (RMS); R_{GAT} = 30.1 kΩ	13	15.5	18	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−15.5	–	+15.5	dB
G_{vrx}	voltage gain in receive mode; the difference between RIN1 and RIN2 to LSP	V_{RIN} = 20 mV (RMS); R_{GAR} = 66.5 kΩ; R_L = 50 Ω	16	18.5	21	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−18.5	–	+14.5	dB
$V_{O(p-p)}$	output voltage (peak-to-peak value)	V_{RIN} = 150 mV (RMS); R_{GAR} = 374 kΩ; R_L = 33 Ω; V_{BB} = 9.0 V; note 1	–	7.5	–	V
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to R_{SWR} = 365 kΩ		−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

Note

1. Corresponds to 200 mW output power.

BLOCK DIAGRAM



The pin numbers given in parenthesis are for the TEA1094A.

(1) TEA1094A only.

Fig.1 Block diagram.

PINNING

SYMBOL	PINS		DESCRIPTION
	TEA1094	TEA1094A	
DLC/$\overline{\text{MUTER}}$	1	1	dynamic limiter timing adjustment; receiver channel mute input
RIN1	2	2	receiver amplifier input 1
RIN2	3	3	receiver amplifier input 2
n.c.	4	–	not connected
GAR	5	4	receiver gain adjustment
LSP	6	5	loudspeaker amplifier output
n.c.	7	–	not connected
GND	8	6	ground reference
n.c.	9	–	not connected
V_{BB}	10	7	supply voltage
VOL	11	8	receiver volume adjustment
SWR	12	9	switching range adjustment
STAB	13	10	reference current adjustment
SWT	14	11	switch-over timing adjustment
n.c.	15	–	not connected
IDT	16	12	idle mode timing adjustment
PD	–	13	power-down input
n.c.	17	–	not connected
MICGND	18	14	ground reference for the microphone amplifier
MUTET	19	15	transmit channel mute input
MOUT	20	16	microphone amplifier output
GAT	21	17	microphone gain adjustment
MIC	22	18	microphone input
RNOI	23	19	receive noise envelope timing adjustment
RENV	24	20	receive signal envelope timing adjustment
RSEN	25	21	receive signal envelope sensitivity adjustment
TNOI	26	22	transmit noise envelope timing adjustment
TENV	27	23	transmit signal envelope timing adjustment
TSEN	28	24	transmit signal envelope sensitivity adjustment

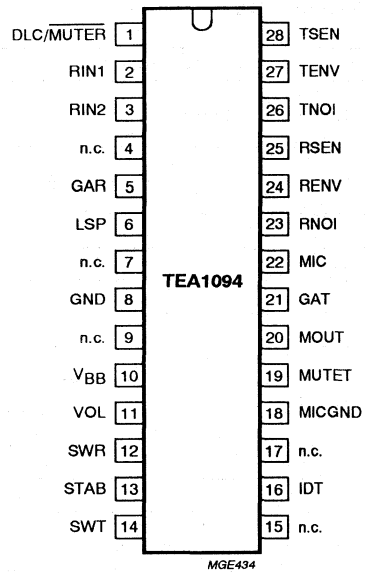


Fig.2 Pin configuration (TEA1094).

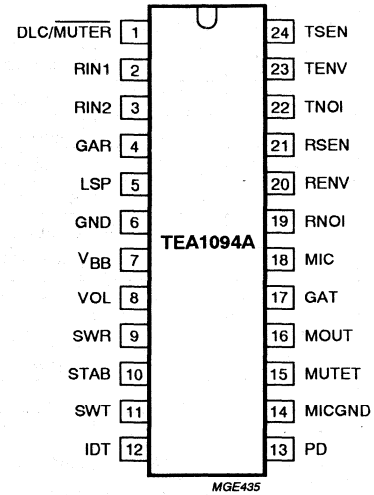


Fig.3 Pin configuration (TEA1094A).

FUNCTIONAL DESCRIPTION

General

The values given in the functional description are typical values unless otherwise specified.

A principle diagram of the TEA106X is shown on the left side of Fig.4. The TEA106X is a transmission circuit of the TEA1060 family intended for hand-set operation.
It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone and a hybrid.
For more details on the TEA1060 family, please refer to *"data Handbook IC03"*. The right side of Fig.4 shows a principle diagram of the TEA1094 and TEA1094A, hands-free add-on circuits with a microphone amplifier, a loudspeaker amplifier and a duplex controller.

As can be seen from Fig.4, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case.
The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1094 and TEA1094A detects which channel has the 'largest' signal and then controls the gain of the microphone amplifier and the loudspeaker amplifier so that the sum of the gains remains constant.
As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode).

   The gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.

2. Receive mode (Rx mode).

   The gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.

3. Idle mode.

   The gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

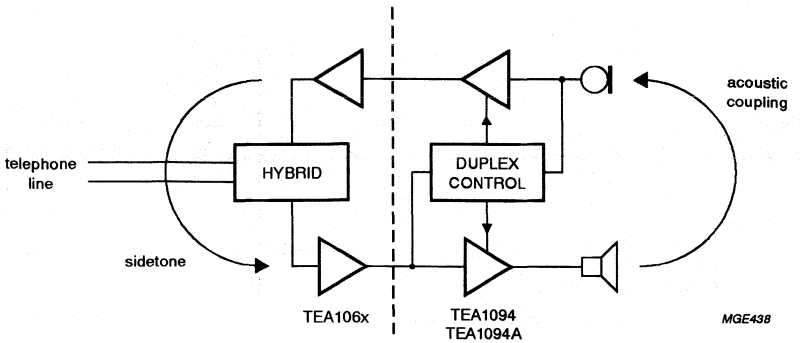


Fig.4 Hands-free telephone set principles.

Supply: pins V_{BB}, GND and PD

The TEA1094 and TEA1094A must be supplied with an external stabilized voltage source between pins V_{BB} and GND. In the idle mode, without any signal, the internal supply current is 3.1 mA at V_{BB} = 5 V.

To reduce the current consumption during pulse dialling or register recall (flash), the TEA1094A is provided with a power-down (PD) input. When the voltage on PD is HIGH the current consumption from V_{BB} is 180 μA.

Microphone channel: pins MIC, GAT, MOUT, MICGND and MUTET (see Fig.5)

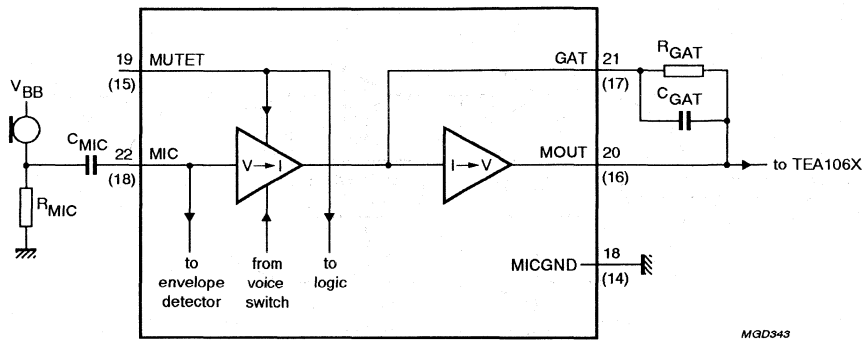
The TEA1094 and TEA1094A have an asymmetrical microphone input MIC with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1094 and TEA1094A. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum.

Switch-over from one mode to the other is smooth and click-free. The output capability at pin MOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the microphone amplifier (from pins MIC to MOUT) can be adjusted from 0 dB up to 31 dB to suit specific application requirements. The gain is proportional to the value of R_{GAT} and equals 15.5 dB with R_{GAT} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GAT} to ensure stability of the microphone amplifier. Together with R_{GAT}, it also provides a first-order low-pass filter.

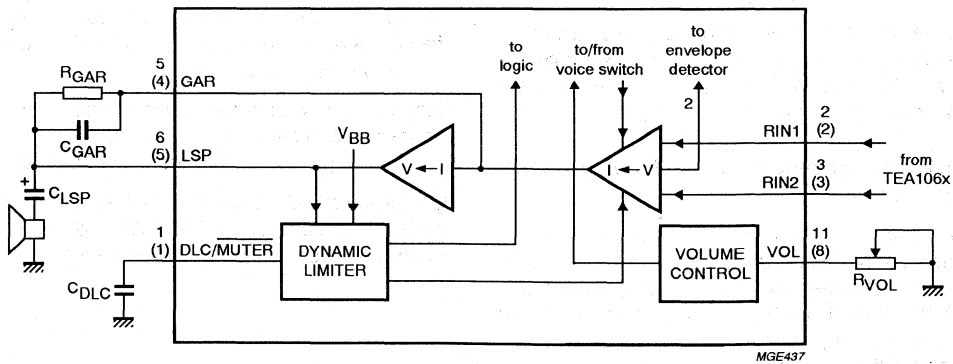
By applying a HIGH level on pin MUTET, the microphone amplifier is muted and the TEA1094 and TEA1094A are automatically forced into the receive mode.



The pin numbers given in parenthesis refer to the TEA1094A.

Fig.5 Microphone channel.

Loudspeaker channel



The pin numbers given in parenthesis refer to the TEA1094A.

Fig.6 Loudspeaker channel.

LOUDSPEAKER AMPLIFIER: PINS RIN1, RIN2, GAR AND LSP

The TEA1094 and TEA1094A have symmetrical inputs for the loudspeaker amplifier with an input resistance of 40 kΩ between RIN1 and RIN2 (2 × 20 kΩ). The input stage can accommodate signals up to 390 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The gain of the input stage varies according to the mode of the TEA1094 and TEA1094A. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker connected as a single-ended load (between LSP and GND).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 0 dB up to 33 dB to suit specific application requirements. The gain from RIN1 and RIN2 to LSP is proportional to the value of R_{GAR} and equals 18.5 dB with R_{GAR} = 66.5 kΩ. A capacitor connected in parallel with R_{GAR} can be used to provide a first-order low-pass filter.

VOLUME CONTROL: PIN VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

DYNAMIC LIMITER: PIN DLC/$\overline{\text{MUTER}}$

The dynamic limiter of the TEA1094 and TEA1094A prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{BB} falls below 2.9 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{RIN} is below 390 mV (RMS)].

When the supply voltage drops below an internal threshold voltage of 2.9 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.9 V, the gain of the loudspeaker amplifier is increased again.

By forcing a level lower than 0.2 V on pin DLC/$\overline{\text{MUTER}}$, the loudspeaker amplifier is muted and the TEA1094 (TEA1094A) is automatically forced into the transmit mode.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

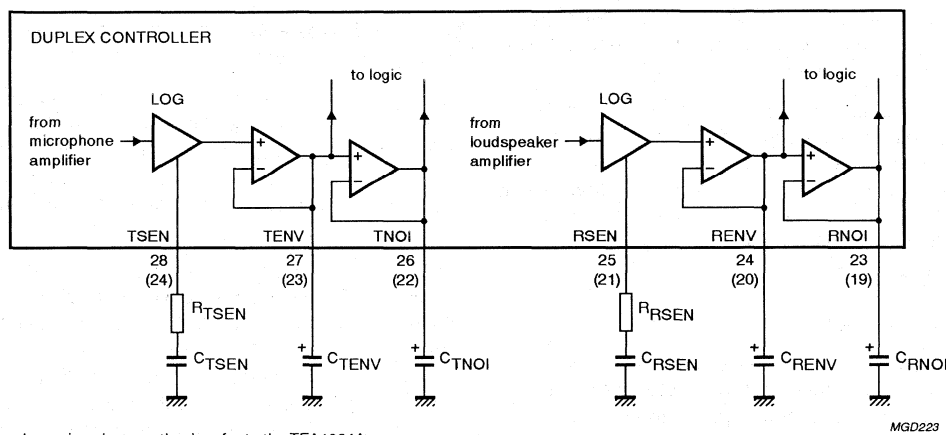
The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelope detectors are shown in Fig.7.

For the transmit channel, the input signal at MIC is 40 dB amplified to TSEN. For the receive channel, the differential signal between RIN1 and RIN2 is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first-order high-pass filter. In the basic application, see Fig.13, it is assumed that V_{MIC} = 1 mV (RMS) and V_{RIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is sufficient to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is sufficient for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

To determine the noise level, the signals on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.13 the value of both capacitors is 4.7 μF. At room temperature, the 1 μA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms.

This is small enough to track background noise and not to be influenced by speech bursts. The 120 μA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.8.



The pin numbers given in parenthesis refer to the TEA1094A.

Fig.7 Signal and noise envelope detectors.

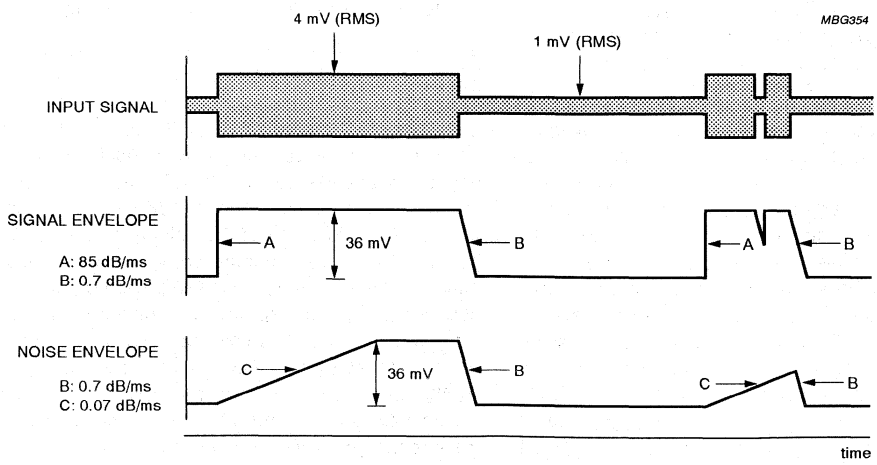
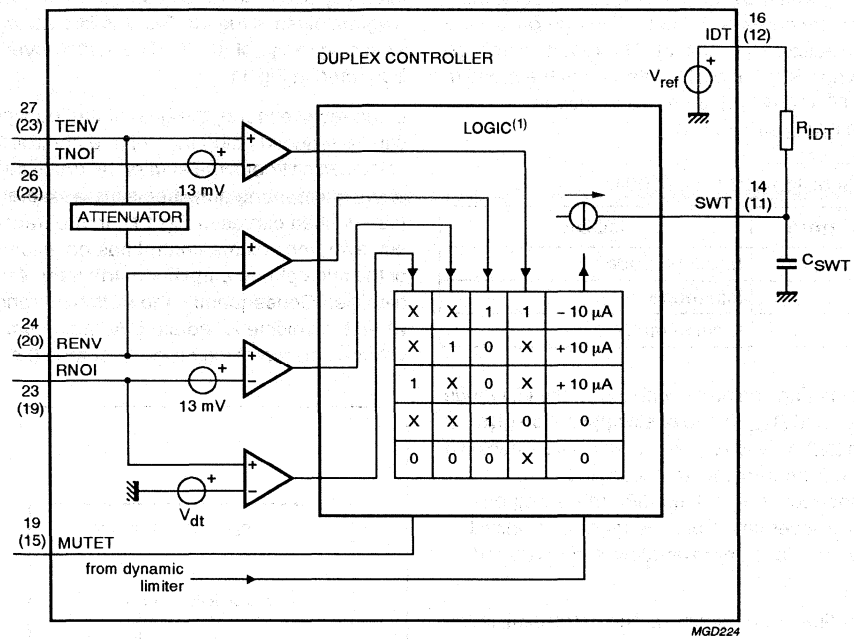


Fig.8 Signal and noise envelope waveforms.

DECISION LOGIC: PINS IDT AND SWT



The pin numbers given in parenthesis refer to the TEA1094A.

(1) When MUTET = HIGH, +10 µA is forced.
When DLC/MUTER < 0.2 V, −10 µA is forced.

Fig.9 Decision logic.

The TEA1094 and TEA1094A select their modes of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV} - V_{NOI} = 13$ mV. This so called speech/noise threshold is implemented in both channels.

The signal on MIC contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech.

As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1094 (TEA1094A) to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard applications, does not consider input signals between RIN1 and RIN2 as noise when they have a level greater than 127 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.9, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1094 (TEA1094A) and can vary between −400 and +400 mV (see Table 1).

Table 1 Modes of TEA1094; TEA1094A

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.13, C_{SWT} is 220 nF and R_{IDT} is 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time, from receive mode or transmit mode to idle mode, is equal to $4 \times R_{IDT}C_{SWT}$ and is approximately 2 seconds (idle mode time).

The inputs MUTET and DLC/$\overline{\text{MUTER}}$ overrule the decision logic. When MUTET goes HIGH, the capacitor C_{SWT} is charged with 10 μA thus resulting in the receive mode. When the voltage on pin DLC/$\overline{\text{MUTER}}$ goes lower than 0.2 V, the capacitor C_{SWT} is discharged with 10 μA thus resulting in the transmit mode.

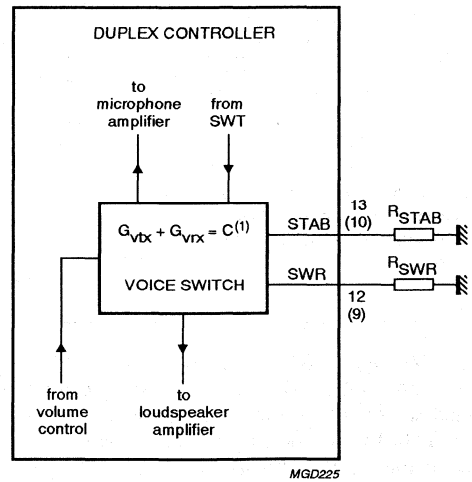
VOICE-SWITCH: PINS STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.10. With the voltage on SWT, the TEA1094 (TEA1094A) voice-switch regulates the gains of the transmit and the receive channel so that the sum of both is kept constant.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gains are halfway.

The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.13, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.11.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.11). In the transmit mode, however, the volume control has no influence on the gain of the microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.



The pin numbers given in parenthesis refer to the TEA1094A.

(1) C = constant.

Fig.10 Voice switch.

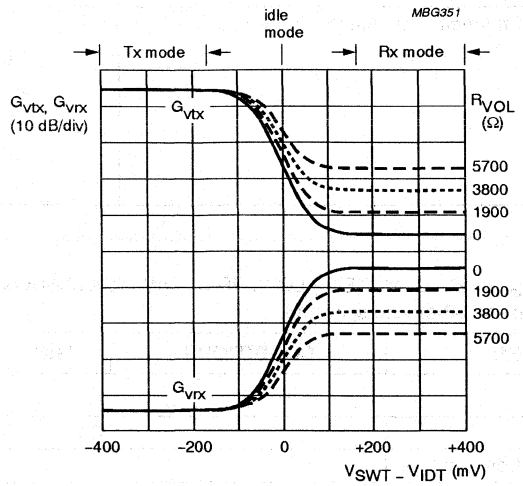


Fig.11 Switch-over behaviour.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins V_{BB}, RIN1 and RIN2		V_{GND} – 0.4	V_{BB} + 0.4	V
$V_{RIN(max)}$	maximum voltage on pins RIN1 and RIN2		V_{GND} – 1.2	V_{BB} + 0.4	V
$V_{BB(max)}$	maximum voltage on pin V_{BB}		V_{GND} – 0.4	12.0	V
P_{tot}	total power dissipation	T_{amb} = 75 °C			
	TEA1094		–	1000	mW
	TEA1094A		–	910	mW
	TEA1094T		–	625	mW
	TEA1094AT		–	590	mW
	TEA1094AM		–	438	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1094	45	K/W
	TEA1094A	50	K/W
	TEA1094T	70	K/W
	TEA1094AT	75	K/W
	TEA1094AM	104	K/W

CHARACTERISTICS

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTET = LOW; PD = LOW (TEA1094A only); R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_{BB}, GND and PD)						
V_{BB}	supply voltage		3.3	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	3.1	4.4	mA
POWER-DOWN INPUT PD (TEA1094A ONLY)						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{PD}	input current	PD = HIGH	–	2.5	5	μA
$I_{BB(PD)}$	current consumption from pin V_{BB} in power-down condition	PD = HIGH	–	180	240	μA
Microphone channel (MIC, GAT, MOUT, MUTET and MICGND)						
MICROPHONE AMPLIFIER						
$\|Z_i\|$	input impedance between pins MIC and MICGND		17	20	23	kΩ
G_{vtx}	voltage gain from pin MIC to MOUT in transmit mode	V_{MIC} = 1 mV (RMS)	13	15.5	18	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		–15.5	–	+15.5	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{MIC} = 1 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{MIC} = 1 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
V_{notx}	noise output voltage at pin MOUT	pin MIC connected to MICGND through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	–100	–	dBmp

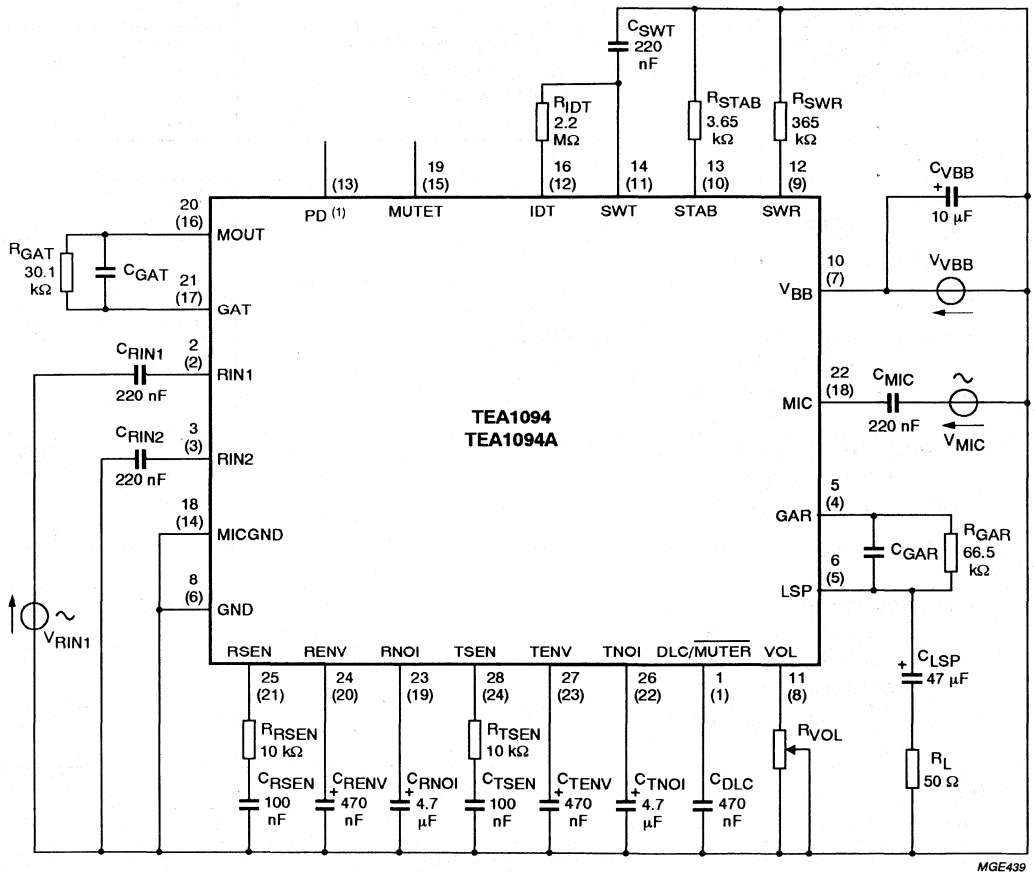
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSMIT MUTE INPUT MUTET						
V_{IL}	LOW level input voltage		V_{GND} − 0.4	−	0.3	V
V_{IH}	HIGH level input voltage		1.5	−	V_{BB} + 0.4	V
I_{MUTET}	input current	MUTET = HIGH	−	2.5	5	μA
ΔG_{vtxm}	voltage gain reduction with MUTET active	MUTET = HIGH	−	80	−	dB
Loudspeaker channel (RIN1, RIN2, GAR, LSP and DLC/$\overline{\text{MUTER}}$)						
LOUDSPEAKER AMPLIFIER						
$\lvert Z_i \rvert$	input impedance	between pins RIN1 or RIN2 and GND	17	20	23	kΩ
		between pins RIN1 and RIN2	34	40	46	kΩ
G_{vrx}	voltage gain in receive mode; between RIN1 and RIN2 to LSP	V_{RIN} = 20 mV (RMS)	16	18.5	21	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−18.5	−	+14.5	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RIN} = 20 mV (RMS); T_{amb} = −25 to +75 °C	−	±0.3	−	dB
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RIN} = 20 mV (RMS); f = 300 to 3400 Hz	−	±0.3	−	dB
$V_{RIN(rms)}$	maximum input voltage between RIN1 and RIN2 (RMS value)	R_{GAR} = 11.8 kΩ; for 2% THD in input stage	−	390	−	mV
$V_{norx(rms)}$	noise output voltage at pin LSP (RMS value)	inputs RIN1 and RIN2 short-circuited through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	−	80	−	μV
CMRR	common mode rejection ratio		−	50	−	dB
ΔG_{vrxv}	voltage gain variation related to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	−	3	−	dB
OUTPUT CAPABILITY						
$V_{OSE(p-p)}$	output voltage (peak-to-peak value)	V_{RIN} = 300 mV (RMS); note 1	3.5	4.5	−	V
		V_{RIN} = 150 mV (RMS); R_{GAR} = 374 kΩ; R_L = 33 Ω; V_{BB} = 9.0 V; note 2	−	7.5	−	V
I_{OM}	maximum output current at LSP (peak value)		150	500	−	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DYNAMIC LIMITER						
t_{att}	attack time when V_{RIN} jumps from 20 mV to 20 mV + 10 dB	R_{GAR} = 374 kΩ	–	–	5	ms
t_{rel}	release time when V_{RIN} jumps from 20 mV + 10 dB to 20 mV	R_{GAR} = 374 kΩ	–	250	–	ms
THD	total harmonic distortion at V_{RIN} = 20 mV + 10 dB	R_{GAR} = 374 kΩ; $t > t_{att}$	–	0.9	5	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.9	–	V
t_{att}	attack time when V_{BB} jumps below $V_{BB(th)}$		–	1	–	ms
MUTE RECEIVE						
$V_{DLC(th)}$	threshold voltage required on pin DLC/$\overline{\text{MUTER}}$ to obtain mute receive condition		V_{GND} – 0.4	–	0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC/$\overline{\text{MUTER}}$ in mute receive condition	V_{DLC} = 0.2 V	–	100	–	μA
ΔG_{vrxm}	voltage gain reduction in mute receive condition	V_{DLC} < 0.2 V	–	80	–	dB
Envelope and noise detectors (TSEN, TENV, RSEN, RENV, RNOI and TNOI)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from MIC to TSEN		37.5	40	42.5	dB
$G_{v(RSEN)}$	voltage gain between RIN1 and RIN2 to RSEN		–2.5	0	+2.5	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\Delta V_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 μA	–	18	–	mV
$\Delta V_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 μA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	μA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	μA
ΔV_{ENV}	voltage difference between pins RENV and TENV	when 10 μA is sourced from both RSEN and TSEN; envelope detectors tracking; note 3	–	±3	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pins TNOI or RNOI		0.75	1	1.25	μA
$I_{sink(NOI)}$	maximum current sunk by pins TNOI or RNOI		–	120	–	μA
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	when 5 μA is sourced from both RSEN and TSEN; noise detectors tracking; note 3	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pins RIN1 and RIN2 (RMS value)		–	127	–	mV
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	$V_{RIN} < V_{RINDT}$; note 4	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 4	–	13	–	mV
SWITCH-OVER						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	μA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	μA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	μA
Voice switch (STAB and SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to 365 kΩ	−40	–	+12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to 50 mW output power.
2. Corresponds to 200 mW output power.
3. Corresponds to ±1 dB tracking.
4. Corresponds to 4.3 dB noise/speech recognition level.



The pin numbers given in parenthesis refer to the TEA1094A.

(1) TEA1094A only.

Fig.12 Test circuit.

APPLICATION INFORMATION

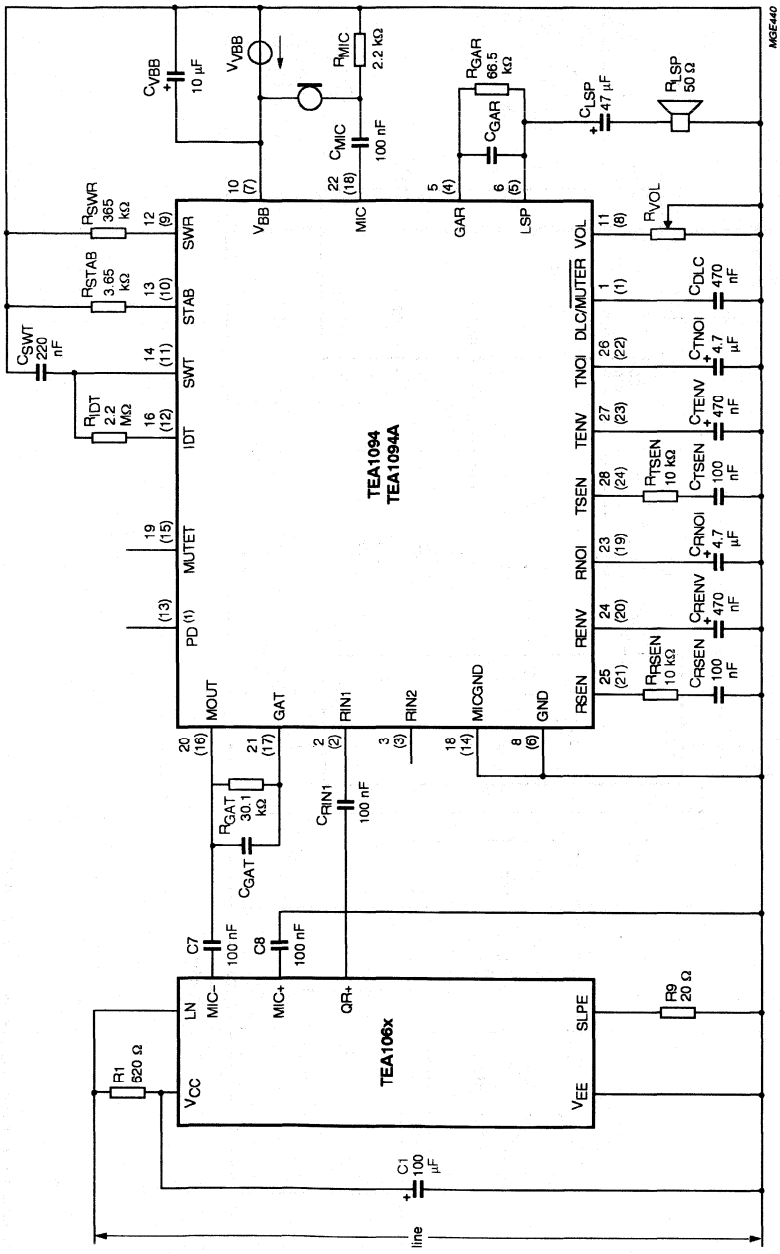


Fig.13 Basic application diagram.

The pin numbers given in parenthesis refer to the TEA1094A.

(1) TEA1094A only.

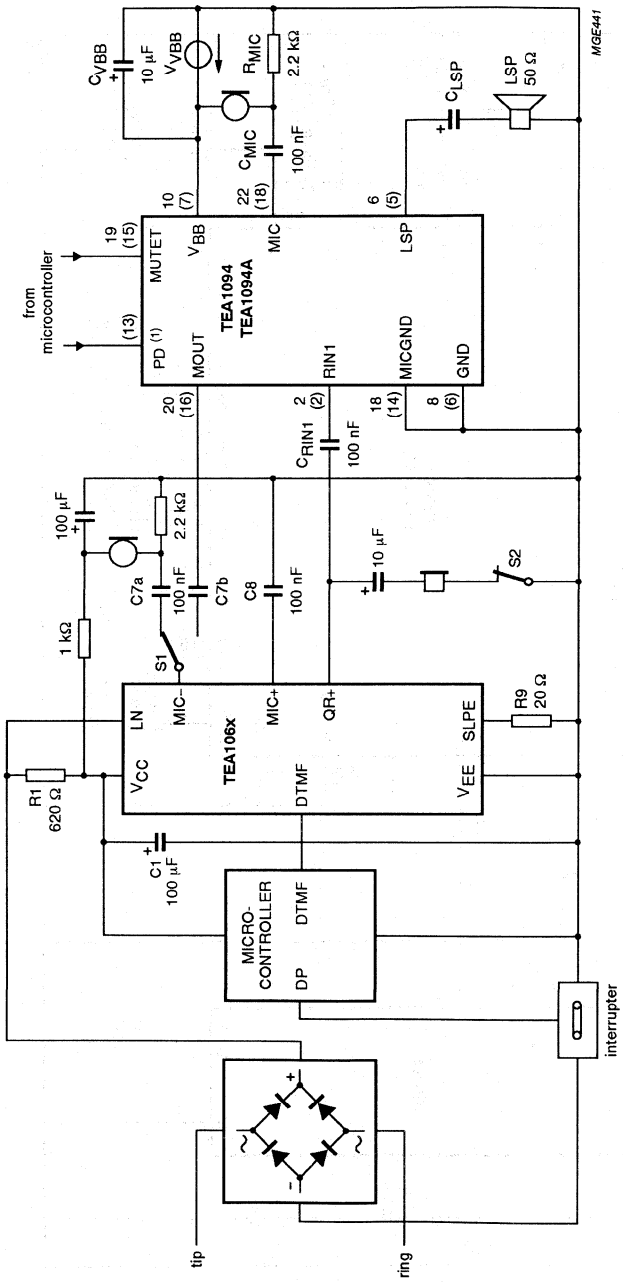


Fig.14 Application example.

The pin numbers given in parenthesis refer to the TEA1094A.

(1) TEA1094A only.

Voice switched speakerphone IC TEA1095

FEATURES

- External power supply with power-down function
- Transmit channel with:
  - externally adjustable gain
  - transmit mute function
- Receive channel with:
  - externally adjustable gain
  - logarithmic volume control via a linear potentiometer
  - receive mute function
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:

    externally adjustable sensitivity

    externally adjustable signal envelope time constant

    externally adjustable noise envelope time constant
  - decision logic with:

    externally adjustable switch-over timing

    externally adjustable idle mode timing

    externally adjustable dial tone detector in receive channel
  - voice switch control with:

    adjustable switching range

    constant sum of gain during switching

    constant sum of gain at different volume settings.

APPLICATIONS

- Mains, battery or line-powered telephone sets
- Cordless telephones
- Answering machines
- Fax machines.

GENERAL DESCRIPTION

The TEA1095 is a bipolar circuit intended for use in mains, battery or line-powered telephone sets, cordless telephones, answering machines and fax machines. In conjunction with a member of the TEA106X, TEA111X families of transmission or TEA1096 transmission/listening-in circuits, the device offers a hands-free function. It incorporates a transmit amplifier, a receiver channel amplifier and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1095	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
TEA1095T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

QUICK REFERENCE DATA

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTETX = LOW; MUTERX = LOW; PD = LOW; R_{VOL} = 0 Ω; measured in test circuit of Fig.11 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BB}	supply voltage		2.9	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	2.7	3.8	mA
G_{vtx}	voltage gain from TXIN to TXOUT in transmit mode	V_{TXIN} = 1 mV(RMS); R_{GATX} = 30.1 kΩ	–	15.5	–	dB
ΔG_{vtxr}	gain adjustment with R_{GATX}		−15.5	–	+24.5	dB
G_{vrx}	voltage gain in receive mode from RXIN to RXOUT	V_{RXIN} = 20 mV(RMS); R_{GARX} = 16.5 kΩ	–	6.5	–	dB
ΔG_{vrxr}	gain adjustment with R_{GARX}		−20.5	–	+19.5	dB
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to R_{SWR} = 365 kΩ		−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

BLOCK DIAGRAM

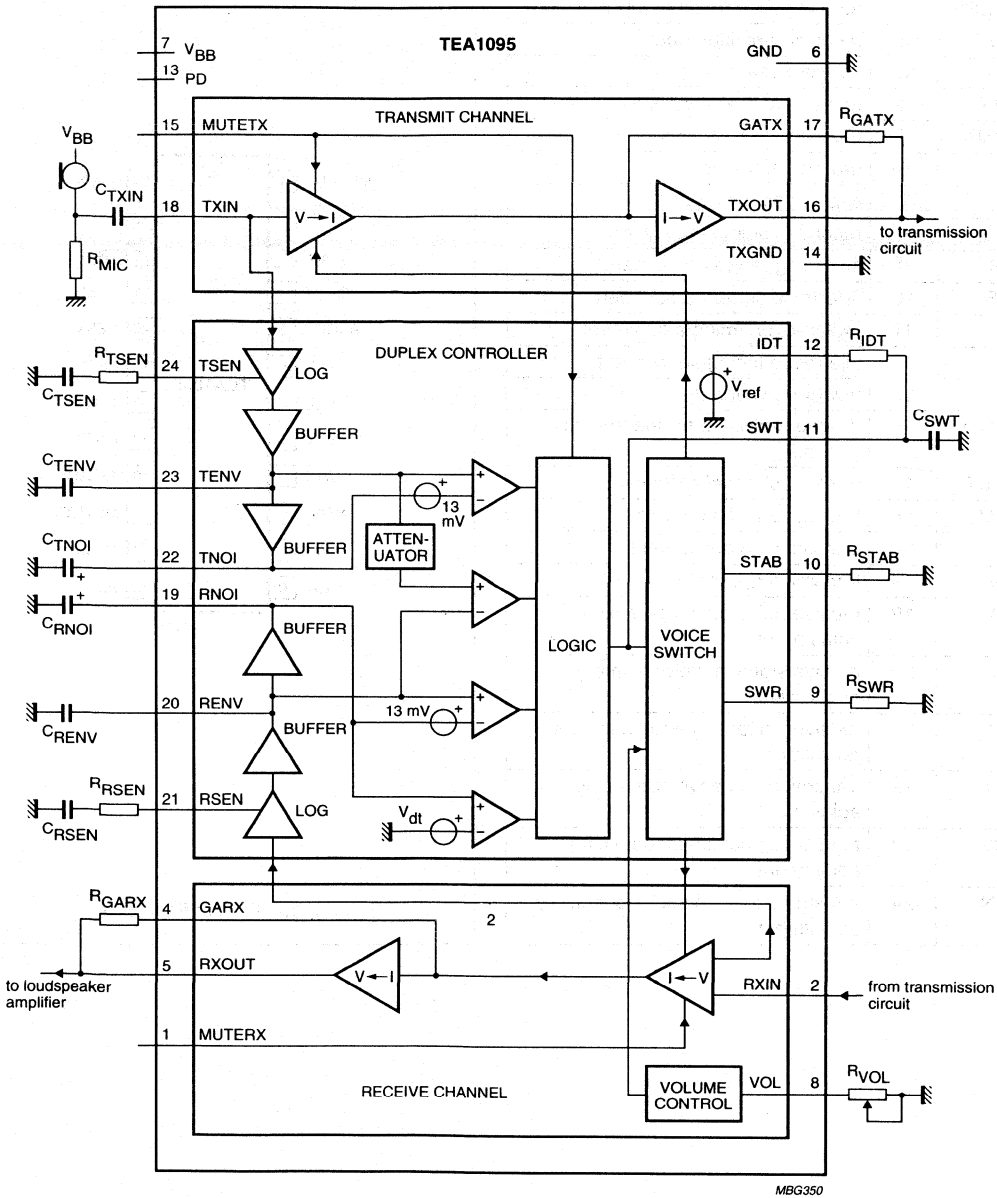


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MUTERX	1	receiver channel mute input
RXIN	2	receiver amplifier input
n.c.	3	not connected
GARX	4	receiver gain adjustment
RXOUT	5	receiver amplifier output
GND	6	ground reference
V_{BB}	7	supply voltage input
VOL	8	receiver volume adjustment
SWR	9	switching range adjustment
STAB	10	reference current adjustment
SWT	11	switch-over timing adjustment
IDT	12	idle mode timing adjustment
PD	13	power-down input
TXGND	14	ground reference for the transmit channel
MUTETX	15	transmit channel mute input
TXOUT	16	transmit amplifier output
GATX	17	transmit gain adjustment
TXIN	18	transmit amplifier input
RNOI	19	receive noise envelope timing adjustment
RENV	20	receive signal envelope timing adjustment
RSEN	21	receive signal envelope sensitivity adjustment
TNOI	22	transmit noise envelope timing adjustment
TENV	23	transmit signal envelope timing adjustment
TSEN	24	transmit signal envelope sensitivity adjustment

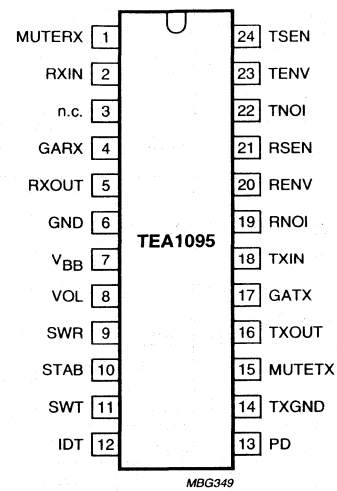


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The values given in the functional description are typical values except when otherwise specified.

A principle diagram of the TEA1096 is shown on the left side of Fig.3. The TEA1096 is a transmission and listening-in circuit. It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone, a loudspeaker amplifier and a hybrid. For more details on the TEA1096 circuit (please refer to *Data Handbook IC03*). The right side of Fig.3 shows a principle diagram of the TEA1095, a hands-free add-on circuit with a transmit amplifier, a receiver amplifier and a duplex controller.

As can be seen from Fig.3, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1095 detects which channel has the 'largest' signal and then controls the gains of the transmit amplifier and the receiver amplifier such that the sum of the gains remains constant. As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode): the gain of the transmit amplifier is at its maximum and the gain of the receiver amplifier is at its minimum.
2. Receive mode (Rx mode): the gain of the receiver amplifier is at its maximum and the gain of the transmit amplifier is at its minimum.
3. Idle mode: the gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

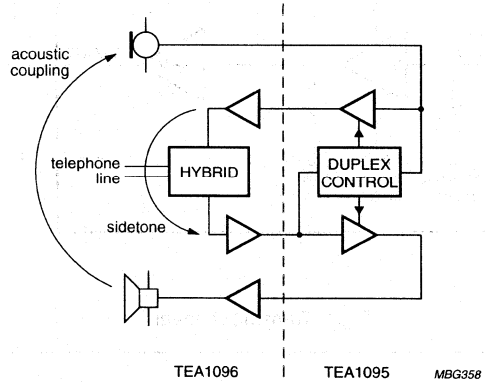


Fig.3 Hands-free telephone set principles.

Supply: pins V_{BB}, GND and PD

The TEA1095 must be supplied with an external stabilized voltage source between pins V_{BB} and GND. In idle mode, without any signal, the internal supply current is 2.7 mA at V_{BB} = 5 V.

To reduce current consumption during pulse dialling or register recall (flash), the TEA1095 is provided with a power-down (PD) input. When the voltage on PD is HIGH, the current consumption from V_{BB} is 140 µA.

Transmit channel: pins TXIN, GATX, TXOUT, TXGND and MUTETX

The TEA1095 has an asymmetrical transmit input (TXIN) with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1095. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The output capability at pin TXOUT is 20 µA (RMS).

In the transmit mode, the overall gain of the transmit amplifier (from pin TXIN to TXOUT) can be adjusted from 0 dB to 40 dB to suit application specific requirements. The gain is proportional to the value of R_{GATX} and equals 15.5 dB with R_{GATX} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GATX} to ensure stability of the transmit amplifier. Together with R_{GATX}, it also provides a first-order low-pass filter.

By applying a HIGH level on pin MUTETX, the transmit amplifier is muted and the TEA1095 is automatically forced into the receive mode.

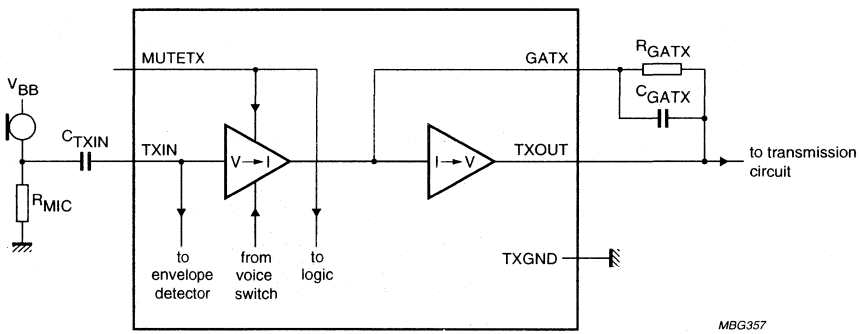


Fig.4 Transmit channel

Receive channel

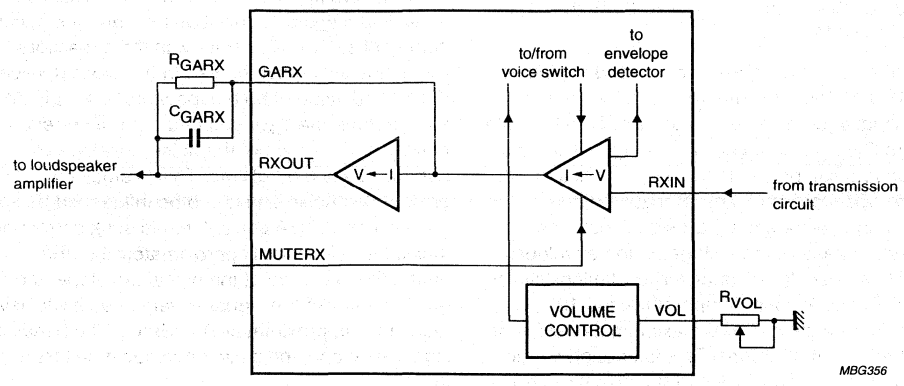


Fig.5 Receive channel

RECEIVER AMPLIFIER: PINS RXIN, GARX, RXOUT AND MUTERX

The TEA1095 has an asymmetrical input (RXIN) for the receiver amplifier with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1095. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free.

In the receive mode, the overall gain of the receive amplifier can be adjusted from −14 dB to +26 dB to suit application specific requirements. The gain from RXIN to RXOUT is proportional to the value of R_{GARX} and equals 6.5 dB with R_{GARX} = 16.5 kΩ. A capacitor connected in parallel with R_{GARX} can be used to provide a first-order low-pass filter.

By applying a HIGH level on pin MUTERX, the receiver amplifier is muted and the TEA1095 is automatically forced into the transmit mode.

VOLUME CONTROL: PIN VOL

The receiver amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain of the receiver amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelopes detectors are shown in Fig.6.

For the transmit channel, the input signal at TXIN is 40 dB amplified to TSEN. For the receive channel, the input signal at RXIN is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}.

The capacitors connected in series with the two resistors block any DC component and form a first order high-pass filter. In the basic application (see Fig.12), it is assumed that V_{TXIN} = 1 mV (RMS) and V_{RXIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitors C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is enough to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is enough for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

To determine the noise level, the signal on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.12, the value of both capacitors is 4.7 μF. At room temperature, the 1 μA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms. This is small enough to track background noise and not to be influenced by speech bursts. The 120 μA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.7.

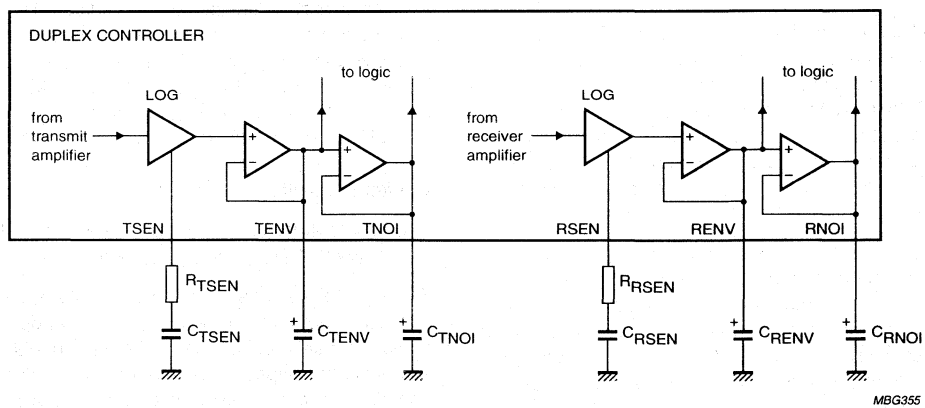


Fig.6 Signal and noise envelope detectors.

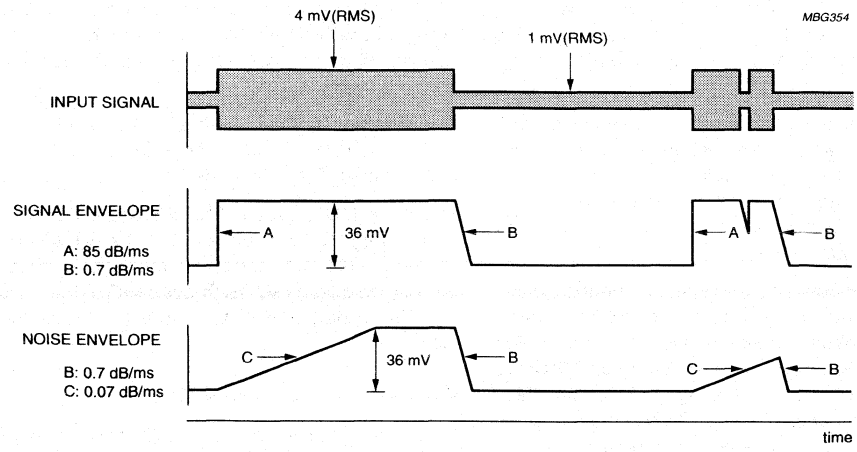
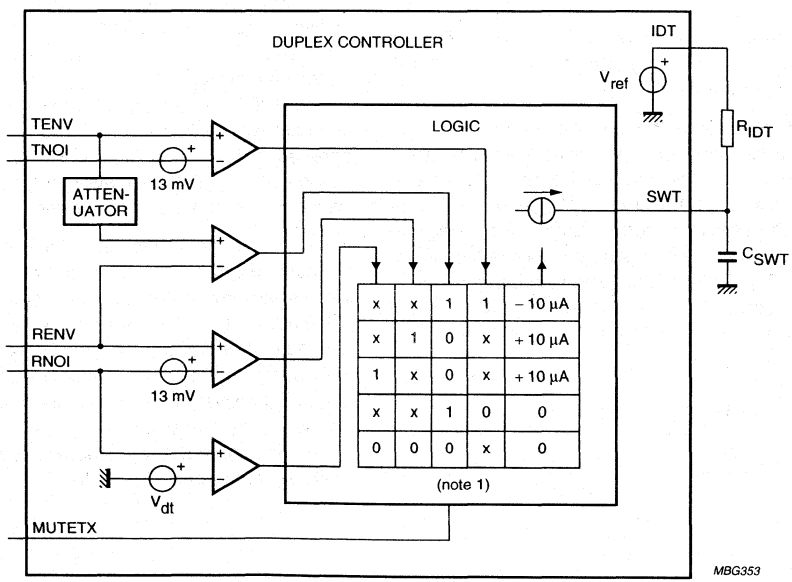


Fig.7 Signal and noise envelope waveforms.

DECISION LOGIC: PINS IDT AND SWT



x	x	1	1	− 10 µA
x	1	0	x	+ 10 µA
1	x	0	x	+ 10 µA
x	x	1	0	0
0	0	0	x	0

(1) When MUTETX = HIGH +10 µA is forced. When MUTERX = HIGH −10 µA is forced.

Fig.8 Decision logic.

The TEA1095 selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV-NOI}$ = 13 mV. This so called speech/noise threshold is implemented in both channels.

The signal on TXIN contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the transmit amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1095 to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard application, does not consider the input signals at RXIN as noise when they have a level greater than 42 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.8, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1095 and can vary between −400 mV and +400 mV.

Table 1 Modes of TEA1095.

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.12, C_{SWT} is chosen at 220 nF and R_{IDT} at 2.2 MΩ.

This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time from receive mode or transmit mode to idle mode is equal to $4 \times R_{IDT} C_{SWT}$ and is approximately 2 s (idle mode time).

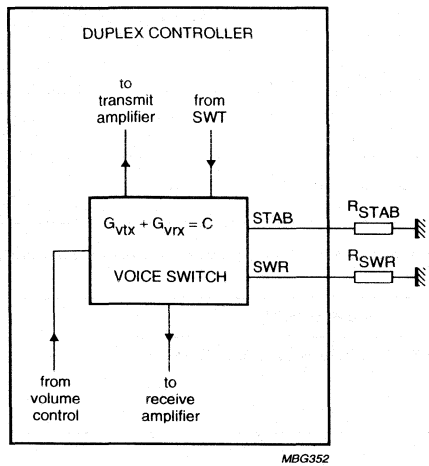
The inputs MUTETX and MUTERX overrule the decision logic. When MUTETX goes HIGH, the capacitor C_{SWT} is charged with 10 μA resulting in the receive mode. When the voltage on pin MUTERX goes HIGH, the capacitor C_{SWT} is discharged with 10 μA resulting in the transmit mode.

VOICE-SWITCH: PINS STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.9. With the voltage on SWT, the TEA1095 voice-switch regulates the gains of the transmit and the receive channel such that the sum of both is kept constant.

In the transmit mode, the gain of the transmit amplifier is at its maximum and the gain of the receive amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both transmit and receive amplifier gains are halfway. The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be equal to 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.12, R_{SWR} is equal to 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.10.

In the receive mode, the gain of the receive amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the transmit amplifier is increased at the same time (see dashed curves in Fig.10). In the transmit mode however, the volume control has no influence on the gain of the transmit amplifier or the gain of the receive amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.



Where C = constant.

Fig.9 Voice switch.

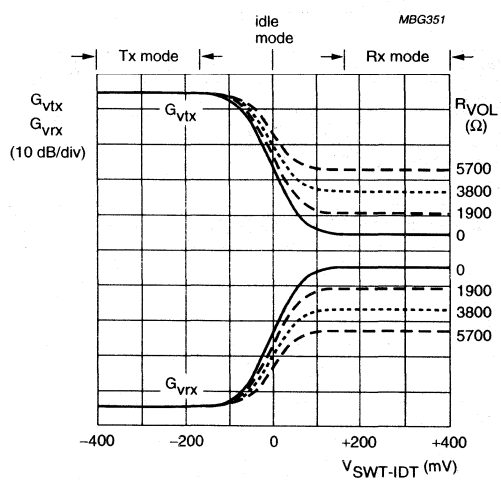


Fig.10 Switch-over behaviour.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins V_{BB}, and RXIN		V_{GND} – 0.4	V_{BB} + 0.4	V
$V_{RIN(max)}$	maximum voltage on pin RXIN		V_{GND} – 1.2	V_{BB} + 0.4	V
$V_{BB(max)}$	maximum voltage on pin V_{BB}		V_{GND} – 0.4	12.0	V
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1095	50	K/W
	TEA1095T	75	K/W

CHARACTERISTICS

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTETX = LOW; MUTERX = LOW; PD = LOW; R_{VOL} = 0 Ω; measured in test circuit of Fig.11; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_{BB}, PD and GND)						
V_{BB}	supply voltage		2.9	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	2.7	3.8	mA
POWER-DOWN INPUT PD						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{PD}	power-down input current	PD = HIGH	–	2.5	5	µA
$I_{BB(PD)}$	current consumption from pin V_{BB} in power-down mode	PD = HIGH	–	140	190	µA
Transmit channel (TXIN, GATX, TXOUT, MUTETX and TXGND)						
TRANSMIT AMPLIFIER						
$\|Z_i\|$	input impedance between pins TXIN and TXGND		17	20	23	kΩ
G_{vtx}	voltage gain from pin TXIN to TXOUT in transmit mode	V_{TXIN} = 1 mV (RMS)	–	15.5	–	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GATX}		–15.5	–	+24.5	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{TXIN} = 1 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{TXIN} = 1 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{notx}	noise output voltage at pin TXOUT	pin TXIN connected to TXGND through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	–100	–	dBmp
TRANSMIT MUTE INPUT MUTETX						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{MUTETX}	input current	MUTETX = HIGH	–	2.5	5	µA
ΔG_{vtxm}	voltage gain reduction with MUTETX active	MUTETX = HIGH	–	80	–	dB
Receive channel (RXIN, GARX, RXOUT and MUTERX)						
RECEIVE AMPLIFIER						
$\|Z_i\|$	input impedance between pins RXIN and GND		17	20	23	kΩ
G_{vrx}	voltage gain in receive mode; between RXIN and RXOUT	V_{RXIN} = 20 mV (RMS)	–	6.5	–	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GARX}		–20.5	–	+19.5	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RXIN} = 20 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RXIN} = 20 mV (RMS); f_i = 300 to 3400 Hz	–	±0.3	–	dB
$V_{norx(rms)}$	noise output voltage at pin RXOUT (RMS value)	input RXIN short-circuited through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	20	–	µV
ΔG_{vrxv}	voltage gain variation referenced to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	–	3	–	dB
RECEIVE MUTE INPUT MUTERX						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{MUTERX}	input current	MUTERX = HIGH	–	2.5	5	µA
ΔG_{vrxm}	gain reduction with MUTERX active	MUTERX = HIGH	–	80	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Envelope and noise detectors (TSEN, TENV, RSEN and RENV)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from TXIN to TSEN		–	40	–	dB
$G_{v(RSEN)}$	voltage gain between RXIN to RSEN		–	0	–	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\varphi_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 μA	–	18	–	mV
$\varphi_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 μA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	μA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	μA
ΔV_{ENV}	voltage difference between pins RENV and TENV	when 10 μA is sourced from both RSEN and TSEN; envelope detectors tracking; note 1	–	±3	–	mV
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pins TNOI or RNOI		0.75	1	1.25	μA
$I_{sink(NOI)}$	maximum current sunk by pins TNOI or RNOI		–	120	–	μA
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	when 2 μA is sourced from both RSEN and TSEN; noise detectors tracking; note 1	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pin RXIN (RMS value)		–	42	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	$V_{RXIN} < V_{RINDT}$; note 2	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 2	–	13	–	mV
SWITCH-OVER						
$I_{sourceSWT}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	µA
$I_{sinkSWT}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	µA
$I_{idleSWT}$	current sourced from pin SWT in idle mode		–	0	–	µA
Voice switch (STAB and SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to 365 kΩ	–40	–	+12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to ±1 dB tracking.
2. Corresponds to 4.3 dB noise/speech recognition level.

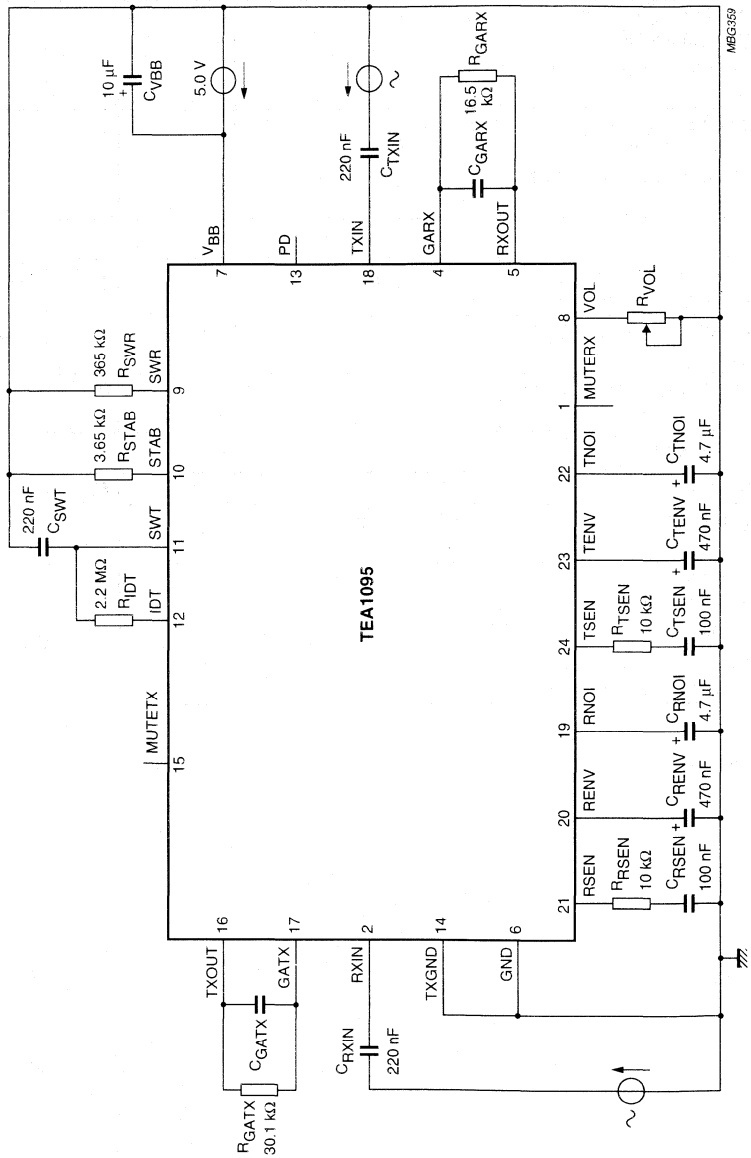


Fig.11 Test circuit.

APPLICATION INFORMATION

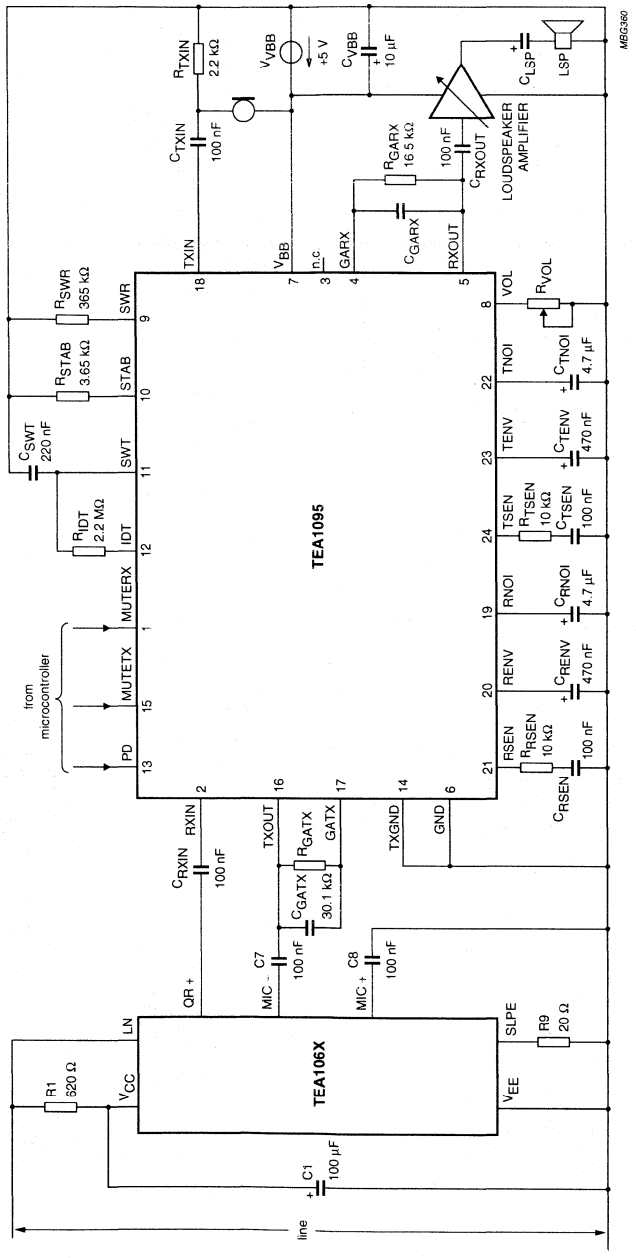
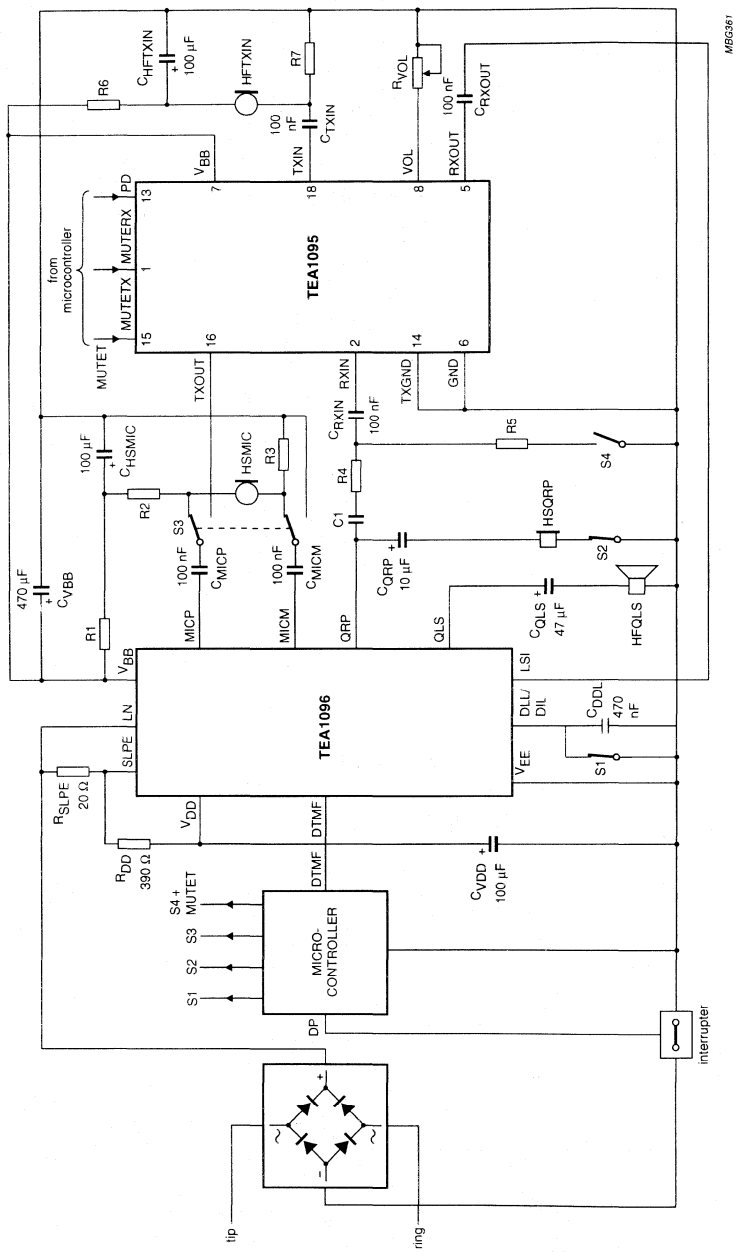


Fig.12 Basic application diagram.



MODE	SWITCH				MUTET
	S1	S2	S3	S4	
Hands-free	OPEN	OPEN	TXOUT	OPEN	LOW
Handset	CLOSED	CLOSED	HSMIC	OPEN	DON'T CARE
Handset plus listening-in	OPEN	CLOSED	HSMIC	CLOSED	HIGH

Fig.13 Application example.

TEA1095—Voice switched speakerphone IC AN95083

Author: Jean–Marie Malaurie

ABSTRACT

The TEA1095 is a high performance, low power consumption voice switched speakerphone IC designed for integration of a handsfree function in terminal environments.

A detailed description of the IC, advices on adjustments and a worked–out application example are contained in this report.

SUMMARY

A detailed description of the TEA1095 is given. In conjunction with TEA1096 (transmission circuit with built–in loudspeaker amplifier), it offers a handsfree function. The TEA1095 incorporates a microphone amplifier and a duplex controller with signal and noise monitors on the transmit and receive channels. A cookbook gives the general application steps.

NOTES

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1. INTRODUCTION

The TEA1095 is a circuit which, in combination with TEA1096 (transmission circuit with built–in loudspeaker amplifier), offers a handsfree function. It incorporates a microphone amplifier, a volume control of the receive channel and a duplex controller with signal and noise monitor on the transmit and receive channel. In contrary with the Philips handsfree circuits TEA1093 and TEA1094, the TEA1095 has neither integrated supply nor loudspeaker amplifier. This makes the TEA1095 more flexible for implementation in applications with external loudspeaker amplifier, external supply, such as cordless telephones and answering machines.

The function of the handsfree application will be illustrated with the help of fig 1.1.

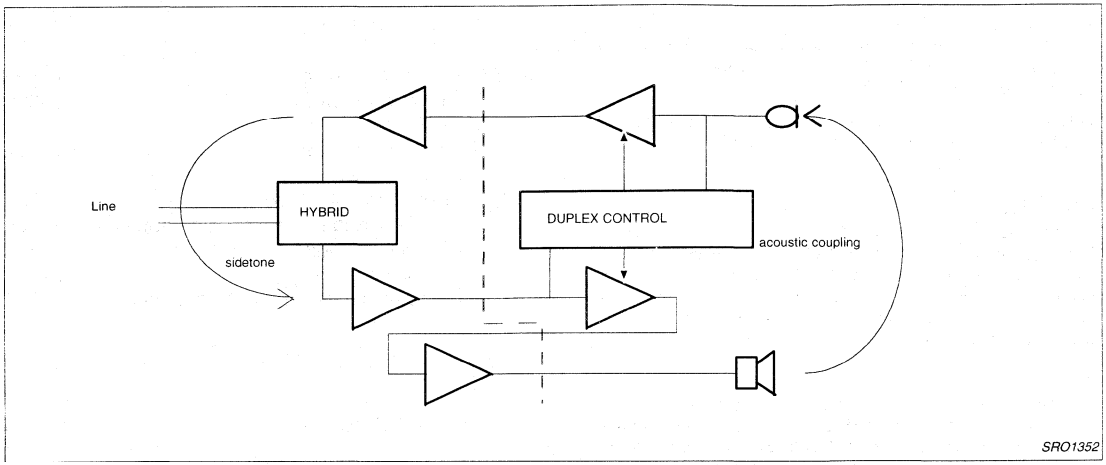


Figure 2.1 Handsfree Telephone Set Principle

The left side of fig 1.1 shows a principle diagram of a part of the TEA1096 circuit by means of a receiving amplifier, a transmit amplifier, the loudspeaker amplifier and the hybrid. The right side of fig 1.1 shows a principle diagram of a part of the TEA1095 circuit by means of the microphone amplifier and the duplex controller.

As can be seen from fig 1.1, a closed loop is formed via the amplifiers, the antisidetone network and the acoustic coupling between loudspeaker and microphone. When the loop–gain is higher than one, the set starts howling. In a full–duplex application, this would be the case. To avoid howling, the duplex controller reduces the loop–gain to a value much lower than one.

The duplex controller of the TEA1095 monitors the signal and noise on both the transmit and the receive channel in order to detect which channel contains the 'largest' signal. As a result, the duplex controller reduces the gain of the channel which contains the smallest signal. This is done such that the sum of the transmit and the receive gains remains constant.

As a result, the circuit can be in three stable modes to be referred to throughout this report::

Transmit mode (Tx–mode): the gain of the microphone amplifier is at its maximum and the gain of the receive path (to loudspeaker amplifier) is reduced.

Receive mode (Rx–mode): the gain of the receive path is at its maximum and the gain of the microphone amplifier is reduced.

Idle mode (Ix–mode): the gain of the microphone amplifier and of the receive path are halfway their maximum and reduced values.

The difference between the maximum gain and the reduced gain is called the switching range.

This report gives a detailed description of the TEA1095 and its application with the TEA1096. The description is given by means of the block diagram of the TEA1095 (&2) and by discussing every detail of the sub–blocks (&3). The application is discussed by giving a guideline for application (the application cookbook &4) and by giving an application example (&5). EMC aspects are also discussed (&6). The appendices contain a measurement setup for the electro–acoustical adjustment of the TEA1095 handsfree application (A), a list of abbreviations (B) and application diagrams of the TEA1095 (fig. C1, C2).

2. BLOCK DIAGRAM

In this chapter, the block diagram of the TEA1095 is shown by means of fig.2.1. The pinning of the TEA1095 is given by means of fig.2.2. A short description of the block diagram is given including the function of the external components.

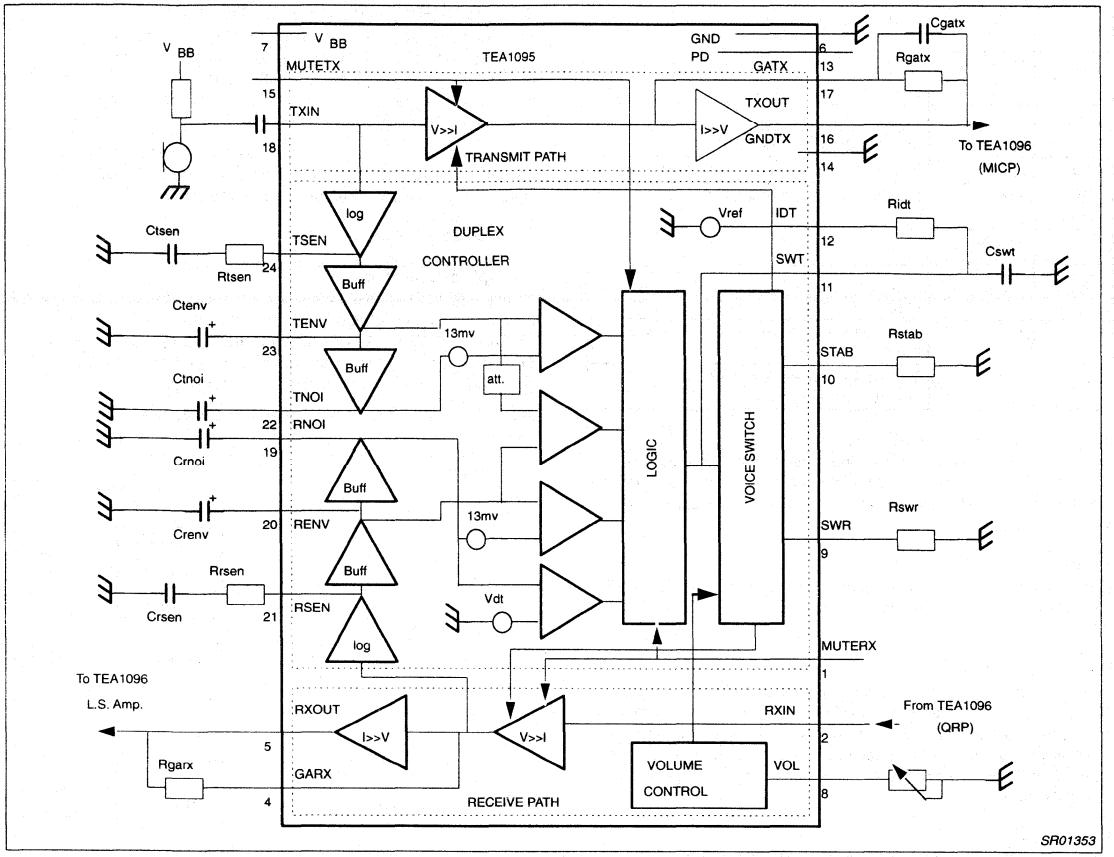


Figure 2–1. Block Diagram of TEA1095

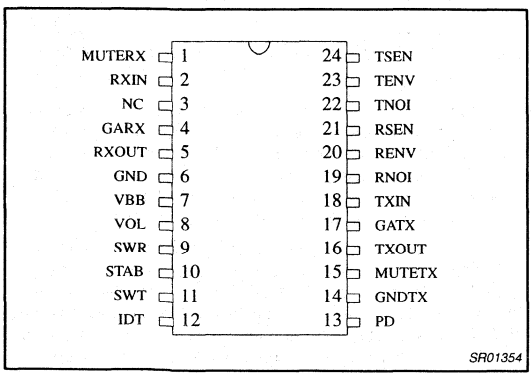


Figure 2.2. Pinning of TEA1095

PIN	NAME	DESCRIPTION
1	MUTERX	Receive channel mute input
2	RXI	Receive channel input
3	NC	Not connected
4	GARX	Receive gain adjustment
5	RXOUT	Receive channel output
6	GND	Ground reference
7	VBB	Positive supply input
8	VOL	Receive channel volume adjustment
9	SWR	Switching range adjustment
10	STAB	Reference current adjustment
11	SWT	Switching timing adjustment
12	IDT	Idle–mode timing adjustment
13	PD	Power–down input

14	GNDTX	Ground reference for microphone amplifier
15	MUTETX	Transmit channel mute input
16	TXOUT	Transmit channel output
17	GATX	Microphone gain adjustment
18	TXIN	Microphone amplifier input
19	RNOI	Receive noise envelope timing adjustment
20	RENV	Receive signal envelope timing adjustment
21	RSEN	Receive signal envelope sensitivity adjustment
22	TNOI	Transmit noise envelope timing adjustment
23	TENV	Transmit signal envelope timing adjustment
24	TSEN	Transmit signal envelope sensitivity adjustment

In fig.2.1 it can be seen that the IC consists out of four parts: the supply, the microphone amplifier, the receive path and the duplex controller. These blocks will be shortly described below including the function of the external components. The detailed description will follow in chapter 3.

Supply :
The circuit is supplied between pins VBB and GND. The TEA1095 can be switched into a low power consumption mode with the pin PD.

Microphone amplifier :
The handsfree microphone signal is amplified from pin TXIN to pin TXOUT. The signal reference is GNDTX, a "clean ground" which has to be connected to GND. The input TXIN has to be coupled to the microphone by means of a capacitor. The gain of the amplifier can be set with Rgatx. This amplifier can be muted by making pin MUTETX high.

Receive path :
The receive signal is amplified from pin RXIN to pin RXOUT. The input RXIN has to be coupled by means of a capacitor. The gain of the amplifier can be set with Rgarx, and the volume of the receive signal can be adjusted by means of the potentiometer connected between input VOL and GND. This channel can be muted by making pin MUTERX high.

Duplex controller :
From both the transmit and receive signal, signal and noise envelopes are made. The transmit signal envelope is on pin TENV and the receive one on pin RENV. The transmit noise envelope is on pin TNOI and the receive one on pin RNOI. The timing of the envelopes can be set by the capacitors Ctenv, Ctnoi, Crenv and Crnoi. The sensitivity of the envelope detectors can be set by means of the RC combinations Rtsen with Ctsen for the transmit envelope and Rrsen with Crsen for the receive one. The resistors set the sensitivity and the capacitors block the DC–component, creating also high–pass filters.

The logic determines to which mode (Tx, Rx or Ix–mode) the set has to switch over. The timing for switching to the Tx or the Rx –mode is determined with the capacitor Cswt. The timing for switching to the Ix–mode is set by the combination Cswt and Ridt. The switching range is determined by the resistor Rswr. Resistor Rstab has a fixed value.

3. DESCRIPTION OF THE TEA1095

This chapter describes in detail the four blocks of the duplex controller circuit TEA1095: the supply (3.1), the microphone amplifier (3.2), the receive path (3.3) and the duplex controller (3.4). For each block the principle of operation is described and its adjustments and performances are discussed.

All values given in this chapter are typical and at room temperature unless otherwise stated. For more details of the TEA1095 specification, see TEA1095 device specification.

3.1 Supply block

Principle of operation
As opposite to TEA1093 which includes an integrated supply which stabilizes a supply voltage out of the line current and as the TEA1094, the TEA1095 has no integrated supply. This makes the TEA1095 most suitable for applications where the handsfree controller is supplied from an external voltage source.

In fig. 3.1.1, different supply arrangements with TEA1095 are shown.

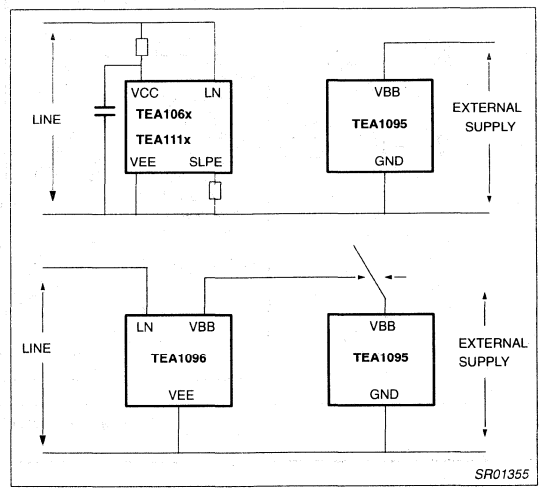


Figure 3.1.1. Supply Arrangement Examples With TEA1095

As can be seen, the line current flows through the TEA106x or the TEA1096, while the TEA1095 is supplied from an external voltage source. Nevertheless, as can be seen in the bottom example, TEA1096 is able to provide this supply, leading to a line–powered very integrated solution. The common reference for all signals is GND on TEA1095 and VEE on TEA106x or TEA1096 side.

In case of a line–powered application using TEA106x or TEA111x, the TEA1095 as well as an external loudspeaker amplifier can be supplied via a large coil (or TEA1081) connected between line and VBB. At VBB, a capacitor has to be connected to serve as reservoir. The TEA1095 and the loudspeaker amplifier have to be referenced at SLPE in order not to influence the transmission characteristics.

In fig.3.1.1 no galvanic insulation is drawn. When such is needed, the insulation can be done in the supply part or in the signal interfacing. In the supply part, the galvanic insulation can be done in the main–adaptor. In the signal interfacing between the TEA1095

and the TEA106x, the galvanic insulation can be done either with transformers or with opto–couplers.

The power consumption of the TEA1095 can be dramatically reduced when its functionalities are not required by making pin PD high.

Adjustments and performances

The voltage which can be applied between VBB and GND may vary between 2.9 V and 12 V. The 12 V is an absolute maximun rating. When a supply is used which may generate, during transients, a higher voltage, an appropriate protection device must be applied between VBB and GND in order to control this voltage.

The current consumption of the TEA1095 is typically 2.7 mA at VBB = 5 V. At higher voltages, the current consumption slightly increases.

In power–down mode, the current consumption is typically reduced to 140 mA at VBB = 5 V.

3.2 MICROPHONE AMPLIFIER BLOCK

In the first paragraph of this chapter, the principle of operation of the microphone amplifier is described as well as its adjustments and performance. In the second paragraph, the mute transmit function is described.

3.2.1 Microphone amplifier

Principle of operation

In fig. 3.2.1 the block diagram of the microphone amplifier of the TEA1095 is depicted together with the interconnection with the TEA1096.

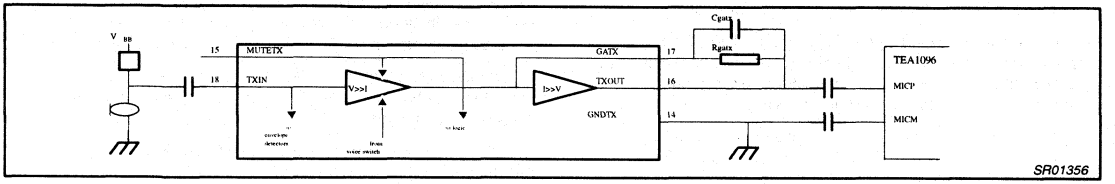


Figure 3.2.1. Block Diagram of the Microphone Path

As can be seen in fig.3.2.1, the microphone amplifier is referenced to pin GNDTX instead of being referenced to GND. This is in order to prevent interference from other blocks of the TEA1095 or of the application, GNDTX is called a clean ground. The input and output signals of the microphone channel have to be referenced to GNDTX. Pin GNDTX itself has to be referenced to GND.

The input of the microphone amplifier is pin TXIN. It is an assymmetrical input well suited for electret microphones. Induced signals in the short wire between the microphone and pin TXIN are assumed to be negligible. This in contrary with the handset microphone which is connected via the handset cord. The TEA106x/TEA111x families as well as the TEA1096 have symmetrical microphone inputs.

The output of the microphone amplifier is pin TXOUT. When interconnecting the TEA1095 and the TEA1096, pin TXOUT is preferably connected to the TEA1096 input MICP, in that case, pin MICM of the TEA1096 is connected to pin GNDTX.

As can be seen in fig.3.2.1, the microphone amplifier is built up out of two parts: a preamplifier and an end–amplifier. The gain of the preamplifier is determined by the duplex controller block, see & 3.4. The gain of the end–amplifier is determined by the external feedback resistor Rgatx.

The overall gain (Atx) of the microphone amplifier from input TXIN to output TXOUT in TX–mode is given as:

Atx = 20 * log (0.72 * Rgatx / Rstab).

With Rstab being the resistor at pin STAB of 3.65 k.

Adjustments and performances

A handsfree microphone, referenced to GNDTX, can be connected to the input TXIN via a DC blocking capacitor Ctxi. Together with the input impedance of pin TXIN of 20 k, this capacitor form a first order high–pass filter which can be used to adjust the transmit curve.

The handsfree electret microphone can be supplied from VBB via a resistor. However, during normal operation, VBB may contain a small riple, and due to poor power supply rejection of electret microphones it is advised to add an RC smoothing filter in the feeding part, as shown in fig.3.2.2.

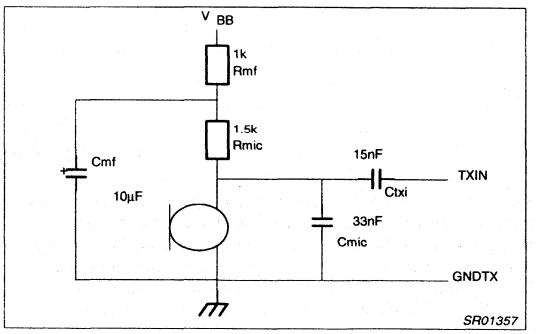


Figure 3.2.2. Supply Arrangement for Electret Microphone

As shown in fig.3.2.2, the RC smoothing filter is referenced to GNDTX in order to have one good reference for the whole microphone signal path. On the printed circuit board lay–out GNDTX can be connected with a separate wire to pin VEE of the TEA1096 in order to reduce ground interference as much as possible.

The sensitivity of the electret microphone is set via resistor Rmic. By putting a capacitor Cmic in parallel with the microphone, a first order low–pass filter is formed for the microphone signal in order to adjust the transmit curve.

Via the resistor Rgatx, the gain of the microphone amplifier can be adjusted from –15 to +25 dB to suit application specific requirements. With the resistor Rgatx = 30.1 k, the gain equals typically 15.5 dB.

Capacitor Cgatx is applied in parallel with resistor Rgatx to ensure stability of the microphone amplifier, it also provides a first order low–pass filter for the adjustment of the transmit curve.

The input of the microphone amplifier can handle signals up to 18 mVrms with 2% total harmonic distortion. However, the microphone input signal is also used by the duplex controller, see &3.4. At 10 mVpeak at the input, the positive part of the signal on pin TSEN starts clipping which might influence the switching behavior. It is therefore advisable to keep the microphone input signal below this level.

The output drive capability at pin TXOUT is 20 mArms.

The output noise at TXOUT of the TEA1095 is –100 dBmp (psophometrically weighted) at a gain of 15 dB. With a sending gain of the TEA1096 set at 35 dB (total handsfree transmit gain of 50 dB), the noise level on the line will be : –65 dBmp.

In TX–mode, the noise level will be at its maximum. In Ix–mode and Rx–mode, the noise at TXOUT will be lower because the contribution of the preamplifier is reduced. However, the bottom level of the sending noise at TXOUT is limited by the end–amplifier and is about –110 dBmp.

The bottom level of the sending noise on the line is determined either by the speech circuit (TEA1096 or TEA106x/TEA111x) or by the noise at TXOUT increased by the transmit gain of the speech circuit, whichever is largest. When in Ix–mode, the noise on the line is due to TXOUT noise level, it can be reduced by changing the distribution of the gains between TEA1095 and speech circuit : increasing the transmit gain of the TEA1095 and decreasing with the same value the gain on the speech circuit side by modification of the attenuation placed between TXOUT and MICP of the speech circuit.

3.2.2 Transmit mute

During handsfree operation, the microphone can be muted by making pin MUTETX high, so conversation cannot be heard by the other party. When the microphone amplifier is muted, automatically the TEA1095 switches over to the RX–mode, see also &3.4.

When a logic high is applied to MUTETX, meaning the voltage on MUTETX is higher than 1.5 V, the microphone preamplifier is muted. The end–amplifier can still be used by applying a current signal on GATX. The obtained gain reduction is 80 dB. The current which has to be sourced into pin MUTETX when high is typically 2.5 mA.

When MUTETX is logic low, meaning the voltage on MUTETX is lower than 0.3 V or pin MUTETX is left open, the microphone amplifier is not muted.

The maximum allowable voltage on pin MUTETX is VBB+0.4 V, the minimum allowable is GND–0.4 V.

3.3 Receive path block

The block diagram of the complete receive path block is depicted in fig.3.3.1

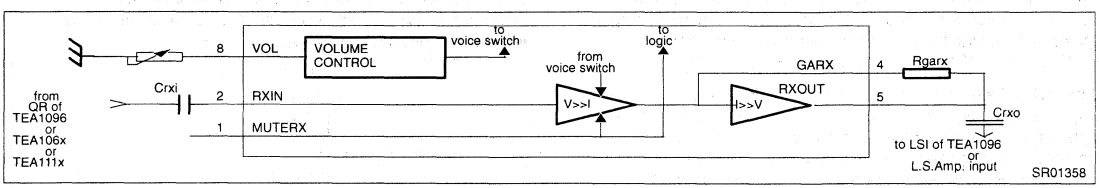


Figure 3.3.1. Principle of the Receive Path

As can be seen in fig.3.3.1, the receive channel is built up out of two parts: the receive path itself and the volume control. In the first paragraph of this chapter, the principle of operation of the receive path is described as well as its adjustments and performances. In the second paragraph, the same items are described for the volume control. In the third paragraph, the receive mute function is described.

3.3.1 Receive path

Principle of operation

As can be seen in fig.3.3.1, the input of the receive channel, pin RXIN is assymetrical and the signal has to be referenced to GND. The input RXIN can be connected, via a decoupling capacitor, to the earphone output QRP of the speech circuit (TEA1096 or TEA106x/TEA111x).

The output of the receive channel is pin RXOUT. When interconnecting the TEA1095 and the TEA1096, pin RXOUT is connected via a decoupling capacitor to input pin LSI of the TEA1096.

As can be seen in fig.3.3.1, the receive path itself is built up out of two parts: a preamplifier and an end–amplifier. The gain of the preamplifier is determined by the duplex controller block. The gain of the end–amplifier is determined by the external feedback resistor Rgarx.

The overall gain (Arx) of the receive path from input RXIN to output RXOUT is given as:

Arx = 20 * log(0.46 * Rgarx / Rstab).

With Rstab being the resistor at STAB of 3.65 k.

ADJUSTMENTS AND PERFORMANCES

The input signal for the receive channel has to be coupled in via the capacitor Crxi to block DC. Together with the input impedance of 20 k at RXIN, a first order high–pass filter is introduced which can be used to adjust the receive curve and/or to reduce any low frequency unwanted signal coming from the line.

The input RXIN can handle signal up to 390 mVrms with a total harmonic distortion of 2%.

The input RXIN is biased at around 0V with respect to GND. By applying a signal to the input, it can become negative. The protection on this pin is made different from other pins which makes it possible to have RXIN as low as –1.2 V without damaging the circuit.

The output RXOUTcan be connected to the LSI input of TEA1096 or the input of any loudspeaker amplifier via a decoupling capacitor Crxo. The output is biased at 1.4 V referenced to GND. Together with the input impedance of the loudspeaker amplifier, Crxo forms a first order high–pass filter. With the resistor Rgarx, the gain of the receive path can be adjusted from –20 to +20 dB. The gain equals typically 6.3 dB with resistor Rgarx=16.2 k. A capacitor Cgarx can be connected in parallel with Rgarx to provide a low pass filter which can be used to adjust the loudspeaker amplifier curve.

The output drive capability at pin RXOUT is 100mArms.

The noise level at the output RXOUT is –91 dBmp at a gain of 6 dB and with the input RXIN shorted with 200 to GND.

3.3.2 Volume control

Principle of operation

Via the volume control block, the volume of the receive signal can be adjusted by the external potentiometer connected to pin VOL. By changing the potentiometer resistance, the gain of the preamplifier varies through the duplex controller. Volume control doesn't affect the transmit gain in Tx–mode.

Adjustments and performances

Out of pin VOL a current Ivol, set by Rstab, see &3.4, is flowing which is proportional to the absolute temperature (PTAT). At room temperature this current is around 10 mA. Together with the resistance of the potentiometer, the current Ivol creates a PTAT voltage on pin VOL. This PTAT voltage is processed by the volume control block, as a result, a temperature independent volume reduction of the output receive signal of 3 dB is obtained at approximately every increase of 950 of the potentiometer resistance.

This means that a linear potentiometer can be used to control the volume logarithmically, thus in dB. With the advised value of 10 k, the maximum gain reduction of the volume control is more than 30 dB. However, this maximum gain reduction is limited by the switching range, see &3.4. When the resistance of the potentiometer is zero, the receive gain is maximum in Rx–mode.

When digital volume control is desired, the switches can be either MOSFETs or analog switches with very low saturation voltage. Due to saturation voltage, it is advised not to use bipolar transistors as switches.

When a voltage is applied to pin VOL to control the volume, preferably this voltage has to be a PTAT voltage source. If not, the obtained gain varation is no longer temperature compensated.

3.3.3 Receive mute

During handsfree operation, the receive channel can be muted by making pin MUTERX high. As a result the receive signal is reduced by 80 dB, also the TEA1095 is internally forced into Tx–mode.

When a logic high is applied to MUTERX, meaning a voltage higher than 1.5 V, the receive preamplifier is muted. The end amplifier can still be used by applying a current signal on GARX. The obtained gain reduction is 80 dB when the volume control is set at maximum volume. The current which has to be sourced into pin MUTERX when high is typically 2.5 mA.

When MUTERX is logic low, meaning the voltage is lower than 0.3 V or pin MUTERX is left open, the receive path is muted.

The maximum allowable voltage on pin MUTERX is VBB+0.4 V, the minimum allowable is GND–0.4 V.

3.4 Duplex controller block

In this chapter, the principle of operation of the duplex controller will be described as well as its adjustments and performances. This will be done with the help of fig.3.4.1.

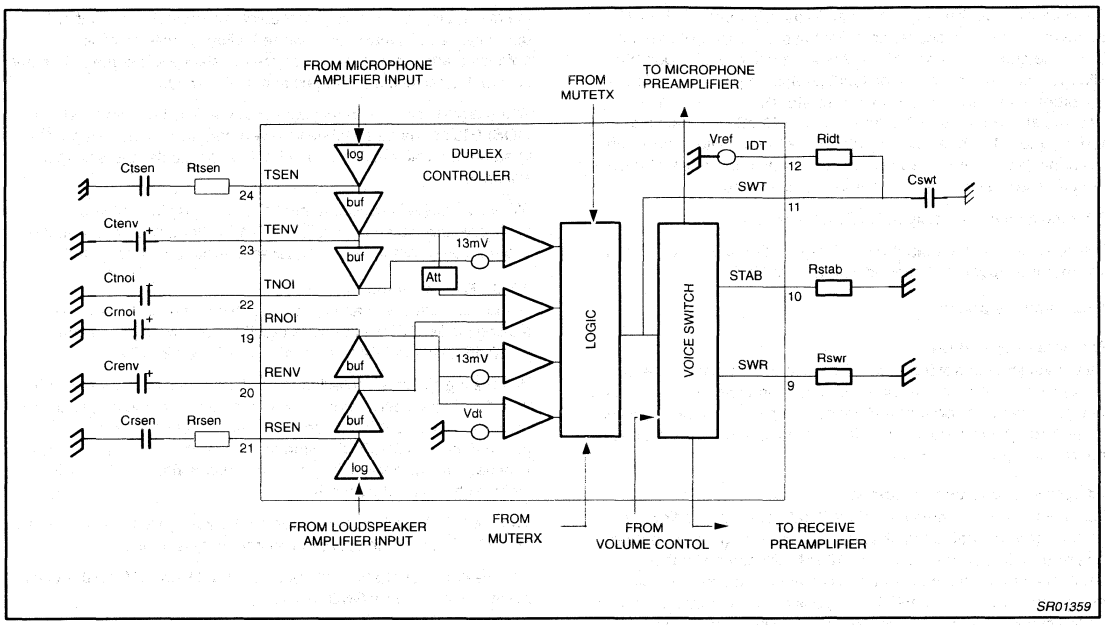


Figure 3.4.1. Principle of the Duplex Controller

As can be seen in fig.3.4.1, the duplex controller is built up out of signal and noise envelope detector, decision logic and a voice switch.

The signal and noise envelope detectors determine the signal envelope and the noise envelope of both the transmit and receive signal. These envelopes are used by the decision logic to determine to which mode the TEA1095 has to switch over (Tx, Rx or Ix–mode). The logic charges and discharges the capacitor Cswt and the resulting voltage on pin SWT controls the voice switch. The voice switch switches over the TEA1095 between the three modes while keeping the loopgain constant.

In paragraphs 3.4.1 to 3.4.3, the principle of operation of the three parts is given. In paragraph 3.4.4, the adjustments and performances of the complete duplex controller are given.

3.4.1d Signal and noise envelope detectors

The signal and noise monitors of the transmit and receive channels are globally the same.

Therefore, the principle of the detectors will be explained with the help of one of them: the signal and noise detector of the transmit channel.

The microphone signal on pin TXIN is sent to the first stage of the detector, see fig.3.4.1. The first stage amplifies the microphone signal from pin TXIN to pin TSEN with an internal gain of 40 dB. Via the RC combination RtsenCtsen, the signal on TSEN is converted into a current. This conversion determines the sensitivity of the envelope detector. The current is logarithmically compressed and internally converted to a voltage which represents the compressed microphone signal. At room temperature, an increase of the microphone signal with a factor of 2 will increase the signal envelope with 18 mV if the current through TSEN stays between 0.8 and 160 mArms. Outside this region the compression is less accurate.

The compressed microphone signal is buffered by the second stage to pin TENV. As the buffer can source 120mA and sink 1mA, the signal on TENV follows the positive peaks of the compressed signal, this signal is called the signal envelope. The time constants of the signal envelope are therefore determined by the combination of the internal current sources and the capacitor Ctenv.

The voltage on TENV is buffered by the third stage to pin TNOI. As this buffer can source 1 mA and sink 120 mA, the signal on TNOI follows the negative peaks of the signal on TENV. This is called the noise envelope because it represents the background noise. The time constants of the noise envelope are determined by the combination of the internal current sources and the capacitor Ctnoi. Both capacitors Ctnoi and Crnoi are provided with a start–up circuit. During start–up the capacitors are charged with approximately 40 mA up to 1.9 V. The starter will restart when the voltage on the capacitors drops below 0.9 V.

As can be seen in fig.3.4.1, the principle of operation of the signal and noise envelope detectors of the receive channel is equal to the one of the transmit channel. However, the gain of the first stage (input to pin RSEN) is 0 dB instead of 40 db for the transmit channel, this is in order to compensate the level on TXIN which is not yet amplified.

The behavior of the envelopes is illustrated in fig.3.4.2 where the signal and noise envelope of one channel are depicted together with the input signal.

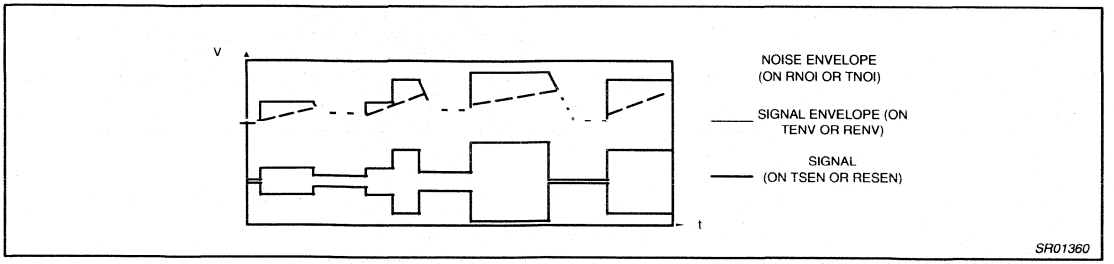


Figure 3.4.2. Typical Behavior of the Signal and Noise Detectors

In fig.3.4.2 it is shown that when the input signal raises quickly, the envelope signal follows immediately and the noise envelope slowly follows the envelope signal. When the input signal decreases, the envelope signal follows immediatly but nevertheless less quickly than when it raises, the noise envelope follows immediatly the decrease of the envelope signal and never crosses it.

3.4.2 Decision logic

The signal and noise envelopes of the transmit and receive signal are used by the decision logic to determine in which mode the TEA1095 has to be.

The output of the logic is a current source which charges or discharges the capacitor Cswt at pin SWT. If the logic determines Tx–mode, the capacitor Cswt is discharged with 10 mA. When Rx–mode is determined, Cswt is charged with 10 mA. When Ix–mode is determined, the current source is zero and the voltage on SWT becomes equal to the voltage on pin IDT via the current provided through the resistor Ridt. The time constants of the duplex controller are therefore determined by the combination of the internal current sources, the capacitor Cswt and the resistor Ridt.

As can be seen in fig.3.4.1, the envelopes are not used directly by the decision logic.

First, to have a clear choice between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference of 13mV. This so called speech/noise threshold is implemented in both the receive and the transmit channel. At the end of paragraph 3.4.4 a way to increase this threshold is discussed.

Second, the signal on TXIN contains both the signal of the local talker as well as the signal coming from the loudspeaker (acoustic coupling). In Rx–mode, the contribution of the loudspeaker overrules the contribution of the local talker. As a result, the signal envelope on TENV is mainly formed by the loudspeaker signal, to correct this, an attenuator is placed between TENV and the TENV/RENV comparator. The attenuation equals the attenuation applied to the microphone amplifier gain. Thus when the TEA1095 is in Rx–mode, the attenuation equals the switching range.

Third, when a dial tone is present on the line, without measures this would be recognized as noise after some delay because its level is constant. As a result, the TEA1095 would go to Ix–mode and the user of the set would hear the dial tone fade away. Therefore, a dial tone detector is incorporated which doesn't consider input signals as noise when they have a level higher than the dial tone level. The dial tone level, represented by Vdt in fig.3.4.1, is adjustable by Rsen.

COMPARATOR TENV/TNOI	1	x	x	0	x
COMPARATOR TENV/RENV	1	0	0	1	0
COMPARATOR RENV/RNOI	x	1	x	x	0
COMPARATOR RNOI/VDT	x	x	1	x	0
OUTPUT CURRENT	−10μA	+10μA	+10μA	0μA	0μA

SR01366

Figure 3.4.3. Truth Table of the Detection Logic

When these three corrections are made, the signal and noise envelopes are used by the comparators and the logic. As already explained, the output of the logic is a current source. The relation between the current source and the output of the comparators is given in the table of fig.3.4.3. If for instance, TENV>RENV (transmit signal larger than receive signal) and TENV>TNOI (transmit signal more than 4.3 dB larger than noise level), then the output current will be −10 mA.

When pin MUTETX is made high, see paragraph 3.2.2, the output current is forced to be +10 mA, which forces the TEA1095 into Rx–mode and mutes the microphone amplifier. When pin MUTERX is made high, see paragraph 3.3.3, the output current is forced to be −10 mA, which forces the TEA1095 into Tx–mode and mutes the receive path. When both MUTETX and MUTERX are made high, both channels are muted.

The voltage on pin SWT is internally limited to IDT–0.4 V and IDT+0.4 V.

3.4.3 Voice switch

With the voltage on pin SWT, the voice switch regulates the gain of the microphone preamplifier and the receive channel preamplifier in such a way that the sum of the transmit and receive gain is kept constant. This is done to keep the loop gain of the handsfree telephone set constant, see also the introduction &1. The switch–over behavior of the voice switch will be described with the help of fig.3.4.4.

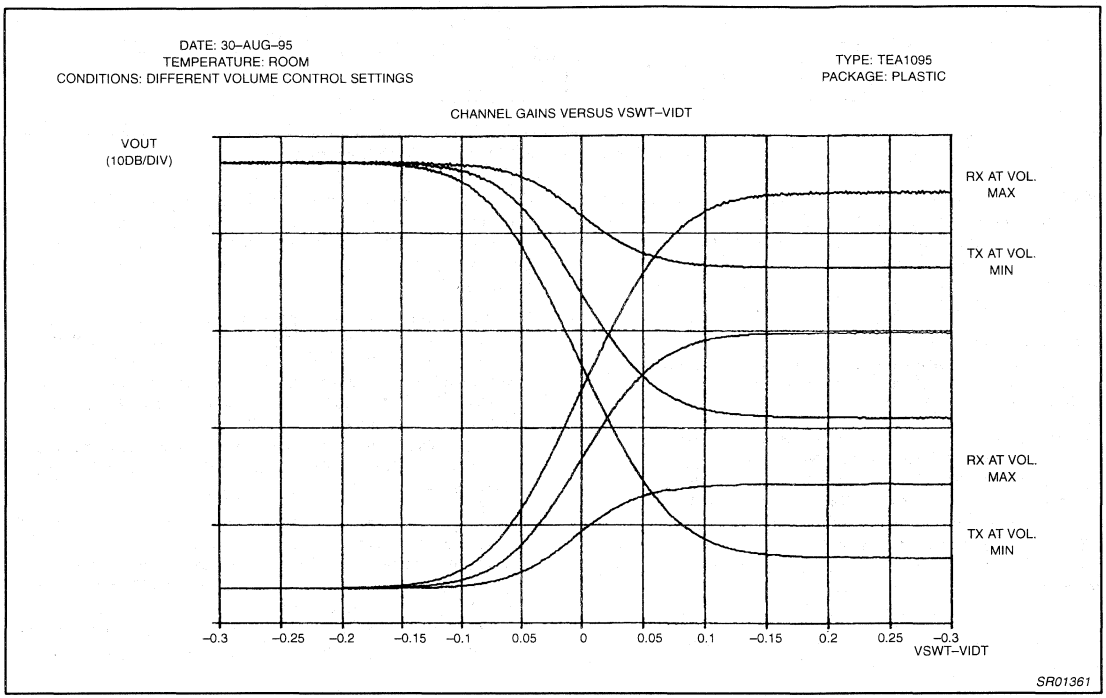


Figure 3.4.4. Behavior of the Voice Switch

When the voltage on SWT is more than 180 mV below the voltage on IDT, the TEA1095 is fully switch to Tx–mode (gain of the transmit path at maximum and gain of the receive path at minimum). When the voltage on SWT is more than 180 mV above the voltage on IDT, the TEA1095 is fully switch to Rx–mode (gain of the receive path at maximum and gain of the transmit path at minimum). The TEA1095 is considered to be in Ix–mode when the voltage on SWT equals the voltage on IDT. When the capacitor Cswt is charged or discharged, the voltage on SWT varies and as a result the voice switch will smoothly switch over between the modes keeping the sum of the transmit and receive gains constant.

The difference between the maximum and the minimum gain of the receive or transmit preamplifiers is called the switching range. This range is determined by the ratio of Rswr and Rstab, see paragraph 3.4.4. Both Rswr and Rstab set internally used reference currents which are proportional to absolute temperature (PTAT).

As already stated in &3.3 the volume control acts upon the receive preamplifier via the control of the voice switch. As a result, the loop gain of the handsfree set is kept constant when the volume of the receive path is adjusted. However, the voice switch is designed such that the volume control has no influence in Tx–mode. In the extreme case, when the volume of the receive channel is reduced with the value of the switching range, the TEA1095 virtually does not switch over. In order to avoid inversion of the gain in Rx–mode, the volume control range of the TEA1095 cannot be larger than the switching range.

3.4.4 Adjustments and performances

The adjustment of the duplex controller has to be performed according to the following recipe:

Determine the switching range

Determine dial tone detector level

Determine sensitivity

Determine timings

Ad 1. Determine switching range

The switching range Asw is determined by the ratio of the two resistors Rswr and Rstab according to:

Asw (dB) = 20 * log (Rswr / Rstab)

The resistor Rstab has to be taken 3.65 k.Ω The value of the resistor Rswr can vary between 3.65 kΩ and 1.5 MΩ resulting in a

switching range between 0 dB and 52 dB. With Rswr of 365 kΩ, the switching range is typically set to 40 dB.

The switching range is calculated out of the loop gain (Aloop). In a handsfree application, the loop gain has to be smaller than one (<0 dB) and can be calculated as follows:

Aloop = Atx1095 + Atx1096 + Ast + Arx1096 + Arx1095 + Als1096 + Aac – Asw.

with Atx1095 = sending gain of the TEA1095 (TXIN to TXOUT)

Atx1096 = sending gain of the TEA1096 (MIC to LN)

Ast = electrical sidetone

Arx1096 = receive gain of the TEA1096 (LN to QR)

Arx1095 = receive path gain of the TEA1095 (RXIN to RXOUT)

Als1096 = loudspeaker amplifier gain of the TEA1096 (LSI to QLS)

Aac = electro–acoustic coupling from loudspeaker to microphone (QLS to TXIN)

Asw = switching range

In this calculation, the worst case has to be taken for Ast and Aac. Furthermore, for safety, it is advised to choose Asw large enough to compensate spreads (margin from 10 to 15 dB).

The electrical sidetone is the difference (in dB) between the wanted receive signal on the TEA1096 and the unwanted part of the transmit signal received while having an equal signal level on pin LN for both the transmit and the receive signal. Ast is dependent of frequency and connecting conditions of the set (line lenght, line impedance).

The acoustic coupling is dependent on the environment of the telephone set, for the determination of Aac, the worst condition has to be searched.

If a certain minimum volume control range is required, the switching range must not be chosen smaller.

In appendix A, a method for measuring the required switching range, based on the above calculation, is given.

It is also possible to determine the switching range by experiments:

As for the calculation, it is necessary to identify what are the worst conditions for sidetone and acoustic coupling. In these worst conditions, Rswr can be adjusted in such a way that the handsfree telephone set is at the limit of howling. Then the determined value of Rswr must be increased in order to have a margin of 10 dB to 15 dB.

Handsfree behavior will be more comfortable for the user if the switching range is not too large. So, **it is advised to take care of the acoustic coupling between the loudspeaker and the microphone** which might come from the cabinet of the terminal itself.

Ad 2. Determine dial tone detector level

The dial tone detector level is determined by the value of Rrsen according to:

Vdialtone = 4.2 mA * Rrsen

With Rrsen of 10 k, the dial tone detector level will be 42 mVrms. This means, a continuous signal on the input RXIN larger than 42 mVrms will be recognized as a dial tone.

Ad 3. Determine sensitivity

The sensitivity is set by Rrsen and Rtsen. The resistor Rrsen is already determined by the dial tone detector level. It must however be checked if the choosen value for Rrsen is a practical one for the dynamic range of the logarithmic compressor. The optimized range for the compression is when the current flowing through pin RSEN is between 0.8 to 160 mArms. This means that at nominal receiving signal the current through RSEN is preferably around 11 mArms. This gives a maximum dynamic range of plus and minus 23 dB.

The same counts for pin TSEN.

The resistor Rtsen has to be chosen in such a way that both channels have the same priority for the duplex controller. This can be obtained by choosing Rtsen according to:

20 * log (Rtsen) = 20 * log (Rrsen) – Atx1095 – Atx1096 – Ast – Arx1096 + Atsen + 1/2 Aloop

with Atsen = internal gain from TXIN to TSEN = 40 dB.

In this relation, the maximum loop gain and the worst case sidetone are used. If it is prefered to give the transmit channel priority above the receive channel, the value of Rtsen has to be chosen smaller. For the opposite, the value of Rtsen has to be chosen larger. With respect to the calculated setting, Rtsen and Rrsen can be varied with plus and minus 1/2 * Aloop (in dB).

In appendix A, a method for determining the required Rtsen, based on the above calculation, is given.

The capacitors Ctsen and Crsen form first order high–pass filters respectively with Rtsen and Rrsen to reduce influence of low frequencies on the switching behavior. It is suggested to choose the capacitors Ctsen and Crsen such that the cut–off frequencies of the filters are similar.

When the calculated sensitivity setting is implemented, subjective tests with real telephone lines will be necessary to come to the optimal sensitivity setting.

Once Rrsen is determined, it would also be possible to determine Rtsen only by experiments. In this case, subjective tests with different line conditions (attenuation, impedance, length) have to be carried–out until the optimal sensitivity setting is found.

Ad 4. Determine timings

The timings which can be set are : signal envelope timing and noise envelope timing for both channels, switch–over timing and idling timing.

The signal envelope timing is set by the capacitors Ctenv and Crenv. Because of the logarithmic compression between TSEN and TENV respectively RSEN and RENV, the timing can be expressed in dB/ms. At room temperature, the following relation counts :

Timing I / (3 * C) (in dB/ms)

With I = charge or discharge current from pin TENV, RENV, TNOI, RNOI

C = timing capacitor Ctenv, Crenv, Ctnoi, Crnoi

With the advisable signal envelope timing capacitors Ctenv and Crenv of 470 nF, the maximum attack–timing of the signal envelopes will be around 85 dB/ms (I=120 mA). This is enough to track normal speech. The release timing will be 0.7 dB/ms (I=1 mA). This is

enough to smoothen the signal envelope and to eliminate the influence of room echoes on the switching behavior.

With the advisable noise envelope timing capacitors Ctnoi and Crnoi of 4.7 mF, the attack timing of the noise envelopes will be 0.07 dB/ms (I=1 mA). This is small enough to track background noise and not to be influenced by speech bursts. The maximum release timing will be 8.5 dB/ms (I=120 mA). This is enough to track the signal envelope during release because the signal envelope release timing is 0.7 dB/ms which is a factor smaller. It is advised to choose the signal envelope timing and the noise envelope timing of both channels equal for optimum operation of the duplex controller.

The switch–over timing is determined by the value of the switch–over capacitor Cswt. The idling timing is determined by the combination of Cswt and the idling resistor Ridt.

The output current of pin SWT is Iswt, a voltage difference over Cswt can be obtained according to :

Vswt/t = Iswt / Cswt (mV/ms).

With the advised value of 220 nF for Cswt, the obtained voltage difference is 45 mV/ms. The switch–over time is dependent on the voltage difference which has to be generated on pin SWT. Suppose the set is in full Tx–mode, then the voltage on SWT will be V(IDT)–400 mV, see fig.3.4.4. To reach Rx–mode a voltage difference of 580 mV must be generated to end up a voltage of V(IDT)+180 mV. So in this case the switch–over time will be 13 ms. When the set is in Ix–mode, the voltage on SWT equals the voltage on IDT, in that case switching to Tx–mode or to Rx–mode requires a voltage generation of only 180 mV and they will be reached in 4ms.

The idling timing is determined by an RC time constant. It is supposed that Ix–mode is reached when a time (tidt) is elapsed:

tidt = 4 * Ridt * Cswt

With the advised value for Ridt of 2.2 M, an idling time of around 2 seconds is obtained. To have a clearly determined idling timing, it is advised not to use a capacitor with a high leakage current.

When the calculated timing settings are implemented, subjective tests with real telephone lines will be necessary to be sure that the optimal timings have been set.

4. APPLICATION COOKBOOK

In this chapter, the procedure for making a basic application with a speech and listening–in IC TEA1096 and the handsfree duplex controller TEA1095 will be given. With the help of Fig. C1 in appendix, the design flow is given as a number of steps which should be made. As far a as possible for every step, the components involved and their influence on every step are given. The preferred values are given between brackets.

The application of fig. C1 is a basic application of the TEA1095 voice switched speakerphone IC with the TEA1095 speech and listening–in circuit.

As can be seen in fig. C1, only a few components have a fixed value. All other values will follow from the cookbook of fig. 4.1.

DC setting :

Adjust the DC setting of the TEA1096 to the local PTT requirements.

Voltage LN–VEE	Refer to 4 and/or to 12 (N5 : ETT94001)
DC slope	
Supply point VCC	
Supply point VBB	
Artificial inductor	
Impedance and sidetone :	

After setting the required set impedance, the sidetone has to be optimized using the two sidetone netwoks in order to minimize the loop gain in all line conditions. AGC can be adjusted at that step.

Set active impedance	Refer to 4 and/or to 12 (N° : ETT94001)
Sidetone	
AGC	

TEA1096 transmit and receive gains

Transmit gain	Total transmit and receive gains have to be siplitted between TEA1096 and TEA1095. It is suggested to leave 15dB of transmit gain for the TEA1095 and to adjust the receive gain between LN and QRP at –3 dB.
	Ctxo and MICP input impedance form a high–pass filter.
Receive gain	A capacitor in parallel with the transmit gain resistor (between TEA1096 pins 17 and 11) form a low–pass filter.
	A resistor bridge can be inserted between TXOUT of TEA1095 and MICP of TEA1096.
	A capacitor in parallel with the receive gain resistor (between TEA1096 pins 26 and 25) form a low–pass filter.
	For more details, refer to 4 and/or to 12 (N5 : ETT94001)

TEA1095 microphone amplifier (see & 3.2):

After the sensitivity and the curve of the microphone are adjusted, the gain can be adjusted to the desired value

Step	Adjustment
Microphone sensitivity	Rmic sets the sensitivity. Together with Rmf, Rmic provides the polarisation of the electret.
Frequency curve	Cmic with Rmic and the output impedance of the electret form a low–pass filter. Ctxin with the 20 k input impedance at TXIN form a high–pass filter.
Transmit gain and stability	Rgatx sets the microphone amplifier gain : Atx=20*log(0.72*Rgatx/Rstab) Cgatx may be necessary for stability and forms a low–pass filter with Rgatx.

TEA1096 loudspeaker amplifier :

The gain is fixed at 35.5 dB , a high–pass filter can be made, the dynamic limiter timing can be chosen.

Frequency curve	Crxo and/or capacitor in series with loudspeaker can form high–pass filters
Dynamic limiter timing	Capacitor at pin DLL.

TEA1095 receive channel (see & 3.3) :

The gain of the receive pass and the curve can be adjusted. The volume control range can be chosen.

Receive gain	Rgarx : the total receive gain of the set is equal to receive gain of the TEA1096 (–3 dB ?), the gain of the loudspeaker amplifier (35.5 dB) and the gain set with Rgarx.
Receive curve	Crxi with the input impedance of 20 k at pin RXI form a high–pass filter (a cut–off frequency between 100 and 200 Hz is advised),
Volume control	Cgarx in parallel with Rgarx forms a low–pass filter. A linear potentiometer of 10 k is suggested (3 dB for each 950).

TEA1095 Duplex controller (see & 3.4) :

When all gains are adjusted, the switching range can be determined. Then the dial tone detector level followed by the sensitivities can be set. Finally the timings of the envelopes and the switching are adjusted.

Switching range	Loop gain : Aloop=Atx1095+Atx1096+Ast+Arx1096+Arx1095+Als1096+Aac–Asw < 0dB Choose Asw with safety margin
Dial tone detector	Adjust Rswr : Asw=20log(Rswr/Rstab) with Rstab fixed at 3.65k
Sensitivities	Rrsen : Vdialtone=4.2 mA*Rsen Rtsen for balanced sensitivities between Tx and Rx
Signal envelopes	Ctsen form a high–pass filter with Rtsen Crsen form a high–pass filter with Rrsen
Noise envelopes	Ctenv (0.47 mF), Crenv (0.47 mF) :
Switch–over timing	maximum attack : 120 m/(3*Cenv) (dB/ms), release : 1 m/(3*Cenv) (dB/ms)
Ix–mode timing	Ctnoi (4.7 mF), Crnoi (4.7 mF) : attack : 1 m/(3*Ctnoi) (dB/ms), maximum release : 120 m/(3*Ctnoi) (dB/ms)
	Cswt (220 nF) : Vswt/t=10m/Cswt (mV/ms)
	Ridt (2.2 M) : time constant=4*Ridt*Cswt

Fig. 4.1 Steps in the design flow of the TEA1095 with TEA1096

5. APPLICATION EXAMPLE

In this chapter, a basic application example of the TEA1095 with the TEA1096 is depicted. Only the essential elements are given, for instance no bridge, no protection, no ringer, no line interruptor are included.

Fig. C2 gives the basic handsfree application of the TEA1095 together with the speech and listening–in circuit TEA1096. This application doesn't include handset telephony (which would have to be added by means of analog switches) but only basic handsfree telephony.

– **DC setting** : nominal DC characteristic and nominal V BB of 3.6 V are chosen.

– Impedance and sidetone : the impedance is a complex one (220 , 825 //115 nF). A standard 600 impedance would save six components.

– TEA1096 transmit and receive gains : the transmit gain of TEA1096 is set at 30.5dB by means of a resistor bridge (22 k, 7.5 k at microphone input combined with an internal gain of 43 dB set by 32.5 k). The cut–off frequency of the high–pass filter is set at 110 Hz by 2*100 nF in series, the cut–off frequency of the low–pass filter is set at 7.2 kHz by 680 pF//32.5 k.

The receive gain of TEA1096 is set at –3 dB by 82.5 k. The cut–off frequency of the low–pass filter is set at 4.1 kHz by 470 pF//82.5 k.

–**TEA1095 microphone amplifier** : the sensitivity of the electret microphone is set by Rmic=1.5 k. The microphone power supply is filtered by Rmf, Cmf with a cut–off frequency of 16Hz. An electrical low–pass filter is provided with Cmic, in combination with the effect of the cabinet and the self curve of the electret, it adjusts the high frequency part of the transmit curve. A high–pass filter is formed with Ctxin and the 20 k input impedance at TXIN, its cut–off frequency is set at 530 Hz (a higher cut–off frequency may be necessary to better minimize the room echo and/or to better compensate the line attenuation).

The gain of the microphone channel is set at 15.5 dB by Rgatx=30.1 k, a low–pass filter with Cgatx=2.2 nF would provide a cut–off frequency of 2.4 kHz.

– Loudspeaker amplifier : nominal loudspeaker amplifier application is made (gain of 35.5 dB).

– TEA1095 receive channel : the gain of the receive path of the TEA1095 is set at –7 dB by Rgarx=3.65 k (the total receive gain of the set is : 35.5 – 3 – 7 = 25.5 dB). A high–pass filter with a cut–off frequency of 120 Hz is formed by Crxin=68nF and the input impedance of 20 k at RXIN. A low–pass filter with Cgarx=15 nF would provide a cut–off frequency of 2.9 kHz for the adjustment of the loudspeaker curve.

A 10k linear potentiometer provides a volume control range of about 31dB.

– Duplex controller : after optimized acoustic adaptation (reduction of acoustic coupling between loudspeaker and microphone and good sidetone adaptation) the switching range is set at 40dB by Rswr=365k, including safety margin.

With Rrsen=10 k, the dial tone detector level is set at 42 mV which means 60 mVrms on line.

With Crsen=100 nF, the cut–off frequency of the high–pass filter is 160 Hz.

Rtsen and Ctsen respectively equal Rrsen and Crsen in order to balance transmit and receive sensitivities.

With Ctenv and Crenv=0.47 mF, the max. attack time of the signal envelopes is set at 85 dB/ms.

With Ctnoi and Crnoi=4.7 mF, the max. attack time of the noise envelopes is set at 0.07 dB/ms.

The switch–over timing is nominally set by Cswt=220 nF and the idling timing by Ridt=2.2 M.

Due to its large flexibility (range of adjustments and architecture), the TEA1095 can be implemented in a lot of environments, offering handsfree function with various speech interfaces and loudspeaker amplifiers, with or without external supply.

6. ELECTROMAGNETIC COMPATIBILITY

As no common international specification exists for RFI immunity, and as different assembly methods may lead to different solutions, only some advices can be provided.

It is advisable to take care of the impedance of the GND, the smallest is always the best. Even if it is required to separate low level microphone signals on GNDTX from high level signals (loudspeaker or others), GND and GNDTX traces must be as wide as possible.

Also, the connection of Rstab, Rswr, Rgatx and Rgarx has to be done with very short traces (specially STAB input which sets all the gains must be very immune).

VOL and TXI inputs may also be sensitive (RF signals entering these pins would be amplified). Rvol can be connected with short traces if possible or VOL input may be lightly decoupled by a capacitor to GND. Care has to be taken with the lay–out of the microphone amplifier, which is also helpfull for the noise, providing a good decoupling to GNDTX. A low–pass RC filter may be added at the input of the amplifier.

It is not allowed to put a capacitor directly between STAB and GND, only an RC network can be implemented if it helps (365 , 4.7 nF).

RXIN input may also be decoupled to GND.

A low impedance capacitor in parallel with the electrolythic one between VBB and GND may help.

7. REFERENCES

TEA1095 Voice Switched Speakerphone IC

Device specification

Philips Semiconductors

SEMICONDUCTORS FOR TELECOM SYSTEMS – IC03 –

3 TEA1094 Handsfree IC

Device specification

TEA1096 / TEA1096A Line interface and Listening–in ICs

Device specification

5 TEA1081 Supply circuit with power–down for telephone set peripherals

Device specification

6 TEA1083 / TEA1083A Call progress monitor for line–powered telephone set

Device specification

TEA1085 / TEA1085A Listening–in circuit for line–powered telephone set

Device specification

TEA1112 / TEA1112A / TEA1113 Low voltage versatile telephone transmission circuits with dialler interface

Device specifications

9 TEA1062 / TEA1062A Low voltage versatile telephone transmission circuits with dialler interface

Device specification

10 TEA1064A / TEA1064B Low voltage versatile telephone transmission circuits with dialler interface and level dynamic limiting

Device specification

Application of the TEA1094 handsfree circuit (ETT/AN94004)

Application of the TEA1096 transmission and listening–in circuit (ETT94001)

Measures to meet EMC requirements for TEA1060–family speech transmission circuits (ETT89016)

Application of the speech transmission circuit TEA1062 (ETT89008)

Application of the versatile speech/transmission circuit TEA1064 in full electronic telephone sets (ETT89009)

Philips Semiconductors

Wirebound telecom

APPLICATIONS HANDBOOK

APPENDIX A MEASUREMENT SETUP

This appendix describes how the loop gain and the sensitivity setting can be measured. These measurements provide a base for obtaining of the final values which, however, can only be reached by performing subjective tests.

For determining the loop gain, the worst case for both acoustical coupling and sidetone must be considered. This can be done with the measurement setup of fig. A.1.

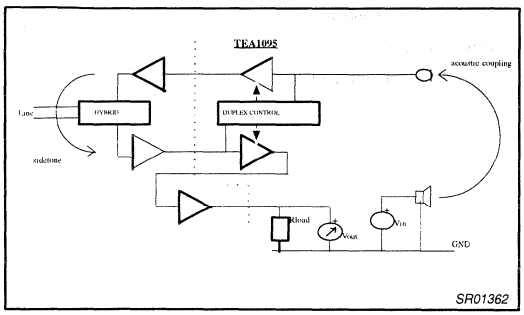


Figure A.1. Setup for Loop

The loudspeaker is disconnected from the set and an electrical signal is applied to it. The acoustical signal coming from the loudspeaker is coupled to the microphone (Aac), transmitted to the line (Atx1095 + Atx1096), returns via sidetone (Ast) and is amplified again to the loudspeaker output of the TEA1096 (Arx1096 + Arx1095 + Als1096). The output is loaded with a loudspeaker equivalent impedance (Rload), it has to be checked that the TEA1096 loudspeaker amplifier is not saturated and that its gain is not reduced by the dynamic limiter. The total gain of this loop is reduced with the switching range (Asw).

The gain from the loudspeaker connection (Vin) to the loudspeaker amplifier output (Vout) is the loop gain (Aloop), given as:

20 * log (Vout / Vin) = Aloop

Aloop = Aac + Atx1095 + Atx1096 + Ast + Arx1096 + Arx1095 + Als1096 – Asw

This measurement has to be carried–out with a Vin level avoiding saturation of the loudspeaker amplifier (start with 100 mVrms) in the frequency range 200 Hz to 5000 Hz (100 to10000 Hz for high quality aparatus).

From the curve obtained, the maximum gain (<0 dB) indicates the gain margin.

Sidetone curve changes with line impedance, so, the Aloop curve will change in the same way. It is advisable to double–check with different line conditions (impedance and length) that the identified worst line condition is really the worst all over the frequency range.

Moving around the set also modifies acoustic coupling, so, it is advised to proceed as for sidetone.

The measurement combining both worst case conditions of sidetone and acoustical coupling gives the worst case loop gain and thus the gain margin.

All transmit and receive gains and curves are supposed to be set, the value of the switching range however, can only be finalized after the measurement. Therefore, during the measurement, the switching range must be set to a preliminary value. An advised preliminary value for measurement is 40 dB.

When the correct switching range is set, the sensitivity settings can be determined.

Rrsen is determined to get the correct tone detector level.

For determining the sensitivity, calculations can be done as described in &3.4.4. It is also possible measuring the correct sensitivity setting with measurement setup of fig. A. 2.

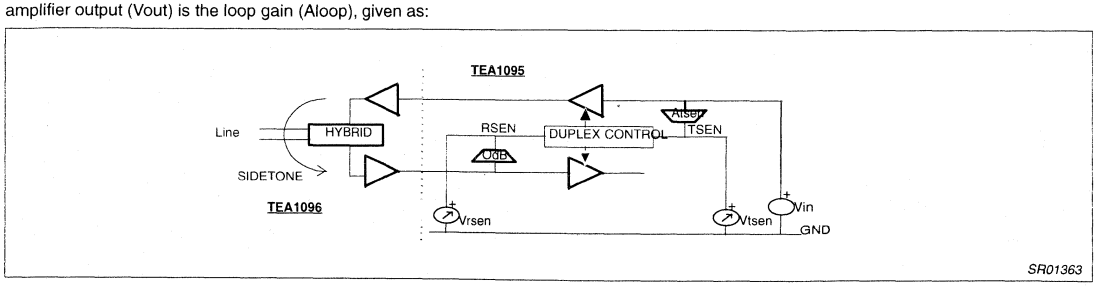


Figure A.2. Simplified Measurement Setup for Determining Sensitivity

Both the loudspeaker and microphone are disconnected from the set. An input signal (Vin) of 1 mVrms is applied to the microphone input. This signal is amplified to pin TSEN (Atsen), it is also transmitted to the line, returns via sidetone, is amplified by the TEA1096 to the TEA1095 pin RXIN and buffered to pin RSEN. The ratio of the signal on pin TSEN (Vtsen) and RSEN (Vrsen) is given as :

20 * log (Vtsen/Vrsen) = Atsen – Atx1095 – Atx1096 – Ast – Arx1096

This measurement has to be done in nominal line and environment conditions in the frequency range 300 Hz to 3400 Hz. The TEA1095 must be forced in Tx–mode by making pin MUTERX high, the receive channel is muted but Vrsen is not affected.

Out of the measured ratio of Vtsen and Vrsen it follows :

20 * log (Rtsen / Rrsen) = 20 * log (Vtsen / Vrsen) + Aloop / 2
(see &3.4.4, Ad.3)

Both the ratio of Vtsen and Vrsen and Aloop are frequency dependent, so the optimal value of Rtsen would be frequency dependent. However, this can be simplified by using the lowest value of 20*log(Vtsen/Vrsen) and the highest value of Aloop to obtain the correct Rtsen.

The value of Rtsen found is a starting point for obtaining the final value which can only be reached by subjective tests with real telephone conditions.

APPENDIX B LIST OF ABBREVIATIONS AND DEFINITIONS

Aac	Electro–acoustic coupling (electrically measured)
AGC	Automatic line loss compensation of the TEA1096
Aloop	Loop gain of a handsfree telephone set
Als1096	TEA1096 loudspeaker amplifier gain
Arx1095	Gain of the receive path of TEA1095
Arx1096	Receive gain of TEA1096
Ast	Sidetone gain
Asw	Switching range
Atsen	Gain from TXIN to TSEN of 40dB
Atx1095	Gain of the transmit path of TEA1095
Atx1096	Transmit gain of the TEA1096
Cgarx	Capacitor setting receive path amplifier low–pass filter
Cgatx	Capacitor setting microphone amplifier low–pass filter
Cmf	Microphone supply filter capacitor
Cmic	Microphone low–pass filter capacitor
Crenv	Capacitor determining the receive signal envelope
Crnoi	Capacitor determining the receive noise envelope
Crsen	DC blocking capacitor of receive sensitivity setting
Crxi	Receive input capacitor
Crxo	Receive output capacitor
Cswt	Switch–over timing capacitor
Ctenv	Capacitor determining the transmit signal envelope
Ctnoi	Capacitor determining the transmit noise envelope
Ctsen	DC blocking capacitor of transmit sensitivity setting
Ctxin	Microphone amplifier input capacitor
Ctxo	Transmit output capacitor
dBmp	dBm psophometrically weighted (0dBmp=1mW)
Vswt	Voltage difference on SWT
GARX	Receive gain adjustment pin
GATX	Transmit gain adjustment pin
GND	Ground reference pin
GNDTX	Ground reference pin for microphone signals
IDT	Idle–mode timing adjustment pin
Iswt	Output current through pin SWT (from logic)
Ix–mode	Idle mode
LN	Positive line terminal of TEA1096 or TEA106x
LSI	Loudspeaker amplifier input of TEA1096
MICP,MICM	Microphone input of TEA1096
MOSFET	Meta Oxide Field Effect Transistor
MUTERX	Receive channel mute
MUTETX	Transmit channel mute
NC	not connected
PD	Power–down input pin (reduced power consumption)
PTAT	Proportional to absolute temperature
PTT	Public telephone company
QRP	Earphone amplifier output of TEA1096
RENV	Receive signal envelope timing adjustment pin
RFI	Radio frequency interference
Rgarx	Resistor setting receive path amplifier gain
Rgatx	Resistor setting transmit path amplifier gain
Ridt	Resistor setting Ix–mode timing
Rload	Loudspeaker equivalent load resistor
Rmf	Microphone supply filter resistor
Rmic	Resistor setting microphone sensitivity
RNOI	Receive noise envelope timing adjustment pin
Rrsen	Resistor setting sensitivity of the receive envelopes
RSEN	Receive signal envelope sensitivity adjustment pin
Rslpe	Resistor setting slope of the DC characteristic of TEA1096
Rstab	Resistor setting an internally used PTAT current
Rswr	Resistor setting switching range

Rtnoi	Resistor increasing microphone speech/noise threshold
Rtsen	Resistor setting sensitivity of the transmit envelopes
Rvol	Volume control potentiometer
RXIN	Receive path input
RXOUT	Receive path output
Rx–mode	Receive mode
SLPE	DC slope pin of TEA1096 or TEA106x
STAB	Reference current pin
SWR	Switching range adjustment pin
SWT	Switch–over timing adjustment pin
TENV	Transmit signal envelope timing adjustment pin
Tidt	Idle mode timing
TNOI	Transmit noise envelope timing adjustment pin
TSEN	Transmit signal envelope sensitivity adjustment pin
TXIN	Microphone amplifier input
TXOUT	Transmit path output
Tx–mode	Transmit mode
VBB	Positive supply input of TEA1095
Vdt, Vdialtone	Dial tone detector level
VEE	Reference pin on TEA1096
VOL	Volume adjustment pin

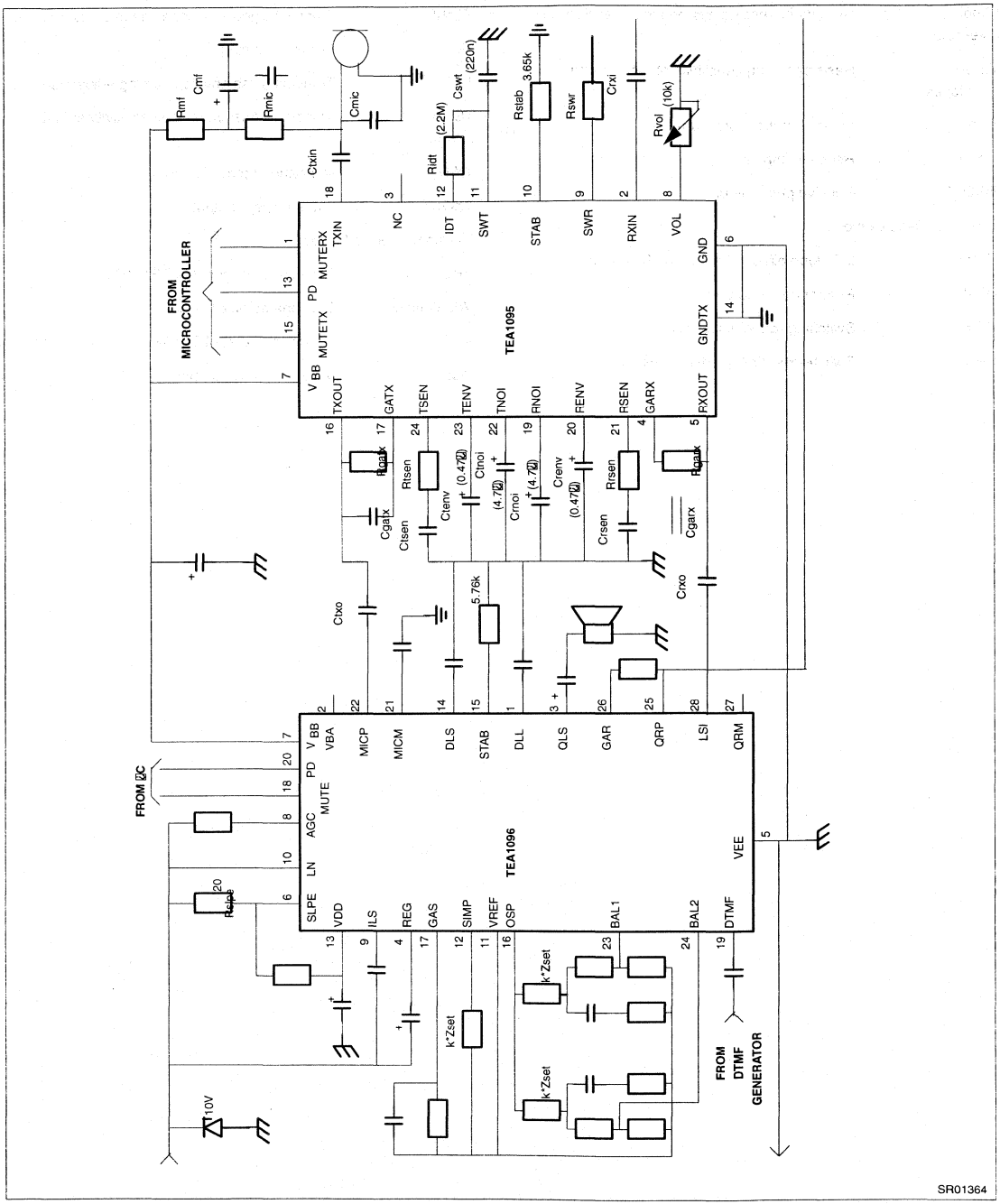


Figure C1. Basic Application of TEA1095 With TEA1096

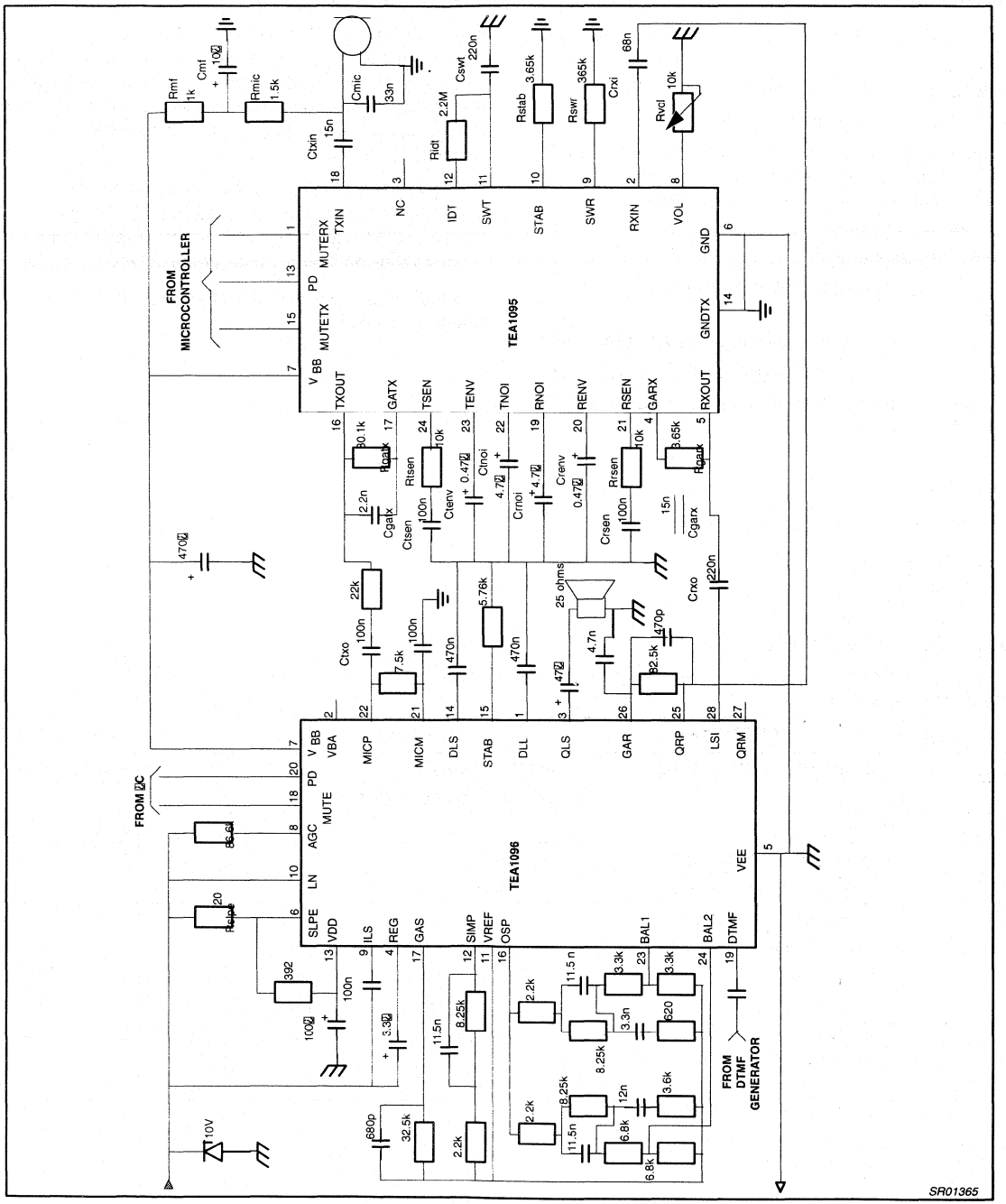


Figure C2. Basic Application of TEA1095 With TEA1096

Versatile cordless transmisssion circuit TEA1118; TEA1118A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- Provides a supply for external circuits
- Symmetrical high impedance transmit inputs (62.5 kΩ) with large signals handling capabilities [up to 1 V (RMS value) with less than 2% THD]
- Receive amplifier for dynamic, magnetic or piezoelectric earpieces
- AGC line loss compensation for transmit and earpiece amplifiers
- DTMF input with confidence tone (TEA1118A only)
- MUTE input for pulse or DTMF dialling (TEA1118A only)
- Transmit mute function, also enabling the DTMF input (TEA1118A only).

GENERAL DESCRIPTION

The TEA1118 and TEA1118A are bipolar integrated circuits that perform all speech and line interface functions required in cordless telephone base stations. The ICs operate at a line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

The TEA1118A offers in addition to the TEA1118 electronic switching between speech and dialling. Moreover the transmit amplifier can be disabled during speech condition by means of a transmit mute function.

All statements and values refer to all versions unless otherwise specified.

APPLICATIONS

- Cordless telephone base stations
- Fax machines
- Answering machines.

QUICK REFERENCE DATA

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
V_{LN}	DC line voltage		3.35	3.65	3.95	V
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_P = 0 mA	–	2.9	–	V
G_{vtrx}	typical voltage gain range					
	transmit amplifier (TEA1118A only)	V_{TX} = 200 mV (RMS)	–	–	11.3	dB
	transmit amplifier (TEA1118 only)	V_{TX} = 200 mV (RMS)	5.3	–	11.3	dB
	receive amplifier	V_{IR} = 4 mV (RMS)	19	–	31	dB
ΔG_{vtrx}	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 75 mA	–	5.8	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1118M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TEA1118T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TEA1118AM	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TEA1118AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

BLOCK DIAGRAMS

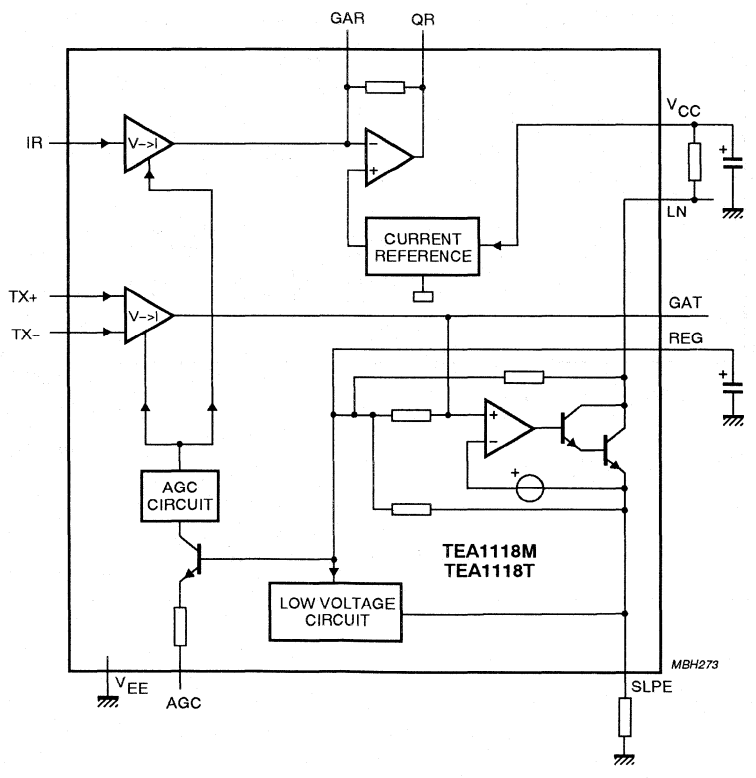


Fig.1 Block diagram (TEA1118).

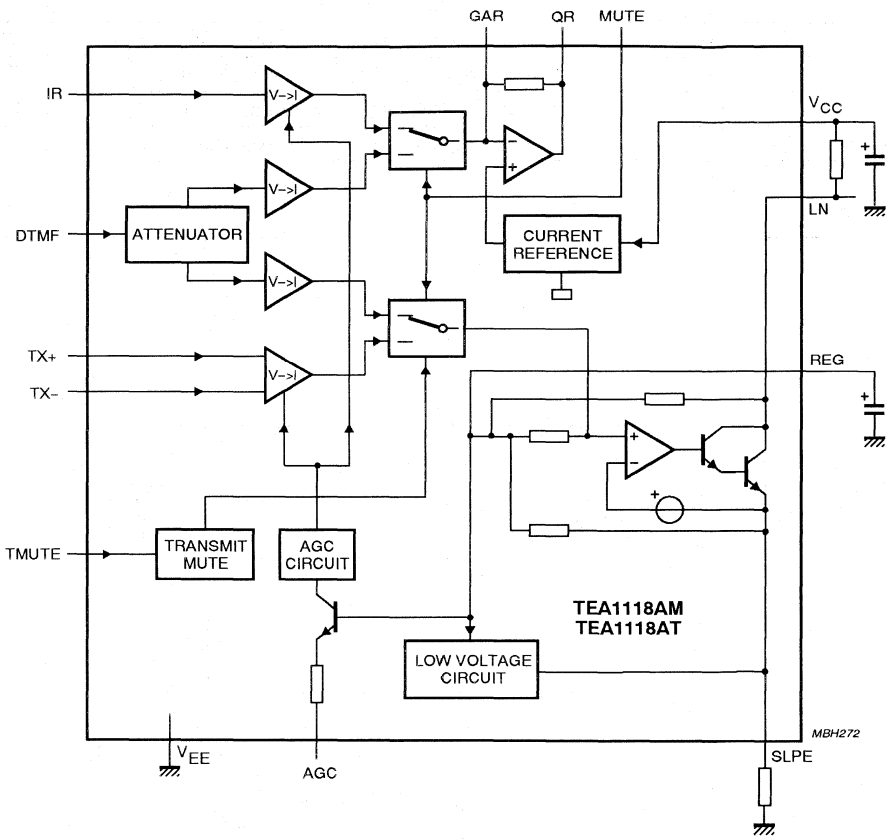


Fig.2 Block diagram (TEA1118A).

PINNING

SYMBOL	TEA1118		TEA1118A		DESCRIPTION
	SO14	SSOP16	SO14	SSOP16	
LN	1	1	1	1	positive line terminal
SLPE	2	2	2	2	slope (DC resistance) adjustment
REG	3	3	3	3	line voltage regulator decoupling
GAT	4	4	–	–	transmit gain adjustment
TMUTE	–	–	4	5	transmit mute input
DTMF	–	–	5	6	dual-tone multi-frequency input
MUTE	–	–	6	8	mute input to select speech or dialling mode
IR	7	9	7	9	receive amplifier input
AGC	8	10	8	10	automatic gain control/line loss compensation
TX–	9	11	9	11	inverting transmit amplifier input
TX+	10	12	10	12	non-inverting transmit amplifier input
V_{EE}	11	13	11	13	negative line terminal
QR	12	14	12	14	receive amplifier output
GAR	13	15	13	15	receive gain adjustment
V_{CC}	14	16	14	16	supply voltage for speech circuit and peripherals
n.c.	5 and 6	5 to 8	–	4 and 7	not connected

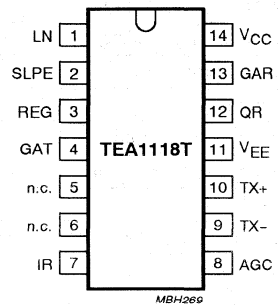


Fig.3 Pin configuration (TEA1118T).

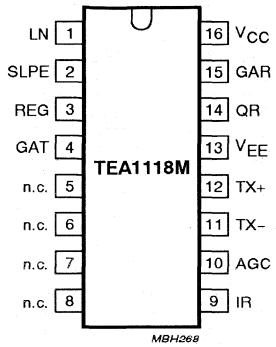


Fig.4 Pin configuration (TEA1118M).

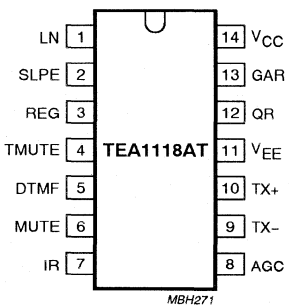


Fig.5 Pin configuration (TEA1118AT).

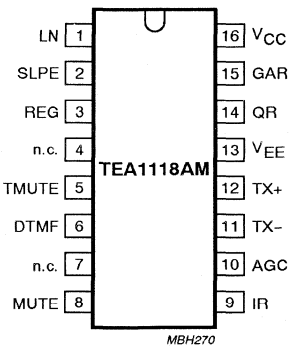


Fig.6 Pin configuration (TEA1118AM).

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supplies (pins LN, SLPE, V_{CC} and REG)

The supply for the TEA1118 and TEA1118A and their peripherals is obtained from the telephone line.

The ICs generate a stabilized reference voltage (V_{ref}) between pins LN and SLPE. This reference voltage is equal to 3.35 V, is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). It can be increased by connecting the R_{VA} resistor between pins REG and SLPE (see Fig.11), or decreased by connecting the R_{VA} resistor between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor (C_{REG}) which is connected to V_{EE}. This capacitor, converted into an equivalent inductance (see Section "Set impedance"), realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current. Figure 7 illustrates the supply configuration.

The ICs regulate the line voltage at pin LN, and it can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_P - I^* = I_{sh}$$

where:

I_{line}: line current

I_{CC}: current consumption of the IC

I_P: supply current for peripheral circuits

I^*: current consumed between LN and V_{EE}

I_{sh}: the excess line current shunted to SLPE (and V_{EE}) via LN.

The preferred value for R_{SLPE} is 20 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the transmit gain and the DTMF gain (TEA1118A only), the gain control characteristics, the sidetone level and the maximum output swing on the line.

The internal circuitry of the TEA1118 and TEA1118A is supplied from pin V_{CC}. This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC}. It may also be used to supply peripheral circuits such as dialling or control circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as shown by the formula (see also Figs 8 and 9). R_{CCint} is the internal equivalent resistance of the voltage supply point, and I_{rec} is the current consumed by the output stage of the earpiece amplifier.

$$V_{CC} = V_{CC0} - R_{CCint} \times (I_P - I_{rec})$$

$$V_{CC0} = V_{LN} - R_{CC} \times I_{CC}$$

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 7.5 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At currents below 7.5 mA, the circuit has limited transmit and receive levels. This is called the low voltage area.

Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuits is illustrated in Fig.10.

Transmit amplifier (pins TX+, TX– and GAT)

The TEA1118 and TEA1118A have symmetrical transmit inputs. The input impedance between pins TX+ and TX– is equal to 62.5 kΩ; the input impedance between pins TX+/TX– and V_{EE} is equal 36.5 kΩ. The voltage gain from pins TX+/TX– to pin LN is set at 11.3 dB.

Automatic gain control is provided on this amplifier for line loss compensation.

The gain of the TEA1118 can be decreased by connecting an external resistor R_{GAT} between pins GAT and REG. The adjustment range is equal to 6 dB. A capacitor C_{GAT} connected between pins GAT and REG can be used to provide a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAT} \times (R_{GATint} // R_{GAT})$. R_{GATint} is the internal resistor which sets the gain with a typical value of 27 kΩ.

Transmit mute (pin TMUTE; TEA1118A only)

The transmit amplifier can be disabled by activating the transmit mute function. When TMUTE is LOW, the normal speech mode is entered, depending on the level on MUTE. When TMUTE is HIGH, the transmit amplifier inputs are disabled while the DTMF input is enabled (no confidence tone is provided). The voltage gain between LN and TX+/TX– is attenuated; the gain reduction is 80 dB.

Receive amplifier (pins IR, GAR and QR)

The receive amplifier has one input (IR) and one output (QR). The input impedance between pins IR and V_{EE} is 20 kΩ. The voltage gain from pin IR to pin QR is set at 31 dB. The gain can be decreased by connecting an external resistor R_{GAR} between pins GAR and QR; the adjustment range is 12 dB. Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability.

The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times (R_{GARint} // R_{GAR})$. R_{GARint} is the internal resistor which sets the gain with a typical value of 100 kΩ. The condition $C_{GARS} = 10 \times C_{GAR}$ must be fulfilled to ensure stability.

Automatic gain control is provided on this amplifier for line loss compensation.

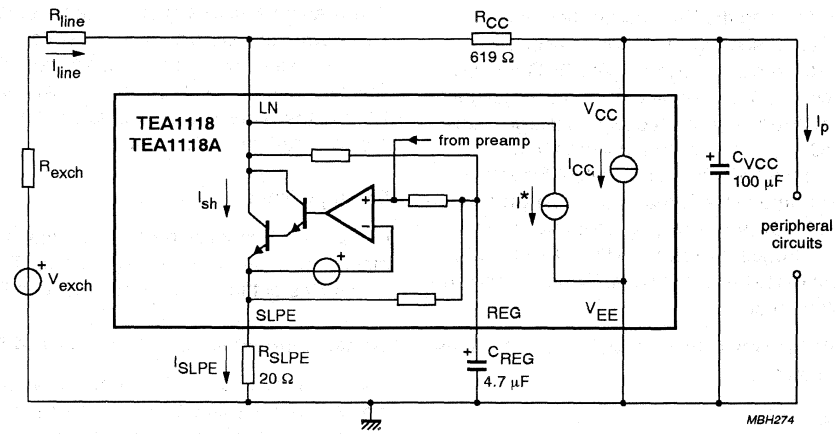
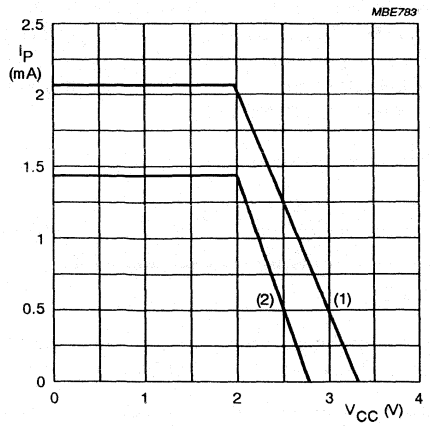


Fig.7 Supply configuration.



(1) With R_{VA} resistor.
(2) Without R_{VA} resistor.

Fig.8 Typical current I_P available from V_{CC} for peripheral circuits at I_{line} = 15 mA.

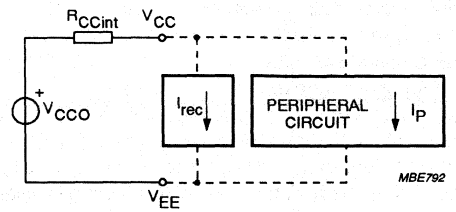
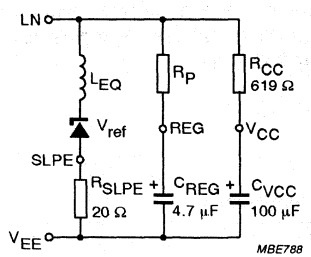
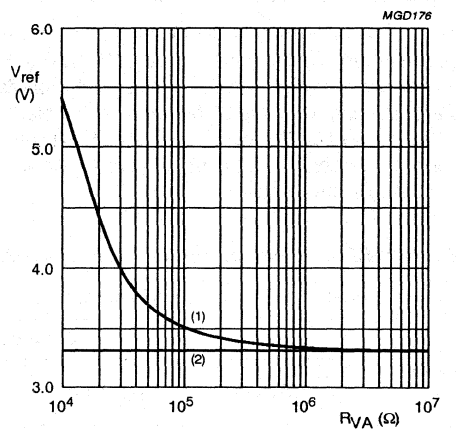


Fig.9 V_{CC} voltage supply for peripheral.



$L_{EQ} = C_{REG} \times R_{SLPE} \times R_P$.
R_P = internal resistance (15.5 kΩ).

Fig.10 Equivalent impedance between LN and V_{EE}.



(1) influence of R_{VA} on V_{ref}.
(2) V_{ref} without influence of R_{VA}.

Fig.11 Reference voltage adjustment by R_{VA}.

Automatic Gain Control (pin AGC)

The TEA1118 and TEA1118A perform automatic line loss compensation. The automatic gain control varies the gain of the transmit amplifier and the gain of the receive amplifier in accordance with the DC line current.
The control range is 5.8 dB (which corresponds approximately to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km). The ICs can be used with different configurations of feeding bridge (supply voltage and bridge resistance) by connecting an external resistor R_{AGC} between pins AGC and V_{EE}. This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

DTMF amplifier (pin DTMF; TEA1118A only)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones can be heard in the earpiece at a low level (confidence tone).

The TEA1118A has an asymmetrical DTMF input.
The input impedance between DTMF and V_{EE} is 20 kΩ.
The voltage gain from pin DTMF to pin LN is 17.4 dB.

The automatic gain control has no effect on the DTMF amplifier.

Mute function (pin MUTE; TEA1118A only)

The mute function performs the switching action between the speech mode and the dialling mode. When MUTE is LOW or open-circuit, the transmit and receive amplifiers inputs are enabled while the DTMF input is disabled, depending on the TMUTE level. When MUTE is HIGH, the DTMF input is enabled and the transmit and receive amplifiers inputs are disabled.

Sidetone suppression

The TEA1118 and TEA1118A anti-sidetone network comprising $R_{CC}//Z_{line}$, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Fig.12) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{[R_{ast2} \times (R_{ast3} + R_{SLPE})]}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value chosen for Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines.
The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the TEA1118 and TEA1118A attenuates the receive signal from the line by 32 dB before it enters the receive amplifier.
The attenuation is almost constant over the whole audio frequency range.

A Wheatstone bridge configuration (see Fig.13) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Applications Handbook for Wired Telecom Systems, IC03b"*, order number 9397 750 00811.

MUTE and TMUTE levels for different modes (TEA1118A only)

Table 1 Required MUTE and TMUTE levels to enable the different possible modes

MODE	CHANNEL				MUTE	TMUTE
	TRANSMIT	RECEIVE	DTMF	CONFIDENCE TONE		
Speech	on	on	off	off	LOW	LOW
DTMF dialling	off	off	on	on	HIGH	X[1]
Transmit mute	off	on	on	off	LOW	HIGH

Note

1. X = don't care.

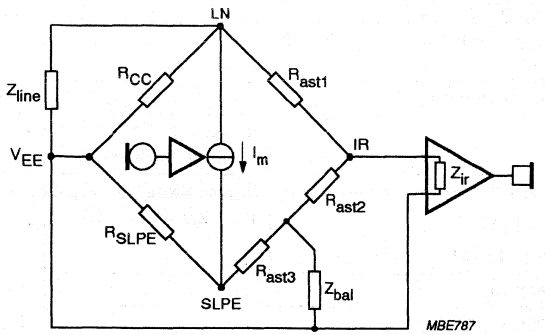


Fig.12 Equivalent circuit of TEA1118 and TEA1118A family anti-sidetone bridge.

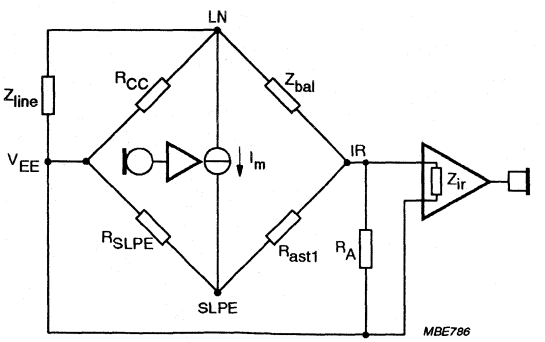


Fig.13 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

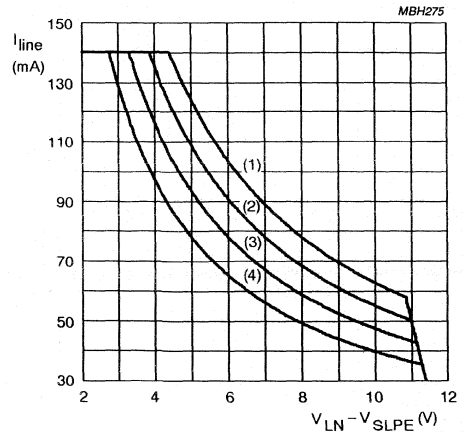
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		V_{EE} – 0.4	12	V
	repetitive line voltage during switch-on or line interruption		V_{EE} – 0.4	13.2	V
$V_{n(max)}$	maximum voltage on all pins		V_{EE} – 0.4	V_{CC} + 0.4	V
I_{line}	line current	R_{SLPE} = 20 Ω; see Figs 14 and 15	–	140	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 14 and 15			
	TEA1118T; TEA1118AT		–	384	mW
	TEA1118M; TEA1118AM		–	312	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

HANDLING

This device meets class 2 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

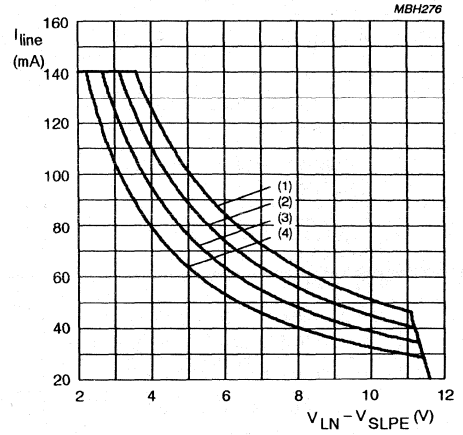
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air			
	TEA1118T; TEA1118AT		130	K/W
	TEA1118M; TEA1118AM	mounted on epoxy board 40.1 × 19.1 × 1.5 mm	160	K/W



(1) T_{amb} = 45 °C; P_{tot} = 615 mW.
(2) T_{amb} = 55 °C; P_{tot} = 538 mW.
(3) T_{amb} = 65 °C; P_{tot} = 461 mW.
(4) T_{amb} = 75 °C; P_{tot} = 384 mW.

Fig.14 SO14 safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 500 mW.
(2) T_{amb} = 55 °C; P_{tot} = 437 mW.
(3) T_{amb} = 65 °C; P_{tot} = 375 mW.
(4) T_{amb} = 75 °C; P_{tot} = 312 mW.

Fig.15 SSOP16 safe operating area.

CHARACTERISTICS

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies (pins V_{LN}, V_{CC}, SLPE and REG)						
V_{ref}	stabilized voltage between LN and SLPE		3.1	3.35	3.6	V
V_{LN}	DC line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.45	–	V
		I_{line} = 15 mA	3.35	3.65	3.95	V
		I_{line} = 140 mA	–	–	6.9	V
$V_{LN(exR)}$	DC line voltage with an external resistor R_{VA}	$R_{VA(SLPE-REG)}$ = 27 kΩ	–	4.4	–	V
$\Delta V_{LN}T$	DC line voltage variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	±30	–	mV
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_P = 0 mA	–	2.9	–	V
R_{CCint}	equivalent supply voltage resistance	I_P = 0.5 mA	–	550	620	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit amplifier (pins TX+, TX− and GAT)						
$\|Z_i\|$	input impedance					
	differential between pins TX+ and TX−		–	62.5	–	kΩ
	single-ended between pins TX+/TX− and V_{EE}		–	36.5	–	kΩ
G_{vtx}	voltage gain from TX+/TX− to LN	V_{TX} = 200 mV (RMS)	10.1	11.3	12.5	dB
ΔG_{vtxf}	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx}T$	gain variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	60	–	dB
ΔG_{vtxr}	gain voltage reduction range (TEA1118 only)	external resistor connected between GAT and REG	–	–	6	dB
$V_{LN(max)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.4	1.7	–	V
		I_{line} = 4 mA; THD = 10%	–	0.8	–	V
$V_{TX(max)}$	maximum transmit input voltage (RMS value)	I_{line} = 15 mA; THD = 2%	–	0.45	–	V
		I_{line} = 75 mA; THD = 2%	–	0.9	–	V
V_{notx}	noise output voltage at pin LN; pins TX+/TX− shorted through 200 Ω	psophometrically weighted (P53 curve)	–	−84	–	dBmp
Transmit mute (pin TMUTE; TEA1118A only)						
ΔG_{vtxm}	gain reduction	TMUTE = HIGH	–	80	–	dB
V_{IL}	LOW level input voltage		V_{EE} − 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{TMUTE}	input current	input level = HIGH	–	1.25	3	μA
Receive amplifier (pins IR, QR and GAR)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
G_{vrx}	voltage gain from IR to QR	V_{IR} = 4 mV (RMS)	29.8	31	32.2	dB
ΔG_{vrxf}	gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vrx}T$	gain variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxr}	gain voltage reduction range	external resistor connected between GAR and QR	–	–	12	dB
$V_{o(rms)}$	maximum receive signal (RMS value)	I_P = 0 mA sine wave drive; R_L = 150 Ω; THD = 2%	–	0.25	–	V
		I_P = 0 mA sine wave drive; R_L = 450 Ω; THD = 2%	–	0.35	–	V
$V_{norx(rms)}$	noise output voltage at pin QR (RMS value)	IR open-circuit; R_L = 150 Ω; psophometrically weighted (P53 curve)	–	−86	–	dBVp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic gain control (pin AGC)						
ΔG_{vtrx}	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 75 mA;	–	5.8	–	dB
I_{start}	highest line current for maximum gain		–	26	–	mA
I_{stop}	lowest line current for minimum gain		–	61	–	mA
DTMF amplifier (pin DTMF; TEA1118A only)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
G_{vtx}	voltage gain from DTMF to LN	V_{DTMF} = 100 mV (RMS); MUTE or TMUTE = HIGH	16.2	17.4	18.6	dB
ΔG_{vtxf}	gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx}T$	gain variation with temperature referenced to 25 °C	T_{amb} = −25 to + 75 °C	–	±0.4	–	dB
G_{vrx}	voltage gain from DTMF to QR (confidence tone)	V_{DTMF} = 100 mV (RMS); R_L = 150 Ω	–	−18	–	dB
Mute function (pin MUTE; TEA1118A only)						
V_{IL}	LOW level input voltage		V_{EE} − 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{MUTE}	input current	input level = HIGH	–	1.25	3	μA
ΔG_{trxm}	gain reduction for transmit and receive amplifiers	MUTE = HIGH	–	80	–	dB

APPLICATION INFORMATION

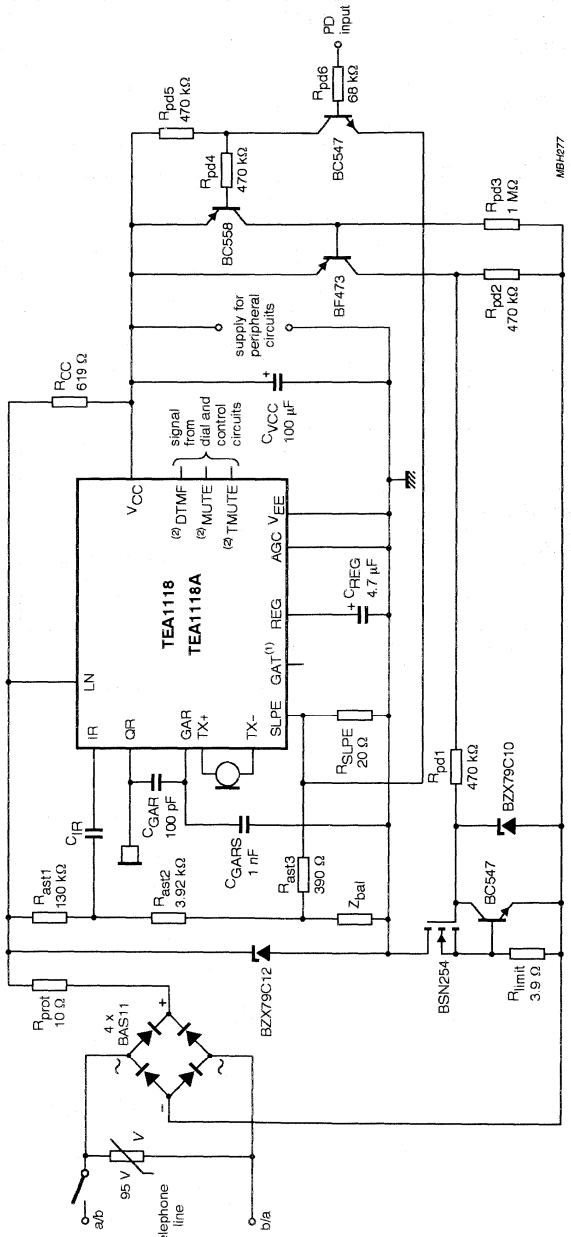


Fig.16 Typical application of the TEA1118 and TEA1118A in sets with pulse dialling or flash facilities.

(1) TEA1118 only.
(2) TEA1118A only.

Data processor for cellular radio (DPROC2) UMA1002

FEATURES

- Single chip solution to all the data handling and supervisory functions
- Configuration to both AMPS and TACS
- Additional JTACS option
- I^2C-bus serial control
- All analog interface and filtering functions fully implemented on chip
- Error handling in hardware reduces software requirements
- Robust SAT decoding and transponding circuitry
- Low current consumption by on-chip power-down modes
- Reduced system current consumption by new integrated power-saving features
  - Majority voting includes more intelligence
  - On-chip control filler word filter
  - BCH error filter
  - Possibility to program ESCC bits
- Small physical size: SO28L or LQFP32
- External peripheral component count reduced
  - On-chip selectable clock divider
  - Integrated pull-up resistor at TXLINE
- Simplified reset and abort software routines possible
- The SO28 version is fully compatible with UMA1000LT and UMF1000T.

GENERAL DESCRIPTION

The UMA1002 is a low power CMOS LSI device incorporating the data tranceiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	2.7	3.0	5.5	V
I_{DD}	supply current normal operation with external clock	–	1.3	1.8	mA
T_{amb}	operating ambient temperature	−30	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1002T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UMA1002H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

BLOCK DIAGRAM

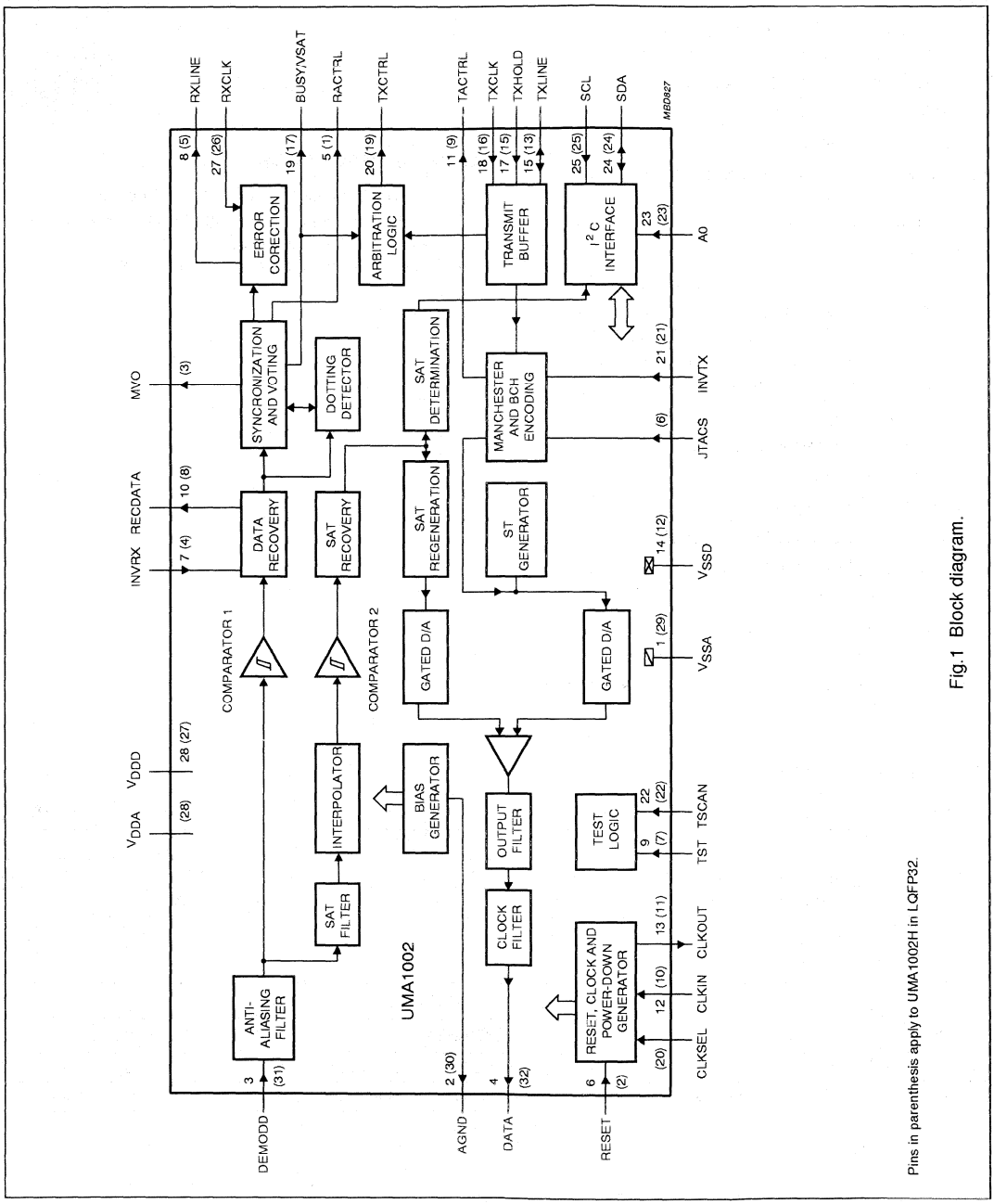


Fig.1 Block diagram.

Pins in parenthesis apply to UMA1002H in LQFP32.

PINNING

SYMBOL	PIN		DESCRIPTION
	SO28	LQFP32	
V_{SSA}	1	29	Negative analog supply (0 V). To be connected low-ohmic to V_{SSD}.
AGND	2	30	Internally generated analog signal ground. Voltage level = $\frac{1}{2}V_{DDA}$. This pin should be connected to a blocking capacitor, no DC load allowed.
DEMODD	3	31	DEMODD inputs analog data and SAT signals from the RF demodulator. This pin should normally be AC-coupled. See chapter "AC characteristics".
DATA	4	32	Data is an analog output which provides the Manchester encoded and filtered data signal, SAT and signalling tone. This signal should normally be AC-coupled into the Audio/Data summer. See chapter "AC characteristics".
RACTRL	5	1	Received audio control output. Open-drain output used to blank the audio path to the earpiece when a sequence of dotting followed by a synchronization word or 2 synchronization words separated by 77 bits is detected. RACTRL and TACTRL functions can be combined using one line. Output level LOW means audio muted.
RESET	6	2	Master reset input resetting all internal flip-flops to the specified state. This input has no influence on analog parts, but must be controlled by an active HIGH microcontroller port.
INVRX	7	4	This input inverts the sense of received data stream, which allows RF demodulators with high or low local oscillators to be used. The AMPS and TACS specifications define NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC2 depends on the receiver local oscillator. Input LOW means data normal.
RXLINE	8	5	Received data signal output to the system controller. Maximum data rate is 100 kbits/s.
TST	9	7	Test input pin (note 1).
RECDATA	10	8	Output of the recovered digital data signal (note 1).
TACTRL	11	9	Transmitter audio control output. This open-drain output is used to blank the audio path and enable the data path to the modulator during data bursts on the RVC. Output level LOW means audio muted.
CLKIN	12	10	1.2 MHz or 9.6 MHz external master clock input. This input signal should be accurate to 100×10^{-6} and have a worst case 60 : 40 mark-space ratio.
CLKOUT	13	11	Output of 1.2 MHz clock signal (for APROC) derived from CLKIN.
V_{SSD}	14	12	Negative digital supply (0 V), internally connected to substrate. To be connected low-ohmic to V_{SSA}.
TXLINE	15	13	Open-drain bi-directional data line to the system controller (internal 100 kΩ pull-up). Maximum data rate is 100 kbits/s.
n.c.	16	14	Not connected.
TXHOLD	17	15	This input holds off transmission of data when set to HIGH.
TXCLK	18	16	Transmitted data clock input from the system controller.
BUSY/VSAT	19	17	Output indicating the status of the RECC by providing output information based on a majority decision on the last 3 consecutive Busy/Idle bits (FVC = logic 0). Output level LOW means channel idle. Indicating the result of the comparison of the measured SAT and the expected SAT colour-code bits (I^2C-bus register) in the voice channel mode (FVC = logic 1 and ENSM = logic 1). Output level LOW means incoming SAT not equal to expected SAT.

SYMBOL	PIN		DESCRIPTION
	SO28	LQFP32	
TXCTRL	20	19	Transmitter control open-drain output used to disable the transmitter during an RECC access failure. Output level LOW means RF disabled.
INVTX	21	21	This input inverts the sense of transmitted data stream, which allows RF modulators with high or low local oscillators to be used. The AMPS and TACS specifications define NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator. Input LOW means data inverted.
TSCAN	22	22	Test switch input, only enabled if TST = logic 1, but should have a defined state.
A0	23	23	Input to select the least significant bit of the I^2C-bus address.
SDA	24	24	Serial data input/output (I^2C-bus).
SCL	25	25	Serial clock input (I^2C-bus).
n.c.	26	18	Not connected.
RXCLK	27	26	Received data clock input from the system controller.
V_{DDD}	28	27	Digital supply voltage (+3 V).
V_{DDA}	–	28	Analog supply voltage (+3 V).
MVO	–	3	Majority voting output indicating that on FOCC the first 3 received words do not differ from each other and thus the majority decision over 5 words can already be carried out. Because of the required speed, indication is at this pin (and not via the I^2C-bus) which can be monitored by the system controller. Output LOW means the receiver can be switched off.
JTACS	–	6	Digital input signal for JTACS, input HIGH means that data is routed from TXLINE directly without processing to gated DAC (if enabled by STEN bit).
CLKSEL	–	20	Input switch for internal divide-by-8 or divide-by-1 divider between CLKIN and CLKOUT (internal pull-down → divide-by-1 is default if not bonded out in SO28 package).

Note

1. Must not be connected in existing applications.

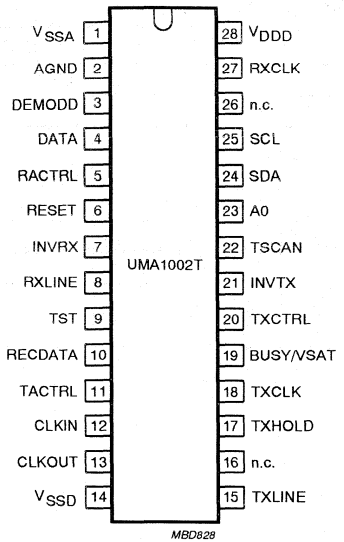


Fig.2 Pin configuration for SO28, SOT136-1.

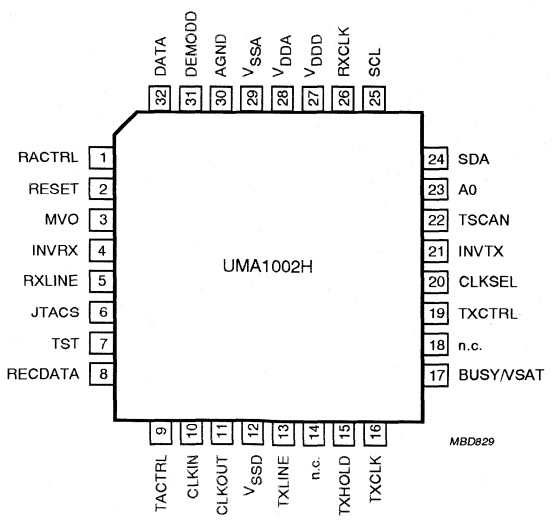


Fig.3 Pin configuration for LQFP32, SOT358-1.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	6.5	V
I_{DD}	supply current		–	50	mA
I_I	DC input current (any input)		–	±10	mA
I_O	DC output current (any output)		–	±10	mA
V_I	input voltages (all inputs)	$V_{DD(max)}$ = 6.0 V	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation		–	300	mW
P_o	power dissipation per output		–	10	mW
T_{amb}	operating ambient temperature		−30	+70	°C
T_{stg}	storage temperature		−65	+150	°C

DC CHARACTERISTICS

V_{DD} = 3 V (V_{DDA} and V_{DDD} externally connected); T_{amb} = −30 to +70 °C; f_{CLKIN} = 1.2 MHz (if CLKSEL = logic 0); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	3.0	5.5	V
I_{DD}	operating supply current at pins V_{DDD} and V_{DDA}	in FVC	–	1.3	1.8	mA
		in FOCC	–	0.4	–	mA
Digital inputs: INVRX, INVTX, CLKSEL, TXHOLD, TXCLK, A0, RESET, RXCLK, TST, TSCAN, CLKIN and JTACS						
V_{IL}	LOW level input voltage		−0.3	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.8V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	LOW/HIGH level input leakage current	pins without pull-down	–	–	1	μA
$R_{pdCLKSEL}$	CLKSEL internal pull-down resistance		–	200	–	kΩ
$R_{pdJTACS}$	JTACS internal pull-down resistance		–	200	–	kΩ
R_{pdTST}	TST internal pull-down resistance		–	200	–	kΩ
Digital push-pull outputs: RXLINE, BUSY/VSAT, RECDATA, MVO and CLKOUT						
V_{OL}	LOW level output voltage	I_{sink} = 1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = −1 mA	V_{DD} − 0.4	–	–	V
Open-drain n-channel outputs: TXCTRL, TACTRL and RACTRL						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	–	0.4	V
Open-drain n-channel input/output: TXLINE						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	–	0.4	V
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
$R_{puTXLINE}$	internal pull-up resistance		–	100	–	kΩ
I²C-bus pins: SCL and SDA						
t_{data}	data conversion rate		–	–	100	kbits/s
Analog reference pin: AGND						
V_{AGND}	DC voltage level	for V_{DD} = 2.7 to 5.5 V	–	$0.5V_{DD}$	–	V

AC CHARACTERISTICS

V_{DD} = 3 V (V_{DDA} and V_{DDD} externally connected); T_{amb} = –30 to +70 °C; f_{CLKIN} = 1.2 MHz (if CLKSEL = logic 0); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data rate of data transfer link: RXCLK, RXLINE, TXCLK, TXLINE						
t_{data}	data conversion rate		–	–	500	kbit/s
Clock input: CLKIN (CLKSEL = logic 0)						
C_i	input capacitance		–	5	–	pF
T_{CLKIN}	clock input period time		833.25	833.33	833.42	ns
t_{CLKINH}	clock input HIGH time		40	50	60	$\%T_{CLKIN}$
t_r	clock input rise time		–	50	–	ns
t_f	clock input fall time		–	50	–	ns
Clock input: CLKIN (CLKSEL = logic 1)						
T_{CLKIN}	clock input period time		–	104.17	–	ns
t_{CLKINH}	clock input HIGH time		40	50	60	$\%T_{CLKIN}$
t_r	clock input rise time		–	5	–	ns
t_f	clock input fall time		–	5	–	ns
Analog output: DATA						
V_{DATA}	DC output voltage level		–	V_{AGND}	–	V
$V_{o(p-p)}$	output voltage level for signalling tone (peak-to-peak value)	V_{DD} = 3 V; note 1	1.14	1.2	1.26	V
		V_{DD} = 5 V; note 1	1.9	2.0	2.1	V
THD	total harmonic distortion for Supervisory Audio Tone (SAT)		–	–	10	%
R_L	allowed load resistance to AC ground		10	–	–	kΩ
C_L	allowed load capacitance to AC ground		–	–	100	pF
Analog input: DEMODD						
V_{DEMODD}	DC input voltage level	100 kΩ resistor external to AGND	–	V_{AGND}	–	V
$V_{i(p-p)}$	data input voltage level (peak-to-peak value)	input via a 10 nF capacitor	200	250	600	mV
$V_{i(p-p)}$	SAT input voltage level (peak-to-peak value)		50	–	–	mV
Z_i	input impedance		1	–	–	MΩ

Note

1. Plus supply voltage variation (ΔV_{DD}), R_L = 10 kΩ.

FUNCTIONAL DESCRIPTION

General

The UMA1002 (DPROC2) is a single-chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.

These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction, decoding and encoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation.

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels. Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticeable by the user. A data rate of 10 kbits/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig.4.

A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz) is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analogous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the 'loop'. At the base station this signal is used to ascertain the overall quality of the communication link.

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

The key requirements of a hand-held portable cellular set are:

- Small physical size
- Minimum number of interconnections (serial bus)
- Low power consumption
- Low cost.

The DPROC2 is a member of our Cellular Radio chip set, based on the I²C-bus, which meets these requirements.

A cellular radio system schematic using the chip set is shown in Fig.11.

DPROC2 power-saving features

To support current saving in the application DPROC2 has three different modes of circuit operation implemented. They are decoded by the I²C-bus register bit FVC and by activity on the data transfer link (TXCLK and TXLINE). In power-down mode the relevant digital circuits have the clock disabled, the analog circuits have the bias currents and the switched capacitor clock switched off.

- Normal mode: all circuit parts are operating (e.g. on Voice channels)
- Power-down mode 1: the SAT path is in power-down (e.g. during access of the RECC)
- Power-down mode 2: the SAT path and the total data transmit path are in power-down (e.g. for Idle state, DPROC2 operating only on FOCC).

System power-saving features

Besides the above mentioned power-down modes DPROC2 also includes features to reduce system current (e.g. switching off parts of the receiver, and put the system controller into Idle mode for longer periods of time).
All these features are controlled by the I²C-bus. For further explanation of the following features refer to the Section I²C-bus registers.

MAJORITY VOTING (ONLY IN LQFP32)

Majority voting includes more intelligence. This feature is enabled in FOCC with I²C-bus bit MAJ = logic 1.
If 3 consecutive identical words have been received it is signalled via pin MVO. Therefore during the last 2 frame words the receiver could be switched off to save system current consumption.

CONTROL FILLER WORDS FILTER

System current can be further reduced by an on-chip control filler words filter in FOCC, which enables the detection of consecutive identical control filler words.
If consecutive control filler words are identical (i.e. DCC, CMAC and WFOM) they will not be passed on to the microcontroller. Consequently the system controller can remain in power-saving mode.

PROGRAMMING OF ESCC BITS

There is a possibility to program the expected ESCC bits, so that DPROC2 can compare expected and received SAT and signal any inconsistency to the system controller via BUSY/VSAT pin. Consequently there is no need to read the measured SAT periodically via the I²C-bus.

BCH ERROR FILTER

If this feature is enabled, DPROC2 will not pass on to the microcontroller words with BCH errors. Consequently the microcontroller can remain in power-saving mode. This feature in combination with the control filler feature is defined in Table 8.

SELECTABLE CLOCK DIVIDER (ONLY IN LQFP32)

An on-chip selectable divide-by-8 clock divider reduces external peripheral component count.

Power-up state and master reset (RESET)

RESET should be HIGH as soon as power supply is available.

DPROC2 will not respond reliably to any inputs (including RESET) until 100 μs after the power supply has settled within the specified tolerance. The analog sections of the device will have stabilized within 5 ms. No on-chip power-on reset is provided, therefore before the device can enter normal operation RESET must be held HIGH.

RESET is an active HIGH master reset input, with a minimum active pulse width of 4 μs which may be used to reset the total logic within DPROC2 to a predefined state as illustrated in Tables 1 and 2. It is preferably only used during power-up, during normal operation it is recommended to use the fully synchronous reset signals derived from the I²C-bus bits FVC, STS and TXRST (see Table 4). To ensure correct operation TXCLK must be held HIGH during RESET operation.

Table 1 Predefined state of the digital output pins

OUTPUT	STATE
RXLINE	HIGH
TXCTRL	high-impedance (HIGH)
TACTRL	high-impedance (HIGH)
RACTRL	high-impedance (HIGH)
BUSY/VSAT	HIGH
TXLINE	HIGH (by 100 kΩ internal pull-up resistor)
RECDATA	LOW
MVO	HIGH
SDA	high-impedance (HIGH)

Table 2 Predefined state of the I²C-bus registers

REGISTER	BIT							
	7	6	5	4	3	2	1	0
Status (read)	LOW	LOW	LOW	HIGH	LOW	LOW	HIGH	HIGH
Control 1 (write)	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
Control 2 (write)	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

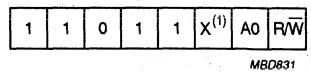
I²C-bus serial data link (SDA; SCL)

SDA is the bi-directional data line, SCL is the clock input from an I²C-bus master. These constitute a typical I²C link and conform to standard I²C-bus characteristics.
A detailed description of the I²C-bus specification, with applications, is given in the brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

- Data rate up to 100 kbits/s.

SLAVE ADDRESS SELECT (A0)

Selection of the device slave address is achieved by connecting A0 to either V_{SS} or V_{DDD}. The slave address is defined in accordance with the I²C-bus specifications as shown in Fig.4



(1) X = don't care.

Fig.4 Device slave address.

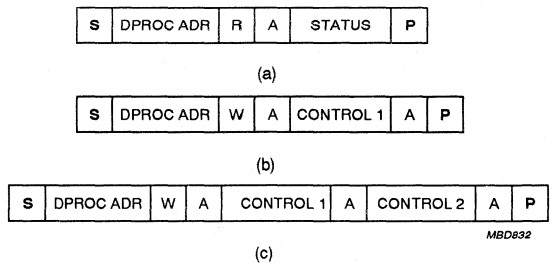
I²C-BUS REGISTERS

The I²C-bus register block resides internally within the I²C-bus interface block and contains various items of status and control information which are transferred to and from DPROC2 via the I²C-bus. The block is organized into three 8-bit registers:

- Status register which contains read only items
- Control registers 1 and 2 which contain write only items

Table 3 I²C-bus register map

REGISTER	BIT							
	7	6	5	4	3	2	1	0
Status (read)	–	–	WSYNC	BUSY	TXABRT	TXIP	MSCC1	MSCC0
Control 1 (write)	BUFEN	SERV	STS	TXRST	ABREN	FVC	STEN	SATEN
Control 2 (write)	MAJ	MR1	MR0	DBCH	DCFM	ENSM	ESCC1	ESCC0



(a) Read from DPROC2 status register.
(b) Write to DPROC2 control register 1.
(c) Write to all DPROC2 control registers.

Where:
S = START condition
W = read/write bit (logic 0 = write)
R = read/write bit (logic 1 = read)
A = acknowledge bit
P = STOP condition
DPROC ADR = slave address of DPROC2.

Fig.5 I²C-bus data format.

Table 4 Description of I²C-bus register map

REGISTER BITS	LOGIC LEVEL	DESCRIPTION
Control Register 1		
BUFEN	0	1.2 MHz signal not available at pin CLKOUT
	1	1.2 MHz signal is available at pin CLKOUT
SERV	0	serving system data stream B selected
	1	serving system data stream A selected
STS(1)	0	TACS selected
	1	AMPS selected
TXRST	1	terminates a message being transmitted on the reverse channel; monostable signal causing a reset of the message transmission circuitry and resets the I²C-bus bits TXABRT, TXIP and clears the transmit buffer
ABREN	1	DPROC2 has permission to abort data transmission and disable RF on the RECC following the detection of a channel access attempt collision
	0	no permission for above operations
FVC(2)	0	control channel format selected
	1	voice channel format selected
STEN	0	disables output of signalling tone to pin DATA
	1	enables output of signalling tone to pin DATA if FVC = logic 1
SATEN	0	disables output of SAT transponded signal to pin DATA
	1	enables output of SAT transponded signal to pin DATA if FVC = logic 1
Control Register 2		
MAJ	0	majority voting procedure on FOCC using all 5 frame words, MVO output is always HIGH
	1	majority voting procedure on FOCC using the first 3 frame words, if they are all identical the MVO pin goes LOW (see Fig.6)
MR0, MR1	see Table 5	determines set-up time of MVO signal with respect to beginning of the next dotting (see Fig.6)
DBCH	see Table 8	BCH error filter
DCFM	see Table 8	control filler message filter
ENSM	0	enable SAT monitoring; ESCC bits are not used
	1	enable SAT monitoring; ESCC bits are used for following function
ESCC0, ESCC1	see Table 6	expected SAT colour code bits; the incoming SAT is compared to these bits, the result (expected or not expected SAT frequency) is given out by the BUSY/VSAT pin (when FVC = logic 1), which prevents periodical reading from the I²C-bus status register

REGISTER BITS	LOGIC LEVEL	DESCRIPTION
Status Register		
WSYNC	0	DPROC2 has not acquired frame synchronization in accordance with FOCC format
	1	DPROC2 has acquired frame synchronization in accordance with FOCC format
BUSY		indicates the status of RECC, determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits of the FOCC and is also routed to pin BUSY/VSAT
	0	channel idle
	1	channel busy
		indicates the result of the comparison of the incoming SAT and the stored SAT Colour Code bits in the Voice Channel mode and is also routed to pin BUSY/VSAT
	0	incoming SAT not equal to expected SAT
	1	incoming SAT equal to expected SAT
TXABRT		indicates that a RECC access attempt has been aborted without successful message transmission
	0	no access collision detected
	1	transmission attempt aborted
TXIP	0	no transmission on RECC or RVC in progress
	1	data transmission by DPROC2 on RECC or RVC in progress
MSCC1, MSCC0	see Table 7	provides information about the current measured SAT colour code

Notes

1. Changing this register bit resets internally the receive and transmit logic circuitry.
2. Changing this register bit resets internally the receive logic circuitry.

Table 5 Set-up time of MVO signal

MR0	MR1	t_{MVO} (ms)
0	0	3
0	1	6
1	0	9
1	1	12

Table 6 Expected SAT colour code

ESCC1	ESCC0	SAT FREQUENCY (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

Table 7 Measured SAT colour code

MSCC1	MSCC0	SAT FREQUENCY (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

Table 8 Conditions for transmission of received words to system controller

DBCH	DCFM	BCH ERROR BIT	CHANGE IN CONTROL FILLER WORD DETECTED	TRANSMISSION OF CONTROL FILLER WORD TO SYSTEM CONTROLLER
0	0	x	x	yes
0	1	0	0	no
0	1	0	1	yes
0	1	1	x	yes
1	0	0	x	yes
1	0	1	x	no
1	1	0	0	no
1	1	0	1	yes
1	1	1	x	no

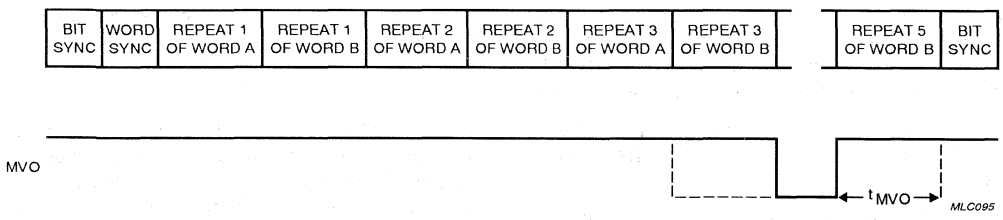


Fig.6 Timing of MVO output.

Digital circuit blocks

GENERAL

The majority of the digital circuitry within the DPROC2 device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig.1.

DATA RECOVERY

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Comparator Block, on which it performs the following functions:

- Clock recovery
- Manchester decoding
- Data regeneration.

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase-locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable 'bandwidth' to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1.2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output. The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a logic 1 otherwise it is latched as a logic 0.

SAT RECOVERY

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.

The recovery is performed using a digital phase-locked loop.

SAT DETERMINATION

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the I^2C status registers MSCC0 and MSCC1.

SAT REGENERATION

The SAT Regeneration Block generates a digital SAT stream for transponding back to the base station. The transponded SAT is phase-locked to the recovered SAT by means of a second digital phase-locked-loop. To minimize the total harmonic distortion of the output signal the transponded SAT is then processed by a delta modulator before being passed on to the Gated Digital-to-Analog converter.

DOTTING DETECTOR

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL, after a Word Synchronization Block has been received, for the duration of the burst.

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

- Frame Synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination.

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11-bit Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC2 has achieved frame synchronization.

In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode.

Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

FVC: After detection of 2 consecutive sync words the circuit leaves its Search Mode and enters the Lock Mode. The data word in between is considered as valid and already stored for Majority Voting. Whenever a sync word was found the incoming data stream is examined 88 bits later for sync again. Whenever a valid sync word is detected the following data word is given to the Majority Voting block. After missing two consecutive sync words the circuit goes back to the search mode (scanning for sync every bit). If a sync word is then detected again, the following data word is immediately accepted (and not only after two correctly timed sync words). The detection process of sync words is independent of the detection of dotting. The audio mute via pin RACTRL is activated either by receiving a sync word after detection of a dotting sequence or by entering Lock Mode.

Majority Voting Block

The Majority Voting Block performs the following functions:

- Identifying position and validity of frames in the received data stream
- Extracting five repeats of each word from a valid frame
- Performing a bit-wise majority decision on the five repeats of the data word.

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC2 is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searched for and extracted by DPROC2. On the Forward Voice Channel the extraction of a data word for majority voting is described in the Section "Word Synchronization Detector".

DPROC2 enables two mechanisms for Majority Voting. The first is based on 5 words and is described above. The other mechanism is based on 3 consecutive identical words and thus enabling switch-off of parts of the receiver during reception of the remaining two words (see Table 5 and Fig.6).

Error Correction Block

The Error Correction Block performs the following functions:

- Extraction of a valid message from the Majority-Voted Word
- Computation of the S1 and S3 syndromes
- Correction of up to one error in the word
- Communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$1 + X + X^6$ and $1 + X + X^2 + X^4 + X^6$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC2 only corrects up to one error although the code used has a Hamming distance of five. The occurrence of

two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

RECEIVED DATA SERIAL LINK

The Received Data Serial Link transfers data and control information from DPROC2 to the System Controller. The data is transferred on RXLINE under control of a clock signal RXCLK, generated by the System Controller. The system controller is informed of the arrival of a decoded data word in the DPROC2 output register by RXLINE being driven LOW. If the system controller chooses to ignore the received data or only partially clock the data out, the DPROC2 will reset the receive buffer for the next word after the period RWIN (see Fig.8).

Data format

Each Received Data word consists of 4 bytes. The word format is shown in Fig.7(a). The sense and function of the fields is shown in Table 9.

Link protocol

The Received Data protocol is described by the timing diagram Fig.8(a) and has the following parameters:

- Maximum receive window (RWIN)
  - Control Channel (TACS) = 47 ms MAJ = 0
  - Control Channel (TACS) = 30.5 ms MAJ = 1 (in FOCC only)
  - Control Channel (AMPS) = 37 ms MAJ = 0
  - Control Channel (AMPS) = 23.8 ms MAJ = 1 (in FOCC only)
- Minimum clock period (t_{CLKmin}) = 2 μs
- Minimum clock hold-off (t_{WAIT}) = 2 μs.

TRANSMIT DATA SERIAL INTERFACE

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC2 over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

Data format

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig.7(b). The sense and function of the fields is shown in Table 10.

Link protocol

Messages are normally up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. However, DPROC2 will transmit messages of any word length. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC2 to control the transfer of data words. DPROC2 has an on-chip buffer which can hold one complete word of a message. While new words are being loaded into DPROC2, within the time period Buffer clear to end of TWIN, DPROC2 will maintain uninterrupted data transmission. The System Controller can abort the transmission of a message at any point activating the I^2C-bus signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 4). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig.8(b) and has the following parameters:

- Maximum transmit window (TWIN)
  - voice channel (TACS) = 60 ms
  - voice channel (AMPS) = 48 ms
  - control channel (TACS) = 29 ms
  - control channel (AMPS) = 23 ms
- Minimum clock period (t_{CLKmin}) = 2 μs
- Minimum wait period (t_{WAIT}) = 2 μs.

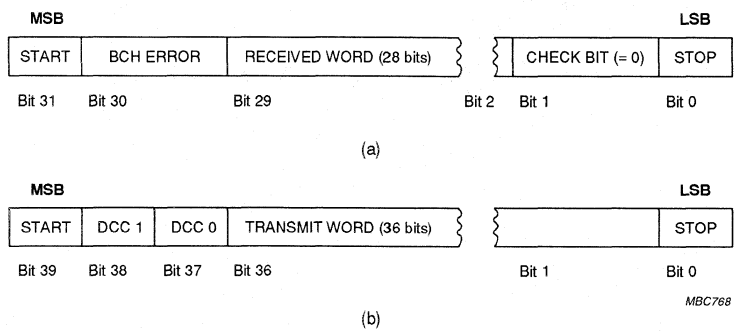
Note that TXRST will clear the transmit buffer.

Table 9 Received data word

BIT	TITLE	SENSE	FUNCTION
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	LOW	if detected as HIGH indicates that a transmission error has occurred on the microprocessor to DPROC2 serial link
0	stop	HIGH	identifies end of the word

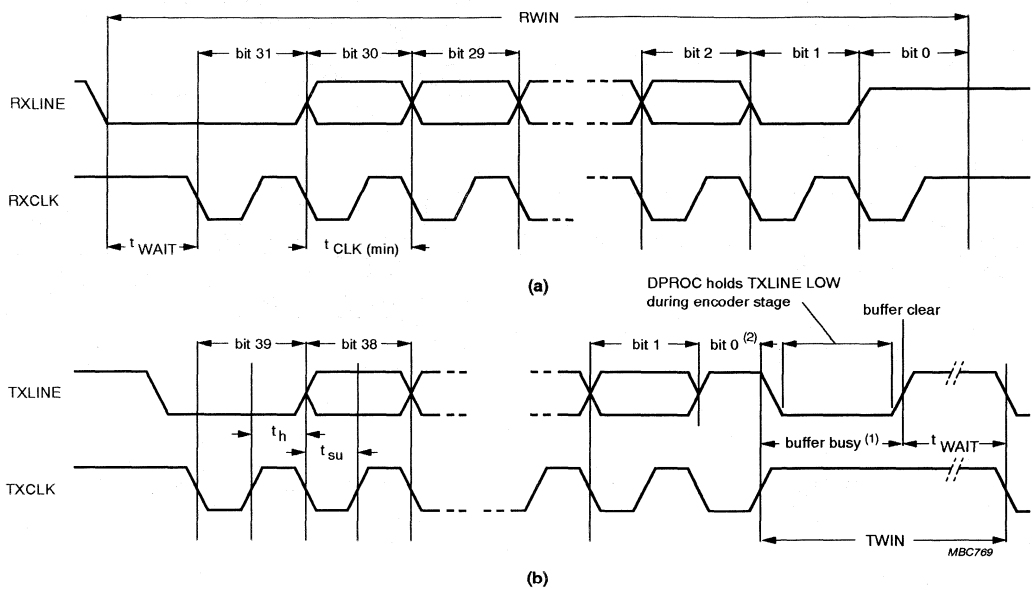
Table 10 Transmit data word

BIT	TITLE	SENSE	FUNCTION
39	start	LOW	identifies start of word
38 and 37	DCC	binary data	digital colour code (see Table 11)
36 to 1	transmit data	binary data	transmit data word
0	stop	HIGH	identifies end of the word



(a) Received data word.
(b) Transmit data word.

Fig.7 Data word formats.



(1) The buffer time depends on whether the first or subsequent words are being loaded.

(2) The system controller should monitor the TXLINE during bit 0, if the status of TXLINE does not change from a HIGH-to-LOW on the rising edge of TXCLK, then a framing error has occurred. This can be caused by glitches on the clock line or if an arbitration error occurred while the DPROC2 transmit register was being loaded. The system controller should recover the situation by holding TXLINE HIGH and supplying clocks on TXCLK until TXLINE goes LOW. Then the situation should be treated as a normal channel arbitration failure as described in Section "Reverse Control Channel Access Arbitration" - "Abort procedure (see Fig.10)".

(a) DPROC2 to microcontroller link; receive data timing.

(b) Microcontroller to DPROC2 link; transmit data timing.

Where:

t_h >100 ns

t_{su} >500 ns.

Fig.8 Data timing diagrams.

BCH AND MANCHESTER ENCODING BLOCK

The functions performed by this circuit block include:

- Reception of data from the System Controller
- Parity generation
- Message construction
- Manchester encoding.

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48-bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic equation:

$$1 + X^3 + X^4 + X^5 + X^8 + X^{10} + X^{12}$$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.

The streams are formed out of the four possible field types:

- Dotting (data inversions)
- 11-bit Synchronization Word
- Digital Colour Code (see Table 11)
- 48-bit code word.

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 11.

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

REVERSE CONTROL CHANNEL ACCESS ARBITRATION

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time. This function is performed by DPROC2 monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC2 the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ORed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing I²C-bus register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

Initial state

- Transmitter disabled
- DPROC2 transmit circuitry in power-up state
- TXCTRL line HIGH.

Table 11 Digital colour code; 7-bit word

DCC1	DCC0	CODED DCC						
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1
1	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	0	0

Access attempt procedure

1. System Controller decides to send message(1).
2. System Controller drives TXCTRL LOW directly.
3. System Controller switches transmitter power-on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).
4. System Controller sets TXRST via I²C-bus to DPROC2.
5. System Controller sets ABREN via I²C (if required) allowing DPROC2 to control the transmitter.
6. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.
7. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.
8. System Controller transfers the first word of the message to DPROC2 via serial link(1).
9. DPROC2 sets I²C-bus signal TXIP and starts sending message while monitoring Busy/Idle status.
10. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.
11. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.
12. System controller loads the subsequent words of the message into DPROC2 when the buffer becomes clear as shown in Fig.8(b).
13. On completion of entire message DPROC2 clears TXIP and 25 ms later the System Controller disables transmitter via I²C-bus.
14. System Controller finally sends TXRST to prepare DPROC2 for next transmission.

Abort procedure (see Fig.10)

1. DPROC2 immediately disables transmitter output by driving TXCTRL LOW.
2. DPROC2 sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC2 for next transmission.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

(1) At stage 1 the system controller may choose to preload DPROC2 with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC2. Figure 9 illustrates the DPROC2 data transmission timing.

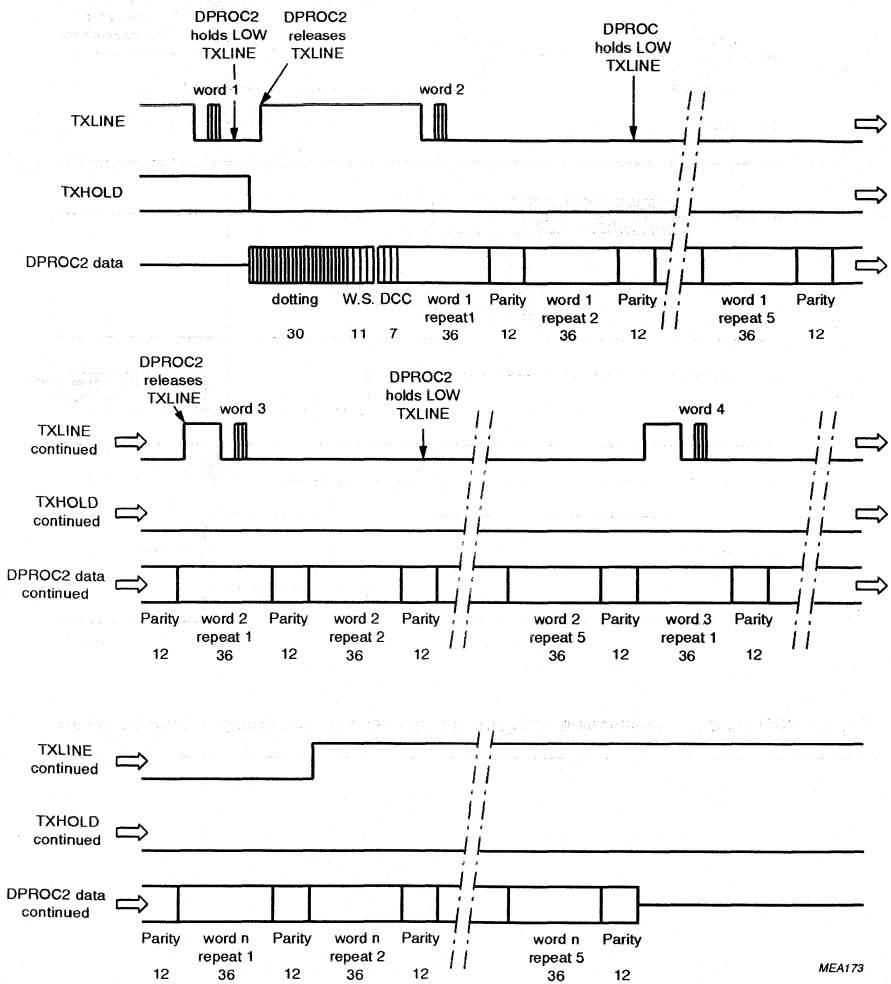


Fig.9 DPROC2 data transmission timing/microcontroller interface.

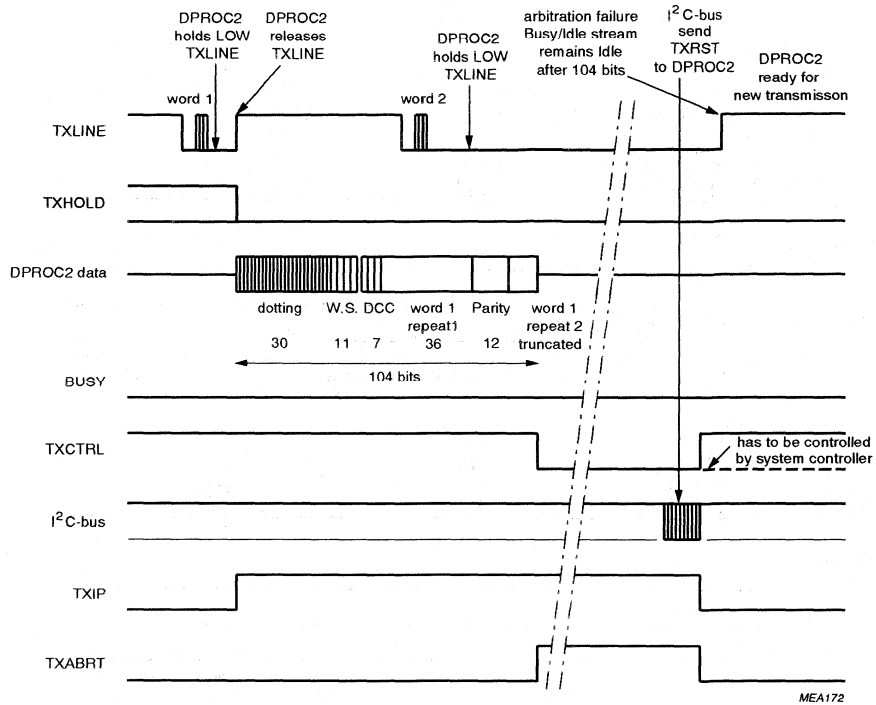


Fig.10 DPROC data transmission timing/microcontroller interface during arbitration failure.

Analog circuit blocks

General

The analog signal processing functions on DPROC2 are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by RC active filters, passive interpolators and comparators.

The RC sections, the Anti-Alias Filter and the Clock Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolator increases the sampling rate from 300 kHz to 1.2 MHz. The sampled analog signals from the Passive Interpolator is converted to a sampled 2-state digital signal by a Comparator. The Gated Digital-to-Analog converters and Analog Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROC2 output signals, and conversion to the sampled analog domain.

These analog sections of the device are shown in Fig.1.

Bias Generator

The Bias Generator generates the analog ground reference voltage (AGND) used internally within the DPROC2 device. To minimize noise AGND must be externally decoupled to V_{SSA} as shown in Fig.12. It also contains a current reference to generate all bias currents for the analog circuits.

Anti-Aliasing Filter

The Anti-Aliasing Filter is placed before the SAT filter block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Aliasing Filter is a time-continuous RC-active low-pass filter.

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the SAT filter. This reduces the coarseness of the zero-crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Comparators

The Comparators form the analog-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers which convert the filtered sampled analog signals into 2-state sampled digital signals containing only the zero-crossing information from the analog signal. To prevent unwanted signals being processed by the digital circuitry both comparators have a hysteresis implemented

Gated Digital-to-Analog and Analog Summer

The Gated Digital-to-Analog converters and Analog Summer form the interface between the digital and analog circuitry on the transmit path of DPROC2. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal.

The data streams are enabled by the I^2C signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analog conversion and sub-sampling operation is performed by the Gated Digital-to-Analog converters and Analog Summer. The typical relative signal weights applied in the summer (with respect to the data path) are shown in Table 12.

Table 12 Typical relative signal weight

SIGNAL	RELATIVE OUTPUT LEVEL AMPS AND TACS
ST or DATA	1.0
SAT	0.25

Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC2 output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC-coupling from the DATA pin.

Clock Filter

The Clock Noise Filter is a non-critical continuous time RC-active low-pass filter used to remove any switching transient residues from the output signal. It contains an output driver stage to provide a low output impedance and sufficient driving capability for the pin DATA

APPLICATION INFORMATION

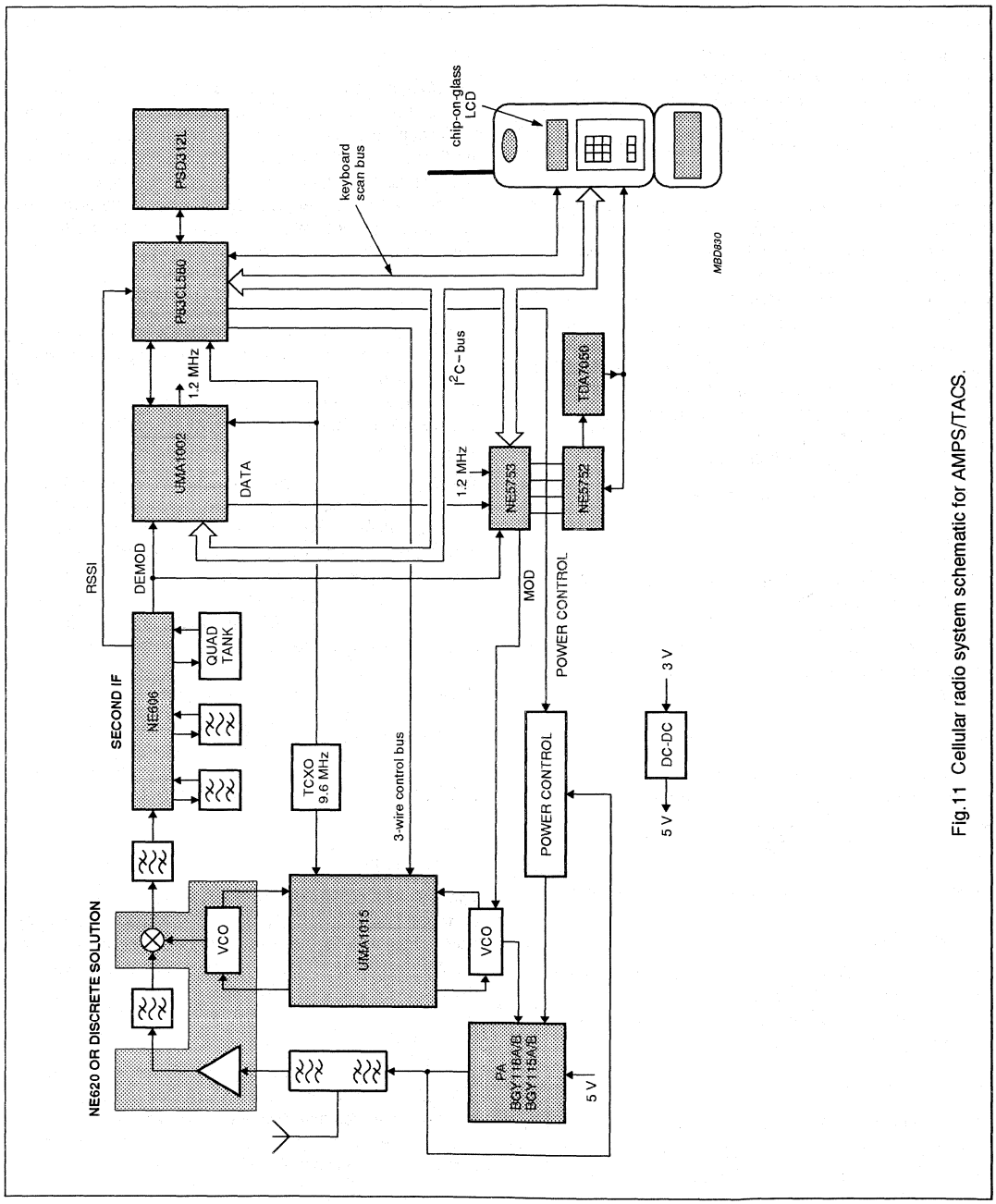


Fig.11 Cellular radio system schematic for AMPS/TACS.

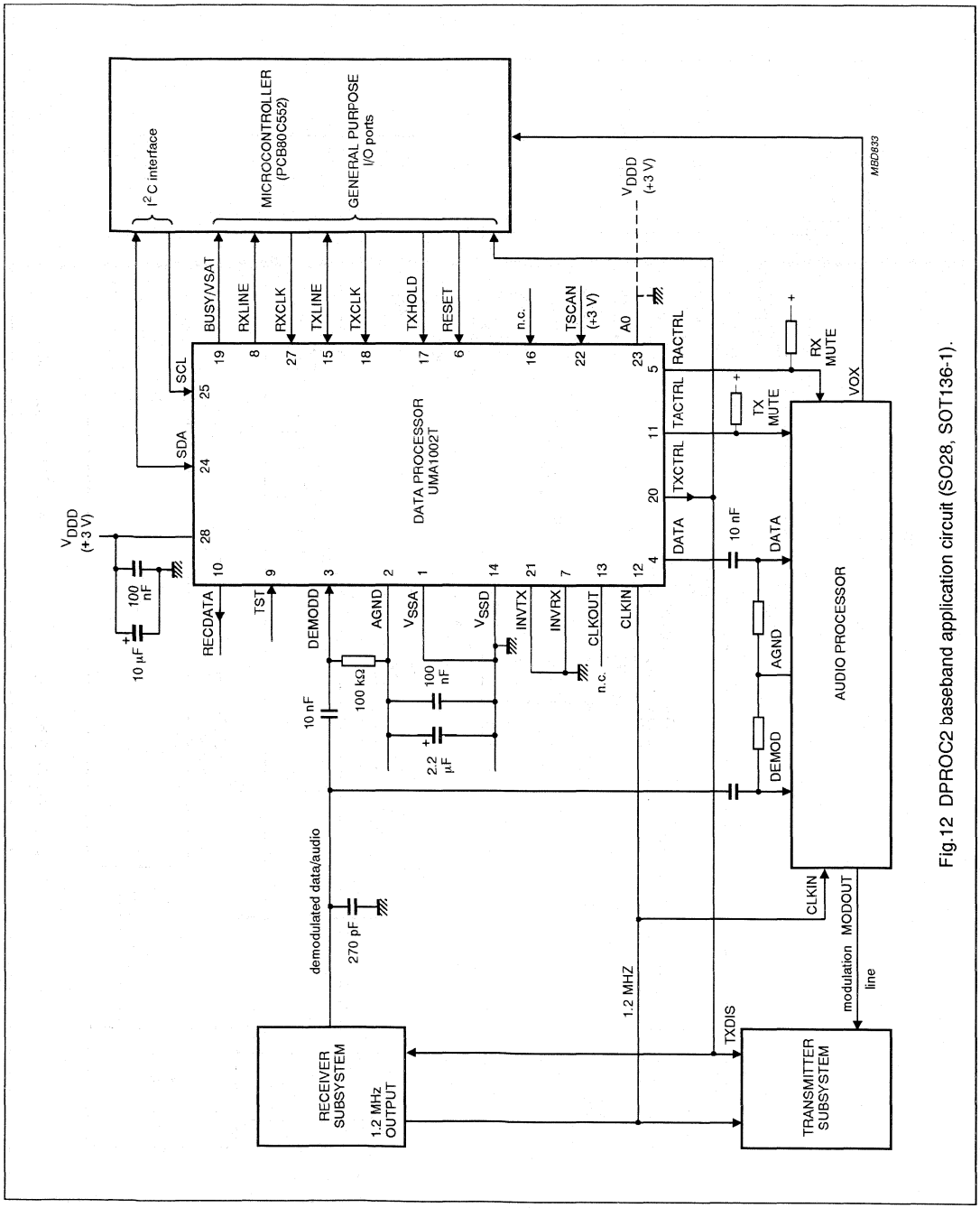


Fig.12 DPROC2 baseband application circuit (SO28, SOT136-1).

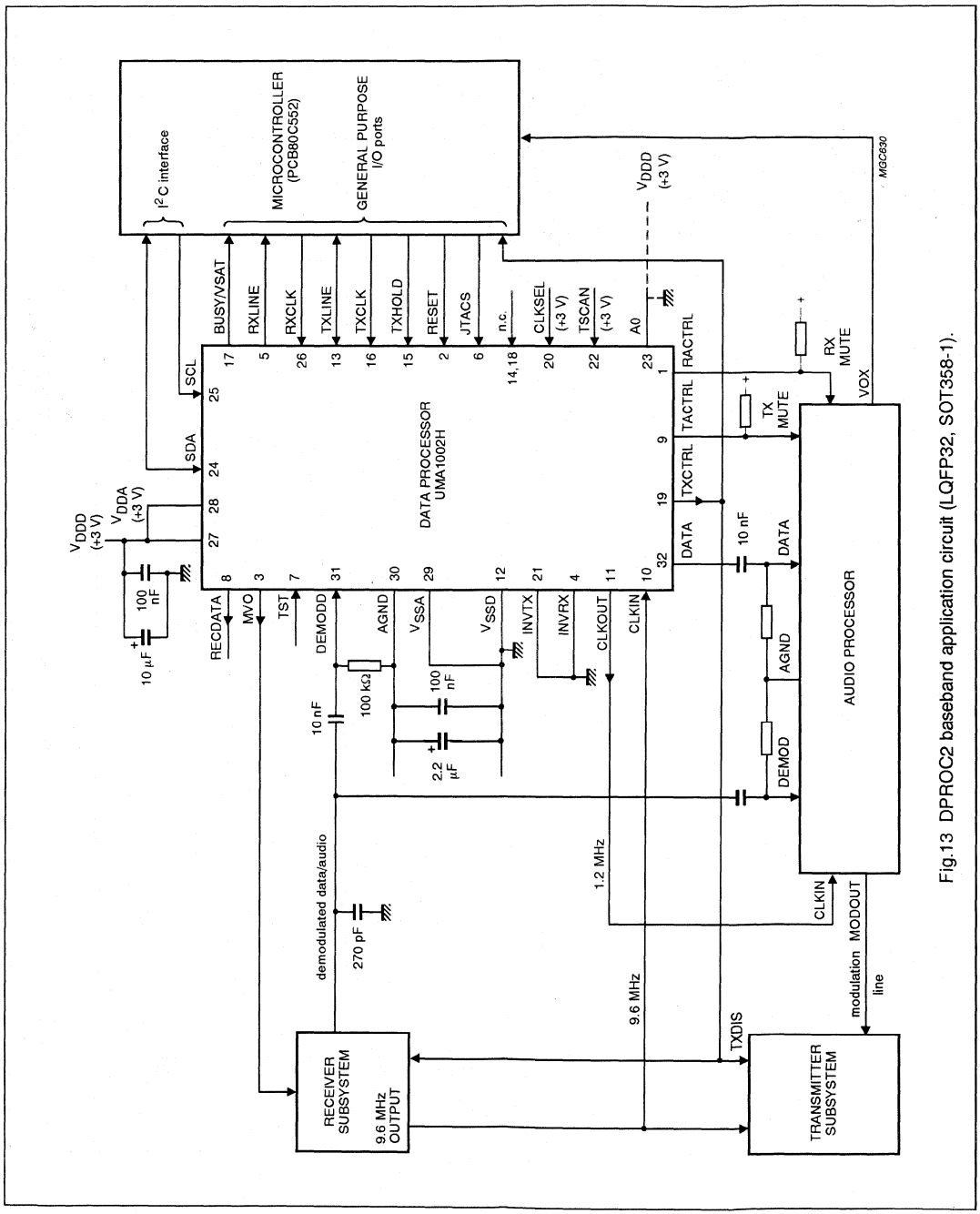
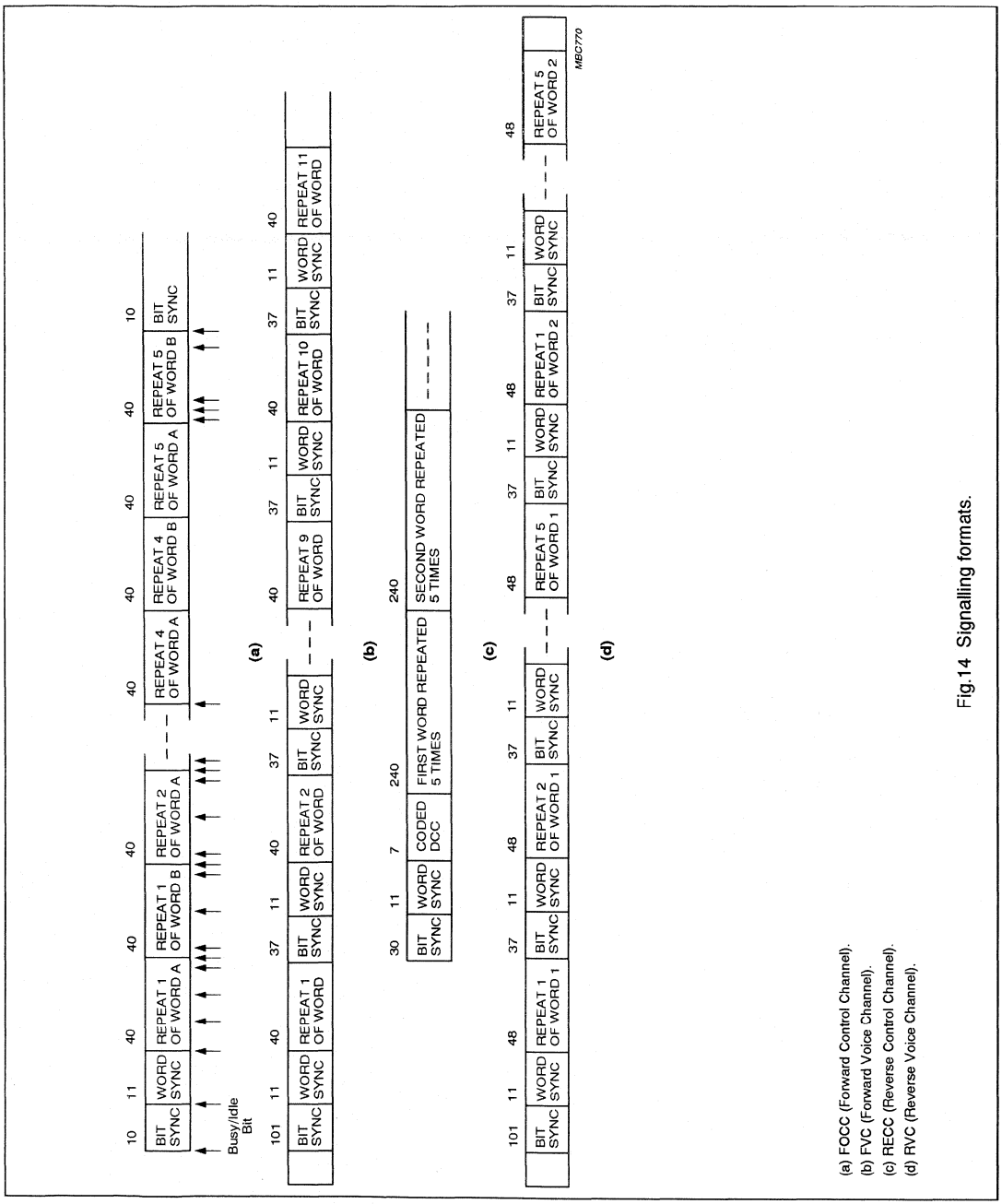


Fig.13 DPROC2 baseband application circuit (LQFP32, SOT358-1).

SIGNALLING FORMATS



(a) FOCC (Forward Control Channel).
(b) FVC (Forward Voice Channel).
(c) RECC (Reverse Control Channel).
(d) RVC (Reverse Voice Channel).

Fig.14 Signalling formats.

Section 10
Compandors

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The Philips Family of High Performance Compandors

	V_{CC}	I_{CC}	Pins	Packages	ALC Voltage	Reference Gain	Unity Down	Power Features	Key	Applications
NE/SA570	6-24V	3.2mA	16	D, F, N	Both Channels	Fixed 1.8V	775mV$_{RMS}$	No	– Excellent Unity Gain Tracking Error – Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
NE/SA571	6-18V	3.2mA	16	D, F, N	Both Channels	Fixed 1.8V	775mV$_{RMS}$	No	– Excellent Unity Gain Tracking Error – Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
NE/SA572	6-2V	6mA	16	D, F, N	Both Channels	Fixed 2.5V	100mV$_{RMS}$	No	– Independent Attack & Release time – Good THD – Need an Ext Summing Op Amp	High Performance Audio Circuits "Hi-Fi Studio Quality"
NE/SA575	3-7V	3-5.5mA	20	D, DK, N	Right Channels	$V_{CC}/2$	100mV$_{RMS}$	No	– Two uncommitted On-chip Op Amps Available – Low Voltage	Consumer Audio Audio Circuits "Commercial Quality"
NE/SA576	2-7V	1-3mA*	14	D, N	Right Channels	$V_{CC}/2$	100mV$_{RMS}$	No	– Low Power – Low External Component Count	Battery Powered Systems "Commercial Quality"
NE/SA577	2-7V	1-2mA*	14	D, N	Right Channels	$V_{CC}/2$	10mV to 1mV$_{RMS}$	No	– Low Power – Programmable Unity Gain	Battery Powered Systems "Commercial Quality"
NE/SA578	2-7V	1-2mA*	16	D, N	Right Channels	$V_{CC}/2$	10mV to 1mV$_{RMS}$	Yes (170µA)	– Low Power – Programmable Unity Gain – Power Down – Mute Function Summing Capability (DTMF) – 600Ω Drive Capability	Battery Powered Systems "Commercial Quality"

NOTE: NE/SA5750 and SA5752/5753 are also Excellent Audio Processor Components for High Performance Cordless and Cellular Applications that include the Companding Function
*I_{CC} varies with V_{CC}
Packages include: NE: 0 to 70°C; SA: -40 to +85°C; N: Plastic DIP; D; Plastic SO; F: Ceramic DIP; DK: SSOP (Shrink Small Outline Package)
Applications include: Cordless Phones, Cellular Phones, Wireless Mics, Modems, Consumer Audio and Two-Way Communications.

Compandor NE570/571/SA571

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

FEATURES

- Complete compressor and expandor in one IChip
- Temperature compensated
- Greater than 110dB dynamic range
- Operates down to 6VDC
- System levels adjustable with external components
- Distortion may be trimmed out
- Dynamic noise reduction systems
- Voltage-controlled amplifier

PIN CONFIGURATION

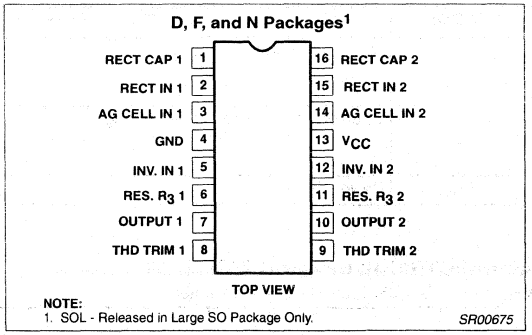


Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio
- Telephone trunk compandor—570
- Telephone subscriber compandor—571
- High level limiter
- Low level expandor—noise gate
- Dynamic filters
- CD Player

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline Large (SOL)	0 to +70°C	NE570D	SOT162-1
16-Pin Ceramic Dual In-Line Package (Cerdip)	0 to +70°C	NE570F	0582B
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE570N	SOT28-4
16-Pin Plastic Small Outline Large (SOL)	0 to +70°C	NE571D	SOT162-1
16-Pin Ceramic Dual In-Line Package (Cerdip)	0 to +70°C	NE571F	0582B
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE571N	SOT28-4
16-Pin Plastic Small Outline Large (SOL)	-40 to +85°C	SA571D	SOT162-1
16-Pin Ceramic Dual In-Line Package (Cerdip)	-40 to +85°C	SA571F	0582B
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA571N	SOT28-4

BLOCK DIAGRAM

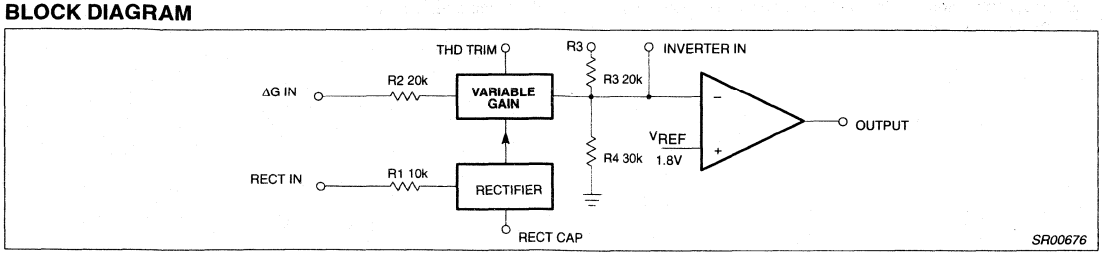


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage 570 571	 24 18	VDC
T_A	Operating ambient temperature range NE SA	 0 to 70 -40 to +85	°C
P_D	Power dissipation	400	mW

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			LIMITS			UNITS
			NE570			NE/SA571[5]			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		6		24	6		18	V
I_{CC}	Supply current	No signal		3.2	4.8		3.2	4.8	mA
I_{OUT}	Output current capability		±20			±20			mA
SR	Output slew rate			±.5			±.5		V/µs
	Gain cell distortion[2]	Untrimmed Trimmed		0.3 0.05	1.0		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15		±5	±15	%
	Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±20	±100		±30	±150	mV
	Expandor output noise	No signal, 15Hz-20kHz[1]		20	45		20	60	µV
	Unity gain level[6]	1kHz	-1	0	+1	-1.5	0	+1.5	dBm
	Gain change[2, 4]			±0.1	±0.2		±0.1		dB
	Reference drift[4]			±5	±10		+2, -25	+20, -50	mV
	Resistor drift[4]			+1, -0			+8, -0		%
	Tracking error (measured relative to value at unity gain) equals [V_O - V_O (unity gain)] dB - V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB V_2 = -30dBm, V_1 = 0dB		+0.2 +0.2	 -0.5, +1		+0.2 +0.2	 -1, +1.5	dB
	Channel separation			60			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at T_A = 25°C.
5. Electrical characteristics for the SA571 only are specified over -40 to +85°C temperature range.
6. 0dBm = 775mV_{RMS}.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{avg}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{avg}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})_e - t/\tau + G_{final} \; ; \; \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V_{RMS}) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expander circuits.

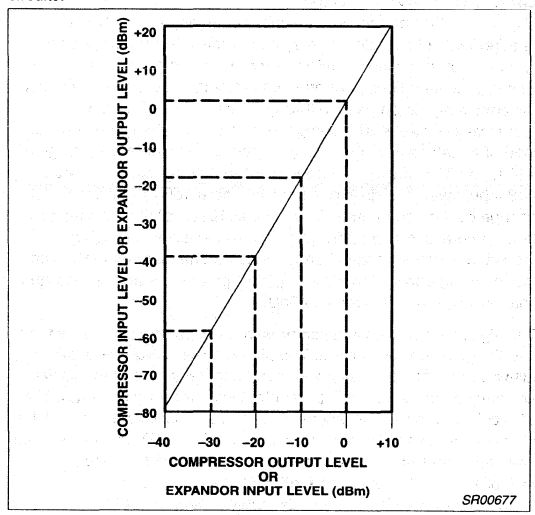


Figure 3. Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT

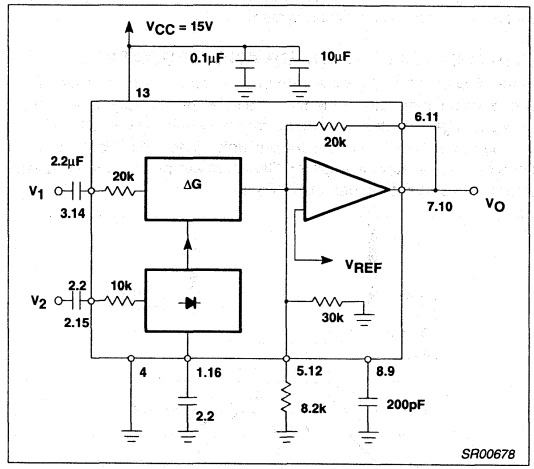


Figure 4. Typical Test Circuit

INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components.

This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 5 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expander are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 6 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

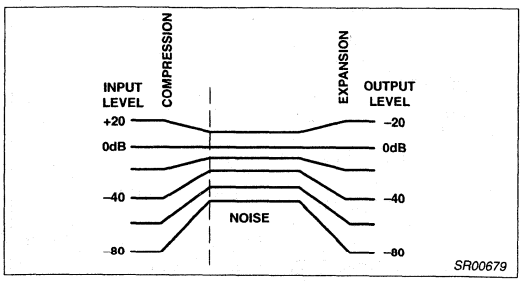


Figure 5. Restricted Dynamic Range Channel

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 7 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 8 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

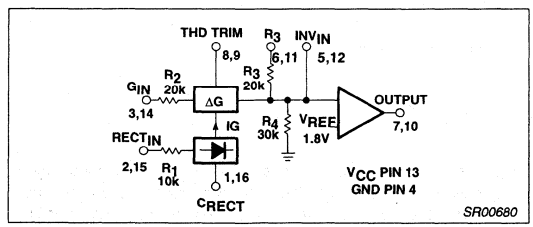


Figure 6. Chip Block Diagram (1 of 2 Channels)

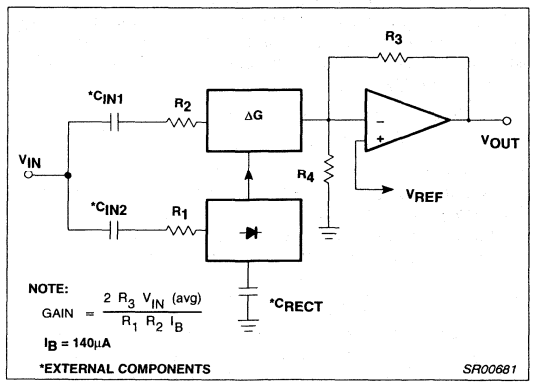


Figure 7. Basic Expander

$$V_{REF} = \left(1 + \frac{R_{DCTOT}}{30k}\right) 1.8V$$

The output of the expander will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4} V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.

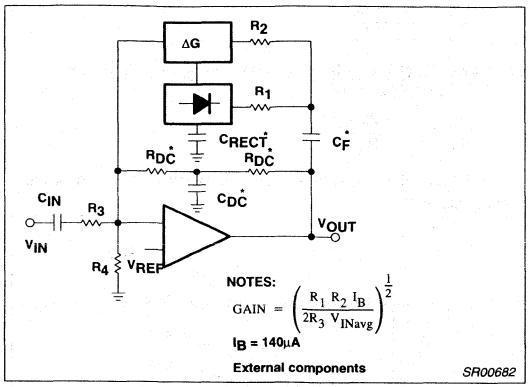


Figure 8. Basic Compressor

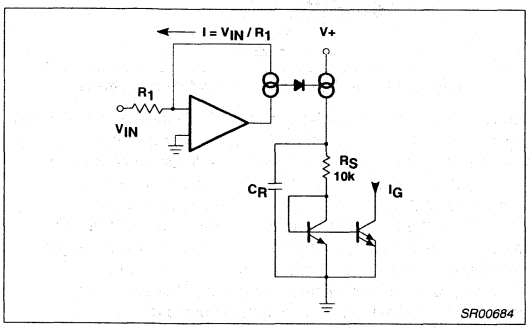


Figure 9. Rectifier Concept

CIRCUIT DETAILS—RECTIFIER

Figure 9 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.

Figure 10 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the *a* of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The *a*'s of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 11 shows the rectifier accuracy vs input level at a frequency of 1kHz.

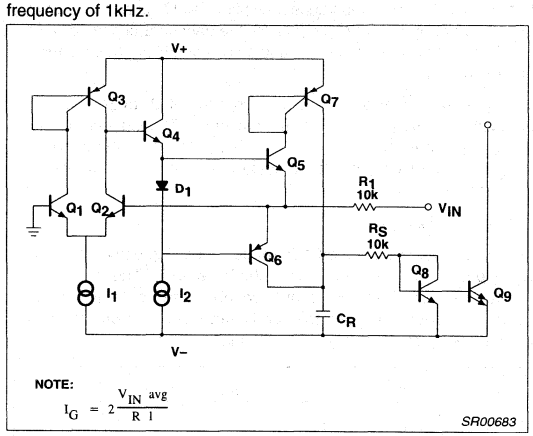


Figure 10. Simplified Rectifier Schematic

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 12. The response at all three levels is flat to well above the audio range.

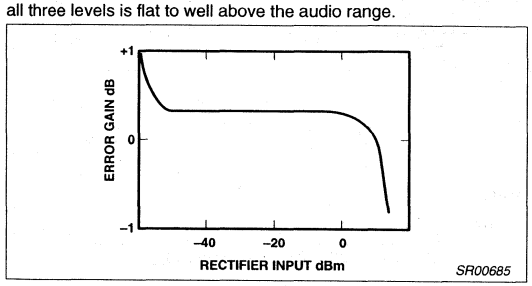


Figure 11. Rectifier Accuracy

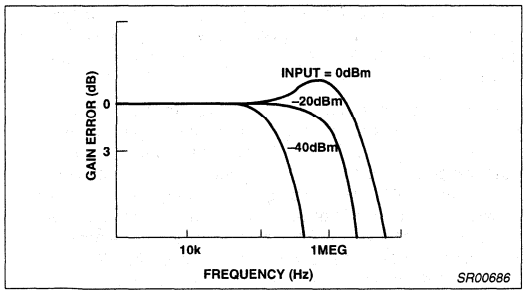


Figure 12. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 13 is a diagram of the variable gain cell. This is a linearized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} (=V_{IN}/R_2) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1}=I_1+I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

$I_2-(I_1+I_{IN})=I_1-I_{IN}=I_{C2}$.

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

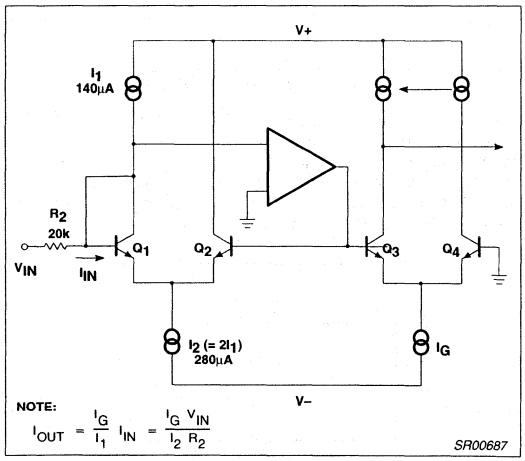


Figure 13. Simplified ΔG Cell Schematic

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G=I_{C3}+I_{C4}$ and $I_{OUT}=I_{C4}-I_{C3}$ will yield the multiplier transfer function,

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN} I_G}{R_2 I_1}$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

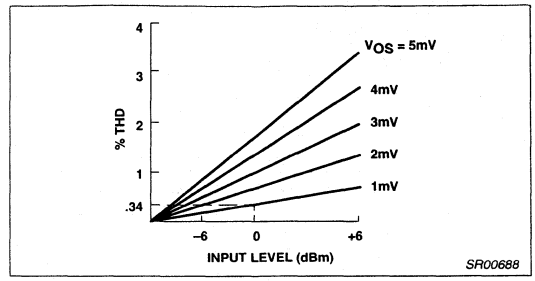


Figure 14. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 14 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated

second harmonic distortion. Figure 15 shows the simple trim network required.

Figure 16 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

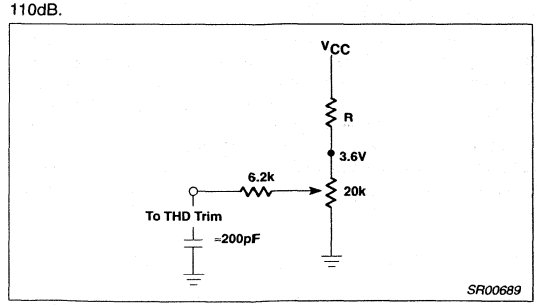


Figure 15. THD Trim Network

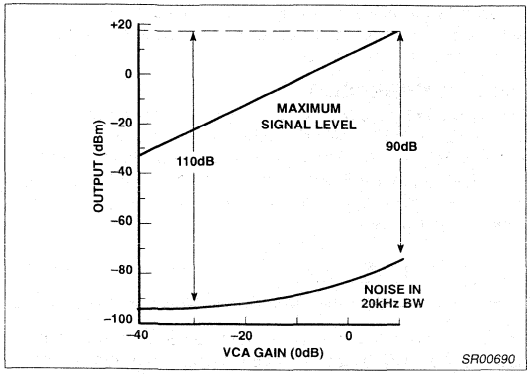


Figure 16. Dynamic Range of NE570

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 17 shows such a trim network.

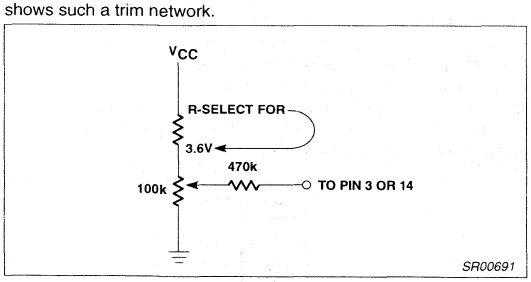


Figure 17. Control Signal Feedthrough

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 18 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

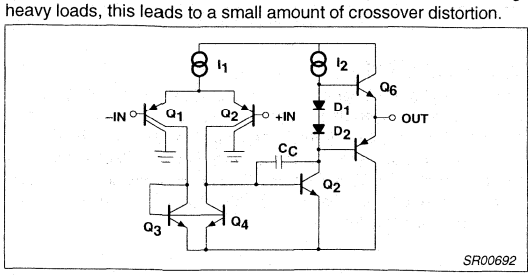


Figure 18. Operational Amplifier

RESISTORS

Inspection of the gain equations in Figures 7 and 8 will show that the basic compressor and expander circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 19 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

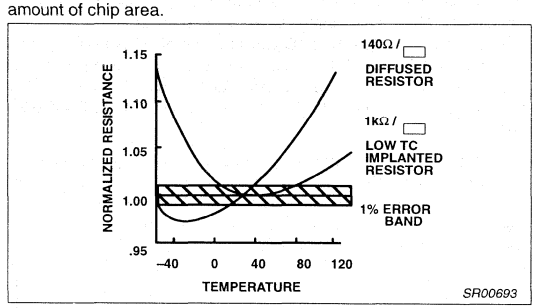


Figure 19. Resistance vs Temperature

Applications for compandors NE570/571/SA571 AN174

APPLICATIONS

The following circuits will illustrate some of the wide variety of applications for the NE570.

BASIC EXPANDOR

Figure 1 shows how the circuit would be hooked up for use as an expandor. Both the rectifier and ΔG cell inputs are tied to V_{IN} so that the gain is proportional to the average value of (V_{IN}). Thus, when V_{IN} falls 6dB, the gain drops 6dB and the output drops 12dB. The exact expression for the gain is

$$\text{Gain exp.} = \left[\frac{2\ R_3\ V_{IN}\ (avg)}{R_1\ R_2\ I_B}\right]^2$$

$I_B = 140\mu A$

The maximum input that can be handled by the circuit in Figure 1 is a peak of 3V. The rectifier input current can be as large as $I=3V/R_1=3V/10k=300\mu A$. The ΔG cell input current should be limited to $I=2.8V/R_2=2.8V/20k=140\mu A$. If it is necessary to handle larger input voltages than 0 ±2.8V peak, external resistors should be placed in series with R_1 and R_2 to limit the input current to the above values.

Figure 1 shows a pair of input capacitors C_{IN1} and C_{IN2}. It is now necessary to use both capacitors if low level tracking accuracy is not important. If R_1 and R_2 are tied together and share a common capacitor, a small current will flow between the ΔG cell summing node and the rectifier summing node due to offset

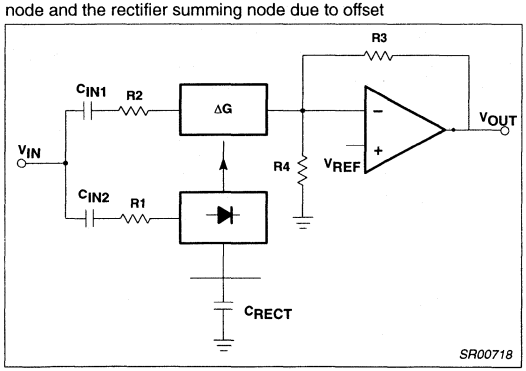


Figure 1. Basic Expandor

voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.

The output of the expandor is biased up to 3V by the DC gain provided by R_3, R_4. The output will bias up to

$$V_{OUTDC} = 1 + \frac{R_3}{R_4}\ V_{REF}$$

For supply voltages higher than 6V, R_4 can be shunted with an external resistor to bias the output up to V_{CC}.

Note that it is possible to externally increase R_1, R_2, and R_3, and to decrease R_3 and R_4. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, R_1 and R_2 may be increased; if a larger output is required, R_3 may be increased. To obtain the largest dynamic range out of this circuit, the rectifier input should always be as large as possible (subject to the ±300μA peak current restriction).

BASIC COMPRESSOR

Figure 2 shows how to use the NE570/571 as a compressor. It functions as an expandor in the feedback loop of an op amp. If the input rises 6dB, the output can rise only 3dB. The 3dB increase in output level produces a 3dB increase in gain in the ΔG cell, yielding a 6dB increase in feedback current to the summing node. Exact expression for gain is

$$\text{Gain comp.} = \left[\frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (avg)}\right]^{\frac{1}{2}}$$

The same restrictions for the rectifier and ΔG cell maximum input current still hold, which place a limit on the maximum compressor output. As in the expandor, the rectifier and ΔG cell inputs could be made common to save a capacitor, but low level tracking accuracy would suffer. Since there is no DC feedback path around the op amp through the ΔG cell, one must be provided externally. The pair of resistors R_{DC} and the capacitor C_{DC} must be provided. The op amp output will bias up to

$$V_{OUTDC} = \left(1 + \frac{R_{DC}}{R_4}\right) V_{REF}$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the ±300μA peak current restriction). If the input signal is small, a large output can be produced by reducing R_3 with the attendant decrease in input impedance, or by increasing R_1 or R_2. It would be best to increase R_2 rather than R_1 so that the rectifier input current is not reduced.

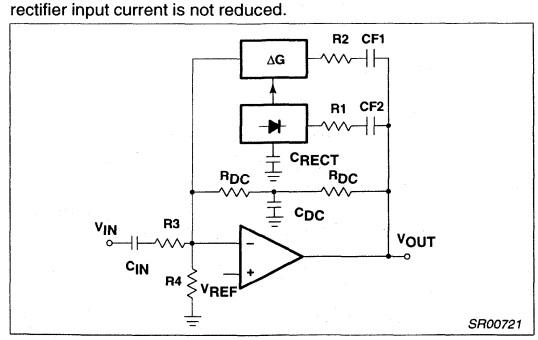


Figure 2. Basic Compressor

DISTORTION TRIM

Distortion can be produced by voltage offsets in the ΔG cell. The distortion is mainly even harmonics, and drops with decreasing input signal (input signal meaning the current into the ΔG cell). The THD trim terminal provides a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 3 is suitable, as would be any other capable of delivering ±30μA into 100Ω resistor tied to 1.8V.

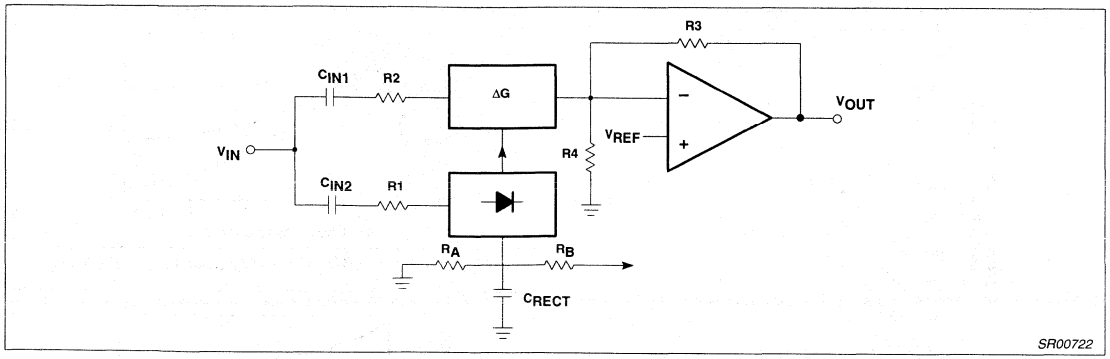


Figure 3. Expandor With Low Level Mistracking

LOW LEVEL MISTRACKING

The compandor will follow a 2-to-1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias current of <100nA that produces errors at low levels. The magnitude signal level drops to a 1μA average, the bias current will produce a 10% or 1dB error in gain. This will occur at 42dB below the maximum input level.

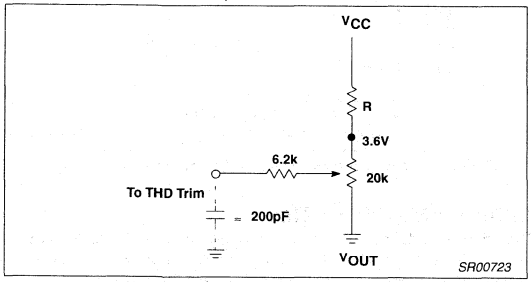


Figure 4. THD Trim Network

It is possible to deviate from the 2-to-1 transfer characteristic at low levels as shown in the circuit of Figure 4. Either R_A or R_B, (but not both), is required. The voltage on C_{RECT} is $2 \times V_{BE}$ plus V_{IN} avg. For low level inputs V_{IN} avg is negligible, so we can assume 1.3V as the bias on C_{RECT}. If R_A is placed from C_{RECT} to AND we will bleed off a current I=1.3V/R_A. If the rectifier average input current is less than this value, there will be no gain control input to the ΔG cell so that its gain will be zero and the expandor output will be zero. As the input level is raised, the input current will exceed 1.3V/R_A and the expandor output will become active. For large input signals, R_A will have little effect. The result of this is that we will deviate from the 2-to-1 expansion, present at high levels, to an infinite expansion at low levels where the output shuts off completely. Figure 5 shows some examples of tracking curves which can be obtained. Complementary curves would be obtained for a compressor, where at low level signals the result would be infinite compression. The bleed current through R_A will be a function of temperature because of the two V_{BE} drops, so the low level tracking will drift with temperature. If a negative supply is available, if would be desirable to tie R_A to that, rather than ground, and to increase its value accordingly. The bleed current will then be less sensitive to the V_{BE} temperature drift.

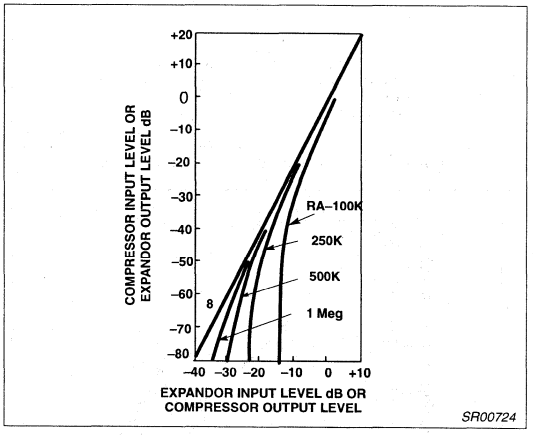


Figure 5. Mistracking With R_A

R_B will supply an extra current to the rectifier equal to $(V_{CC}–1.3V)R_B$. In this case, the expandor transfer characteristic will deviate towards 1-to-1 at low levels. At low levels the expandor gain will stop dropping and the expansion will cease. In a compressor, this would lead to a lack of compression at low levels. Figure 6 shows some typical transfer curves. An R_B value of approximately 2.5M would trim the low level tracking so as to match the Bell system N2 trunk compandor characteristic.

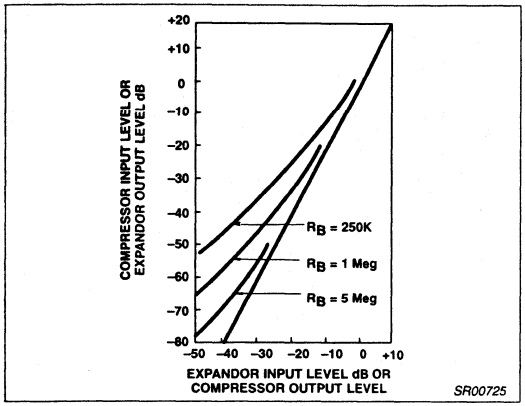


Figure 6. Mistracking With R_B

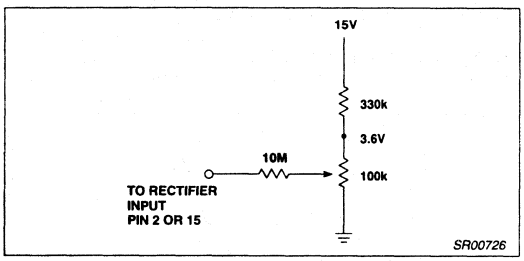


Figure 7. Rectifier Bias Current Compensation

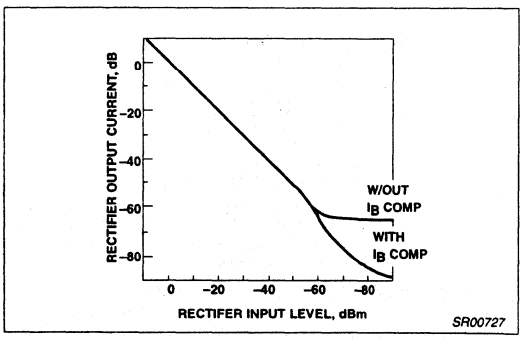


Figure 8. Rectifier Performance With Bias Current Compensation

RECTIFIER BIAS CURRENT CANCELLATION

The rectifier has an input bias current of between 50 and 100nA. This limits the dynamic range of the rectifier to about 60dB. It also limits the amount of attenuation of the ΔG cell. The rectifier dynamic range may be increased by about 20dB by the bias current trim network shown in Figure 7. Figure 8 shows the rectifier performance with and without bias current cancellation.

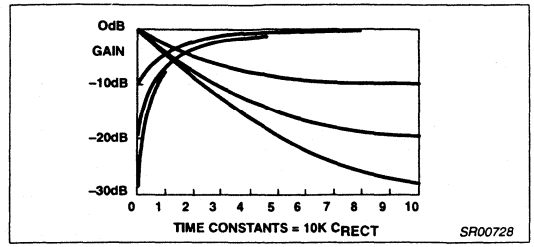


Figure 9. Gain vs Time Input Steps of ±10, ±20, ±30dB

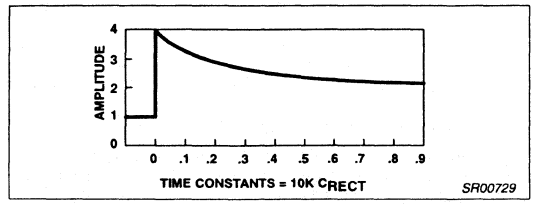


Figure 10. Compressor Attack Envelope +12dB Step

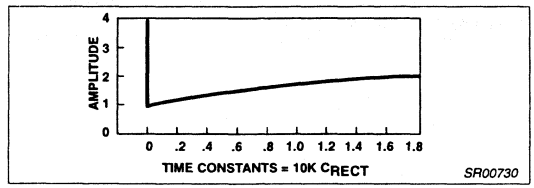


Figure 11. Compressor Release Envelope −12dB Step

ATTACK AND DECAY TIME

The attack and decay times of the compandor are determined by the rectifier filter time constant $10k \times C_{RECT}$. Figure 9 shows how the gain will change when the input signal undergoes a 10, 20, or 30dB change in level.

The attack time is much faster than the decay, which is desirable in most applications. Figure 10 shows the compressor attack envelope for a +12dB step in input level. The initial output level of 1 unit instantaneously rises to 4 units, and then starts to fall towards its final value of 2 units. The CCITT recommendation on attack and decay times for telephone system compandors defines the attack time as when the envelope has fallen to a level of 3 units, corresponding to t=0.15 in the figure. The CCITT recommends an attack time of 3 ±2ms, which suggests an RC product of 20ms. Figure 11 shows the compressor output envelope when the input level is suddenly reduced 12dB. The output, initially at a level of 4 units, drops 12dB to 1 unit and then rises to its final value of 2 units. The CCITT defines release time as when the output has risen to 1.5 units, and suggests a value of 13.5 ±9ms. This corresponds to t=0.675 in the figure, which again suggests a 20ms RC product. Since R_1=10k, the CCITT recommendations will be met if C_{RECT}=2μF.

There is a trade-off between fast response and low distortion. If a small C_{RECT} is used to get very fast attack and decay, some ripple

will appear on the gain control line and produce distortion. As a rule, a 1μF C_{RECT} will produce 0.2% distortion at 1kHz. The distortion is inversely proportional to both frequency and capacitance. Thus, for telephone applications where C_{RECT}=2μF, the ripple would cause 0.1% distortion at 1kHz and 0.33% at 800Hz. The low frequency distortion generated by a compressor would be cancelled (or undistorted) by an expandor, providing that they have the same value of C_{RECT}.

FAST ATTACK, SLOW RELEASE HARD LIMITER

The NE570/571 can be easily used to make an excellent limiter. Figure 12 shows a typical circuit which requires of an NE570/571, of an LM339 quad comparator, and a PNP transistor. For small signals, the ΔG cell is nearly off, and the circuit runs at unity gain as set by R_8, R_7. When the output signal tries to exceed a + or −1V peak, a comparator threshold is exceeded. The PNP is turned on and rapidly charges C_4 which activates the ΔG cell. Negative feedback through the ΔG cell reduces the gain and the output signal level. The attack time is set by the RC product of R_{18} and C_4, and the release time is determined by C_4 and the internal rectifier resistor, which is 10k. The circuit shown attacks in less than 1ms and has a release time constant of 100ms. R_9 trickles about 0.7μA through the rectifier to prevent C_4 from becoming completely discharged. The gain cell is activated when the voltage on Pin 1 or 16 exceeds two diode drops. If C_4 were allowed to become completely discharged, there would be a slight delay before it recharged to >1.2V and activated limiting action.

A stereo limiter can be built out of 1 NE570/571, 1 LM339 and two PNP transistors. The resistor networks R_{12}, R_{13} and R_{14}, R_{15}, which set the limiting thresholds, could be common between channels. To gang the stereo channels together (limiting in one channel will produce a corresponding gain change in the second channel to maintain the balance of the stereo image), then Pins 1 and 16 should be jumpered together. The outputs of all 4 comparators may then be tied together, and only one PNP transistor and one capacitor C_4 need be used. The release time will then be the product 5kxC_4 since two channels are being supplied current from C_4.

USE OF EXTERNAL OP AMP

The operational amplifiers in the NE570/571 are not adequate for some applications.

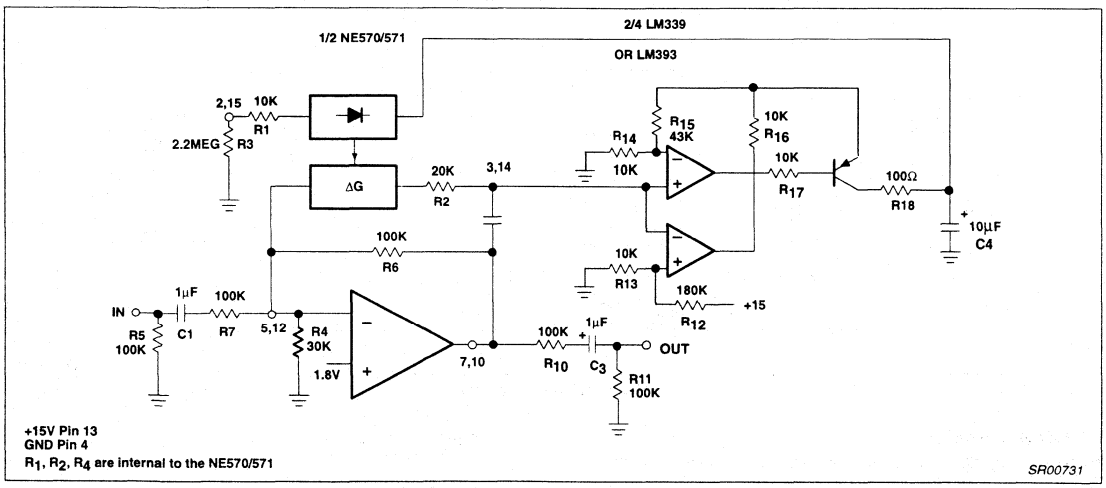


Figure 12. Fast Attack, Slow Release Hard Limiter

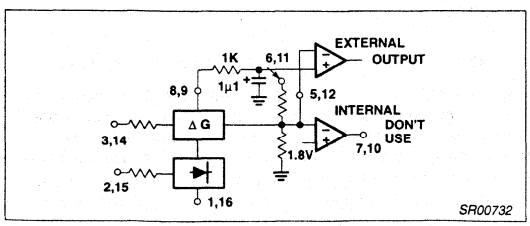


Figure 13. Use of External Op Amp

The slew rate, bandwidth, noise, and output drive capability can limit performance in many systems. For best performance, an external op amp can be used. The external op amp may be powered by bipolar supplies for a larger output swing.

Figure 13 shows how an external op amp may be connected. The non-inverting input must be biased at about 1.8V. This is easily accomplished by tying it to either Pin 8 or 9, the THD trim pins, since these pins sit at 1.8V. An optional RC decoupling network is shown which will filter out the noise from the NE570/571 reference (typically about 10μV in 20kHz BW). The inverting input of the external op amp is tied to the inverting input of the internal op amp. The output of the external op amp is then used, with the internal op amp output left to float. If the external op amp is used single supply (+V_{CC} and ground), it must have an input common-mode range down to less than 1.8V.

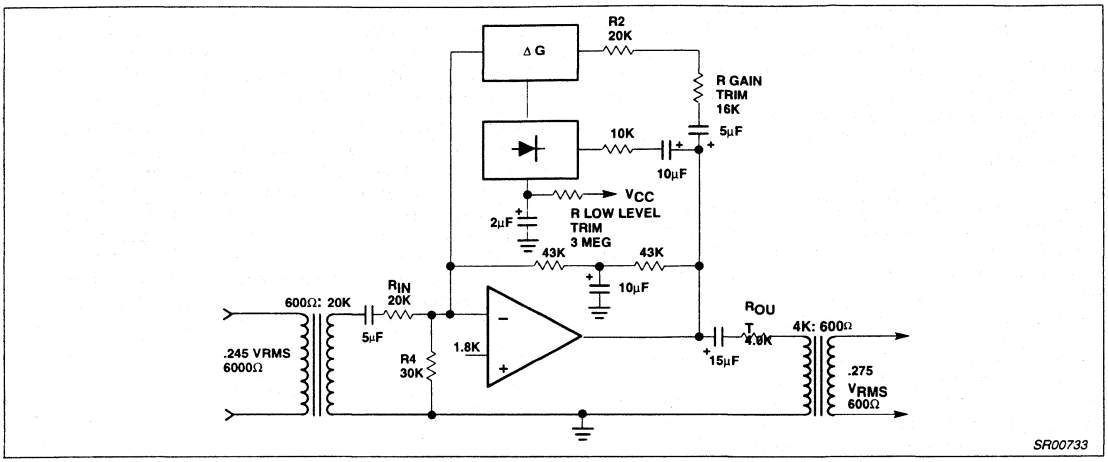


Figure 14. N2 Compressor

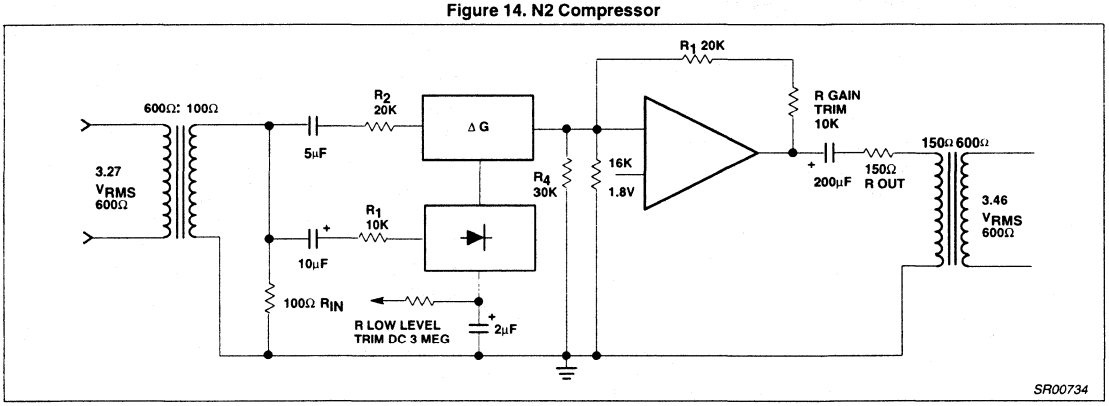


Figure 15. N2 Expandor

N2 COMPANDOR

There are four primary considerations involved in the application of the NE570/571 in an N2 compandor. These are matching of input and output levels, accurate 600Ω input and output impedances, conformance to the Bell system low level tracking curve, and proper attack and release times.

Figure 14 shows the implementation of an N2 compressor. The input level of $0.245V_{RMS}$ is

stepped up to $1.41V_{RMS}$ by the 600Ω: 20kΩ matching transformer. The 20k input resistor properly terminates the transformer. An internal 20kΩ resistor (R_3) is provided, but for accurate impedance termination an external resistor should be used. The output impedance is provided by the 4kΩ output resistor and the 4kΩ: 600Ω output transformer.

The $0.275V_{RMS}$ output level requires a 1.4V op amp output level. This can be provided by increasing the value of R_2 with an external resistor, which can be selected to fine trim the gain. A rearrangement of the compressor gain equation (6) allows us to determine the value for R_2.

$$R_2 = \frac{\text{Gain}^2 \times 2 \times R_3 \times V_{IN\ avg}}{R_1 \times I_B}$$

$$= \frac{1^2 \times 2 \times 20k \times 1.27}{10k \times 140\mu A}$$

$$= 36.3k$$

The external resistance required will thus be 36.3k–20k=16.3k.

The Bell-compatible low level tracking characteristic is provided by the low level trim resistor from C_{RECT} to V_{CC}. As shown in Figure 6, this will skew the system to a 1:1 transfer characteristic at low levels. The 2μF rectifier capacitor provides attack and release times of 3ms and 13.5ms, respectively, as shown in Figures 10 and 11. The R-C-R network around the op amp provides DC feedback to bias the output at DC.

An N2 expandor is shown in Figure 15. The input level of $3.27V_{RMS}$ is stepped down to 1.33V by the 600Ω:100Ω transformer, which is terminated with a 100Ω resistor for accurate impedance matching. The output impedance is accurately set by the 150Ω output resistor

and the 150Ω:600Ω output transformer. With this configuration, the 3.46V transformer output requires a 3.46V op amp output. To obtain this output level, it is necessary to increase the value of R_3 with an external trim resistor. The new value of R_3 can be found with the expandor gain equation

$$R_3 = \frac{R_1\ R_2\ I_B\ \text{Gain}}{2\ V_{IN}\ \text{avg}}$$

$$= \frac{10\text{k} \times 20\text{k} \times 140\mu\text{A} \times 2.6}{2 \times 1.20}$$

$$= 30.3\text{k}$$

An external addition to R_3 of 10k is required, and this value can be selected to accurately set the high level gain.

A low level trim resistor from C_{RECT} to V_{CC} of about 3M provides matching of the Bell low-level tracking curve, and the 2μF value of C_{RECT} provides the proper attack and release times. A 16k resistor from the summing node to ground biases the output to $7V_{DC}$.

VOLTAGE-CONTROLLED ATTENUATOR

The variable gain cell in the NE570/571 may be used as the heart of a high quality voltage-controlled amplifier (VCA). Figure 16 shows a typical circuit which uses an external op amp for better performance, and an exponential converter to get a control characteristic of –6dB/V. Trim networks are shown to null out distortion and DC shift, and to fine trim gain to 0dB with 0V of control voltage.

Op amp A_2 and transistors Q_1 and Q_2 form the exponential converter generating an exponential gain control current, which is fed into the rectifier. A reference current of 150μA, (15V and R_{20}=100k), is attenuated a factor of two (6dB) for every volt increase in the control voltage. Capacitor C_6 slows down gain changes to a 20ms time constant ($C_6 \times R_1$) so that an abrupt change in the control voltage will produce a smooth sounding gain change. R_{18} assures that for large control voltages the circuit will go to full attenuation. The rectifier bias current would normally limit the gain reduction to about 70dB. R_{18} draws excess current out of the rectifier. After approximately 50dB of attenuation at a –6dB/V slope, the slope steepens and attenuation becomes much more rapid until the circuit totally shuts off at about 9V of control voltage. A_1 should be a low noise high slew rate op amp. R_{13} and R_{14} establish approximately a 0V bias at A_1's output.

With a 0V control voltage, R_{19} should be adjusted for 0dB gain. At 1V(–6dB gain) R_9 should be adjusted for minimum distortion with a large (+10dBm) input signal. The output DC bias (A_1 output) should be measured at full attenuation (+10V control voltage) and then R_8 is adjusted to give the same value at 0dB gain. Properly adjusted, the circuit will give typically less than 0.1% distortion at any gain with a DC output voltage variation of only a few millivolts. The clipping level (140μA into Pin 3, 14) is ±10V peak. A signal-to-noise ratio of 90dB can be obtained.

If several VCAs must track each other, a common exponential converter can be used. Transistors can simply be added in parallel with Q_2 to control the other channels. The transistors should be maintained at the same temperature for best tracking.

AUTOMATIC LEVEL CONTROL

The NE570 can be used to make a very high performance ALC as shown in Figure 17. This circuit hook-up is very similar to the basic compressor shown in Figure 2 except that the rectifier input is tied to the input rather than the output. This makes gain inversely proportional to input level so that a 20dB drop in input level will produce a 20dB increase in gain. The output will remain fixed at a constant level. As shown, the circuit will maintain an output level of ±1dB for an input range of +14 to –43dB at 1kHz. Additional external components will allow the output level to be adjusted. Some relevant design equations are:

$$\text{Output level} = \frac{R_1\ R_2\ I_B}{2\ R_3}\left(\frac{V_{IN}}{V_{IN}\ (\text{avg})}\right)$$

$$I_B = 140\text{mA}$$

$$\text{Gain} = \frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (\text{avg})} \quad \text{where}$$

$$\frac{V_{IN}}{V_{IN}\ (\text{avg}} = \frac{\pi}{2\sqrt{2}} = 1.11 \text{ (for sine wave)}$$

If ALC action at very low input levels is not desired, the addition of resistor R_X will limit the maximum gain of the circuit.

$$\text{Gain max} = \frac{\frac{R_1 + R_X}{1.8V} \times R_2 \times I_B}{2\ R_3}$$

The time constant of the circuit is determined by the rectifier capacitor, C_{RECT}, and an internal 10k resistor.

$\tau = 10\text{k}\ C_{RECT}$

Response time can be made faster at the expense of distortion. Distortion can be approximated by the equation:

$$\text{THD} = \left(\frac{1\mu\text{F}}{C_{RECT}}\right)\left(\frac{1\text{kHz}}{\text{freq.}}\right) \times 0.2\%$$

VARIABLE SLOPE COMPRESSOR-EXPANDOR

Compression and expansion ratios other than 2:1 can be achieved by the circuit shown in Figure 18. Rotation of the dual potentiometer causes the circuit hook-up to change from a basic compressor to a basic expandor. In the center of rotation, the circuit is 1:1, has neither compression nor expansion. The (input) output transfer characteristic is thus continuously variable from 2:1 compression, through 1:1 up to 1:2 expansion. If a fixed compression or expansion ratio is desired, proper selection of fixed resistors can be used instead of the potentiometer. The optional threshold resistor will make the compression or expansion ratio deviate towards 1:1 at low levels. A wide variety of (input) output characteristics can be created with this circuit, some of which are shown in Figure 18.

HI-FI COMPANDOR

The NE570 can be used to construct a high performance compandor suitable for use with music. This type of system can be used for noise reduction in tape recorders, transmission systems, bucket brigade delay lines, and digital audio systems. The circuits to be described contain features which improve performance, but are not required for all applications.

A major problem with the simple NE570 compressor (Figure 2) is the limited op amp gain at high frequencies.

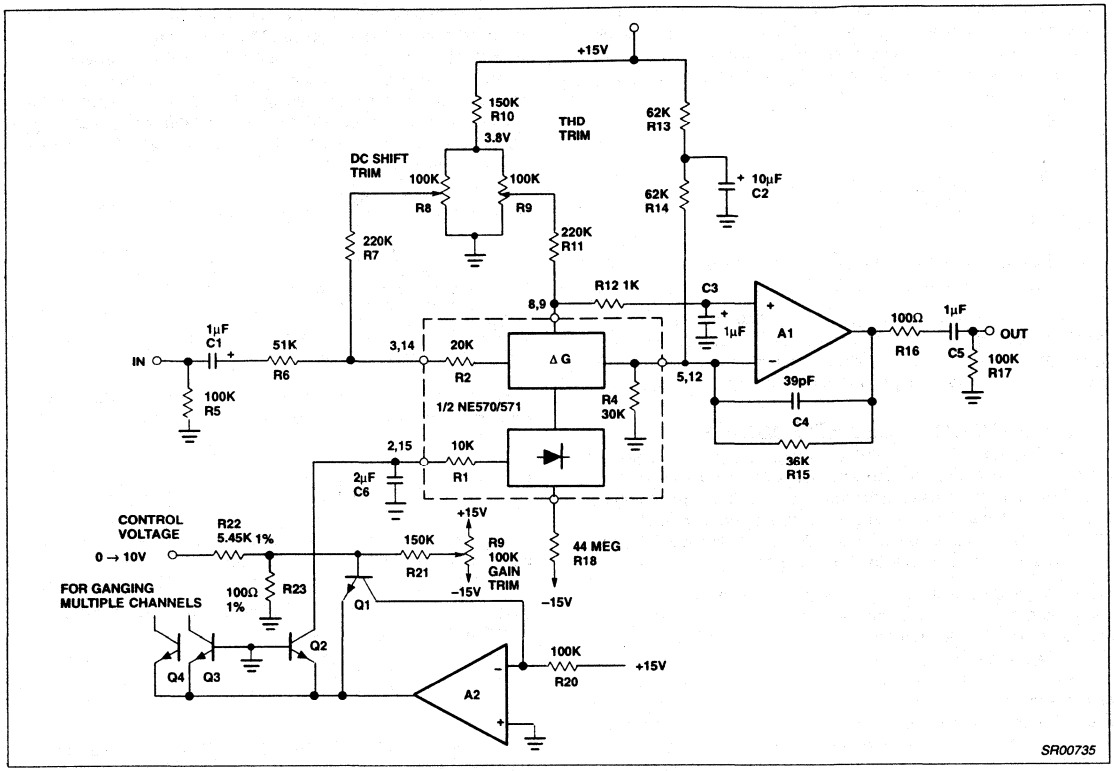


Figure 16. Voltage-Controlled Attenuator

For weak input signals, the compressor circuit operates at high gain and the 570 op amp simply runs out of loop gain. Another problem with the 570 op amp is its limited slew rate of about 0.6V/µs. This is a limitation of the expandor, since the expandor is more likely to produce large output signals than a compressor.

Figure 20 is a circuit for a high fidelity compressor which uses an external op amp and has a high gain and wide bandwidth. An input compensation network is required for stability.

Another feature of the circuit in Figure 20 is that the rectifier capacitor (C_9) is not grounded, but is tied to the output of an op amp circuit. This circuit, built around an LM324, speeds up the compressor attack time at low signal levels. The response times of the simple expandor and compressor (Figures 1 and 2) become longer at low signal levels. The time constant is not simply $10k \times C_{RECT}$, but is really:

$$\left(10k + 2\left(\frac{0.026V}{I_{RECT}}\right)\right) \times C_{RECT}$$

When the rectifier input level drops from 0dBm to –30dBm, the time constant increases from $10.7k \times C_{RECT}$ to $32.6k \times C_{RECT}$. In systems where there is unity gain between the compressor and expandor, this will cause no overall error. Gain or loss between the compressor and expandor will be a mistracking of low signal dynamics. The circuit with the LM324 will greatly reduce this problem for systems which cannot guarantee the unity gain.

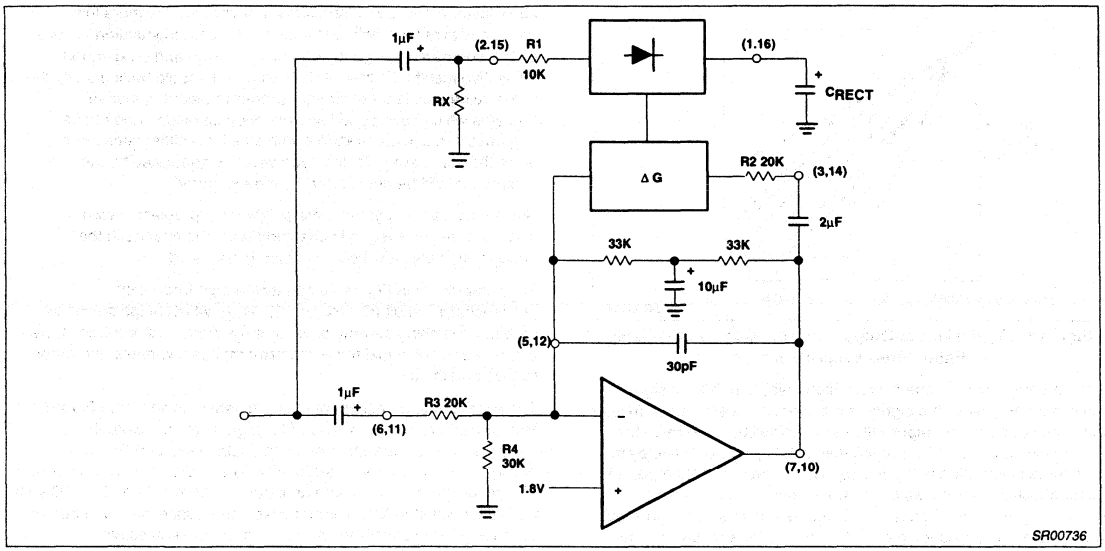


Figure 17. Automatic Level Control

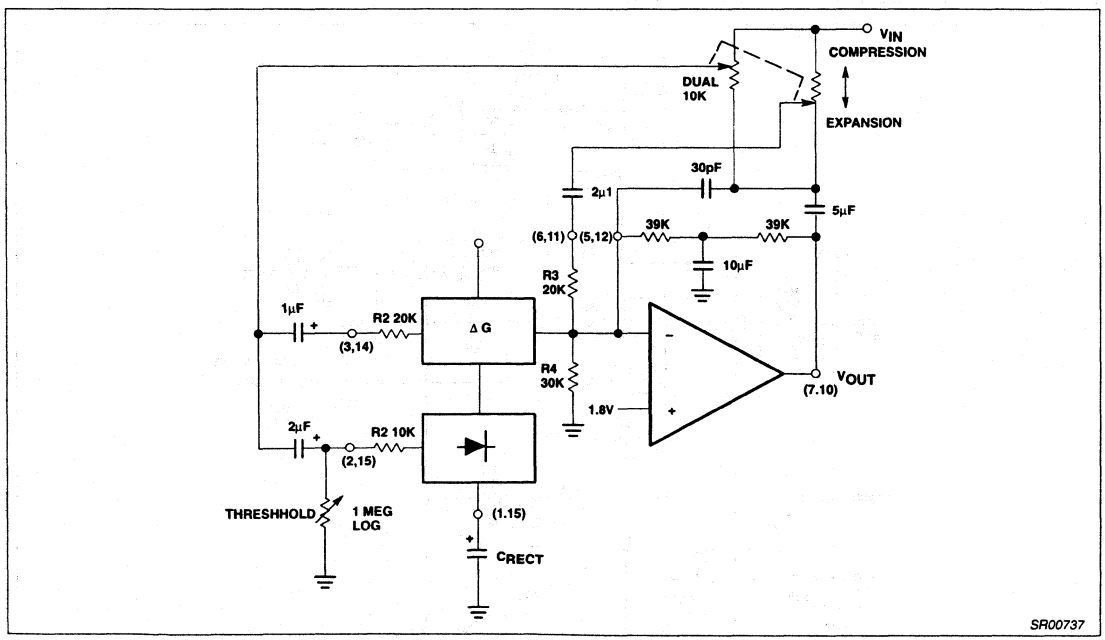


Figure 18. Variable Slope Compressor-Expandor

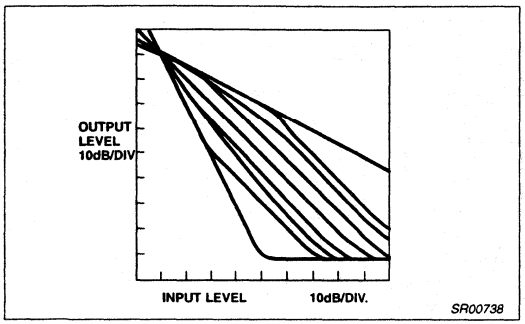


Figure 19. Typical Input-Output Tracking Curves of Variable Ratio Compressor-Expandor

When a compressor is operating at high gain, (small input signal), and is suddenly hit with a signal, it will overload until it can reduce its gain. Overloaded, the output will attempt to swing rail to rail. This compressor is limited to approximately a $7V_{P-P}$ output swing by the brute force clamp diodes D_3 and D_4. The diodes cannot be placed in the feedback loop because their capacitance would limit high frequency gain. The purpose of limiting the output swing is to avoid overloading any succeeding circuit such as a tape recorder input.

The time it takes for the compressor to recover from overload is determined by the rectifier capacitor C_9. A smaller capacitor will allow faster response to transients, but will produce more low frequency third harmonic distortion due to gain modulation. A value of 1µF seems to be a good compromise value and yields good subjective results. Of course, the expandor should have exactly the same value rectifier capacitor for proper transient response. Systems which have good low frequency amplitude and phase response can use compandors with smaller rectifier capacitors, since the third harmonic distortion which is generated by the compressor will be undistorted by the expandor.

Simple compandor systems are subject to a problem known as breathing. As the system is changing gain, the change in the background noise level can sometimes be heard.

The compressor in Figure 20 contains a high frequency pre-emphasis circuit (C_2, R_5 and C_8, R_{14}), which helps solve this problem. Matching de-emphasis on the expandor is required. More complex designs could make the pre-emphasis variable and further reduce breathing.

The expandor to complement the compressor is shown in Figure 21. Here an external op amp is used for high slew rate. Both the compressor and expandor have unity gain levels of 0dB. Trim networks are shown for distortion (THD) and DC shift. The distortion trim should be done first, with an input of 0dB at 10kHz. The DC shift should be adjusted for minimum envelope bounce with tone bursts. When applied to consumer tape recorders, the subjective performance of this system is excellent.

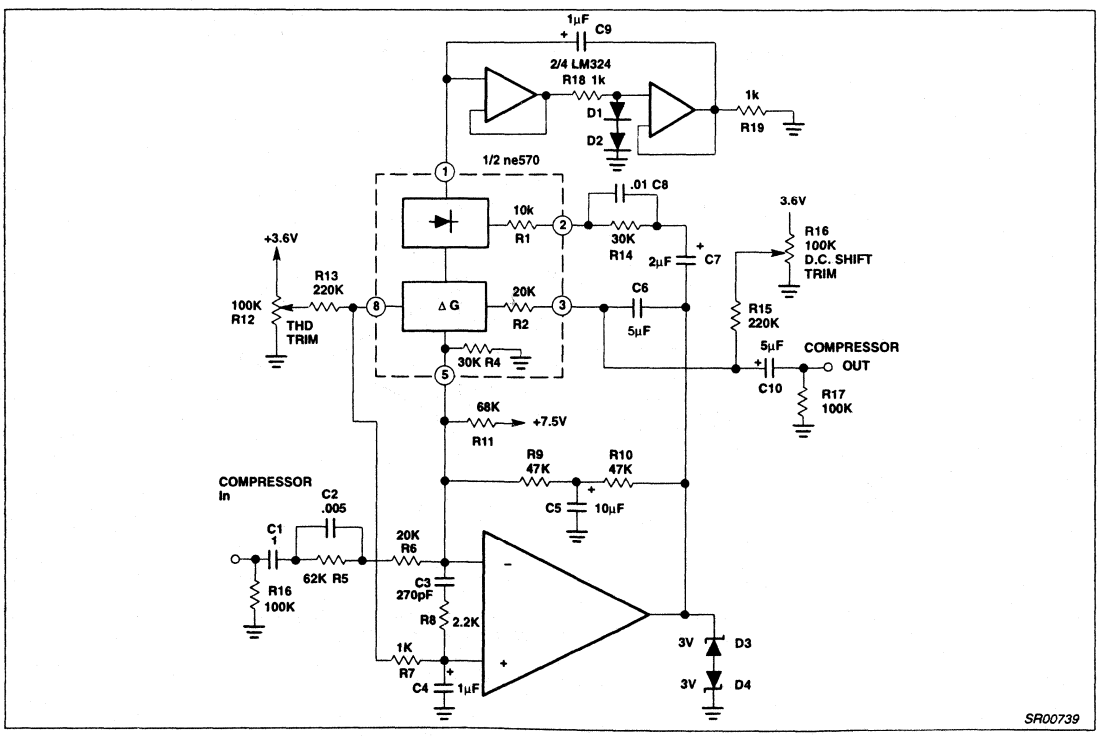


Figure 20. Hi-Fi Compressor With Pre-emphasis

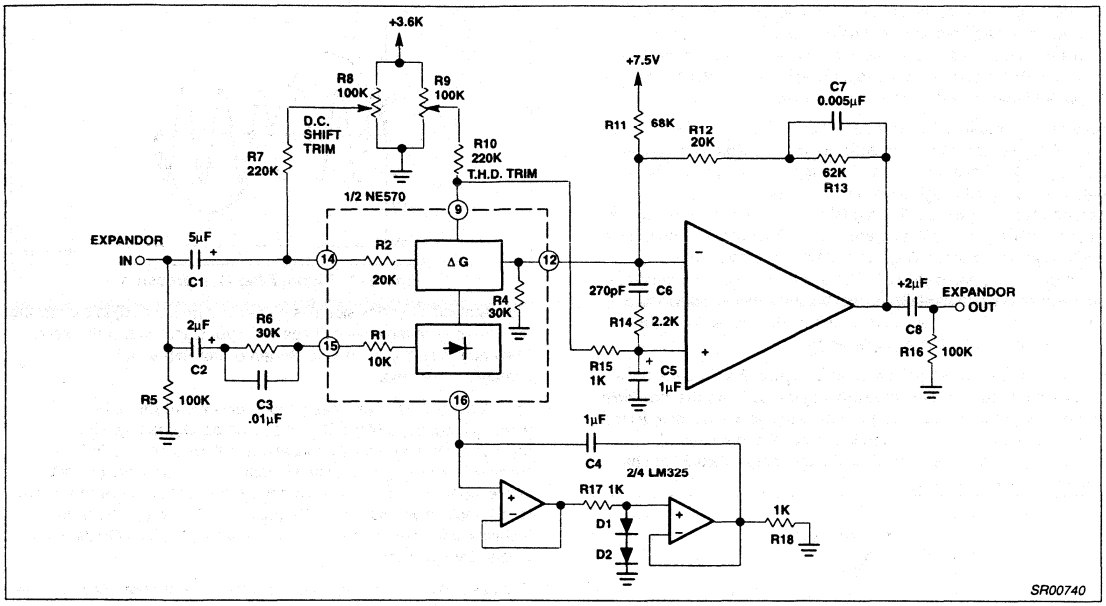


Figure 21. Hi-Fi Expandor With De-emphasis

Compandor cookbook AN176

Compandors are versatile, low cost, dual-channel gain control devices for audio frequencies. They are used in tape decks, cordless telephones, and wireless microphones performing noise reduction. Electronic organs, modems and mobile telephone equipment use compandors for signal level control.

So what is companding? Why do it at all? What happens when we do it? Compandor is the contraction of the two words compressor and expandor. There is one basic reason to compress a signal before sending it through a telephone line or recording it on a cassette tape: to process that signal (music, speech, data) so that all parts of it are above the inherent noise floor of the transmission medium and yet not running into the max. dynamic range limits, causing clipping and distortion. The diagrams below demonstrate the idea; they are not totally correct because in the real world of electronics the 3kHz tone is riding on the 1kHz tone. They are shown separated for better explanation.

Figure 1 is the signal from the source. Figure 2 shows the noise always in the transmission medium. Figure 3 shows the max limits of the transmission medium and what happens when a signal larger than those limits is sent through it. Figure 4 is the result of compressing the signal (note that the larger signal would not be clipped when transmitted).

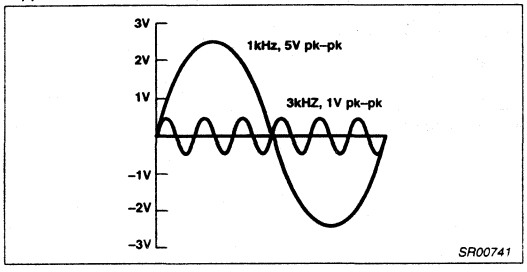


Figure 1. Original Signal Input

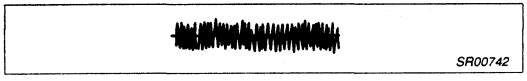


Figure 2. Wide-Band Noise Floor of Transmission Line

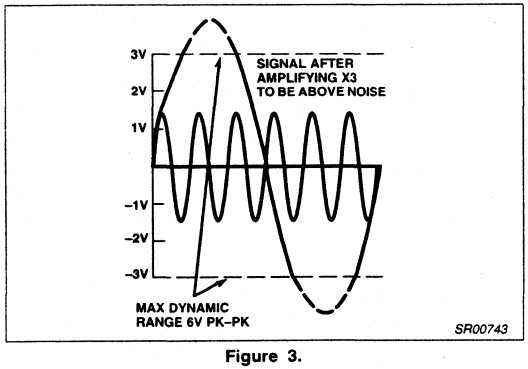


Figure 3.

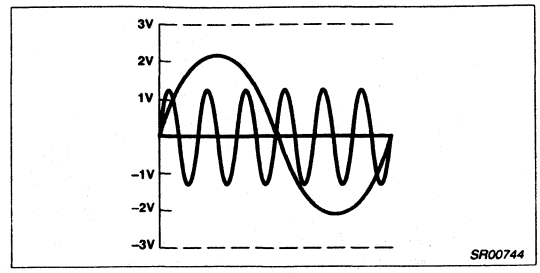


Figure 4. Signal After Compression

The received/playback signal is processed (expanded) in exactly the same — only inverted — ratio as the input signal was compressed. The end result is a clean, undistorted signal with a high signal-to-noise ratio.

This document has been designed to give the reader a basic working knowledge of the Signetics Compandor family. The analyses of three primary applications will be accompanied by "recipes" describing how to select external components (for both proper operation and function modification). Schematic and artwork for an application board are also provided. For comprehensive technical information consult the Compandor Product Guide or the Linear Data Manual.

The basic blocks in a compandor are the current-controlled variable gain cell (ΔG), voltage-to-current converter (rectifier), and operational amplifier. Each Signetics compandor package has two identical, independent channels with the following block diagrams (notice that the 570/71 is different from the 572).

The operational amplifier is the main signal path and output drive.

BLOCK DIAGRAMS

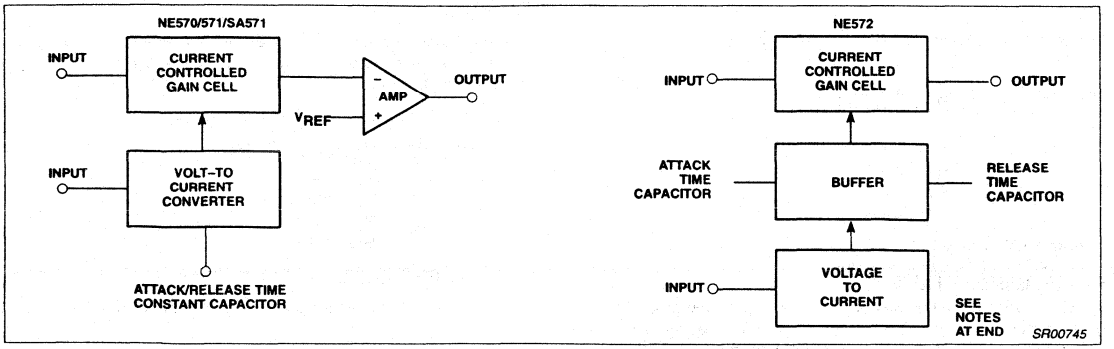


Figure 5. Block Diagrams

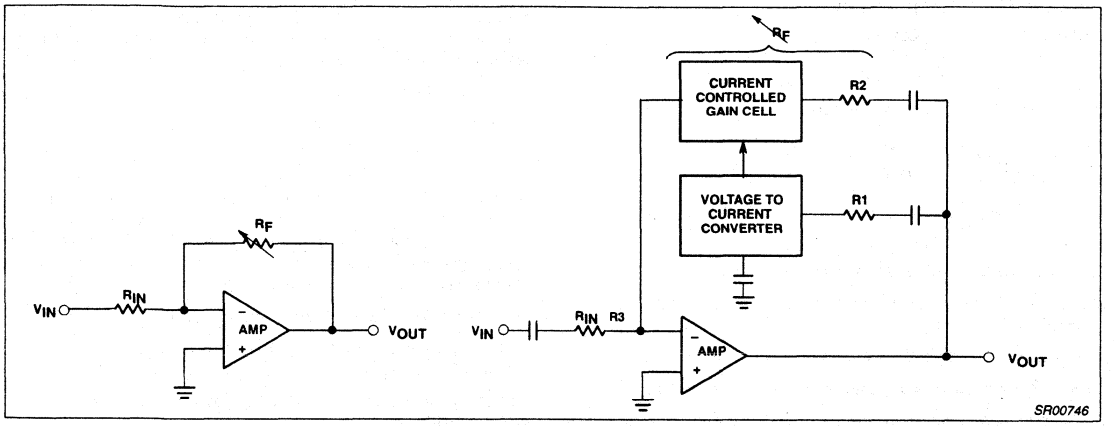


Figure 6. Basic Compressor

The full-wave averaging rectifier measures the AC amplitude of a signal and develops a control current for the variable gain cell.

The variable gain cell uses the rectifier control current to provide variable gain control for the operational amplifier gain block.

The compandor can function as a Compressor, Expandor, and Automatic Level Controller or as a complete compressor/expandor system as described in the following:

1) The COMPRESSOR function processes uncontrolled input signals into controlled output signals. The purpose of this is to avoid distortion caused by a narrow dynamic range medium, such as telephone lines, RF and satellite transmissions, and magnetic tape. The Compressor can also limit the level of a signal.

2) The EXPANDOR function allows a user to increase the dynamic range of an incoming compressed signal such as radio broadcasts.

3) The compressor/expandor system allows a user to retain dynamic range and reduce the effects of noise introduced by the transmission medium.

4) The AUTOMATIC LEVEL CONTROL (ALC) function (like the familiar automatic gain control) adjusts its gain proportionally with the input amplitude. This ALC circuit therefore transforms a widely varying input signal into a fixed amplitude output signal without clipping and distortion.

HOW TO DESIGN COMPANDOR CIRCUITS

The rest of the cookbook will provide you with basic compressor, expandor, and automatic level control application information. A NE570/571 has been used in all of the circuits. If high-fidelity audio or separately programmable attack and decay time are needed, the NE572 with a low noise op amp should be used.

The compressor (see Figure 6) utilizes all basic building blocks of the compandor. In this configuration, the variable gain cell is placed in the feedback loop of the standard inverting amplifier circuit. The gain equation is $A_V = -R_F/R_{IN}$. As shown above, the variable gain cell acts as a variable feedback resistor (R_F) (See Figure 6).

As the input signal increases above the crossover level of 0dB, the variable resistor decreases in value. This causes the gain to decrease, thus limiting the output amplitude.

Below the crossover level of 0dB, an increase in input signal causes the variable resistor to increase in value, thereby causing the output signal's amplitude to increase.

In the compressor configuration, the rectifier is connected to the output.

The complete equation for the compressor gain is:

$$\text{Gain comp.} = \left[\frac{R_1 R_2 I_B}{2 R_3 V_{IN}(avg)}\right]^{\frac{1}{2}}$$

where: $R_1 = 10k$
$R_2 = 20k$
$R_3 = 20k$
$I_B = 140\mu A$

$V_{IN}(avg)=0.9(V_{IN(RMS)})$

COMPRESSOR RECIPE

1) DC bias the output half way between the supply and ground to get maximum headroom. The circuit in Figure 7 is designed around a system supply of 6V, thus the output DC level should be 3V.

$V_{OUT\ DC}=(1+(2R_{DC}/R_4))\ V_{REF}$

where: $R_4=30k$
$V_{REF}=1.8V$
R_{DC} is external

manipulating the equation, the result is. . .

$$R_{DC} = \left(\left(\frac{V_{OUT}}{V_{REF}}\right) - 1\right)\frac{R_4}{2}$$

Note that the $C_{(DC)}$ should be large enough to totally short out any AC in this feedback loop.

2) Analyze the OUTPUT signal's anticipated amplitude.

a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

b) if larger than 3.0V peak, R_1 will also need to be increased.

By limiting the peak input currents we avoid signal distortion.

3) The input and output coupling caps need to be large enough not to attenuate any desired frequencies ($X_C=1/(6.28xf)$).
4) The C_{RECT} should be 1µF to 2µF for initial setup. This directly affects Attack and Release times.
5) An input buffer may be necessary if the source's output impedance needs matching.
6) Pre-emphasis may be used to reduce noisepumping, breathing, etc., if present. See the NE570/571 data sheet for specific details.
7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. Refer to data sheet for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.

8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network. (This technique prevents infinite compression at low input levels.)

The EXPANDOR utilizes all the basic building blocks of the compandor (see Figure 8). In this configuration the variable gain cell is placed in the inverting input lead of the operational amplifier and acts as a variable input resistance, R_{IN}. The basic gain equation for operational amplifiers in the standard inverting feedback loop is $A_V=-R_F/R_{IN}$.

As the input amplitude increases above the crossover level of 0dBM, this variable resistor decreases in value, causing the gain to increase, thus forcing the output amplitude to increase (refer to Figure 11).

Below the crossover level, an increase in input amplitude causes the variable resistor to increase in value, thus forcing the output amplitude to decrease.

The complete equation for the expandor gain is:

Gain expandor=$(2R_3V_{IN}(avg))/R_1R_2I_B$

where: $R_1 = 10k$
$R_2 = 20k$
$R_3 = 20k$
$I_B = 140\mu A$

$V_{IN}(avg)=0.9\ (V_{IN(RMS)})$

In the expandor configuration the rectifier is connected to the input.

EXPANDOR RECIPE

1) DC bias the output halfway between the supply and ground to get maximum headroom. The circuit in Figure 9 is designed around a system supply of 6V so the output DC level should be 3V.

$V_{OUT\ DC}=(1+R_3/R_4)V_{REF}$

where: $R_3 = 20k$
$R_4 = 30k$
$V_{REF} = 1.8V$

Note that when using a supply voltage higher than 6V the DC output level should be adjusted. To increase the DC output level, it is recommended that R_4 be decreased by adding parallel resistance to it. (Changing R_3 would also affect the expandor's AC gain and thus cause a mismatch in a companding system.)

2) Analyze the input signal's anticipated amplitude:

a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

b) if larger than 3.0V peak, R_1 will also need to be increased. (see INGREDIENTS)

By limiting the peak input currents we avoid signal distortion.

3) The input and output decoupling caps need to be large enough not to attenuate any desired frequencies.

4) The C_{RECT} should be 1µF to 2µF for initial setup.

5) An input buffer may be necessary if the source's output impedance needs matching.

6) De-emphasis would be necessary if the complementary compressor circuit had been pre-emphasized (as in a tape deck application). See the Hi-Fi Expandor application in the Linear Data Manual.

7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. See Linear Data Manual for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.

8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network (see Linear Data Manual). (This technique prevents infinite expansion at low input levels.)

In the ALC configuration, (Figure 10), the variable gain cell is placed in the feedback loop of the operational amplifier (as in the Compressor) and the rectifier is connected to the input.

As the input amplitude increases above the crossover point, the overall system gain decreases proportionally, holding the output amplitude constant.

As the input amplitude decreases below the crossover point, the overall system gain increases proportionally, holding the output amplitude at the same constant level.

The complete gain equation for the ALC is:

$$\text{Gain} = \frac{R_1 R_2 I_B}{2 R_3 V_{IN}\,(avg)}$$

$$\text{Output Level} = \frac{R_1 R_2 I_B}{2 R_3}\left(\frac{V_{IN}}{V_{IN}\,(avg)}\right)$$

where $\frac{V_{IN}}{V_{IN}\,(avg)} = \frac{\pi}{2\sqrt{2}} = 1.11$ (for sine wave)

Note that for very low input levels, ALC may not be desired and to limit the maximum gain, resistor R_X has been added. The modified gain equation is:

$$\text{Gain max.} = \frac{(R_1 + R_X) \cdot R_2 \cdot I_B}{2 R_3}$$

$R_X \equiv$ ((desired max gain)×26k)−10k

INGREDIENTS

[Application guidelines for internal and external components (and input/output constraints) needed to tailor (cook) each of the three entrees (applications) to your taste.]

R_1 (10kΩ) limits input current to the rectifier. This current should not exceed an AC peak value of ±300μA. An external resistor may be placed in series with R_1 if the input voltage to the rectifier will exceed ±3.0V peak (i.e., 10k×300μA=3.0V).

R_2 (20kΩ) limits input current to the variable gain cell. This current should not exceed an AC peak value of ±140μA. Again, an external resistor has to be placed in series with R_2 if the input voltage to the variable gain cell exceeds ±2.8V (i.e., 20k×140μA).

R_3 (20kΩ) acts in conjunction with R_4 as the feedback resistor (R_F) (expandor configuration) in the equation. (R_3's value can be either reduced or increased externally.) However, it is recommended that R_4 be the one to change when adjusting the output DC level.

R_4 (30kΩ) acts as the input resistor (R_{IN}) in the standard non-inverting op amp circuit. (Its value can only be reduced.)

$V_{OUT\,DC}=(1+(R_3/R_4))V_{REF}$
(for the Expandor)
$V_{OUT\,DC}=(1+(2R_{DC}/R_4))V_{REF}$
(for the Compandor, ALC)

[The purpose of these DC biasing equations is to allow the designer to set the output halfway between the supply rails for largest headroom (usually some positive voltage and ground).]

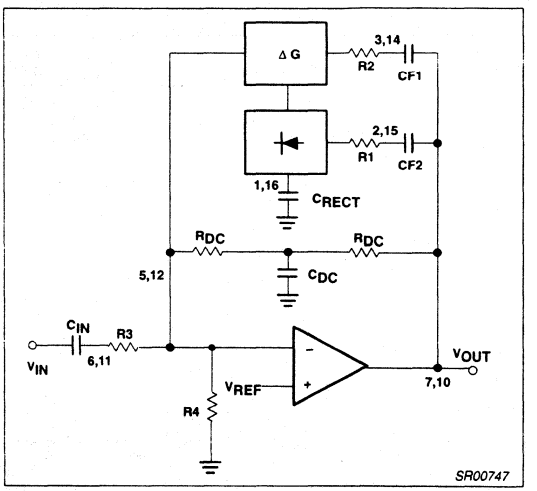


Figure 7. Basic Compressor

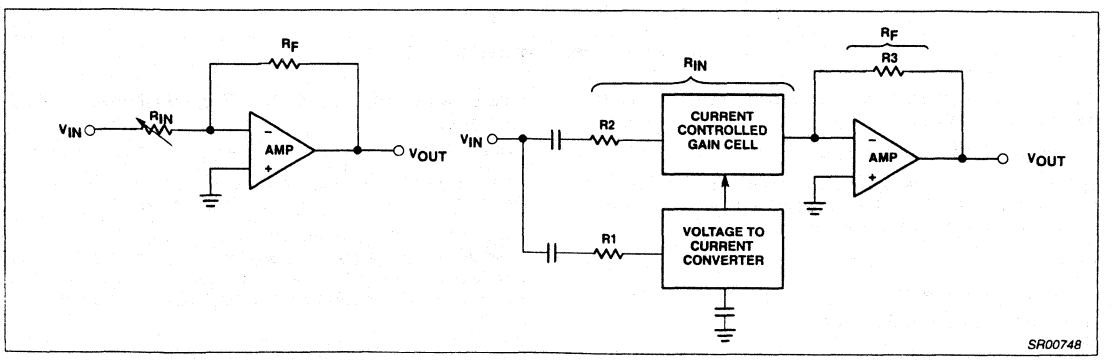


Figure 8. Basic Expandor

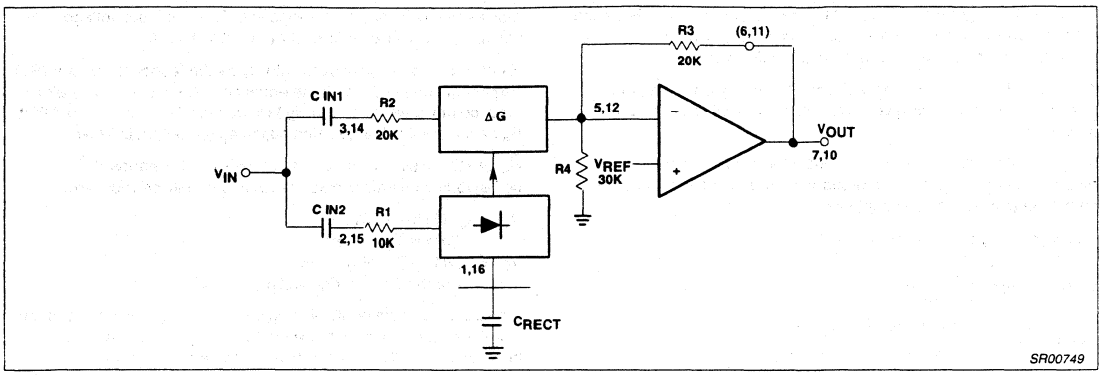


Figure 9. Basic Expandor

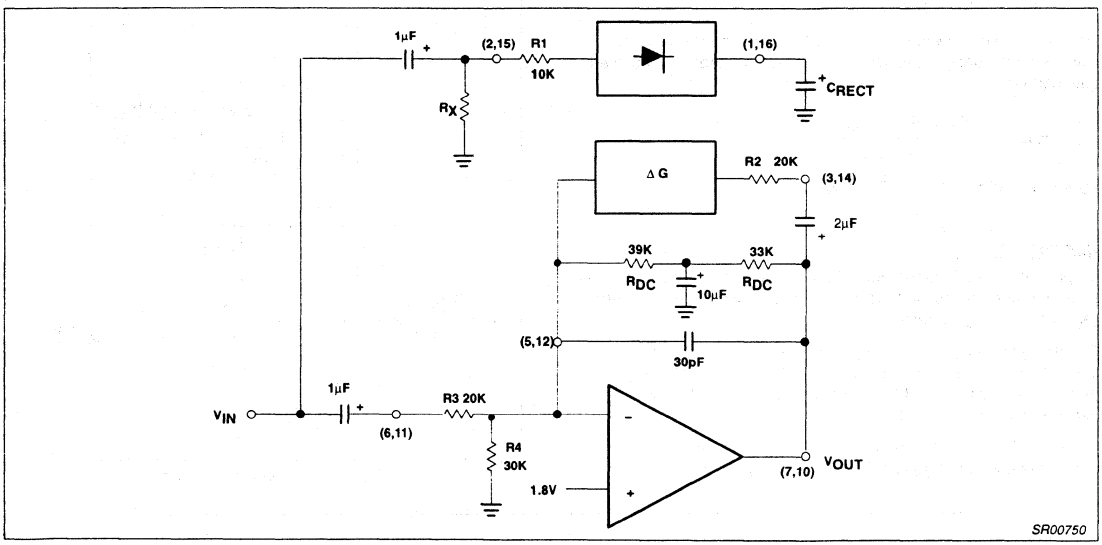


Figure 10. Automatic Level Control

C_{DC} acts as an AC shunt to ground to totally remove the DC biasing resistors from the AC gain equation.

C_F caps are AC signal coupling caps.

C_{RECT} acts as the rectifier's filter cap and directly affects the response time of the circuit. There is a trade-off, though, between fast attack and decay times and distortion.

The time constant is: $10k \times C_{RECT}$

The total harmonic distortion (THD) is approximated by:

$THD \cong (1\mu F/C_{RECT})(1kHz/freq.) \times 0.2\%$

NOTES:
The NE572 differs from the 570/571 in that:

1. There is no internal op amp.
2. The attack and release times are programmed separately.

SYSTEM LEVELS OF A COMPLETE COMPANDING SYSTEM

Figure 11 demonstrates the compressing and expanding functions:

Point A represents a wide dynamic range signal with a maximum amplitude of +16dB and minimum amplitude of –80dB.

Point B represents the compressor output showing a 2:1 reduction in dynamic range (–40dB is increased to –20dB, for example). Point B can also be seen as the dynamic range of a transmission medium. Transmission noise is present at the –60dB level from Point B to Point C.

Point C represents the input signal to the expandor.

Point D represents the output of the expandor. The signal transformation from Point C to D represents a 1:2 expansion.

Expansion and one channel of Compression (which can be switched to Automatic Level Control).

APPLICATION BOARD

Shown below is the schematic (Figure 12) for Signetics' NE570/571 evaluation/demo board. This board provides one channel of

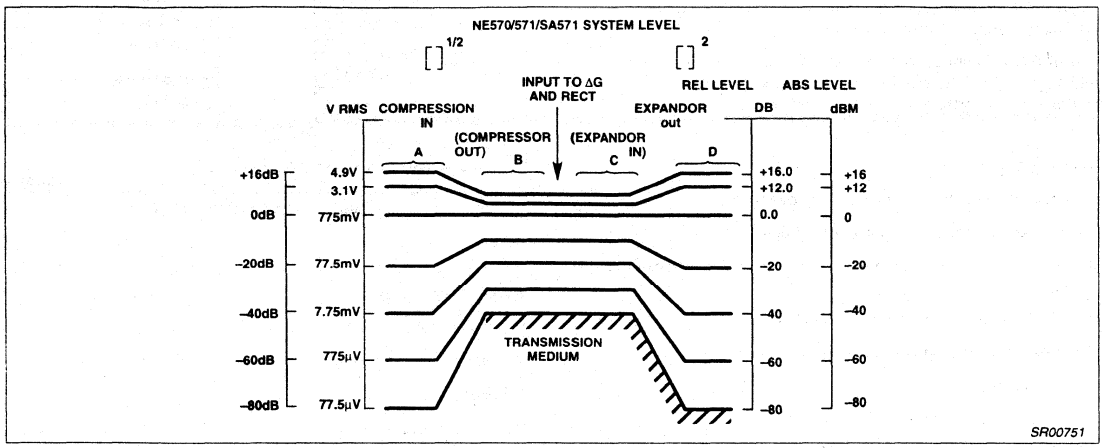


Figure 11. System Levels of a Complete Companding System

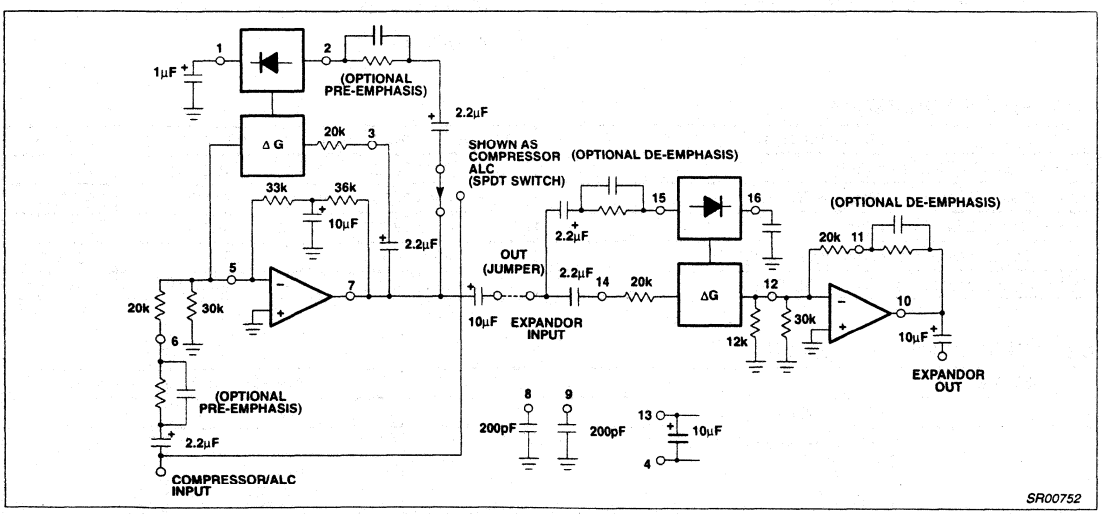


Figure 12.

Programmable analog compandor — NE/SA572

DESCRIPTION

The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- Independent control of attack and recovery time
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external op amp
- Wide dynamic range—greater than 110dB
- Temperature-compensated gain control
- Low distortion gain cell
- Low noise—6μV typical
- Wide supply voltage range—6V-22V
- System level adjustable with external components

PIN CONFIGURATION

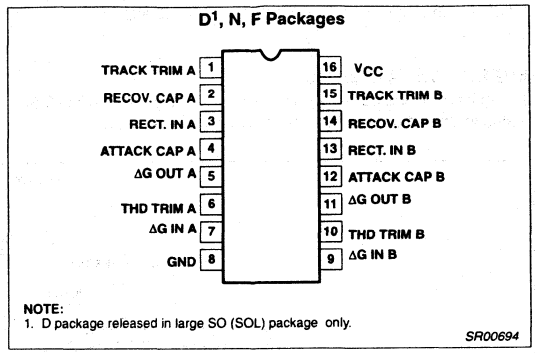


Figure 1. Pin Configuration

APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High-level limiter
- Low-level noise gate
- State variable filter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO)	0 to +70°C	NE572D	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE572N	SOT38-4
16-Pin Plastic Small Outline (SO)	–40 to +85°C	SA572D	SOT109-1
16-Pin Ceramic Dual In-Line Package (Cerdip)	–40 to +85°C	SA572F	0582B
16-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA572N	SOT38-4

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range		
	NE572	0 to +70	°C
	SA572	–40 to +85	
P_D	Power dissipation	500	mW

BLOCK DIAGRAM

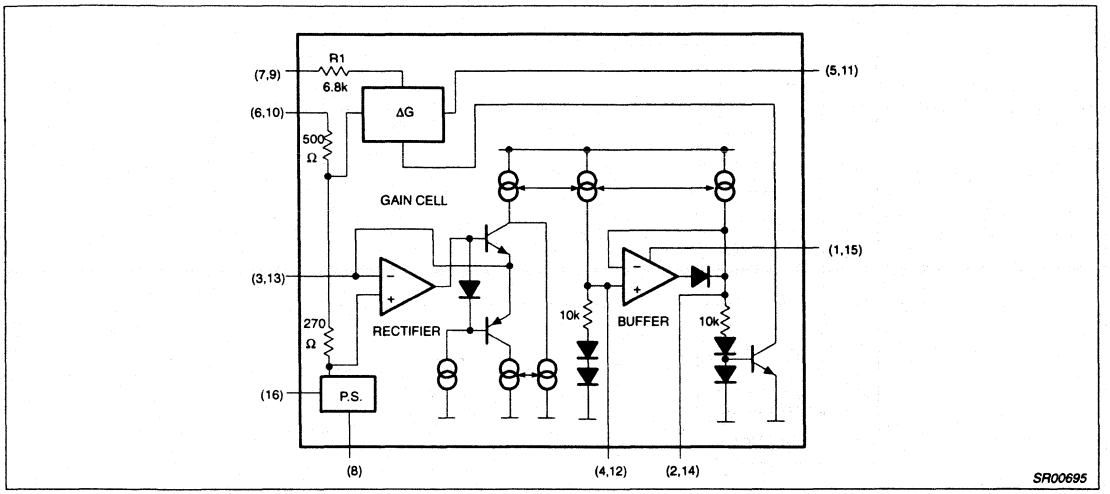


Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC}=15V, T_A=25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = 100mV$_{RMS}$ at 1kHz; $V_1 = V_2$; R_2 = 3.3kΩ; R_3 = 17.3kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	NE572			SA572			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		22	6		22	V_{DC}
I_{CC}	Supply current	No signal			6			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (untrimmed)	1kHz C_A=1.0μF		0.2	1.0		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz C_R=10μF		0.05			0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25			0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20–20kHz)		6	25		6	25	μV
	DC level shift (untrimmed)	Input change from no signal to 100mV$_{RMS}$		±20	±50		±20	±50	mV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dB
	Large–signal distortion	V_1=V_2=400mV		0.7	3.0		0.7	3	%
	Tracking error (measured relative to value at unity gain)= [V_O–V_O (unity gain)]dB –V_2dB	Rectifier input V_2=+6dB V_1=0dB V_2=–30dB V_1=0dB		±0.2 ±0.5	 –1.5 +0.8		±0.2 ±0.5	 –2.5 +1.6	dB
	Channel crosstalk	200mV$_{RMS}$ into channel A, measured output on channel B	60			60			dB
PSRR	Power supply rejection ratio	120Hz		70			70		dB

TEST CIRCUIT

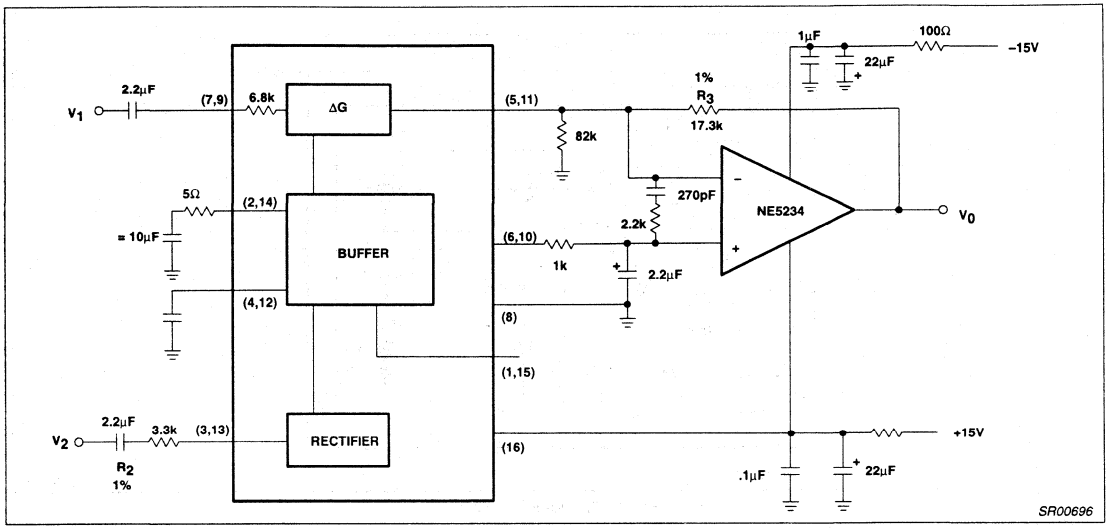


Figure 3. Test Circuit

AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1µF and 1.0µF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7µF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0µF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0-70 The SA572 is intended for applications from –40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 4 shows the circuit configuration of the gain cell. Bases of the differential pairs Q_1-Q_2 and Q_3-Q_4 are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of Q_1-Q_2 and the V_{BE} of Q_3-Q_4 equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q3Q4}} = \Delta_{BE_{Q1Q2}}$$

($V_{BE} = V_T I_{IN} IC/IS$)

$$V_T I_n \left(\frac{\frac{1}{2}I_G + \frac{1}{2}I_O}{I_S} \right) - V_T I_n \left(\frac{\frac{1}{2}I_G - \frac{1}{2}I_O}{I_S} \right)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

$$V_T I_n \left(\frac{I_1 + I_{IN}}{I_S} \right) - V_T I_n \left(\frac{I_2 - I_1 - I_{IN}}{I_S} \right) \quad (2)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \quad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within ±25μA into the THD trim pin.

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only 6μV in the audio spectrum (10Hz-20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 5. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN(AVG)}}{R_2}$$

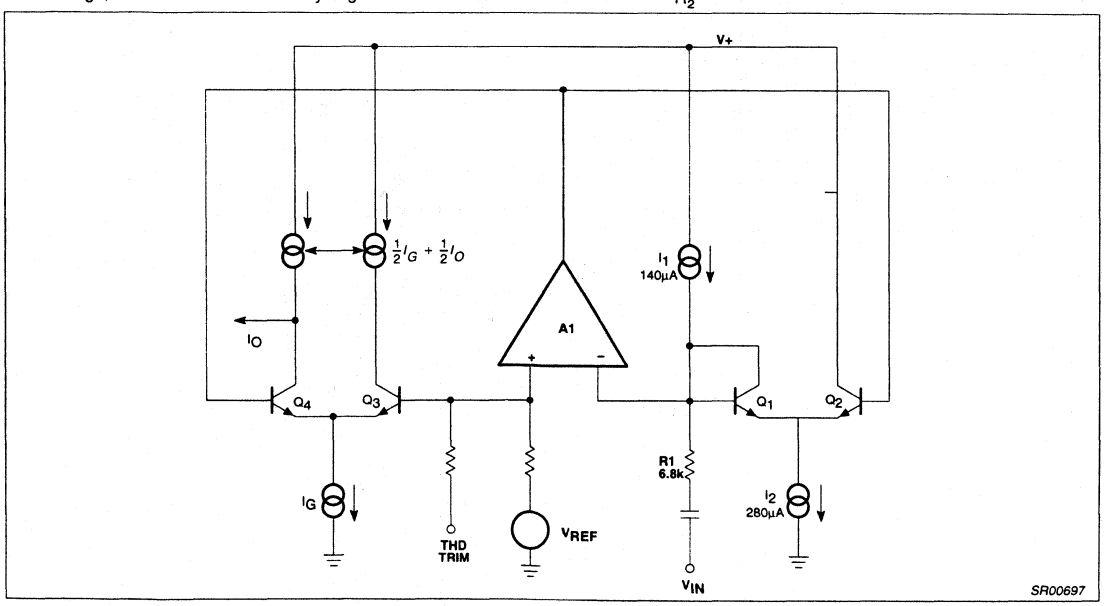


Figure 4. Basic Gain Cell Schematic

The internal bias scheme limits the maximum output current I_R to be around 300μA. Within a ±1dB error band the input range of the rectifier is about 52dB.

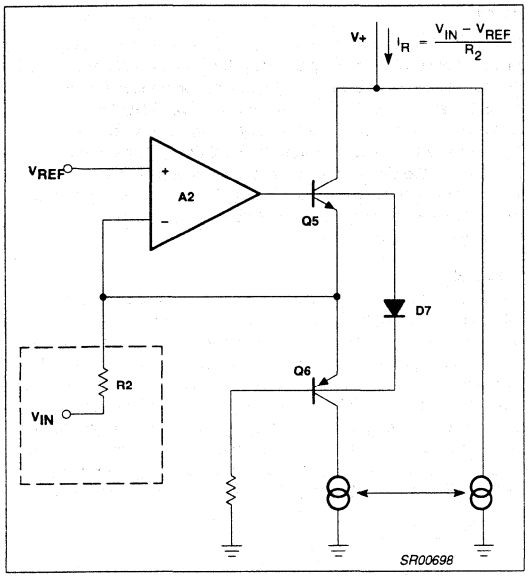


Figure 5. Simplified Rectifier Schematic

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 6, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\, e^{\frac{-t}{\tau_A}} + Ga_{FNL}$$

Ga_{INT}=Initial Gain

Ga_{FNL}=Final Gain

$\tau_A = R_A \bullet CA = 10k \bullet CA$

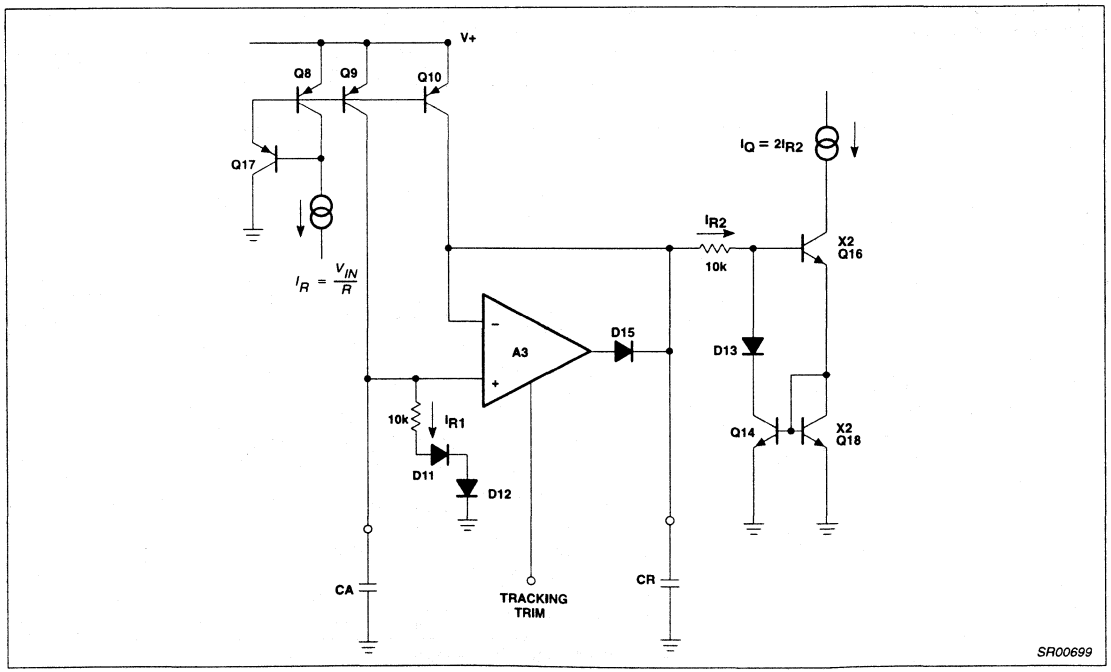


Figure 6. Buffer Amplifier Schematic

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{RINT} - G_{RFNL})\, e^{\frac{-t}{\tau_R}} + G_{RFNL}$$

$$G_R(t)=(G_{R\,INT}-G_{R\,FNL})\, e + G_{R\,FNL}$$

$$\tau R = R_R \bullet CR = 10k \bullet CR$$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of ±3μA.

Basic Expandor

Figure 7 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \qquad (5)$$

(I_1=140μA)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA • 6.8k=952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B \frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant. *5COL

Basic Compressor

Figure 8 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}}\right)^{\frac{1}{2}} \qquad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4}\right) \qquad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

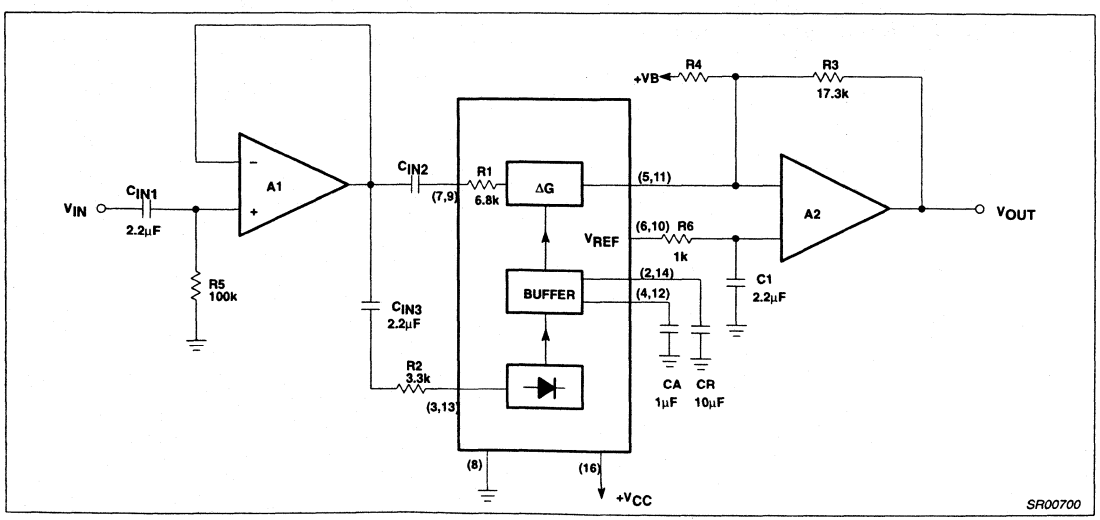


Figure 7. Basic Expandor Schematic

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 9 shows the system level diagram for reference.

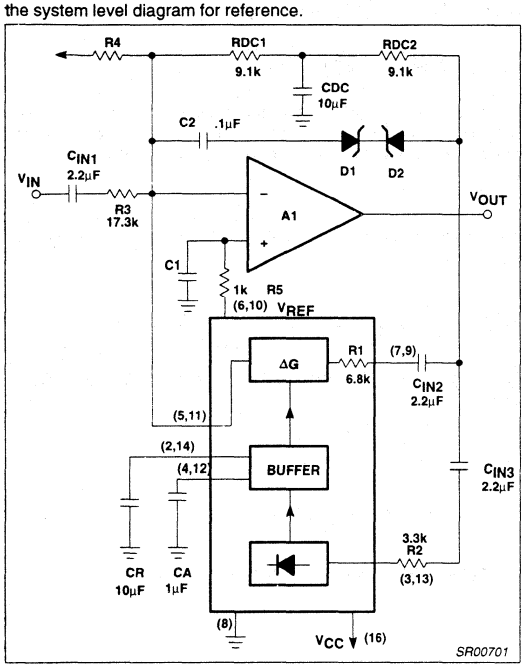


Figure 8. Basic Compressor Schematic

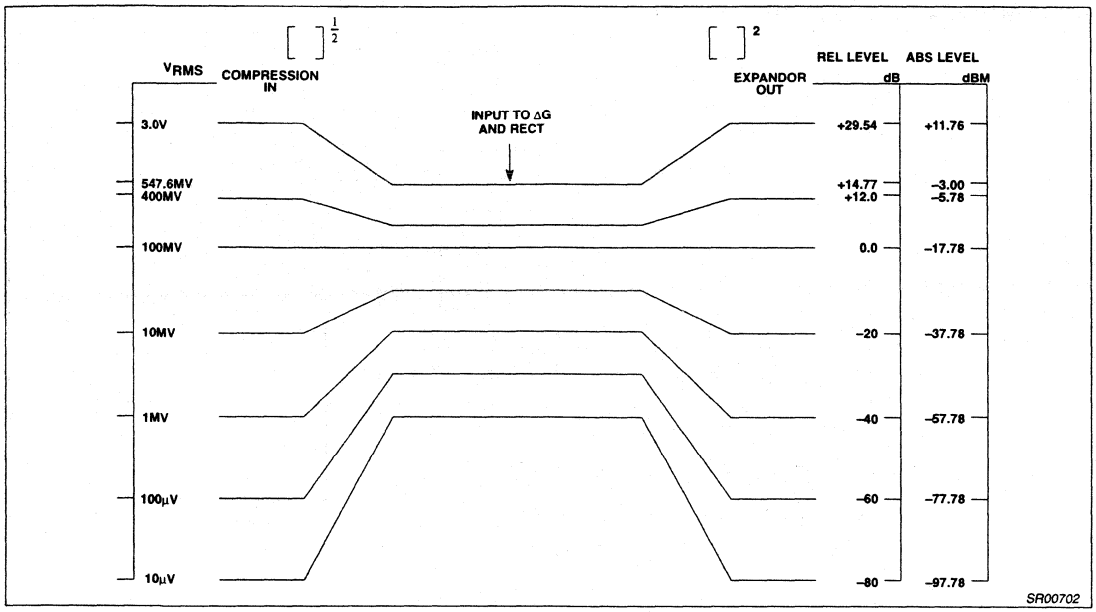
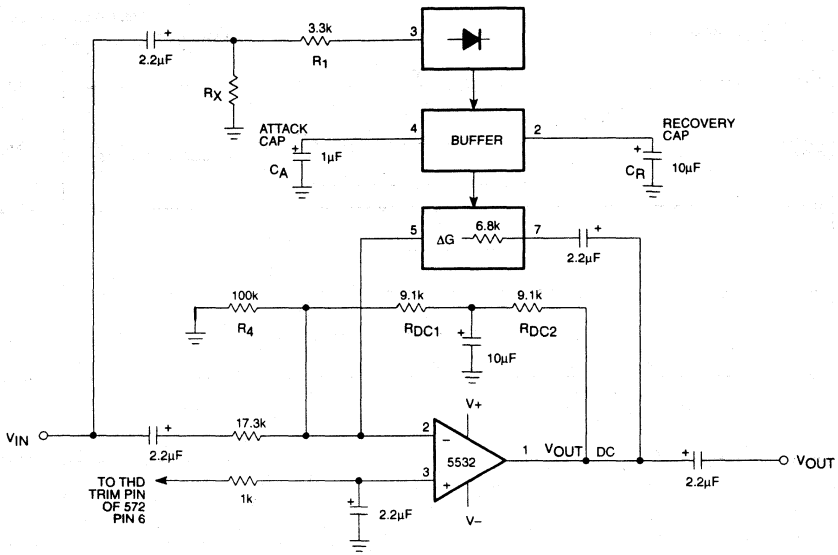


Figure 9. NE572 System Level

Automatic level control using the NE572 AN175

NE572 AUTOMATIC LEVEL CONTROL



$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right)$$

WHERE: $R_4 = 100k$
$R_{DC1} = R_{DC2} = 9.1k$
$V_{REF} = 2.5V$

$$\text{OUTPUT LEVEL} = \left(\frac{R_1 R_2 I_B}{2R_3}\right)\left(\frac{V_{IN}}{V_{IN(avg)}}\right)$$

WHERE: $R_1 = 6.8k$ (Internal)
$R_2 = 3.3k$
$R_3 = 17.3k$
$I_B = 140\mu A$

$$\text{Gain} = \frac{R_1 R_2 I_B}{2R_3 V_{IN}\,(avg)}$$

ATTACK TIME = (10k) C_A

RECOVERY TIME = (10k) C_R

TO LIMIT THE GAIN AT VERY LOW INPUT LEVELS, ADD R_X:

$$\text{GAIN MAX.} = \frac{\frac{R_1 + R_X}{2.5V} \times R_2 \times I_B}{2R_3}$$

$$\frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{2\sqrt{2}} = 1.11$$

(FOR SINE WAVES)

NOTE:
Pin numbers are for side A of the NE572.

SR00753

Low voltage compandor | NE/SA575

DESCRIPTION

The NE/SA575 is a precision dual gain control circuit designed for low voltage applications. The NE/SA575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

FEATURES

- Operating voltage range from 3V to 7V
- Reference voltage of 100mV$_{RMS}$ = 0dB
- One dedicated summing op amp per channel and two extra uncommitted op amps
- 600Ω drive capability
- Single or split supply operation
- Wide input/output swing capability
- 3000V ESD protection

PIN CONFIGURATION

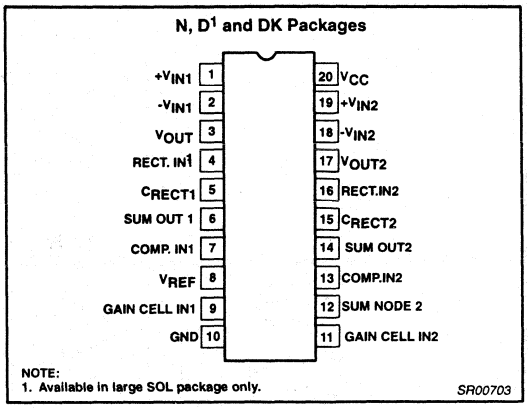


Figure 1. Pin Configuration

APPLICATIONS

- Portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Portable broadcast mixers
- Wireless microphones
- Modems
- Electric organs
- Hearing aids

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE575N	SOT146-1
20-Pin Plastic Small Outline Large	0 to +70°C	NE575D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	0 to +70°C	NE575DK	SOT266-1
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA575N	SOT146-1
20-Pin Plastic Small Outline Large	-40 to +85°C	SA575D	SOT163-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA575DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING		UNITS
			NE575	SA575	
V_{CC}	Single supply voltage		–0.3 to 8	–0.3 to 8	V
V_{IN}	Voltage applied to any other pin		–0.3 to (V_{CC}+0.3)	–0.3 to (V_{CC}+0.3)	V
T_A	Operating ambient temperature range		-40 to +85	-40 to +85	°C
T_{STG}	Storage temperature range		-65 to +150	-65 to +150	°C
θ_{JA}	Thermal impedance	DIP	68	68	°C/W
		SOL	112	112	°C/W
		SSOP	117	117	°C/W

BLOCK DIAGRAM and TEST CIRCUIT

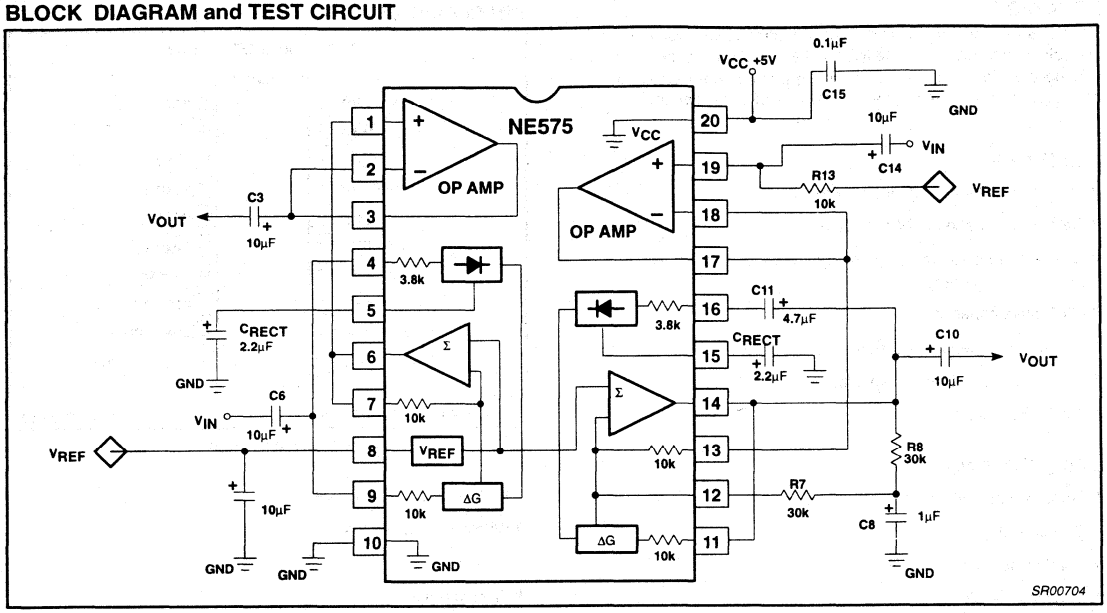


Figure 2. Block Diagram and Test Circuit

DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 25°C. Minimum and Maximum values are for the full operating temperature range: 0 to 70°C for NE575, -40 to +85°C for SA575, except SSOP package is tested at +25°C only. V_{CC} = 5V, unless otherwise stated. Both channels are tested in the Expandor mode (see Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
For compandor, including summing amplifier									
V_{CC}	Supply voltage[1]		3	5	7	3	5	7	V
I_{CC}	Supply current	No signal	3	4.2	5.5	3	4.2	5.5	mA
V_{REF}	Reference voltage[2]	V_{CC} = 5V	2.4	2.5	2.6	2.4	2.5	2.6	V
R_L	Summing amp output load		10			10			kΩ
THD	Total harmonic distortion	1kHz, 0dB BW = 3.5kHz		0.12	1.0		0.12	1.5	%
E_{NO}	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	20		6	30	µV
0dB	Unity gain level	1kHz	-1.0		1.0	-1.5		1.5	dB
V_{OS}	Output voltage offset	No signal	-100		100	-150		150	mV
	Output DC shift	No signal to 0dB	-50		50	-100		100	mV
	Tracking error relative to 0dB	Gain cell input = 0dB, 1kHz Rectifier input = 6dB, 1kHz	-0.5		0.5	-1.0		1.0	dB
		Gain cell input = 0dB, 1kHz Rectifier input = -30dB, 1kHz	-0.5		0.5	-1.0		1.0	dB

DC ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Crosstalk	1kHz, 0dB, C_{REF} = 220µF		-80	-65		-80	-65	dB
For operational amplifier									
V_O	Output swing	R_L = 10kΩ	V_{CC}-0.4	V_{CC}		V_{CC}-0.4	V_{CC}		V
R_L	Output load	1kHz	600			600			Ω
CMR	Input common-mode range		0		V_{CC}	0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V to 4.5V	-0.5		0.5	-1		1	µA
V_{OS}	Input offset voltage			3			3		mV
A_{VOL}	Open-loop gain	R_L = 10kΩ		80			80		dB
SR	Slew rate	Unity gain		1			1		V/µs
GBW	Bandwidth	Unity gain		3			3		MHz
E_{NI}	Input voltage noise	BW = 20kHz		2.5			2.5		µV
PSRR	Power supply rejection ratio	1kHz, 250mV		60			60		dB

NOTES:
1. Operation down to V_{CC} = 2V is possible, but performance is reduced. See curves in Figure 7a and 7b.
2. Reference voltage, V_{REF}, is typically at 1/2V_{CC}.

FUNCTIONAL DESCRIPTION

This section describes the basic subsystems and applications of the NE/SA575 Compandor. More theory of operation on compandors can be found in AN174 and AN176. The typical applications of the NE/SA575 low voltage compandor in an Expandor (1:2), Compressor (2:1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 3, 4, 5 respectively.

The NE/SA575 has two channels for a complete companding system. The left channel, A, can be configured as a 1:2 Expandor while the right channel, B, can be configured as either a 2:1 Compressor, a 1:2 Expandor or an ALC. Each channel consists of the basic companding building blocks of rectifier cell, variable gain cell, summing amplifier and V_{REF} cell. In addition, the NE/SA575 has two additional high performance uncommitted op amps which can be utilized for application such as filtering, pre-emphasis/de-emphasis or buffering.

Figure 6 shows the complete schematic for the applications demo board. Channel A is configured as an expandor while channel B is configured so that it can be used either as a compressor or as an ALC circuit. The switch, S1, toggles the circuit between compressor and ALC mode. Jumpers J1 and J2 can be used to either include the additional op amps for signal conditioning or exclude them from the signal path. Bread boarding space is provided for R1, R2, C1, C2, R10, R11, C10 and C11 so that the response can be tailored for each individual need. The components as specified are suitable for the complete audio spectrum from 20Hz to 20kHz.

The most common configuration is as a unity gain non-inverting buffer where R1, C1, C2, R10, C10 and C11 are eliminated and R2 and R11 are shorted. Capacitors C3, C5, C8, and C12 are for DC blocking. In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors C4 and C9 are for setting the attack and release time constant.

C6 is for decoupling and stabilizing the voltage reference circuit. The value of C6 should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be. R12 provides DC reference voltage to the amplifier of channel B. R6 and R7 provide a DC feedback path for the summing amp of channel B, while C7 is a short-circuit to ground for signals. C14 and C15 are for power supply decoupling. C14 can also be eliminated if the power supply is well regulated with very low noise and ripple.

DEMONSTRATED PERFORMANCE

The applications demo board was built and tested for a frequency range of 20Hz to 20kHz with the component values as shown in Figure 6 and V_{CC} = 5V. In the expandor mode, the typical input dynamic range was from -34dB to +12dB where 0dB is equal to 100mV_{RMS}. The typical unity gain level measured at 0dB @ 1kHz input was ±0.5dB and the typical tracking error was ±0.1dB for input range of -30 to +10dB.

In the compressor mode, the typical input dynamic range was from -42dB to ±18dB with a tracking error +0.1dB and the typical unity gain level was ±0.5dB.

In the ALC mode, the typical input dynamic range was from -42dB to +8dB with typical output deviation of ±0.2dB about the nominal output of 0dB. For input greater than +9dB in ALC configuration, the summing amplifier sometimes exhibits high frequency oscillations. There are several solutions to this problem. The first is to lower the values of R6 and R7 to 20kΩ each. The second is to add a current limiting resistor in series with C12 at Pin 13. The third is to add a compensating capacitor of about 22 to 30pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18dB yielding a dynamic range of over 60dB.

EXPANDOR

The typical expandor configuration is shown in Figure 3. The variable gain cell and the rectifier cell are in the signal input path. The V_{REF} is always 1/2 V_{CC} to provide the maximum headroom without clipping. The 0dB ref is 100mV_{RMS}. The input is AC coupled through C5, and the output is AC coupled through C3. If in a system the inputs and outputs are AC coupled, then C3 and C5 can be eliminated, thus requiring only one external component, C4. The variable gain cell and rectifier cell are DC coupled so any offset

voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.
The expandor gain expression and the attack and release time constant is given by Equation 1 and Equation 2, respectively.

Equation 1.

$$\text{Expandor gain} = \frac{4V_{IN}(avg)}{3.8k \times 100\mu A}$$

where $V_{IN}(avg) = 0.95V_{IN(RMS)}$

Equation 2.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

COMPRESSOR

The typical compressor configuration is shown in Figure 4. In this mode, the rectifier cell and variable gain cell are in the feedback path. R6 and R7 provide the DC feedback to the summing amplifier. The input is AC coupled through C12 and output is AC coupled through C8. In a system with inputs and outputs AC coupled, C8 and C12 could be eliminated and only R6, R7, C7, and C13 would be required. If the external components R6, R7 and C7 are eliminated, then the output of the summing amplifier will motor-boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.
The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4, respectively.

Equation 3.

$$\text{Compressor gain} = \left[\frac{3.8k \times 100\mu A}{4V_{IN}(avg)}\right]^{1/2}$$

where $V_{IN}(avg) = 0.95V_{IN(RMS)}$

Equation 4.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

AUTOMATIC LEVEL CONTROL

The typical Automatic Level Control circuit configuration is shown in Figure 5. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through C12 and C13 and the output is AC coupled through C8. Once again, as in the previous cases, if the system input and output signals are already AC coupled, then C12, C13 and C8 could be eliminated. Concerning the compressor, removing R6, R7 and C7 will cause motor-boating in absence of signals. C_{COMP} is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60dB with the output within ±0.5dB typical. The necessary design expressions are given by Equation 5 and Equation 6, respectively.

Equation 5.

$$\text{ALC gain} = \frac{3.8k \times 100\mu A}{4V_{IN}(avg)}$$

Equation 6.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C9$$

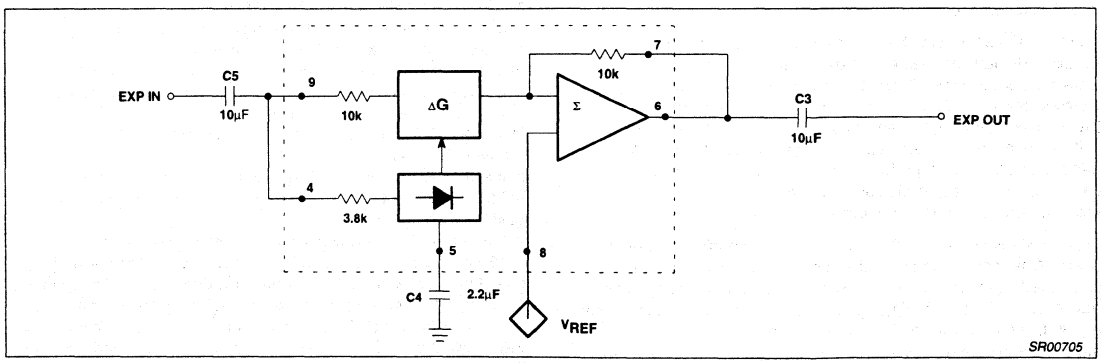


Figure 3. Typical Expandor Configuration

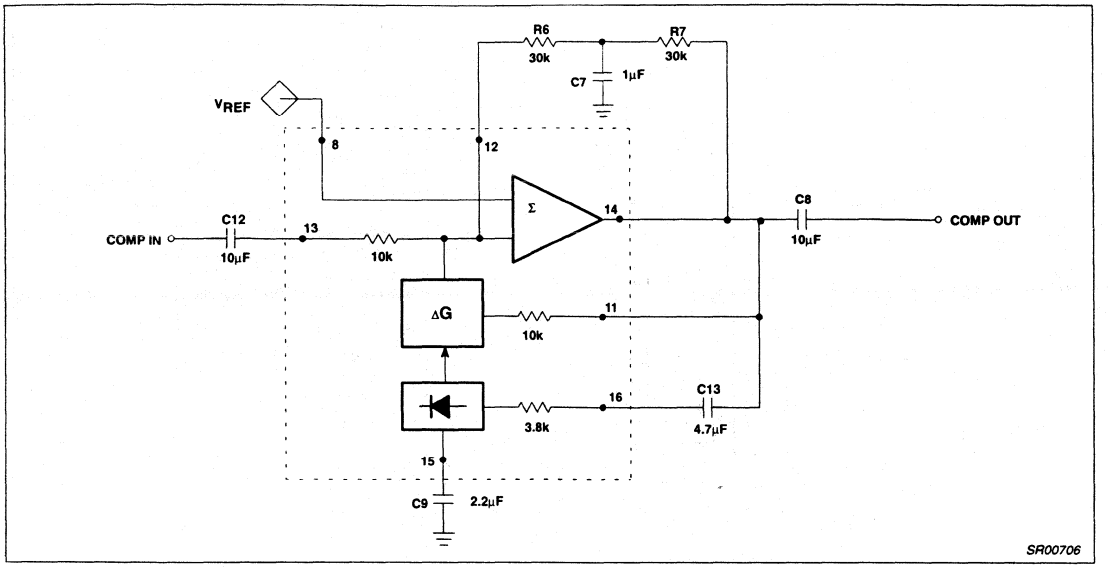


Figure 4. Typical Compressor Configuration

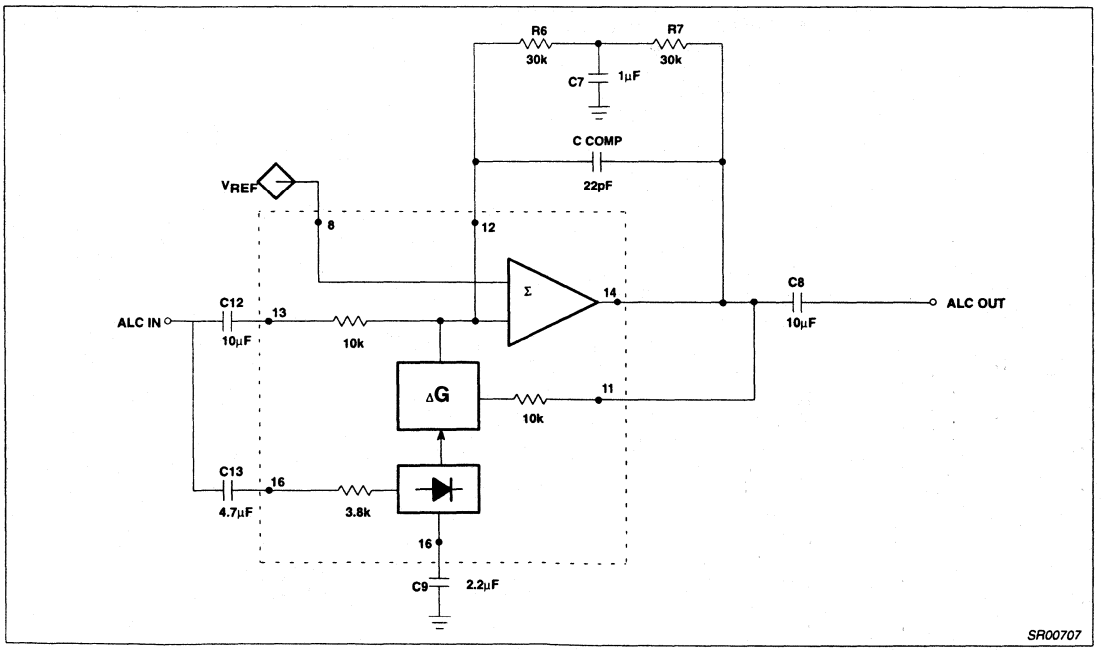


Figure 5. Typical ALC Configuration

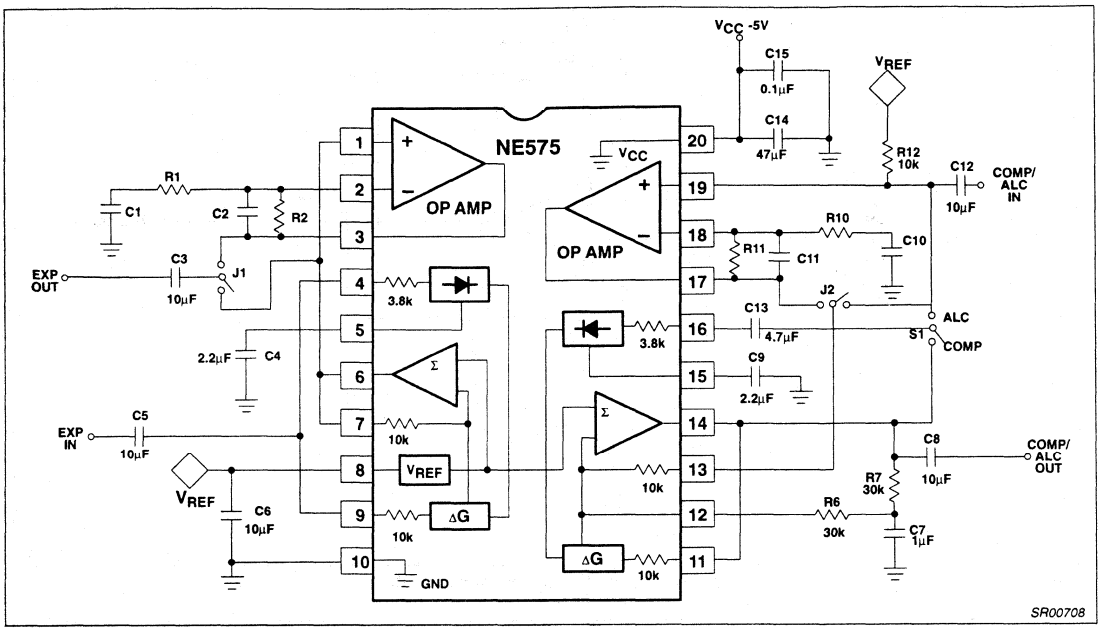
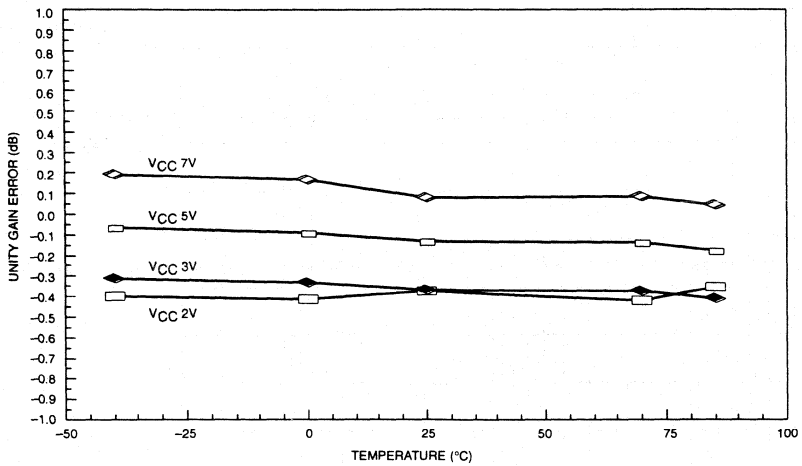
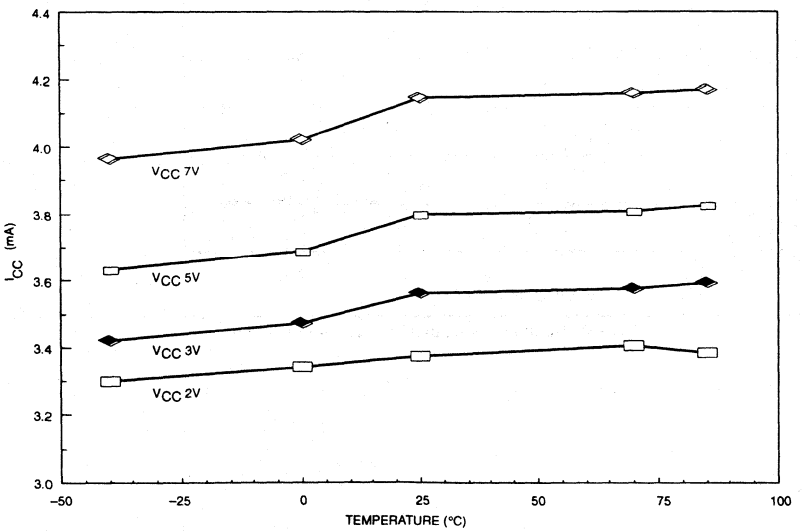


Figure 6. NE/SA575 Low Voltage Expandor/Compressor/ALC Demo Board



a. Unity Gain Error vs Temperature and V_{CC}



b. I_{CC} vs Temperature and V_{CC}

SR00709

Figure 7. Temperature and V_{CC} Curves

TYPICAL PERFORMANCE CHARACTERISTICS

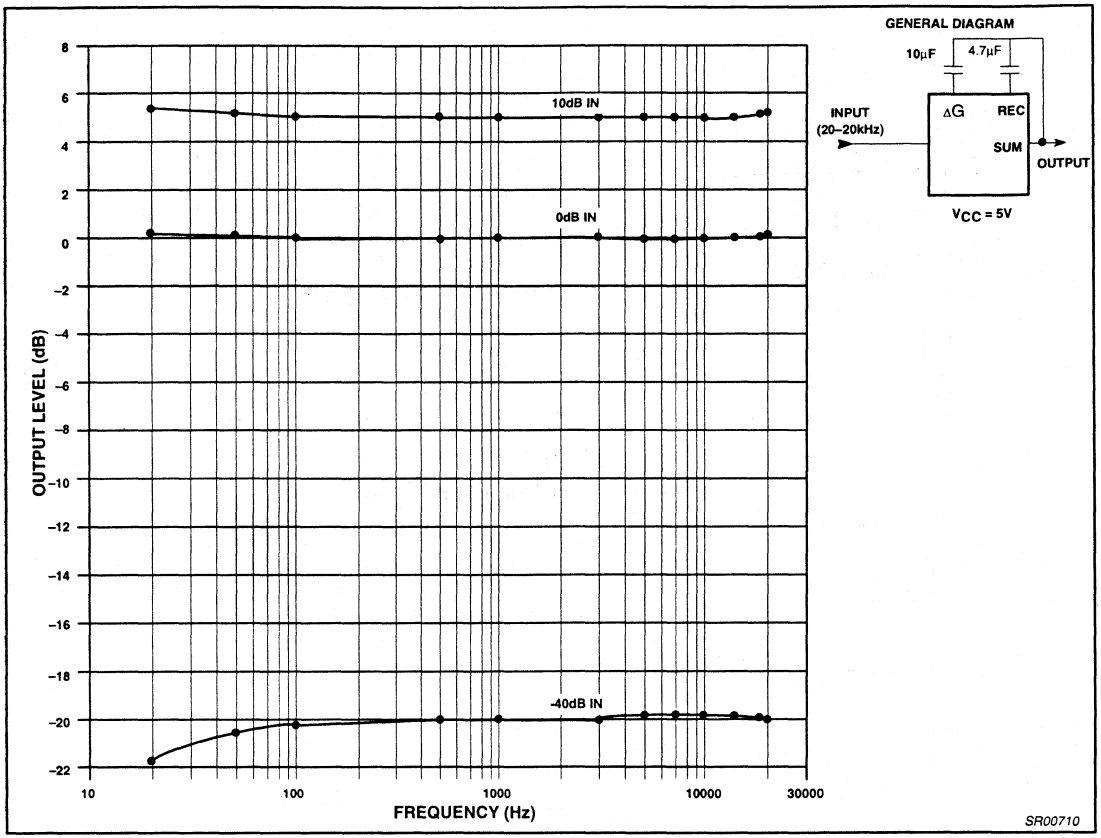


Figure 8. Compressor Output Frequency Response

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

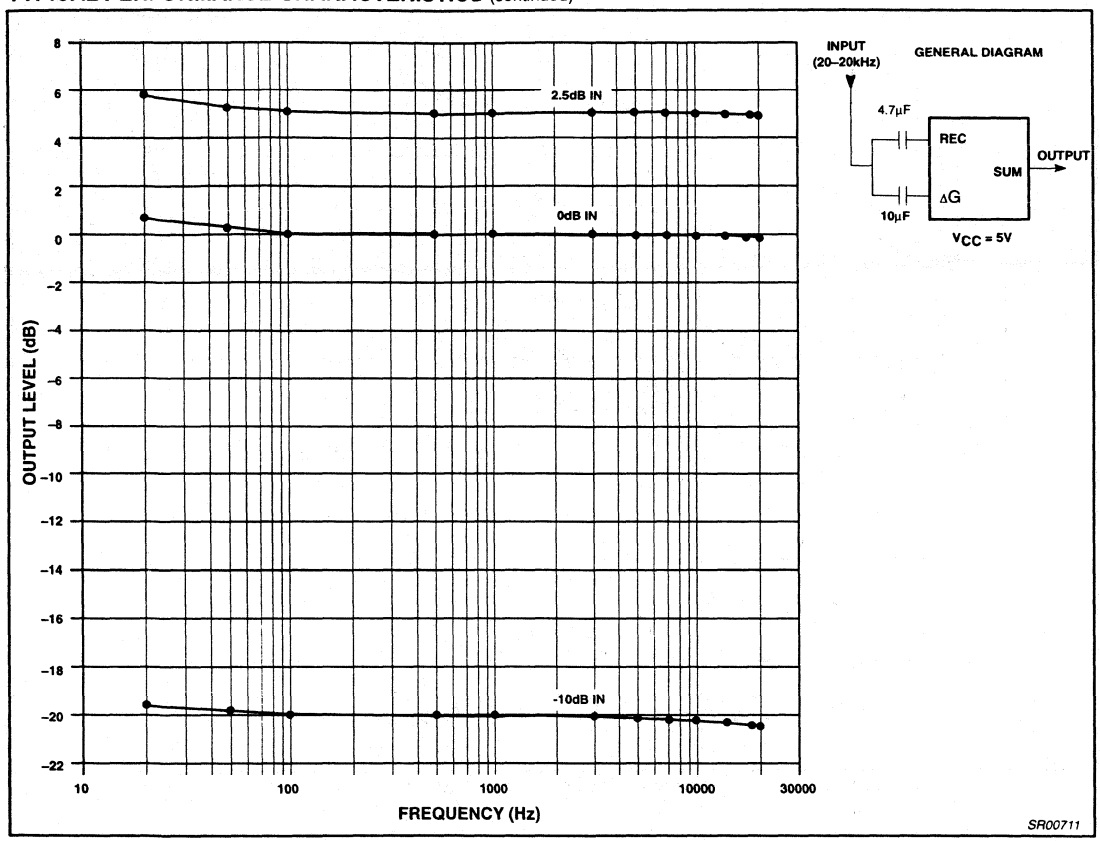


Figure 9. Expandor Output Frequency Response

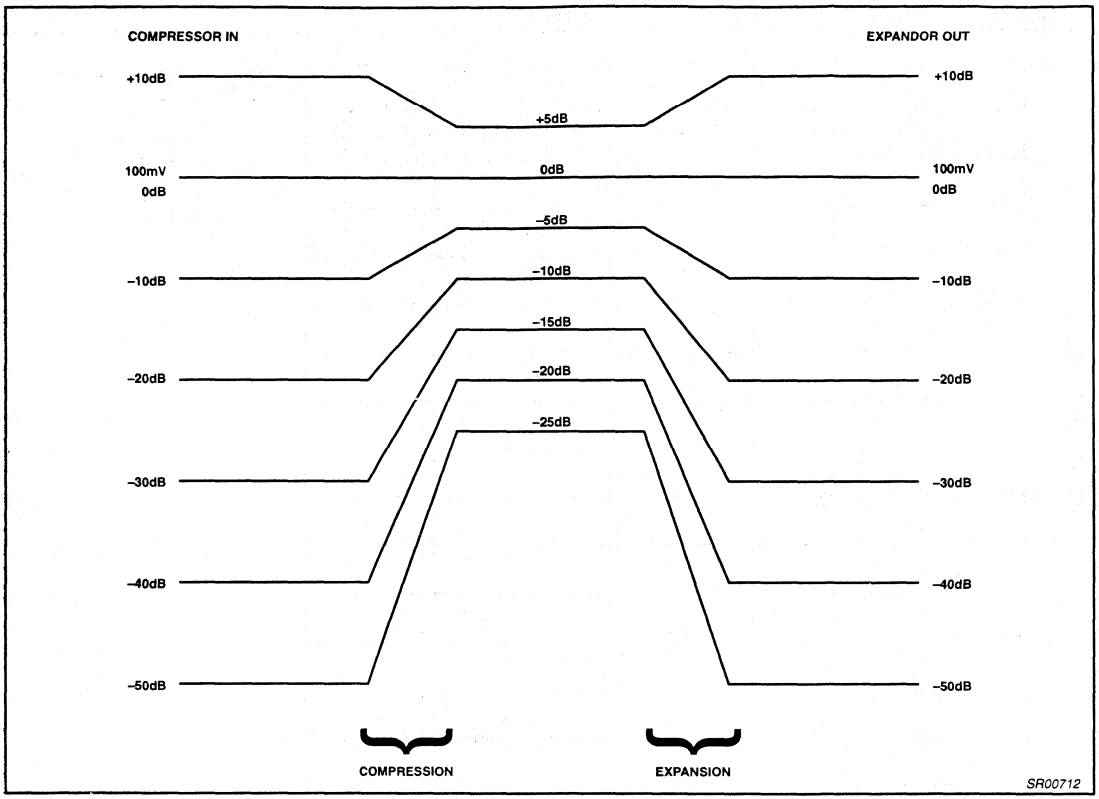


Figure 10. The Companding Function

Low power compandor — NE/SA576

DESCRIPTION

The NE/SA576 is a unity gain level programmable compandor designed for low power applications. The NE576 is internally configured as an expandor and a compressor to minimize external component count.

The NE576 can operate at 1.8V. During normal operations, the NE576 can operate from at least a 2V battery. If the battery voltage drops to 1.8V, this part will still continue to function, however, turning on the part at a V_{CC} of 1.8V requires two external resistors to bring V_{REF} to half V_{CC}. One resistor connects between V_{CC} and V_{REF}; the other connects from V_{REF} to ground. A typical value for these external resistors is approximately 20k. A lower value can be used, but the power consumption will go up.

The NE576 is available in a 14-pin plastic DIP and SO packages.

FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- Over 80dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- ESD hardened

PIN CONFIGURATION

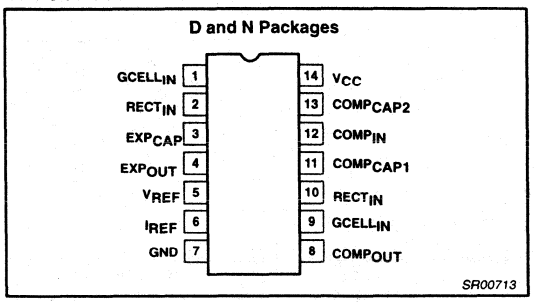


Figure 1. Pin Configuration

APPLICATIONS

- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE576N	SOT27-1
14-Pin Plastic Small Outline (SO)	0 to +70°C	NE576D	SOT108-1
14-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA576N	SOT27-1
14-Pin Plastic Small Outline (SO)	–40 to +85°C	SA576D	SOT108-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE576	SA576	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT

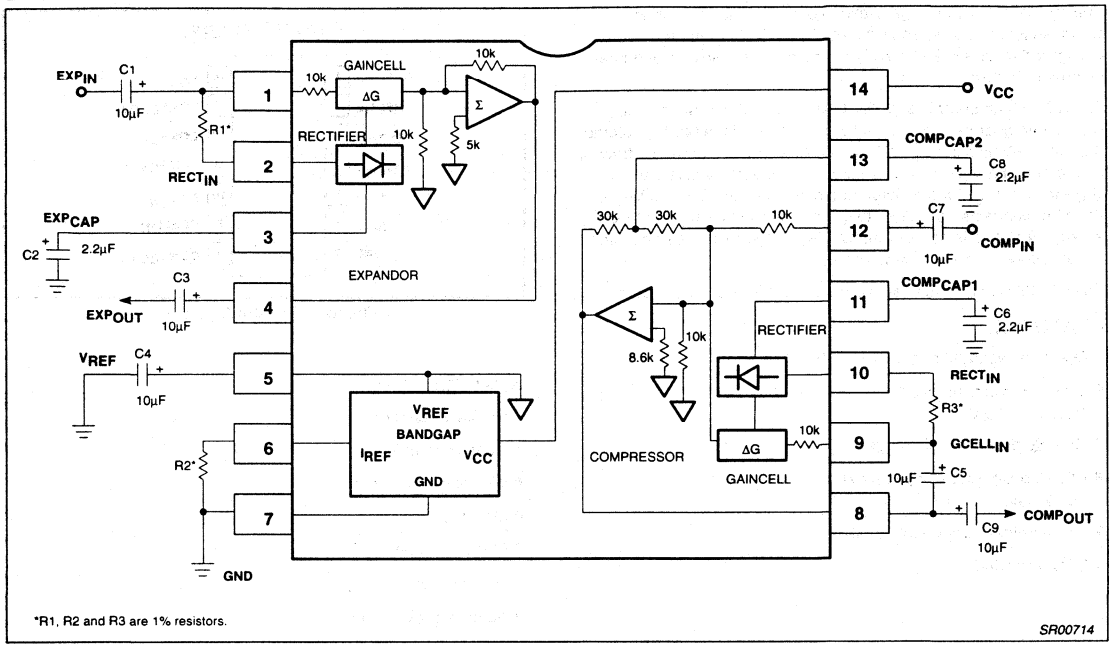


Figure 2. Block Diagram and Test and Application Circuit

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA576			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	3	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V		1.8		V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	30	µV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80		dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see description on front page of NE576 data sheet.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

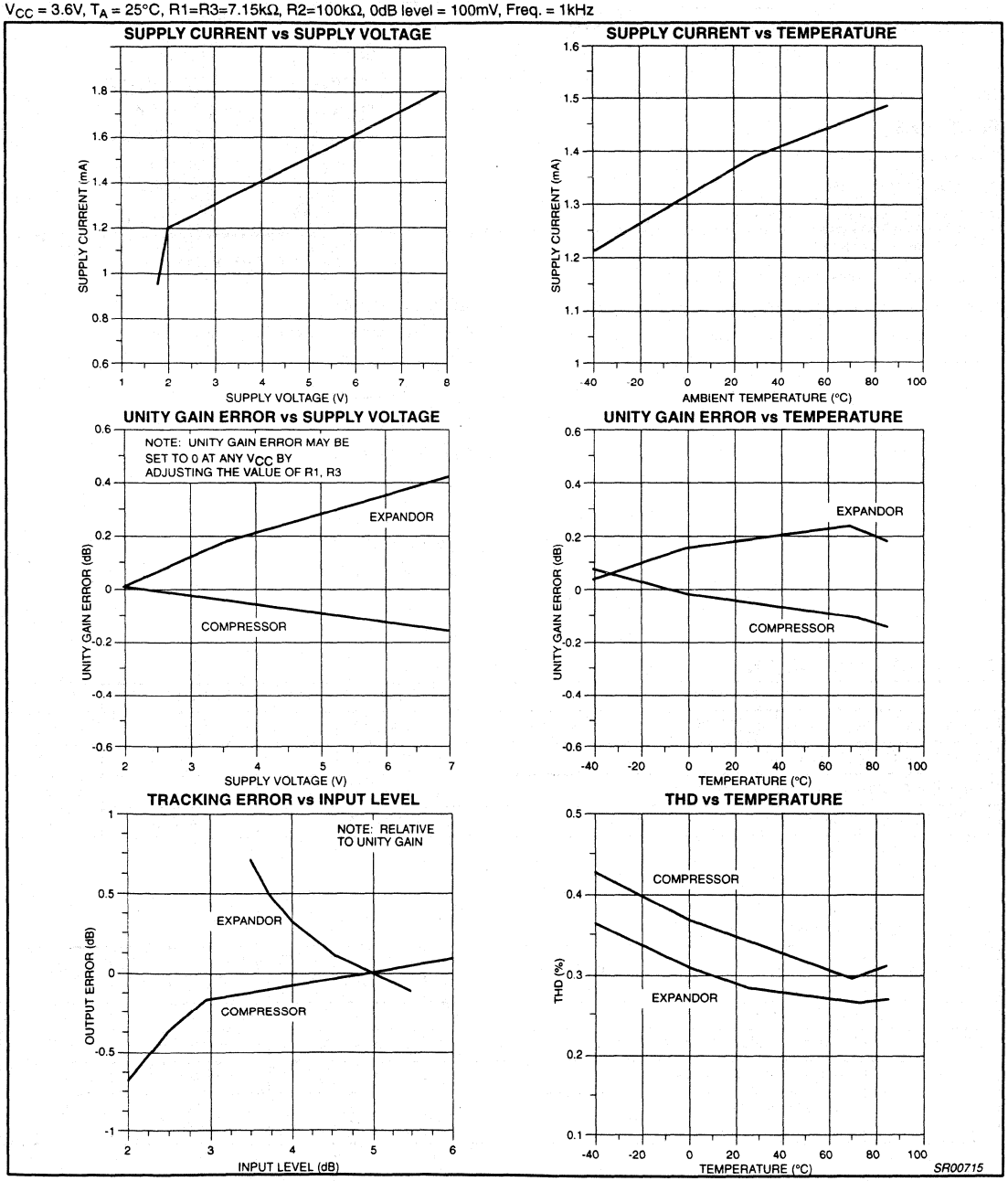


Figure 3. Typical Performance Characteristics

Unity gain level programmable low power compandor NE/SA577

DESCRIPTION

The NE/SA577 is a unity gain level programmable compandor designed for low power applications. The NE577 is internally configured as an expandor and a compressor to minimize external component count.

The NE577 is available in a 14-pin plastic DIP and SO packages.

FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable ($10mV_{RMS}$ to $1.0V_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- SA577 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

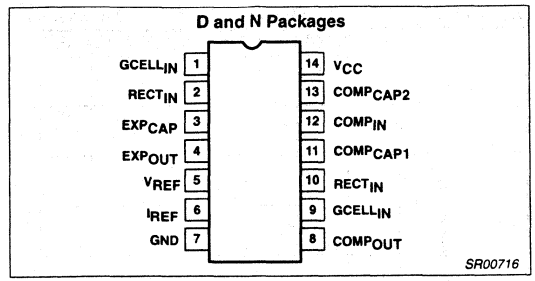


Figure 1. Pin Configuration

APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE577N	SOT27-1
14-Pin Plastic Small Outline (SO)	0 to +70°C	NE577D	SOT108-1
14-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA577N	SOT27-1
14-Pin Plastic Small Outline (SO)	–40 to +85°C	SA577D	SOT108-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE577	SA577	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA577			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	2	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	25	μV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10μF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see application note AN1762.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT

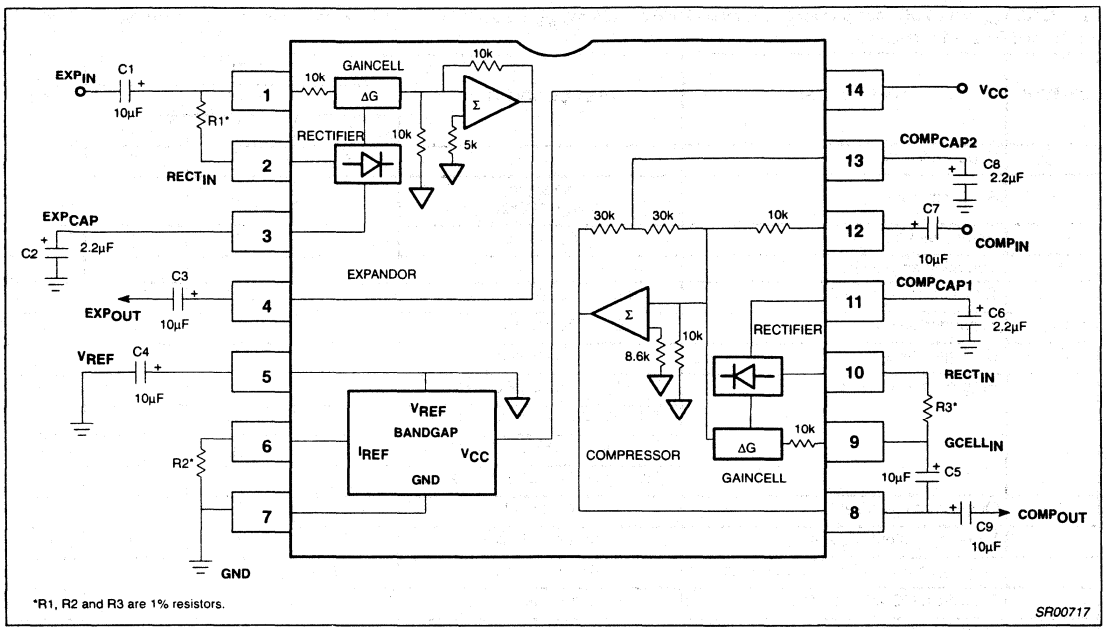


Figure 2. Block Diagram and Test and Application Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

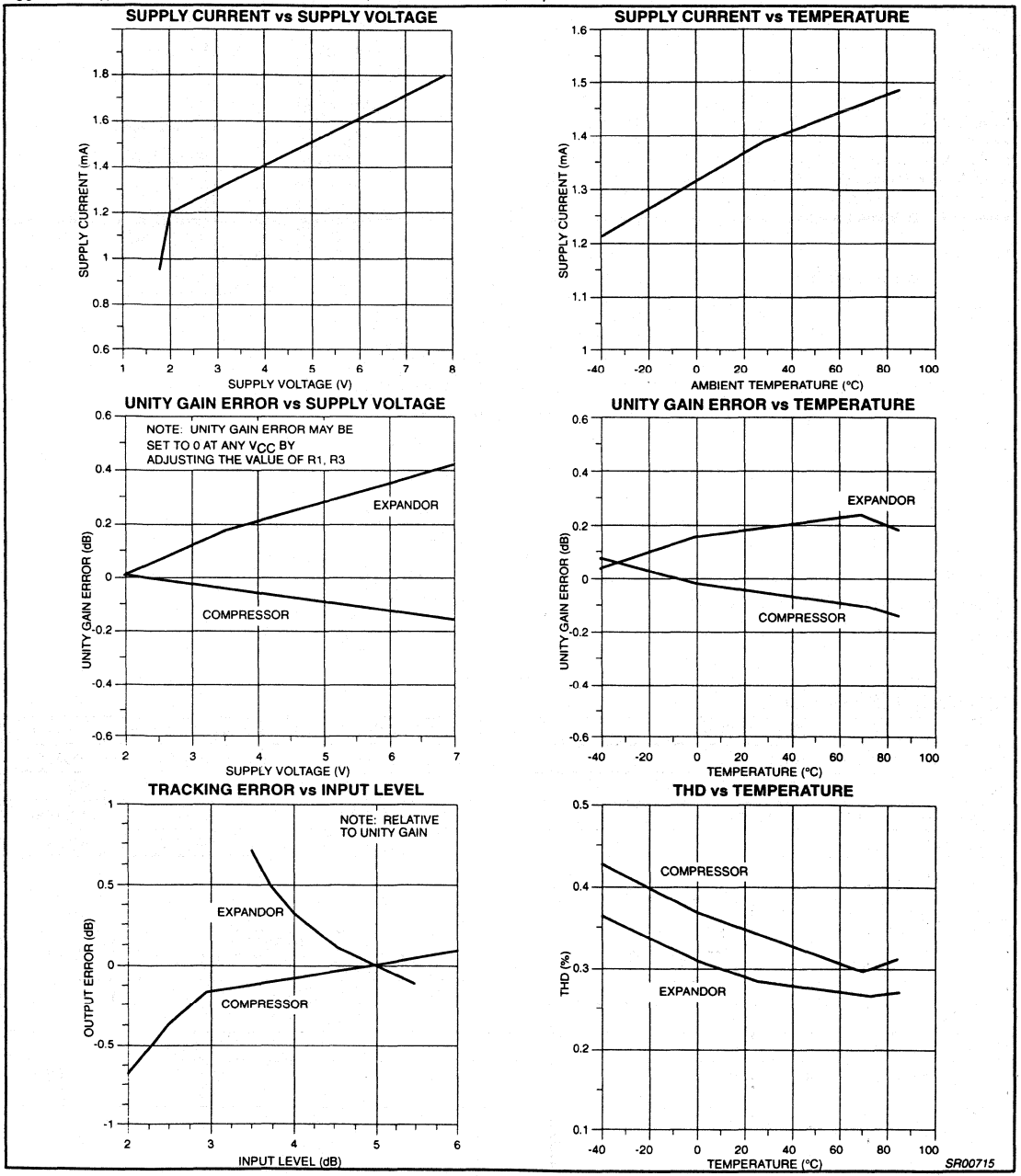


Figure 3. Typical Performance Characteristics

Unity gain level programmable low power compandor NE/SA578

DESCRIPTION

The NE/SA578 is a unity gain level programmable compandor designed for low power applications. The NE578 is internally configured as an expandor and a compressor to minimize external component count.

The summing amplifiers of the NE578 have 600Ω drive capability and the inverting input of the compressor amplifier is accessible through Pin 9 for summing multiple external signals. Power Down/Mute function is active low and requires an open collector output logic configuration at Pin 8. If Power Down/Mute is not needed, Pin 8 should be left open. When the part is muted, supply current drops to 170mA at 3.6V. The NE578 is available in a 16-pin plastic DIP and SO packages.

FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable ($10mV_{RMS}$ to $1.0V_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability
- Low external component count
- SA578 meets cellular radio specifications
- ESD hardened
- Power Down mode (I_{CC} = 170μA @ 3.6V)
- Mute function
- Multiple external summing capability
- 600Ω drive capability

PIN CONFIGURATION

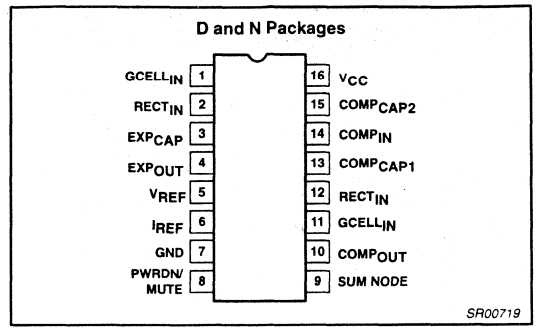


Figure 1. Pin Configuration

APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE578N	SOT28-4
16-Pin Plastic Small Outline (SO)	0 to +70°C	NE578D	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA578N	SOT28-4
16-Pin Plastic Small Outline (SO)	–40 to +85°C	SA578D	SOT109-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE578	SA578	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT

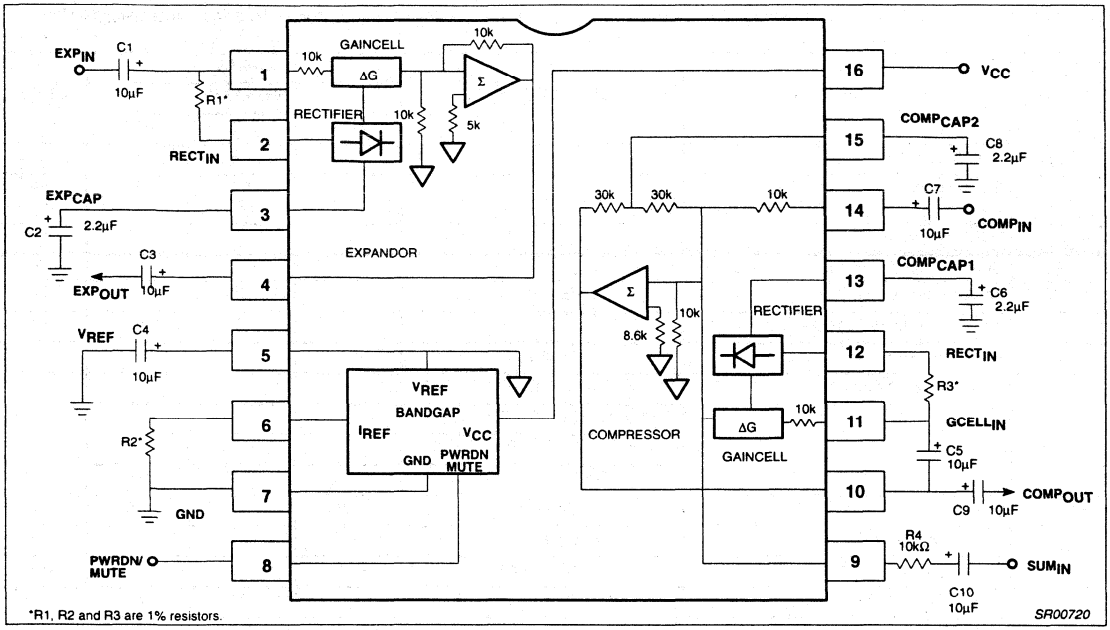


Figure 2. Block Diagram and Test and Application Circuit

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA578			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current operating power down	No signal, R_2 = 100kΩ		1.4 170	2	mA µA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp minimum output load			600		Ω
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.0	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	20	µV
0dB	Unity gain level	0dB at 1kHz	–1.0	0.18	1.0	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		
	Power Down/Mute low level		0		0.4	V
	Power Down/Mute input current	Pin 8 grounded		–65		µA

NOTE:
1. Operation down to V_{CC} = 1.8V is possible.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

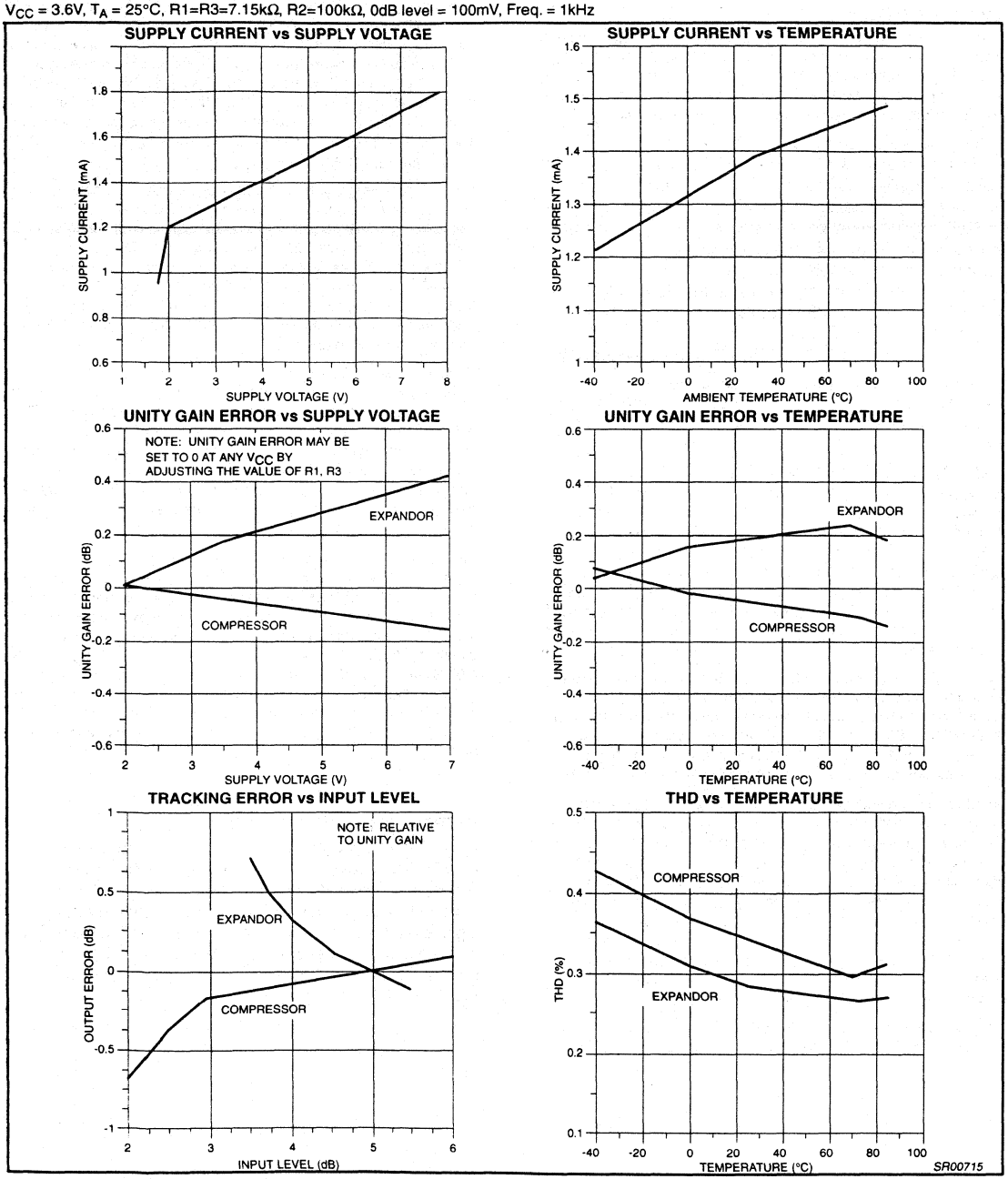


Figure 3. Typical Performance Characteristics

Companding with the NE577 and NE578 AN1762

Author: Alvin K. Wong

INTRODUCTION

This application note is written for the designer who understands the basic functions of companding and wants to use the NE577 or NE578. If a designer is not familiar with the functionality of compandors, a good discussion can be found in the earlier Philips Semiconductors compandor data sheets and applications notes.

Key topics discussed in this paper are:

- How to program the unity gain level (0dB)
- How to implement an automatic level control
- How to get the best companding performance under strict design requirements
- How to set the attack and recovery time
- How to operate at 1.8V
- How to sum external signals using the NE578
- How to power-down the NE578
- How to mute the NE578
- How to use the NE577 and NE578 as a dual expandor

But before reviewing these areas, a summary of Philips Semiconductors compandor family will be presented. A system designer can then determine which compandor is best for the design.

SUMMARY OF COMPANDOR FAMILY

In the past, Philips Semiconductors offered four different types of compandors: the NE570, NE571, NE572, and NE575. Each of the four compandors has its own 'claim to fame'. The NE570 and NE571 are known to work well in high performance audio applications. The only real difference between the two is that the NE570 has a slight edge in performance. However when separate attack and recovery times are needed, the NE572 is the compandor to choose. The NE575 becomes useful when there are low voltage requirements.

With the increasing demand for low current consumption, good flexibility, and ease of use in semiconductors, Philips Semiconductors is offering three additional compandors to its family, the NE576, NE577 and NE578. These compandors typically require an I_{CC} of 1.4mA at a V_{CC} of 3.6V, but Philips Semiconductors has demonstrated that these new chips are functional down to 1.8V.

In addition to having low power consumption, the NE578 has a power-down mode. In this mode, the chip consumes only 170µA. This power-down mode is useful when the functionality of the chip is not needed at all times. In the power-down mode , the NE578 maintains all of its pin voltages at all their normal DC operating voltages. Because all of the capacitors remain charged in this mode, the power-up state will occur quickly. Powering down automatically mutes the NE578. Having the mute function internal to the NE578 audio section eliminates the need for an external switch. The NE578 is the only compandor in the family that has power-down and mute functions.

To allow for greater flexibility, the 0dB level is now programmable for the NE577 and NE578. However, for the NE576, the 0dB level is specified and set at $100mV_{RMS}$. The earlier compandors also have a set unity gain (0dB) level. The NE570 and NE571 have a set 0dB level at $775mV_{RMS}$. While the NE572 and the NE575 both have their 0dB levels at $100mV_{RMS}$. If a designer wanted a different 0dB level, two op amps would have to be implemented in the design. One of the op amps would connect to the input of the compandor, while the other op amp would connect to the output. But with the NE577 and NE578, these external op amps are no longer needed. The 0dB level can be programmed from $10mV_{RMS}$ to $1V_{RMS}$ with three external resistors.

Many of the external parts in the previous family of compandors are now internal to the device. Additionally, the left side of the chip is configured as an expandor, and the right side is configured as a compressor. This allows for minimum part count and fewer variations in systems design. The external capacitors are also reduced in value which saves board space and cost. The only trade-off with using smaller capacitors is that there is less filtering. Because of this new approach, the NE576, NE577 and NE578 are easy to implement in any design.

Table 1 shows a brief summary of all the compandors. The seven different compandors offer a wide range of flexibility: different types of packages, power-down capability, programmable or fixed unity gain, different reference voltages, a wide range of operating voltages and currents, different pin outs, etc. From this information, a designer can quickly choose a compandor which best meets the design requirements. After a compandor is chosen from the table, a designer can find additional help from data sheets and application notes.

Since power consumption is important in most designs, it is important to discuss them in this application note. The NE570, NE571, and NE572 have built in voltage regulators, therefore, the current consumption remains roughly the same over the specified supply voltages. This can be especially useful when the power supply is not regulated very well. However with the NE575, NE576, NE577, and NE578, the current consumption will drop as the supply voltage decreases. For this, the power consumption will drop also. This means one can operate the part at a very low power level. This is a good feature for any design having strict power consumption guidelines.

INTRODUCING NE577 AND NE578

Figure 1 and 2 show block diagrams of the NE577 and NE578 respectively. The only substantial difference between the two is that the NE578 has a power-down capability, mute function and summing capabilities (for signals like DTMF tones). In addition the NE578 summing amplifiers are capable of driving 600Ω loads. Listed below are the basic functions of each external component for Figure 1 (NE577).

Companding with the NE577 and NE578 AN1762

Table 1. Compandor Family Overview

	NE570	NE571	NE572	NE575	NE576	NE577	NE578
V_{CC}	6–24V	6–18V	6–22V	3–7V	2–7V	2–7V	2–7V
I_{CC}	3.2mA	3.2mA	6mA	3–5.5mA*	1–3mA*	1–2mA*	1–2mA*
Number of Pins	16	16	16	20	14	14	16
Packages NE: 0 to +70°C SA: –40 to +85°C N: Plastic DIP D: Plastic SO F: Ceramic DIP DK: SSOP (Shrink Small Outline Package)	NE570F NE570N NE570D	NE571F NE571N NE571D SA571F SA571N SA571D	NE572N NE572D SA572F SA572N SA572D	NE575N NE575D NE575DJ SA575N SA575D SA575DK	NE576N NE576D SA576N SA576D	NE577N NE577D SA577N SA577D	NE578N NE578D SA578N SA578D
ALC (Automatic Level Control)	Both Channels	Both Channels	Both Channels	Right Channel	Right Channel	Right Channel	Right Channel
Reference Voltage	Fixed 1.8V	Fixed 1.8V	Fixed 2.5V	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2
Unity Gain	775mV_{RMS}	775mV_{RMS}	100mV_{RMS}	100mV_{RMS}	100mV_{RMS}	10mV to 1V_{RMS}	10mV to 1V_{RMS}
Power-Down	NO	NO	NO	NO	NO	NO	YES (170µA)
Key Features	-Excellent Unity Gain Tracking Error -Excellent THD	-Excellent Unity Gain Tracking Error -Excellent THD	-Independent Attack & Recovery Time -Good THD -Needs ext. summing op amp	-2 Uncommited on-chip op amps available -Low voltage	-Low power -Low external component count	-Low power -Programmable unity gain	-Low power -Programmable unity gain -Power down -Mute function -Summing capability (DTMF) -600Ω drive capability
Applications Cordless Phones Cellular Phones Wireless Mics Modems Consumer Audio Two-way Communications	High performance audio circuits "Hi–Fi Commercial Quality"	High performance audio circuits "Hi–Fi Commercial Quality"	High performance audio circuits "Hi–Fi Studio Quality"	Consumer audio circuits "Commercial Quality"	Battery powered systems "Commercial Quality"	Battery powered systems "Commercial Quality"	Battery powered systems "Commercial Quality"

NOTES: NE5750/5751 are also excellent audio processor components for high performance cordless and cellular applications that include the companding function..
*I_{CC} varies with V_{CC}.

R1 – Determines the Unity Gain Level for the Expandor

R2 – Determines What Value the Reference Current (I_{REF}) will be for the Part (Also Affects Unity Gain Level)

R3 – Determines the Unity Gain Level for the Compressor

C1 – DC Blocking Capacitor

C2 – Determines the Attack and Recovery Time for the Expandor

C3 – DC Blocking Capacitor

C4 – Used to AC Ground the V_{REF} Pin

C5 – Provides AC Path from Gain Cell to Output of Summing Amp

C6 – Determines the Attack and Recovery Time for the Compressor

C7 – DC Blocking Capacitor

C8 – Provides AC Ground for the DC Feedback Path

C9 – DC Blocking Capacitor

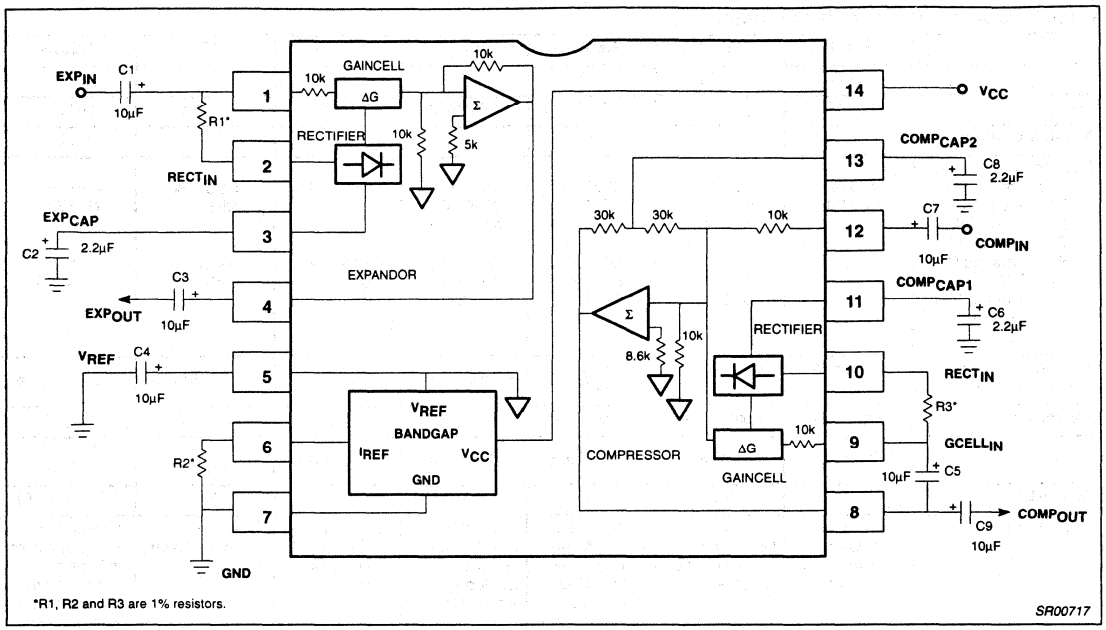


Figure 1 . NE577 Block Diagram

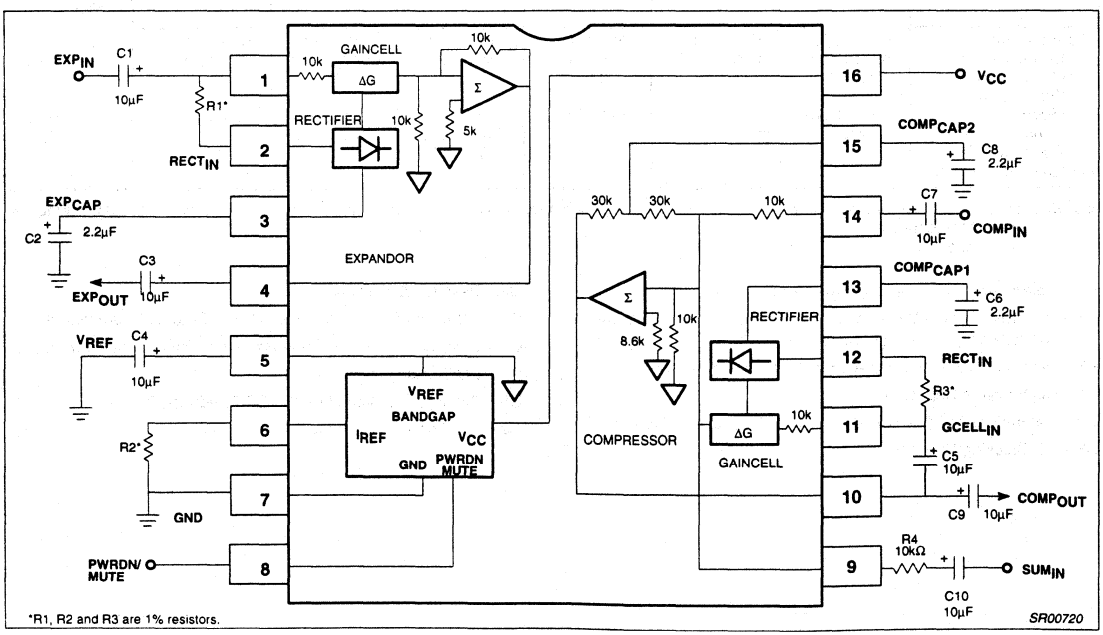


Figure 2 . NE578 Block Diagram

Listed below are the basic functions of each external component for Figure 2 (NE578).

R1 – Determines the Unity Gain Level for the Expandor

R2 – Determines What Value the Reference Current (I_{REF}) will be for the Part (Also Affects Unity Gain Level)

R3 – Determines the Unity Gain Level for the Compressor

R4 – Used to Set the Gain of an External Signal like DTMF Tones and Sum them with the Companded Signal

C1 – DC Blocking Capacitor

C2 – Determines the Attack and Recovery Time for the Expandor

C3 – DC Blocking Capacitor

C4 – Used to AC Ground the V_{REF} Pin

C5 – Provides AC Path from Gain Cell to Output of Summing Amp

C6 – Determines the Attack and Recovery Time for the Compressor

C7 – DC Blocking Capacitor

C8 – Provides AC Ground for the DC Feedback Path

C9 – DC Blocking Capacitor

C10 – DC Blocking Capacitor

HOW TO PROGRAM THE UNITY GAIN LEVEL (0dB)

Three external resistors R1, R2, and R3 define the unity gain level. Both the NE577 and the NE578 0dB levels can vary from $10mV_{RMS}$ to $1.0V_{RMS}$. These limits are used in product characterization, but these parts can function over a wider 0dB level range.

In most applications the 0dB level is equal for both the compressor and expandor side. Therefore, R1 and R3 are equal in value. R3 sets the 0dB level for the compressor side, and R1 sets the 0dB level for the expandor side. However, there could be a situation where a design requires different 0dB levels for compression and expansion. This will not be a problem with the NE577 or NE578, due to the separate 0dB level programming.

Using the formulas below, a designer can calculate the resistor values for a desired unity gain level.

Formula 1: $$R_2 = \frac{V_{BG}}{I_{REF}}$$

where
V_{BG} = Bandgap Voltage
I_{REF} = Reference Current
(V_{BG} is brought out on Pin 6 and R2 determines the I_{REF} value)

Formula 2: $$R_1 = \frac{0.9 \cdot V_{IN_{RMS}}}{I_{REF}}$$

where $V_{IN_{RMS}}$ is the 0dB level
($R_1 = R_3$ in most cases)

Programming the Unity Gain Level for the NE577 also applies for the NE578.

Example:

Program the NE577 or NE578 for a 0dB Level at $100mV_{RMS}$

Step 1: V_{BG}=1.26V.....Typically
I_{REF}=12.6μA.....Good Starting Point

$$R_2 = \frac{1.26V}{12.6}\mu A$$

R_2 = 100k

Step 2:

$$R_1 = R_3 = \frac{0.9V_{IN_{RMS}}}{I_{REF}}$$

$$R_1 = R_3 = \frac{(0.9V)\ (100mV_{RMS})}{12.6\mu A}$$

$\therefore R_1 = R_3 = 7.15k$

Step 3: $R_1 = R_3 = 7.15k$ (1% value)
R_2 = 100k (1% value)

Step 4: Plug in these resistor values and measure for unity gain. Adjust accordingly for accuracy.

NOTE:
Rough Limits for Resistors:
$1k \leq R1 \leq 100k$ (1% values)
$20k \leq R2 \leq 200k$ (1% values)
$1k \leq R3 \leq 100k$ (1% values)

Rough Limits for I_{REF}
$6.3\mu A \leq I_{REF} \leq 63\mu A$

The example above gives pretty close results. A designer should use 1% resistors to get the best performance. Below in Table 2 are some recommended values to get started:

Table 2. Recommended Resistor Values for Different 0dB Levels

0dB Level	dBv	R_2	R_1 & R_3
$1.0V_{RMS}$	0	24.3k	18.7k
$316.2mV_{RMS}$	–10	100k	22.6k
$100mV_{RMS}$	–20	100k	7.15k
$10mV_{RMS}$	–40	200k	1.33k

PARAMETERS THAT LIMIT THE DYNAMIC RANGE

The above example is a good place to start, but to get the optimum performance from the NE577 and NE578, a designer needs to understand certain key parameters. I_{REF} is important because it determines the values for all three resistors (R1, R2, and R3). Since I_{REF} is directly related to I_{CC} (see Figure 3), one should be careful in choosing a value. If one chooses a high I_{REF} current, power consumption goes up. However the output signal will have excellent low level distortion (see Figures 4 and 5). If one chooses a low I_{REF} value, distortion at the output will increase slightly. Conversely, the power consumption is reduced, which might be worth the trade-off in battery operated designs.

The dynamic range of the NE577 and NE578 is determined by supply voltage (V_{CC}) and reference current (I_{REF}). I_{REF} determines how well the compandor will perform with low level input signals. The supply voltage determines how high (in level) an input signal can be before clipping appears on the output (in some cases increasing I_{REF} also helps). A designer needs to estimate the input

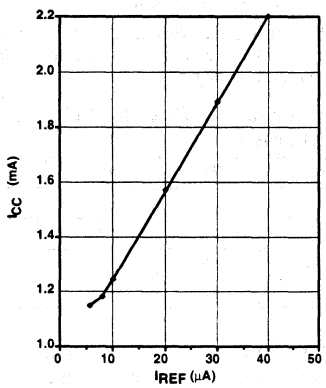
range going into the compandor so that an appropriate V_{CC} and I_{REF} can be chosen.

The bandgap voltage (V_{BG}) slightly varies over a wide range of I_{REF} currents (Figure 6). Figure 7 shows how I_{REF} varies with R2. The higher R2 is, the lower I_{REF} is. Figure 8 shows how the dynamic range varies over different values of I_{REF} (the higher the supply voltage the better the dynamic range). The graphs in Figures 3 - 8 were taken at V_{CC}=3.6V, F=1kHz and 0dB level=100mV_{RMS}. The I_{REF} current was limited between 5μA and 40μA.

It can be seen that I_{REF} plays an important role in current consumption, THD, and dynamic range. With the aid of these figures, one can determine an I_{REF} which meets the design goals.

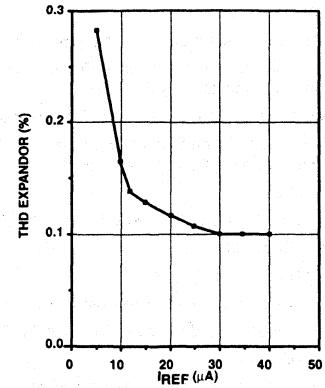
Example:
Making use of the graphs in Figures 3 - 8 and formulas 1 and 2, design a compandor with a 0dB level of 100mV_{RMS}. Try to achieve a THD of 0.1 on the compressor side with wide dynamic range. Operate at a supply voltage of 3.6V but with the lowest possible current consumption.

Step 1: According to Figure 5, an I_{REF} of 30μA is required for approximately 0.1% distortion.



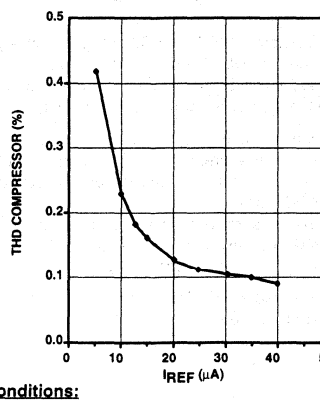
Test Conditions:
V_{CC} = 3.6V F = 1kHz 0dB = 100mV_{RMS} SR00754

Figure 3 . I_{REF} vs I_{CC}



Test Conditions:
V_{CC} = 3.6V F = 1kHz 0dB = 100mV_{RMS} SR00755

Figure 4 . I_{REF} vs THD, Expandor Side



Test Conditions:
V_{CC} = 3.6V F = 1kHz 0dB = 100mV_{RMS} SR00756

Figure 5 . I_{REF} vs THD, Compressor Side

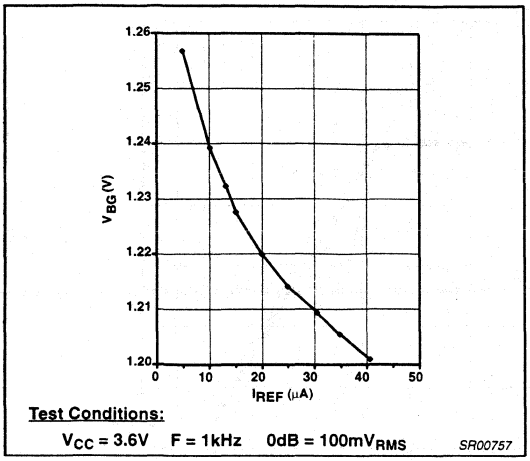


Figure 6 . I_{REF} vs V_{BG}

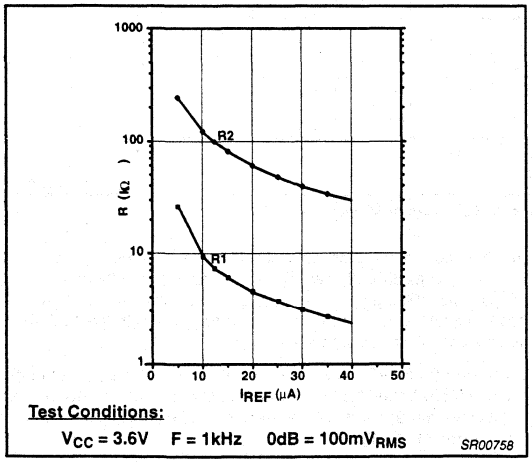


Figure 7 . I_{REF} vs R2, R1

Step 2: From Figure 8, the dynamic range is approximately 92dB. So far the requirements have been met.

Step 3: Figure 3 shows us that I_{CC} is at 1.9mA with no input signal (that's not bad at all!).

Step 4: Calculating R1, R2, and R3

Graphical Method:
From Figure 7: For I_{REF}=30μA and 0dB=100mV_{RMS} R1=R3=3k R2=40k

Actual resistors available: R1=R3=3.01k (1%) R2=40.2k (1%)

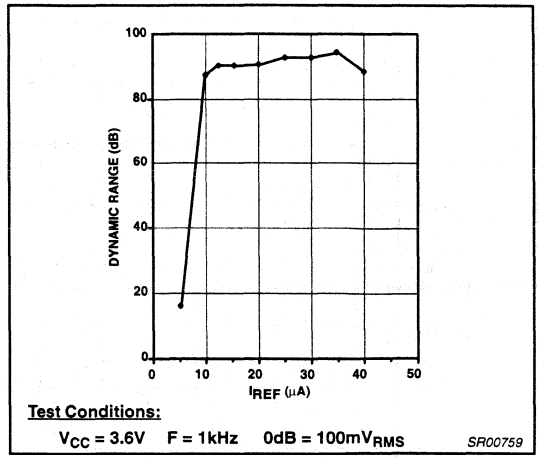


Figure 8 . I_{REF} vs Dynamic Range

Formula Method:
From Figure 6: V_{BG}=1.21V for I_{REF}=30μA therefore, using formula 1:

$$R_2 = \frac{V_{BG}}{I_{REF}}$$

$$R_2 = \frac{1.21V}{30\mu A}$$

R_2 = 40.33k
R_2 = 40.2k (available in 1%)

Recall from formula 2:

$$R_1 = \frac{0.9V_{IN_{RMS}}}{I_{REF}}$$

$$R_1 = \frac{(0.9V)\ (100mV_{RMS})}{30\mu A}$$

R_1 = 3k
R_1 = 3.01k (available in 1%)

Connect these external resistors with the determined values and adjust for optimum performance.

Bench results:
After completing the exercise above, the resistors were connected and the results are given below.

I_{CC} = 1.89mA (with no input signal)
THD = 0.1 (measured on spectrum analyzer)
0dB = 109mV_{RMS} (off by 0.8dB...good!) Dynamic Range = 92dB

These results are very close to what was predicted and by tweaking R1 and R3, the 0dB error can be further reduced to zero.

BANDWIDTH OF COMPANDOR

Figure 9 shows the typical bandwidth for the NE577 and NE578. The graphs were taken with a V_{CC} of 3.6V and a 0dB level of 100mV_{RMS}. The bandwidth of the expandor, the compressor, and the compandor (where a signal goes through the compressor and the expandor) is shown in this figure. Although the NE577 and NE578 are conservatively specified with a 20kHz bandwidth, Figure 9 reveals that it is actually around 300kHz.

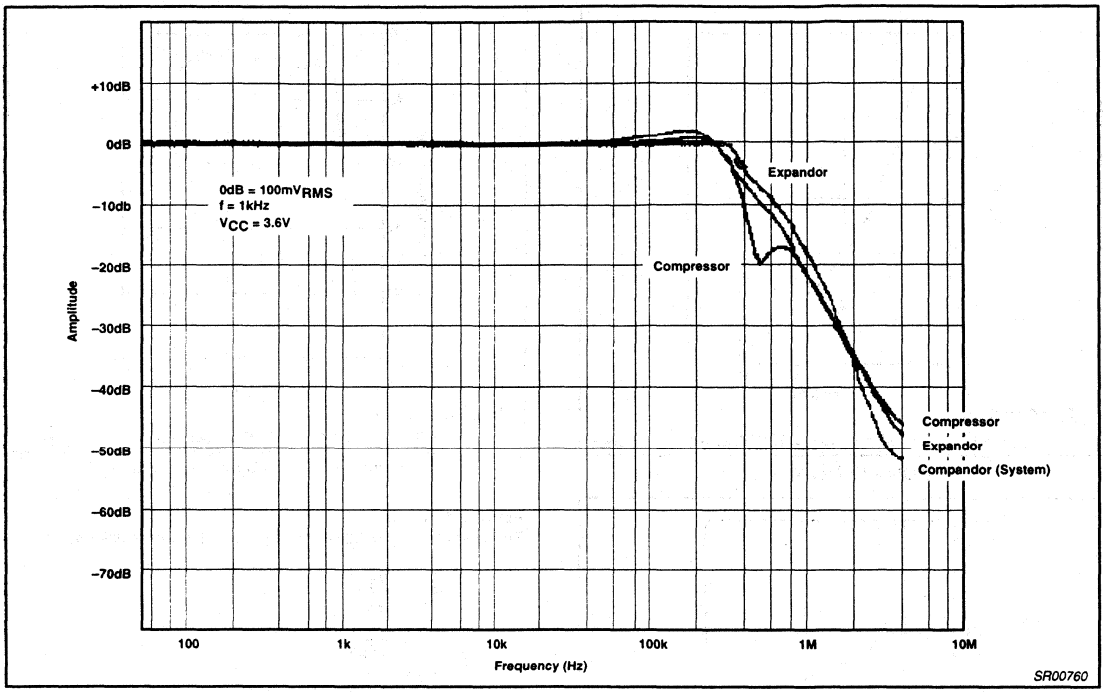


Figure 9 . Bandwidth of NE577 and NE578 Demo Board

HOW TO SET THE ATTACK AND RECOVERY TIMES

C2 and C6, from figures 1 and 2, set the attack and recovery times for the NE577 and NE578. Application Note 174 (AN174) defines A and R times and also describes how they are measured on the bench. Formula 3 shows how the A and R time can be calculated.

Formula 3:

Attack Time [ms] = 10k * C2 or C6
Release Time [ms] = 4 * Attack Time

Although a fast attack time is desirable, one must remember that there is a trade-off with low distortion. As a general rule, a 1μF capacitor for C2 will produce 0.2% THD at 1kHz. Since CCITT recommends an RC time constant of 20ms for the attack time, a 2μF capacitor is recommended for telephony applications because it has only 0.1% THD at 1kHz and 0.33% at 800Hz.

Note: AN174 can be found in the 1989 Linear Data Manual, Volume 1, or the RF Handbook.

IMPLEMENTING A PROGRAMMABLE AUTOMATIC LEVEL CONTROL

The function of an automatic level control (ALC) is to take a given range of input signals and provide a constant AC output level. This type of function is useful in many audio applications. One such application can be found in tape recorders. When a tape recorder with ALC is recording a conversation, a soft spoken person will be heard just as well as a loud spoken person during play back.

Another useful application for ALC could be with telephony. A person who has difficulty hearing, will not have to ask the other party to speak up. If the phone already has a volume control, the user has to adjust the volume for different parties. But with the ALC, the volume only has to be set once.

Different constant AC output levels of an ALC can be 'programmed' with the NE577 and NE578. This allows the designer to choose the output level that is needed in the design, and eliminates the need for an external op amp.

The compressor side of the NE577 and NE578 can be configured to function as an automatic level control (ALC). Figure 10 and 11 show how this can be done. The circuit shown for the NE577/78 ALC is set up to provide a constant output level of $100mV_{RMS}$ with an input range from –34dB to +20dB at 1kHz (see Figure 12).

Below are some design equations for the ALC:

$$\text{AC output level}(V_{RMS}) = \left[\frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a}}\right] \cdot 1.11 \qquad \text{Eq 1.}$$

where $R_{1_a} = R_{2_a} = 10k$ (internal)

$$I_{REF} = \frac{V_{BG}}{R_2}$$

$$\text{Maximum Gain} = \frac{4(R_3 + R_X) \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{CC}} \qquad \text{Eq 2.}$$

$$\text{Gain} = \frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{IN_{RMS}}} \qquad \text{Eq 3.}$$

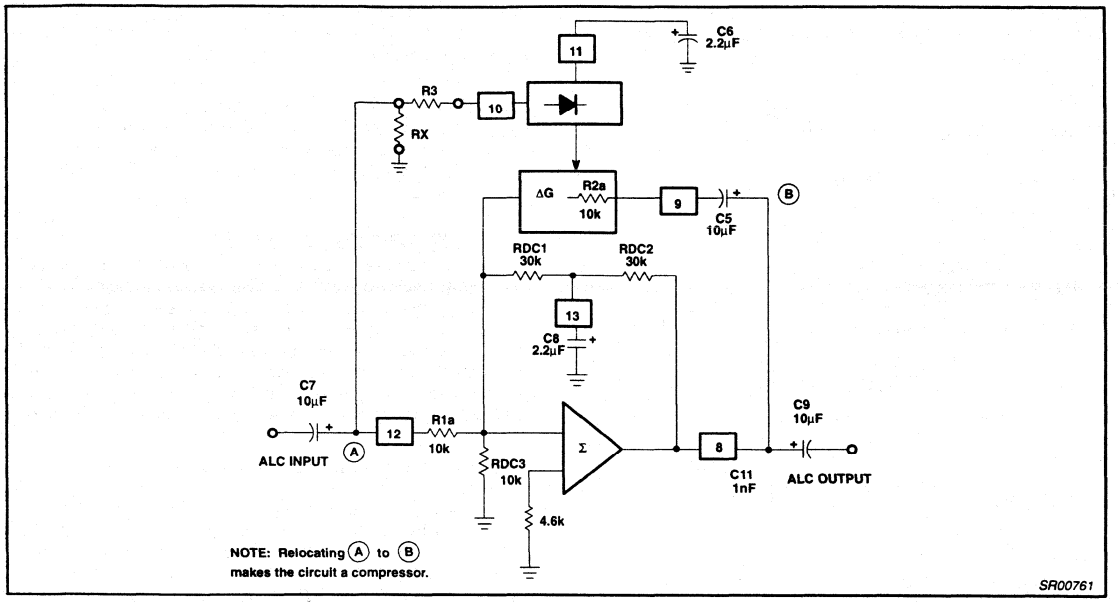


Figure 10 . NE577 ALC Configuration

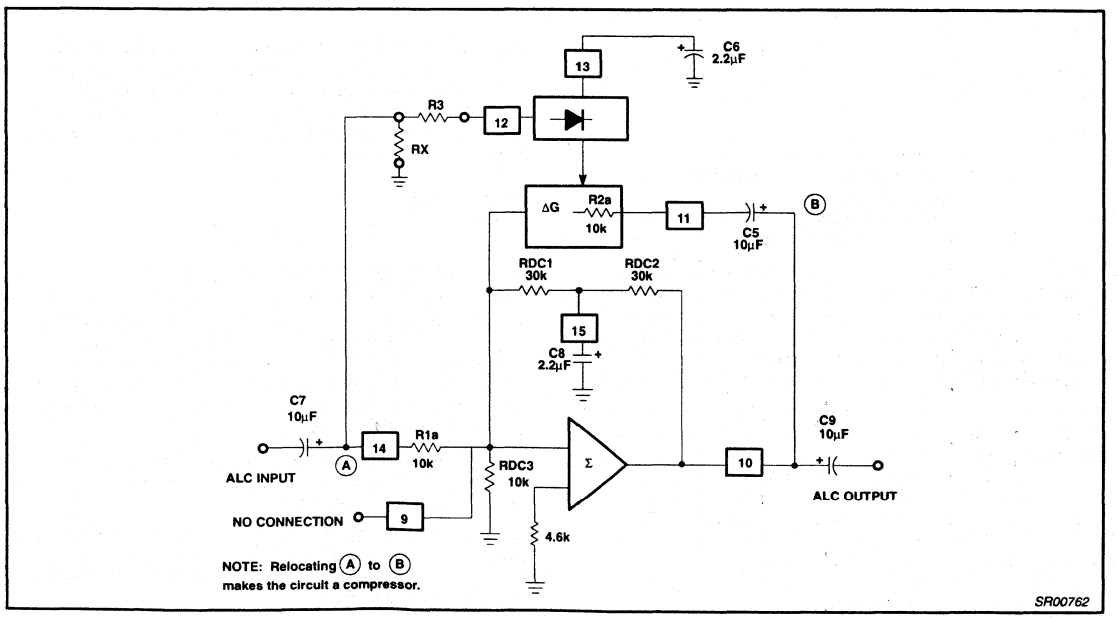


Figure 11 . NE578 ALC Configuration

Example:
Design an ALC with a constant output level of $100mV_{RMS}$ with a maximum gain of 10.

Step 1: From Eq 1

$$\text{AC output level}(V_{RMS}) = \left[\frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a}}\right] \cdot 1.11$$

where $R_{1_a} = R_{2_a} = 10k$ (internal)

$$I_{REF} = \frac{V_{BG}}{R_2}$$

In terms of R_3

$$R_3 = \frac{[\text{AC output level}(V_{RMS})]\ R_{1_a}}{(1.11)\ (R_{2_a})\ I_{REF}}$$

assuming $R_2 = 100k$ and $V_{BG} = 1.26V$.

$$R_3 = \frac{100mV_{RMS} \cdot 10k}{1.11 \cdot 10k \cdot 12.6\mu A}$$

$$R_3 = 7.15k$$

Step 2: From Eq 2

$$\text{Maximum Gain} = \frac{4(R_3 + R_X) \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{CC}}$$

In terms of R_X

$$R_X = \frac{(\text{Max. Gain})\ (V_{CC})\ (R_{1_a})}{4R_{2_a} \cdot I_{REF}} - R_3$$

$$R_X = \frac{(10)\ (3.6V)\ (10k)}{4\ (10k)\ 12.6\mu A} - 7.15k$$

$$R_X = 707.1k$$

$$R_X = 715k \text{ (available)}$$

Step 3:

–connect resistors to circuit
–measure AC output level and adjust R3 for best accuracy
–check maximum gain by applying a low input level and adjust Rx for best results

Figure 12 shows the characteristics of the NE577/578 ALC circuit without Rx. The output stays at a constant $100mV_{RMS}$ level for a wide range of different input AC voltages. Any AC input signal above the cross-over point (unity gain level) is attenuated while any signal below the cross-over point is amplified. The cross-over point is where the input signal is equal to the output signal, where $A_V=1$.

Figure 13 reveals the dynamic range of the NE577 ALC circuit using Rx. The input range of the ALC is reduced. Instead of a $2mV_{RMS}$ input signal to get $100mV_{RMS}$ on the output, a $10mV_{RMS}$ input signal is now required (for Rx=681k). The purpose of limiting the maximum gain of the circuit is to prevent amplification of background noise. To alleviate this problem, Rx is used. Since the ALC was designed with a maximum gain of 10, any input signal below 10mV will not be amplified with a gain greater than 10 ($100mv_{RMS}/10=10mv_{RMS}$). Using Rx can be an advantage because the threshold of the ALC can be set.

Figure 14 shows that as Rx increases so does A_V. In some applications it might be useful to make Rx a potentiometer. This will allow the user to adjust the threshold for different environmental conditions.

Figures 15-18 show the results of using the ALC for different constant output levels. V_{CC} and I_{REF} limit the dynamic range. The upper part of the range can be increased by either increasing V_{CC} and/or I_{REF}. The lower part of the range can be improved by increasing I_{REF}.

EXTRA FEATURES FOR NE578

The NE578 has three extra functions over the NE577. These are power-down, mute and summing capabilities. To implement the power-down/mute mode, Pin 8 should be active low (open collector configuration, see Figure 19). If the power-down/mute feature is not used, Pin 8 should be left open. The NE578 only consumes 170µA of current at 3.6V when Pin 8 is activated. The power-down/mute mode is useful in designs when the function of the chip is not utilized at all times. This feature is a necessity where power conservation is critical.

In cellular and cordless applications, it is common to mix DTMF tones with the audio signal. This usually requires another op amp in which to mix the signals. With the NE578, however, the DTMF tones can be mixed internally on the compressor side. The DTMF signal is also compressed with the audio signal and ready for data transmission. Figure 2 shows that the summing of signals can be done at Pin 9 with R4 and C10. If amplification is not needed, then a 10k resistor is a recommended value for R4. In addition the summing amplifiers are capable of driving 600Ω loads.

THE NE577 AND NE578 AS A DUAL EXPANDOR

The compressor side can actually be configured as an expandor for both the NE577 and NE578. Figure 20 shows how this can be done. Because Pin 9 of the NE578 is available to the designer, the compressor side can not only be configured as an expandor, but as an expandor with summing capabilities.

OPERATING AT 1.8V

The NE577 and NE578 can operate at 1.8V.

NE577 AND NE578 DEMO BOARDS

Figures 21 shows the DIP package layout for the NE577 and NE578 demo boards, respectively. Figures 22 shows the SO layout for the NE577 and NE578 demo boards, respectively. The layouts are configured such that R1, R2, R3, and Rx can be removed and replaced easily. A switch is also available to change the operating mode of the compressor to an ALC configuration and vice versa (position the switch to the right for ALC mode).

When the compressor side is being evaluated, disconnect Rx completely from the socket on the demo boards. Rx should only be used when the compandor is being used for ALC.

For the NE578 demo board, two extra post are available. One is for power-down; the other is for summing external signals. To power-down, simply ground this post. To sum signals, connect the external signal to the proper post.

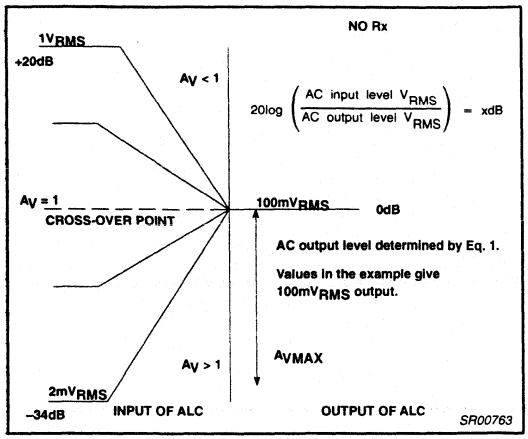


Figure 12 . Dynamic Range of NE577 ALC Demonstration Board Without R_X

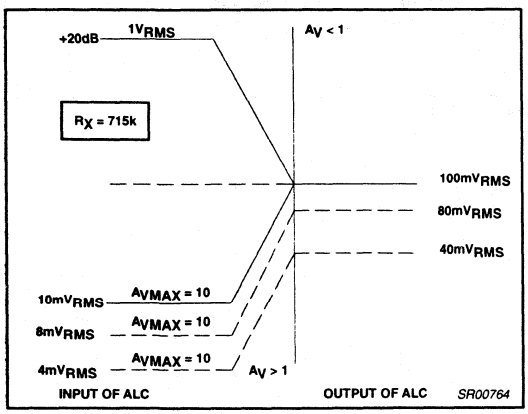


Figure 13 . Dynamic Range of NE577 ALC Demo Board with R_X = 715kΩ

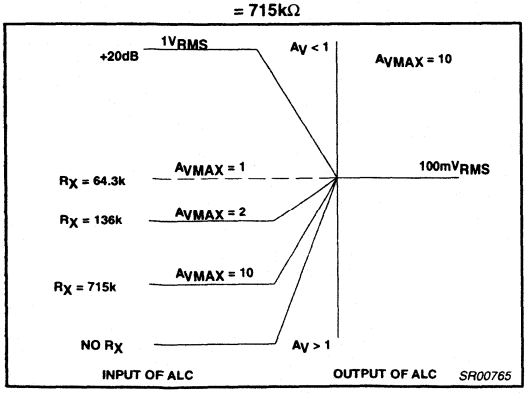


Figure 14 . Dynamic Range of NE577 ALC Demo Board with Different R_X Values

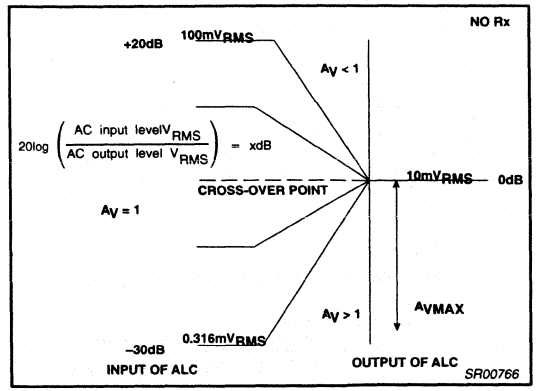


Figure 15 . NE577 ALC: AC Output Level = 10mV$_{RMS}$

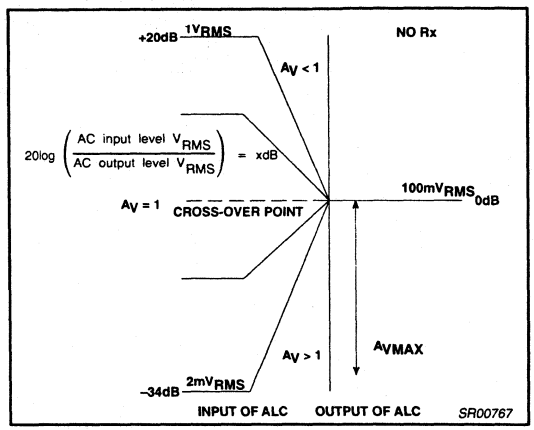


Figure 16 . NE577 ALC: AC Output Level = 100mV$_{RMS}$

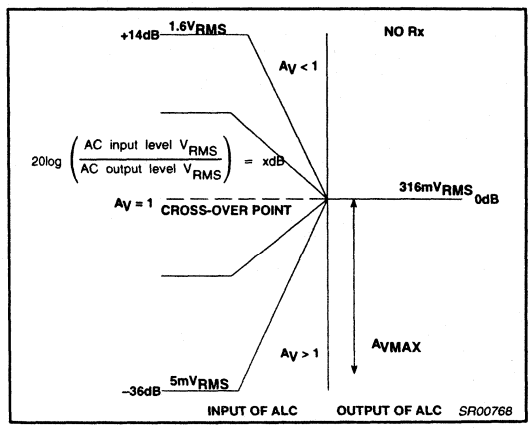


Figure 17 . NE577 ALC: AC Output Level = 316mV$_{RMS}$

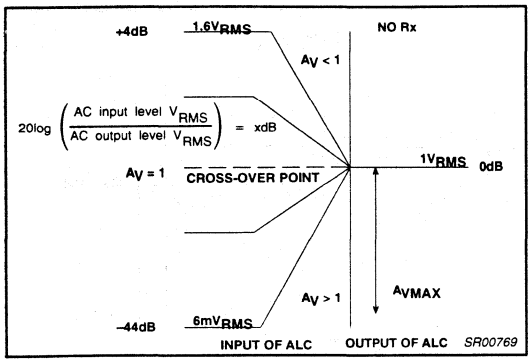


Figure 18 . NE577 ALC: AC Output Level = $1V_{RMS}$

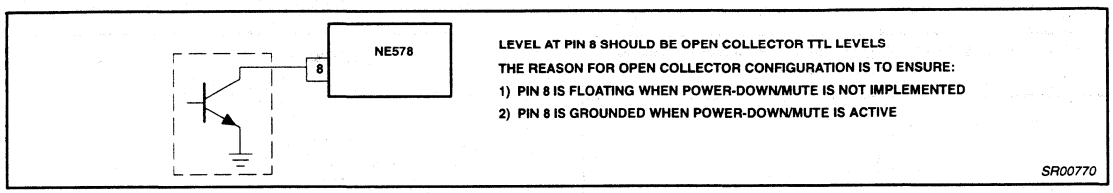


Figure 19 . Proper Use of NE578 Pin 8

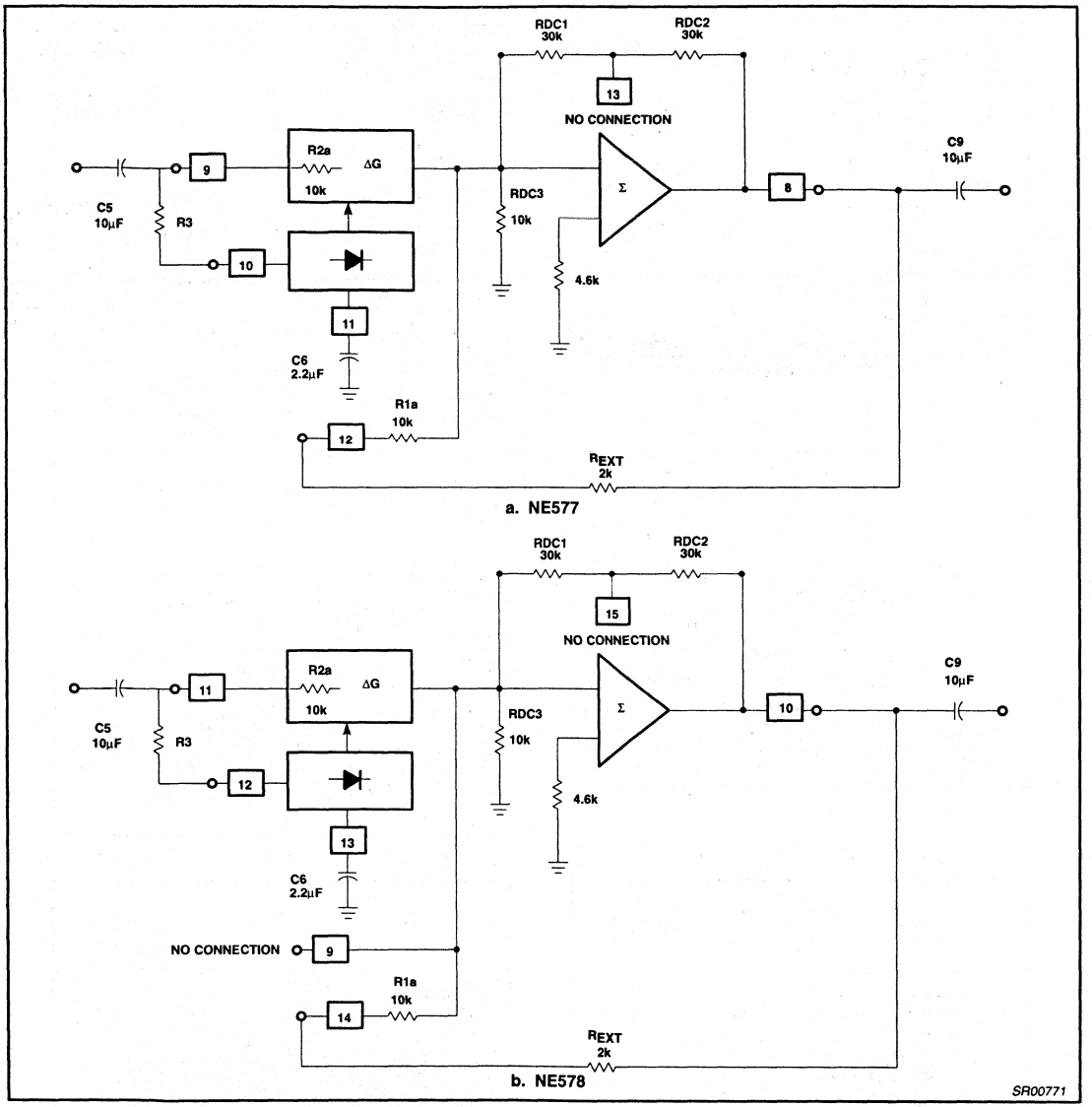
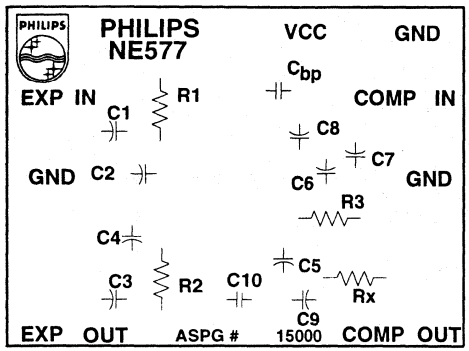
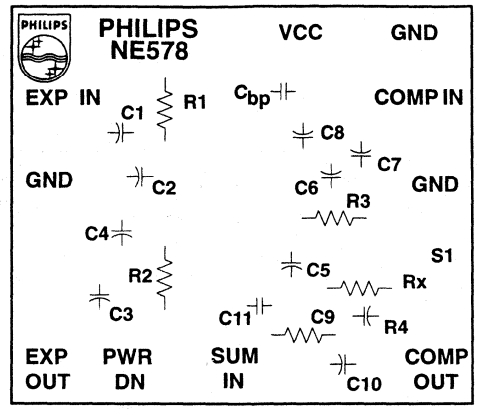


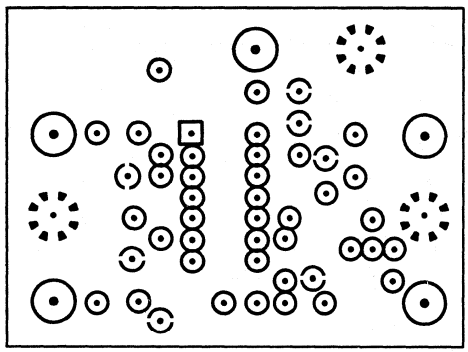
Figure 20 . Expandor Configuration for the Compressor Side



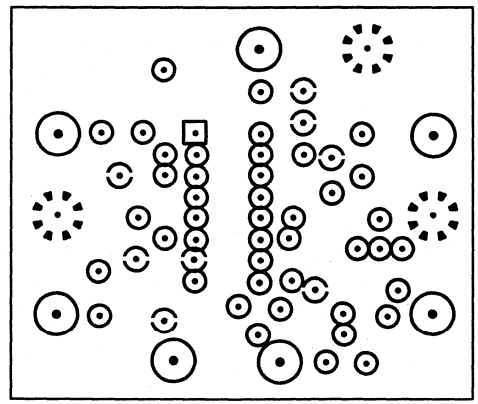
NE577 DIP Top Silk Screen



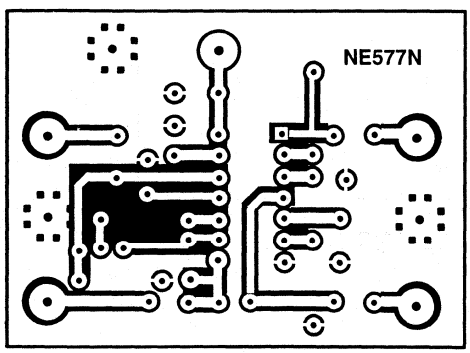
NE578 DIP Top Silk Screen



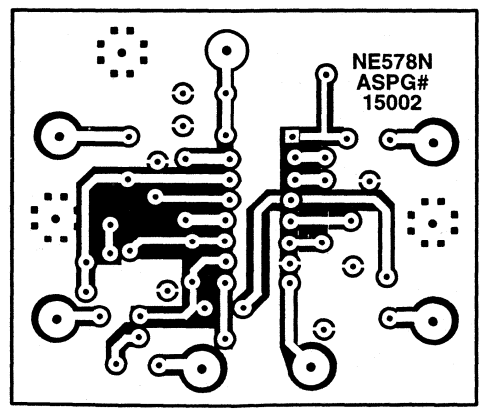
Top View



Top View



Bottom View

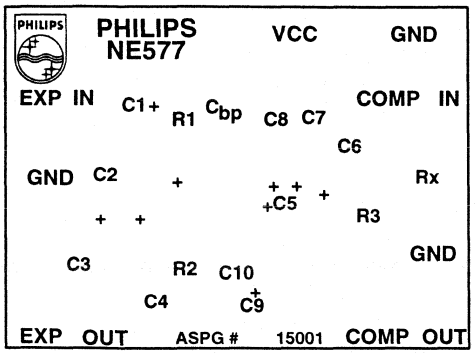


Bottom View

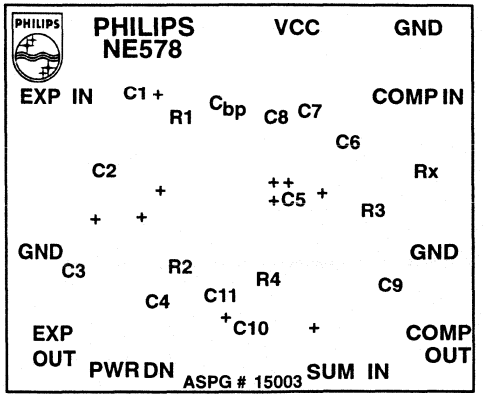
NOTE: C10 eliminated as of 11/30/94.

SR00772

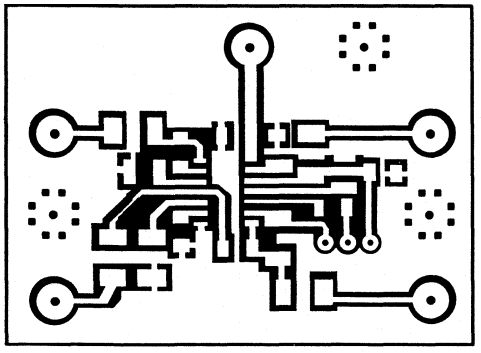
Figure 21 . NE577 and NE578 DIP Application Board Layout



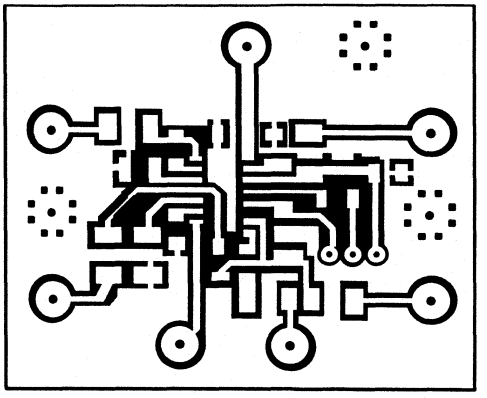
NE577 SO Top Silk Screen



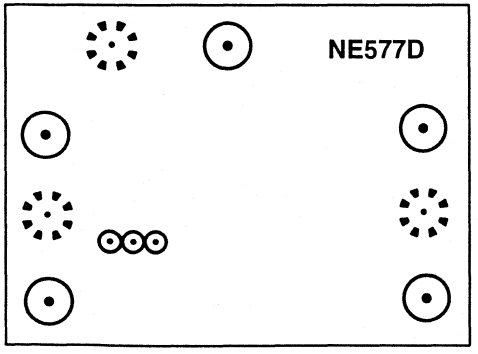
NE578 SO Top Silk Screen



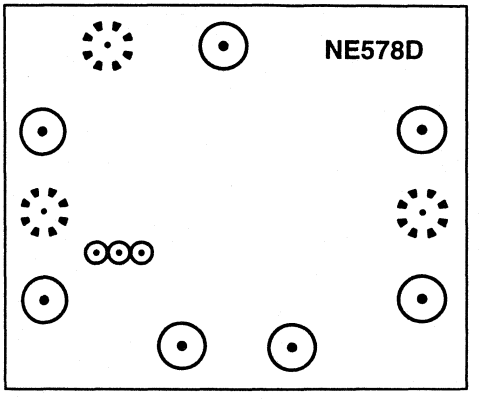
Top View



Top View



Bottom View



Bottom View

NOTE. C11 eliminated as of 11/30/94.

SR00773

Figure 22 . NE577 and NE578 SO Application Board Layout

Section 11
Display Drivers

CONTENTS

PCF2104 family	LCD controller/driver	11–3
PCF2113 family	LCD Driver	11–6
PCF2116 family (PCF2114X; PCF2116X)	LCD controller/drivers	11–61
PCF8566	Universal LCD driver for low multiplex rates	11–66
PCF8576C	Universal LCD driver for low multiplex rates	11–69
PCF8578	LCD row/column driver for dot matrix graphic displays	11–72
PCF8579	LCD column driver for dot matrix graphic displays	11–77

LCD controller/driver PCF2104 family

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF2104 integrated circuit is similar to the PCF2114 but does not contain the high voltage generator. It is optimized for chip-on-glass applications. The letter X in PCF2104X specifies the character set in the Character Generator ROM (CGROM). The different character sets currently available are specified by the letters C and L. Other character sets are available on request.

The PCF2104 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with a 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages which results in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana characters. The PCF2104 interfaces to most microcontrollers via a 4 or 8-bit bus or, via the 2-wire I²C-bus.

Packages

- PCF2104XU/12; chip with bumps on Flexible Film Carrier (FFC)
- Pin grid array PGA144 (samples only).

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM

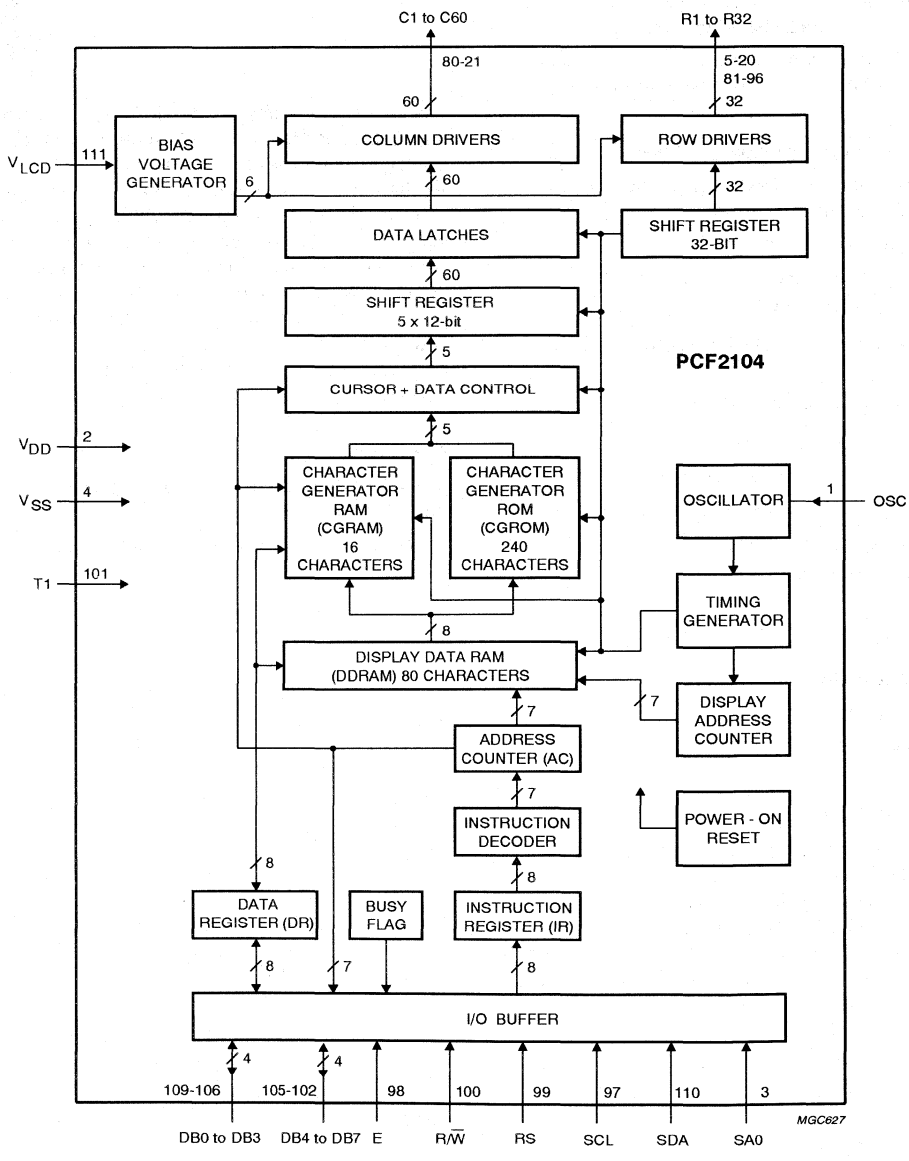


Fig.1 Block diagram.

PINNING

SYMBOL	FFC PAD	DESCRIPTION
OSC	1	oscillator/external clock input
V_{DD}	2	logic supply voltage
SA0	3	I^2C-bus address pin input
V_{SS}	4	ground
R8 to R5	5 to 8	LCD row driver outputs
R32 to R29	9 to12	LCD row driver outputs
R24 to R17	13 to 20	LCD row driver outputs
C60 to C1	21 to 80	LCD column driver outputs
R9 to R16	81 to 88	LCD row driver outputs
R25 to R28	89 to 92	LCD row driver outputs
R1 to R4	93 to 96	LCD row driver outputs
SCL	97	I^2C-bus serial clock input
E	98	data bus clock input
RS	99	register select input
R/$\overline{W}$	100	read/write input
T1	101	test pad input
DB7 to DB0	102 to 109	bidirectional data bus input/output
SDA	110	I^2C-bus serial data input/output
V_{LCD}	111	LCD supply voltage input

FEATURES

- Single chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only
- Icon blink function
- On-chip:
  - generation of LCD supply voltage, independent of V_{DD}, programmable by instruction (external supply also possible)
  - temperature compensation of on-chip generated V_{LCD}: –8 to –12 mV/K at 5.0 V (programmable by instruction)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240, 5 × 8 characters
- Character generator RAM: 16, 5 × 8 characters; 3 characters used to drive 120 icons, 6 characters used if icon-blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I^2C-bus interface
- CMOS compatible
- 18 row, 60 column outputs
- Mux rates 1 : 18 (for normal operation) and 1 : 2 (for icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 1.8 to 4.0 V (up to 5.5 V if external V_{LCD} is used); chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 100 μA):
  - icon mode: <5 μA
  - power-down mode: <1 μA
- Power control mode automatically reduces power when $V_{LCD} \approx V_{DD}$.

Note

Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced.
In most applications it is possible to use V_{DD} as V_{LCD}; never use the voltage generator in icon mode.

GENERAL DESCRIPTION

The PCF2113 is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2 line by 12 and 1 line by 24 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2113 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I^2C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The letter 'X' in PCF2113X characterizes the built-in character set. Various character sets can be manufactured on request.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

PACKAGE

- PCF2113XU; chip in tray
- PCF2113XU/10; chip on FFC
- PCF2113XU/2; chip with bumps in tray
- PCF2113XH; LQFP100.

BLOCK DIAGRAM

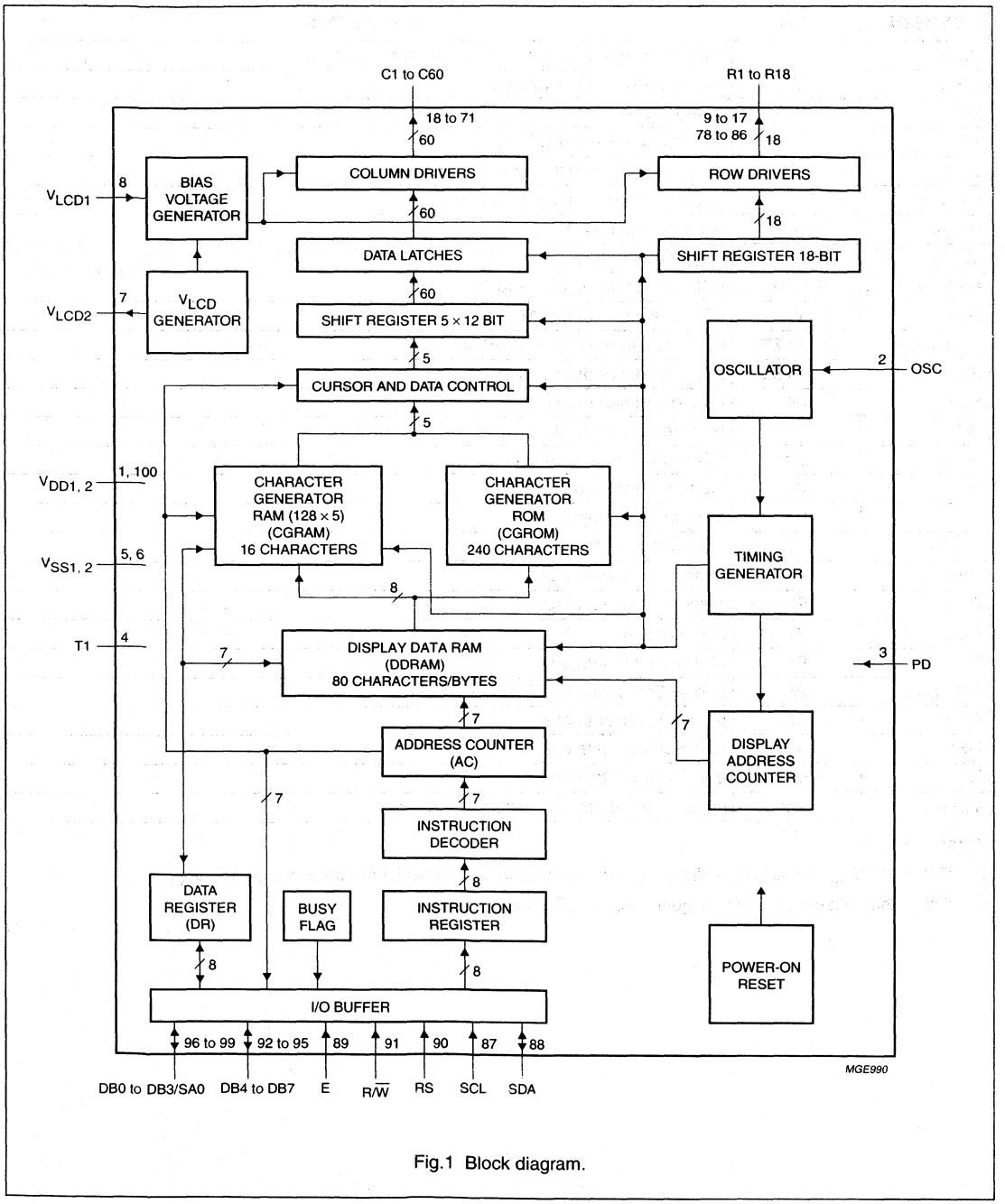


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD1}	1	supply voltage for all except high voltage generator
OSC	2	oscillator/external clock input
PD	3	power-down pad input
T1	4	test pad (connected to V_{SS})
V_{SS1}	5	ground for all except high voltage generator
V_{SS2}	6	ground for high voltage generator
V_{LCD2}	7	V_{LCD} output; note 1
V_{LCD1}	8	V_{LCD} input; note 2
R9 to R16	9 to 16	LCD row driver outputs 9 to 16
R18	17	LCD row driver output 18
C60 to C1	18 to 77	LCD column driver outputs 60 to 1
R8 to R1	78 to 85	LCD row driver outputs 8 to 1
R17	86	LCD row driver output 17
SCL	87	I^2C serial clock input
SDA	88	I^2C serial data input/output
E	89	data bus clock input
RS	90	register select input
$R/\overline{W}$	91	read/write input
DB7	92	bi-directional data bus
DB6	93	bi-directional data bus
DB5	94	bi-directional data bus
DB4	95	bi-directional data bus
DB3/SA0	96	bi-directional data bus/I^2C address pin
DB2	97	bi-directional data bus
DB1	98	bi-directional data bus
DB0	99	bi-directional data bus
V_{DD2}	100	supply voltage for high voltage generator

Notes

1. This is the V_{LCD} output pin, if V_{LCD} is generated internally. This pin has to be connected to V_{LCD1}.
2. This is the voltage used for the generation of LCD bias levels.

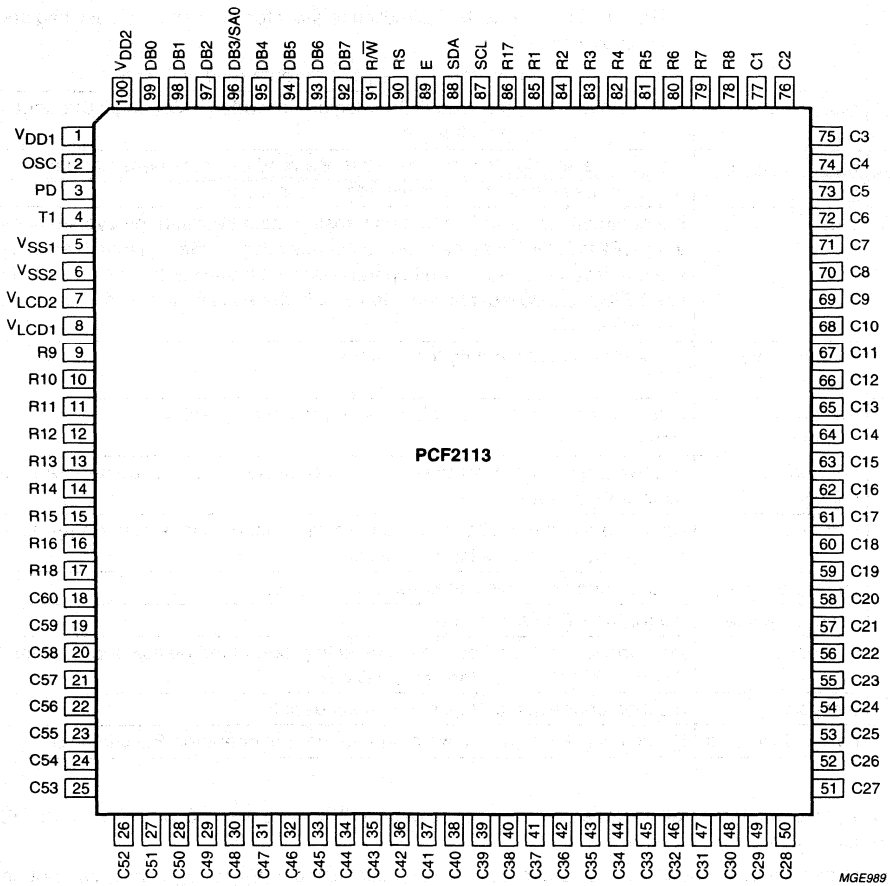


Fig.2 Pin configuration (LQFP100).

Pin functions

NAME	FUNCTION	DESCRIPTION
RS	register select	RS selects the register to be accessed for read and write; there is an internal pull-up on this pin RS = logic 0 selects the instruction register for write and the busy flag and address counter for read RS = logic 1 selects the data register for both read and write
R/$\overline{W}$	read/write	R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation; there is an internal pull-up on this pin
E	data bus clock	the E pin is set high to signal the start of a read or write operation; data is clocked in or out of the chip on the negative edge of the clock
DB7 to DB0	data bus	the bi-directional, 3-state data bus transfers data between the system controller and the PCF2113; DB7 may be used as the busy flag, signalling that internal operations are not yet completed; in 4-bit operations the 4 higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open circuit; there is an internal pull-up on each of the data lines
C1 to C60	column driver outputs	these pins output the data for columns
R1 to R18	row driver outputs	these pins output the row select waveforms to the display; R17 and R18 drive the icons
V_{LCD}	LCD power supply	positive power supply for the liquid crystal display; this may be generated on-chip or supplied externally
OSC	oscillator	when the on-chip oscillator is used this pin must be connected to V_{DD}; an external clock signal, if used, is input at this pin
SCL	serial clock line	input for the I^2C-bus clock signal
SDA	serial data line	I/O for the I^2C-bus data line
SA0	address pin	the hardware sub-address line is used to program the device sub-address for two different PCF2113s on the same I^2C bus
T1	test pad	must be connected to V_{SS}; not user accessible
PD	power-down pad	PD selects chip power-down mode; for normal operation PD = logic 0

Note

1. When I^2C-bus is used, the parallel interface pin E must be defined: E = logic 0. In I^2C-bus read mode DB7 to DB0 should be connected to V_{DD} or left open.
   a) When the parallel bus is used, pins SCL and SDA must be connected to V_{SS} or V_{DD}; they may not be left unconnected.
   b) In case the 4-bit interface is used without reading out from the PCF2113 (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB4 can either be set to V_{SS} or V_{DD} instead of leaving them open.

FUNCTIONAL DESCRIPTION

LCD supply voltage generator

The LCD supply voltage may be generated on-chip. The voltage generator is controlled by two internal 6-bit registers, V_A and V_B. The nominal LCD operating voltage at room temperature is given by the relationships:

$$V_{OP\_nom} = [(\text{integer value of register}) \times 0.08 + 1.82]\ V$$

Programming ranges are as follows (t_{ref} = 27 °C)

Programmed value: 1 to 63.
Voltage: 1.90 to 6.84 V.

Values producing more than 6.5 V at operating temperature are not allowed. Operation above this voltage may damage the device. When programming the operating voltage the V_{LCD} temperature coefficient must be taken into account.

Values below 2.2 V are below the specified operating range of the chip and are therefore not allowed.

Value 0 for V_A and V_B switches the generator off (i.e. V_A = 0 in character mode, V_B = 0 in icon mode, $V_A = V_B = 0$ in power control mode switches the generator off).

Usually register V_A is programmed with the voltage for character mode and register V_B with the voltage for icon mode.

When V_{LCD} is generated on-chip the V_{LCD} pins should be decoupled to V_{SS} with a suitable capacitor. The generated V_{LCD} is independent of V_{DD} and is temperature compensated. When the generator is switched off an external voltage may be supplied at connected pins $V_{LCD1,2}$. $V_{LCD1,2}$ may be higher or lower than V_{DD}.

The LCD supply voltage generator ensures that, as long as V_{DD} is in the valid range (1.8 to 4 V), the required peak voltage V_{OP} = 5.2 V can be generated at any time.

LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels and is given by the relationships given in Tables 1 and 2. Using a 5-level bias scheme for 1 : 18 maximum rate allows V_{LCD} <5 V for most LCD liquids.

Table 1 Optimum/maximum values for V_{OP} (off pixels start darkening; $V_{off} = V_{th}$)

MUX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.272	3.7	5.2 V
1 : 2	3	2.236	2.283	3.9 V

Table 2 Minimum values for V_{OP} (on pixels clearly visible; $V_{on} > V_{th}$)

MUX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.12	3.2	4.6 V
1 : 2	3	1.2	1.5	2.1 V

Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC pin must be connected to V_{DD}.

External clock

If an external clock is to be used this is input at the OSC pin. The resulting display frame frequency is given by

$$f_{frame} = \frac{f_{OSC}}{3072}$$

Only in the power-down state is the clock allowed to be stopped (OSC connected to V_{ss}), otherwise the LCD is frozen in a DC state.

Power-on reset

The on-chip power-on reset block initializes the chip after power-on or power failure. This is a synchronous reset and requires 3 OSC cycles to be executed.

Power-down mode

The chip can be put into power-down mode where all static currents are switched off (no internal oscillator, no bias level generation, all LCD-outputs are internally connected to V_{SS}) when PD = logic 1.

During power-down information in RAMs and the chip state are preserved. Instruction execution during power-down is possible when externally clocking pad OSC.

The device should be put into 'display off' mode (instruction 'display control') before putting the chip in power-down mode, otherwise the LCD output voltages are not defined.

Registers

The PCF2113 has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed. The instruction register stores instruction codes such as 'display clear' and 'cursor shift', and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written from but not read by the system controller. The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the 'read data' instruction.

Busy flag

The busy flag indicates the internal status of the PCF2113. Logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output to pin DB7 when RS = logic 0 and R/$\overline{W}$ = logic 1. Instructions should only be written after checking that the busy flag is logic 0 or waiting for the required number of cycles.

Address Counter (AC)

The address counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands 'set CGRAM address' and 'set DDRAM address'. After a read/write operation the address counter is automatically incremented or decremented by 1.
The address counter contents are output to the bus (DB6 to DB0) when RS = logic 0 and R/$\overline{W}$ = logic 1.

Display Data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data represented by 8-bit character codes.

RAM locations which are not used for storing display data can be used as general purpose RAM. The basic RAM to display addressing scheme is shown in Fig.3. With no display shift the characters represented by the codes in the first 24 RAM locations starting at address 00 in line 1 are displayed. Figures 4 and 5 show the display mapping for right and left shift respectively.

When data is written to or read from the DDRAM wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together.
The address ranges and wrap- around operations for the various modes are shown in Table 3.

Table 3 Address space and wrap-around operation

MODE	1 × 24	2 × 12
address space	00 to 4F	00 to 27; 40 to 67
read/write wrap-around (moves to next line)	4F to 00	27 to 40; 67 to 00
display shift wrap-around (stays within line)	4F to 00	27 to 00; 67 to 40

Character Generator ROM (CGROM)

The Character Generator ROM (CGROM) generates 240 character patterns in 5 x 8 dot format from 8-bit character codes. Figures 7 to 9 show the character sets that are currently implemented.

Character Generator RAM (CGRAM)

Up to 16 user defined characters may be stored in the Character Generator RAM (CGRAM). Some CGRAM characters (see Fig.17) are also used to drive icons (6 if icons blink and both icon rows are used in application; 3 if no blink but both icon rows are used in application; 0 if no icons are driven by the icon rows). The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.7). Figure 10 shows the addressing principle for the CGRAM.

Cursor control circuit

The cursor control circuit generates the cursor (underline and/or cursor blink as shown in Fig.6) at the DDRAM address contained in the address counter. When the address counter contains the CGRAM address the cursor will be inhibited.

Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

LCD row and column drivers

The PCF2113 contains 18 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 11 to 13 show typical waveforms. Unused outputs should be left unconnected.

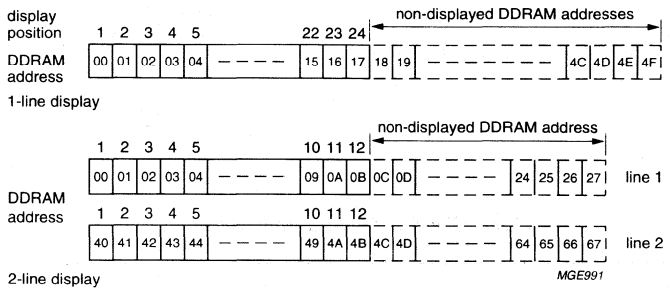


Fig.3 DDRAM to display mapping: no shift.

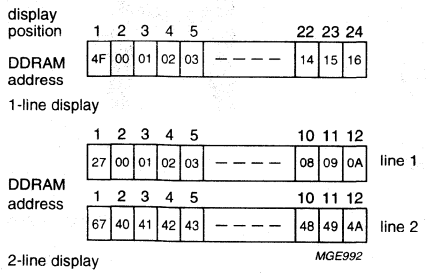


Fig.4 DDRAM to display mapping: right shift.

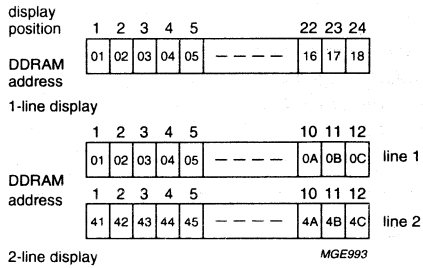


Fig.5 DDRAM to display mapping: left shift.

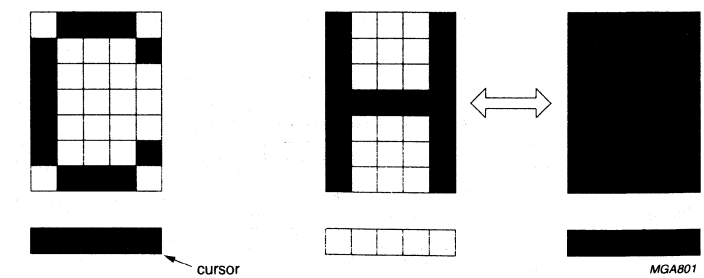
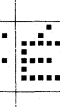
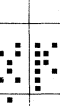


Fig.6 Cursor and blink display examples.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

MGE994

Fig.7 Character set 'A' in CGROM.

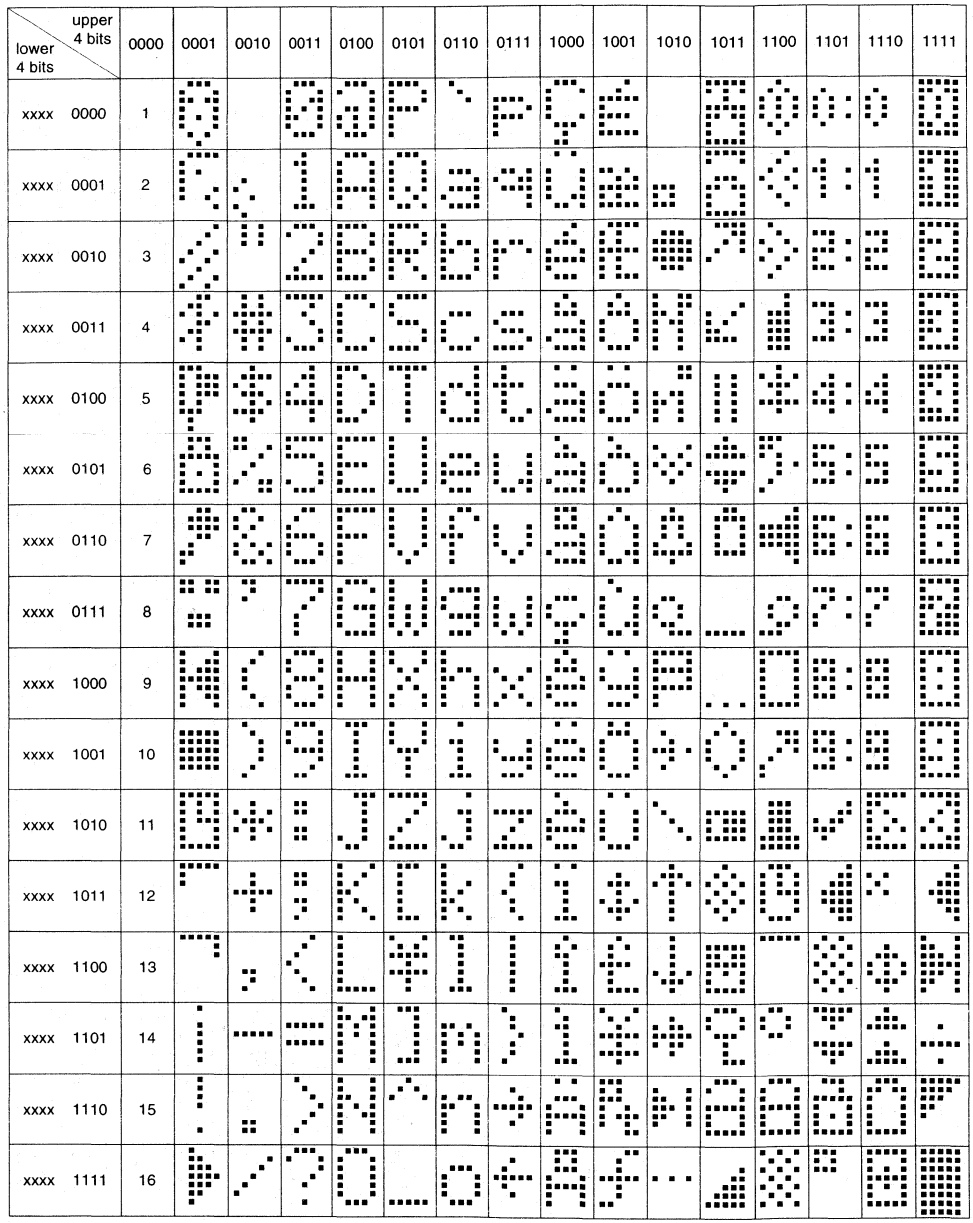
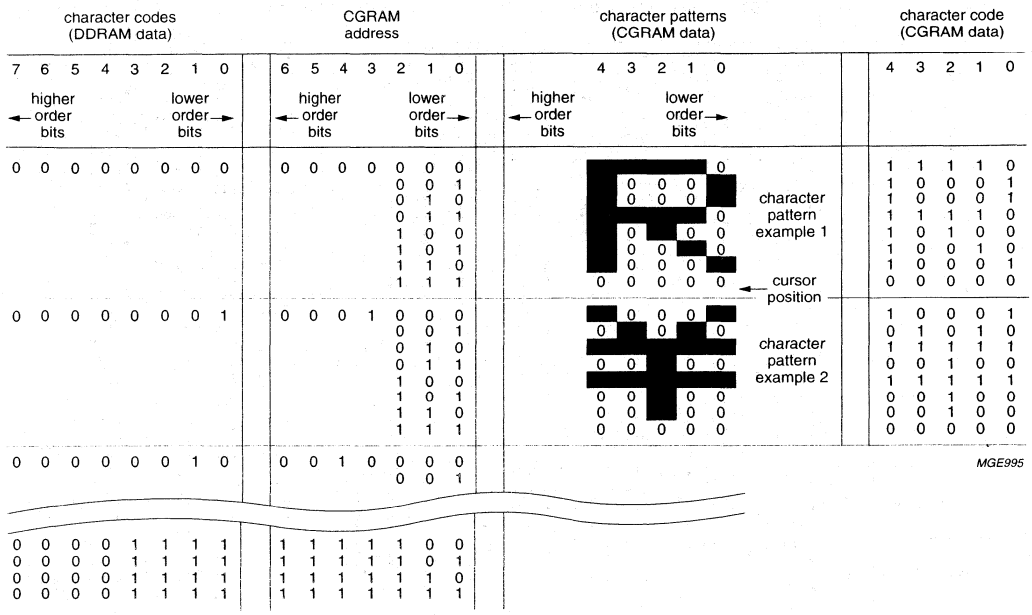


Fig.8 Character set 'D' in CGROM.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

MGD689

Fig.9 Character set 'E' in CGROM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th position will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in Fig.7.

As shown in Figs 7 and 10, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'set CGRAM address' command. Bit 6 can be set using the 'set DDRAM address' command in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'read busy flag and address counter' command.

Fig.10 Relationship between CGRAM addresses and data and display patterns.

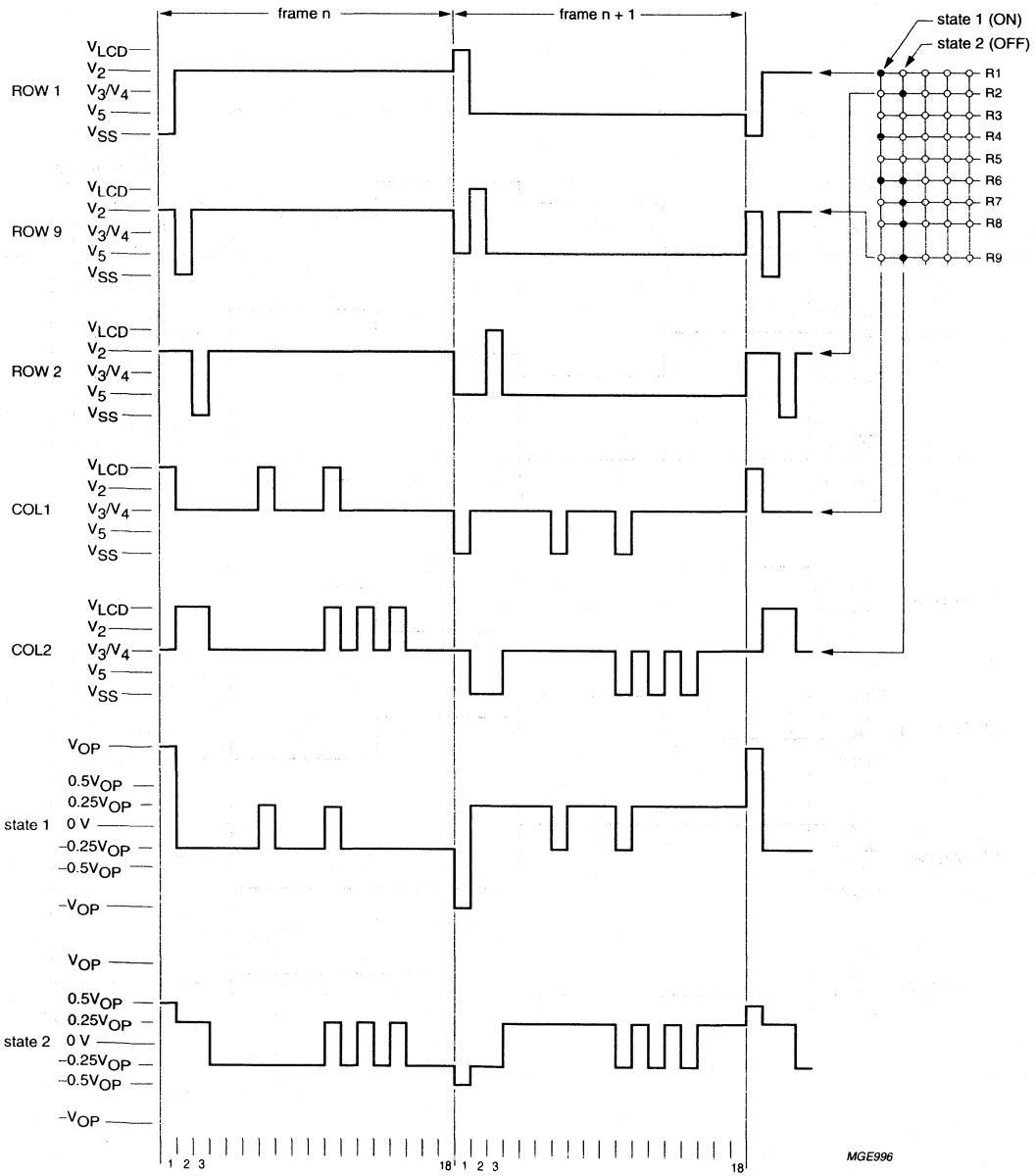


Fig.11 Typical LCD waveforms; character mode.

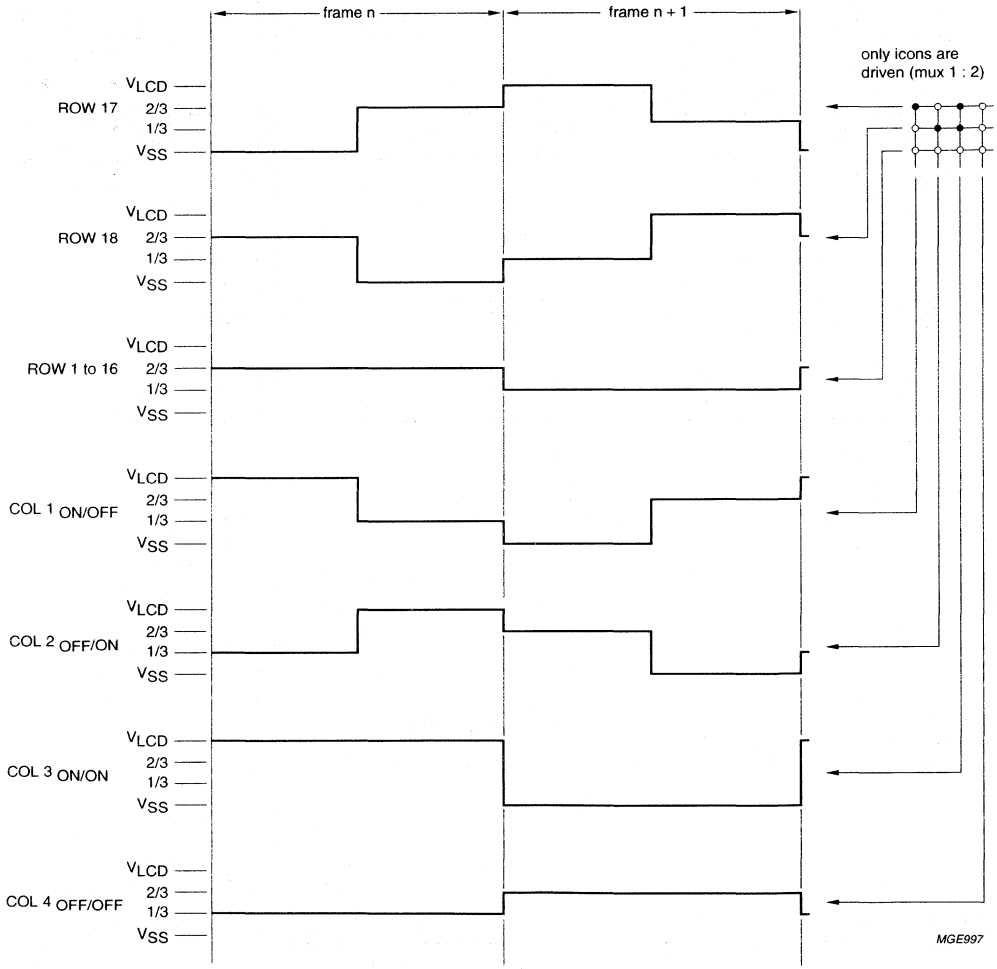
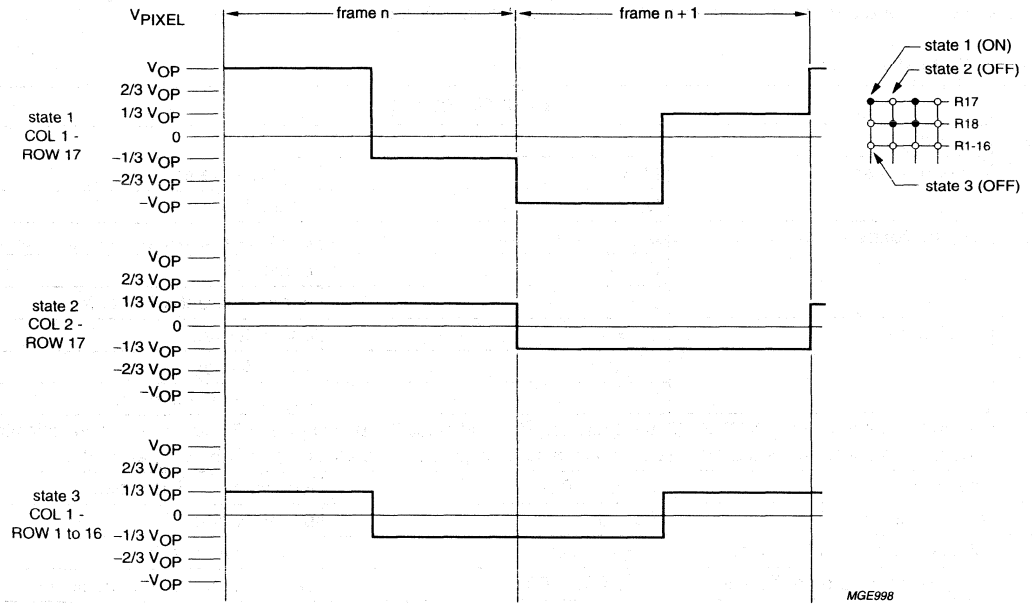


Fig.12 Mux 1 : 2 LCD waveforms; icon-mode.



$V_{ON(rms)} = 0.745V_{OP}$.

$V_{OFF(rms)} = 0.333V_{OP}$.

$$D = \frac{V_{ON}}{V_{OFF}} = 2.23$$

Fig.13 Mux 1 : 2 LCD waveforms; icon-mode.

Reset function

The PCF2113 automatically initializes (resets) when power is turned on. The reset executes a 'clear display', requiring 165 OSC cycles, and after the reset the chip has the state shown in Table 4.

Table 4 State after reset

STEP	DESCRIPTION		
1	clear display		
2	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
3	display control	D = 0	display off
		C = 0	cursor off
		B = 0	cursor character blink off
4	function set	DL = 1	8-bit interface
		M = 0	1-line display
		H = 0	normal instruction set
5	default address pointer to DDRAM; the busy flag (BF) indicates the busy state (BF = logic 1) until initialization ends; the busy state lasts 2 ms; the chip may also be initialized by software; see Tables 17 and 18		
6	icon control	IM, IB = 00	icons/icon blink disabled
7	power control	PC = 0	power control off
8	display/screen configuration	L, P, Q = 000	default configurations
9	V_{LCD} temperature coefficient	TC1, TC2 = 00	default temperature coefficient
10	set V_{LCD}	V_A, V_B = 0 (V_{LCD} generator off)	
11	I^2C-bus interface reset		

INSTRUCTIONS

Only two PCF2113 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Before internal operation, control information is stored temporarily in these registers, to allow interface to various types of MPUs which operate at different speeds or to allow interface to peripheral control ICs.
The PCF2113 operation is controlled by the instructions shown in Table 5 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate PCF2113 functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the MPU program load.
The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than the 'read busy flag' and 'read address' instruction will be executed. Because the busy flag is set to logic 1 while an instruction is being executed, check to make sure it is on logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 5. An instruction sent while the busy flag is logic 1 will not be executed.

Table 5 Instruction set for I²C-bus commands

CONTROL BYTE								COMMAND BYTE								I²C-BUS COMMANDS
Co	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	note 1

Note

1. R/$\overline{W}$ is set together with the slave address.

Table 6 instruction set with parallel bus commands; note 1

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 0 or 1												
NOP	0	0	0	0	0	0	0	0	0	0	no operation	3
Function set	0	0	0	0	1	DL	0	M	0	H	sets interface Data Length (DL) and number of display lines (M); extended minstr. set control (H)	3
Read busy flag and address counter	0	1	BF	A_C							reads the Busy Flag (BF) indicating internal operating is being performed and reads address counter contents	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data from CGRAM or DDRAM	3
H = 0												
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 0 in address counter	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 0 in address counter; also returns shifted display to original position; DDRAM contents remain unchanged	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction and specifies shift of display; these operations are performed during data write and read	3
Display control	0	0	0	0	0	0	1	D	C	B	sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B); D = 0 (display off) puts chip into power-down mode	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	moves cursor and shifts display without changing DDRAM contents	3
Set CGRAM address	0	0	0	1	A_{CG}						sets CGRAM address; bit 6 is to be set by the command 'set DDRAM address'; look at the description of the commands	3
Set DDRAM address	0	0	1	A_{DD}							sets DDRAM address	3

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 1												
Reserved	0	0	0	0	0	0	0	0	0	1	do not use	–
Screen configuration	0	0	0	0	0	0	0	0	1	L	set screen configuration	3
Display configuration	0	0	0	0	0	0	0	1	P	Q	set display configuration	3
Icon/power control	0	0	0	0	0	0	1	IM	IB	PC	set icon mode (IM), icon blink (IB), power control (PC)	3
Temperature control	0	0	0	0	0	1	0	0	TC1	TC2	set temperature coefficient (TCx)	3
Reserved	0	0	0	1	X	X	X	X	X	X	do not use	–
Set V_{LCD}	0	0	1	V	voltage						store V_{LCD} in register V_A or V_B (V)	3

Note

1. X = don't care.

Table 7 Explanations of symbols used in Table 6

BIT	0	1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	cursor character blink off: character at cursor position does not blink	cursor character blink on: character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
H	use basic instruction set	use extended instruction set
L (no impact, if M = 1)	left/right screen: standard connection (as in PCF2114); 1st 12 chararacters of 24: columns are from 1 to 60 2nd 12 characters of 24: columns are from 1 to 60	left/right screen: mirrored connection (as in PCF2116); 1st 12 characters of 24: columns are from 1 to 60 2nd 12 characters of 24: columns are from 60 to 1
P	column data: left to right (as in PCF2116); column data is displayed from 1 to 60	column data: right to left; column data is displayed from 60 to 1
Q	row data: top to bottom (as in PCF2116); row data is displayed from 1 to 16 and icon row data is in 17 and 18	row data: bottom to top; row data is displayed from 16 to 1 and icon row data is in 18 and 17
IM	character mode; full display	icon mode; only icons displayed
IB	icon blink disabled	icon blink enabled
PC	power control off; V_{LCD} = programmed value	power control on; voltage generator is switched off and V_{DD} is used for V_{LCD} if $V_B < V_{DD} < V_A$
V	set V_A	set V_B
M	1-line by 24 display	2-line by 12 display
C_0	last control byte; see Table 5	another control byte follows after data/command

Table 8 Explanation of TC1 and TC2 used in Table 6

TC1	TC2	DESCRIPTION
0	0	V_{LCD} temperature coefficient 0
1	0	V_{LCD} temperature coefficient 1
0	1	V_{LCD} temperature coefficient 2
1	1	V_{LCD} temperature coefficient 3; for ranges for TC see Chapter "DC characteristics"

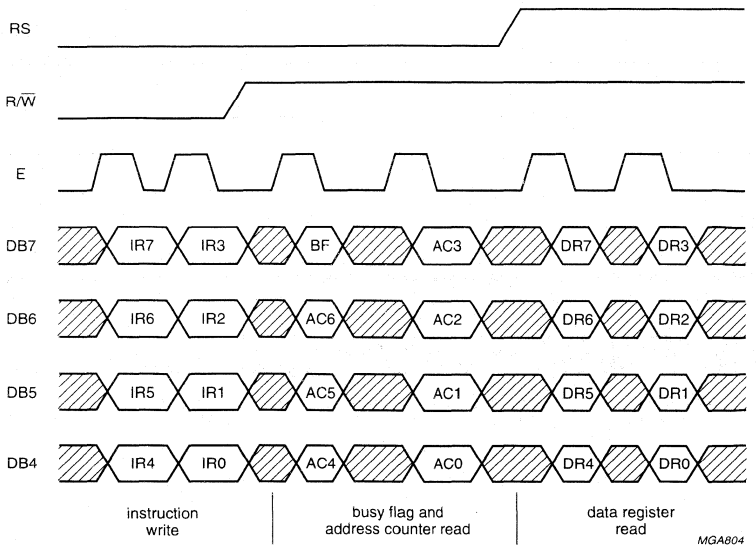
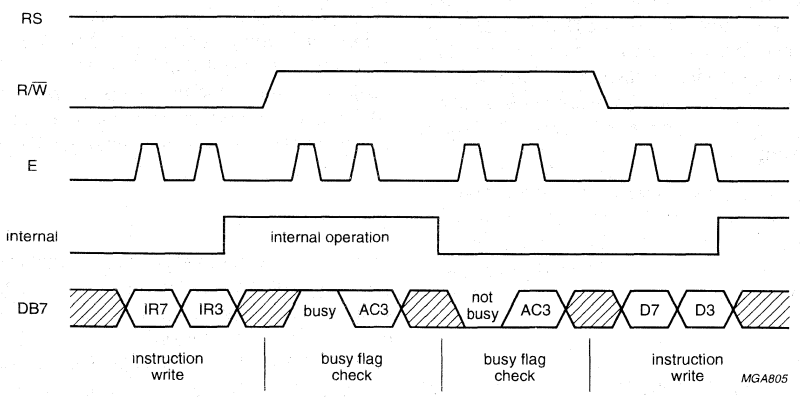


Fig.14 4-bit transfer example.



IR7, IR3: instruction 7th, 3rd bit.
AC3: address counter 3rd bit.
D7, D3: data 7th, 3rd bit.

Fig.15 An example of 4-bit data transfer timing sequence.

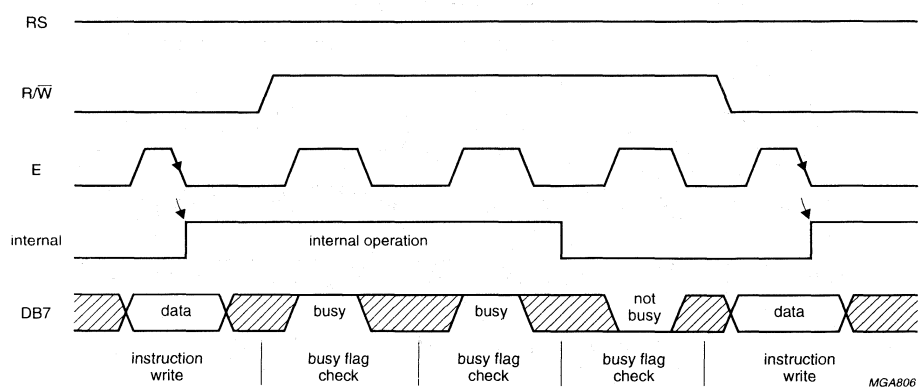


Fig.16 Example of busy flag checking timing sequence.

Clear display

'Clear display' writes character code 20 (hexadecimal) into all DDRAM addresses (the character pattern for character code 20 must be blank pattern), sets the DDRAM address counter to logic 0 and returns display to its original position if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display. Sets entry mode I/D = logic 1 (increment mode). S of entry mode does not change.

The instruction 'clear display' requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

Return home

'Return home' sets the DDRAM address counter to logic 0 and returns display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

Entry mode set

I/D

When I/D = logic 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

S

When S = logic 1, the entire display shifts either to the right (I/D = logic 0) or to the left (I/D = logic 1) during a DDRAM write. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing into or reading out of the CGRAM. When S = logic 0 the display does not shift.

Display control (and partial power-down mode)

D

The display is on when D = logic 1 and off when D = logic 0. Display data in the DDRAM are not affected and can be displayed immediately by setting D to logic 1.

When the display is off (D = logic 0) the chip is in partial power-down mode:

- The LCD-outputs are connected to V_{SS}
- The LCD generator and bias generator are turned off.

3 OSC cycles are required after sending the 'display off' instruction to ensure all outputs are at V_{SS}, afterwards OSC can be stopped. If the oscillator is running during partial power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (OSC = V_{SS}).

To ensure $I_{DD} < 1\ \mu A$ the parallel bus pins DB7 to DB0 should be connected to V_{DD}; RS, R/$\overline{W}$, to V_{DD} or left open and PD to V_{DD}. Recovery from power-down mode: PD back to logic 0, if necessary OSC back to V_{DD}, send a 'display control' instruction with D = logic 1.

C

The cursor is displayed when C = logic 1 and inhibited when C = logic 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.6).

B

The character indicated by the cursor blinks when B = logic 1. The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 s, with $f_{BLINK} = \frac{f_{OSC}}{52\,224}$

The cursor underline and the cursor character blink can be set to display simultaneously.

Cursor or display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor shift'.

Function set

DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = logic 1 or in two nibbles (DB7 to DB4) when DL = logic 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 should be left open (internal pull-ups). Hence in the first 'function set' instruction after power-on N and H are set to logic 1. A second 'function set' must then be sent (2 nibbles) to set N and H to their required values.

'Function set' from I^2C-interface sets the DL bit to logic 1.

M

Chooses either 1-line by 24 display (M = 0) or 2-line by 12 display (M = 1).

H

When H = logic 0 the chip can be programmed via the standard 11 instruction codes used in the PCF2116 and other LCD controllers.

When H = logic 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons.

Set CGRAM address

'Set CGRAM address' sets bits 5 to 0 of the CGRAM address A_{CG} into the address counter (binary A[5] to A[0]). Data can then be written to or read from the CGRAM.

Attention: the CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (binary A[6] to A[0]). With the 'set CGRAM address' command, only bits 5 down to 0 are set. Bit 6 can be set using the 'set DDRAM address' command first, or by using the auto-increment feature during CGRAM write. All bits 6 to 0 can be read using the 'read busy flag' and 'read address' command.

When writing to the lower part of the CGRAM, make sure that bit 6 of the address is not set (e.g. by an earlier DDRAM write or read action).

Set DDRAM address

'Set DDRAM address' sets the DDRAM address A_{DD} into the address counter (binary A[6] to A[0]). Data can then be written to or read from the DDRAM.

Read busy flag and read address

'Read busy flag' and 'read address' read the Busy Flag (BF) and Address Counter (AC). BF = logic 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = logic 0. It is recommended that the BF status is checked before a next write operation is executed.

At the same time, the value of the address counter expressed in binary A[6] to A[0] is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data D[7] to D[0] to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous 'set CGRAM address' or 'set DDRAM address' command. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D[4] to D[0] of CGRAM data are valid, bits D[7] to D[5] are 'don't care'.

Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent 'set address' command determines whether the CGRAM or DDRAM is to be read.

The 'read data' instruction gates the content of the Data Register (DR) to the bus while E is high. After E goes low again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

Note: the only three instructions that update the Data Register (DR) are:

- 'set CGRAM address'
- 'set DDRAM address'
- 'read data' from CGRAM or DDRAM.

Other instructions (e.g. 'write data', 'cursor/display shift', 'clear display', 'return home') do not modify the data register content.

EXTENDED FUNCTION SET INSTRUCTIONS AND FEATURES

New instructions

H = logic 1 sets the chip into alternate instruction set mode.

Icon control

The PCF2113 can drive up to 120 icons. See Fig.17 for CGRAM to icon mapping.

IM

When IM = logic 0 the chip is in character mode. In character mode characters and icons are driven (mux 1 : 18). The V_{LCD} generator, if used, produces the V_{LCD} voltage programmed in register V_A.

When IM = logic 1 the chip is in icon mode. In icon mode only the icons are driven (mux 1 : 2) and the V_{LCD} voltage generator, if used, produces the V_{LCD} voltage programmed in register V_B.

Power control (see Section "PC") can be used in both icon and character mode to save current. In this case, when $V_B < V_{DD} < V_A$ the V_{LCD} voltage generator is switched off and V_{DD} is used as V_{LCD}.

IB

Icon blink control is independent of the cursor/character blink function.

When IB = logic 0 icon blink is disabled. Icon data is stored in CGRAM character 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons).

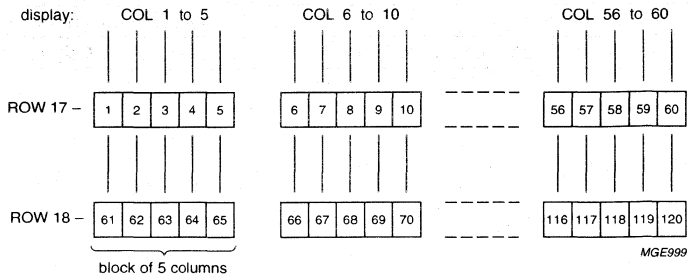
When IB = logic 1 icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons). These bits also define icon state when icon blink is not used.

Icon states for the odd phase are stored in CGRAM character 4 to 6 (another 120 bits for the 120 icons). When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

Table 9 Blink effect for icons and cursor character blink

PARAMETER	EVEN PHASE	ODD PHASE
Cursor underline	on	off
Cursor character blink	block (all on)	normal (display character)
Icons	state 1: CGRAM character 0 to 2	state 2: CGRAM character 4 to 6



icon no.	phase	ROW/COL	character codes	CGRAM address	CGRAM data	icon view
			7 6 5 4 3 2 1 0 MSB LSB	6 5 4 3 2 1 0 MSB LSB	4 3 2 1 0 MSB LSB	
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
56-60	even	17/56-60	0 0 0 0 0 0 0 1	0 0 0 1 0 1 1	1 1 1 1 1	
61-65	even	18/1-5	0 0 0 0 0 0 0 1	0 0 0 1 1 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	even	18/56-60	0 0 0 0 0 0 1 0	0 0 1 0 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	odd (blink)	18/56-60	0 0 0 0 0 1 1 0	0 1 1 0 0 1 1	0 0 1 1 0	

MGG001

CGRAM data bit = logic 1 turns the icon on, data bit = logic 0 turns the icon off.
Data in character codes 0 to 2 define the icon-states when icon blink is disabled or during the even phase when icon blink is enabled.
Data in character codes 4 to 6 define the icon-state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled).

Fig.17 CGRAM to icon mapping.

PC

PC = logic 1 enables power control. If V_{DD} lies above both programmed V_{LCD} values, V_A and V_B, V_A is generated. If V_{DD} lies below both programmed values, V_B is generated. If $V_B < V_{DD} < V_A$ the V_{LCD} generator is switched off and V_{DD} is used as V_{LCD}, thus reducing current consumption. This can be useful in many cases (e.g. battery operation in icon mode). Current consumption is reduced by about a factor 4 compared to character mode mux 1 : 18.

To disable power control send the 'icon/power control' instruction with PC = 0.

Power control operation

IM	PC	CONDITION	V_{LCD}
Power control off			
0	0	character mode	generates V_A
1	0	icon mode	generates V_B
Power control on (character or icon mode)			
X(1)	1	$V_{DD} > V_A$	generates V_A
		$V_B < V_{DD} < V_A$	use V_{DD}
		$V_{DD} < V_A$ and $< V_B$	generates V_B

Note

1. X = don't care.

Screen configuration

L: default is L = logic 0.

L = logic 0: the two halves of a split screen are connected in a standard way i.e. column 1/61, 2/62 to 60/120.

L = logic 1: the two halves of a split screen are connected in a mirrored way i.e. column 1/120, 2/119 to 60/61. This allows single layer PCB or glass layout.

Display configuration

P, Q: default is P, Q = logic 0.

P = logic 1 mirrors the column data.

Q = logic 1 mirrors the row data.

TC1, TC2

Default is TC1, TC2 = logic 0. This selects the default temperature coefficient for the internally generated V_{LCD}. TC1,TC2 = 10,01 and 11 selects alternative temperature coefficients 1, 2 and 3 respectively.

Set V_{LCD}

V_{LCD} value is programmed by instruction. Two on-chip registers hold V_{LCD} values for character mode and icon mode respectively (V_A and V_B). The generated V_{LCD} value is independent of V_{DD}, allowing battery operation of the chip.

V_{LCD} programming:

1. send 'function set' instruction with H = 1
2. send set 'V_{LCD} instruction' to write to voltage register:
   a) DB7, DB6 = 10: DB5 to DB0 are V_{LCD} of character mode (V_A)
   b) DB7, DB6 = 11: DB5 to DB0 are V_{LCD} of icon mode (V_B)
   c) DB5 to DB0 = 000000 switches V_{LCD} generator off (when selected)
   d) During 'display off' and power-down V_{LCD} generator is also disabled
3. send 'function set' instruction with H = 0 to resume normal programming.

V_{LCD} with power control: V_{DD} is used instead of generating V_{LCD} when $V_B < V_{DD} < V_A$ (see Section "Icon control"). Power control is controlled by the 'icon/power control' instruction.

Reducing current consumption

Reducing current consumption can be achieved by one of the options mentioned in Table 10.

Table 10 Reducing current consumption

ORIGINAL MODE	ALTERNATIVE MODE
Character mode	icon mode (control bit IM)
Display on	display off (control bit D)
Any mode	power-down (PD pin)
V_{LCD} generation	power control (control bit PC) V_{DD} used for V_{LCD} when $V_B < V_{DD} < V_A$ (V_{LCD} generator switched off)

When V_{LCD} lies outside the V_{DD} range and must be generated, it is usually more efficient to use the on-chip generator than an external regulator.

Table 11 Use of the V_A and V_B registers

MODE	V_A	V_B
Normal operation	V_{LCD} character mode	V_{LCD} icon mode
Power control	V_{LCD} upper limit	V_{LCD} lower limit

INTERFACE TO MPU: PARALLEL INTERFACE

The PCF2113 can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS, and R/$\overline{W}$ are required. See Chapter "Pin functions".

In 4-bit mode data is transferred in two cycles of 4 bits each using pins DB7 to DB4 for transaction. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second. Data transfer is complete after two 4-bit data transfers. Note that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction. See Figs 14 to 17 for examples of bus protocol.

In 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

INTERFACE TO MPU: I²C-BUS INTERFACE

Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF2113 read and write cycles is shown in Figs 23 to 24. The slow down feature of the I²C-bus protocol (receiver holds SCL low during internal operations) is not used in the PCF2113.

Definitions

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

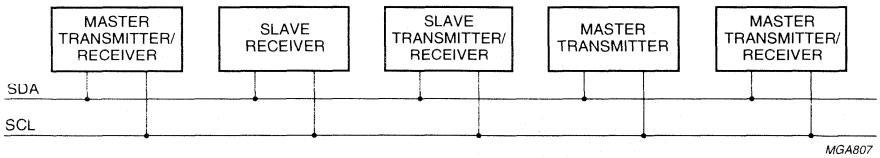


Fig.18 System configuration.

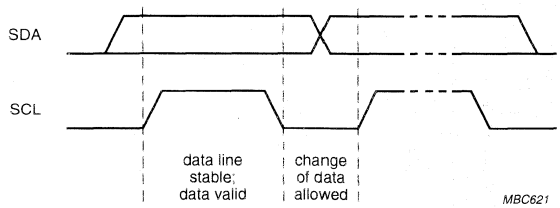


Fig.19 Bit transfer.

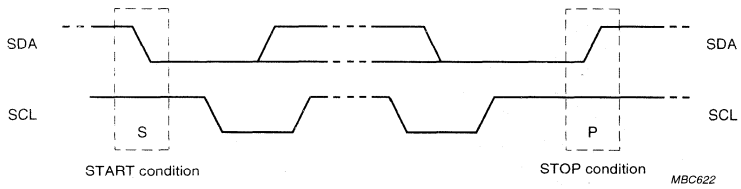


Fig.20 Definition of START and STOP conditions.

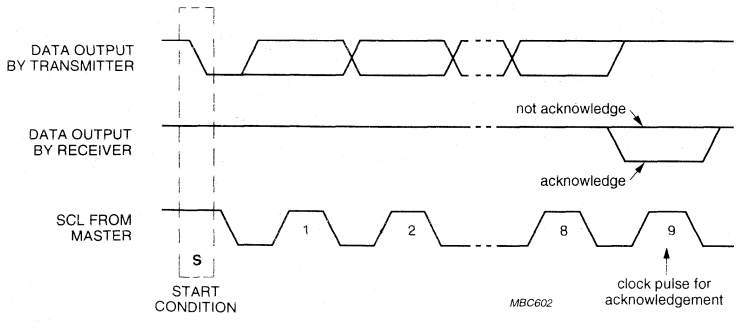


Fig.21 Acknowledgement on the I²C-bus.

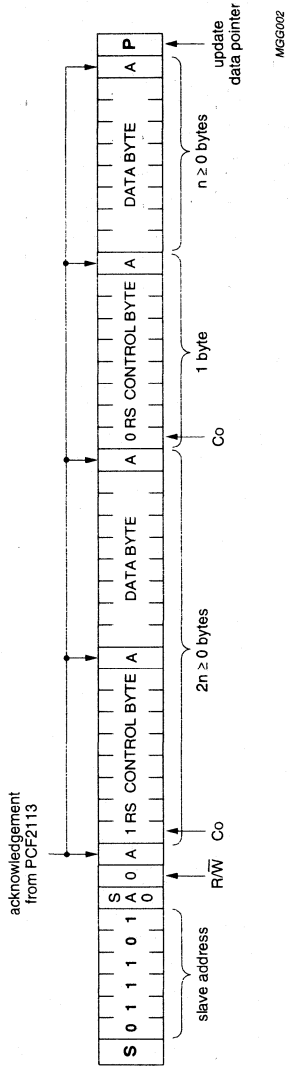
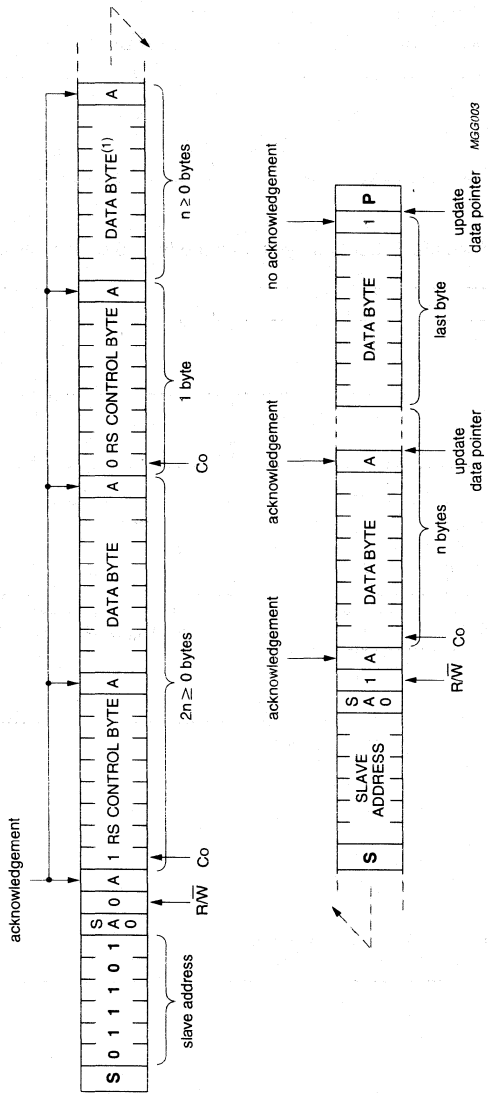


Fig.22 Master transmits to slave receiver; write mode.



(1) Last data byte is a dummy byte (may be omitted).

Fig.23 Master reads after setting word address; write word address, set RS; 'read data'.

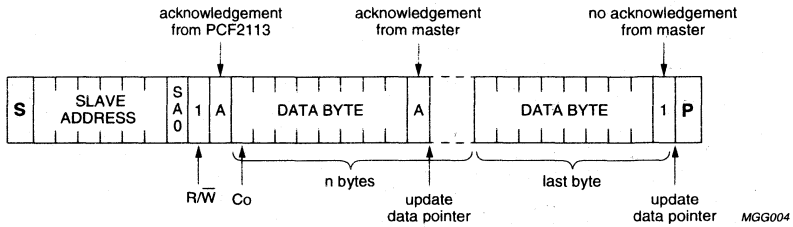


Fig.24 Master reads slave immediately after first byte; read mode (RS previously defined).

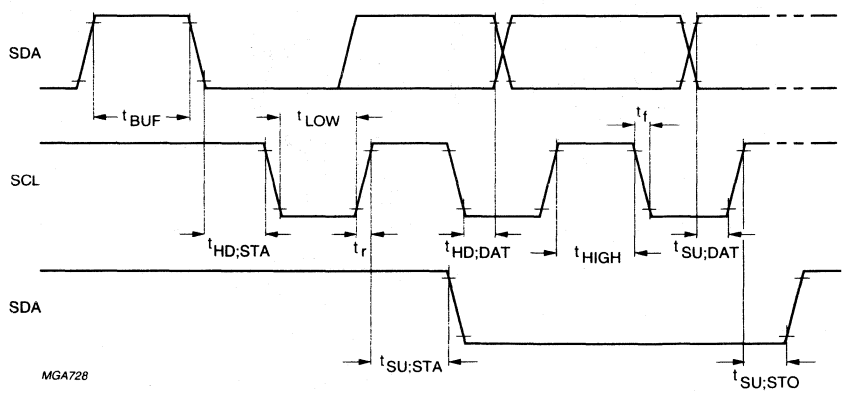


Fig.25 I²C-bus timing diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_{LCD}	LCD supply voltage	−0.5	+7.5	V
V_I	input voltage OSC, RS, R/$\overline{W}$, E and DB7 to DB0	−0.5	V_{DD} + 0.5	V
V_O	output voltage R1 to R18, C1 to C60 and V_{LCD}	−0.5	V_{LCD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

V_{DD} = 1.8 to 4.0 V (external V_{LCD}: V_{DD} = 1.8 to 5.5 V); V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage	internal V_{LCD} generation	1.8	–	4.0	V
V_{DD}	supply voltage	external V_{LCD}	1.8	–	5.5	V
V_{LCD}	LCD supply voltage		2.2	–	6.5	V
I_{SS}	supply current, external V_{LCD}	note 1				
I_{SS1}	supply current 1		–	60	120	µA
I_{SS3}	supply current 3	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	45	80	µA
I_{SS4}	supply current 4 (icon mode)	V_{DD} = 3 V; V_{LCD} = 2.5 V; note 2	–	25	45	µA
I_{SS5}	supply current 5 (power-down mode)	V_{DD} = 3 V; V_{LCD} = 2.5 V; DB7 to DB0, RS, R/$\overline{W}$ = 1; OSC = 0; PD = 1	–	0.5	5	µA
I_{SS}	supply current, internal V_{LCD}	notes 1, 3				
I_{SS6}	supply current 6		–	200	400	µA
I_{SS8}	supply current 8	V_{DD} = 3 V; V_{LCD} = 5 V; note 2	–	200	400	µA
I_{SS9}	supply current 9 (icon mode)	V_{DD} = 3 V; V_{LCD} = 2.5 V; note 2	–	100	–	µA
V_{POR}	power-on reset voltage level	note 4	–	1.3	1.6	V
Logic						
V_{IL1}	LOW level input voltage T1, E, RS, R/$\overline{W}$, DB[7..0] and SA0		0	–	0.3V_{DD}	V
V_{IH1}	HIGH level input voltage T1, E, RS, R/$\overline{W}$, DB[7..0] and SA0		0.7V_{DD}	–	V_{DD}	V
$V_{IL1\ PD}$	LOW level input voltage PD		0	–	0.2V_{DD}	V
$V_{IH1\ PD}$	HIGH level input voltage PD		0.8V_{DD}	–	V_{DD}	V
V_{oscL}	LOW level input voltage OSC		0	–	V_{DD} − 1.5	V
V_{oscH}	HIGH input voltage OSC		V_{DD} − 0.1	–	V_{DD}	V
I_{OL1}	LOW level output current DB[7..0]	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	4	–	mA
$-I_{OH}$	HIGH level output current DB[7..0]	V_{OH} = 4 V; V_{DD} = 5 V	1	8	–	mA
I_{pu}	pull-up current DB[7..0]	V_I = V_{SS}	0.04	0.15	1	µA
I_{L1}	leakage current OSC, E, RS, R/$\overline{W}$, DB[7..0] and SA0	V_I = V_{DD} or V_{SS}	−1	–	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus						
SDA AND SCL						
V_{IL2}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH2}	HIGH level input voltage		$0.7V_{DD}$	–	5.5	V
I_{L2}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
C_i	input capacitance	note 8	–	–	10	pF
I_{OL2}	LOW level output current (SDA)	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
R_{ROW}	row output resistance R1 to R18	note 6	–	10	30	kΩ
R_{COL}	column output resistance C1 to C60	note 6	–	15	40	kΩ
V_{tol1}	bias tolerance R1 to R18 and C1 to C60	note 7	–	20	130	mV
V_{tol2}	V_{LCD} tolerance	T_{amb} = 25 °C; note 3	–	40	150 (tbf)	mV
$T_{Coeff}0$	V_{LCD} temperature coefficient 0	note 5	–	−7.6	–	mV/K
$T_{Coeff}1$	V_{LCD} temperature coefficient 1	note 5	–	−8.4	–	mV/K
$T_{Coeff}2$	V_{LCD} temperature coefficient 2	note 5	–	−10.4	–	mV/K
$T_{Coeff}3$	V_{LCD} temperature coefficient 3	note 5	–	−12.4	–	mV/K

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.
2. T_{amb} = 25 °C; f_{OSC} = 200 kHz.
3. LCD outputs are open-circuit; HV generator is on; load current I_{VLCD} (at V_{LCD}) = 5 μA.
4. Resets all logic when $V_{DD} < V_{POR}$; 3 OSC clock cycles required.
5. Temperature coefficient at V_{OP} = 5.0 V. Typical range ±2 mV/K.
6. Resistance of output terminals (R1 to R18 and C1 to C60) with a load current of 20 μA; outputs measured one at a time; external V_{LCD}.
7. LCD outputs open-circuit; external V_{LCD}.
8. Tested on sample basis.

AC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.2 – 6.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock)	V_{DD} = 5.0 V	45	81	147	Hz
f_{OSC}	oscillator frequency (not available at any pin)		140	250	450	kHz
f_{OSC}	external clock frequency		tbf	–	450	kHz
t_{OSCST}	oscillator start-up time after power-down		–	200	300	µs
Bus timing characteristics: parallel interface; note 1						
WRITE OPERATION (WRITING DATA FROM MPU TO PCF2113)						
T_{cy}	enable cycle time		500	–	–	ns
PW_{EH}	enable pulse width		220	–	–	ns
t_{ASU}	address set-up time		50	–	–	ns
t_{AHD}	address hold time		25	–	–	ns
t_{DSW}	data set-up time		60	–	–	ns
t_{HD}	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2113 TO MPU)						
t_{CYCLE}	enable cycle time		500	–	–	ns
P_{WEH}	enable pulse width		220	–	–	ns
t_{ASU}	address set-up time		50	–	–	ns
t_{AH}	address hold time		25	–	–	ns
t_{DHD}	data delay time		–	–	150	ns
t_{HD}	data hold time		20	–	100	ns
Timing characteristics: I^2C-bus interface; note 1						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	µs
t_{HIGH}	SCL clock high period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SCL, SDA rise time		–	–	300	ns
t_f	SCL, SDA fall time		–	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Note

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

TIMING CHARACTERISTICS

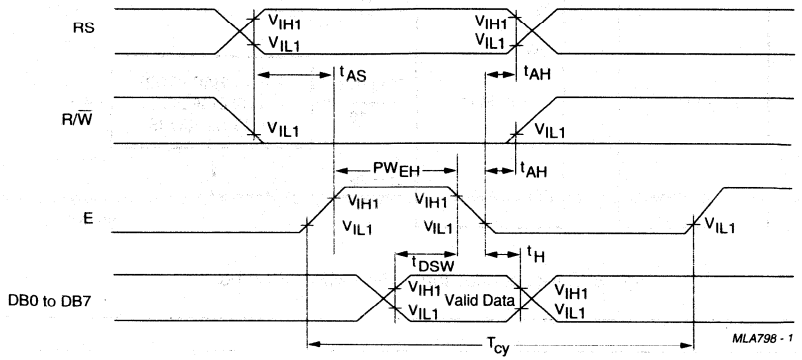


Fig.26 Parallel bus write operation sequence; writing data from MPU to PCF2113.

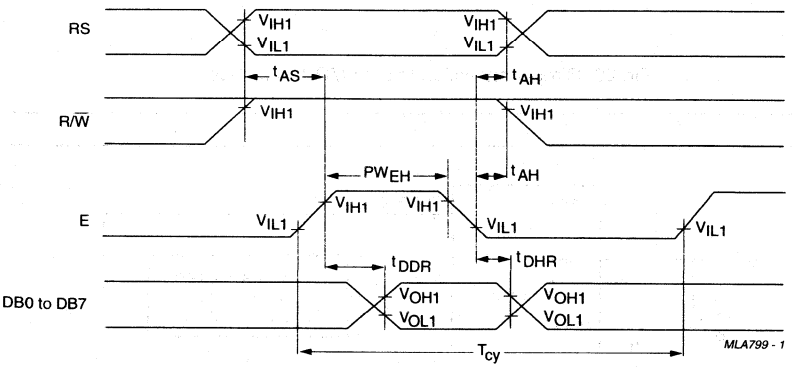


Fig.27 Parallel bus read operation sequence; reading data from PCF2113 to MPU.

APPLICATION INFORMATION

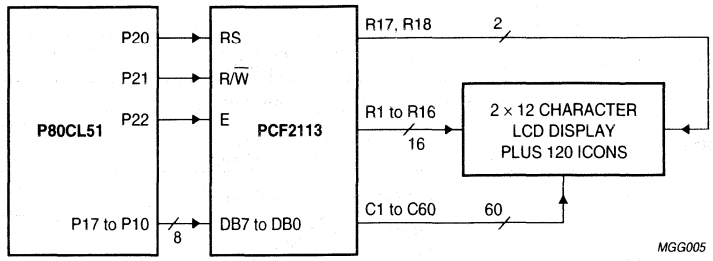


Fig.28 Direct connection to 8-bit MPU; 8-bit bus.

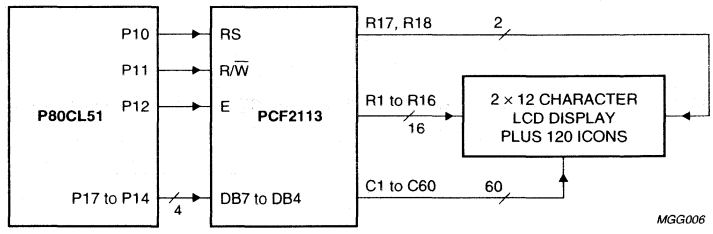


Fig.29 Direct connection to 8-bit MPU; 4-bit bus.

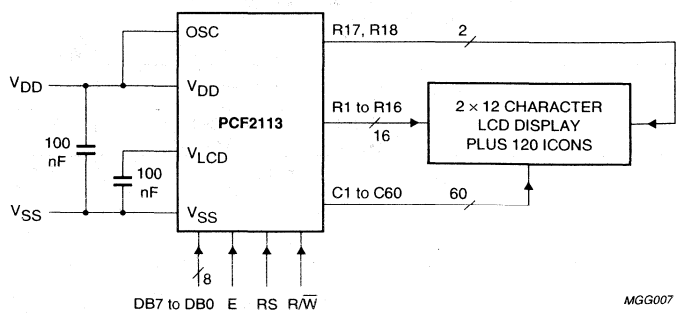


Fig.30 Typical application using parallel interface.

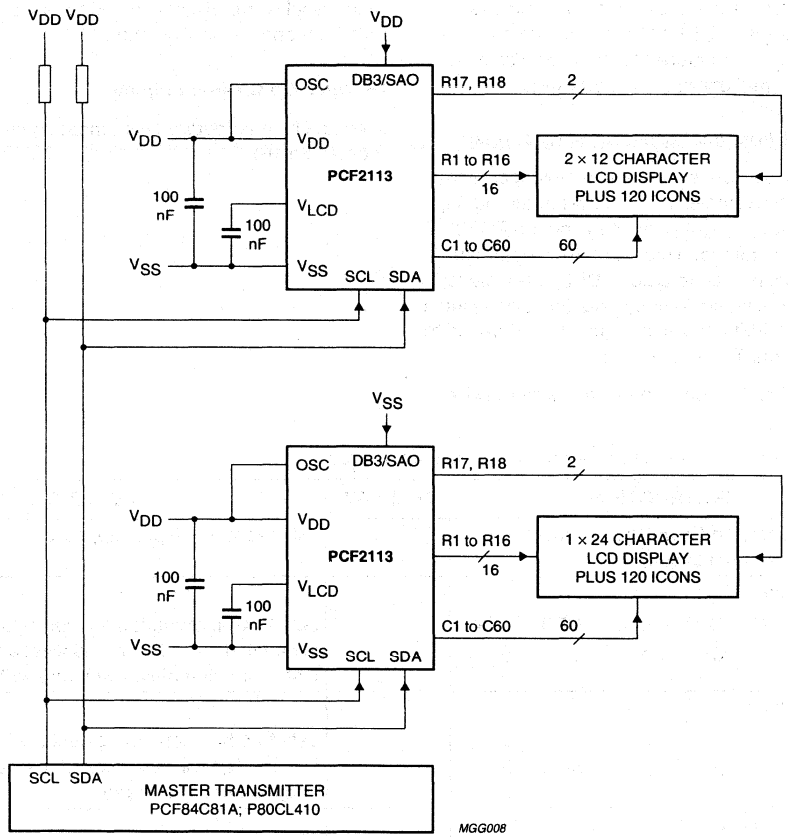


Fig.31 Application using I²C-bus interface.

8-bit operation, 1-line display using internal reset

Table 13 shows an example of a 1-line display in 8-bit operation. The PCF2113 functions must be set by the 'function set' instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and DDRAM contents remain unchanged, display data entered first can be displayed when the 'return home' operation is performed.

4-bit operation, 1-line display using internal reset

The program must set functions prior to 4-bit operation. Table 12 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2113 attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 12 step 3).

Thus, DB4 to DB7 of the 'function set' are written twice.

8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the eighth character is completed (see Table 5). Note that both lines of the display are always shifted together; data does not shift from one line to the other.

I^{2}C operation, 1-line display

A control byte is required with most commands (see Table 16).

Table 12 4-bit operation, 1-line display example; using internal reset

STEP	INSTRUCTION						DISPLAY	OPERATION
1	power supply on (PCF2113 is initialized by the internal reset circuit)							initialized; no display appears
2	function set							
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		sets to 4-bit operation; in this instance operation is handled as 8-bits by initialization and only this instruction completes with one write
	0	0	0	0	1	0		
3	function set							
	0	0	0	0	1	0		sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$; 4-bit operation starts from this point and resetting is needed
	0	0	0	0	0	0		
4	display on/off control							
	0	0	0	0	0	0	_	turns on display and cursor; entire display is blank after initialization
	0	0	1	1	1	0		
5	entry mode set							
	0	0	0	0	0	0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM; display is not shifted
	0	0	0	1	1	0		
6	'write data' to CGRAM/DDRAM							
	1	0	0	1	0	1	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	0	0	0		

Table 13 8-bit operation, 1-line display example; using internal reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2113 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes 'H'
7 to 11			
12	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	writes 'S'
13	entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS**_	sets mode for display shift at the time of write
14	'write data' to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**HILIPS** _	writes space
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ILIPS M**_	writes 'M'
16			

STEP	INSTRUCTION	DISPLAY	OPERATION
17	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**MICROKO_**	writes 'O'
18	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
19	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
20	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 0 0 1 1	**ICROCO**	writes 'C' correction; the display moves to the left
21	cursor/display shift 0 0 0 0 0 1 1 1 0 0	**MICROCO**	shifts the display and cursor to the right
22	cursor/display shift 0 0 0 0 0 1 0 1 0 0	**MICROCO_**	shifts only the cursor to the right
23	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ICROCOM_**	writes 'M'
24			
25	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS M**	returns both display and cursor to the original position (address 0)

Table 14 8-bit operation, 1-line display and icon example; using internal reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2113 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	set CGRAM address 0 0 0 1 0 0 0 0 0 0	_	sets the CGRAM address to position of character 0; the CGRAM is selected
6	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon even phase; icons appears
7			
8	set CGRAM address 0 0 0 1 1 1 0 0 0 0	_	sets the CGRAM address to position of character 4; the CGRAM is selected
9	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon odd phase
10			
11	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 1
12	icon/power control 0 0 0 0 0 0 1 0 1 0	_	icons blink
13	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 0

STEP	INSTRUCTION	DISPLAY	OPERATION
14	set DDRAM address 0 0 1 0 0 0 0 0 0 0		sets the DDRAM address to the first position; DDRAM is selected
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes 'P'; the cursor is incremented by 1 and shifted to the right
16	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes 'H'
17 to 20			
21	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS**	returns both display and cursor to the original position (address 0)

Table 15 8-bit operation, 2-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2113 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 0 0		sets to 8-bit operation; selects 2-line display and voltage generator off
3	display on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6 to 10			
11	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS_**	writes 'S'
12	set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** _	sets DDRAM address to position the cursor at the head of the 2nd line
13	'write data' to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M**_	writes 'M'
14 to 19			

STEP	INSTRUCTION	DISPLAY	OPERATION
20	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	PHILIPS MICROCO_	writes 'O'
21	'write data' to CGRAM/DDRAM 0 0 0 0 0 0 0 1 1 1	PHILIPS MICROCO_	sets mode for display shift at the time of write
22	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	HILIPS ICROCOM_	writes 'M'; display is shifted to the left; the first and second lines shift together
23			
24	return home 0 0 0 0 0 0 0 0 1 0	PHILIPS MICROCOM	returns both display and cursor to the original position (address 0)

Table 16 Example of I²C operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1)

STEP	I²C BYTE	DISPLAY	OPERATION
1	I²C start		initialized; no display appears
2	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		during the acknowledge cycle SDA will be pulled-down by the PCF2113
3	send a control byte for 'function set' Co RS 0 0 0 0 0 0 Ack 0 0 0 0 0 0 0 0 1		control byte sets RS for following data bytes
4	function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		selects 1-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction
5	display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	turns on display and cursor; entire display shows character 20H (blank in ASCII-like character sets)
6	entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
7	I²C start	_	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	send a control byte for 'write data' Co RS 0 0 0 0 0 0 Ack 0 1 0 0 0 0 0 0 1	_	
10	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	 **P**_	writes 'P'; the DDRAM has been selected at power-up; the cursor is incremented by 1 and shifted to the right

STEP	I²C BYTE	DISPLAY	OPERATION
11	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	**PH_**	writes 'H'
12 to 15	| | | |		
16	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS_**	writes 'S'
17	(optional I²C stop) I²C start + slave address for write (as step 8)	**PHILIPS_**	
18	control byte Co RS 0 0 0 0 0 0 Ack 1 0 0 0 0 0 0 0 1	**PHILIPS_**	
19	return home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	sets DDRAM address 0 in address counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the Data Register (DR)
20	I²C start	**PHILIPS**	
21	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	during the acknowledge cycle the content of the DR is loaded into the internal I²C interface to be shifted out; in the previous instruction neither a 'set address' nor a 'read data' has been performed; therefore the content of the DR was unknown. The R/W has to be set to 1 while still in I²C-write mode.
22	control byte for read Co RS 0 0 0 0 0 0 Ack 0 1 1 0 0 0 0 0 1	**PHILIPS**	DDRAM content will be read from following instructions

STEP	I²C BYTE	DISPLAY	OPERATION
23	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	PHILIPS	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C interface
24	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	PHILIPS	8 × SCL; code of letter 'H' is read first; during master acknowledge code of 'I' is loaded into the I²C interface
25	'read data': 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	PHILIPS	no master acknowledge; after the content of the I²C interface register is shifted out no internal action is performed; no new data is loaded to the interface register, Data Register (DR) is not updated, Address Counter (AC) is not incremented and cursor is not shifted
26	I²C stop	PHILIPS	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the read acknowledge.

Table 17 Initialization by instruction, 8-bit interface (note 1)

STEP										DESCRIPTION
power-on or unknown state										
					|				
wait 2 ms after V_{DD} rises above V_{POR}										
					|				
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					|				
wait 2 ms										
					|				
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					|				
wait more than 40 µs										
					|				
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					|				BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
					|				
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	function set (interface is 8 bits long); specify the number of display lines.
0	0	0	0	1	1	0	M	0	H	
0	0	0	0	0	0	1	0	0	0	display off
0	0	0	0	0	0	0	0	0	1	clear display
0	0	0	0	0	0	0	1	I/D	S	entry mode set
					|				
Initialization ends										

Note

1. X = don't care.

Table 18 Initialization by instruction, 4-bit interface. Not applicable for I²C-bus operation

STEP						DESCRIPTION
Power-on or unknown state						
Wait 2 ms after V_{DD} rises above V_{POR}						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
Wait 2 ms						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
Wait 40 μs						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
						BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (set interface to 4 bits long)
0	0	0	0	1	0	interface is 8 bits long
0	0	0	0	1	0	function set (interface is 4 bits long)
0	0	0	M	0	H	specify number of display lines.
0	0	0	0	0	0	
0	0	1	0	0	0	display off
0	0	0	0	0	0	clear display
0	0	0	0	0	1	
0	0	0	0	0	0	entry mode set
0	0	0	1	I/D	S	
Initialization ends						

BONDING PAD LOCATIONS

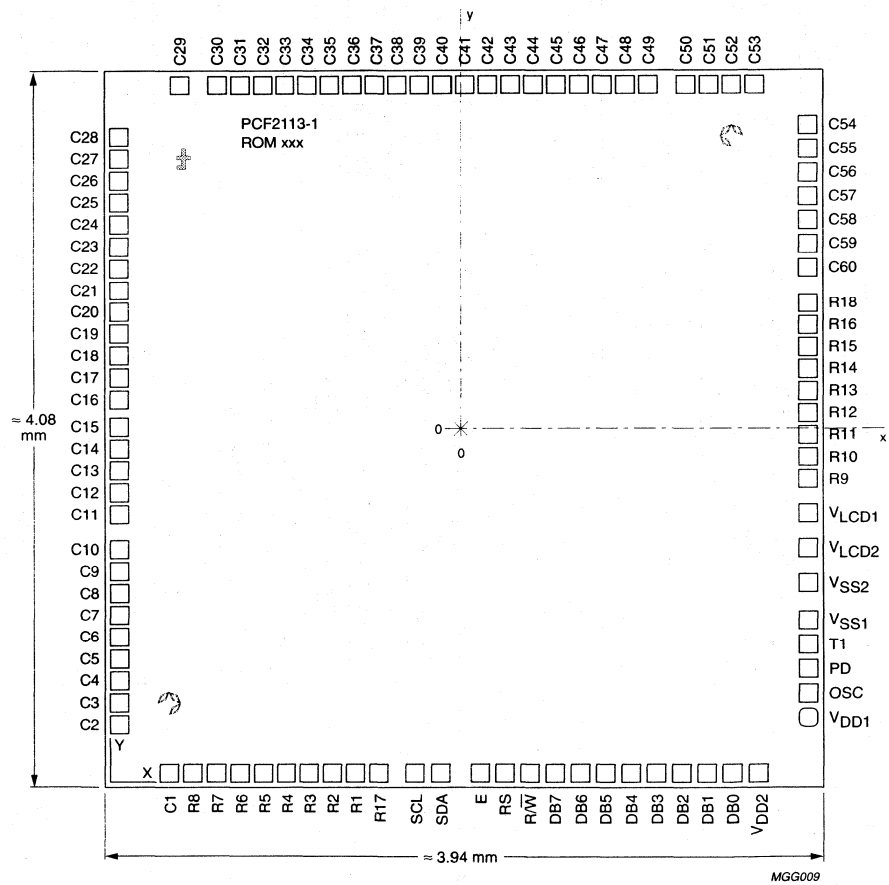


Fig.32 Bonding pad locations.

Table 19 Bonding pad locations (dimensions in μm). All x/y coordinates are referenced to centre of chip (see Fig.32)

SYMBOL	PAD	X	Y
V_{DD1}	1	1811.3	−1547.1
OSC	2	1811.3	−1416.5
PD	3	1811.3	−1285.9
T1	4	1811.3	−1155.3
V_{SS1}	5	1811.3	−1024.7
V_{SS2}	6	1811.3	−822.1
V_{LCD2}	7	1811.3	−633.9
V_{LCD1}	8	1811.3	−446.3
R9	9	1811.3	−264.0
R10	10	1811.3	−144.0
R11	11	1811.3	−24.0
R12	12	1811.3	96.0
R13	13	1811.3	216.0
R14	14	1811.3	336.0
R15	15	1811.3	456.0
R16	16	1811.3	576.0
R18	17	1811.3	696.0
C60	18	1811.3	889.4
C59	19	1811.3	1009.4
C58	20	1811.3	1129.4
C57	21	1811.3	1249.4
C56	22	1811.3	1369.4
C55	23	1811.3	1489.4
C54	24	1811.3	1609.4
C53	25	1536.5	1877.7
C52	26	1416.5	1877.7
C51	27	1296.5	1877.7
C50	28	1176.5	1877.7
C49	29	983.9	1877.7
C48	30	863.9	1877.7
C47	31	743.9	1877.7
C46	32	623.9	1877.7
C45	33	503.9	1877.7
C44	34	383.9	1877.7
C43	35	263.9	1877.7
C42	36	143.9	1877.7
C41	37	23.9	1877.7
C40	38	−96.1	1877.7L

SYMBOL	PAD	X	Y
C39	39	−216.1	1877.7
C38	40	−336.1	1877.7
C37	41	−456.1	1877.7
C36	42	−576.1	1877.7
C35	43	−696.1	1877.7
C34	44	−816.1	1877.7
C33	45	−936.1	1877.7
C32	46	−1056.1	1877.7
C31	47	−1176.1	1877.7
C30	48	−1296.1	1877.7
C29	49	−1488.7	1877.7
C28	50	−1811.3	1609.4
C27	51	−1811.3	1489.4
C26	52	−1811.3	1369.4
C25	53	−1811.3	1249.4
C24	54	−1811.3	1129.4
C23	55	−1811.3	1009.4
C22	56	−1811.3	889.4
C21	57	−1811.3	769.4
C20	58	−1811.3	649.4
C19	59	−1811.3	529.4
C18	60	−1811.3	409.4
C17	61	−1811.3	289.4
C16	62	−1811.3	169.4
C15	63	−1811.3	23.2
C14	64	−1811.3	−96.8
C13	65	−1811.3	−216.8
C12	66	−1811.3	−336.8
C11	67	−1811.3	−456.8
C10	68	−1811.3	−649.4
C9	69	−1811.3	−769.4
C8	70	−1811.3	−889.4
C7	71	−1811.3	−1009.4
C6	72	−1811.3	−1129.4
C5	73	−1811.3	−1249.4
C4	74	−1811.3	−1369.4
C3	75	−1811.3	−1489.4
C2	76	−1811.3	−1609.4

SYMBOL	PAD	X	Y
C1	77	−1542.7	−1877.7
R8	78	−1422.4	−1877.7
R7	79	−1302.4	−1877.7
R6	80	−1182.4	−1877.7
R5	81	−1062.4	−1877.7
R4	82	−942.4	−1877.7
R3	83	−822.4	−1877.7
R2	84	−702.4	−1877.7
R1	85	−582.4	−1877.7
R17	86	−462.4	−1877.7
SCL	87	−271.2	−1877.7
SDA	88	−130.2	−1877.7
E	89	74.4	−1877.7
RS	90	205.1	−1877.7
RW	91	335.7	−1877.7
DB7	92	468.8	−1877.7
DB6	93	603.8	−1877.7
DB5	94	738.8	−1877.7
DB4	95	873.8	−1877.7
DB3	96	1008.8	−1877.7
DB2	97	1143.8	−1877.7
DB1	98	1278.8	−1877.7
DB0	99	1413.8	−1877.7
V_{DD2}	100	1546.0	−1877.7
Sign C1		−1518.0	−1387.7
Sign C2		1405.0	1671.3
Sign f		−1491.0	1602.3

LCD controller/drivers

PCF2116 family (PCF2114X; PCF2116X)

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF2116 family of LCD controller/drivers consists of 2 similar members: PCF2116X and PCF2114X, later referred to as PCF2116. The specific differences are expressed in separate paragraphs for PCF2116X and PCF2114X respectively.

The letter X in PCF2116X or PCF2114X specifies the character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, G and J. Set 'A' in PCF2116A characterises the built-in standard character set. Other character sets are available on request.

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana characters. The PCF2116 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus.

The PCF2116K differs from the existing PCF2116 family only in the V_{LCD}/V_{OP} generation section.

Packages

- PCF2116XU/10; chip on FFC
- PCF2114XU/10; chip on FFC
- PCF2116XU/12; chip with bumps on FFC
- PCF2114XU/12; chip with bumps on FFC
- PCF2116K; LQFP128 (14 × 20 mm)
- Pin grid array PGA144 (samples only).

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2114XU/2116XU	116	FFC116	–
PCF2116KH/KHZ	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

BLOCK DIAGRAM

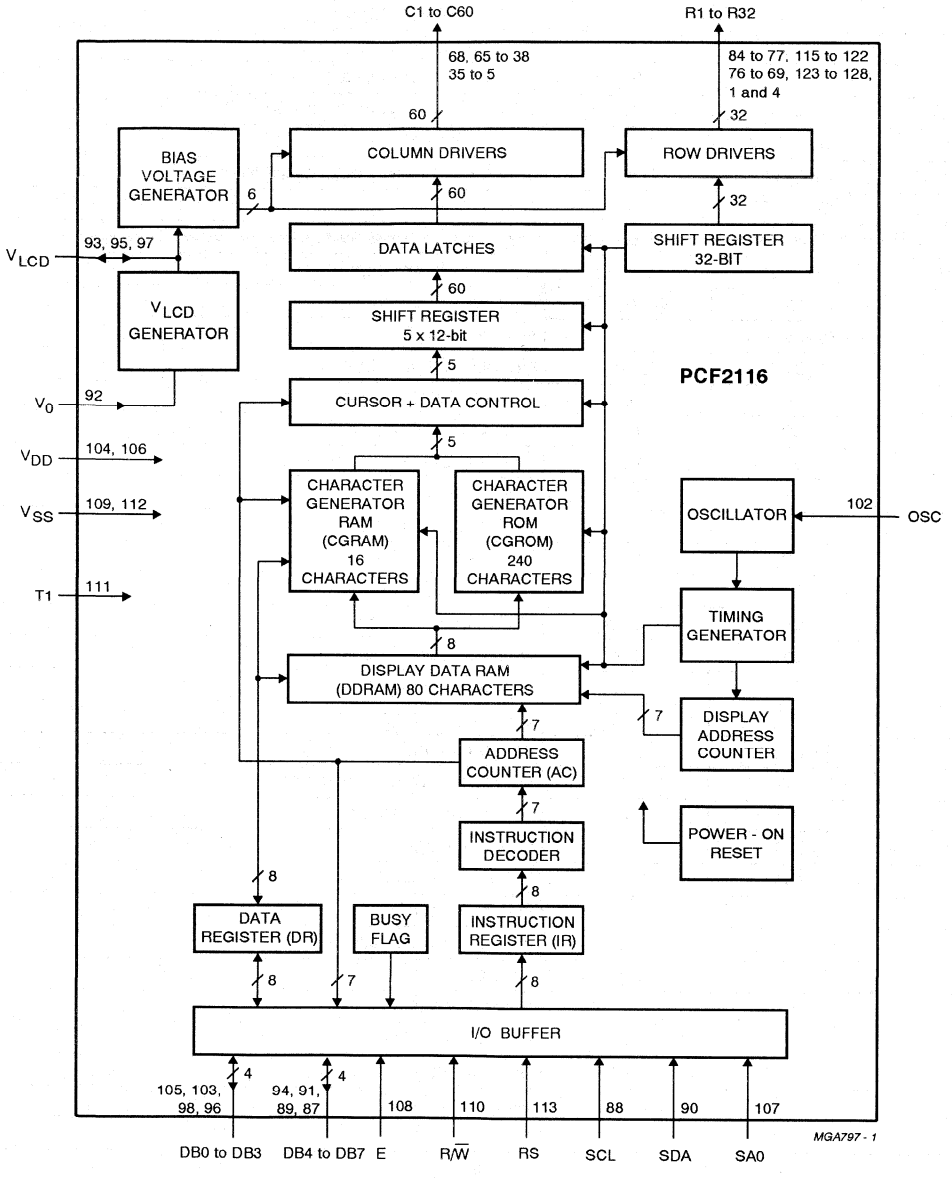


Fig.1 Block diagram.

PINNING

SYMBOL	LQFP128 PIN	FFC PAD	DESCRIPTION
R31	1	27	LCD row driver output
n.c.	2 and 3	–	not connected
R32	4	28	LCD row driver output
C60 to C30	5 to 35	29 to 59	LCD column driver outputs 60 to 30
n.c.	36 and 37	–	not connected
C29 to C2	38 to 65	60 to 87	LCD column driver outputs 29 to 2
n.c.	66 and 67	–	not connected
C1	68	88	LCD column driver output 1
R24 to R17	69 to 76	89 to 96	LCD row driver outputs
R8 to R1	77 to 84	97 to 104	LCD row driver outputs
n.c.	85 and 86	–	not connected
DB7	87	105	bidirectional data bus
SCL	88	106	I^2C-bus serial clock input
DB6	89	107	bidirectional data bus
SDA	90	108	I^2C-bus serial data input/output
DB5	91	109	bidirectional data bus
V_0	92	110	control input for V_{LCD}
V_{LCD1}	93	111	LCD supply voltage
DB4	94	112	bidirectional data bus
V_{LCD2}	95	113	LCD supply voltage
DB3	96	114	bidirectional data bus
V_{LCD3}	97	115	LCD supply voltage
DB2	98	116	bidirectional data bus
n.c.	99 to 101	–	not connected
OSC	102	1	oscillator/external clock input
DB1	103	2	bidirectional data bus
V_{DD2}	104	3	supply voltage
DB0	105	4	bidirectional data bus
V_{DD1}	106	5	supply voltage
SA0	107	6	I^2C-bus address pin
E	108	7	data bus clock
V_{SS1}	109	8	ground (logic)
$R/\overline{W}$	110	9	read/write
T1	111	10	test pad (connect to V_{SS})
V_{SS2}	112	11	ground (logic)
RS	113	12	register select
n.c.	114	–	not connected
R9 to R16	115 to 122	13 to 20	LCD row driver outputs
R25 to R30	123 to 128	21 to 26	LCD row driver outputs

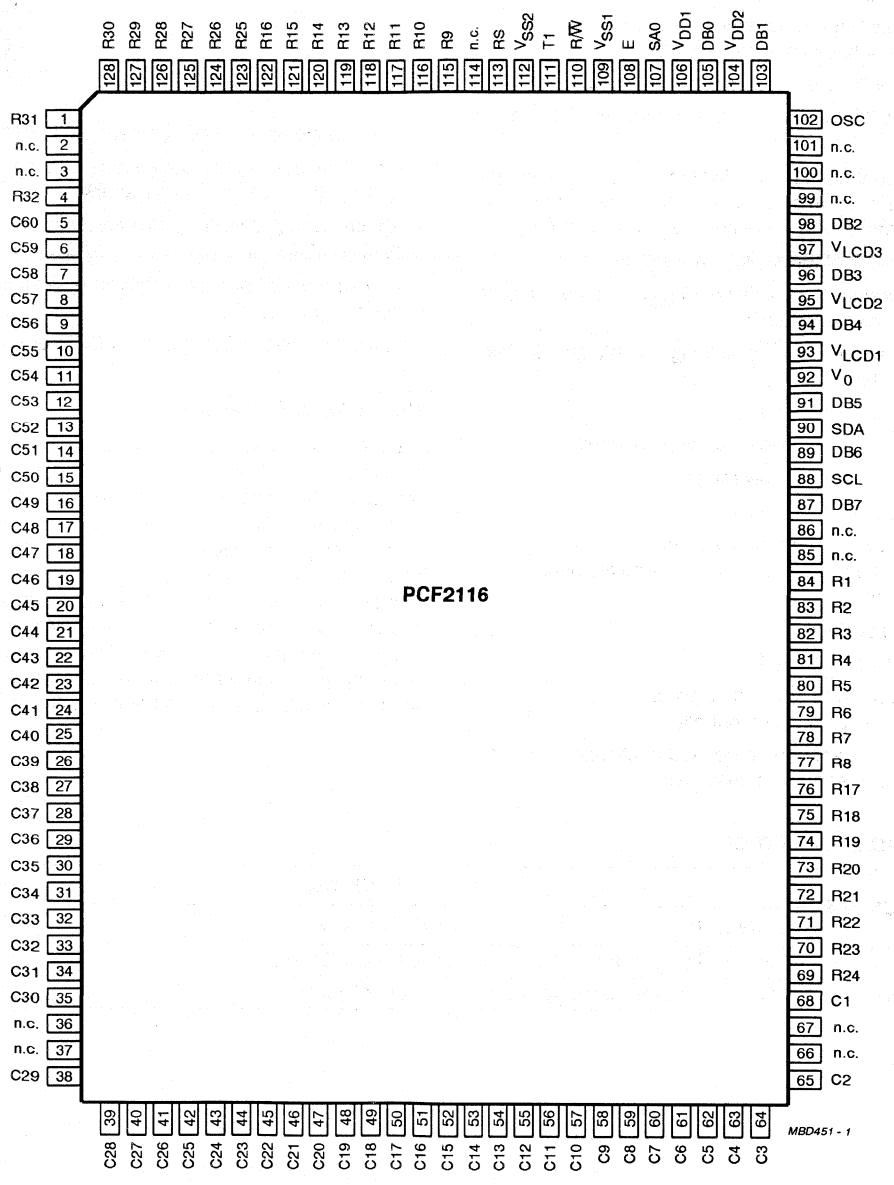


Fig.2 Pin configuration.

Universal LCD driver for low multiplex rates

PCF8566

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2.5 to 6 V power supply range
- Low power consumption
- Power saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40 lead plastic very small outline package (VSO40; SOT158-1)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8566P	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF8566T	VSO40	plastic very small outline package; 40 leads	SOT158-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM

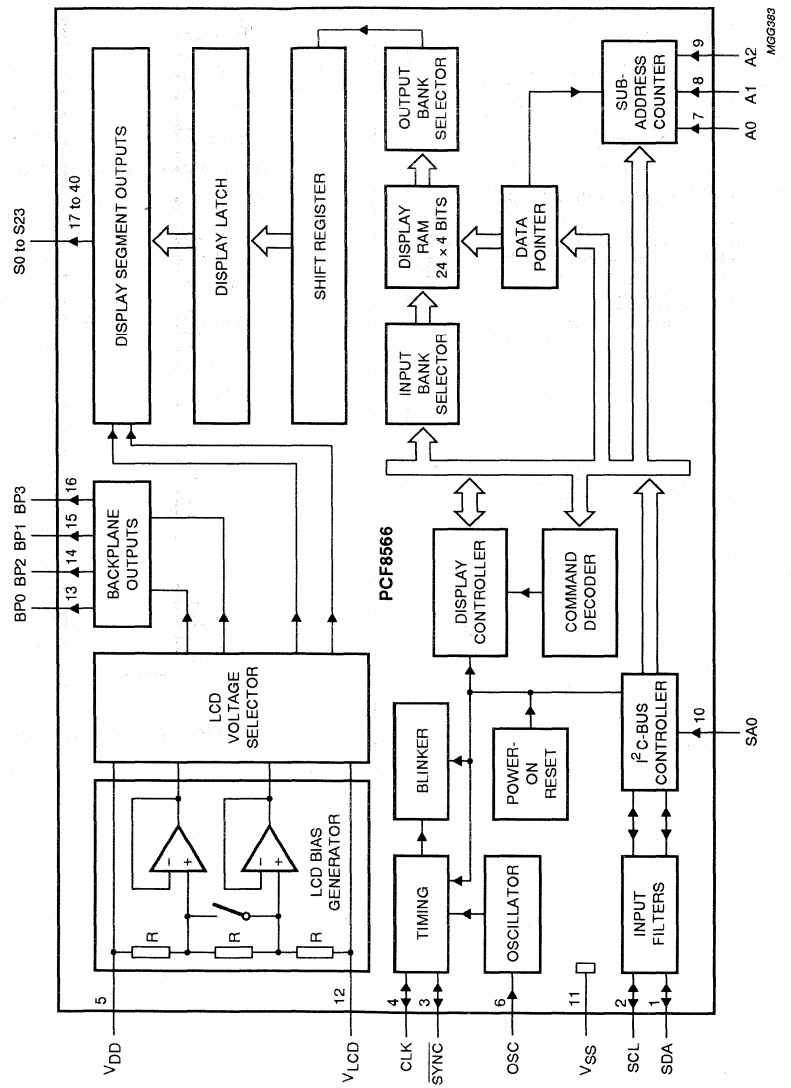


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data input/output
SCL	2	I²C-bus clock input/output
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	positive supply voltage
OSC	6	oscillator input
A0	7	I²C-bus subaddress inputs
A1	8	
A2	9	
SA0	10	I²C-bus slave address bit 0 input
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0	13	LCD backplane outputs
BP2	14	
BP1	15	
BP3	16	
S0 to S23	17 to 40	LCD segment outputs

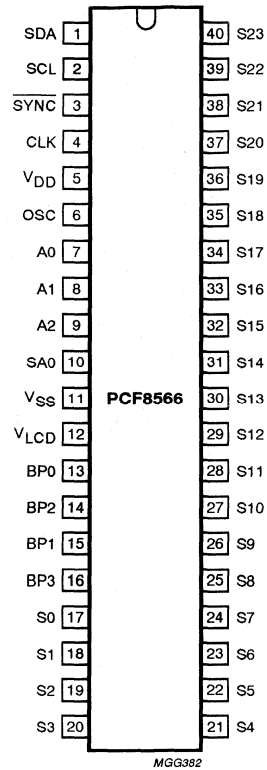


Fig.2 Pin configuration.

Universal LCD driver for low multiplex rates PCF8576C

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 6 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both and multiple PCF8576C applications
- Space-saving 56-lead plastic very small outline package (VSO56) or 64-lead low profile quad flat package (LQFP64)
- No external components
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576C is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576CT	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576CU	–	uncased chip in tray	–
PCF8576CU/10	FFC	chip-on-film frame carrier	–
PCF8576CH	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

BLOCK DIAGRAM

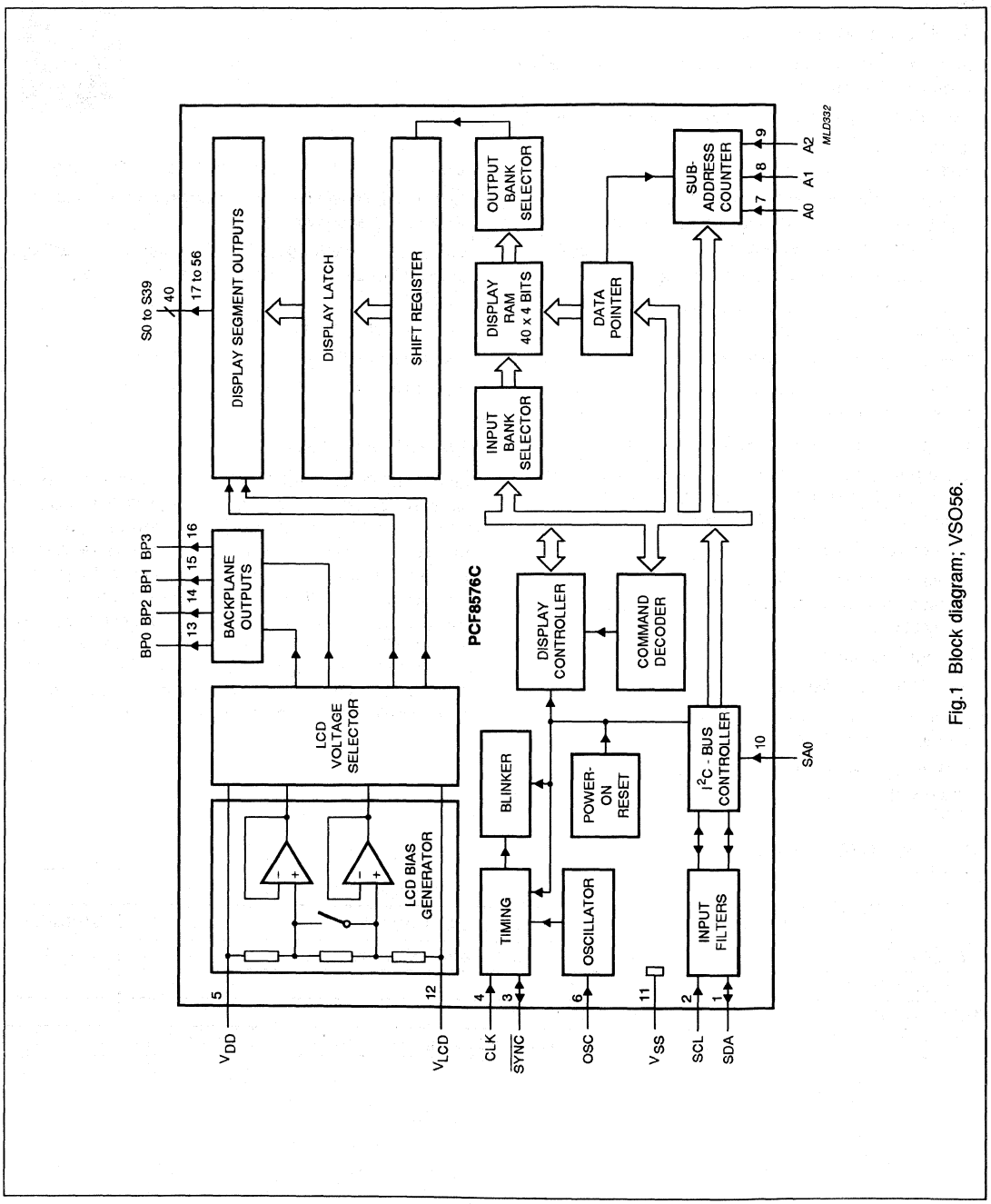


Fig.1 Block diagram; VSO56.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT190	SOT314	
SDA	1	10	I²C-bus serial data input/output
SCL	2	11	I²C-bus serial clock input
$\overline{SYNC}$	3	12	cascade synchronization input/output
CLK	4	13	external clock input
V_{DD}	5	14	supply voltage
OSC	6	15	oscillator input
A0 to A2	7 to 9	16 to 18	I²C-bus subaddress inputs
SA0	10	19	I²C-bus slave address input; bit 0
V_{SS}	11	20	logic ground
V_{LCD}	12	21	LCD supply voltage
BP0, BP2, BP1, BP3	13 to 16	25 to 28	LCD backplane outputs
S0 to S39	17 to 56	29 to 32, 34 to 47, 49 to 64, 2 to 7	LCD segment outputs
n.c.	–	1, 8, 9, 22 to 24, 33 and 48	not connected

LCD row/column driver for dot matrix graphic displays

PCF8578

FEATURES

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack and 64 pin quad flat pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

GENERAL DESCRIPTION

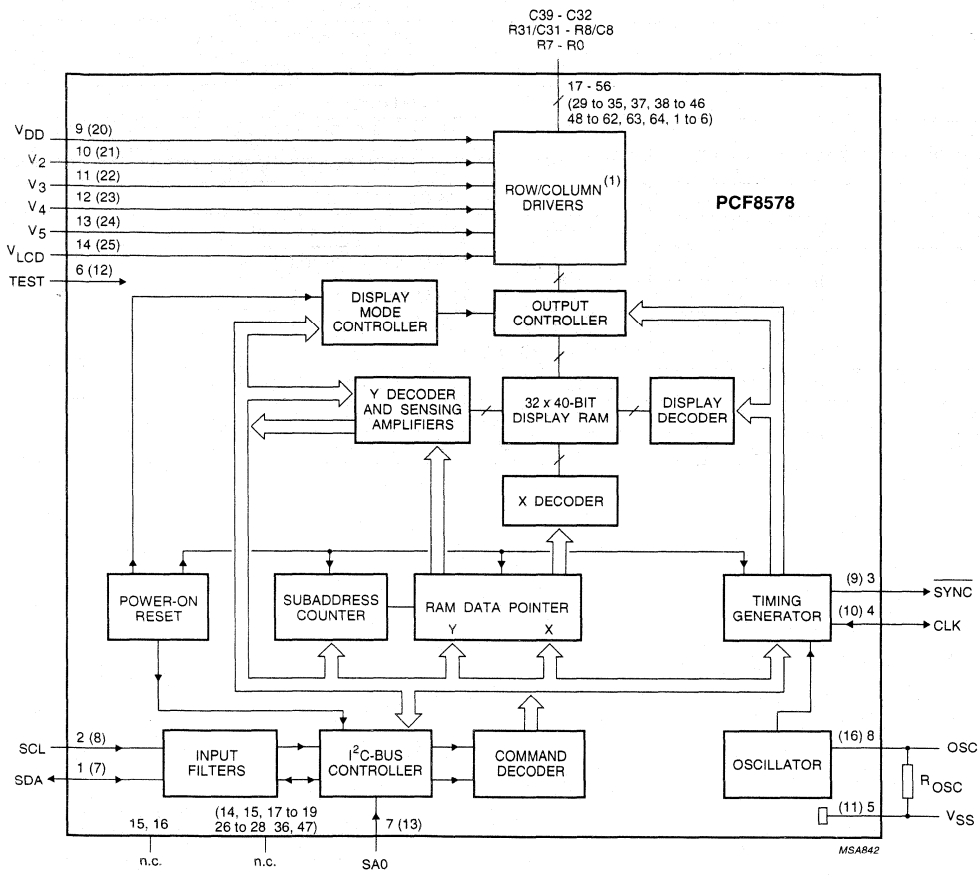
The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8578T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8578U7	–	chip with bumps on tape	–
PCF8578H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM



(1) LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the 64-pin version.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I^2C-bus serial data input/output
SCL	2	8	I^2C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization output
CLK	4	10	external clock input/output
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I^2C-bus slave address input (bit 0)
OSC	8	16	oscillator input
V_{DD}	9	20	positive supply voltage
V_2 to V_5	10 to 13	21 to 24	LCD bias voltage inputs
V_{LCD}	14	25	LCD supply voltage
n.c.	15, 16	14, 15, 17 to 19, 26 to 28, 36, 47	not connected
C39 to C32	17 to 24	29 to 35, 37	LCD column driver outputs
R31/C31 to R8/C8	25 to 48	38 to 46, 48 to 62	LCD row/column driver outputs
R7 to R0	49 to 56	63, 64, 1 to 6	LCD row driver outputs

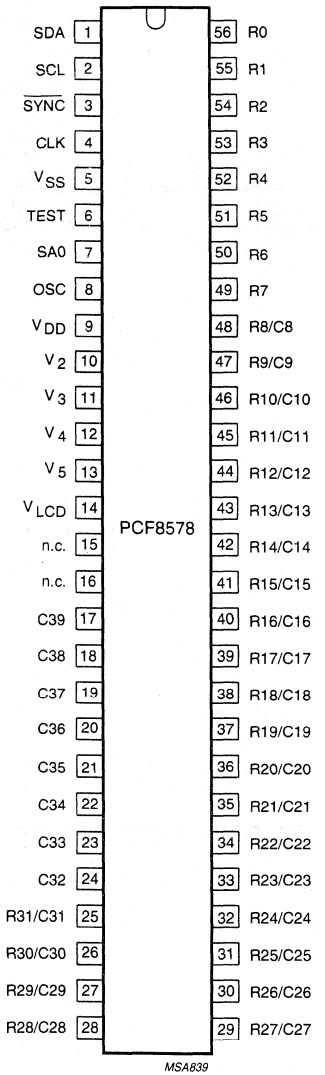


Fig.2 Pin configuration (VSO56).

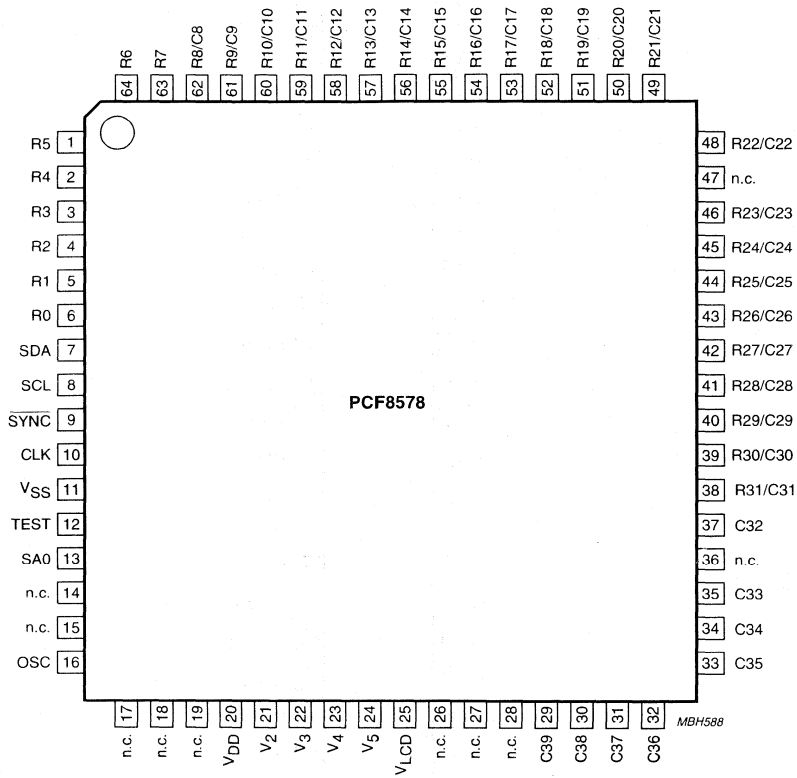


Fig.3 Pin configuration (LQFP64).

LCD column driver for dot matrix graphic displays

PCF8579

FEATURES

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead plastic mini-pack and 64-pin plastic low profile quad flat package
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

GENERAL DESCRIPTION

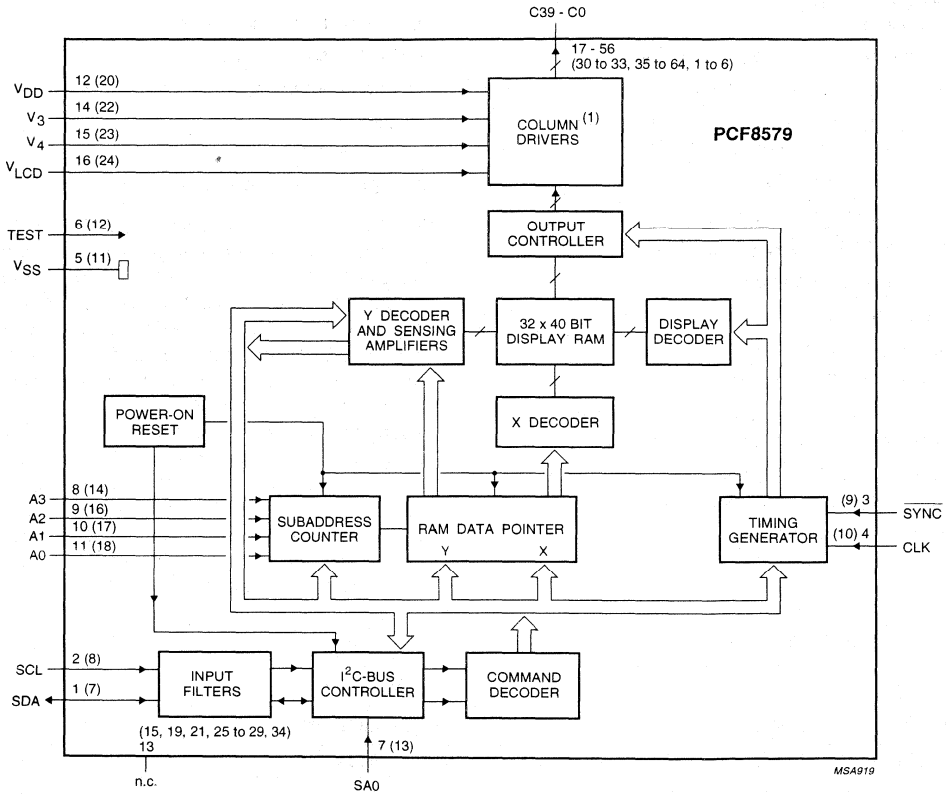
The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 × 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8579T	VSO56	plastic very small outline package; 56 leads	SOT190
PCF8579U7	–	chip with bumps on tape	–
PCF8579H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM



(1) LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the 64-pin version.

Fig.1 Block diagram.

PINNING

SYMBOL	PINS		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I²C-bus serial data input/output
SCL	2	8	I²C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization input
CLK	4	10	external clock input
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I²C-bus slave address input (bit 0)
A3 to A0	8 to 11	14, 16 to 18	I²C-bus subaddress inputs
V_{DD}	12	20	supply voltage
n.c.	13(1)	15, 19, 21,25 to 29, 34	not connected
V_3, V_4	14 and 15	22 and 23	LCD bias voltage inputs
V_{LCD}	16	24	LCD supply voltage
C39 to C0	17 to 56	30 to 33, 35 to 64 and 1 to 6	LCD column driver outputs

Note

1. Do not connect, this pin is reserved.

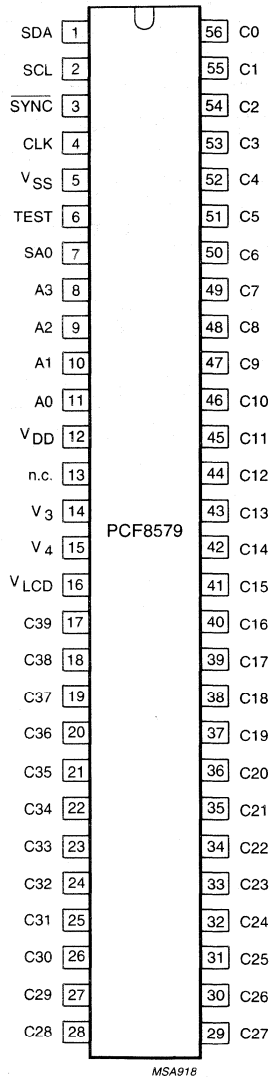


Fig.2 Pin configuration (VSO56).

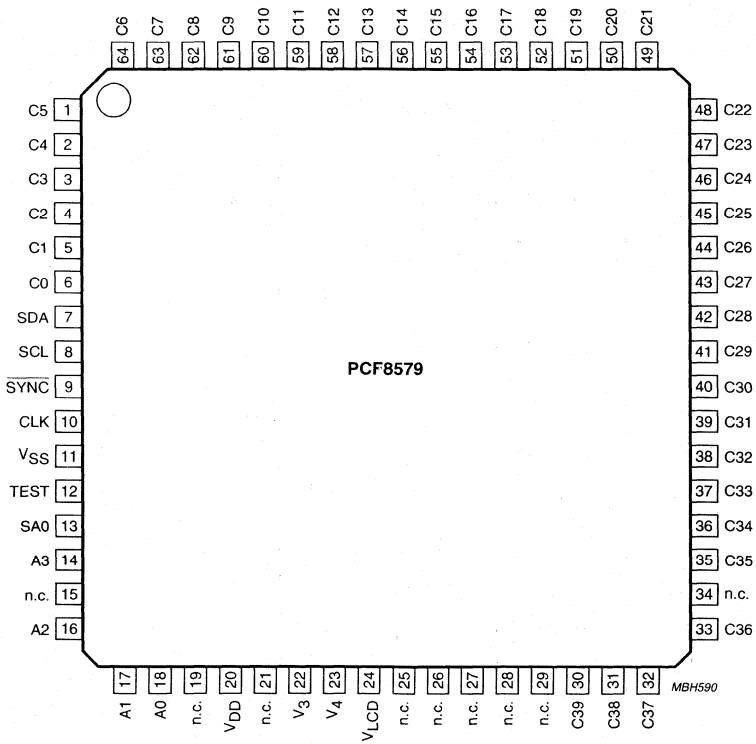


Fig.3 Pin configuration (LQFP64).

Section 12
Microcontrollers

WIRELESS COMMUNICATIONS

CONTENTS

80CL580/83CL580	Low–voltage single–chip 8–bit microcontroller	12–3
P83CL781; P83CL782	Low–voltage 8–bit microcontrollers	12–74
P90CL301BFH (C100)	Low–voltage 16–bit microcontroller	12–111

1 FEATURES

- Full static 80C51 Central Processing Unit
- 8-bit CPU, ROM, RAM, I/O in a 56-lead VSO or 64-lead QFP package
- 6 kbytes ROM Program Memory, expandable externally to 64 kbytes (only P83CL580)
- 256 bytes RAM Data Memory, expandable externally to 64 kbytes
- Five 8-bit ports; 40 I/O lines
- Three 16-bit Timer/Event counters
- External memory expandable up to 128 kbytes, external ROM up to 64 kbytes and/or RAM up to 64 kbytes
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector nested interrupt structure with two priority levels
- Full duplex serial port (UART)
- I^2C-bus interface for serial transfer on two lines
- Analog-to-digital converter (ADC) with Power-down mode; 4 input channels and 8-bit ADC
- Pulse Width Modulated (PWM) output (8-bit resolution)
- Watchdog Timer
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four 8-byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- Modes of reduced activity: Power-down and Idle modes
- Wake-up via external interrupts at Port 1
- Frequency range: 0 to 12 MHz. For ADC operation minimum 250 kHz at 2.7 V
- Supply voltage: 2.5 to 6.0 V
- Very low current consumption: typically 4.5 mA at 2.5 V and 8 MHz
- Operating temperature range: −40 to +85 °C.

2 GENERAL DESCRIPTION

The P80CL580; P83CL580 (hereafter generally referred to as P8xCL580) is manufactured in an advanced CMOS technology. The instruction set of the P8xCL580 is based on that of the 80C51 and consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. The device operates over a wide range of supply voltages and has low power consumption; there are two software selectable modes for power reduction: Idle and Power-down. For emulation purposes, the P85CL580 (piggy-back version) with 256 bytes of RAM is recommended.

This data sheet details the specific properties of the P80CL580; P83CL580; for details of the 80C51 core see *"Data Handbook IC20"* and for the I^2C-bus refer to *"The I^2C-bus and how to use it"* ordering nr. 9398 393 40011".

2.1 ROMless version: P80CL580

The P80CL580 is the ROMless version of the P83CL580. The mask options on the P80CL580 are fixed as follows:

- All ports have option '1S' (standard port, HIGH after reset), except ports P1.6 and P1.7 which have option '2S' (open-drain, HIGH after reset)
- Oscillator option: Oscillator 3
- Power-on-reset option: off.

3 APPLICATIONS

The P8xCL580 is an 8-bit general purpose microcontroller especially suited for cordless telephone and mobile communication applications. The P8xCL580 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P80CL580HFT	VSO56	plastic very small outline package; 56 leads	SOT190-1
P83CL580HFT			
P80CL580HFH	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm	SOT319-2
P83CL580HFH			

5 BLOCK DIAGRAM

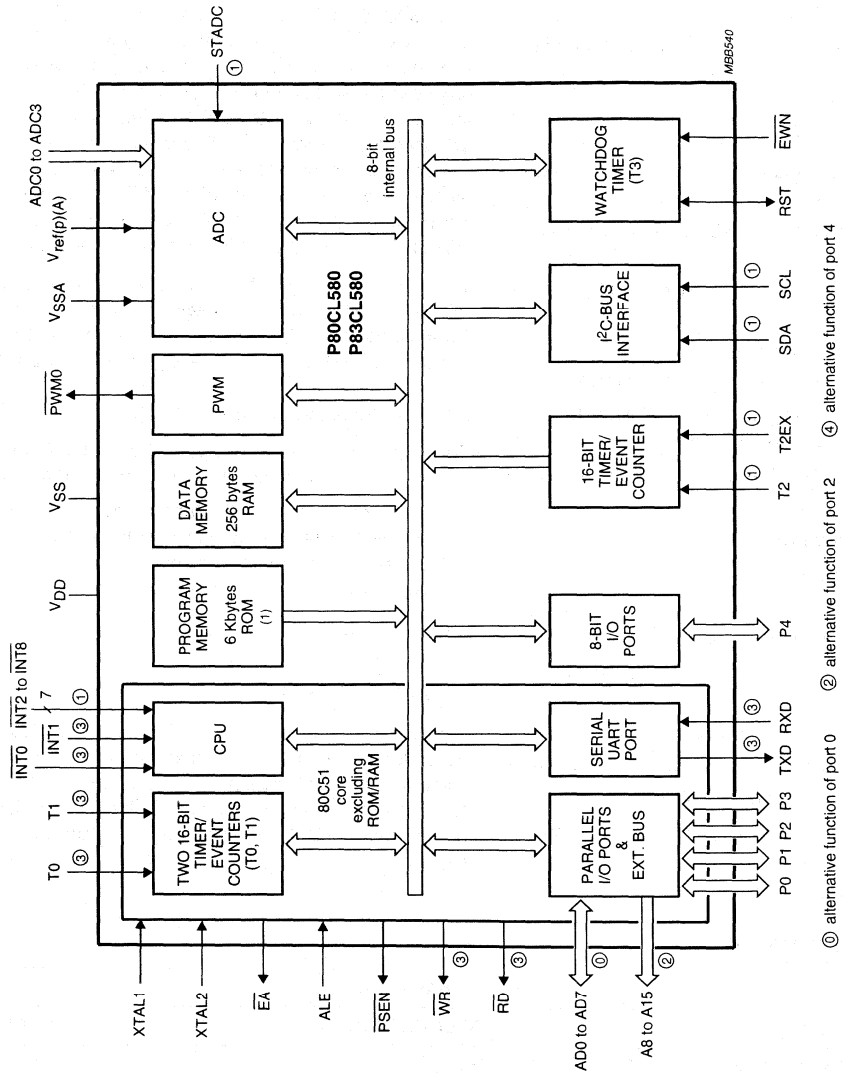


Fig.1 Block diagram.

6 FUNCTIONAL DIAGRAM

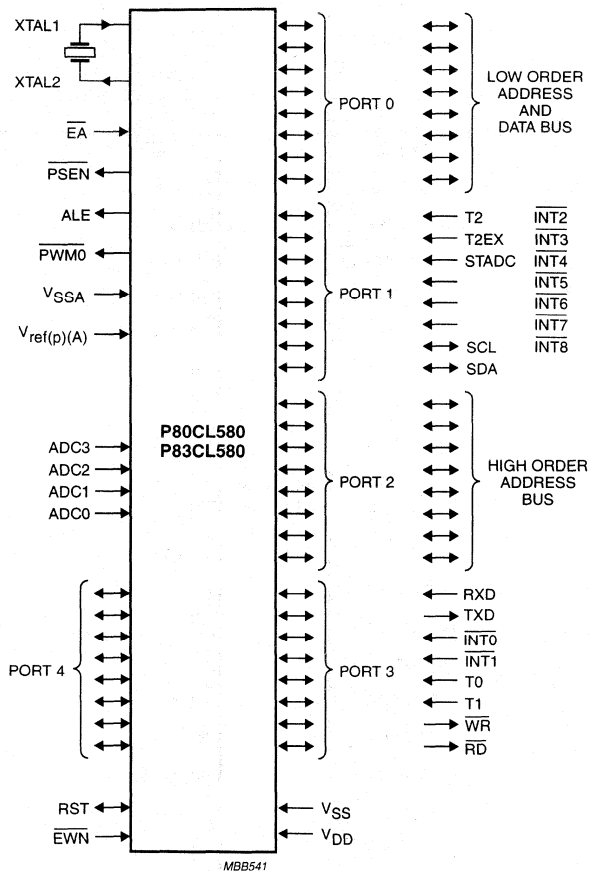


Fig.2 Functional diagram.

7 PINNING INFORMATION

7.1 Pinning

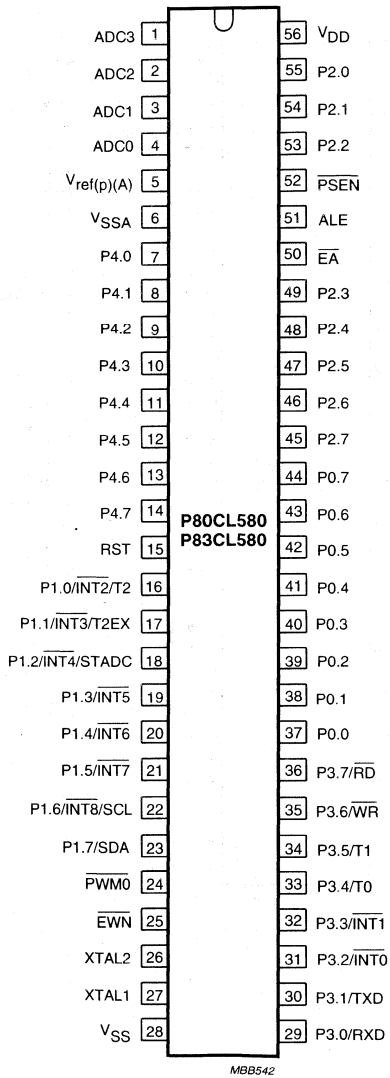


Fig.3 Pin configuration for VSO56 package.

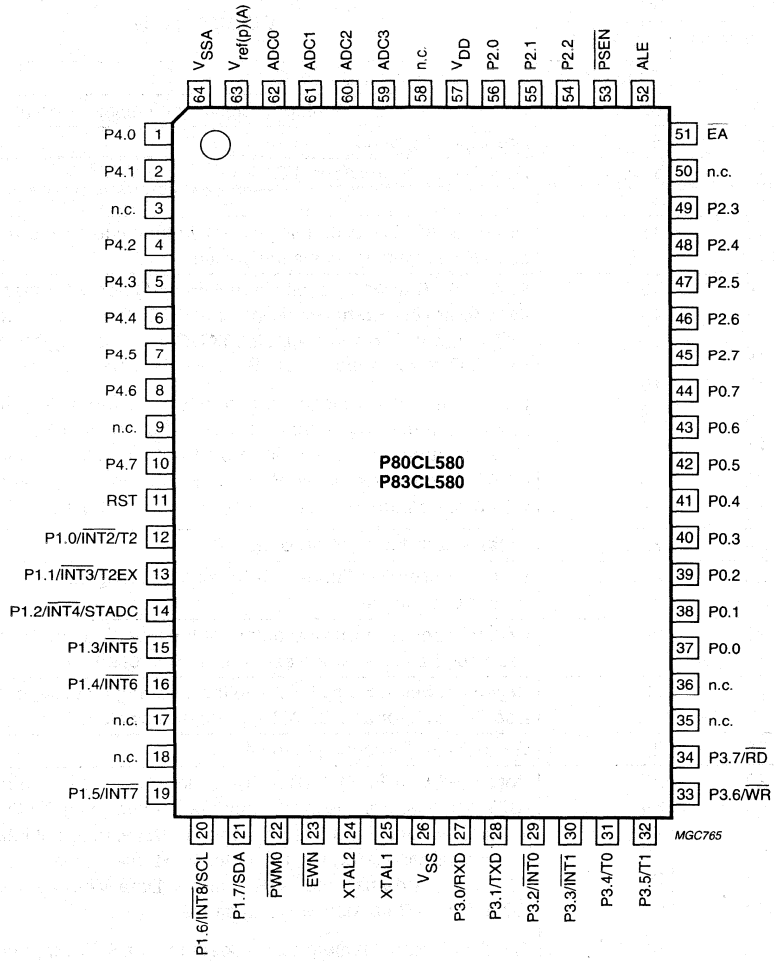


Fig.4 Pin configuration for QFP64 package.

7.2 Pin description

Table 1 Pin description for VSO56 (SOT190-1) and QFP64 (SOT319-2)
For more extensive description of the port pins see Chapter 10 "I/O facilities".

SYMBOL	PIN		DESCRIPTION
	VSO56	QFP64	
ADC3 to ADC0	1 to 4	59 to 62	4 input channels to the ADC.
$V_{ref(p)(A)}$	5	63	Positive potential of analog-to-digital conversion reference resistor.
V_{SSA}	6	64	Analog part ground.
P4.0 to P4.7	7 to 14	1, 2, 4 to 8, 10	**Port 4**: 8-bit bidirectional I/O port.
RST	15	11	**Reset**: a HIGH level on this pin for two machine cycles while the oscillator is running resets the device.
P1.0/$\overline{INT2}$/T2	16	12	**Port 1 (P1.0 to P1.7)**: 8-bit bidirectional I/O port with internal pull-ups; **$\overline{INT2}$ to $\overline{INT8}$**: external interrupt inputs; **T2**: Timer T2 input; **T2EX**: Timer T2 external input; **STADC**: external trigger of the ADC; **SCL**: I^2C-bus interface clock; **SDA**: I^2C-bus interface data. Port 1 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups, and in that state can be used as inputs (note P1.6 and P1.7 are open-drain only). The Port 1 output buffer can sink/source 4 LS TTL loads. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL} see Chapter 23) due to the internal pull-ups.
P1.1/$\overline{INT3}$/T2EX	17	13	
P1.2/$\overline{INT4}$/STADC	18	14	
P1.3/$\overline{INT5}$	19	15	
P1.4/$\overline{INT6}$	20	16	
P1.5/$\overline{INT7}$	21	19	
P1.6/$\overline{INT8}$/SCL	22	20	
P1.7/SDA	23	21	
$\overline{PWM0}$	24	22	**Pulse Width Modulation output 0**.
$\overline{EWN}$	25	23	**Enable Watchdog Timer**: enable for Watchdog Timer and enable Power-down mode.
XTAL2	26	24	**Crystal oscillator output**: output of the inverting amplifier of the oscillator. Left open when external clock is used.
XTAL1	27	25	**Crystal oscillator input**: input to the inverting amplifier of the oscillator, also the input for an externally generated clock source.
V_{SS}	28	26	Ground: circuit ground potential.
P3.0/RXD	29	27	**Port 3 (P3.0 to P3.7)**: 8-bit bidirectional I/O port with internal pull-ups; **RXD**: serial port receiver data input (asynchronous); **TXD**: serial port transmitter data output (asynchronous); **$\overline{INT0}$**: external interrupt 0; **$\overline{INT1}$**: external interrupt 1; **T0**: Timer 0 external input; **T1**: Timer 1 external input; **$\overline{WR}$**: external Data Memory write strobe; **$\overline{RD}$**: external Data Memory read strobe. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL} in the characteristics; see Chapter 23) due to the internal pull-ups.
P3.1/TXD	30	28	
P3.2/$\overline{INT0}$	31	29	
P3.3/$\overline{INT1}$	32	30	
P3.4/T0	33	31	
P3.5/T1	34	32	
P3.6/$\overline{WR}$	35	33	
P3.7/$\overline{RD}$	36	34	

SYMBOL	PIN		DESCRIPTION
	VSO56	QFP64	
P0.0 to P0.7	37 to 44	37 to 44	**Port 0**: 8-bit open-drain bidirectional I/O port. As an open-drain output port it can sink 8 LS TTL loads. Port 0 pins that have logic 1s written to them float, and in that state will function as high impedance inputs. Port 0 is also the multiplexed low order address and data bus during access to external memory. The strong internal pull-ups are used while emitting logic 1s within the low order address.
P2.0 to P2.7	55 to 53, 49 to 45	56 to 54, 49 to 45	**Port 2**: 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups, and in that state can be used as inputs. The Port 2 output buffer can sink/source 4 LS TTL loads. Port 2 emits the high-order address byte during accesses to external memory that use 16-bit addresses (MOVX @DPTR). In this application it uses the strong internal pull-ups when emitting logic 1s. During accesses to external memory that use 8-bit addresses (MOVX @Ri). Port 2 emits the contents of the P2 Special Function Register.
$\overline{EA}$	50	51	**External Access**. When $\overline{EA}$ is held HIGH the CPU executes out of internal Program Memory (unless the program counter exceeds 17FFH). Holding $\overline{EA}$ LOW forces the CPU to execute out of external memory regardless of the value of the Program Counter.
ALE	51	52	**Address Latch Enable**. Output pulse for latching the low byte of the address during access to external memory. ALE is emitted at a constant rate of $1/6 \times f_{osc}$, and may be used for external timing or clocking purposes (assuming MOVX instructions are not used).
$\overline{PSEN}$	52	53	**Program Store Enable**. Output read strobe to external Program Memory. When executing code out of external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle. However, during each access to external Data Memory two $\overline{PSEN}$ activations are skipped.
V_{DD}	56	57	Power supply.
n.c.	–	3, 9, 17, 18, 35, 36, 50 and 58	Not connected.

8 FUNCTIONAL DESCRIPTION

The functional description of the device is described in:

Chapter 9 "Memory organization"

Chapter 10 "I/O facilities"

Chapter 11 "Timer/event counters"

Chapter 12 "Pulse Width Modulated output"

Chapter 13 "Analog-to-digital converter (ADC)"

Chapter 14 "Reduced power modes"

Chapter 15 "I2C-bus serial I/O"

Chapter 16 "Standard serial interface SIO0: UART"

Chapter 17 "Interrupt system"

Chapter 18 "Oscillator circuitry"

Chapter 19 "Reset"

8.1 General

The P8xCL580 is a stand-alone high-performance CMOS microcontroller designed for use in real-time applications such as cordless telephone and mobile communications, instrumentation, industrial control, intelligent computer peripherals and consumer products.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 kbytes of Program Memory and/or up to 64 kbytes of Data Memory.

The P8xCL580 contains a 6 kbytes Program Memory (ROM; P83CL580); a static 256 bytes Data Memory (RAM); 40 I/O lines; three 16-bit timer/event counters; a fifteen-source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit, 4-channel 8-bit A/D converter, Watchdog Timer and Pulse Width Modulation output.

The device has two software selectable modes of reduced activity for power reduction:

- **Idle mode**; freezes the CPU while allowing the derivative functions (timers, serial I/O, ADC, PWM) and interrupt system to continue functioning.
- **Power-down mode**; saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

In addition, two serial interfaces are provided on-chip:

- a standard UART serial interface, and
- a standard I^2C-bus serial interface. The I^2C-bus serial interface has byte oriented master and slave functions allowing communication with the whole family of I^2C-bus compatible devices.

8.2 CPU timing

A machine cycle consists of a sequence of 6 states. Each state lasts for two oscillator periods, thus a machine cycle takes 12 oscillator periods or 1 μs if the oscillator frequency (f_{osc}) is 12 MHz.

9 MEMORY ORGANIZATION

The P8xCL580 has 6 kbytes of Program Memory (ROM; P83CL580 only) plus 256 bytes of Data Memory (RAM) on board. The device has separate address spaces for Program and Data Memory (see Fig.6). Using Port latches P0 and P2, the P8xCL580 can address up to 64 kbytes of external memory. The CPU generates both read ($\overline{RD}$) and write ($\overline{WR}$) signals for external Data Memory accesses, and the read strobe ($\overline{PSEN}$) for external Program Memory.

9.1 Program Memory

The P83CL580 contains 6 kbytes of internal ROM. After reset the CPU begins execution at location 0000H. The lower 6 kbytes of Program Memory can be implemented in either on-chip ROM or external Program Memory.

If the $\overline{EA}$ pin is tied to V_{DD}, then Program Memory fetches from addresses 0000H to 17FFH are directed to the internal ROM. Fetches from addresses 1800H to FFFFH are directed to external ROM. Program Counter values greater than 17FFH are automatically addressed to external memory regardless of the state of the $\overline{EA}$ pin.

9.2 Data Memory

The P8xCL580 contains 256 bytes of internal RAM and 40 Special Function Registers (SFRs). Figure 6 shows the internal Data Memory space divided into the lower 128 bytes, the upper 128 bytes, and the SFRs space. Internal RAM locations 0 to 127 are directly and indirectly addressable. Internal RAM locations 128 to 255 are only indirectly addressable. The Special Function Register locations 128 to 255 bytes are only directly addressable.

9.3 Special Function Registers (SFRs)

The upper 128 bytes are the address locations of the SFRs. Figures 7 and 8 show the Special Function Registers space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 directly addressable locations in the SFR address space. Bit addressable SFRs are those that end in 000B.

9.4 Addressing

The P8xCL580 has five methods for addressing source operands:

- Register
- Direct
- Indirect
- Immediate
- Base-Register plus Index-Register-Indirect.

The first three methods can be used for addressing destination operands. Most instructions have a 'destination/source' field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four register banks through Direct or Indirect
- Lower 128 bytes of internal RAM through Direct or Indirect; upper 128 bytes of internal RAM through Direct
- Special Function Registers through Direct
- External Data Memory through Indirect
- Program Memory look-up tables through Base-Register plus Index-Register-Indirect.

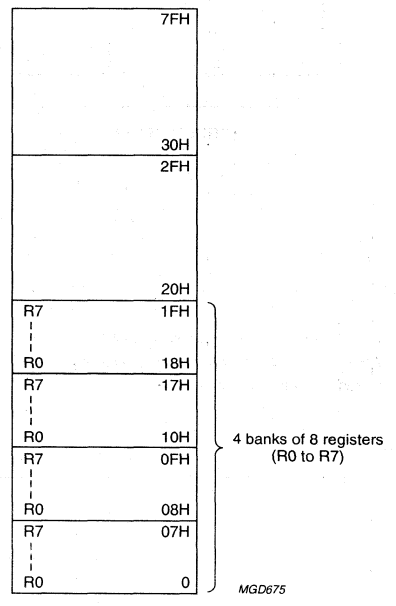
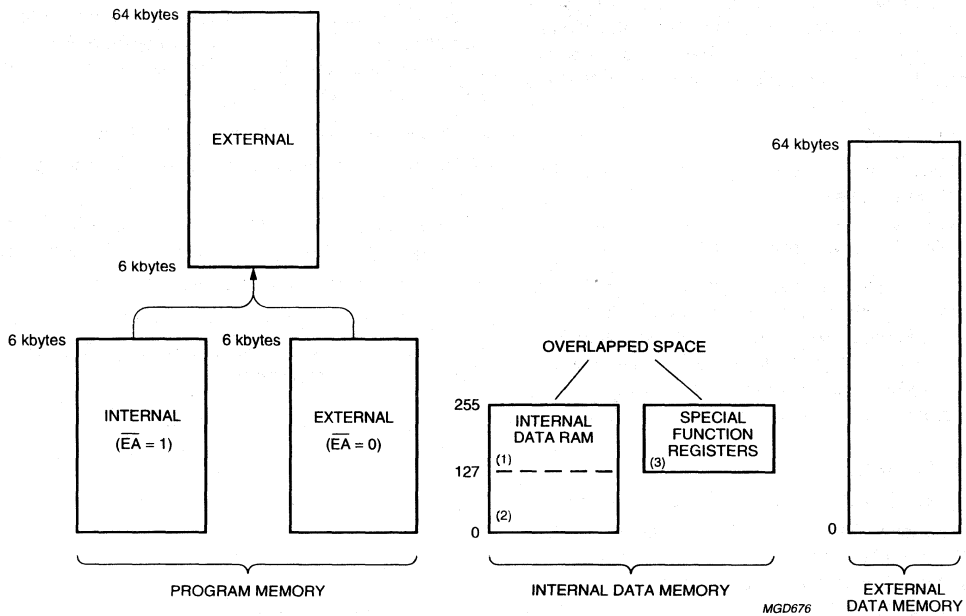


Fig.5 The lower 128 bytes of internal RAM.



(1) Accessible via indirect addressing only.
(2) Accessible via direct and indirect addressing.
(3) Accessible via direct addressing.

Fig.6 Memory map.

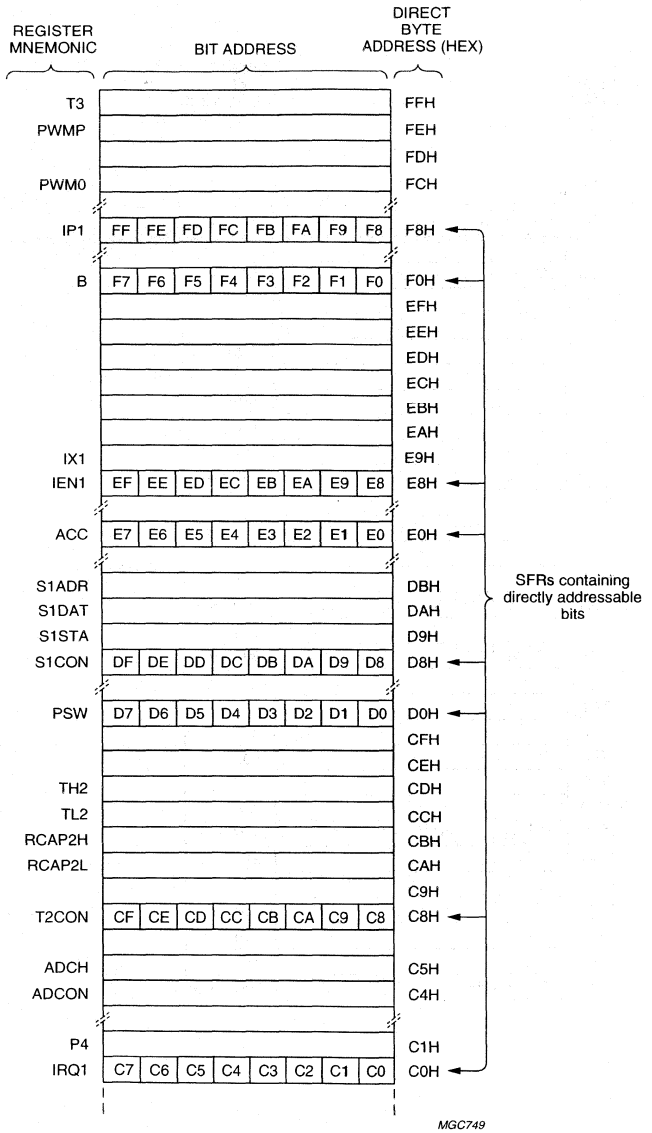


Fig.7 Special Function Register memory map.

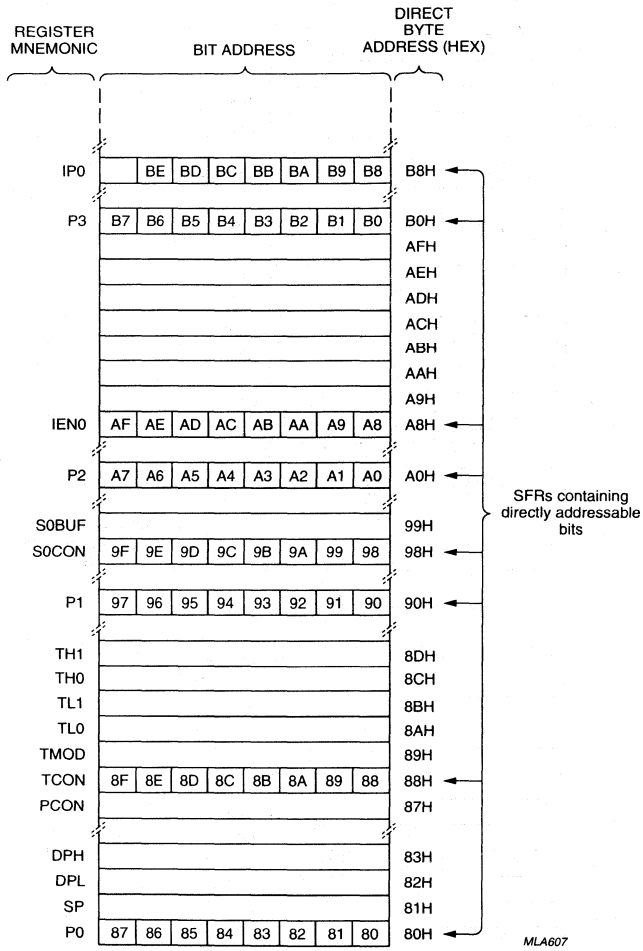


Fig.8 Special Function Register memory map (continued).

10 I/O FACILITIES

10.1 Ports

The P8xCL580 has 40 I/O lines treated as one 8-bit port plus 32 individually addressable bits or as five parallel 8-bit addressable ports. Port 4 has no alternative function. Ports 0, 1, 2 and 3 have the following alternative functions:

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Used for a number of special functions:

- Provides the inputs for the external interrupts: $\overline{INT2}$ to $\overline{INT8}$.
- External activation of Timer 2: T2.
- External trigger of the ADC: STADC.
- The I^2C-bus interface: SCL and SDA.

Port 2 Provides the high-order address when expanding the device with external Program or Data Memory.

Port 3 Pins can be configured individually to provide:

- External interrupt request inputs: $\overline{INT1}$ and $\overline{INT0}$.
- Counter input: T1 and T0.
- Control signals to read and write to external memories: $\overline{RD}$ and $\overline{WR}$.
- UART input and output: RXD and TXD.

To enable a port pin alternative function, the port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (SFRs P0 to P4), an output driver and input buffer. Ports 1, 2, 3 and 4 have internal pull-ups (except P1.6 and P1.7). Figure 9(a) shows that the strong transistor 'p1' is turned on for only 2 oscillator periods after a LOW-to-HIGH transition in the port latch. When on, it turns on 'p3' (a weak pull-up) through the inverter. This inverter and 'p3' form a latch which holds the logic 1. In Port 0 the pull-up 'p1' is only on when emitting logic 1s for external memory access. Writing a logic 1 to a Port 0 bit latch leaves both output transistors switched off so that the pin can be used as an high-impedance input.

10.2 Port options

Thirtyeight of the 40 port pins (excluding P1.6 and P1.7 with option 2S only) may be individually configured with one of the following options. These options are also shown in Fig.9.

Option 1 **Standard Port**; quasi-bidirectional I/O with pull-up. The strong booster pull-up 'p1' is turned on for two oscillator periods after a LOW-to-HIGH transition in the port latch; Fig.9(a).

Option 2 **Open-drain**; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; see Fig.9(b).

Option 3 **Push-pull**; output with drive capability in both polarities. Under this option, pins can only be used as outputs; see Fig.9(c).

10.3 Port 0 options

The definition of port options for Port 0 is slightly different. Two cases are considered. First, access to external memory ($\overline{EA}$ = 0 or access above the built-in memory boundary) and second, I/O accesses.

10.3.1 External memory accesses

Option 1 True logic 0 and logic 1 are written as address to the external memory (strong pull-up to be used).

Option 2 An external pull-up resistor is required for external accesses.

Option 3 Not allowed for external memory accesses as the port can only be used as output.

10.3.2 I/O Accesses

Option 1 When writing a logic 1 to the port latch, the strong pull-up 'p1' will be on for 2 oscillator periods. No weak pull-up exists. Without an external pull-up, this option can be used as a high-impedance input.

Option 2 Open-drain; quasi-directional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor. See Fig.9(b).

Option 3 Push-Pull; output with drive capability in both polarities. Under this option pins can only be used as outputs. See Fig.9(c).

10.4 SET/RESET options

Individual mask selection of the post-reset state is available with any of the above pins. The required selection is made by appending 'S' or 'R' to Options 1, 2, or 3 above.

Option R RESET, at reset this pin will be initialized LOW.

Option S SET, at reset this pin will be initialized HIGH.

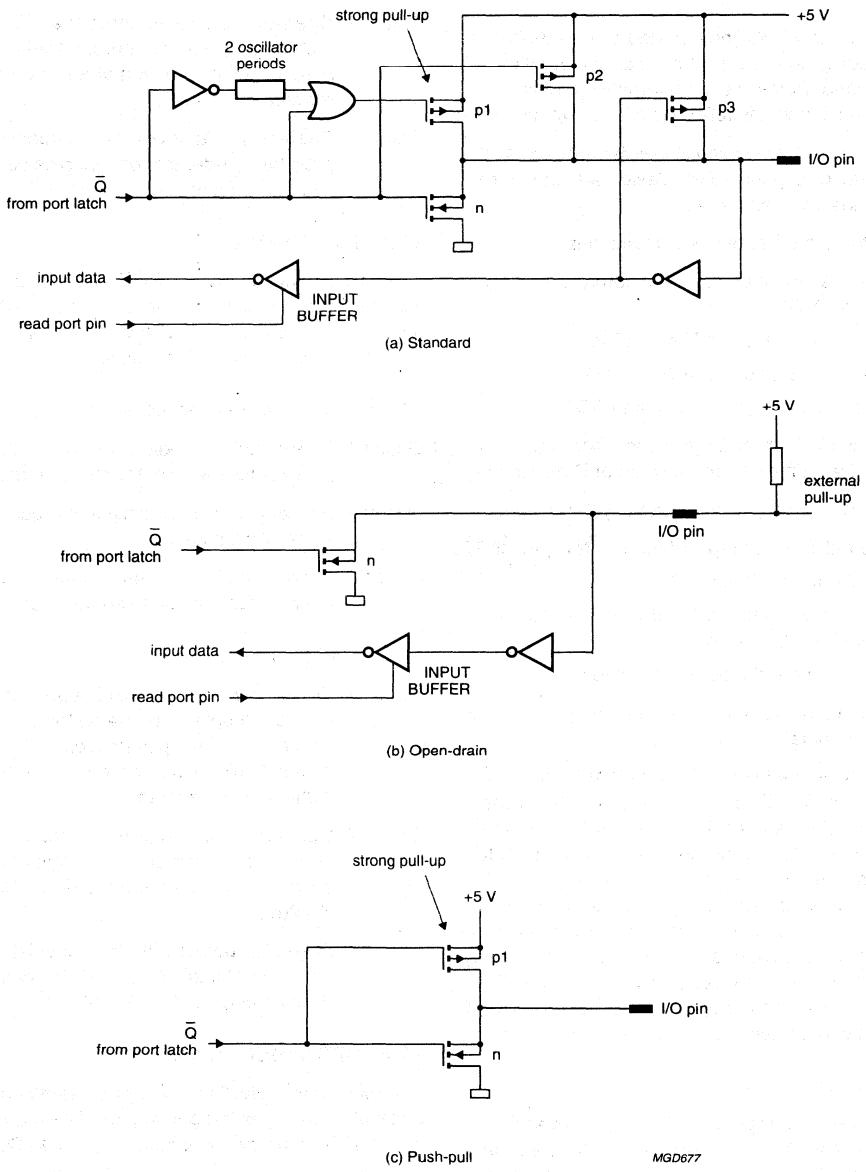


Fig.9 Port configuration options.

11 TIMER/EVENT COUNTERS

The P8xCL580 contains three 16-bit timer/event counter registers; Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

In the 'Timer' operating mode the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is $1/12 \times f_{osc}$.

In the 'Counter' operating mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes 2 machine cycles (24 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $1/24 \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

11.1 Timer 0 and Timer 1

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

11.2 Timer T2

Timer T2 is a 16-bit timer/counter that can operate (like Timer 0 and 1) either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register; see Tables 2 and 3.

Three operating modes are available Capture, Auto-reload and Baud Rate Generator, which also are selected via the T2CON register; see Table 4.

11.2.1 CAPTURE MODE

Figure 10 shows the Capture mode. Two options in this mode, may be selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt.

11.2.2 AUTO-RELOAD MODE

Figure 11 shows the Auto-reload mode. Also two options in this mode are selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit.

11.2.3 BAUD RATE GENERATOR MODE

The Baud Rate Generator mode is selected when RTCLK = 1. It will be described in conjunction with the serial port (UART); see Section 16.3.2.

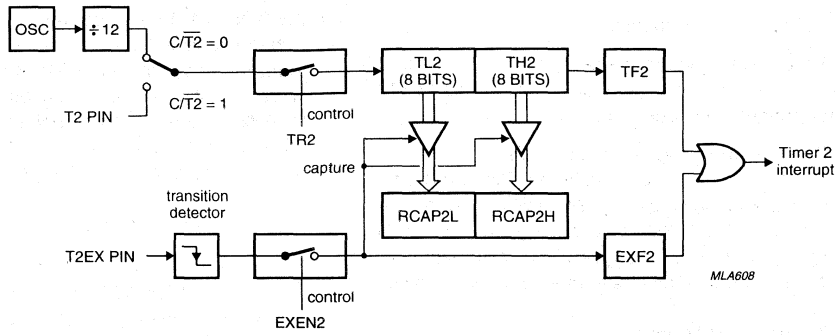


Fig.10 Timer 2 in Capture mode.

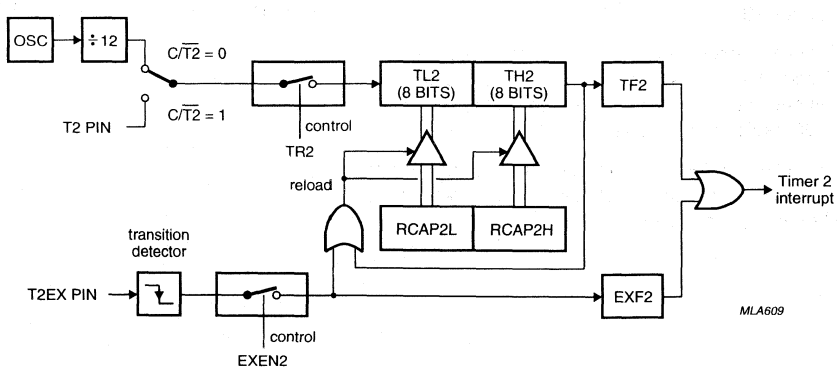


Fig.11 Timer 2 in Auto-Reload mode.

11.3 Timer/Counter 2 Control Register (T2CON)

Table 2 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	GF2	RTCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 3 Description of T2CON bits.

BIT	SYMBOL	DESCRIPTION
7	TF2	**Timer 2 overflow flag**. Set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when RTCLK = 1.
6	EXF2	**Timer 2 external flag.** Set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
5	GF2	**General purpose flag** bit.
4	RTCLK	**Receive/transmit clock flag**. When set, causes the UART serial port to use Timer 2 overflow pulses for its receive and transmit clock in Modes 1 and 3. RTCLK = 0 causes Timer 1 overflows to be used for the receive and transmit clock.
3	EXEN2	**Timer 2 external enable flag**. When set, allows a capture or reload to occur as a result of a negative transition on T2EX, if Timer 2 is not being used to clock the serial port. EXEN2 = 0, causes Timer 2 to ignore events at T2EX.
2	TR2	**Start/stop control for Timer 2**. TR2 = 1 starts the timer.
1	C/$\overline{T2}$	**Timer or counter select for Timer 2**. C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $^1/_{12} \times f_{osc}$. C/$\overline{T2}$ = **1** selects the external event counter; negative edge triggered.
0	CP/$\overline{RL2}$	**Capture/Reload flag**. When set, captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When RTCLK = 1, this bit is ignored and the timer is forced to auto-reload on a Timer 2 overflow.

Table 4 Timer 2 operating modes; X = don't care.

RTCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	Off

11.4 Watchdog Timer

In addition to Timer T2 and the standard timers, a Watchdog Timer (consisting of an 11-bit prescaler and an 8-bit timer) is also incorporated.

The Watchdog Timer is controlled by the Watchdog Enable pin ($\overline{EWN}$). When $\overline{EWN}$ = 0, the timer is enabled and the Power-down mode is disabled. When $\overline{EWN}$ = 1, the timer is disabled and the Power-down mode is enabled. In the Idle mode the Watchdog Timer and reset circuitry remain active.

The Watchdog Timer is shown in Fig. 12.

The timer frequency is derived from the oscillator frequency using the following formula:

$$f_{timer} = \frac{f_{osc}}{(12 \times 2048)}.$$

When a timer overflow occurs, the microcontroller is reset and a reset output pulse is generated at the RST pin. To prevent a system reset the timer must be reloaded in time by the application software. If the processor suffers a hardware/software malfunction, the software will fail to reload the timer. This failure will produce a reset upon overflow thus preventing the processor running out of control.

The Watchdog Timer can only be reloaded if the condition flag WLE (PCON.4) has been previously set by software. At the moment the counter is loaded the condition flag is automatically cleared.

The time interval between the timer reloading and the occurrence of a reset is dependent upon the reloaded value. For example, this time period may range from 2 ms to 500 ms when using an oscillator frequency f_{osc} = 12 MHz.

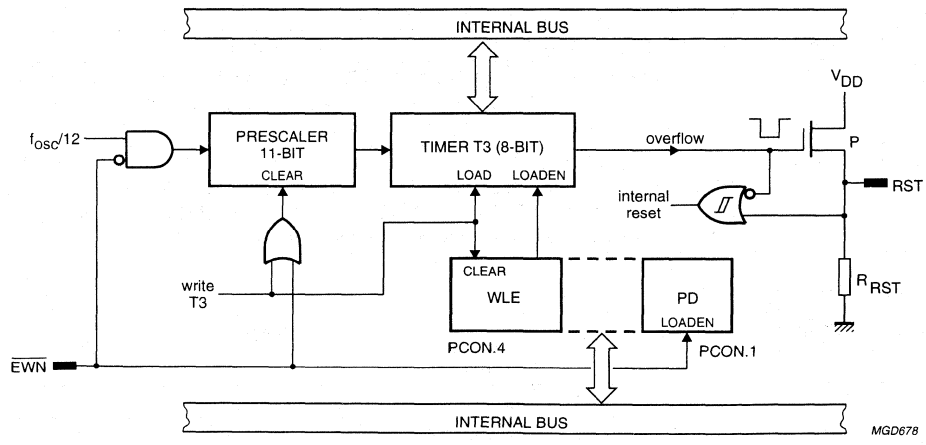


Fig.12 Functional diagram of the T3 Watchdog Timer.

12 PULSE WIDTH MODULATED OUTPUT

One Pulse Width Modulated output channel ($\overline{PWM0}$) is provided which outputs pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler (PWMP) that generates the clock for the counter. The 8-bit counter counts modulo 255, i.e. from 0 to 254 inclusive. The value held in the 8-bit counter is compared to the contents of the register PWM0.

Provided the contents of this register are greater than the counter value, the $\overline{PWM0}$ output is set LOW. If the contents of register PWM0 are equal to, or less than the counter value, the $\overline{PWM0}$ output is set HIGH. The pulse-width-ratio is therefore defined by the contents of register PWM0. The pulse-width-ratio will be in the range 0 to $^{255}/_{255}$ and may be programmed in increments of $^{1}/_{255}$.

The repetition frequency (f_{PWM}) at the $\overline{PWM0}$ output is given by:

$$f_{PWM} = \frac{f_{osc}}{\{2 \times (1 + PWMP) \times 255\}}$$

For f_{osc} = 12 MHz the above formula gives a repetition frequency range of 92 Hz to 23.5 kHz.

By loading the PWM0 register with either 00H or FFH, the $\overline{PWM0}$ output can be retained at a constant HIGH or LOW level respectively. When loading FFH into the PWM0 register, the 8-bit counter will never actually reach this value.

The $\overline{PWM0}$ output pin is driven by push-pull drivers and is not shared with any other function.

12.1 Prescaler Frequency Control Register (PWMP)

Table 5 Prescaler Frequency Control Register (address FEH)

7	6	5	4	3	2	1	0
PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Table 6 Description of PWMP bits

BIT	SYMBOL	DESCRIPTION
7 to 1	PWMP.7 to PWMP.0	Prescaler division factor = (PWMP) + 1.

12.2 Pulse Width Register (PWM0)

Table 7 Pulse Width Register (address FCH)

7	6	5	4	3	2	1	0
PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Table 8 Description of PWM0 bits

BIT	SYMBOL	DESCRIPTION
7 to 1	PWM0.7 to PWM0.0	LOW/HIGH ratio of $\overline{PWM0}$ signal = $\frac{(PWM0)}{\{255 - (PWM0)\}}$

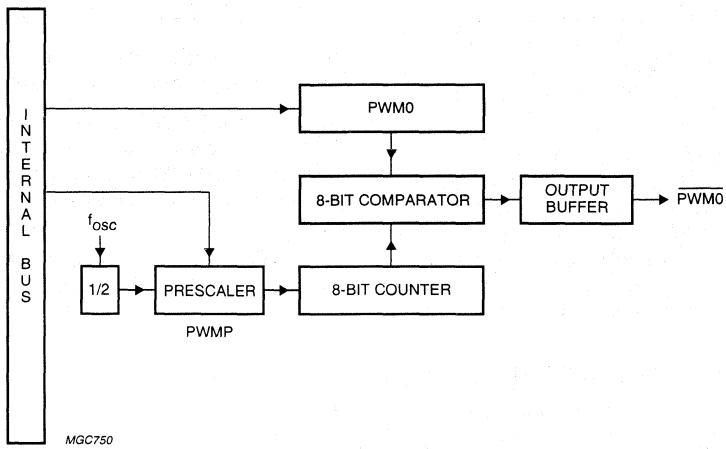


Fig.13 Functional diagram of Pulse Width Modulated output ($\overline{PWM0}$).

13 ANALOG-TO-DIGITAL CONVERTER (ADC)

The analog input circuitry consists of a 4-bit analog multiplexer and an ADC with 8-bit resolution. The analog reference voltage ($V_{ref(p)(A)}$) and analog ground (V_{SSA}) are connected via separate input pins. The conversion is selectable from 24 machine cycles (24 μs at f_{osc} = 12 MHz) to 48 machine cycles. The functional diagram of the ADC is shown in Fig. 14.

The ADC is controlled using the ADC Control Register (ADCON). Input channels are selected by the analog multiplexer via the ADCON register bits AADR0 and AADR1. The completion of the 8-bit ADC conversion is flagged by ADCI in the ADCON register and the result is stored in the Special Function Register ADCH (address C5H).

An ADC conversion in progress is unaffected by an external software ADC start.

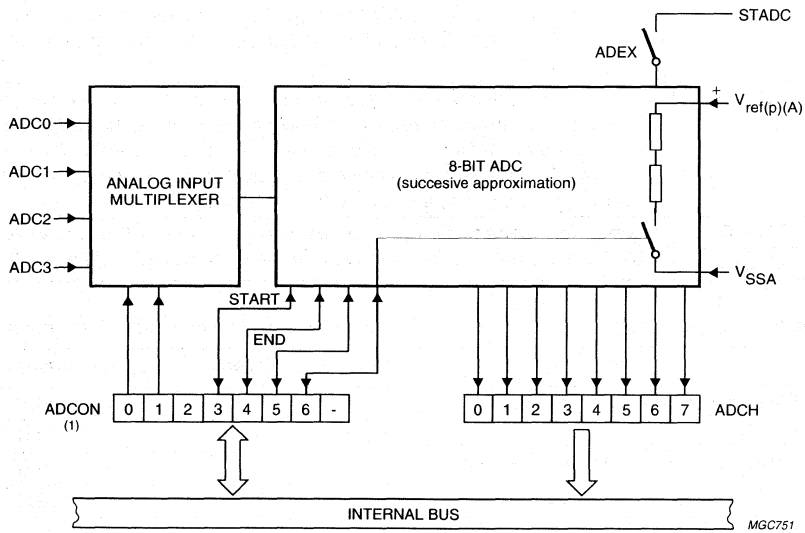
The result of a completed conversion remains unaffected provided ADCI = 1. While ADCS = 1 or ADCI = 1, a new ADC start will be blocked and consequently lost.

An ADC conversion already in progress is aborted when the Power-down mode is entered. The result of a completed conversion (ADCI = 1) remains unaffected when entering the Idle or Power-down mode.

The analog-to-digital conversion can be started in 3 ways:

- Start in operating mode, continue in operating mode.
- Start in operating mode, by setting the ADCS bit, then go to Idle mode.
- Set the ADEX bit, go to the Idle mode and start conversion externally via the STADC pin.

For the three cases mentioned above the internal flag ADCI is set upon completion of the conversion.



(1) For the descriptions of ADCON bits see Table 10.

Fig.14 Functional diagram of analog input.

13.1 ADC Control Register (ADCON)

Table 9 ADC Control Register (address C4H)

7	6	5	4	3	2	1	0
–	ADPD	ADEX	ADCI	ADCS	CKDIV	AADR1	AADR0

Table 10 Description of ADCON bits

BIT	SYMBOL	DESCRIPTION
7	–	Reserved.
6	ADPD	**Power-down.** This bit switches off the resistor reference to save power even when the CPU is operating.
5	ADEX	**Enable external start of conversion**. This bit determines whether a conversion can be started using the external pin STADC. When ADEX = 0, a conversion cannot be started externally using STADC. When ADEX = 1, a conversion can be started externally using STADC.
4	ADCI	**ADC interrupt flag**. This flag is set when an ADC conversion result is ready to be read. An interrupt is invoked if this is enabled. This flag must be cleared by software (it cannot be set by software); see Table 11.
3	ADCS	**ADC start and status flag**. When this bit is set an ADC conversion is started. ADCS may be set by software or by the external signal STADC. The ADC logic ensures that this signal is HIGH while the ADC is busy. On completion of the conversion ADCS is reset and after that the interrupt flag ADCI is set. ADCS cannot be reset by software; see Table 11.
2	CKDIV	This bit selects the conversion time, in terms of instruction cycles. This allows the CPU to be run at the maximum frequency (12 MHz) yet keeping the ADC timing at low frequency. When CKDIV = 0, the conversion time is equivalent to 24 instruction cycles. When CKDIV = 1, the conversion time is equivalent to 48 instruction cycles. The conversion time includes a sampling time of 6 cycles.
1	AADR1	**Analog input select**. These bits are used to select one of the four analog inputs; see Table 12. They only can be changed when ADCI and ADCS are both LOW.
0	AADR0	

Table 11 Analog-to-digital operation

ADCI	ADCS	OPERATION
0	0	ADC not busy; a conversion can be started.
0	1	ADC busy; start of a new conversion is blocked.
1	0	Conversion completed; start of a new conversion is blocked.
1	1	Intermediate status for a maximum of one machine cycle before conversion is completed (ADCI = 1, ADCS = 0).

Table 12 Selection of analog input channel

AADR1	AADR0	SELECTED CHANNEL
0	0	AD0
0	1	AD1
1	0	AD2
1	1	AD3

14 REDUCED POWER MODES

There are two software selectable modes of reduced activity for further power reduction: Idle and Power-down.

14.1 Idle mode

Idle mode operation permits the interrupt, serial ports, timer blocks, PWM and ADC to continue to function while the clock to the CPU is halted.

The following functions remain active during the Idle mode:

- Timer 0, Timer 1, Timer 2 and Timer 3
- UART, I^2C-bus interface
- External interrupt
- $\overline{PWM0}$ (reset; output = HIGH)
- ADC.

These functions may generate an interrupt or reset; thus ending the Idle mode.

The instruction that sets bit IDL (PCON.0) is the last instruction executed in the normal operating mode before the Idle mode is activated. Once in Idle mode, the CPU status is preserved along with the Stack Pointer, Program Counter, Program Status Word and Accumulator. The RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 13.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause IDL (PCON.0) to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. The flag bits GF0 (PCON.2) and GF1 (PCON.3) may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an external hardware reset, or an internal reset caused by an overflow of Timer T2. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation. Reset redefines all SFRs but does not affect the on-chip RAM.

14.2 Power-down mode

The Power-down operation freezes the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register.

The instruction that sets PD (PCON.1) is the last executed prior to going into the Power-down mode. Once in the Power-down mode, the oscillator is stopped. The contents of the on-chip RAM and the SFRs are preserved. The port pins output the value held by their respective SFRs. ALE and $\overline{PSEN}$ are held LOW.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The supply voltage must not be reduced until the Power-down mode is entered, and must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

14.3 Wake-up mode

Setting the PD flag in the PCON register forces the controller into the Power-down mode. Setting this flag enables the controller to be woken-up from the Power-down mode with either the external interrupts $\overline{INT2}$ to $\overline{INT8}$, or a reset operation. The wake-up operation has two basic approaches as explained in Section 14.3.1; 14.3.2 and illustrated in Fig.15.

14.3.1 WAKE-UP USING $\overline{INT2}$ TO $\overline{INT8}$

If any of the interrupts $\overline{INT2}$ to $\overline{INT8}$ are enabled, the device can be woken-up from the Power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods. This is controlled by an on-chip delay counter.

14.3.2 WAKE-UP USING RST

To wake-up the P8xCL580, the RST pin must be kept HIGH for a minimum of 24 periods. The on-chip delay counter is inactive. The user must ensure that the oscillator is stable before any operation is attempted.

14.4 Status of external pins

The status of the external pins during Idle and Power-down mode is shown in Table 13. If the Power-down mode is activated whilst accessing external Program Memory, the port data that is held in the Special Function Register P2 is restored to Port 2.

If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor 'p1'; see Fig.9(a).

Table 13 Status of external pins during Idle and Power-down modes

MODE	MEMORY	ALE	$\overline{\text{PSEN}}$	$\overline{\text{PWM0}}$	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4
Idle	internal	1	1	active	port data	port data	port data	port data	port data
	external	1	1	active	floating	port data	address	port data	port data
Power-down	internal	0	0	HIGH	port data	port data	port data	port data	port data
	external	0	0	HIGH	floating	port data	port data	port data	port data

14.5 Power Control Register (PCON)

Idle and Power-down modes are activated by software using this SFR. PCON is not bit addressable, the reset value of PCON is 0XX00000B.

Table 14 Power Control Register (address 87H)

7	6	5	4	3	2	1	0
SMOD	–	–	WLE	GF1	GF0	PD	IDL

Table 15 Description of PCON bits

BIT	SYMBOL	DESCRIPTION
7	SMOD	**Double Baud rate bit**. When set to a logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3.
6 and 5	–	Reserved.
4	WLE	**Watchdog Load Enable**. This flag must be set by software prior to loading the Watchdog Timer (T3). It is cleared when T3 is loaded.
3 and 2	GF1 and GF0	**General purpose flag bits**.
1	PD	**Power-down bit**. Setting this bit activates the Power-down mode. This bit can only be set if input $\overline{\text{EWN}}$ is HIGH. If a logic 1 is written to both PD and IDL at the same time, PD takes precedence.
0	IDL	**Idle mode bit**. Setting this bit activates the Idle mode.

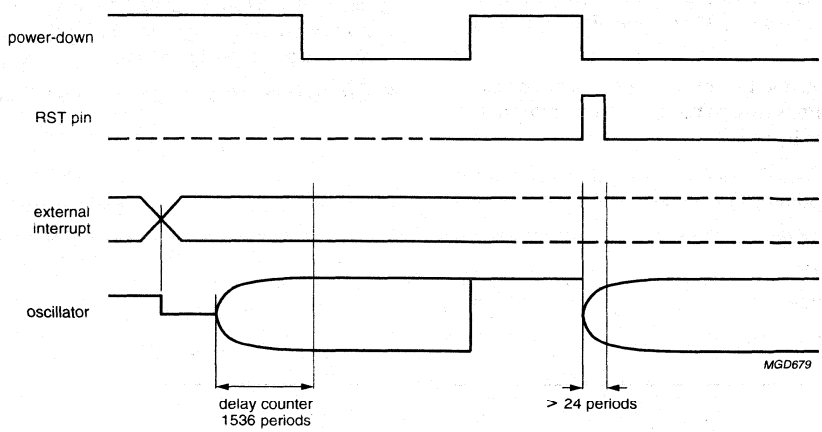


Fig.15 Wake-up operation.

15 I²C-BUS SERIAL I/O

The serial port supports the twin line I²C-bus, which consists of a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines P1.7 and P1.6 respectively.

The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

The I²C-bus serial I/O has complete autonomy in byte handling and operates in 4 modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

These functions are controlled by the Serial Control Register S1CON. S1STA is the Status Register whose contents may also be used as a vector to various service routines. S1DAT is the Data Shift Register and S1ADR is the Slave Address Register. Slave address recognition is performed by on-chip hardware.

Figure 16 is the block diagram of the I²C-bus serial I/O.

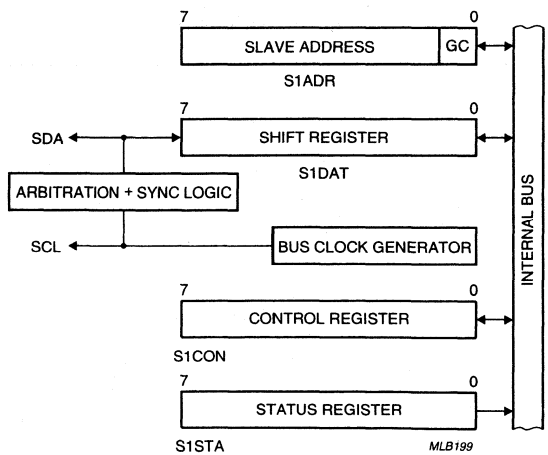


Fig.16 Block diagram of I²C-bus serial I/O.

15.1 Serial Control Register (S1CON)

Table 16 Serial Control Register (SFR address D8H)

7	6	5	4	3	2	1	0
CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Table 17 Description of S1CON bits

BIT	SYMBOL	DESCRIPTION
7	CR2	This bit along with bits CR1 (S1CON.1) and CR0 (S1CON.0) determines the serial clock frequency when SIO is in the Master mode. See Table 18.
6	ENS1	**ENABLE serial I/O**. When ENS1 = 0, the serial I/O is disabled. SDA and SCL outputs are in the high impedance state; P1.6 and P1.7 function as open-drain ports. When ENS1 = 1, the serial I/O is enabled. Output port latches P1.6 and P1.7 must be set to logic 1.
5	STA	**START flag**. When this bit is set in Slave mode, the SIO hardware checks the status of the I^2C-bus and generates a START condition if the bus is free or after the bus becomes free. If STA is set while the SIO is in Master mode, SIO will generate a repeated START condition.
4	STO	**STOP flag**. With this bit set while in Master mode a STOP condition is generated. When a STOP condition is detected on the I^2C-bus, the SIO hardware clears the STO flag. STO may also be set in Slave mode in order to recover from an error condition. In this case no STOP condition is transmitted to the I^2C-bus. However, the SIO hardware behaves as if a STOP condition has been received and releases the SDA and SCL. The SIO then switches to the not addressed slave receiver mode. The STOP flag is cleared by the hardware.
3	SI	**SIO interrupt flag**. This flag is set, and an interrupt is generated, after any of the following events occur: • A start condition is generated in Master mode • Own slave address has been received during AA = 1 • The general call address has been received while GC (S1ADR.0) = 1 and AA = 1 • A data byte has been received or transmitted in Master mode (even if arbitration is lost) • A data byte has been received or transmitted as selected slave • A Stop or Start condition is received as selected slave receiver or transmitter.
2	AA	**Assert Acknowledge**. When this bit is set, an acknowledge (low level to SDA) is returned during the acknowledge clock pulse on the SCL line when: • Own slave address is received • General call address is received; GC (S1ADR.0) = 1 • A data byte is received while the device is programmed to be a Master Receiver • A data byte is received while the device is a selected Slave Receiver. When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own slave address or general call address is received.
1	CR1	These two bits along with the CR2 (S1CON.7) bit determine the serial clock frequency when SIO is in the Master mode. See Table 18.
0	CR0	

Table 18 Selection of the serial clock frequency SCL in a Master mode of operation

CR2	CR1	CR0	f_{osc} DIVISOR	BIT RATE (kHz) AT f_{osc}		
				3.58 MHz	6 MHz	12 MHz
0	0	0	256	14.0	23.4	46.9
0	0	1	224	16.0	26.8	53.6
0	1	0	192	18.6	31.3	62.5
0	1	1	160	22.4	37.5	75.0
1	0	0	960	3.73	6.25	12.5
1	0	1	120	29.8	50.0	100.0
1	1	0	60	59.7	100.0	–
1	1	1	not allowed	–	–	–

15.2 Serial Status Register (S1STA)

S1STA is a read-only register.The contents of this register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I^2C-bus. The status codes for all possible modes of the I^2C-bus interface are given in Tables 21 to 25.

Table 19 Serial Status Register (address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 20 Description of S1STA bits

BIT	SYMBOL	DESCRIPTION
3 to 7	SC4 to SC0	5-bit status code.
0 to 2	–	These three bits are always zero.

Table 21 MST/TRX mode

S1STA VALUE	DESCRIPTION
08H	A START condition has been transmitted.
10H	A repeated START condition has been transmitted.
18H	SLA and W have been transmitted, ACK has been received.
20H	SLA and W have been transmitted, $\overline{ACK}$ received.
28H	DATA of S1DAT has been transmitted, ACK received.
30H	DATA of S1DAT has been transmitted, $\overline{ACK}$ received.
38H	Arbitration lost in SLA, R/W or DATA.

Table 22 MST/REC mode

S1STA VALUE	DESCRIPTION
08H	A START condition has been transmitted.
10H	A repeated START condition has been transmitted.
38H	Arbitration lost while returning $\overline{ACK}$.
40H	SLA and R have been transmitted, ACK received.
48H	SLA and R have been transmitted, $\overline{ACK}$ received.
50H	DATA has been received, ACK returned.
58H	DATA has been received, $\overline{ACK}$ returned.

Table 23 SLV/REC mode

S1STA VALUE	DESCRIPTION
60H	Own SLA and W have been received, ACK returned.
68H	Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned.
70H	General CALL has been received, ACK returned.
78H	Arbitration lost in SLA, R/W as MST. General CALL has been received.
80H	Previously addressed with own SLA. DATA byte received, ACK returned.
88H	Previously addressed with own SLA. DATA byte received, $\overline{ACK}$ returned.
90H	Previously addressed with general CALL. DATA byte has been received, ACK has been returned.
98H	Previously addressed with general CALL. DATA byte has been received, $\overline{ACK}$ has been returned.
A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

Table 24 SLV/TRX mode

S1STA VALUE	DESCRIPTION
A8H	Own SLA and R have been received, ACK returned.
B0H	Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned.
B8H	DATA byte has been transmitted, ACK received.
C0H	DATA byte has been transmitted, $\overline{ACK}$ received.
C8H	Last DATA byte has been transmitted (AA = 0), ACK received.

Table 25 Miscellaneous.

S1STA VALUE	DESCRIPTION
00H	Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition.
F8H	No relevant state information available, SI = 0.

Table 26 Symbols used in Tables 21 to 25.

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	Read bit
W	Write bit
ACK	Acknowledgement (acknowledge bit is logic 0)
$\overline{ACK}$	No acknowledgement (acknowledge bit is logic 1)
DATA	8-bit data byte to or from I^2C-bus
MST	Master
SLV	Slave
TRX	Transmitter
REC	Receiver

15.3 Data Shift Register (S1DAT)

S1DAT contains the serial data to be transmitted or data which has just been received. The MSB (bit 7) is transmitted or received first; i.e. data shifted from right to left.

Table 27 Data Shift Register (SFR address DAH)

7	6	5	4	3	2	1	0
S1DAT.7	S1DAT.6	S1DAT.5	S1DAT.4	S1DAT.3	S1DAT.2	S1DAT.1	S1DAT.0

15.4 Address Register (S1ADR)

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter.

Table 28 Address Register (SFR address DBH)

7	6	5	4	3	2	1	0
SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	GC

Table 29 Description of S1ADR bits

BIT	SYMBOL	DESCRIPTION
7 to 1	SLA6 to SLA0	Own slave address.
0	GC	This bit is used to determine whether the general call address is recognized. When GC = 0, the general call address is not recognized; when GC = 1, the general call address is recognized.

16 STANDARD SERIAL INTERFACE SIO0: UART

This serial port is full duplex which means that it can transmit and receive simultaneously. It is also receive-buffered and can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte has not been read by the time the reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed via the Special Function Register S0BUF. Writing to S0BUF loads the transmit register and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0 Serial data enters and exits through RXD. TXD outputs the shift clock. Eight bits are transmitted/received (LSB first). The baud rate is fixed at $1/12 \times f_{osc}$. See Figs 18 and 19.

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). On receive, the stop bit goes into RB8 in Special Function Register S0CON. The baud rate is variable. See Figs 20 and 21.

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of a logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in S0CON, while the stop bit is ignored. The baud rate is programmable to either $1/32$ or $1/64 \times f_{osc}$. See Figs 22 and 23.

Mode 3 11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable. See Figs 24 and 25.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

16.1 Multiprocessor communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th bit goes into RB8. The following bit is the stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated, but only if RB8 = 1. This feature is enabled by setting bit SM2 in S0CON. One use of this feature, in multiprocessor systems, is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is HIGH in an address byte and LOW in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be sent. The slaves that were not being addressed leave their SM2 bits set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

16.2 Serial Port Control and Status Register (S0CON)

The Serial Port Control and Status Register is the Special Function Register S0CON. The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 30 Serial Port Control Register (address 98H)

7	6	5	4	3	2	1	0
SMO	SM1	SM2	REN	TB8	RB8	TI	RI

Table 31 Description of S0CON bits

BIT	SYMBOL	DESCRIPTION
7	SM0	These bits are used to select the serial port mode; see Table 32.
6	SM1	
5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In these modes, if SM2 = 1, then RI will not be activated if the received 9th data bit (RB8) is a logic 0. In Mode 1, if SM2 = 1, then RI will not be activated unless a valid stop bit was received. In Mode 0, SM2 should be a logic 0.
4	REN	Enables serial reception and is set by software to enable reception, and cleared by software to disable reception.
3	TB8	Is the 9th data bit that will be transmitted in Modes 2 and 3. Set or cleared by software as desired.
2	RB8	In Modes 2 and 3, is the 9th data bit received. In Mode 1, if SM2 = 0 then RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
1	TI	**The transmit interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit time in the other modes, in any serial transmission. Must be cleared by software.
0	RI	**The receive interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial transmission (except see SM2). Must be cleared by software.

Table 32 Selection of the serial port modes

SMO	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	Mode 0	Shift register	$^1/_{12} \times f_{osc}$
0	1	Mode 1	8-bit UART	variable
1	0	Mode 2	9-bit UART	$^1/_{32}$ or $^1/_{64} \times f_{osc}$
1	1	Mode 3	9-bit UART	variable

16.3 Baud rates

The baud rate in Mode 0 is fixed and may be calculated as:

$$\text{Baud Rate} = \frac{f_{osc}}{12}$$

The baud rate in Mode 2 depends on the value of the SMOD bit in Special Function Register PCON and may be calculated as:

$$\text{Baud Rate} = \frac{2^{SMOD}}{64} \times f_{osc}$$

- If SMOD = 0 (value on reset), the baud rate is $1/64 \times f_{osc}$
- If SMOD = 1, the baud rate is $1/32 \times f_{osc}$

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

16.3.1 Using Timer 1 to generate baud rates

When Timer 1 is used as the Baud Rate Generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of the SMOD bit as follows:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \text{Timer 1 Overflow Rate.}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either 'timer' or 'counter' operation in any of its 3 running modes. In most typical applications, it is configured for 'timer' operation, in the Auto-reload mode (high nibble of TMOD = 0010B). In this case the baud rate is given by the formula:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \frac{f_{osc}}{\{12 \times (256 - TH1)\}}$$

By configuring Timer 1 to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload, very low baud rates can be achieved. Table 33 lists commonly used baud rates and how they can be obtained from Timer 1.

Table 33 Commonly used baud rates generated by Timer 1

BAUD RATE (kb/s)	f_{osc} (MHz)	SMOD	C/T	TIMER 1 MODE	RELOAD VALUE
1000.0[1]	12.000	X[2]	X	X	X
375.0[3]	12.000	1	X	X	X
62.5[4]	12.000	1	0	Mode 2	FFH
19.2	11.059	1	0	Mode 2	FDH
9.6	11.059	0	0	Mode 2	FDH
4.8	11.059	0	0	Mode 2	FAH
2.4	11.059	0	0	Mode 2	F4H
1.2	11.059	0	0	Mode 2	E8H
137.5	11.986	0	0	Mode 2	1DH
110.0	6.000	0	0	Mode 2	72H
110.0	12.000	0	0	Mode 1	FEEBH

Notes

1. Maximum in Mode 0.
2. X = don't care
3. Maximum in Mode 2.
4. Maximum in Modes 1 and 3.

16.3.2 Using Timer 2 to generate baud rates

Timer 2 is selected as a Baud Rate Generator by setting the RTCLK bit in T2CON. The Baud Rate Generator mode is similar to the Auto-reload mode, in that a roll-over in TH2 causes Timer 2 registers to be reloaded with the 16-bit value held in the registers RCAP2H and RCAP2L, which are preset by software. Baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as specified below.

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer 2 can be configured for either 'timer' or 'counter' operation. In the most typical applications, it is configured for 'timer' operation ($C/\overline{T2} = 0$). 'Timer' operation is slightly different for Timer 2 when it is being used as a Baud Rate Generator. Normally, as a timer it would increment every machine cycle at a frequency of $1/12 \times f_{osc}$. However, as a Baud Rate Generator it increments every state time at a frequency of $1/2 \times f_{osc}$. In this case the baud rate in Modes 1 and 3 is determined as:

$$\text{Baud Rate} = \frac{f_{osc}}{32 \times \{65536 - (\text{RCAP2H; RCAP2L})\}}$$

Where (RCAP2H; RCAP2L) is the content of registers RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Baud Rate Generator mode for Timer 2 is shown in Fig.17. This figure is only valid if RTCLK = 1. At roll-over TH2 does not set the TF2 bit in T2CON and therefore, will not generate an interrupt. Consequently, the Timer 2 interrupt does not need to be disabled when in the Baud Rate Generator mode. If EXEN2 is set, a HIGH-to-LOW transition on T2EX will set the EXF2 bit, also in T2CON, but will not cause a reload from (RCAP2H; RCAP2L) to (TH2, TL2). Therefore, in this mode T2EX may be used as an additional external interrupt.

When Timer 2 is operating as a timer (TR2 = 1), in the Baud Rate Generator mode, registers TH2 and TL2 should not be accessed (read or write). Under these conditions the timer is being incremented every state time and therefore the results of a read or write may not be accurate. The registers RCAP2H and RCAP2L however, may be read but not written to. A write might overlap a reload and cause write and/or reload errors. If a write operation is required, Timer 2 or RCAP2H/RCAP2L should first be turned off by clearing the TR2 bit.

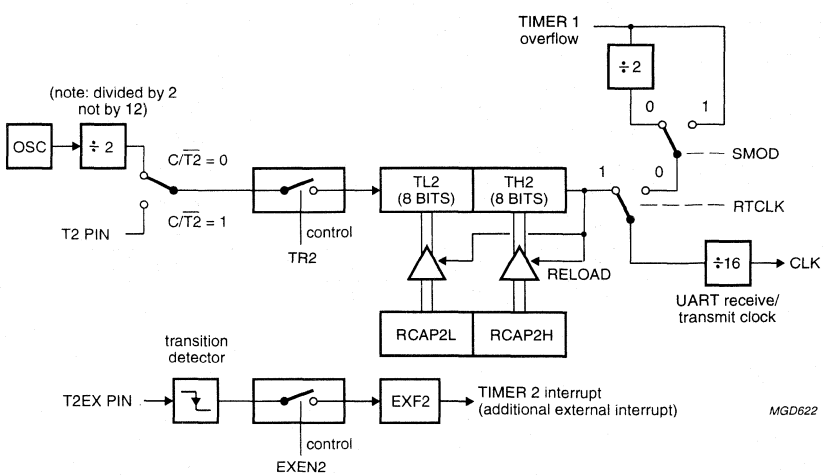


Fig.17 Timer 2 in Baud Rate Generator mode.

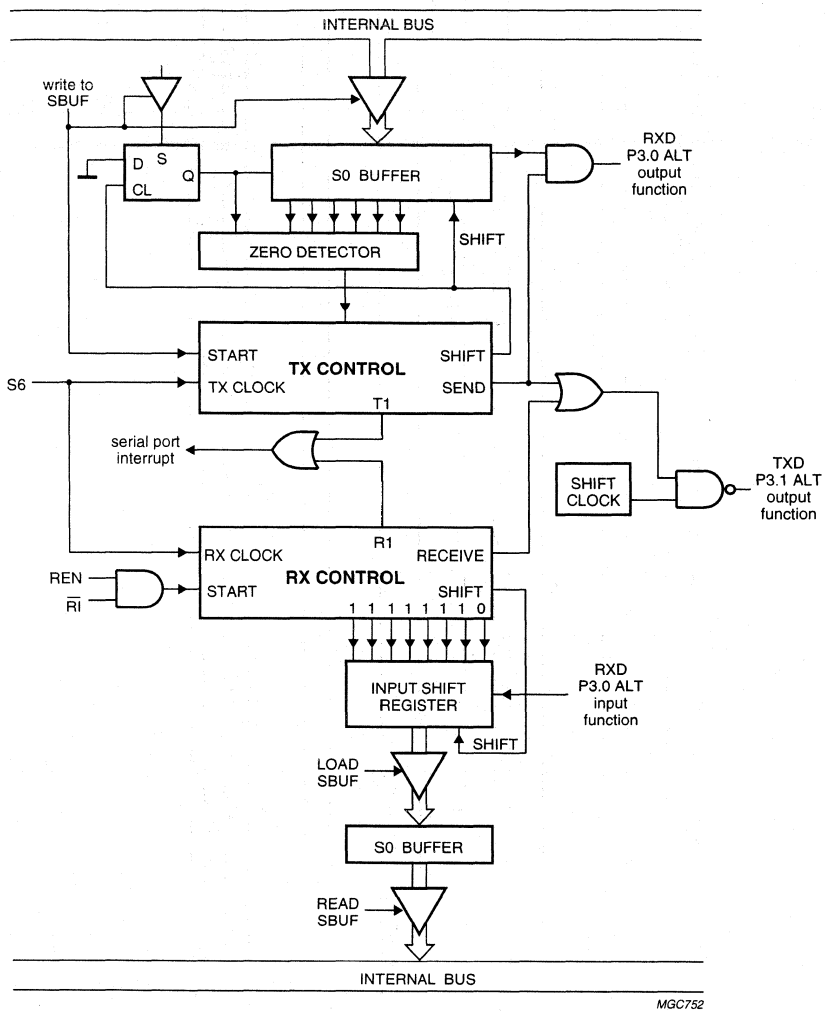


Fig.18 Serial port Mode 0.

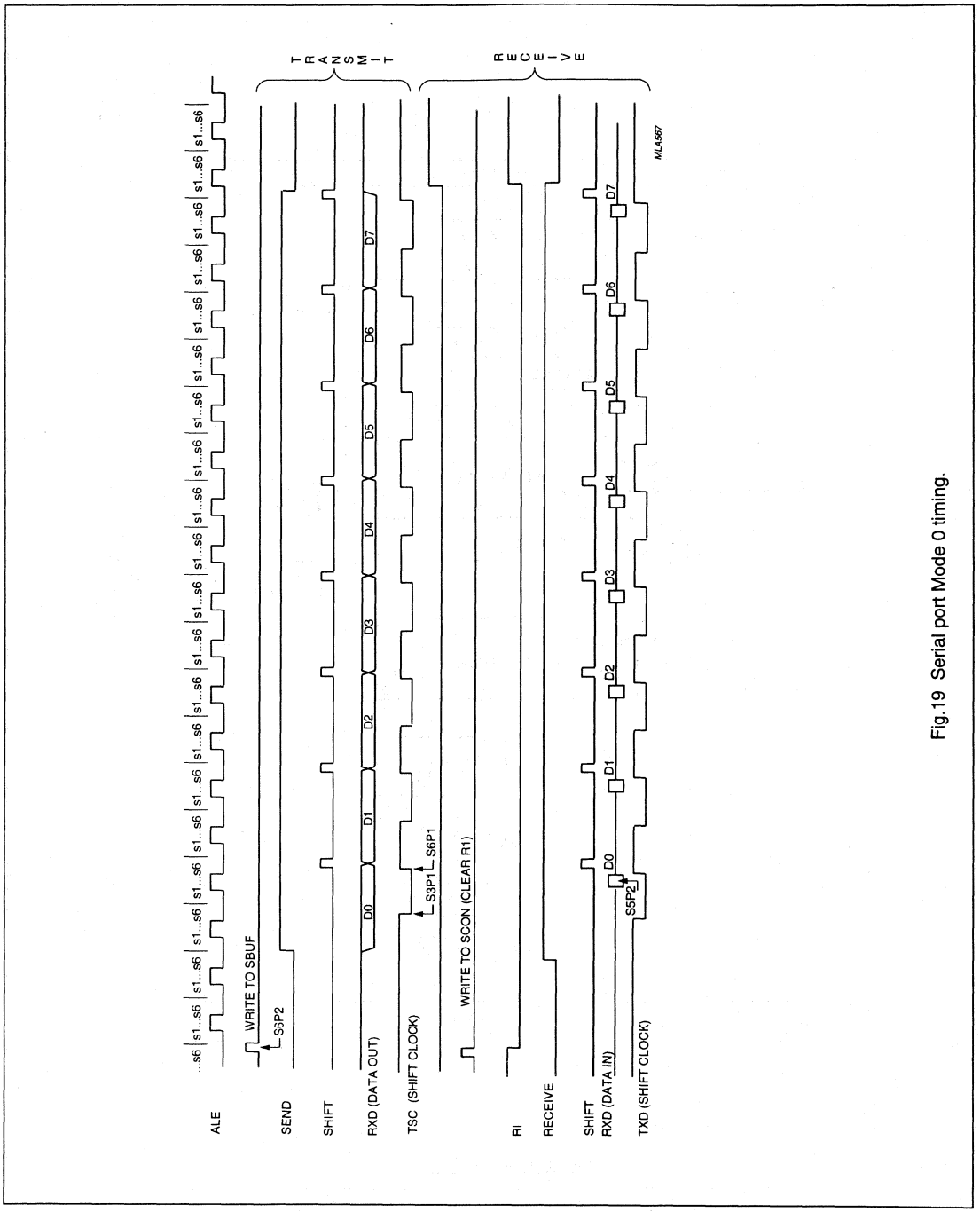


Fig.19 Serial port Mode 0 timing.

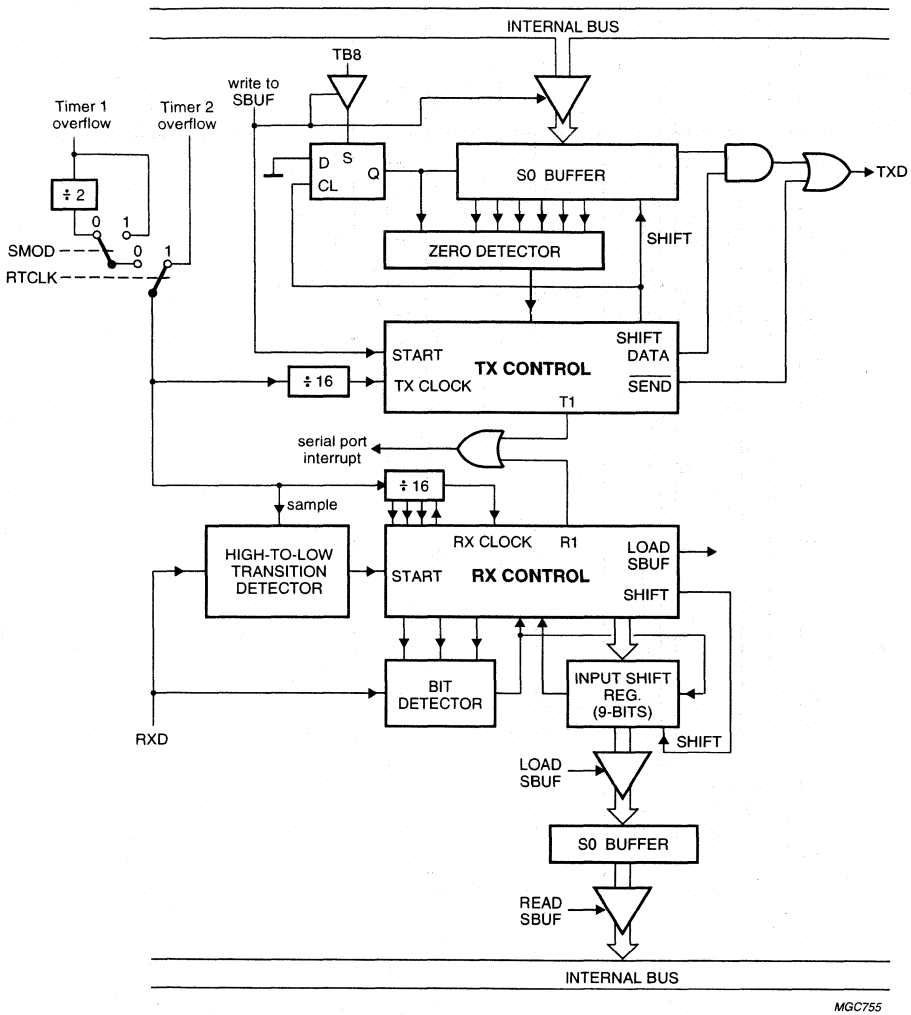


Fig.20 Serial port Mode 1.

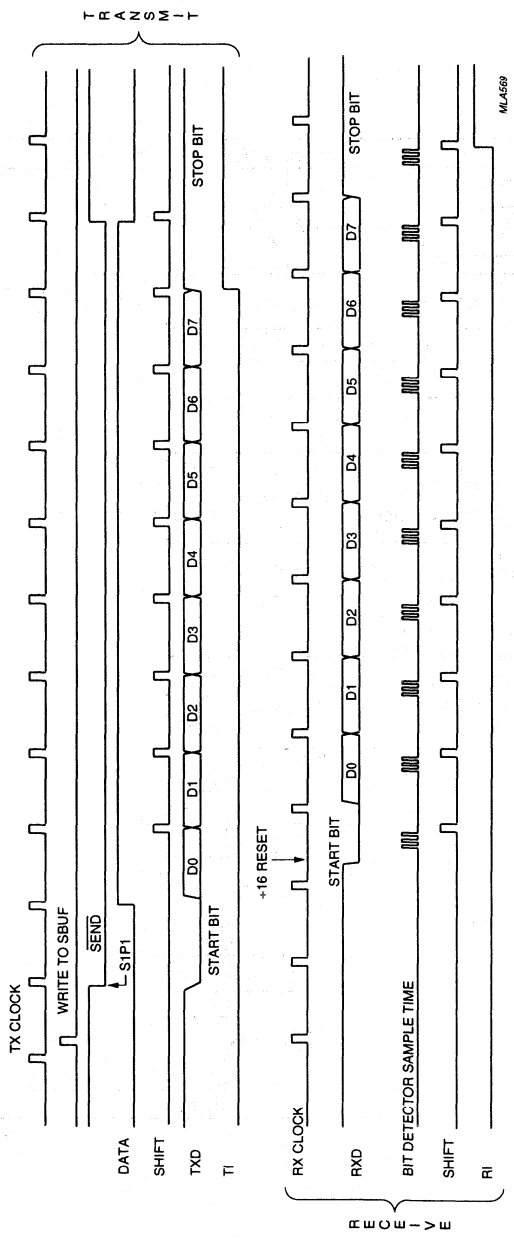


Fig.21 Serial port Mode 1 timing.

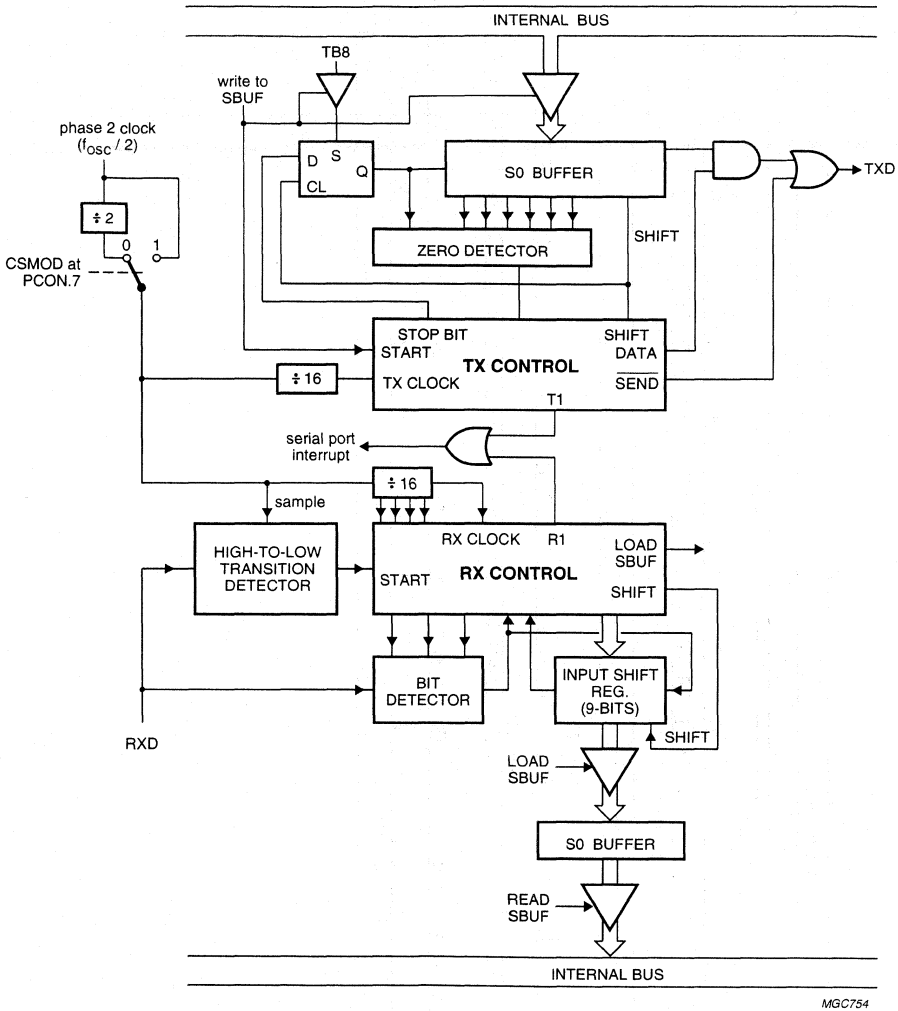


Fig.22 Serial port Mode 2.

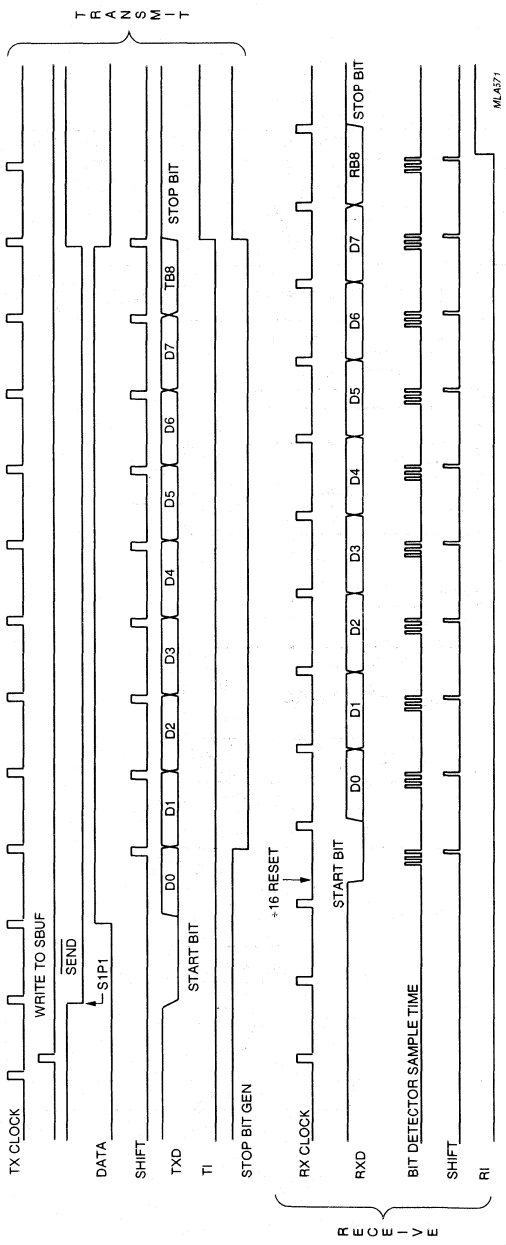


Fig.23 Serial port Mode 2 timing.

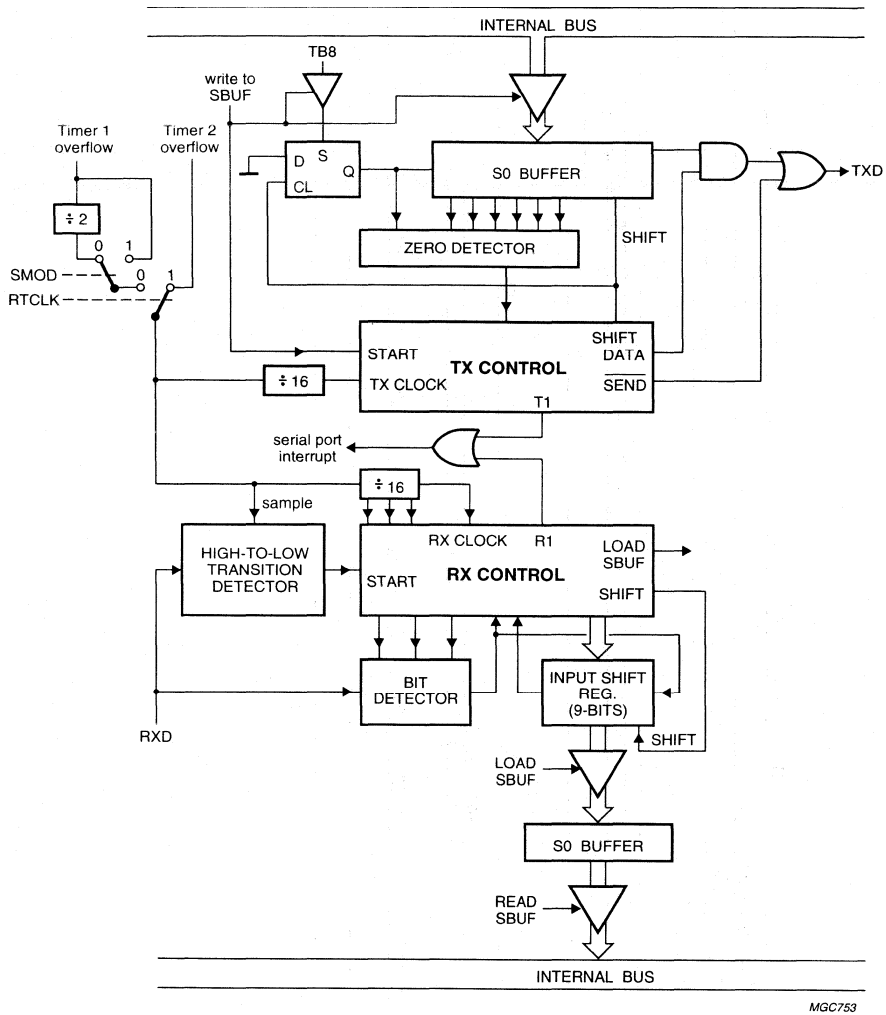


Fig.24 Serial port Mode 3.

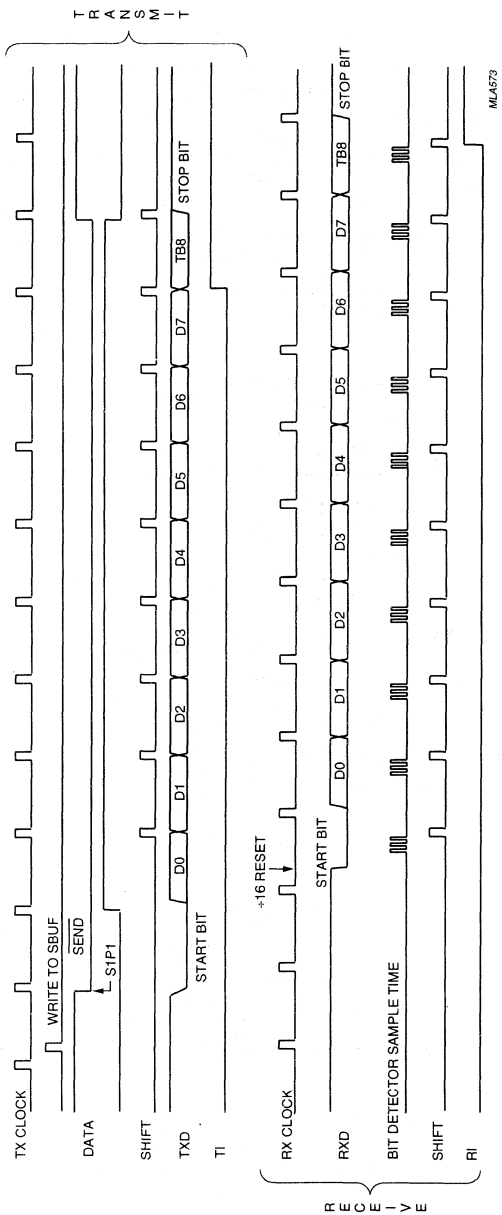


Fig.25 Serial port Mode 3 timing.

17 INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronously to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The P8xCL580 acknowledges interrupt requests from fifteen sources as follows:

- $\overline{INT0}$ to $\overline{INT8}$
- Timer 0, Timer 1 and Timer 2
- I^2C-bus serial I/O
- UART
- ADC.

Each interrupt vectors to a separate location in Program Memory for its service routine. Each source can be individually enabled or disabled by corresponding bits in the Interrupt Enable Registers (1EN0 and 1EN1). The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled. Figure 26 shows the interrupt system.

17.1 External interrupts $\overline{INT2}$ to $\overline{INT8}$

Port 1 lines serve an alternative purpose as seven additional interrupts $\overline{INT2}$ to $\overline{INT8}$. When enabled, each of these lines may wake-up the device from the Power-down mode. Using the Interrupt Polarity Register (IX1), each pin may be initialized to be either active HIGH or active LOW. IRQ1 is the Interrupt Request Flag Register. If the interrupt is enabled, each flag will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled.

A low-priority interrupt can be interrupted by a high-priority interrupt but not by another low-priority interrupt. A high-priority can not be interrupted by any other interrupt. If two interrupt requests of different priority levels are received simultaneously, the request having the highest priority level will be serviced. If interrupt requests of the same priority level are received simultaneously an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence (see Fig.26).

Port 1 interrupts are level sensitive. A Port 1 interrupt will be recognized when a level (HIGH or LOW depending on the Interrupt Polarity Register) on P1.n is held active for at least one machine cycle. The interrupt request is not serviced until the next machine cycle. Figure 27 shows the external interrupt system.

17.2 Interrupt priority

Each interrupt source can be set to either a high priority or to a low priority. If interrupts of the same priority are requested simultaneously, the processor will branch to the interrupt polled first, according to Table 34.

A low priority interrupt routine can only be interrupted by a high priority interrupt. A high priority interrupt routine can not be interrupted.

Table 34 shows the interrupt vectors in order of priority. The vector indicates the ROM location where the appropriate interrupt service routine starts.

Table 34 Interrupt vectors

SYMBOL[1]	VECTOR ADDRESS (HEX)	SOURCE
X0 (highest)	0003	External 0
S1	002B	I^2C port
X5	0053	External 5
T0	000B	Timer 0
T2	0033	Timer 2
X6	005B	External 6
X1	0013	External 1
X2	003B	External 2
X7	0063	External 7
T1	001B	Timer 1
X3	0043	External 3
X8	006B	External 8
SO	0023	UART
X4	004B	External 4
ADC (lowest)	0073	ADC

Note

1. X0 has the highest priority; ADC the lowest.

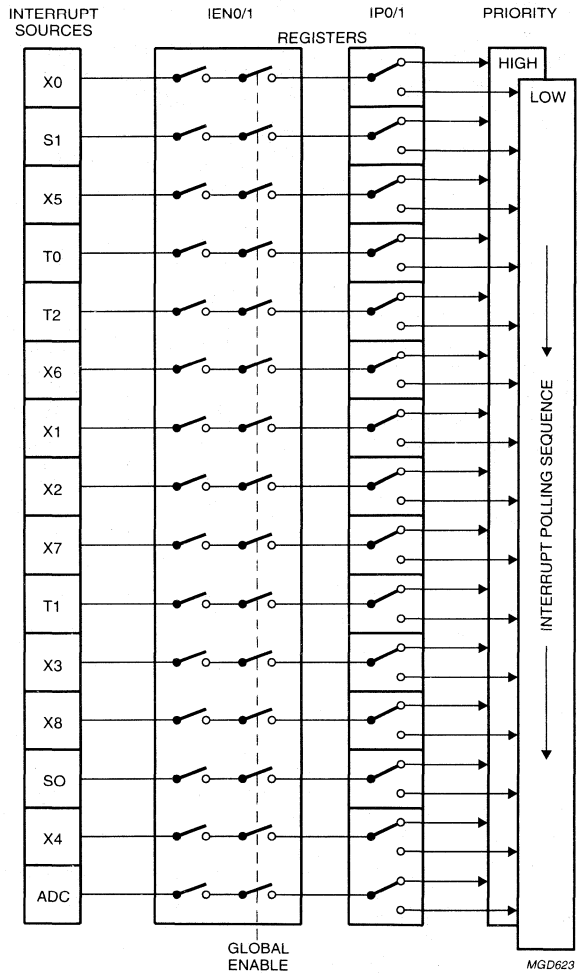


Fig.26 Interrupt system.

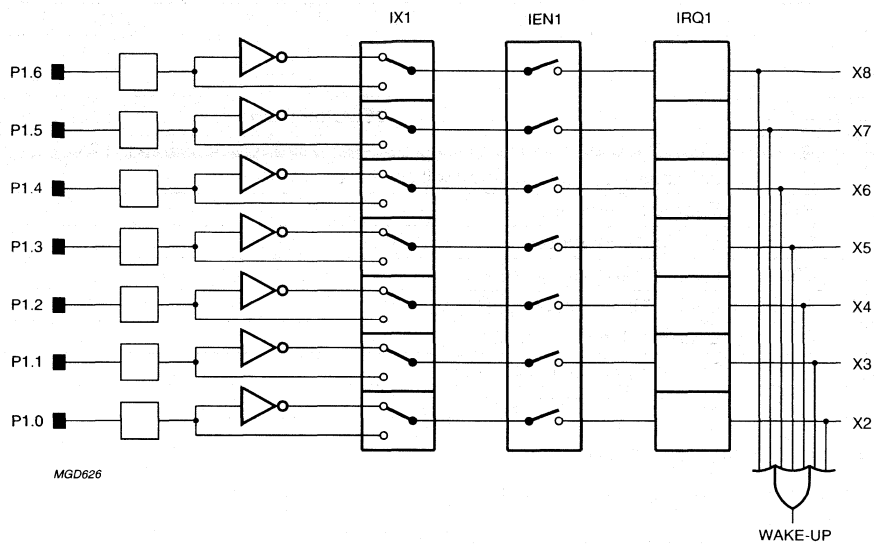


Fig.27 External interrupt configuration.

17.3 Interrupt related registers

The registers IEN0, IEN1, IP0, IP1, IX1 and IRQ1 are used in conjunction with the interrupt system.

Table 35 Special Function Registers related to the interrupt system

ADDRESS	REGISTER	DESCRIPTION
A8H	IEN0	Interrupt Enable Register
E8H	IEN1	Interrupt Enable Register ($\overline{INT2}$ to $\overline{INT8}$)
B8H	IP0	Interrupt Priority Register
F8H	IP1	Interrupt Priority Register ($\overline{INT2}$ to $\overline{INT8}$, ADC)
E9H	IX1	Interrupt Polarity Register
C0H	IRQ1	Interrupt Request Flag Register

17.3.1 Interrupt Enable Register (IEN0)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 36 Interrupt Enable Register (SFR address A8H)

7	6	5	4	3	2	1	0
EA	ET2	ES1	ES0	ET1	EX1	ET0	EX0

Table 37 Description of IEN0 bits

BIT	SYMBOL	DESCRIPTION
7	EA	General enable/disable control. If EA = 0, no interrupt is enabled. If EA = 1, any individually enabled interrupt will be accepted.
6	ET2	Enable T2 interrupt.
5	ES1	Enable I^2C interrupt.
4	ES0	Enable UART SIO interrupt.
3	ET1	Enable Timer 1 interrupt (T1).
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt (T0).
0	EX0	Enable external interrupt 0.

17.3.2 Interrupt Enable Register (IEN1)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 38 Interrupt Enable Register (SFR address E8H)

7	6	5	4	3	2	1	0
EAD	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Table 39 Description of IEN1 bits

BIT	SYMBOL	DESCRIPTION
7	EAD	Enable ADC interrupt.
6	EX8	Enable external interrupt 8.
5	EX7	Enable external interrupt 7.
4	EX7	Enable external interrupt 6.
3	EX5	Enable external interrupt 5.
2	EX4	Enable external interrupt 4.
1	EX3	Enable external interrupt 3.
0	EX2	Enable external interrupt 2.

17.3.3 Interrupt Priority Register (IP0)

Bit values: 0 = low priority; 1 = high priority.

Table 40 Interrupt Priority Register (SFR address B8H)

7	6	5	4	3	2	1	0
–	PT2	PS1	PS0	PT1	PX1	PT0	PX0

Table 41 Description of IP0 bits

BIT	SYMBOL	DESCRIPTION
7	–	Reserved.
6	PT2	Timer 2 interrupt priority level.
5	PS1	I^2C interrupt priority level.
4	PS0	UART SIO interrupt priority level.
3	PT1	Timer 1 interrupt priority level.
2	PX1	External interrupt 1 priority level.
1	PT0	Timer 0 interrupt priority level.
0	PX0	External interrupt 0 priority level.

17.3.4 Interrupt Priority Register (IP1)

Bit values: 0 = low priority; 1 = high priority.

Table 42 Interrupt Priority Register (SFR address F8H)

7	6	5	4	3	2	1	0
PADC	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Table 43 Description of IP1 bits

BIT	SYMBOL	DESCRIPTION
7	PADC	ADC interrupt priority level.
6	PX8	External interrupt 8 priority level.
5	PX7	External interrupt 7 priority level.
4	PX6	External interrupt 6 priority level.
3	PX5	External interrupt 5 priority level.
2	PX4	External interrupt 4 priority level.
1	PX3	External interrupt 3 priority level.
0	PX2	External interrupt 2 priority level.

17.3.5 Interrupt Polarity Register (IX1)

Writing either a logic 1 or logic 0 to any Interrupt Polarity Register bit sets the polarity level of the corresponding external interrupt to an active HIGH or active LOW respectively.

Table 44 Interrupt Polarity Register (SFR address E9H)

7	6	5	4	3	2	1	0
–	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Table 45 Description of IX1 bits

BIT	SYMBOL	DESCRIPTION
7	–	reserved
6	IL8	external interrupt 8 polarity level
5	IL7	external interrupt 7 polarity level
4	IL6	external interrupt 6 polarity level
3	IL5	external interrupt 5 polarity level
2	IL4	external interrupt 4 polarity level
1	IL3	external interrupt 3 polarity level
0	IL2	external interrupt 2 polarity level

17.3.6 Interrupt Request Flag Register (IRQ1)

Table 46 Interrupt Request Flag Register (SFR address C0H)

7	6	5	4	3	2	1	0
–	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Table 47 Description of IRQ1 bits

BIT	SYMBOL	DESCRIPTION
7	–	reserved
6	IQ8	external interrupt 8 request flag
5	IQ7	external interrupt 7 request flag
4	IQ6	external interrupt 6 request flag
3	IQ5	external interrupt 5 request flag
2	IQ4	external interrupt 4 request flag
1	IQ3	external interrupt 3 request flag
0	IQ2	external interrupt 2 request flag

18 OSCILLATOR CIRCUITRY

The on-chip oscillator circuitry of the P8xCL580 is a single-stage inverting amplifier biased by an internal feedback resistor. The oscillator circuit is shown in Fig.29. For operation as a standard quartz oscillator, no external components are needed, except for the 32 kHz option. When using external capacitors, ceramic resonators, coils and RC networks to drive the oscillator, five different configurations are supported (see Table 48 and Fig.28).

In the Power-down mode the oscillator is stopped and XTAL1 is pulled HIGH. The oscillator invertor is switched off to ensure no current will flow regardless of the voltage at XTAL1, for configurations (a), (b), (c), (d), (e) and (g) of Fig.28.

To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Fig.28(f). There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is buffered by a flip-flop.

Various oscillator options are provided for optimum on-chip oscillator performance; these are specified in Table 48 and shown in Fig.28. The required option should be stated when ordering.

Table 48 Oscillator options

OPTION	APPLICATION
Oscillator 1	For 32 kHz clock applications with external trimmer for frequency adjustment. A 4.7 MΩ bias resistor is needed for use in parallel with the crystal; see Fig.28(c).
Oscillator 2	Low-power, low-frequency operations using LC components; see Fig.28(e).
Oscillator 3	Medium frequency range applications.
Oscillator 4	High frequency range applications.
RC oscillator	RC oscillator configuration; see Figs 28(g) and 30.

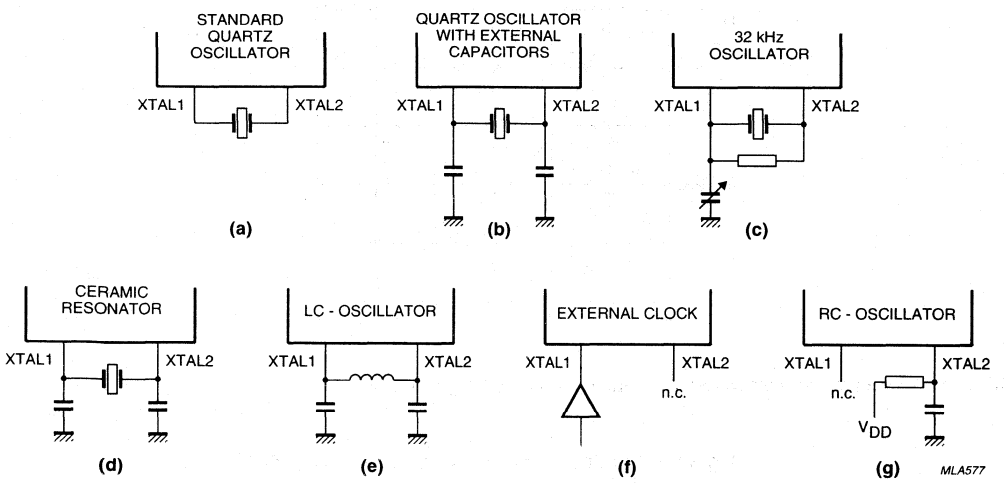


Fig.28 Oscillator configurations.

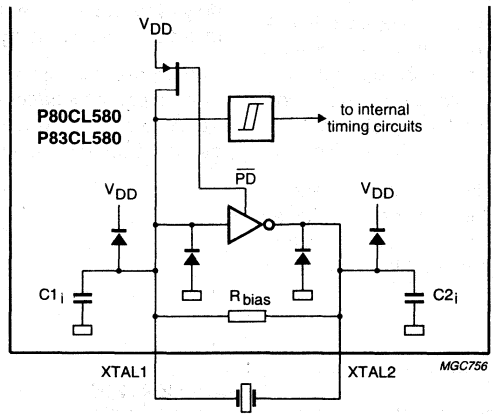
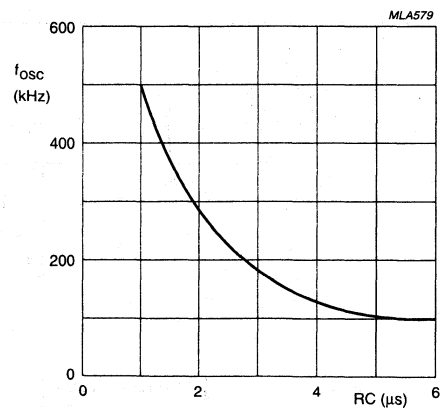


Fig.29 Standard oscillator.



RC oscillator frequency is externally adjustable; 100 kHz ≤ f_{osc} ≤ 500 kHz.

Fig.30 RC oscillator; frequency as a function of RC.

Table 49 Oscillator type selection guide

RESONATOR	FREQUENCY (MHz)	OPTION (see Table 48)	C1 EXT. (pF)		C2 EXT. (pF)		RESONATOR MAX. SERIES RESISTANCE
			MIN.	MAX.	MIN.	MAX.	
Quartz	0.032	Oscillator 1	0	0	5	15	15 kΩ[1]
	1.0		0	30	0	30	600 Ω
	3.58	Oscillator 2	0	15	0	15	100 Ω
	4.0		0	20	0	20	75 Ω
	6.0	Oscillator 3	0	10	0	10	60 Ω
	10.0		0	15	0	15	60 Ω
	12.0	Oscillator 4	0	10	0	10	40Ω
	16.0		0	15	0	15	20 Ω
PXE	0.455		40	50	40	50	10 Ω
	1.0		15	50	15	50	100 Ω
	3.58	Oscillator 2	0	40	0	40	10 Ω
	4.0		0	40	0	40	10 Ω
	6.0		0	20	0	20	5 Ω
	10.0	Oscillator 3	0	15	0	15	6 Ω
	12.0	Oscillator 4	10	40	10	40	6 Ω
LC		Oscillator 2	20	90	20	90	10 µH = 1 Ω 100 µH = 5 Ω 1 mH = 75 Ω

Note

1. 32 kHz quartz crystals with a series resistance >15 kΩ will reduce the guaranteed supply voltage range to 2.5 to 3.5 V.

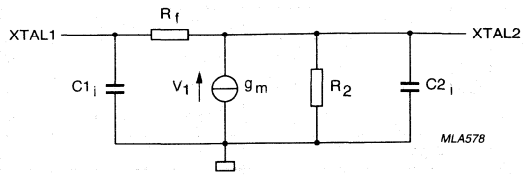


Fig.31 Equivalent circuit diagram.

Table 50 Oscillator equivalent circuit parameters.

The equivalent circuit data of the internal oscillator compares with that of matched crystals.

SYMBOL	PARAMETER	OPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
g_m	transconductance	Oscillator 1; 32 kHz	T_{amb} = +25 °C; V_{DD} = 4.5 V	–	15	–	µS
		Oscillator 2		200	600	1000	µS
		Oscillator 3		400	1500	4000	µS
		Oscillator 4		1000	4000	10000	µS
$C1_i$	input capacitance	Oscillator 1; 32 kHz		–	3.0	–	pF
		Oscillator 2		–	8.0	–	pF
		Oscillator 3		–	8.0	–	pF
		Oscillator 4		–	8.0	–	pF
$C2_i$	output capacitance	Oscillator 1; 32 kHz		–	23	–	pF
		Oscillator 2		–	8.0	–	pF
		Oscillator 3		–	8.0	–	pF
		Oscillator 4		–	8.0	–	pF
R2	output resistance	Oscillator 1; 32 kHz		–	3800	–	kΩ
		Oscillator 2		–	65	–	kΩ
		Oscillator 3		–	18	–	kΩ
		Oscillator 4		–	5.0	–	kΩ

19 RESET

To initialize the P8xCL580 a reset is performed by either of three methods:

- Applying an external signal to the RST pin
- Via Power-on-reset circuitry
- Watchdog Timer.

A reset leaves the internal registers as shown in Chapter 20. The reset state of the port pins is mask-programmable and can be defined by the user.

19.1 External reset using the RST pin

The reset input for the P8xCL580 is RST. A Schmitt trigger is used at the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle. A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. Port pins adopt their reset state immediately after the RST goes HIGH. During reset, ALE and $\overline{PSEN}$ are held HIGH.

The external reset is asynchronous to the internal clock. The RST pin is sampled during state 5, phase 2 of every machine cycle. After a HIGH is detected at the RST pin, an internal reset is repeated until RST goes LOW. The reset circuitry is also affected by the Watchdog timer; see Section 11.4. The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM contents are indeterminate.

19.2 Power-on-reset

The device contains on-chip circuitry which switches the port pins to the customer defined logic level as soon as V_{DD} exceeds 1.3 V; if the mask option 'ON' has been chosen. As soon as the minimum supply voltage is reached, the oscillator will start up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for a further 1536 oscillator periods. During that time the CPU is held in a reset state. A hysteresis of approximately 50 mV at a typical power-on switching level of 1.3 V will ensure correct operation (see Fig.34).

The on-chip Power-on reset circuitry can also be switched off via the mask option 'OFF'. This option reduces the Power-down current to typically 800 nA and can be chosen if external reset circuitry is used. For applications not requiring the internal reset, option 'OFF' should be chosen.

An automatic reset can be obtained by connecting the RST pin to V_{DD} via a 10 µF capacitor. At power-on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles. The Power-on-reset circuitry is shown in Fig.33.

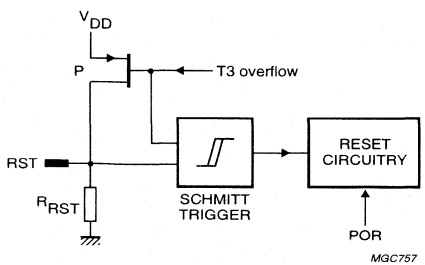


Fig.32 Reset configuration.

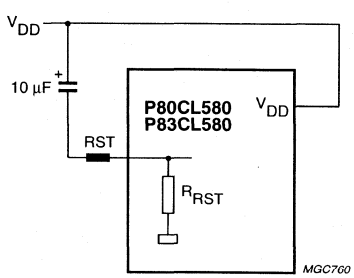


Fig.33 Recommended Power-on-reset circuitry

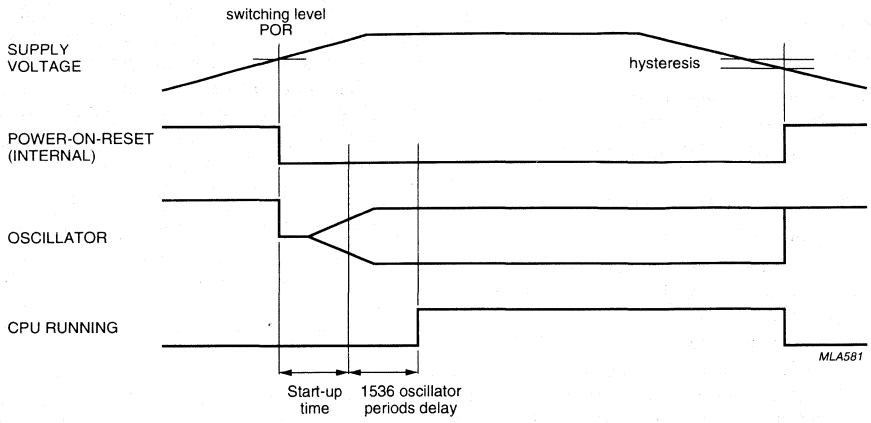


Fig.34 Power-on-reset switching level.

20 SPECIAL FUNCTION REGISTERS_OVERVIEW

The P8xCL580 has 40 SFRs available to the user.

ADDRESS (HEX)	NAME	RESET VALUE (B)	FUNCTION
FF	T3[1]	00000000	Watchdog Timer
FE	PWMP[1]	00000000	Prescaler Frequency Control Register
FC	PWM0[1]	00000000	Pulse Width Register 0
F8	IP1[1]	00000000	Interrupt Priority Register ($\overline{INT2}$ to $\overline{INT8}$, ADC)
F0	B[2]	00000000	B Register
E9	IX1[1]	00000000	Interrupt Polarity Register
E8	IEN1[1][2]	00000000	Interrupt Enable Register 1
E0	ACC[2]	00000000	Accumulator
DB	S1ADR[1]	00000000	I^2C-bus Slave Address Register
DA	S1DAT[1]	00000000	I^2C-bus Data Shift Register
D9	S1STA[1]	11111000	I^2C-bus Serial Status Register
D8	S1CON[1][2]	00000000	I^2C-bus Serial Control Register
D0	PSW[2]	00000000	Program Status Word
CD	TH2[1]	00000000	Timer 2 High byte
CC	TL2[1]	00000000	Timer 2 Low byte
CB	RCAP2H[1]	00000000	Timer 2 Reload/Capture Register High byte
CA	RCAP2L[1]	00000000	Timer 2 Reload/Capture Register Low byte
C8	T2CON[1][2]	00000000	Timer/Counter 2 Control Register
C5	ADCH[1]	11111111	ADC Result Register
C4	ADCON[1]	X0000000	ADC Control Register
C1	P4[1]	XXXXXXXX[3]	Digital I/O Port Register 4
C0	IRQ1[1][2]	00000000	Interrupt Request Flag Register

ADDRESS (HEX)	NAME	RESET VALUE (B)	FUNCTION
B8	IP0[2]	X0000000	Interrupt Priority Register 0
B0	P3[2]	XXXXXXXX[3]	Digital I/O Port Register 3
A8	IEN0[2]	00000000	Interrupt Enable Register
A0	P2[2]	XXXXXXXX[3]	Digital I/O Port Register 2
99	S0BUF	XXXXXXXX	Serial Data Buffer Register 0
98	S0CON[2]	00000000	Serial Port Control Register 0
90	P1[2]	XXXXXXXX[3]	Digital I/O Port Register 1
8D	TH1	00000000	Timer 1 High byte
8C	TH0	00000000	Timer 0 High byte
8B	TL1	00000000	Timer 1 Low byte
8A	TL0	00000000	Timer 0 Low byte
89	TMOD	00000000	Timer 0 and 1 Mode Control Register
88	TCON[2]	00000000	Timer 0 and 1 Control/External Interrupt Control Register
87	PCON	00XX0000	Power Control Register
83	DPH	00000000	Data Pointer High byte
82	DPL	00000000	Data Pointer Low byte
81	SP	00000111	Stack Pointer
80	P0[2]	XXXXXXXX[3]	Digital I/O Port Register 0

Notes

1. P8xCL580 specific SFRs.
2. Bit addressable register.
3. Port reset state determined by the customer.

21 INSTRUCTION SET

The P8xCL580 uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes byte efficiency and execution speed. Assigned opcodes add new high-power operation and permit new addressing modes. The instruction set consists of 49 single-byte, 46 two-byte and 16 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. Multiply and divide instructions execute in 4 μs.

For the description of the **Data Addressing modes** and **Hexadecimal opcode cross-reference** see Table 55.

Table 51 Instruction set description: Arithmetic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A and B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

Table 52 Instruction set description: Logic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

Table 53 Instruction set description: Data transfer

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct (note 1)	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

1. MOV A,ACC is not permitted.

Table 54 Instruction set description: Boolean variable manipulation, Program and machine control

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	•1
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	♦1
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immediate to register and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

Table 55 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data 16	16-bit constant included as bytes 2 and 3 of instruction.
bit	Direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes Program Memory address space.
addr11	111-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F.
•	1, 3, 5, 7, 9, B, D, F.
♦	0, 2, 4, 6, 8, A, C, E.

Table 56 Instruction map

First hexadecimal character of opcode ← **Second hexadecimal character of opcode** →

↓	0	1	2	3	4	5	6 | 7	8 | 9 | A | B | C | D | E | F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri: 0 | 1	INC Rr: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri: 0 | 1	DEC Rr: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri: 0 | 1	ADD A,Rr: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri: 0 | 1	ADDC A,Rr: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri: 0 | 1	ORL A,Rr: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri: 0 | 1	ANL A,Rr: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri: 0 | 1	XRL A,Rr: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data: 0 | 1	MOV Rr,#data: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri: 0 | 1	MOV direct,Rr: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
9	MOV DTPR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri: 0 | 1	SUB A,Rr: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
A	ORL C,/bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB		MOV @Ri,direct: 0 | 1	MOV Rr,direct: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel: 0 | 1	CJNE Rr,#data,rel: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri: 0 | 1	XCH A,Rr: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri: 0 | 1	DJNZ Rr,rel: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
E	MOVX A,@DTPR	AJMP addr11	MOVX A,@Ri: 0 | 1		CLR A	MOV A,direct (1)	MOV A,@Ri: 0 | 1	MOV A,Rr: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
F	MOVX @DTPR,A	ACALL addr11	MOVX @Ri,A: 0 | 1		CPL A	MOV direct,A	MOV @Ri,A: 0 | 1	MOV Rr,A: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7

Note

1. MOV A, ACC is not a valid instruction.

22 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_I	input voltage on any pin with respect to ground (V_{SS})	−0.5	V_{DD} + 0.5	V
I_I, I_O	DC current on any input or output	–	5.0	mA
P_{tot}	total power dissipation	–	300	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C
T_j	operating junction temperature	–	+125	°C

23 DC CHARACTERISTICS

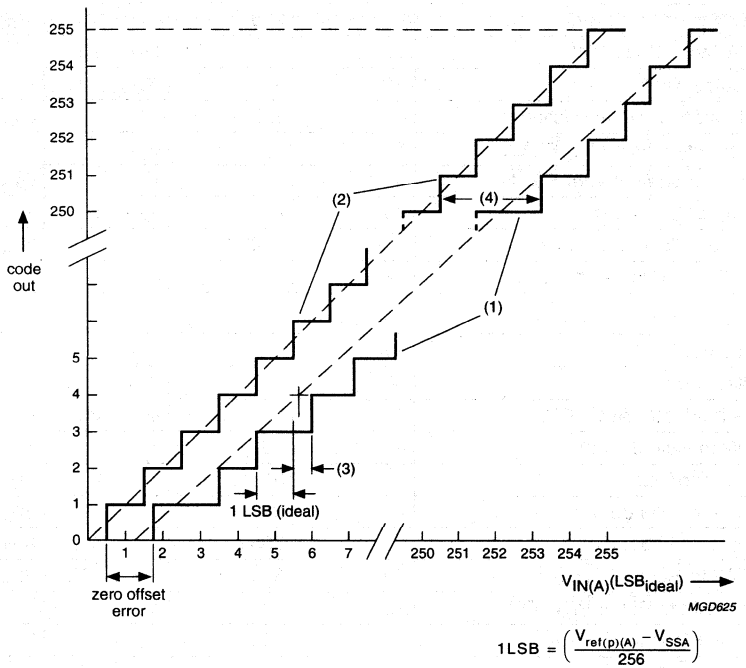
V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +55 °C; see notes 1 and 2; all voltages are with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.5	–	6.0	V
	RAM retention voltage in Power-down mode		1.0	–	6.0	V
I_{DD}	supply current operating	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 3	–	–	27.0	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 3	–	–	5.0	mA
$I_{DD(ID)}$	supply current Idle mode	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 4	–	–	10.0	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 4	–	–	3.0	mA
$I_{DD(PD)}$	Power-down current	V_{DD} = 1.8 V; T_{amb} = 25°C; note 5	–	–	10	µA
Inputs (note 6)						
V_{IL}	LOW level input voltage		V_{SS}	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
I_{LI}	input leakage current (Port 0; $\overline{EA}$)	V_{SS} < V_I < V_{DD}	–	–	±10	µA
Outputs						
I_{OL}	LOW level output current (except SDA; SCL)	V_{DD} = 5 V; V_{OL} = 0.4 V	1.6	–	–	mA
		V_{DD} = 2.5 V; V_{OL} = 0.4 V	0.7	–	–	mA
	LOW level output current SDA; SCL	V_{DD} = 5 V; V_{OL} = 0.4 V	3.0	–	–	mA
	LOW level output current $\overline{PWM0}$	V_{DD} = 5 V; V_{OL} = 0.4 V	3.0	–	–	mA
		V_{DD} = 2.5 V; V_{OL} = 0.4 V	1.6	–	–	mA
I_{OH}	HIGH level output current $\overline{PWM0}$	V_{DD} = 5 V; V_{OH} = V_{DD} − 0.4 V	−3.2	–	–	mA
		V_{DD} = 2.5 V; V_{OH} = V_{DD} − 0.4 V	−1.6	–	–	mA
I_{OH}	HIGH level output current (push-pull options only)	V_{DD} = 5 V; V_{OH} = V_{DD} − 0.4 V	−1.6	–	–	mA
		V_{DD} = 2.5 V; V_{OH} = V_{DD} − 0.4 V	−0.7	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	input current logic 0	V_{DD} = 5 V; V_{IN} = 0.4 V	–	–	–100	µA
		V_{DD} = 2.5 V; V_{IN} = 0.4 V	–	–	–50	µA
I_{ITL}	input current logic 0; HIGH-to-LOW transition	V_{DD} = 5 V; V_{IN} = 0.5V_{DD}	–	–	–1.0	mA
		V_{DD} = 2.5 V; V_{IN} = 0.5V_{DD}	–	–	–500	µA
R_{RST}	RST pull-down resistor		10	–	200	kΩ
Analog inputs (note 7)						
$V_{IN(A)}$	analog input voltage		V_{SSA}	–	V_{DD}	mA
$V_{ref(p)(A)}$	reference voltage		2.7	–	V_{DD}	mA
R_{ref}	resistance between $V_{ref(p)(A)}$ and V_{SSA}		25	–	100	kΩ
C_{AIN}	analog on-chip input capacitance		–	3	–	pF
A_e	absolute error (note 8)		–	–	±1	LSB
OS_e	zero-offset error (note 9)		–	–	±1	LSB
DL_e	differential non-linearity (note 10)		–	–	±1	LSB
M_{ctc}	channel-to-channel matching (note 11)		–	–	±½	LSB

Notes to the DC characteristics

1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3 pins when these make a HIGH-to-LOW transition during bus operations. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make HIGH-to-LOW transitions during bus operations. In the most adverse conditions (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such events it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger strobe input.
2. Capacitive loading on Ports 0 and 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9V_{DD} specification when the address bits are stabilizing.
3. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{DD}.
4. The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{DD}.
5. The power-down current is measured with all output pins disconnected; XTAL1 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification. Therefore, an input voltage below 0.3V_{DD} will be recognized as a logic 0 and an input voltage above 0.7V_{DD} will be recognized as a logic 1.
7. V_{DD} = 2.7 to 6 V; V_{SS} = 0 V; V_{SSA} = 0 V; $V_{ref(p)(A)} = V_{DD}$; T_{amb} = –40 to +85 °C, unless otherwise specified. $f_{xtal(min)}$ = 250 kHz.
8. Absolute error: the maximum difference between actual and ideal code transitions. Absolute error accounts for all deviations of an actual converter from an ideal converter.
9. Zero-offset error: the difference between the actual and ideal input voltage corresponding to the first actual code transition.
10. Differential non-linearity: the difference between the actual and ideal code widths.
11. Channel-to-channel matching: the difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions. Not tested, but verified on sampling basis.



(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential non-linearity (DL_e).
(4) Absolute error.

Fig.35 Analog-to-digital conversion characteristics.

24 AC CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; C_L = 50 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 40 pF for all other outputs unless specified; $t_{CLK} = 1/f_{CLK}$.

SYMBOL	PARAMETER	f_{osc} = 12 MHz		f_{osc} = VARIABLE		UNIT
		MIN.	MAX.	MIN.	MAX.	
Program Memory (Fig.36)						
t_{LHLL}	ALE pulse width	127	–	$2t_{CLK} - 40$	–	ns
t_{AVLL}	address valid to ALE LOW	43	–	$t_{CLK} - 40$	–	ns
t_{LLAX}	address hold after ALE LOW	48	–	$t_{CLK} - 35$	–	ns
t_{LLIV}	ALE LOW to valid instruction in	–	233	–	$4t_{CLK} - 100$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW	58	–	$t_{CLK} - 25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLK} - 35$	–	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in	–	125	–	$3t_{CLK} - 125$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$	–	63	–	$t_{CLK} - 20$	ns
t_{PXAV}	$\overline{PSEN}$ to address valid	75	–	$t_{CLK} - 8$	–	ns
t_{AVIV}	address to valid instruction in	–	302	–	$5t_{CLK} - 115$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float	12	–	0	–	ns
External Data Memory (Figs 37 and 38)						
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLK} - 100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLK} - 100$	–	ns
t_{LLAX}	address hold after ALE LOW	48	–	$t_{CLK} - 35$	–	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in	–	150	–	$5t_{CLK} - 165$	ns
t_{RHDZ}	data float after $\overline{RD}$	–	97	–	$2t_{CLK} - 70$	ns
t_{LLDV}	ALE LOW to valid data in	–	517		$8t_{CLK} - 150$	ns
t_{AVDV}	address to valid data in	–	585	–	$9t_{CLK} - 165$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	200	300	$3t_{CLK} - 50$	$3t_{CLK} + 50$	ns
t_{AVWL}	address valid to $\overline{RD}$ or $\overline{WR}$ LOW	203	–	4	–	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	43	123	$t_{CLK} - 40$	$t_{CLK} + 40$	ns
t_{QVWX}	data valid to $\overline{WR}$ transition	23	–	$t_{CLK} - 60$	–	ns
t_{QVWH}	data valid time $\overline{WR}$ HIGH	433	–	$7t_{CLK} - 150$	–	ns
t_{WHQX}	data hold after $\overline{WR}$	33	–	$t_{CLK} - 50$	–	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float	–	12	–	12	ns

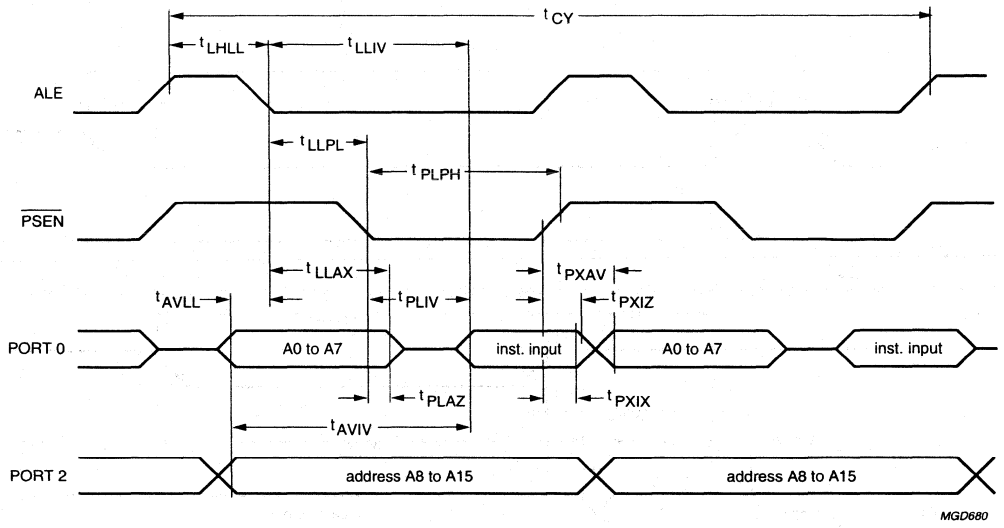


Fig.36 Read from Program Memory.

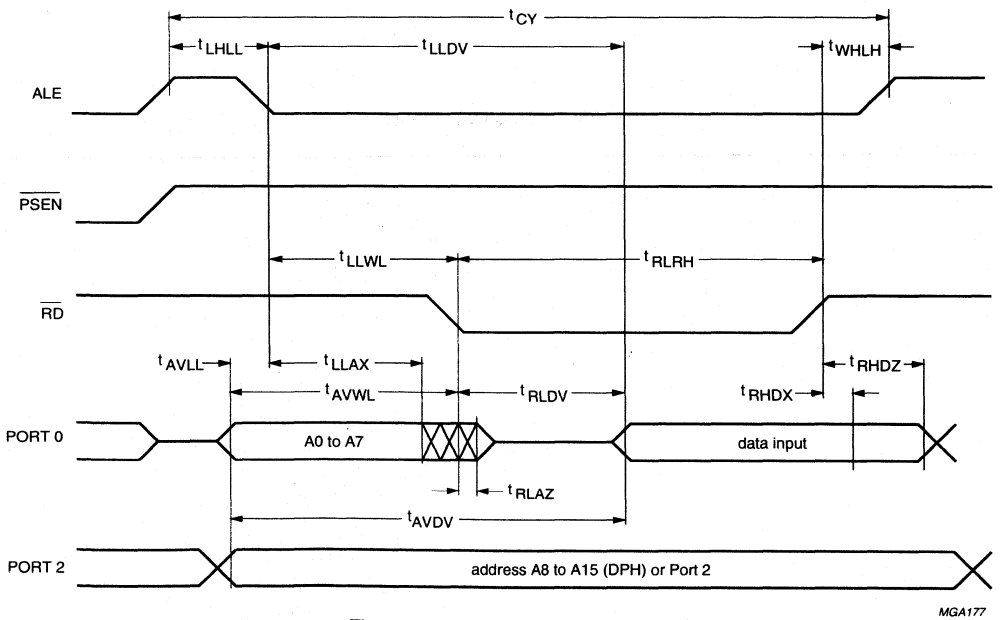


Fig.37 Read from Data Memory.

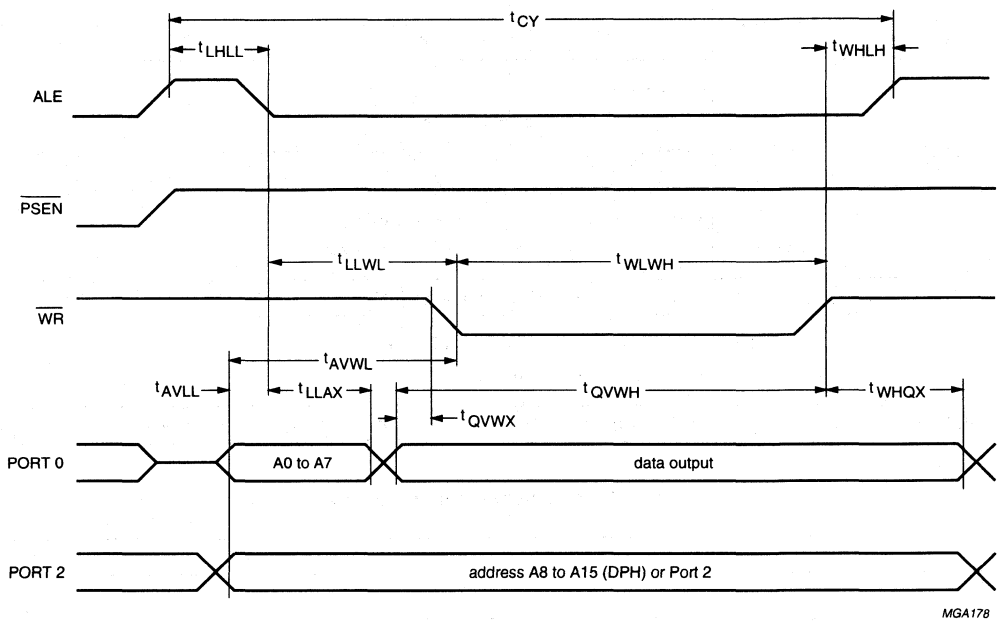


Fig.38 Write to Data Memory.

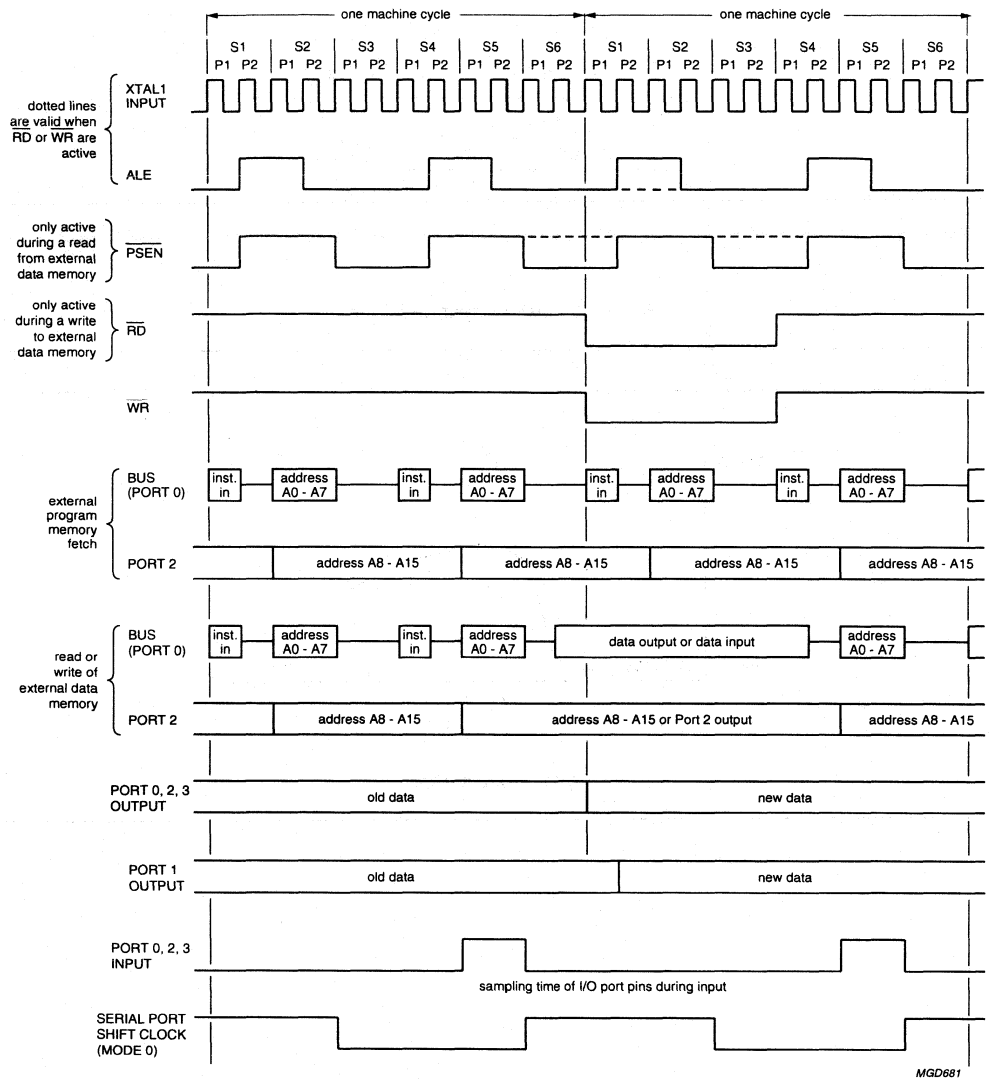


Fig.39 Instruction cycle timing.

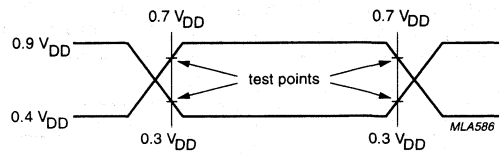


Fig.40 AC testing input waveform.

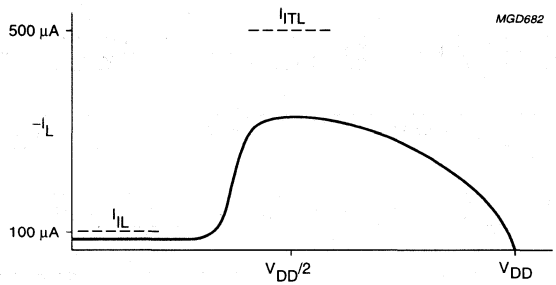
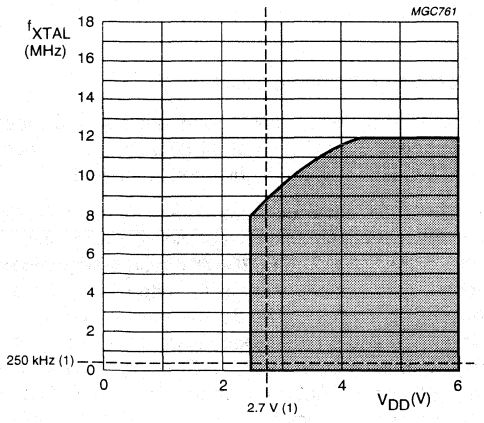


Fig.41 Input current.



(1) The area above the dotted lines give the ADC operating area.

Fig.42 Frequency operating range.

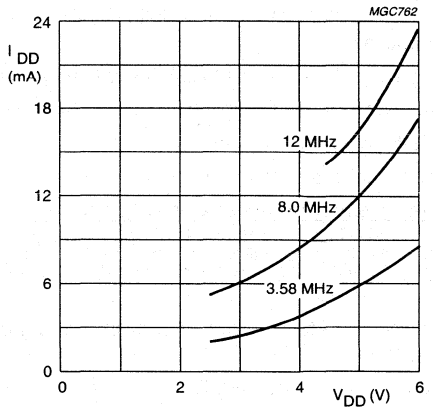


Fig.43 Typical operating current vs frequency and V_{DD}, T_{amb} = 25 °C, oscillator option OSC3.

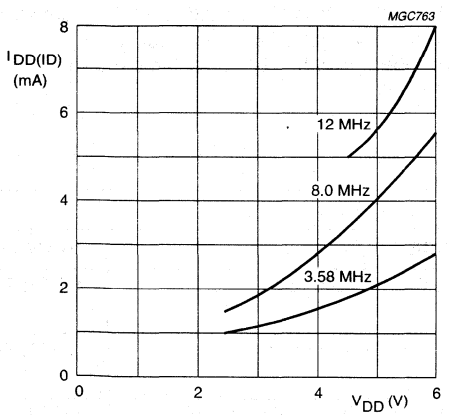


Fig.44 Typical Idle current vs frequency and V_{DD}, T_{amb} = 25 °C, oscillator option OSC3.

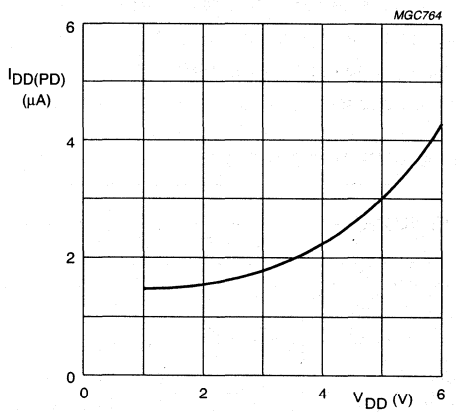


Fig.45 Typical Power-down current vs V_{DD}, T_{amb} = 25 °C.

1 FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a 40 lead DIP or 44 lead QFP package
- 16 kbytes ROM, expandable externally to 64 kbytes
- 256 bytes RAM, expandable externally to 64 kbytes
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- External memory expandable up to 128 kbytes external ROM up to 64 kbytes and/or RAM up to 64 kbytes
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector interrupt structure with two priority levels
- Full duplex serial port (UART)
- I^2C-bus interface for serial transfer on two lines
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four 8 byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- Power-down and Idle modes
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8 to 6.0 V
- Frequency range of DC to 12 MHz
- Very low current consumption
- Operating temperature:
  - 83CL781: –40 to +85 °C
  - 83CL782: –25 to +55 °C.

2 GENERAL DESCRIPTION

The term P83CL781 is used throughout this data sheet to refer to both the P83CL781 and P83CL782; differences between the devices are highlighted in the text.

The P83CL781 is manufactured in an advanced CMOS technology. The instruction set of the P83CL781 is based on that of the 8051. The P83CL781 is an 8-bit general purpose microcontroller especially suited for cordless telephone applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the P85CL781 (Piggy-back version) with 256 bytes of RAM is recommended. The P83CL781 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The P83CL781 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

The P83CL782 is a faster version of the P83CL781 and operates at a maximum frequency of 12 MHz at $V_{DD} \geq 3.1$ V.

This data sheet details the specific properties of the P83CL781; for details of the P83CL781 core and all the I^2C-bus functions see *"Data Handbook IC20"*. This handbook may be ordered using the code 9398 181 30011.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL781HFP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
P83CL782HDP			
P83CL781HFH	QFP44[1]	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1
P83CL782HDH			
P83CL781HFH	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
P83CL781HDH			

Note

1. When using IR reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

4 BLOCK DIAGRAM

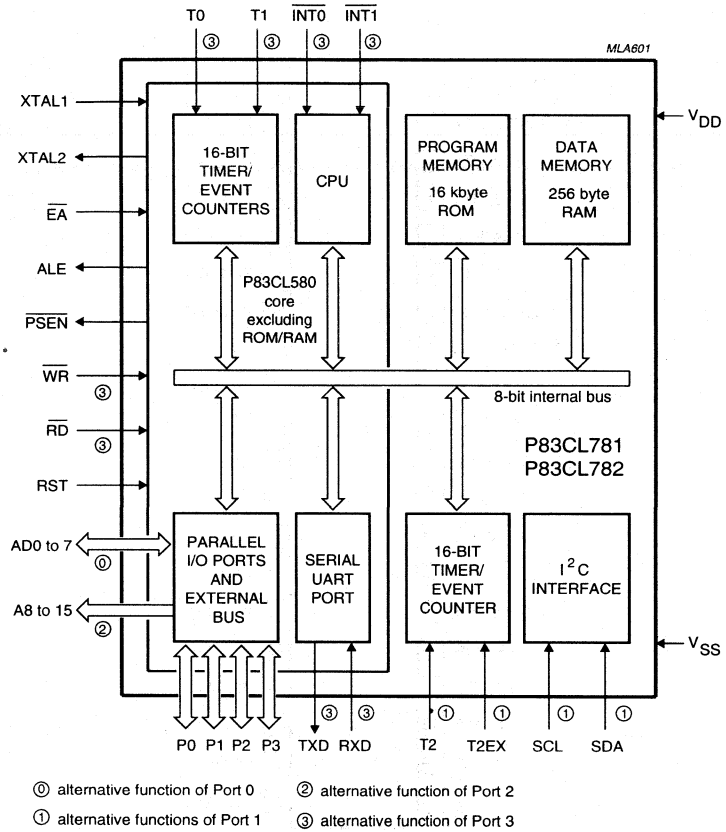


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

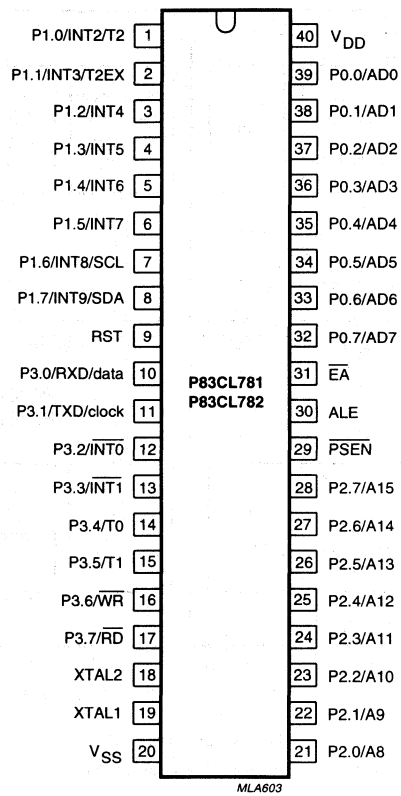


Fig.2 Pin configuration for DIP package.

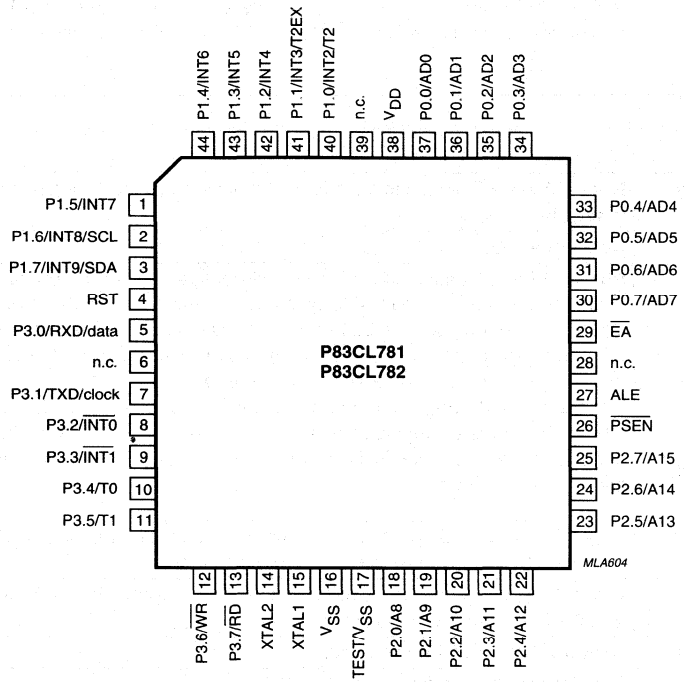


Fig.3 Pin configuration for QFP packages.

5.2 Pin description

Table 1 QFP packages (SOT205 and SOT307)

SYMBOL	PIN	DESCRIPTION
P1.0/INT2/T2	40	**Port 1:** 8-bit bidirectional I/O port with alternative functions. Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}) due to the internal pull-ups. Port 1 output buffers can sink/source 4 LS TTL loads. Port 1 also serves the alternative functions INT2 to INT9 and Timer T2 external input.
P1.1/INT3/T2EX	41	
P1.2/INT4	42	
P1.3/INT5	43	
P1.4/INT6	44	
P1.5/INT7	1	
P1.6/INT8/SCL	2	
P1.7/INT9//SDA	3	
RST	4	**Reset:** A HIGH level on this pin for two machine cycles while the oscillator is running, resets the device.
n.c.	6	Not connected.
P3.0/RXD/data	5	**Port 3:** 8-bit bidirectional I/O port with alternative functions. Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs. As inputs, port pins that are externally pulled LOW will source current (I_{IL}) due to the internal pull-ups. Port 3 output buffers can sink/source 4 LS TTL loads. RXD/data is the serial port receiver data input (asynchronous) or data I/O (synchronous). TXD/clock is the serial port transmitter data output (asynchronous) or clock output (synchronous). $\overline{INT0}$ and $\overline{INT1}$ are external interrupt lines. T0 and T1 are external inputs for Timer 0 and Timer 1 respectively. $\overline{WR}$ is the external memory write strobe and $\overline{RD}$ is the external memory read strobe.
P3.1/TXD/clock	7	
P3.2/$\overline{INT0}$	8	
P3.3/$\overline{INT1}$	9	
P3.4/T0	10	
P3.5/T1	11	
P3.6/$\overline{WR}$	12	
P3.7/$\overline{RD}$	13	
XTAL2	14	**Crystal Output:** Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used.
XTAL1	15	**Crystal Input:** Input to the inverting amplifier that forms the oscillator, also the input for an externally generated clock source.
V_{SS}	16	**Ground:** Circuit ground potential.
TEST/V_{SS}	17	**Test Input:** Must be connected to V_{SS} or left open.
P2.0/A8	18	**Port 2:** 8-bit bidirectional I/O port with alternative functions. Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs. Port 2 output buffers can sink/source 4 LS TTL loads. Port 2 emits the high order address byte during accesses to external memory that use 16-bit addresses (MOVX@DPTR). In this application it uses the strong internal pull-ups when emitting logic 1's. During accesses to external memory that use 8-bit addresses (MOVX@Ri), Port 2 emits the contents of the P2 Special Function Register.
P2.1/A9	19	
P2.2/A10	20	
P2.3/A11	21	
P2.4/A12	22	
P2.5/A13	23	
P2.6/A14	24	
P2.7/A15	25	

SYMBOL	PIN	DESCRIPTION
$\overline{PSEN}$	26	**Program Store Enable:** Read strobe to external program memory. When executing code out of external program memory, $\overline{PSEN}$ is activated twice each machine cycle. However, during each access to external data memory two $\overline{PSEN}$ activations are skipped.
ALE	27	**Address Latch Enable:** Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods and may be used for external timing or clocking purposes.
n.c.	28	Not connected.
$\overline{EA}$	29	**External Access:** When $\overline{EA}$ is held HIGH, the CPU executes out of the internal program memory (unless the Program Counter exceeds 3FFFH). When $\overline{EA}$ is held LOW, the CPU executes out of external program memory regardless of the value of the program counter.
P0.7/AD7	30	**Port 0:** 8-bit open drain bidirectional I/O port with alternative functions. P0.7 to P0.0 provide the 8-bit I/O port. As an open-drain output port it can sink/source 8 LS TTL loads. Port 0 pins that have logic 1s written to them float, and in this state will function as high-impedance inputs. AD7 to AD0 provide the multiplexed low-order address and data bus during accesses to external memory. In this application it uses the strong internal pull-ups when emitting logic 1s.
P0.6/AD6	31	
P0.5/AD5	32	
P0.4/AD4	33	
P0.3/AD3	34	
P0.2/AD2	35	
P0.1/AD1	36	
P0.0/AD0	37	
V_{DD}	38	**Power supply**
n.c.	39	Not connected.

6 FUNCTIONAL DESCRIPTION

6.1 General

The P83CL781 is a stand-alone high-performance CMOS microcontroller designed for use in real-time applications such as instrumentation, industrial control, intelligent computer peripherals and consumer products. The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 kbytes of program memory and/or up to 64 kbytes of data storage.

The P83CL781 contains a non-volatile 16 kbyte read-only program memory; a static 256 byte read/write data memory; 32 I/O lines; three 16-bit timer/event counters; a fifteen-source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit.

The device has two software selectable modes of reduced activity for power reduction; Idle and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial I/O and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

Two serial interfaces are provided on-chip; a standard UART serial interface and an I^2C-bus serial interface. The I^2C-bus serial interface has byte orientated master and slave functions allowing communication with the whole family of I^2C-bus compatible devices.

6.2 CPU timing

A machine cycle consists of a sequence of 6 states. Each state lasts for two oscillator periods, thus a machine cycle takes 12 oscillator periods or 1 μs if the oscillator frequency is 12 MHz.

6.3 Memory organization

The P83CL781 has a 16 kbyte Program Memory (ROM) plus 256 bytes of Data Memory (RAM) on-chip. The device has separate address spaces for Program and Data Memory (see Fig.4). Using Ports P0 and P2, the P83CL781 can address up to 64 kbytes of external memory. The CPU generates both read ($\overline{RD}$) and write ($\overline{WR}$) signals for external Data Memory accesses, and the read strobe ($\overline{PSEN}$) for external Program Memory.

6.3.1 Program memory

The P83CL781 contains 16 kbytes of internal ROM. After reset the CPU begins execution at location 0000H. The lower 16 kbytes of Program Memory can be implemented in either on-chip ROM or external memory. If the $\overline{EA}$ pin is strapped to V_{DD}, then program memory fetches from addresses 0000H through to 3FFFH are directed to the internal ROM. Fetches from addresses 4000H through to FFFFH are directed to external ROM. Program Counter values greater than 3FFFH are automatically addressed to external memory regardless of the state of the $\overline{EA}$ pin.

6.3.2 Data memory

The P83CL781 contains 256 bytes of internal RAM and 34 Special Function Registers (SFRs). Figure 4 shows the internal Data Memory space divided into the lower 128 bytes the upper 128 bytes and the SFR space. Internal RAM locations 0 to 27 are directly and indirectly addressable. Internal RAM locations 128 to 255 are only indirectly addressable. The Special Function Register locations 128 to 255 bytes are only directly addressable.

6.3.3 Special Function Registers

The upper 128 bytes are the address locations of the Special Function Registers. Figures 6 and 7 show the Special Function Registers space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 addressable locations in the SFR address space (SFRs with addresses divisible by eight).

6.4 Addressing

The P83CL781 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect.

The first three methods can be used for addressing destination operands. Most instructions have a 'destination/source' field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register Direct or Register-Indirect
- 256 bytes of internal data RAM through Direct or Register-Indirect
- Special Function Registers through Direct
- External data memory through Register-Indirect
- Program memory look-up tables through Base-Register plus Index-Register-Indirect.

The P83CL781 is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers, Arithmetic Logic Unit and external data bus are all 8-bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.

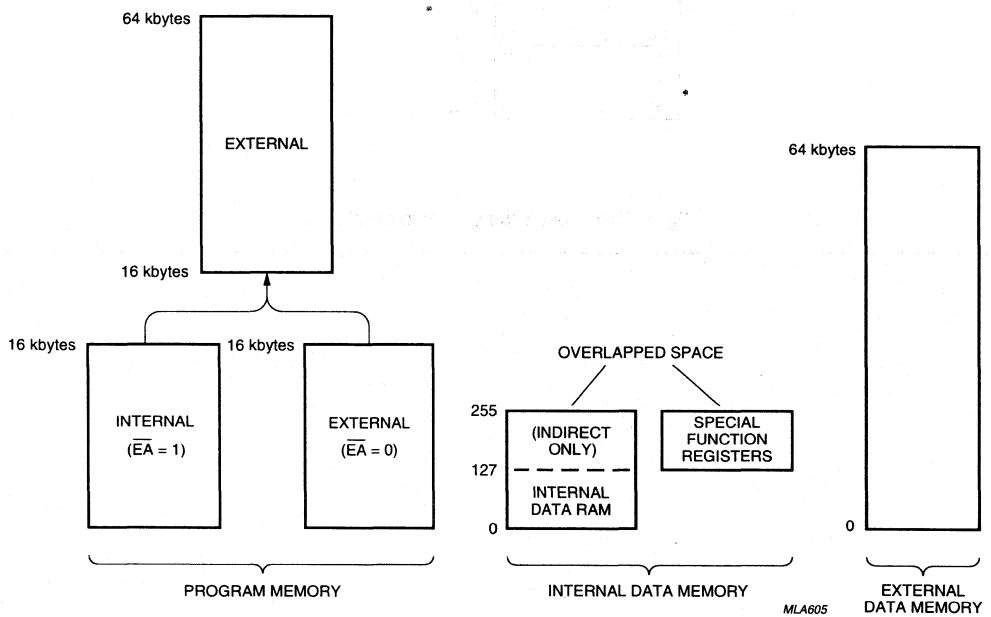


Fig.4 Memory map.

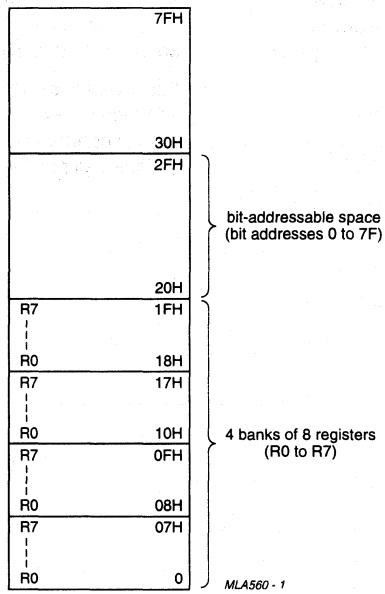


Fig.5 The lower 128 bytes of internal RAM.

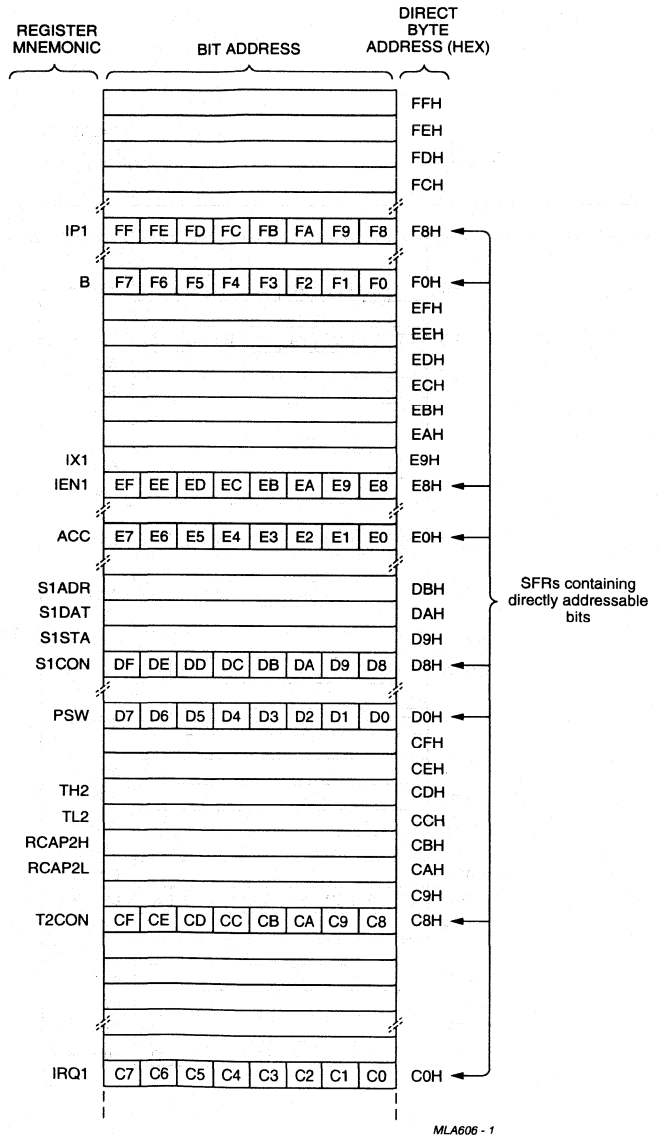


Fig.6 Special Function Register memory map (continued in Fig.7).

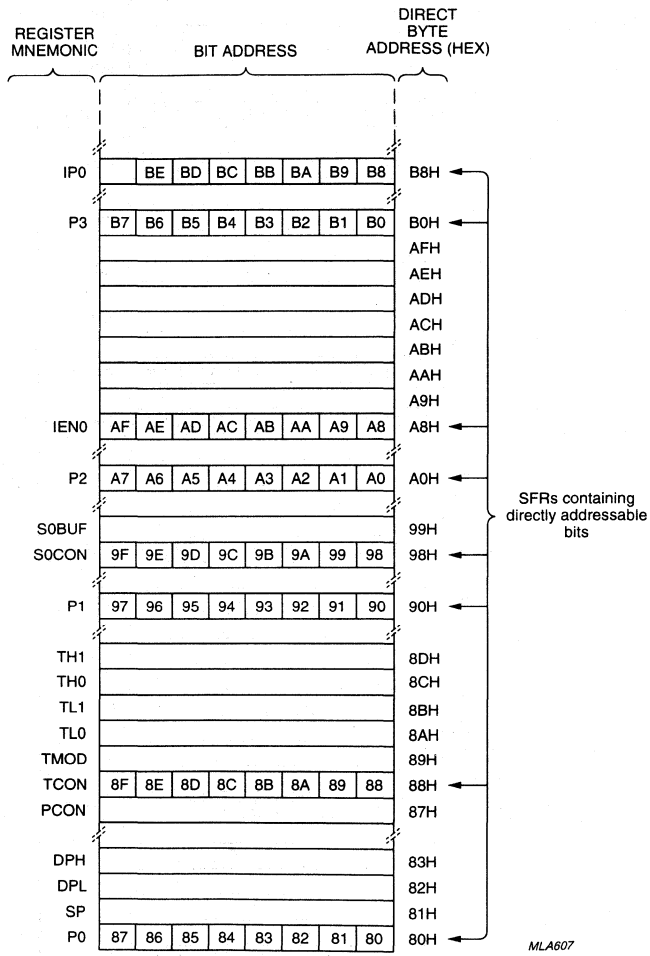


Fig.7 Special Function Register memory map (continued from Fig.6).

6.5 I/O facilities

6.5.1 PORTS

The P83CL781 has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8-bit addressable ports. Ports 0, 1, 2 and 3 perform the following alternative functions:

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Used for a number of special functions:

- Provides the inputs for the external interrupts INT2 to INT9
- External counter/capture of Timer 2
- SCL and SDA for the I^2C-bus interface.

Port 2 Provides the high-order address bus when expanding the device with external program memory and/or external data memory.

Port 3 Pins can be configured individually to provide:

- External interrupt request inputs
- Counter inputs
- Serial port receiver input and transmitter output (UART)
- Control signals to read and write to external memories.

To enable a Port 3 pin alternative function, the Port 3 bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. Ports 1, 2 and 3 have internal pull-ups. Figure 8a shows that the strong transistor p1 is turned on for only 2 oscillator periods after a LOW-to-HIGH transition in the port latch. When on, it turns on p3 (a weak pull-up) through the inverter. This inverter and p3 form a latch which holds the logic 1. In Port 0 the pull-up p1 is only on when emitting logic 1s for external memory access. Writing a logic 1 to a Port 1 bit latch leaves both output transistors switched off so that the pin can be used as an high-impedance input.

6.5.2 PORT OPTIONS

30 of the 32 port pins (excluding P1.6 and P1.7 with option 2S only) may be individually configured with one of the following options. These options are also shown in Fig.8.

Option 1 Standard Port; quasi-bidirectional I/O with pull-up. The strong booster pull-up p1 is turned on for two oscillator periods after a LOW-to-HIGH transition in the port latch (see Fig.8a).

Option 2 Open drain; quasi-bidirectional I/O with n-channel open drain output. Use as an output requires the connection of an external pull-up resistor (see Fig.8c).

Option 3 Push-Pull; output with drive capability in both polarities. Under this option, pins can only be used as outputs (see Fig.8b).

The definition of port options for Port 0 is slightly different. Two cases are examined. First, access to external memory ($\overline{EA}$ = 0 or access above the built-in memory boundary) and second, I/O accesses.

6.5.2.1 External Memory Accesses

Option 1 True 0 and 1 are written as address to the external memory (strong pull-up to be used).

Option 2 An external pull-up resistor is required for external accesses.

Option 3 Not allowed for external memory accesses as the port can only be used as output.

6.5.2.2 I/O Accesses

Option 1 When writing a logic 1 to the port latch, the strong pull-up p1 will be on for 2 oscillator periods. No weak pull-up exists. Without an external pull-up, this option can be used as a high-impedance input.

Option 2 Open drain; quasi-directional I/O with n-channel open drain output. Use as an output requires the connection of an external pull-up resistor. See Fig.8c.

Option 3 Push-Pull; output with drive capability in both polarities. Under this option pins can only be used as outputs.

Individual mask selection of the post-reset state is available with any of the above pins. The required selection is made by appending 'R' or 'S' to options 1, 2, or 3 above.

Option R RESET, after reset this pin will be initialized LOW.

Option S SET, after reset this pin will be initialized HIGH.

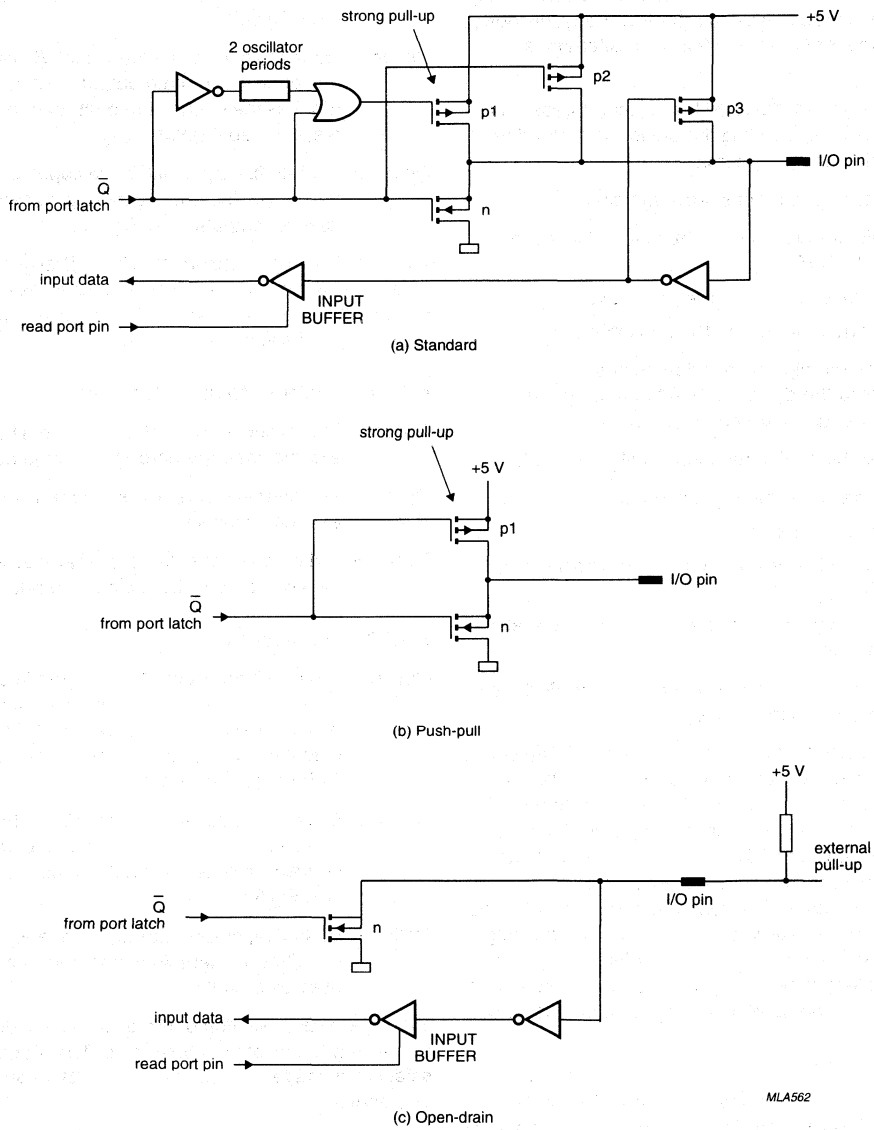


Fig.8 Port configuration options.

6.6 Timer/event counters

The P83CL781 contains three 16-bit timer/event counters: Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

In the 'timer' mode the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is $^1/_{12}f_{osc}$.

In the 'counter' mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes 2 machine cycles (24 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $^1/_{24}f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

6.6.1 Timer T2

Timer T2 is a 16-bit timer/counter that can operate either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register. Three operating modes are available Capture, Auto-Reload and Baud rate generator, these are also selected via the T2CON register.

In the Capture Mode, two options may be selected by the EXEN2 bit in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt. If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt. The Capture Mode is shown in Fig.9.

In the Auto-Reload Mode there are also two options selected by the EXEN2 bit in T2CON. If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software. If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit. The Auto-Reload Mode is shown in Fig.10.

The Baud rate generator Mode is selected when RTCLK = 1. This is described in Section 6.10.

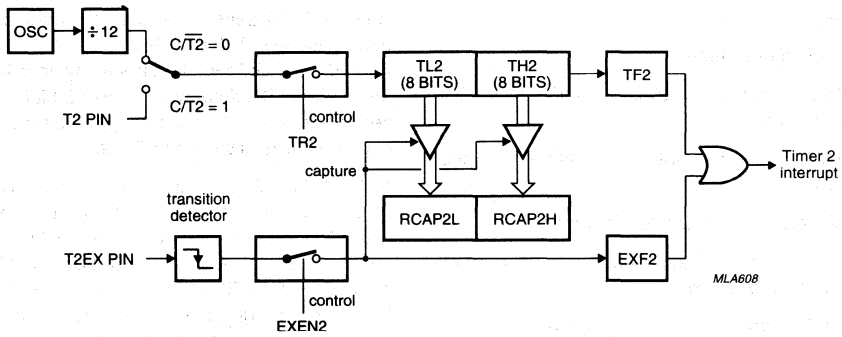


Fig.9 Timer 2 in Capture Mode.

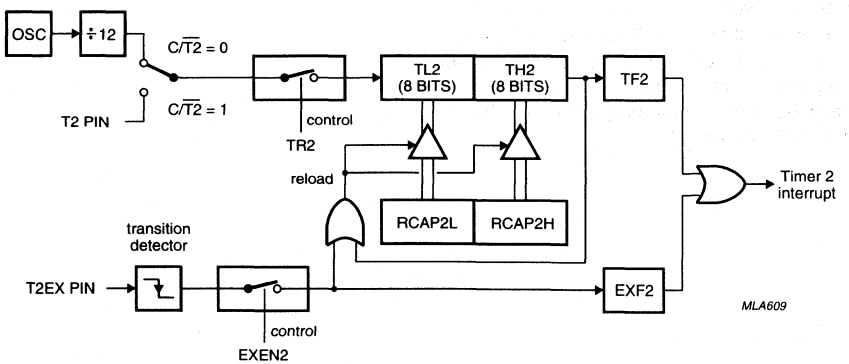


Fig.10 Timer 2 in Auto-Reload Mode.

6.6.2 TIMER/COUNTER 2 CONTROL REGISTER (T2CON)

Table 2 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	GF2	RTCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 3 Description of T2CON bits

BIT	SYMBOL	FUNCTION
T2CON.7	TF2	Timer 2 overflow flag, set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when RTCLK = 1.
T2CON.6	EXF2	Timer 2 external flag is set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
T2CON.5	GF2	General purpose flag bit.
T2CON.4	RTCLK	Transmit clock flag. When set, causes the UART serial port to use Timer 2 overflow pulses for its receive and transmit clock in Modes 1 and 3. RTCLK = 0 causes Timer 1 overflows to be used for the receive and transmit clock.
T2CON.3	EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX, if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
T2CON.2	TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
T2CON.1	C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $^1/_{12}f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge-triggered.
T2CON.0	CP/$\overline{RL2}$	Capture/reload flag. When set captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When RTCLK = 1 this bit is ignored and the timer is forced to auto-reload on a Timer 2 overflow.

Table 4 Timer 2 operating modes

RTCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit auto-reload
0	1	1	16-bit capture
1	X	1	baud rate generator
X	X	0	OFF

6.7 Idle and Power-down operation

Idle mode operation permits the interrupt, serial ports and timer blocks to continue to function while the clock to the CPU is halted.

The following functions remain active during the Idle mode. These functions may generate an interrupt or reset; thus ending the Idle mode.

- Timer 0, Timer 1 and Timer 2
- SIO, I^2C-bus interface
- External interrupt.

The Power-down operation freezes the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register. The Idle and Power-down clock configuration is shown in Fig.11.

6.7.1 IDLE MODE

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before the Idle mode is activated. Once in the Idle mode, the CPU status is preserved along with the Stack Pointer, Program Counter, Program Status Word and Accumulator. The RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 5.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an external hardware reset, or an internal reset caused by an overflow of Timer T2. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation. Reset redefines all SFRs but does not affect the on-chip RAM.

6.7.2 POWER-DOWN MODE

The instruction that sets PCON.1 is the last executed prior to going into the Power-down mode. Once in the Power-down mode, the oscillator is stopped. The contents of the on-chip RAM and the SFRs are preserved. The port pins output the value held by their respective SFRs. ALE and $\overline{PSEN}$ are held LOW.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The supply voltage must not be reduced until the Power-down mode is entered, and must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

6.7.3 WAKE-UP MODE

Setting the PD flag in the PCON register forces the controller into the Power-down mode. Setting this flag enables the controller to be woken-up from the Power-down mode with either the external interrupts INT2 to INT9, or a reset operation.

6.7.3.1 Wake-up using INT2 to INT9

If any of the interrupts INT2 to INT9 are enabled, the device can be woken-up from the Power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods. This is controlled by an on-chip delay counter.

6.7.3.2 Wake-up using RST

To wake-up the P83CL781, the RST pin must be kept HIGH for a minimum of 24 periods. The on-chip delay counter is inactive. The user must ensure that the oscillator is stable before any operation is attempted. Figure 12 illustrates the two possibilities for wake-up.

6.7.4 STATUS OF EXTERNAL PINS

The status of the external pins during Idle and Power-down mode is shown in Table 5. If the Power-down mode is activated whilst accessing external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor p1 (see Fig.8a).

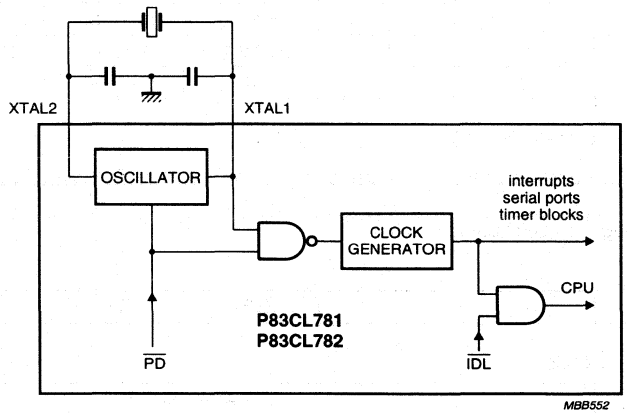


Fig.11 Internal Idle and Power-down clock configuration.

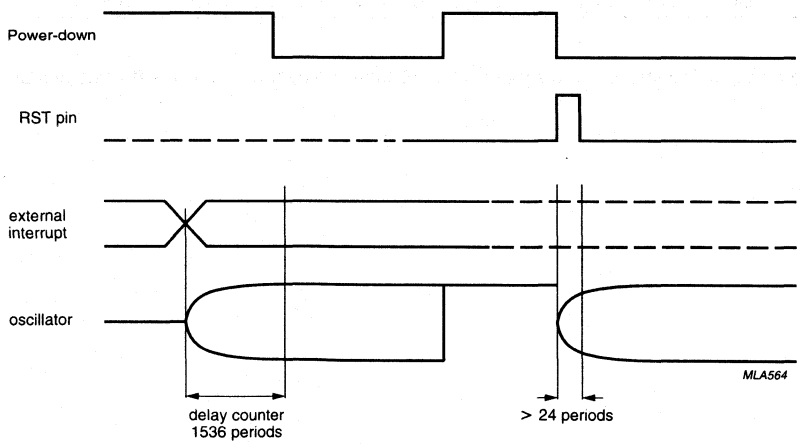


Fig.12 Wake-up operation.

Table 5 Status of external pins during Idle and Power-down modes

MODE	MEMORY	ALE	$\overline{\text{PSEN}}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	internal	1	1	port data	port data	port data	port data
Idle	external	1	1	floating	port data	address	port data
Power-down	internal	0	0	port data	port data	port data	port data
Power-down	external	0	0	floating	port data	port data	port data

6.7.5 Power Control Register (PCON)

The reduced power modes are activated by software using this Special Function Register. PCON is not bit addressable.

Table 6 Power Control Register (SFR address 87H)

7	6	5	4	3	2	1	0
SMOD	–	–	–	GF1	GF0	PD	IDL

Table 7 Description of PCON bits.

BIT	SYMBOL	FUNCTION
PCON.7	SMOD	Double Baud rate bit. When set to a logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3.
PCON.6	–	Reserved
PCON.5	–	Reserved
PCON.4	–	Reserved
PCON.3	GF1	General purpose flag bit
PCON.2	GF0	General purpose flag bit
PCON.1	PD	Power-down bit. Setting this bit activates the Power-down mode; see note 1.
PCON.0	IDL	Idle mode bit. Setting this bit activates the Idle mode; see note 1.

Note

1. If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XX00000).

6.8 I²C-bus serial I/O

The serial port supports the twin line I²C-bus. The I²C-bus consists of two lines: a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines P1.7 and P1.6 respectively. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware. The I²C-bus serial I/O has complete autonomy in byte handling and operates in 4 modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

These functions are controlled by the S1CON register. S1STA is the Status Register whose contents may also be used as a vector to various service routines. S1DAT is the Data Shift Register and S1ADR the Slave Address Register. Slave address recognition is performed by on-chip hardware. The block diagram of the I²C-bus serial I/O is shown in Fig.13.

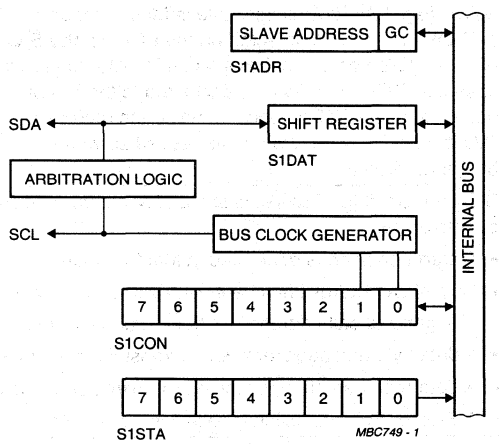


Fig.13 Block diagram of I²C-bus serial I/O.

6.8.1 SERIAL CONTROL REGISTER (S1CON)

Table 8 Serial Control Register (SFR address D8H)

7	6	5	4	3	2	1	0
CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Table 9 Description of S1CON bits

BIT	SYMBOL	FUNCTION
S1CON.7	CR2	This bit along with bits CR1 and CR0 determines the serial clock frequency when SIO is in the Master Mode. See Table 10.
S1CON.6	ENS1	ENABLE serial I/O. When ENS1 = 0, the serial I/O is disabled. SDA and SCL outputs are in the high-impedance state; P1.6 and P1.7 function as open-drain ports. When ENS1 = 1, the serial I/O is enabled. Output port latches P1.6 and P1.7 must be set to logic 1.
S1CON.5	STA	START flag. When this bit is set in Slave Mode, the SIO hardware checks the status of the I^2C-bus and generates a START condition if the bus is free or after the bus becomes free. If STA is set while the SIO is in Master Mode, SIO will generate a repeated START condition.
S1CON.4	STO	STOP flag. With this bit set while in Master Mode a STOP condition is generated. When a STOP condition is detected on the I^2C-bus, the SIO hardware clears the STO flag. STO may also be set in Slave Mode in order to recover from an error condition. In this case no STOP condition is transmitted to the I^2C-bus. However, the SIO hardware behaves as if a STOP condition has been received and releases the SDA and SCL. The SIO then switches to the not addressed slave receiver mode. The STOP flag is cleared by the hardware.
S1CON.3	SI	SIO interrupt flag. This flag is set, and an interrupt is generated, after any of the following events occur: • A start condition is generated in Master Mode. • Own slave address has been received during AA = 1. • The general call address has been received while S1ADR0 and AA = 1. • A data byte has been received or transmitted in Master Mode (even if arbitration is lost). • A data byte has been received or transmitted as selected slave. • A Stop or Start condition is received as selected slave receiver or transmitter.
S1CON.2	AA	Assert Acknowledge. When this bit is set, an acknowledge (LOW level to SDA) is returned during the acknowledge clock pulse on the SCL line when: • Own slave address is received. • General call address is received (S1ADR.0 = 1). • A data byte is received while the device is programmed to be a Master Receiver. • A data byte is received while the device is a selected Slave Receiver. When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own slave address or general call address is received.
S1CON.1	CR1	These two bits along with the CR2 bit determines the serial clock frequency when SIO is in the Master Mode. See Table 10.
S1CON.0	CR0	

Table 10 Selection of the serial clock frequency in the master mode of operation

CR2	CR1	CR0	f_{osc} DIVISOR	BIT RATE (kHz) at f_{osc}		
				3.58 MHz	6 MHz	12 MHz
0	0	0	256	14.0	23.4	46.9
0	0	1	224	16.0	26.8	53.6
0	1	0	192	18.6	31.3	62.5
0	1	1	160	22.4	37.5	75.0
1	0	0	960	3.73	6.25	12.5
1	0	1	120	29.8	50.0	100
1	1	0	60	59.7	100	–
1	1	1	not allowed	–	–	–

6.8.2 DATA SHIFT REGISTER (S1DAT)

S1DAT contains the serial data to be transmitted or data which has just been received. Bit 7 is transmitted or received first; i.e. data shifted from left to right.

Table 11 Data Shift Register (SFR address DAH)

7	6	5	4	3	2	1	0
S1DAT.7	S1DAT.6	S1DAT.5	S1DAT.4	S1DAT.3	S1DAT.2	S1DAT.1	S1DAT.0

6.8.3 ADDRESS REGISTER (S1ADR)

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter.

Table 12 Address Register (SFR address DBH)

7	6	5	4	3	2	1	0
SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	GC

Table 13 Description of S1ADR bits

BIT	SYMBOL	FUNCTION
S1ADR.7 to S1ADR.1	SLA6 to 0	Own slave address.
S1ADR.0	GC	This bit is used to determine whether the general CALL address is recognized. When a logic 0, the general CALL address is not recognized. When a logic 1, the general CALL address is recognized.

6.8.4 SERIAL STATUS REGISTER (S1STA)

The contents of this register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I²C-bus. S1STA is a read-only register. The status codes for all possible modes of the I²C-bus interface are given in Tables 16 to 20.

Table 14 Serial Status Register (SFR address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 15 Description of S1STA bits

BIT	SYMBOL	FUNCTION
S1STA.3 to S1STA.7	SC4 to SC0	5-bit status code.
S1STA.0 to S1STA.2	–	These three bits are held LOW.

Table 16 MST/TRX mode

S1STA VALUE	DESCRIPTION
08H	A START condition has been transmitted.
10H	A repeated START condition has been transmitted.
18H	SLA and W have been transmitted, ACK has been received.
20H	SLA and W have been transmitted, $\overline{\text{ACK}}$ received.
28H	DATA of S1DAT has been transmitted, ACK received.
30H	DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received.
38H	Arbitration lost in SLA, R/W or DATA.

Table 17 MST/REC mode

S1STA VALUE	DESCRIPTION
38H	Arbitration lost while returning $\overline{\text{ACK}}$.
40H	SLA and R have been transmitted, ACK received.
48H	SLA and R have been transmitted, $\overline{\text{ACK}}$ received.
50H	DATA has been received, ACK returned.
58H	DATA has been received, $\overline{\text{ACK}}$ returned.

Table 18 SLV/REC mode

S1STA VALUE	DESCRIPTION
60H	Own SLA and W have been received, ACK returned.
68H	Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned.
70H	General CALL has been received, ACK returned.
78H	Arbitration lost in SLA, R/W as MST. General CALL has been received.
80H	Previously addressed with own SLA. DATA byte received, ACK returned.
88H	Previously addressed with own SLA. DATA byte received, $\overline{\text{ACK}}$ returned.
90H	Previously addressed with general CALL. DATA byte has been received, ACK has been returned.
98H	Previously addressed with general CALL. DATA byte has been received, $\overline{\text{ACK}}$ has been returned.
A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

Table 19 SLV/TRX mode

S1STA VALUE	DESCRIPTION
A8H	Own SLA and R have been received, ACK returned.
B0H	Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned.
B8H	DATA byte has been transmitted, ACK received.
C0H	DATA byte has been transmitted, $\overline{\text{ACK}}$ received.
C8H	Last DATA byte has been transmitted (AA = logic 0), ACK received.

Table 20 Miscellaneous

S1STA VALUE	DESCRIPTION
00H	Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition.

Table 21 Symbols used in Tables 16 to 20

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	Read bit
W	Write bit
ACK	Acknowledgement (acknowledge bit = logic 0)
$\overline{\text{ACK}}$	No acknowledgement (acknowledge bit = logic 1)
DATA	8-bit data byte to or from I^2C-bus
MST	Master
SLV	Slave
TRX	Transmitter
REC	Receiver

6.9 Standard serial interface SIO0: UART

This serial port is full duplex which means that it can transmit and receive simultaneously. It is also receive-buffered and can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte has not been read by the time the reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed via the Special Function Register S0BUF. Writing to S0BUF loads the transmit register and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0 Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at $1/12$ the oscillator frequency.

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first) and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register S0CON. The baud rate is variable.

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in S0CON, while the stop bit is ignored. The baud rate is programmable to either $1/32$ or $1/64$ of the oscillator frequency.

Mode 3 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

6.9.1 MULTIPROCESSOR COMMUNICATIONS

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th bit goes into RB8. The following bit is the stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated, but only if RB8 = 1. This feature is enabled by setting bit SM2 in S0CON. One use of this feature, in multiprocessor systems, is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is HIGH in an address byte and LOW in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be sent. The slaves that were not being addressed leave their SM2 bits set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

6.9.2 Serial Port Control Register (S0CON)

The Serial Port Control and Status Register is the Special Function Register S0CON; shown in Table 22. The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 22 Serial Port Control Register (SFR address 98H)

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 23 Description of S0CON bits

BIT	SYMBOL	FUNCTION
S0CON.7	SM0	These two bits are used to select the serial port mode. See Table 24.
S0CON.6	SM1	
S0CON.5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In these modes, if SM2 = 1, then RI will not be activated if the received 9th data bit (RB8) is a logic 0. In Mode 1, if SM2 = 1, then RI will not be activated unless a valid Stop bit was received. In Mode 0, SM2 should be a logic 0.
S0CON.4	REN	Enables serial reception and is set by software to enable reception, and cleared by software to disable reception.
S0CON.3	TB8	Is the 9th data bit that will be transmitted in Modes 2 and 3. Set or cleared by software as desired.
S0CON.2	RB8	In Modes 2 and 3, is the 9th data bit received. In Mode 1, if SM2 = 0 then RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
S0CON.1	TI	The transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit time in the other modes, in any serial transmission. Must be cleared by software.
S0CON.0	RI	The receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial transmission (for exception see SM2). Must be cleared by software.

Table 24 Selection of the serial port modes

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	0	shift register	$^1/_{12}f_{osc}$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$^1/_{64}f_{osc}$ or $^1/_{32}f_{osc}$
1	1	3	9-bit UART	variable

6.10 Baud rates

The baud rate in Mode 0 is fixed and may be calculated as shown below:

$$\text{Baud rate} = \frac{f_{osc}}{12}$$

The baud rate in Mode 2 depends on the value of the SMOD bit in Special Function Register PCON. If SMOD = 0, (which is the value on reset), the baud rate is $1/64$ the oscillator frequency. If SMOD = 1, the baud rate is $1/32$ the oscillator frequency. The baud rate in Mode 2 may be calculated as shown below:

$$\text{Baud rate} = \frac{2^{SMOD}}{64} \times f_{osc}$$

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

6.10.1 Using Timer 1 to generate baud rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of the SMOD bit as follows:

$$\text{Baud rate} = \frac{2^{SMOD}}{32} \times \text{Timer 1 overflow rate}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either 'timer' or 'counter' operation in any of its 3 running modes. In most typical applications, it is configured for 'timer' operation, in the Auto-Reload mode (high nibble of TMOD = 0010B). In this case the baud rate is given by the formula:

$$\text{Baud rate} = \frac{2^{SMOD}}{32} \times f_{osc} \times \frac{1}{[12 \times (256 - TH1)]}$$

By configuring Timer 1 to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload, very low baud rates can be achieved. Table 25 lists various commonly used baud rates and how they can be obtained from Timer 1.

Table 25 Timer 1 generated commonly used baud rates

BAUD RATE	f_{osc} (MHz)	SMOD	C/T	TIMER 1 MODE	RELOAD VALUE
Mode 0 max: 1 Mbits/s	12	X	X	X	X
Mode 2 max: 375 kbits/s	12	1	X	X	X
Modes 1 and 3: 62.5 kbit/s	12	1	0	2	FFH
19.2 kbits/s	11.059	1	0	2	FDH
9.6 kbits/s	11.059	0	0	2	FDH
4.8 kbits/s	11.059	0	0	2	FAH
2.4 kbits/s	11.059	0	0	2	F4H
1.2 kbits/s	11.059	0	0	2	E8H
137.5 kbits/s	11.986	0	0	2	1DH
110	6	0	0	2	72H
110	12	0	0	1	FEEBH

6.10.2 USING TIMER 2 TO GENERATE BAUD RATES

Timer 2 is selected as a baud rate generator by setting the RTCLK bit in T2CON. The baud rate generator mode is similar to the Auto-Reload mode, in that a roll-over in TH2 causes Timer 2 registers to be reloaded with the 16-bit value held in the registers RCAP2H and RCAP2L, which are preset by software. Baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as specified below.

$$\text{Baud rate} = \frac{\text{Timer 2 overflow rate}}{16}$$

The timer can be configured for either 'timer' or 'counter' operation. In typical applications it is configured for timer operation ($C/\overline{T2} = 0$). Timer operation is slightly different for Timer 2 when it is being used as a baud rate generator. Normally, as a timer it would increment every machine cycle at a frequency of $\frac{1}{12}f_{osc}$. However, as a baud rate generator it increments every state time at a frequency of $\frac{1}{2}f_{osc}$. In this case the baud rate is determined as specified below.

$$\text{Baud rate} = \frac{f_{osc}}{32 \times [65536 - (\text{RCAP2H;RCAP2L})]}$$

Where (RCAP2H;RCAP2L) is the content of registers RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The baud rate generator mode for Timer 2 is shown in Fig.14. This figure is only valid if RTCLK = 1. At roll-over TH2 does not set the TF2 bit in T2CON and therefore, will not generate an interrupt. Consequently, the Timer 2 interrupt does not need to be disabled when in the baud rate generator mode. If EXEN2 is set, a HIGH-to-LOW transition on T2EX will set the EXF2 bit, also in T2CON, but will not cause a reload from (RCAP2H; RCAP2L) to (TH2; TL2). Therefore, in this mode T2EX may be used as an additional external interrupt.

When Timer 2 is operating as a timer (TR2 = 1), in the baud rate generator mode, registers TH2 and TL2 should not be accessed. Under these conditions the timer is being incremented every state time and therefore the results of a read or write may not be accurate. The RCAP registers however, may be read but not written to. A write might overlap a reload and cause write and/or reload errors. If a write operation is required Timer 2 should first be turned off by clearing the TR2 bit.

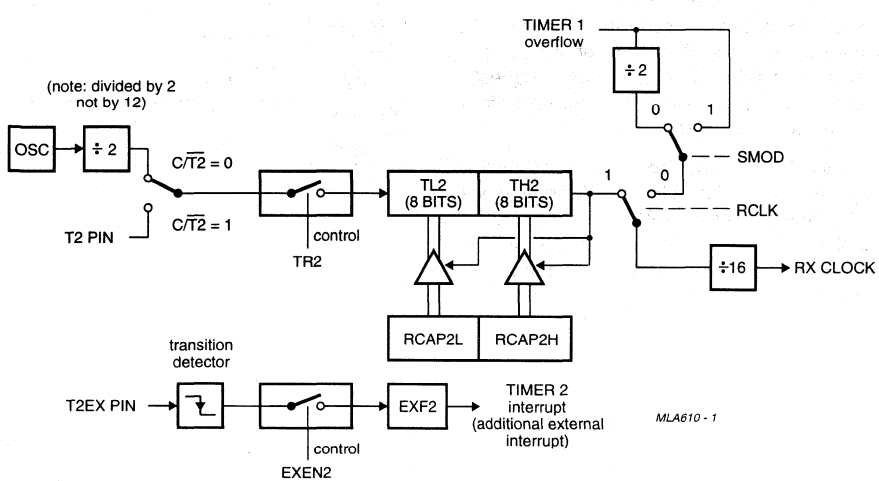


Fig.14 Timer 2 in Baud Rate Generator Mode.

6.11 Interrupt system

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronously to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The interrupt system is shown in Fig.15. The P83CL781 acknowledges interrupt requests from fifteen sources as follows:

- INT0 to INT9
- Timer 0, Timer 1 and Timer 2
- I^2C-bus serial I/O
- UART.

Each interrupt vectors to a separate location in program memory for its service routine. Each source can be individually enabled or disabled by its corresponding bit in the Interrupt Enable Registers (1EN0 and 1EN1). The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled.

6.11.1 External interrupts INT2 to INT9

Port 1 lines serve an alternative purpose as eight additional interrupts INT2 to INT9. When enabled, each of these lines may wake-up the device from the Power-down mode. Using the Interrupt Polarity Register (IX1), each pin may be initialized to be either active HIGH or active LOW. IRQ1 is the Interrupt Request Flag Register. If the interrupt is enabled, each flag will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled.

Port 1 interrupts are level sensitive. A Port 1 interrupt will be recognized when a level (HIGH or LOW depending on the Interrupt Polarity Register) on P1.n is held active for at least one machine cycle. The interrupt request is not serviced until the next machine cycle. The external interrupt configuration is shown in Fig.15.

6.11.2 Interrupt priority

Each interrupt source can be set to either a high priority or to a low priority. If both priorities are requested simultaneously, the processor will branch to the high priority vector. A low priority interrupt can only be interrupted by a high priority interrupt. A high priority interrupt routine can not be interrupted.

Table 26 shows the interrupt vectors in order of priority. X0 having the highest priority; X9 the lowest. The vector indicates the ROM location where the appropriate interrupt service routine starts.

Table 26 Interrupt vectors

SOURCE	SYMBOL	VECTOR
External 0	X0	0003H
I^2C-bus port	S1	002BH
External 5	X5	0053H
Timer 0	T0	000BH
Timer 2	T2	0033H
External 6	X6	005BH
External 1	X1	0013H
External 2	X2	003BH
External 7	X7	0063H
Timer 1	T1	001BH
External 3	X3	0043H
External 8	X8	006BH
UART	SO	0023H
External 4	X4	004BH
External 9	X9	0073H

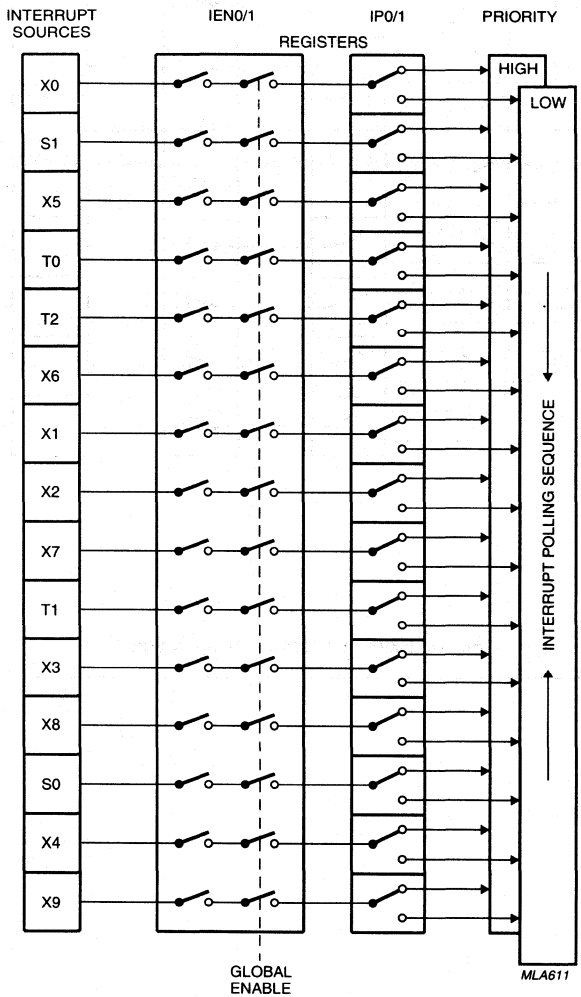


Fig.15 Interrupt system.

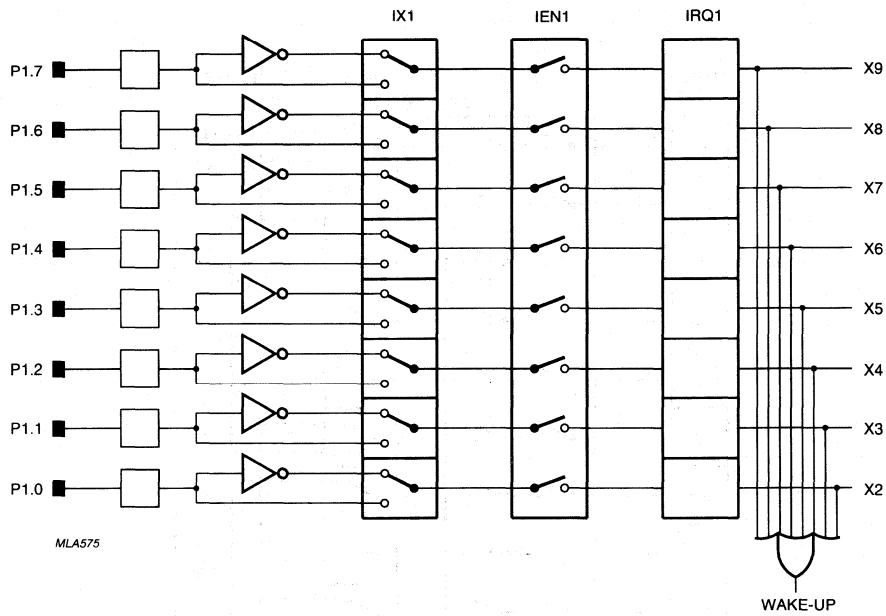


Fig.16 External interrupt configuration.

6.11.3 Interrupt Enable Register (IEN0)

Table 27 Interrupt Enable Register (SFR address A8H)

7	6	5	4	3	2	1	0
EA	ET2	ES1	ES0	ET1	EX1	ET0	EX0

Table 28 Description of IEN0 bits

BIT[1]	SYMBOL	FUNCTION
IEN0.7	EA	General enable/disable control. If EA = 0, no interrupt is enabled. If EA = 1, any individually enabled interrupt will be accepted.
IEN0.6	ET2	enable T2 interrupt
IEN0.5	ES1	enable I^2C-bus interrupt
IEN0.4	ES0	enable UART SIO interrupt
IEN0.3	ET1	enable Timer 1 interrupt (T1)
IEN0.2	EX1	enable external interrupt 1
IEN0.1	ET0	enable Timer 0 interrupt (T0)
IEN0.0	EX0	enable external interrupt 0

Note

1. Where: logic 0 = interrupt disabled; logic 1 = interrupt enabled.

6.11.4 Interrupt Enable Register (IEN1)

Table 29 Interrupt Enable Register (SFR address E8H)

7	6	5	4	3	2	1	0
EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Table 30 Description of IEN1 bits

BIT[1]	SYMBOL	FUNCTION
IEN1.7	EX9	enable external interrupt 9
IEN1.6	EX8	enable external interrupt 8
IEN1.5	EX7	enable external interrupt 7
IEN1.4	EX6	enable external interrupt 6
IEN1.3	EX5	enable external interrupt 5
IEN1.2	EX4	enable external interrupt 4
IEN1.1	EX3	enable external interrupt 3
IEN1.0	EX2	enable external interrupt 2

Note

1. Where: logic 0 = interrupt disabled; logic 1 = interrupt enabled.

6.11.5 Interrupt Priority Register (IP0)

Table 31 Interrupt Priority Register (SFR address B8H)

7	6	5	4	3	2	1	0
–	PT2	PS1	PS0	PT1	PX1	PT0	PX0

Table 32 Description of IP0 bits

BIT[1]	SYMBOL	FUNCTION
IP0.7	–	Reserved
IP0.6	PT2	Timer 2 interrupt priority level
IP0.5	PS1	I^2C-bus interrupt priority level
IP0.4	PS0	UART SIO interrupt priority level
IP0.3	PT1	Timer 1 interrupt priority level
IP0.2	PX1	External interrupt 1 priority level
IP0.1	PT0	Timer 0 interrupt priority level
IP0.0	PX0	External interrupt 0 priority level

Note

1. Where: logic 0 = low priority; logic 1 = high priority.

6.11.6 Interrupt Priority Register (IP1)

Table 33 Interrupt Priority Register (SFR address F8H)

7	6	5	4	3	2	1	0
PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Table 34 Description of IP1 bits

BIT[1]	SYMBOL	FUNCTION
IP1.7	PX9	external interrupt 9 priority level
IP1.6	PX8	external interrupt 8 priority level
IP1.5	PX7	external interrupt 7 priority level
IP1.4	PX6	external interrupt 6 priority level
IP1.3	PX5	external interrupt 5 priority level
IP1.2	PX4	external interrupt 4 priority level
IP1.1	PX3	external interrupt 3 priority level
IP1.0	PX2	external interrupt 2 priority level

Note

1. Where: logic 0 = low priority; logic 1 = high priority.

6.11.7 Interrupt Polarity Register (IX1)

Writing either a logic 1 or logic 0logic 0 to any Interrupt Polarity Register bit sets the polarity level of the corresponding external interrupt to an active HIGH or active LOW respectively.

Table 35 Interrupt Polarity Register (SFR address E9H)

7	6	5	4	3	2	1	0
IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Table 36 Description of IX1 bits

BIT	SYMBOL	FUNCTION
IX1.7	IL9	external interrupt 9 polarity level
IX1.6	IL8	external interrupt 8 polarity level
IX1.5	IL7	external interrupt 7 polarity level
IX1.4	IL6	external interrupt 6 polarity level
IX1.3	IL5	external interrupt 5 polarity level
IX1.2	IL4	external interrupt 4 polarity level
IX1.1	IL3	external interrupt 3 polarity level
IX1.0	IL2	external interrupt 2 polarity level

6.11.8 Interrupt Request Flag Register (IRQ1)

Table 37 Interrupt Request Flag Register (SFR address C0H)

7	6	5	4	3	2	1	0
IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Table 38 Description of IRQ1 bits

BIT	SYMBOL	FUNCTION
IRQ1.7	IQ9	external interrupt 9 request flag
IRQ1.6	IQ8	external interrupt 8 request flag
IRQ1.5	IQ7	external interrupt 7 request flag
IRQ1.4	IQ6	external interrupt 6 request flag
IRQ1.3	IQ5	external interrupt 5 request flag
IRQ1.2	IQ4	external interrupt 4 request flag
IRQ1.1	IQ3	external interrupt 3 request flag
IRQ1.0	IQ2	external interrupt 2 request flag

6.11.9 RELATED REGISTERS

The following registers are used in conjunction with the interrupt system.

Table 39 Related registers

REGISTER	FUNCTION	SFR ADDRESS
IX1	Interrupt Polarity Register	E9H
IRQ1	Interrupt Request Flag Register	C0H
IEN0	Interrupt Enable Register	A8H
IEN1	Interrupt Enable Register (INT2 to INT9)	E8H
IP0	Interrupt Priority Register	B8H
IP1	Interrupt Priority Register (INT2 to INT9)	F8H

6.12 Oscillator circuitry

The on-chip oscillator circuitry of the P83CL781 is a single-stage inverting amplifier biased by an internal feedback resistor. The oscillator circuit is shown in Fig.17. For operation as a standard quartz oscillator, no external components are needed (except at 32 kHz). When using external capacitors, ceramic resonators, coils and RC networks to drive the oscillator, five different configurations are supported (see Table 40 and Fig.18).

In the Power-down mode the oscillator is stopped and XTAL1 is pulled HIGH. The oscillator invertor is switched off to ensure no current will flow regardless of the voltage at XTAL1. To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Fig.18f. There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is buffered by a flip-flop.

Various oscillator options are provided for optimum on-chip oscillator performance; these are specified in Table 40 and shown in Fig.18. The required option should be stated when ordering.

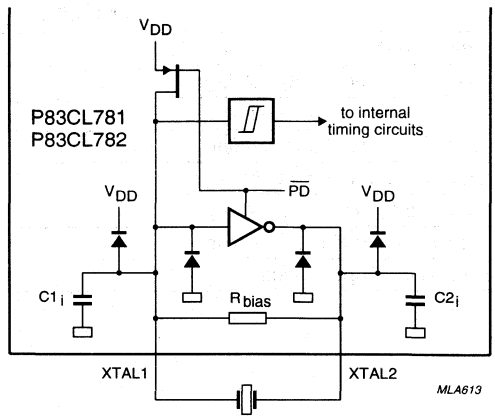


Fig.17 Oscillator.

Table 40 Oscillator options

OSCILLATOR	APPLICATION
Oscillator 1	For 32 kHz clock applications with external trimmer for frequency adjustment. A 4.7 MΩ bias resistor is needed for use in parallel with the crystal. See Fig.18c.
Oscillator 2	For low-power, low-frequency operations using LC components. See Fig.18e.
Oscillator 3	For medium frequency range applications.
Oscillator 4	For high frequency range applications.
RC	RC oscillator configuration. See Fig.18g.

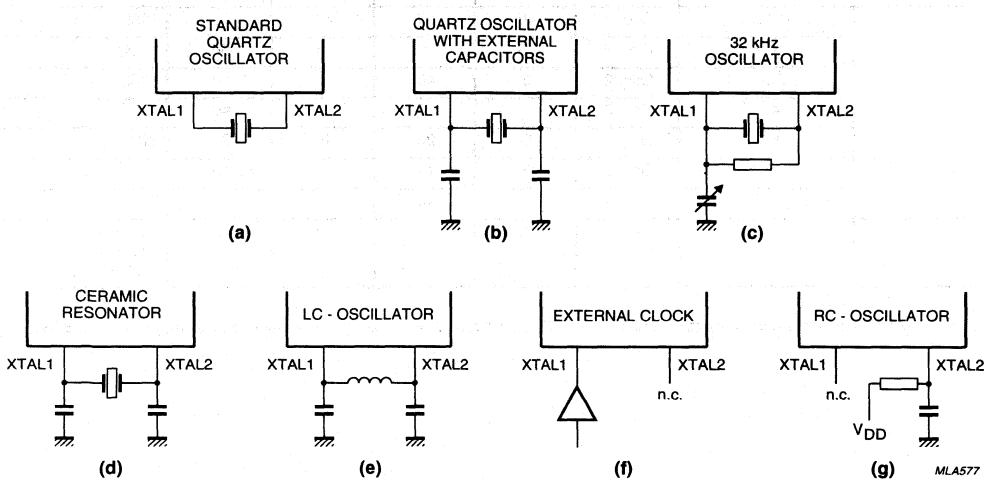


Fig.18 Alternative oscillator configurations.

RESONATOR	FREQUENCY (MHz)	OPTION	c1 ext.(pF)		C2 ext.(pF)		RESONATOR MAX. SERIES RESISTANCE
			MIN.	MAX.	MIN.	MAX.	
Quartz	0.032	Osc. 1	0	0	5	15	15 kΩ; note 1
	1.0	Osc. 2	0	30	0	30	600Ω
	3.58	Osc. 2	0	15	0	15	100Ω
	4.0	Osc. 2	0	20	0	20	75Ω
	6.0	Osc. 3	0	10	0	10	60Ω
	10.0	Osc. 4	0	15	0	15	60Ω
	12.0	Osc. 4	0	10	0	10	40Ω
	16.0	Osc. 4	0	15	0	15	20Ω
PXE	0.455	Osc. 2	40	50	40	50	10Ω
	1.0	Osc. 2	15	50	15	50	100Ω
	3.58	Osc. 2	0	40	0	40	10Ω
	4.0	Osc. 2	0	40	0	40	10Ω
	6.0	Osc. 2	0	20	0	20	5Ω
	10.0	Osc. 3	0	15	0	15	6Ω
	12.0	Osc. 4	10	40	10	40	6Ω
LC		Osc. 2	20	90	20	90	10 μH=1Ω; 100μH=5Ω; 1 mH=75Ω;

NOTES:
1. 32 kHz quartz crystals with a series resistance higher than 15 kΩ will reduce the guaranteed supply voltage range to 2.5 to 3.5V.

Low voltage 16-bit microcontroller P90CL301BFH (C100)

1 FEATURES

- Fully 68000 software compatible
- Static design with 32-bit internal structure
- Power saving modes: Power-down, Stand-by and Idle mode
- External clock input: 27 MHz at 2.7 V
- Single supply voltage of 2.7 to 3.6 V; down to 1.8 V for RAM retention
- 68000-compatible bus interface
- Intel 8051-compatible bus interface
- 16 Mbytes program/data address range
- 8 programmable chip-selects
- Dynamic bus sizing, 16 or 8-bit memory bus port size
- 56 powerful instruction types:
  - 5 basic data types, and
  - 14 addressing modes
- 7 programmable interrupt inputs:
  - a Non-Maskable Interrupt input (NMIN)
  - 14 auto-vectored interrupts and 7 interrupt priority levels
- 24 port pins (multiplexed with other functions)
- 2 UART serial interfaces; an independent baud rate generator with two programmable outputs (UART0 and UART1)
- UART queue with max 256 bytes
- I^2C-bus serial interface 100 Kbauds.
- 2 timer arrays including:
  - two 16-bit reference counter and 8-bit programmable prescaler
  - six 16-bit match/capture registers with equality comparators
- Watchdog timer with 21-bit resolution
- Two 8-bit Pulse Width Modulation (PWM) outputs with 8-bit prescaler
- Four 8-bit analog-to-digital converter (ADC) inputs with Power-down mode
- 512 bytes RAM on-chip
- On-Circuit Emulation (ONCE) mode and internal test-ROM (256 bytes) for on-board testing
- 80-pin LQFP package (typical height 1.4 mm, pitch 0.5 mm)
- Temperature range –40 to +85 °C
- 0.5 micron CMOS low voltage technology.

2 DESCRIPTION

The P90CL301 is a highly integrated low-voltage 16/32-bit microcontroller especially suitable for digital mobile systems such as GSM, DCS1900, IS54/95 and other applications requiring low voltage, low power consumption and high computing power. It is fully software compatible with the 68000.

The P90CL301 optimizes system cost by providing both standard as well as advanced peripheral functions on-chip. The P90CL301 has a full static design and special Idle, Standby and Power-down modes which allow further reduction of the total system power consumption. An 80-pin LQFP package dramatically reduces system size requirements.

2.1 Compatiblity between P90CL301AFH and P90CL301BFH

For functional compatibility between P90CL301AFH (SAC1 process) and P90CL301BFH (C100 process), the following points should be considered when using the P90CL301BFH.

1. Wake-up: To wake up the processor from power-down mode via the activation of an external SPx pin, it is necessary to enable the interrupt mode first by setting the corresponding bit in the SPCON register.
2. SYSCON register: For the P90CL301AFH the bit 11 to 15 in the SYSCON register should not be set in order to keep additional functionality in the P90CL301BFH inactive.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	VERSION	
P90CL301BFH	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1	–40 to +85

4 BLOCK DIAGRAM

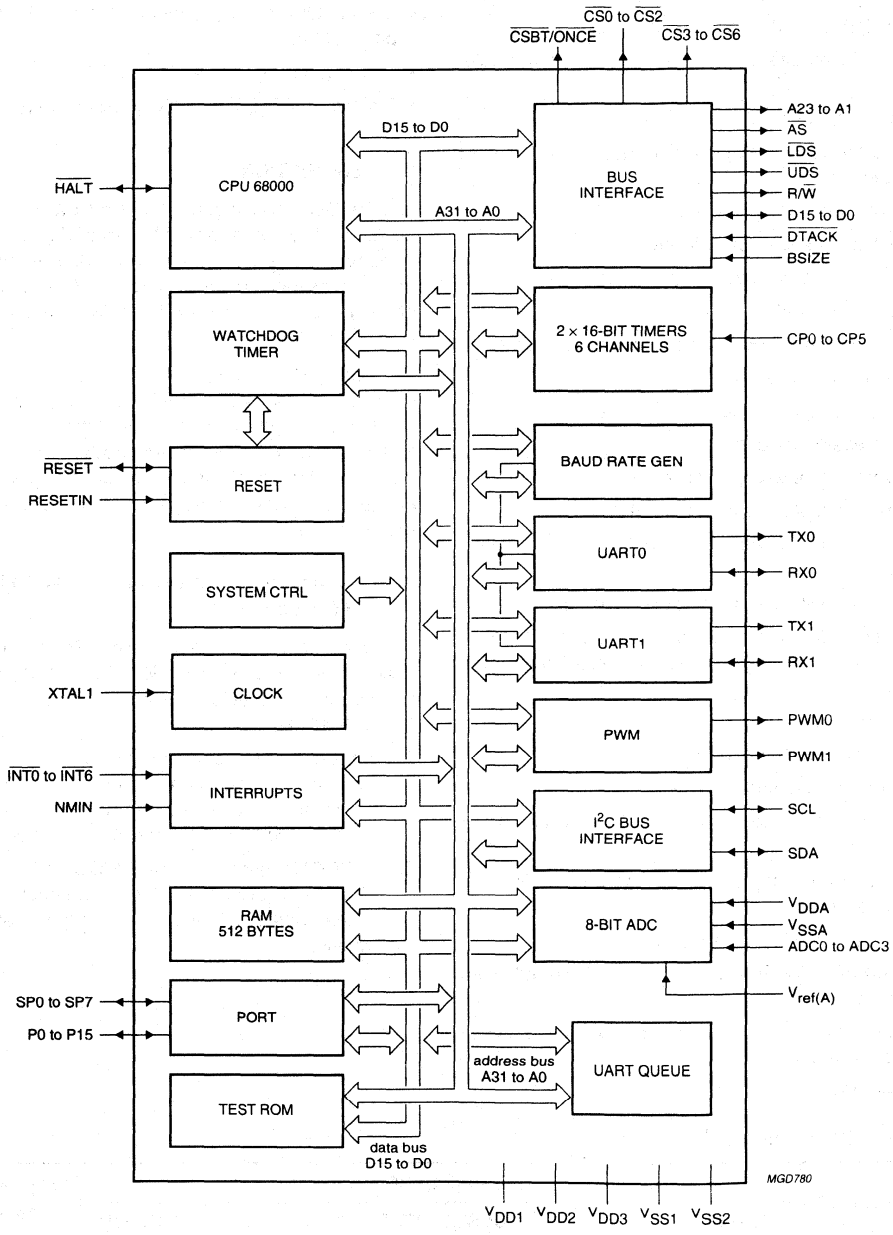


Fig.1 P90CL301 block diagram.

5 PINNING INFORMATION

5.1 Pinning

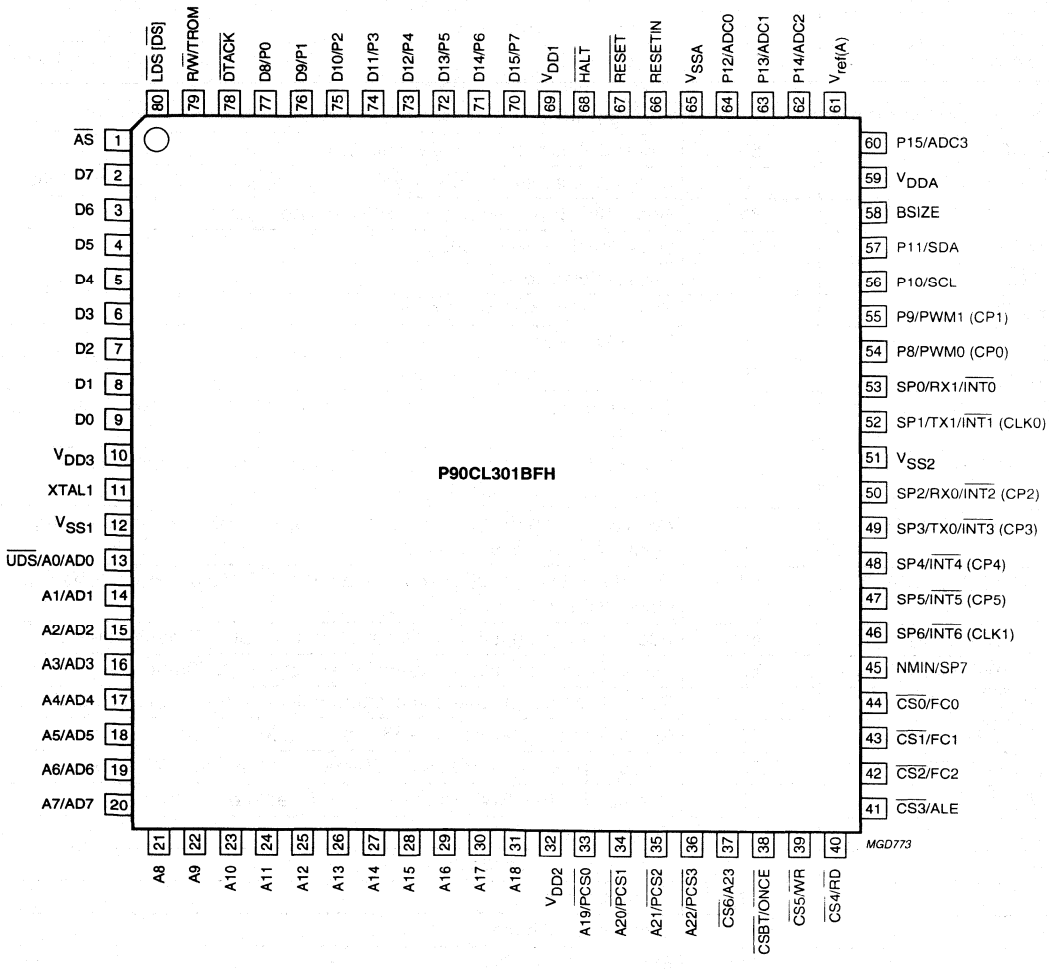


Fig.2 Pinning diagram of the P90CL301BFH (LQFP80).

5.2 Pin description

Table 1 Pin description for the P90CL301

SYMBOL[1]	PIN	FUNCTION
A22/$\overline{PCS3}$ to A19/$\overline{PCS0}$	36 to 33	Upper 4-bits of the address bus or 8051 bus chip-select.
A18 to A8	31 to 21	Upper 11-bits of the 68000 address bus.
A7/AD7 to A1/AD1	20 to 14	Lower 7-bits of the 68000 address bus or lower 7-bits of the 8051 bus.
D7 to D0	2 to 9	Lower 8-bits of data bus.
D15/P7 to D8/P0	70 to 77	Upper 8-bits of data bus or 8-bit Port 7 to Port 0; the selected function after reset is defined by pin BSIZE.
$\overline{AS}$	1	Address strobe.
$\overline{LDS}$ [$\overline{DS}$]	80	Lower Data strobe [word Data strobe].
$\overline{UDS}$/A0/AD0	13	Upper data strobe or LSB of address bus or LSB of 8051 address/data.
R/$\overline{W}$ / TROM	79	Read/Write bus control or test ROM forced input.
$\overline{DTACK}$	78	Data transfer acknowledge.
$\overline{RESET}$	67	Reset (bidirectional).
RESETIN	66	External Power-on-reset input.
$\overline{HALT}$	68	Halt (bidirectional).
BSIZE	58	Data bus size; 8 or 16-bit wide.
SP0/RX1/$\overline{INT0}$	53	Second port pin (bit 0) or Receive data for UART1 or external interrupt input 0.
SP1/TX1/$\overline{INT1}$ (CLK0)	52	Second port pin (bit 1) or Transmit data for UART1 or external interrupt input 1 (external clock of Timer 0).
SP2/RX0/$\overline{INT2}$ (CP2)	50	Second port pin (bit 2) or Receive data for UART0 or external interrupt input 2 (Timer 0 capture input 2).
SP3/TX0/$\overline{INT3}$ (CP3)	49	Second port pin (bit 3) or Transmit data for UART0 or external interrupt input 3 (Timer 1 capture input 3).
SP4/$\overline{INT4}$ (CP4)	48	Second port pin (bit 4) or external interrupt input 4 (Timer 1 capture input 4).
SP5/$\overline{INT5}$ (CP5)	47	Second port pin (bit 5) or external interrupt input 5 (Timer 1 capture input 5).
SP6/$\overline{INT6}$ (CLK1)	46	Second port pin (bit 6) external interrupt input 6 (external clock of timer 1).
NMIN/SP7	45	Non-Maskable Interrupt or second port pin (bit 7).
P8/PWM0 (CP0)	54	Port pin (bit 8) or PWM0 output (Timer 0 capture input 0).
P9/PWM1 (CP1)	55	Port pin (bit 9) or PWM1 output (Timer 0 capture input 1).
V_{DD1}	69	Supply voltage; first pin.
V_{DD2}	32	Supply voltage; second pin.
V_{SS1}	12	Ground; first pin.
V_{SS2}	51	Ground; second pin.
XTAL1	11	External clock input.
V_{DD3}	10	Supply voltage; third pin.
$\overline{CS0}$/FC0 to $\overline{CS2}$/FC2	44 to 42	Chip-select 0 to 2 or data bus function code 2 to 0.
$\overline{CS3}$/ALE	41	Chip-select 3 or 8051 bus address latch.
$\overline{CS4}$/$\overline{RD}$	40	Chip-select 4 or 8051 bus read strobe.
$\overline{CS5}$/$\overline{WR}$	39	Chip-select 5 or 8051 bus write strobe.

SYMBOL[1]	PIN	FUNCTION
P10/SCL	56	Port pin (bit 10) or I^2C-bus Serial Clock.
P11/SDA	57	Port pin (bit 11) or I^2C-bus Serial Data.
$\overline{CS6}$/A23	37	Chip-select 6 or address bit 23.
$\overline{CSBT}$/$\overline{ONCE}$	38	Chip-select boot or ONCE mode forced input.
V_{DDA}	59	ADC supply voltage.
V_{refA}	61	ADC reference voltage.
V_{SSA}	65	ADC ground.
P12/ADC0 to P15/ADC3	64 to 62, 60	Port pin (bit 12 to bit 15) or ADC inputs 0 to 3.

Note

1. The following notation is used to describe the multiple pin definitions:
   a) Function1/Function2/Function3: multiplexed functions on the same pin; Function1 or Function2 or Function3. During and after reset the Function1 is selected.
   b) Function1 (Function2): function done in parallel.
   c) Function1 [Function2]: equivalent function.

6 SYSTEM CONTROL

6.1 Memory organization

The maximum external address space of the controller is 16 Mbytes. It can be partitioned into five address spaces. These address spaces are designated as either User or Supervisor space and as either Program or Data space or as interrupt acknowledge.

For slow memories the CPU can be programmed to insert a number of wait states. This is done via the eight Chip-select Control Registers CSnN. The number of inserted wait states can vary from 0 to 6, or wait states are inserted until the $\overline{\text{DTACK}}$ is pulled LOW by the external address decoding circuitry. If $\overline{\text{DTACK}}$ is asserted continuously, the P90CL301 will run without wait states using bus cycles of three or four clock periods depending on the state of the FBC bit in the SYSCON register.

6.1.1 MEMORY MAP

The memory address space is divided as shown in Table 2; short addressing space with A31 to A15 = 1.

Table 2 Memory address space

ADDRESS (HEX)		DESCRIPTION
FROM	TO	
0000 0000	00FF FFFF	external 16 Mbytes memory
0100 0000	8000 FFFF	not used
8001 0000	8001 FFFF	off-chip 64 kbytes on 8051 bus
8002 0000	FFFF 7FFF	not used
FFFF 8000	FFFF 8AFF	internal registers
FFFF 8B00	FFFF 8FFF	not used
FFFF 9000	FFFF 91FF	internal 512 bytes RAM
FFFF 9200	FFFF BFFF	not used
FFFF C000	FFFF C0FF	internal 256 bytes test ROM
FFFF C100	FFFF FFFF	not used

6.2 Programmable chip-select

In order to reduce the external components associated with memory interface, the 90CL301 provides 8 programmable chip-selects. A specific chip-select $\overline{\text{CSBT}}$ provides default reset values to support a bootstrap operation.

Each chip-select can be programmed with:

- A base address (A23 to A19)
- A memory bank width of 512 kbytes, 1, 2, 4 or 8 Mbytes memory size
- A number of wait states (0 to 6 states, or wait for $\overline{\text{DTACK}}$) to adapt the bus cycle to the memory cycle time.

Chip-selects can be synchronized with read, write, or both read and write, either Address strobe or Data strobe. They can also be programmed to address low byte, high byte or word.

Each chip-select is controlled by a control register CSnN (n = 0 to 7). The control registers are described in Table 3 to 7.

The RESET instruction does not affect the contents of the CSnN registers.

Register CS7N corresponds to register $\overline{\text{CSBT}}$ (address FFFF 8A0EH). After reset $\overline{\text{CSBT}}$ is programmed with a block size of 8 Mbytes with:

- A19 to A23 at logic 0,
- M19 to M22 at logic 1,
- 6 wait states,
- read only mode.

The other chip-selects are held HIGH and will be activated after initialization of their control registers.

When programmed in reduced access mode (read only, write only, low byte, high byte), the wait states are generated internally and if there is any access-violation when the bit WD in the SYSCON register is set to a logic 1 (time-out), the processor will execute a bus error after the time-out delay.

6.2.1 Chip Select Control Registers (CSnN)

Table 3 Chip Select Control Registers; n = 0 to 7 (address FFFF 8A00H to FFFF 8A0CH)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M22	M21	M20	M19	RW1	RW0	MD1	MD0	A23	A22	A21	A20	A19	WS2	WS1	WS0

Table 4 Description of CSnN bits

BIT	SYMBOL	FUNCTION
15 to 12	M22 to M19	Address mask for block size selection; see Table 5.
11 to 10	RW1 to RW0	Read/Write bus control (R/$\overline{W}$); see Table 6.
9 to 8	MD1 to MD0	MODE selection; see Table 7.
7 to 3	A23 to A19	Decoded base address; this should be a multiple of the block size (other codes are reserved for test or reset state); after reset: A23 to A19 = 11111 except for $\overline{CSBT}$.
2 to 0	WS2 to WS0	Wait states 0 to 6 (see Table 8); 7 wait for $\overline{DTACK}$ to be pulled LOW by the external address decoding circuitry.The default value after reset is 6 for $\overline{CSBT}$ and 7 for the other chip-selects.

Table 5 Address mask for block size selection

M22	M21	M20	M19	BLOCK SIZE
0	0	0	0	512 kbytes
0	0	0	1	1 Mbyte
0	0	1	1	2 Mbytes
0	1	1	1	4 Mbytes
1	1	1	1	8 Mbytes; note 1

Table 6 Read/Write bits (R/$\overline{W}$)

RW1	RW0	FUNCTION
0	0	Read only with length of $\overline{AS}$
0	1	Write only with length of $\overline{DS}$
1	0	Write only with length of $\overline{AS}$
1	1	Read/write with length of $\overline{AS}$; note 1

Table 7 Mode selection

MD1	MD0	FUNCTION
0	0	Alternate function
0	1	Low byte access only
1	0	High byte access only
1	1	Word access; note 1

Table 8 Wait states selection

WS2	WS1	WS0	WAIT STATES
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6(1)

Note to Tables 4 to 8

1. The default value after a CPU-reset.

Table 9 Number of clock periods per bus cycle

Number of clock periods per bus cycle, dependent on the programmed length of FBC (Fast Bus Cycle bit in the SYSCON register) and CSn (chip-select).

WAIT STATES	LENGTH OF $\overline{CSn}$ = LENGTH OF $\overline{AS}$			LENGTH OF $\overline{CSn}$ = LENGTH OF $\overline{DS}$			
	FBC = 1		FBC = 0	FBC = 1		FBC = 0	
	READ	WRITE	R/W	READ	WRITE	READ	WRITE
0	3	4	4	3	4	4	4
1	4	4	4	4	5	4	5
2	5	5	5	5	6	5	6
3	6	6	6	6	7	6	7
4	7	7	7	7	8	7	8
5	8	8	8	8	9	8	9
6	9	9	9	9	10	9	10

6.3 Dynamic bus port sizing

The memory bus size can be selected to be 16 or 8-bit wide depending on the ports width of external memories and peripherals. It is possible via the register BSREG to define for each chip-select the bus width to 16-bit or 8-bit used for the transfer of data to or from external memory.

The 7-bit register BSREG defines the bus size affected to each chip-select function (except for $\overline{CSBT}$).

The bus size of the chip-select boot $\overline{CSBT}$ (CS7N) is hardware defined by the pin BSIZE.The state of the pin BSIZE is latched at the end of the reset sequence.

When an address generated by the CPU is identified by a chip-select block as belonging to it's address segment, the corresponding bit of the register BSREG is used to define the sequence of bus transfer in 16 or 8-bit mode. Several chip-selects with different bus sizes should not address the same memory segment. For each case the number of bus cycles necessary to transfer a byte, word or long word is a function of the bus size. For example, a word read on a 8-bit bus will take 2 bus cycles and the high byte is read first. The 8-bit port uses the pins D7 to D0.

See table 11 and 12 and also section 6.2 for more detailed information on the programmable chip-selects and the dynamic bus sizing.

6.3.1 BUS SIZE REGISTER (BSREG)

Table 10 Bus Size Register (address FFFF A811H)

7	6	5	4	3	2	1	0
–	BS6	BS5	BS4	BS3	BS2	BS1	BS0

Table 11 Description of BSREG bits; see note 1

BIT	SYMBOL	DESCRIPTION
7	–	Reserved.
6 to 0	BS6 to BS0	Bus size for the data transfer with respect to the corresponding chip-select ($\overline{CSn}$): If BSn = 0, then the bus size is in 16-bit mode; note 2. If BSn = 1, then the bus size is in 8-bit mode.

Notes

1. n = 0 to 6.
2. The default value after a CPU reset.

Table 12 Bus size depending on BSIZE, CSBTX and BSn.

STATE OF PIN BSIZE	STATE OF BIT CSBTX	BUS SIZE OF CS0 TO CS6 DEPENDING ON BIT BSN IN REGISTER BSREG	BUS SIZE OF CSBT at boot/after boot	PORT PL AVAILABLE (PORT P0..P7)
0	0	BSN: 0 16 BIT 1 8 BIT	16/16	NO
0	1	BSN: 0 16 BIT 1 8 BIT	16/8	YES
1	0	BSN: 0 NOTE 1. 1 8 BIT	8/8	YES
1	1	BSN: 0 16 BIT 1 8 BIT	8/16	NO

Note 1:
The default value after reset of bits BSn (n=0 to 6) in register BSREG is 0 which corresponds to 16-bit mode for CS0 to CS6. In this case, it is recommended to set BSn to 1 in the boot routine. Afterwards if CSBTX is set to 1, BSn can be reset to 0 by software for further transfers in 16-bit mode.

6.4 System Control Register (SYSCON)

The P90CL301 uses a system control register SYSCON for adjusting system parameters. The content of this register is described below. The default values after a CPU-reset are marked with "*". All bits are reset by the reset-instruction, except the IDL bit which is only reset by a CPU-reset.

Table 13 System Control Register (address FFFF 8000H); see note 1

15	14	13	12	11	10	9	8	7[1]	6[1]	5	4	3	2	1[2]	0
WDSC	BPE	CSBTX	STBY	PCLK3	PCLK2	PDE	GF	PCLK1	PCLK0	IM	WD	FBC	PD	IDL	DOFF

Notes

1. The default values after a CPU-reset: PCLK1 = 1 and PCLK0 = 1; all the other bits = 0.
2. All bits are reset by the RESET instruction, except the IDL bit which is only reset by a CPU-reset.

Table 14 Description of SYSCON bits

BIT	SYMBOL	FUNCTION
15	WDSC	Bus error watchdog short cycle. 0* = Normal mode. The bus error watchdog counts 2048 periods before activating the bus error sequence. 1 = Bus error watchdog short cycle. The watchdog counts 16 periods before activating the bus error sequence.
14	BPE	Bus pull-up enable. 0* = Address, Data bus internal pull-ups switched off 1 = Address, Data bus internal pull-ups switched on
13	CSBTX	Invert bus size for chip select boot and mode of port P(0:7). 0* = Normal mode. Bus size is defined by the pin BSIZE. 1 = Chip select boot is defined by the inverted value of the pin BSIZE. The mode change should be executed from the internal RAM or from a memory activated by any other chip select than CSBTN. See also chapter on Dynamic port port sizing including chapter "Dynamic bus port sizing" for further details
12	STBY	CPU stand-by mode. 0* = Normal mode. 1 = Stand-by mode. Only the CPU clock is switched-off, the peripheral clocks are still running. (See fig. 6 Internal clock generation)
11	PCLK3	Prescaler for primary peripheral clock (FCLK) and the UART clock in mode 0. The CPU clock = CLK; FCLK = $^1/_{divisor}\times$ CLK.See Table 15 for divisor values.
10	PCLK2	Prescaler for secondary peripheral clock FCLK2 (derived from the primary peripheral clock FCLK), used for the ADC; the maximum value of the FCLK2 clock is dependent on the supply voltage V_{DD}; see Section 19. If PCLK = 0*, then FCLK is divided by 2; if If PCLK = 1, then FCLK is divided by 4.
9	PDE	If PDE = 0*, then bits A22 to A19 are in normal operation; If PDE =1, then bits A22 to A19 are used as 8051 peripheral chip-select $\overline{PCS3}$ to $\overline{PCS0}$.
8	GF	General purpose flag bit; reset to a logic 0 after CPU-reset.
7	PCLK1	Prescaler for primary peripheral clock (FCLK) and the UART clock in mode 0. The CPU clock = CLK; FCLK = $^1/_{divisor} \times$ CLK.See Table 15 for divisor values.
6	PCLK0	
5	IM	For IM = 0*, level 7 is loaded into the Status Register during interrupt processing to prevent the CPU from being interrupted by another interrupt source. For IM = 1, the current interrupt level is loaded into the Status Register allowing nested interrupts.
4	WD	For WD = 0*, the time-out for bus error detection is switched off. If the time-out is not used, the Watchdog timer can be used to stop a non-acknowledged bus transfer. For WD = 1, the time-out for bus error detection is activated. If no $\overline{DTACK}$ has been sent by the addressed device after 128 $\times$ 16 internal clock cycles the on-chip bus error signal is activated.
3	FBC	FBC = 0*, normal bus cycle; FBC = 1, fast bus cycle. An external read bus cycle can take a minimum of 3 clock periods; the minimum write cycle is still 4 clock periods; in order to get this access time $\overline{DTACK}$ should be asserted on time.
2	PD	PD = 0*, for normal mode; PD = 1, for Power-down mode (see Section 6.8).
1	IDL	IDL = 0*, for normal mode; IDL = 1, for Idle mode (see Section 6.8).
0	DOFF	DOFF = 0*, for normal mode. DOFF = 1, for delay counter off; if set at Wake-up from Power-down the delay counter waiting period is skipped.

Table 15 Prescaler divisor values

PCLK3	PCLK1	PCLK0	DIVISOR (D)	DIVISOR FOR UART IN MODE0
0	0	0	2	6
0	0	1	3	6
0	1	0	4	6
0*	1*	1*	5 (default value after a CPU-reset)	6
1	0	1	6	12
1	1	0	8	12
1	1	1	10	12

6.5 Reset operation

The reset circuitry of the P90CL301 is connected to the pins $\overline{\text{RESET}}$, $\overline{\text{HALT}}$, RESETIN and to the internal Watchdog timer. A Schmitt trigger is used at the input pin for noise rejection. After Power-on a CPU reset is accomplished by holding the $\overline{\text{RESET}}$ pin and the $\overline{\text{HALT}}$ pin LOW for at least 50 oscillator clocks after the oscillator has stabilized.

For further information on the clock generation, see Section 6.6. The CPU responds by reading the reset vectors, the long word at address 000000H is loaded into the Supervisor stack, the long word data at address 000004H is loaded into the program counter PC. The interrupt level is set to 7 in the Status Register and execution starts at the PC location. By pulling the $\overline{\text{RESET}}$ pin LOW and keeping $\overline{\text{HALT}}$ HIGH, only the peripherals are reset.

When V_{DD} is turned on and its rise time does not exceed 10 ms, an automatic reset can be performed by connecting the RESETIN pin to V_{DD} via an external capacitor. The external capacitor is charged via an internal pull-down resistor.

The $\overline{\text{RESET}}$ pin can also be pulled LOW internally by a pull-down transistor activated by an overflow of the Watchdog timer. When the CPU executes a RESET instruction, the $\overline{\text{RESET}}$ pin is pulled LOW. When the CPU is internally halted (at double bus fault), the $\overline{\text{HALT}}$ pin is pulled LOW and only a CPU reset can restart the processor.

The internal signal RESET_AS (Reset Asynchronous) resets the core and all registers.

When an internal Watchdog timer overflow occurs, an internal CPU reset is generated which resets all registers except the SYSCON, PCON, PRL and PRH registers and pulls the $\overline{\text{RESET}}$ pin LOW during 12 clock cycles.

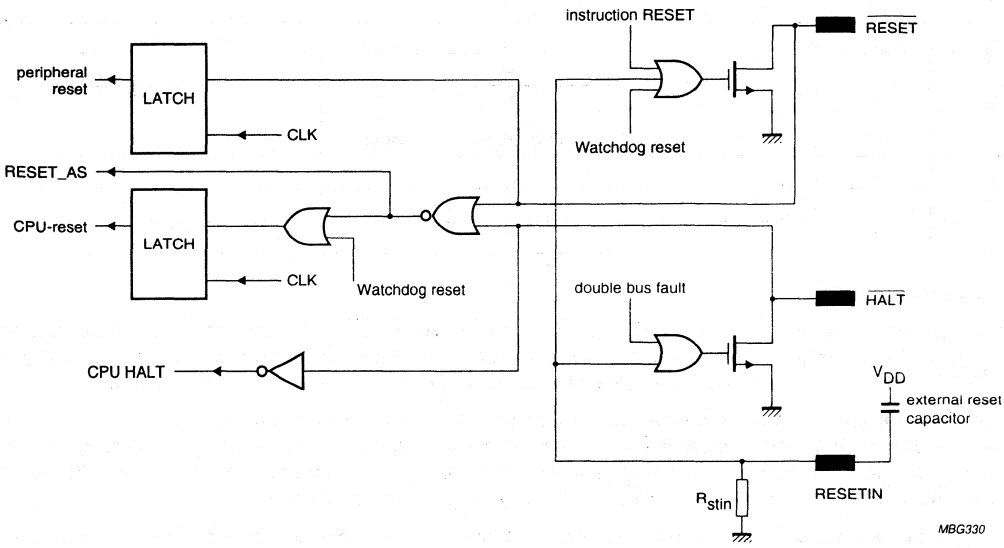


Fig.3 Reset circuitry.

6.6 Clock generation

The P90CL301 can be used where an external clock is available. The duty cycle of the external clock should be 50/50 ±5% over the full temperature and voltage range.

For peripherals like Watchdog timer, I²C, PWM, TIMER, and baud rate generator, a programmable prescaler generates a peripheral clock FCLK.

The prescaler is controlled by the System Control Register (SYSCON). The internal clock is divided by a factor 2, 3, 4, 5, 6, 8 or 10(function of bits PCLK0, PCLK1 and PCLK3; see Table 15).

For the ADC a secondary peripheral clock FCLK2 is derived from the peripheral clock by dividing it either by 4 or 2 (function of the bit PCLK2; see Table 14).

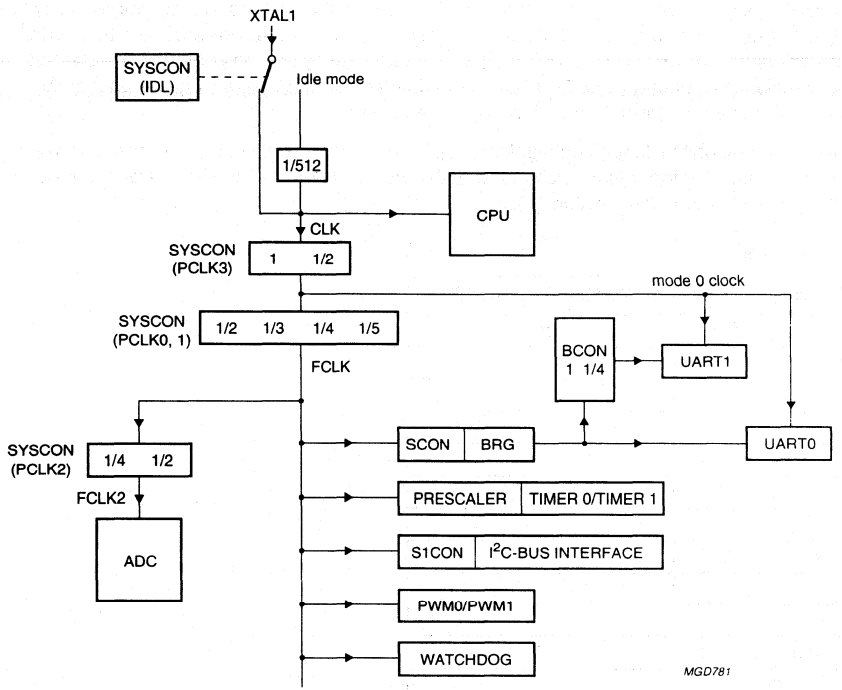


Fig.4 P90CL301 internal clock generation.

6.7 Interrupt controller

An interrupt controller handles all internal and external interrupts. It delivers the interrupt with the highest priority level to the CPU. The following interrupt requests are generated by the on-chip peripherals:

- I^2C
- UARTs: received data / transmitted data
- TIMERs: two flags for the timers T0 and T1

- ADC: analog-to-digital conversion completed.

The external interrupt requests are generated with the pins NMIN and the seven external interrupts $\overline{INT0}$ to $\overline{INT6}$.

6.7.1 INTERRUPT ARBITRATION

The interrupt priority levels are programmable with a value between 0 and 7. Level 7 has the highest priority, level 0 disables the corresponding interrupt source. In case of interrupt requests of equal priority level at the same time a hardware priority mechanism gives priority order as shown in Table 16.

The execution of interrupt routines can be interrupted by another interrupt request of a higher priority level. In 68070 mode (in SYSCON bit IM = 1) when an interrupt is serviced by the CPU, the corresponding level is loaded into the Status Register. This prevents the current interrupt from getting interrupted by any other interrupt request on the same or a lower priority level. If IM is reset, priority level 7 will always be loaded into the Status Register and so the current interrupt cannot be interrupted by an interrupt request of a level less than 7.

Each on-chip peripheral unit including the eight interrupt lines generates only auto-vectored interrupts. No acknowledge is necessary. For external interrupts the vectors 25 to 31 are used, for on-chip peripheral circuits a second table of 7 vectors are used (57 to 63); see Section 7.3.2.

Table 16 Priority order

SIGNAL	PRIORITY ORDER
NMIN	highest
$\overline{INT6}$	
$\overline{INT5}$	
$\overline{INT4}$	
$\overline{INT3}$	
$\overline{INT2}$	
$\overline{INT1}$	
$\overline{INT0}$	
I^2C	
ADC	
UART1 receiver	
UART1 transmitter	
UART0 receiver	
UART0 transmitter	
TIMER 1	
TIMER 0	lowest

6.7.2 EXTERNAL LATCHED INTERRUPTS

NMIN and $\overline{INT0}$ to $\overline{INT6}$ are 8 external interrupt inputs. These pins are connected to the interrupt function only when the corresponding bit in the SPCON control register is set (see SP port description chap. 8). Seven interrupt inputs $\overline{INT0}$ to $\overline{INT6}$ are edge sensitive on HIGH-to-LOW transition and their priority levels are programmable.
The interrupt NMIN is non-maskable (except if it is programmed as a port) and is edge sensitive on HIGH-to-LOW transition. The priority level of NMIN is fixed to 7.

The external interrupts are controlled by the registers LIR0 to LIR3; see Tables 17 and 18.

6.7.2.1 Latched Interrupt Registers (LIR0 to LIR3)

Table 17 Latched Interrupt Registers

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
FFF 8101H	LIR0	PIR1	IPL1.2	IPL1.1	IPL1.0	PIR0	IPL0.2	IPL0.1	IPL0.0
FFF 8103H	LIR1	PIR3	IPL3.2	IPL3.1	IPL3.0	PIR2	IPL2.2	IPL2.1	IPL2.0
FFF 8105H	LIR2	PIR5	IPL5.2	IPL5.1	IPL5.0	PIR4	IPL4.2	IPL4.1	IPL4.0
FFF 8107H	LIR3	PIR7	1	1	1	PIR6	IPL6.2	IPL6.1	IPL6.0

Table 18 Description of LIR0 to LIR3 bits

BIT	SYMBOL	FUNCTION
7 and 3	PIRn	Pending interrupt request. n = 0 to 7; INT7 corresponds to the interrupt NMIN; PIRn = 1, pending interrupt request for pin $\overline{\text{INT}}$n; PIRn = 0* note 1, no pending interrupt; note 2
6 to 4 2 to 0	IPLm.2 to IPLm.0	Interrupt priority level of pins $\overline{\text{INT0}}$ to $\overline{\text{INT6}}$ (fixed to 111 for NMIN in LIR3); m = 0 to 6.

Notes

1. The default value after a CPU-reset.
2. When a valid interrupt request has been detected this bit is set. It is automatically reset by the interrupt acknowledge cycle from the CPU. It can be reset by software by writing a logic 0, however writing a logic 1 has no effect on the flag. To reset only one flag, a logic 0 should be written to the bit address and a logic 1 to the other interrupt requests. The use of BCLR instruction should be avoided (PIR7 is cleared when the pin NMIN is set HIGH).

6.7.2.2 Pending Interrupt Flag register (PIFR)

An additional register PIFR (Pending Interrupt Flag register) contains copies of the PIR flags.

The PIF flag are set at the same time as the PIR flag when an interrupt is activated, but these flags are not reset automatically during the interrupt acknowledge cycle. They can only be cleared by software and keep a trace of the interrupt event.

The detection of an external interrupt is indicated by the corresponding PIF-bit being set to 1.

Table 19 Pending Interrupt Flag Register PIFR (address FFFF 810F)

7	6	5	4	3	2	1	0
PIF7	PIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0

6.7.3 NOTE ON SIMULTANEOUS INTERRUPTS

If an internal interrupt is immediately followed by an external interrupt (i.e. both interrupts occurring within 12 clock cycles) and both these interrupts have the same interrupt level, then the CPU might hang up during the acknowledge cycle of the internal interrupt.

In the interrupt controller a flag WIN is set for each interrupt as soon as the interrupt is activated and will be reset when an interrupt of higher priority occurs or during the acknowledge cycle. The WIN flag is used to determine which PIR flag should be reset.

A conflict occurs if within the interval starting at the CPU sampling of the first internal interrupt and ending at the acknowledge cycle, a second external interrupt resets the WIN flag of the first interrupt (external interrupt have higher

priority than internal). When the CPU acknowledges the first internal interrupt the autovector acknowledge signal cannot be asserted as its WIN flag was reset, and the CPU hangs up.

This situation can be solved by using the bus time-out counter controlled by the system control register SYSCON with the bits WD and WDSC set. In the case of hang-up an internal bus error condition will be asserted after 16 clocks and the CPU will execute the exception SPURIOUS INTERRUPT at vector 60h. In the exception service routine the interrupt flags PIR should be polled to detect which interrupts caused the conflict, the corresponding PIR flags should be cleared by software and a call to the interrupt routines executed.

6.8 Power reduction modes

The P90CL301 supports three power reduction modes. A Power-down mode were the clock is frozen, a standby mode where only the CPU is stopped, and an Idle mode were the external clock is divided by 512 (see Fig.4).

6.8.1 POWER-DOWN MODE

The Power-down operation freezes the oscillator. It can only be activated by setting the PD bit in the SYSCON register and thereafter execute the STOP instruction.

The instruction flow to enter the Power-down mode is:

```
BSET #PD, SYSCON
STOP #$2700.
```

In this state all the register contents are preserved. The CPU remains in this state until an internal reset occurs or a LOW level is present on any of the external interrupt pins $\overline{INT0}$ to $\overline{INT6}$ or NMIN. If the Wake-up is done via an external interrupt, the processor will first execute an external interrupt of level 7. If the IPL level in the LIR register is set to 7, a second interrupt of level 7 will be executed. It is preferable to set the IPL to 0.

In Power-down mode V_{DD} may be reduced to minimize power consumption. However, the supply voltage must not be reduced until Power-down mode is active, and must be restored before a external reset or an interrupt is activated.

In case of an external reset, the pin should be held active until the external oscillator has restarted and stabilized.

In case of an external interrupt Wake-up, any $\overline{INTn}$ or NMIN pin should go LOW and the corresponding bit ESn (n= 0 to 7) in register SPCON should be set. If the DOFF bit in the SYSCON is not set, an internal delay counter ensures that the internal clock is not active before 1536 clock cycles. After that time the oscillator is stable and normal exception processing can be executed. The PD bit is cleared automatically during the wake-up.

In order to have a fast start-up the DOFF bit should be set, switching off the delay counter and enabling the immediate clocking and restart of the controller.

For minimum power consumption during Power-down mode, the address and data pins should be pulled HIGH externally or bit BPE in register SYSCON should be set (i.e. internal pull-ups enabled).

6.8.2 STANDBY MODE

When the bit STBY is set in the system control register, the CPU clock is stopped and the status of the processor is frozen, however the clocks of all other on-chip peripherals are still running at the nominal frequency like:

- Timers
- External and internal interrupts
- UARTs and baud rate generator
- IIC bus interface
- Watchdog
- PWMs
- ADC

The CPU exits this mode when an internal or external interrupt is activated, and proceeds with the normal program execution.

For minimum power consumption internal pull-ups on address and data buses can be switched-on by setting the control bit BPE in the SYSCON register. The pull-ups should be switched-off in normal mode if not needed.

6.8.3 IDLE MODE

In the Idle mode the crystal or external clock is divided by a factor 512. The current is reduced drastically but the controller continues to operate. This mode is entered by setting the bit IDL in the SYSCON register. The next instruction will be executed at a slower speed. To return to normal mode the IDL bit should be reset.

It should be noted that all peripheral functions are also slowed down, and some cannot be used normally for example UART, I^2C, ADC and PWM. The Power-down mode can also be entered from the Idle mode. After a Wake-up the controller restarts in Idle mode.

7 CPU FUNCTIONAL DESCRIPTION

7.1 General

The CPU of the 90CL301 is software compatible with the Motorola MC68000, hence programs written for the MC68000 will run on the 90CL301 without modifications. However, for certain applications the following differences between processors should be noted:

- Differences exist in the address/bus error exception processing since the 90CL301 can provide full error recovery.
- The timing is different for the P90CL301 due to a new internal architecture and technology. The instruction execution timing is different for the same reasons.

7.2 Programming model and data organization

The programming model is identical to the MC68000 one as shown below with seventeen 32-bit registers, a 32-bit Program Counter and a 16-bit Status Register. The eight data registers (D0 to D7) are used for byte, word and long-word operations. The address registers (A0 to A6) and the system stack pointer A7 can be used as software stack pointers and base address registers. In addition, these registers can be used for word and long-word address operations. All seventeen registers can be used as index registers.

The 90CL301 supports 8, 16 and 32-bit integers as well as BCD data and 32-bit addresses. Each data type is arranged in the memory as shown in Fig.6.

Table 20 Format of the Status Register and description of the bits; r = reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T	–	S	–	–	12	11	10	–	–	–	X	N	Z	V	C
Trace mode	r	Supervisor	r		Interrupt mask			r			Extend	Negative	Zero	Overflow	Carry

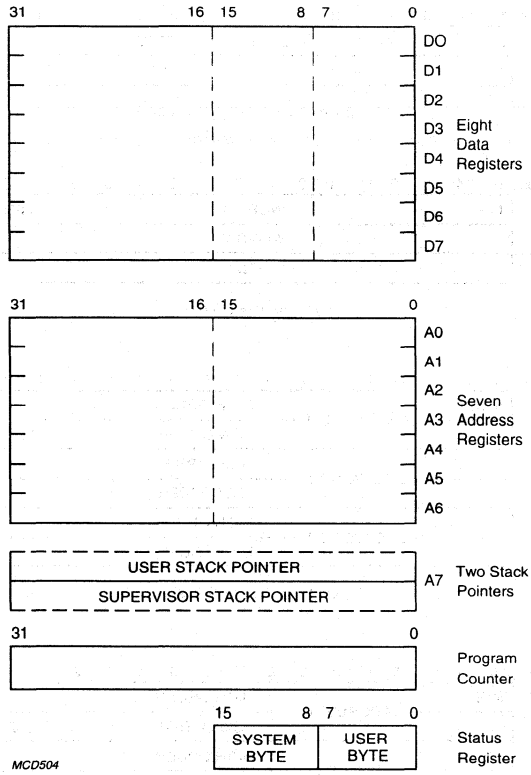


Fig.5 Programming model.

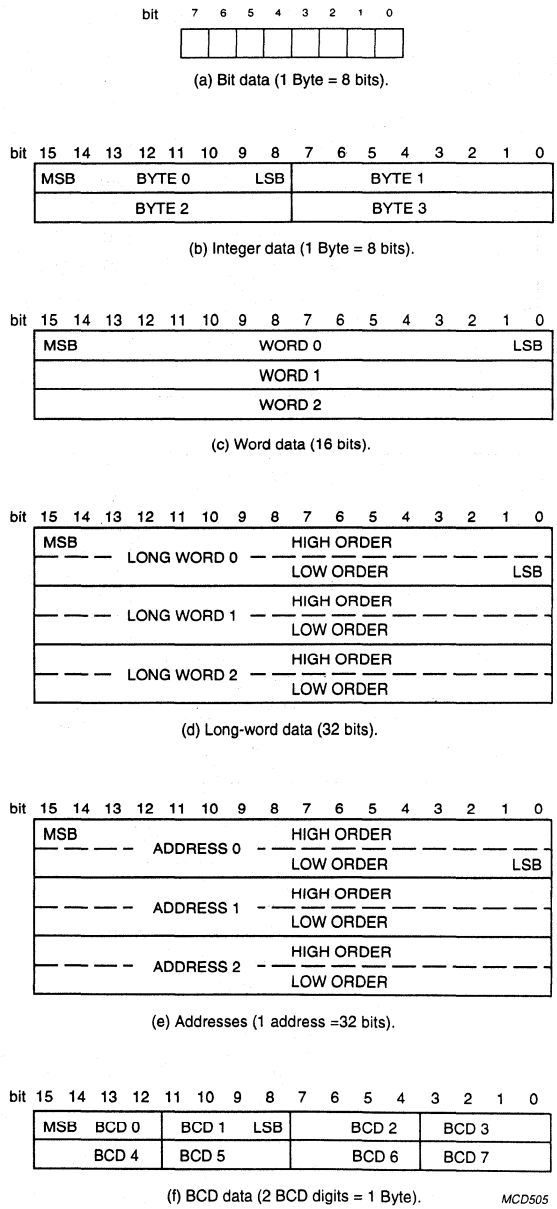


Fig.6 Memory data organization.

7.3 Processing states and exception processing

The 90CL301 operates with a maximum internal clock frequency of 27 MHz down to static operation. Each clock cycle is divided into 2 states. A non-access machine cycle has 3 clock cycles or 6 states (S0 to S5). A minimum bus cycle normally consists of 3 clock cycles (6 states). When $\overline{DTACK}$ is not asserted, indicating that data transfer has not yet been terminated, wait states (WS) are inserted in multiples of 2.

The CPU is always in one of the four processing states:

- Normal,
- Exception,
- Halt,
- Stopped.

The Normal processing state is associated with instruction execution; the memory references fetch instructions or load/save results. A special case of the Normal state is the Stopped state which is entered by the processor when a STOP instruction is executed. In this state the CPU does not make any further memory references.

The Exception state is associated with interrupts, trap instruction, tracing and other exceptional conditions. The exception may be generated internally by an instruction or by any unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt or by reset.

The halted processing state is an indication of a catastrophic hardware failure. For example, if during exception processing of a bus error another bus error occurs, the CPU assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a CPU in the stopped state is not in the halted state or vice versa.

The Supervisor can work in the User or Supervisor state determined by the state of bit S in the Status Register. Accesses to the on-chip peripherals are achieved in the Supervisor state.

All exception processing is performed in the Supervisor state once the current contents of the Status Register has been saved. Then the exception vector number is determined and copies of the Status Register, the program counter and the format/vector number are saved on the Supervisor stack using the Supervisor Stack Pointer (SSP). Finally the contents of the exception vector location is fetched and loaded into the Program Counter (PC).

7.3.1 Reference classification

When the processor makes a reference, it classifies the kind of reference being made, using the encoding of the three function code internal lines. This allows external translation of addresses, control of access, and differentiation of special processor states, such as interrupt acknowledge. Table 21 shows the classification of references.

Table 21 Reference classification

FUNCTION CODE			REFERENCE CLASS
FC2	FC1	FC0	
0	0	0	unassigned
0	0	1	User Data
0	1	0	User Program
0	1	1	unassigned
1	0	0	unassigned
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	interrupt acknowledge

7.3.2 EXCEPTION VECTORS

Exception vectors are memory locations from where the CPU fetches the address of a routine that will handle that exception. All exception vectors are 2 words long, except for the reset vector which consists of 4 words, containing the PC and the SSP. All exception vectors are in the Supervisor Data space.

A vector number is an 8-bit number which, multiplied by 4, gives the address of an exception vector. Vector numbers are generated internally. The memory map for the exception vectors is shown in the Table 22.

Table 22 Exception vector assignment

VECTOR NO.	DEC	HEX	ASSIGNMENT
0	0	000	reset: initial SSP
–	4	004	reset: initial PC
2	8	008	bus error
3	12	00C	address error
4	16	010	illegal instruction
5	20	014	zero divide
6	24	018	CHK instruction
7	28	01C	TRAPV instruction
8	32	020	privilege violation
9	36	024	trace
10	40	028	line 1010 emulator
11	44	02C	line 1111 emulator
12[1]	48	030	unassigned, reserved
13[1]	52	034	unassigned, reserved
14	56	038	format error
15	60	03C	uninitialized interrupt vector
16 to 23[1]	64 to 95	040 to 05C	unassigned, reserved
24	96	060	spurious interrupt
25	100	064	level 1 external interrupt auto-vector
26	104	068	level 2 external interrupt auto-vector
27	108	06C	level 3 external interrupt auto-vector
28	112	070	level 4 external interrupt auto-vector
29	116	074	level 5 external interrupt auto-vector
30	120	078	level 6 external interrupt auto-vector
31	124	07C	level 7 external interrupt auto-vector
32 to 47	128 to 191	080 to 0BF	TRAP instruction vectors
48 to 56[1]	192 to 227	0C0 to 0E3	reserved
57	228	0E4	level 1 on-chip interrupt auto-vector
58	232	0E8	level 2 on-chip interrupt auto-vector
59	236	0EC	level 3 on-chip interrupt auto-vector
60	240	0F0	level 4 on-chip interrupt auto-vector
61	244	0F4	level 5 on-chip interrupt auto-vector
62	248	0F8	level 6 on-chip interrupt auto-vector
63	252	0FC	level 7 on-chip interrupt auto-vector
64 to 255	256 to 1023	100 to 3FF	reserved

Note

1. Vectors 12, 13, 16 to 23 and 48 to 56 are reserved for future enhancements.

7.3.3 INSTRUCTION TRAPS

Traps are exceptions caused by instructions arising from CPU recognition of abnormal conditions during instruction execution or from instructions whose normal behaviour is to cause traps.

Some instructions are used specifically to generate traps. The TRAP instruction always forces an exception and is useful for implementing system calls for User Programs. The TRAPV and CHK instructions force an exception if the User Program detects a run-time error, possibly an arithmetic overflow or a subscript out of bounds. The signed divide (DIVS) and unsigned divide (DIVU) instructions will force an exception if a divide-by-zero operation is attempted.

7.3.4 ILLEGAL AND UNIMPLEMENTED INSTRUCTIONS

Illegal instruction is the term used to refer to any word that is not the first word of a legal instruction. During execution, if such an instruction is fetched an illegal exception occurs.

Words with bits 15 to 12 equal to '1010' or '1111' are defined as unimplemented instructions and separate exception vectors are allocated to these patterns for efficient emulation. This facility means the operating system can detect program errors, or can emulate unimplemented instructions in software.

7.3.5 PRIVILEGE VIOLATIONS

To provide system security, various instructions are privileged and any attempt to execute one of the privileged instruction while the CPU is in the User state provokes an exception. The privileged instructions are:

- STOP
- RESET
- RTE
- MOVE to SR
- AND (word) immediate to SR
- EOR (word) immediate to SR
- OR (word) immediate to SR
- MOVE to USP.

7.4 Tracing

The CPU includes a facility to trace instructions one by one to assist in program development. In the trace state, after each instruction is executed, an exception is forced so that the debugging program can monitor execution of the program under test.

The trace facility uses the T-bit in the Supervisor part of the Status Register. If the T-bit is cleared, tracing is disabled and instructions are executed normally. If the T-bit is set at the beginning of the execution of an instruction, a trace exception will be generated once the instruction has been executed. If the instruction is not executed, either because of an interrupt, or because the instruction is illegal or privileged, the trace exception does also not occur if the instruction is aborted by a reset, bus error, or address error exception. If the instruction is executed, and an interrupt is pending, the trace exception is processed before the interrupt. If the execution of an instruction forces an exception, the forced exception is processed before the trace exception.

As an extreme illustration of the above rules, consider the arrival of an interrupt during the execution of a TRAP instruction, while tracing is enabled. First the trap exception is processed, followed by the trace exception, and finally the interrupt handling routine.

7.5 Stack format

The stack format for exception processing is similar to the MC68010 although the instruction stored is not the same, due to the different architecture. To handle this format the 90CL301 differs from the MC68000 in that:

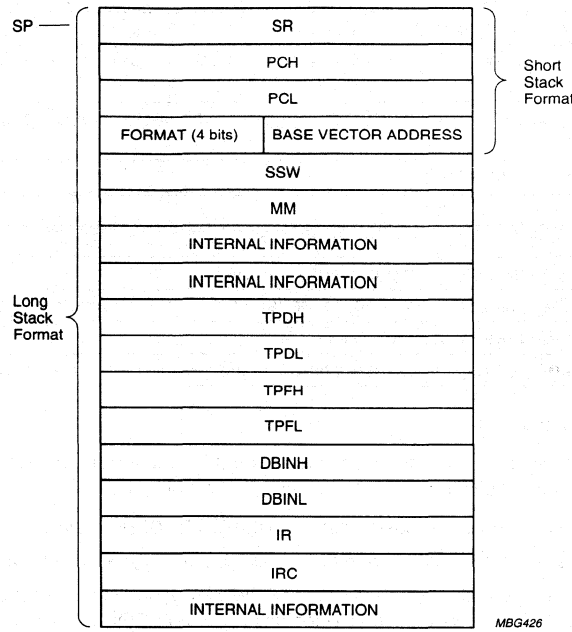


Fig.7 Stack format; see Table 23.

- The stack format is changed.
- The minimum number of words put into or restored from stack is 4 (MC68010 compatible, not 3 as with the MC68000).
- The RTE instruction decides (with the aid of the 4 format bits) whether or not more information has to be restored as follows:
  - The 90CL301 long format is used for bus errors and address error exceptions.
  - All other exceptions use the short format.
- If another format code, other than those listed above, is detected during the restored action, a FORMAT ERROR occurs.

If the user wants to finish the instruction in which the bus or address error occurred, the 90CL301 format must be used on RTE. If no changes to the stack are required during exception processing, the stack format is transparent to the user.

Table 23 Description of the stack format

SYMBOL	DESCRIPTION
SR	Status Register
PCH/PCL	Program Counter High/Low Word
FORMAT	Indicating either a short stack (only the first four words), or the long for bus and address error exceptions
BASE VECTOR ADDRESS	The base vector address of the exception in the vector table; e.g. 8 for a bus error and 12 for an address error
SSW	Special Status Word
MM	Current Move Multiple Mask
TPDH/TPDL	In the event of faulty write cycle, the data can be found here
TPFH/TPFL	The address used during the faulty bus cycle
DBINH/DBINL	Data that has been read prior to the faulty bus cycle can in some cases be found here
IR	Holds the present instruction executed
IRC	Holds either the present instruction executed or the prefetched instruction

7.6 CPU interrupt processing

The general interrupt handling mechanism is described in Section 6.7. An interrupt controller handles all interrupts, resolves the priority problem and passes the highest level interrupt to the CPU.

The CPU interrupt handling follows the same basic rules as in the MC68000. However, some remarks must be made:

- Interrupts with a priority level equal to or lower than the current priority level will not be accepted.
- During the acknowledge cycle of an interrupt, the IPL bits of the Status Register are set to the priority of the acknowledged interrupt or to 7. An exception occurs when bit IM = 0 (SYSCON bit 5). In this case level 7 is loaded into the Status Register (see Section 6.4; Table 14).

If the priority level of the pending interrupt is greater than the current processor priority then:

- The exception processing sequence is started.
- A copy of the Status Register is saved.
- The privilege level is set to Supervisor state.
- Tracing is suppressed.
- The priority level of the processor is set to that of the interrupt being acknowledged or to 7 depending on the IM flag in the System Control Register.

The processor then gets the vector number from the interrupting device, classifies it as an interrupt acknowledge and displays the interrupt level number being acknowledged on the internal address bus.

As all 90CL301 interrupts are auto-vectored, the processor internally generates a vector number corresponding to the interrupt level number.

The processor starts normal exception processing by saving the format word, program counter and Status Register on the Supervisor stack. The value of the vector in the format word is an internally generated vector number multiplied by 4 (format is all zeros). The program counter value is the address of the instruction that would have been executed if the interrupt had not been present. Then the interrupt vector contents are fetched and loaded into the program counter. The interrupt handling routine starts with normal instruction execution.

7.7 Bus arbitration

If the $\overline{\text{HALT}}$ pin is held LOW with $\overline{\text{RESET}}$ HIGH the CPU will stop after completion of the current bus cycle. As long as $\overline{\text{HALT}}$ is LOW, all control signals are inactive and all tri-state lines are placed in the high-impedance state. If the $\overline{\text{HALT}}$ pin is held LOW during the transfer of a word in 8-bit mode, the CPU will continue the transfer of the two bytes before it halts.

8 PORTS

16-bit bidirectional port lines P15 to P0 and 8-bit port lines SP7 to SP0 can be used for general purpose input/output operations. All port pins are multiplexed with other functions, but each one can be individually switched to the port function by setting the corresponding bit in the port control registers PCON for P and SPCON for SP.

The port P7 to P0 is multiplexed with the data bus D15 to D8 and is selected by the pin BSIZE. Each port pin consists of a latch, an output driver with pull-ups and an input buffer.

To use the port as input the port latch should be written with a logic 1. This means only a weak pull-up is on and can be overwritten by an external source logic 0. When outputting a logic 1, a strong pull-up is turned on only for 1 clock period, and then only the weak pull-up maintains the HIGH level. In read mode, two different internal addresses correspond to the port latch or the port pin.The port values are read via register PPL and PPH.

After reset all ports are initialized as input, and the pins are connected to the port latch with exception for the pin NMIN/SP7 which is connected to the interrupt block.

8.1 Port P Control Register (PCON)

The Port P is controlled via the Port Control Register (PCON). The register PCON is only reset by an external reset, and not by the RESET instruction. The port latches are accessed through the registers PRL and PRH.

Table 24 Port Control Register (address FFFF 8503H)

7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E09	E08

Table 25 Description of PCON bits

BIT	SYMBOL	FUNCTION
7 to 0	E15 to E08	If En = 0, then Portn is enabled; En = 1 then alternate function enabled (n = 08 to 15). The default value after reset is logic 0.

8.1.1 Port Latches (PRL and PRH)

Table 26 Port Latches

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
FFFF 8505H	PRL	P7	P6	P5	P4	P3	P2	P1	P0
FFFF 8509H	PRH	P15	P14	P13	P12	P11	P10	P9	P8

8.2 Port SP

The Special Port (SP) includes 8 I/O lines and is controlled via the two registers SPCON and SPR. The registers SPCON and SPR are reset also by a peripheral reset. The port latch is accessed through the register SPR.

8.2.1 Port SP Control Register (SPCON)

Table 27 Port SP Control Register (FFFF 8109H)

7	6	5	4	3	2	1	0
ES7	ES6	ES5	ES4	ES3	ES2	ES1	ES0

Table 28 Description of SPCON bits

BIT	SYMBOL	FUNCTION
7 to 0	ES7 to ES0	If ESn = 0, then Portn is enabled; if ESn = 1, then the alternate function is enabled; n = 0 to 7. The default value after reset is logic 0, except for ES7 which is set at reset.

Table 29 SP port latch (FFFF 810BH)

7	6	5	4	3	2	1	0
SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Table 30 Alternate functions for P and SP pins.
Functions within brackets are parallel functions.

PORT PIN	ALTERNATE FUNCTION
P0	D8
P1	D9
P2	D10
P3	D11
P4	D12
P5	D13
P6	D14
P7	D15
P8	PWM0 (CP0)
P9	PWM1 (CP1)
P10	SCL
P11	SDA
P12	ADC0
P13	ADC1
P14	ADC2
P15	ADC3
SP0	RX1/$\overline{\text{INT0}}$
SP1	TX1/$\overline{\text{INT1}}$ (CLK0)
SP2	RX0/$\overline{\text{INT2}}$ (CP2)
SP3	TX0/$\overline{\text{INT3}}$ (CP3)
SP4	$\overline{\text{INT4}}$ (CP4)
SP5	$\overline{\text{INT5}}$ (CP5)
SP6	$\overline{\text{INT6}}$ (CLK1)
SP7	NMIN

9 8051 PERIPHERAL BUS

The P90CL301 can also directly access the peripheral circuits which are compatible with the 8048/8051 bus.

When the CPU accesses locations located in the 64 kbytes peripheral space, an Address/Data multiplexed access is generated using the AD0 to AD7 lines, the non-multiplexed A8 to A15 lines and the 8051 control bus (ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$). In order to use these three signals the alternate mode of the $\overline{\text{CS5}}$ to $\overline{\text{CS3}}$ should be set. A 8051 bus access is performed

by addressing a byte in the 8001 0000H to 8001 FFFFH range. To reduce the number of interface circuits, the address lines A22 to A19 can be used as peripheral chip-select outputs $\overline{PCS0}$ to $\overline{PCS3}$. This is done by setting the PDE bit (SYSCON) to a logic 1;

- $\overline{PCS0}$ selects memory range 0 kbytes to 16 kbytes
- $\overline{PCS1}$ selects memory range 16 kbytes to 32 kbytes
- $\overline{PCS2}$ selects memory range 32 kbytes to 48 kbytes
- $\overline{PCS3}$ selects memory range 48 kbytes to 64 kbytes.

The timing of the peripheral bus is fixed and compatible with the 8051 peripheral circuits.

10 ON-CHIP PERIPHERAL FUNCTIONS

The P90CL301 integrates a number of peripheral functions connected to the internal bus:

- Timers (T0 and T1)
- Watchdog
- 2 UART interfaces with one UART queue controller using the internal RAM as data buffers.
- I²C-bus interface
- PWM (Pulse Width Modulation)
- ADC (analog-to-digital converter).

These functions are accessible as memory locations on a byte or word basis. The access is auto-acknowledged by on-chip logic. The on-chip peripheral functions can generate auto-vectored interrupts to the CPU using the second vector table (vectors 57 to 63).

10.1 Peripheral interrupt control

The timers T0 and T1, I²C-bus, UART and ADC use a common set of Peripheral Interrupt Control Registers (PICR). These registers are accessible from the CPU and contain the interrupt priority level IPL2 to IPL0 as well as the pending interrupt flags PIR.

PIR is set when a valid interrupt request has been detected. It is automatically reset by the interrupt acknowledge cycle from the CPU. The PIR flag can be reset by software.

The code 111 in IPL represents the interrupt with the highest priority. The code 000 inhibits the interrupt.

10.1.1 Timer Interrupt Register (PICR0)

On timer overflow or on channel capture/match the pending interrupt request flag PIRTn is set. If the interrupt priority level is different from zero, the timer activates an interrupt to the CPU.

Table 31 Timer Interrupt Register (address FFFF 8701H)

7	6	5	4	3	2	1	0
PIRT1	IPLT1.2	IPLT1.1	IPLT1.0	PIRT0	IPLT0.2	IPLT0.1	IPLT0.0

Table 32 Description of PICR0 bits

BIT	SYMBOL	FUNCTION
7	PIRT1	pending interrupt for timer T1

BIT	SYMBOL	FUNCTION
6 to 4	IPLT2.2 to IPLT1.0	interrupt priority level for timer T1
3	PIRT0	pending interrupt for timer T0
2 to 0	IPLT0.2 to IPLT0.0	interrupt priority level for timer T0

10.1.2 UART Interrupt Registers

Each UART can generate two interrupts in transmission and reception via the two registers PICR1 and PICR2.

Table 33 UART Interrupt Registers PICR1 and PICR2

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
FFFF 8703H	PICR1	PIRR0	IPLR0.2	IPLR0.1	IPLR0.0	PIRT0	IPLT0.2	IPLT0.1	IPLT0.0
FFFF 8705H	PICR2	PIRR1	IPLR1.2	IPLR1.2	IPLR1.2	PIRT1	IPLT1.2	IPLT1.1	IPLT1.0

Table 34 Description of PICR1 and PICR2 register bits; n = 0 to 1.

BIT	SYMBOL	FUNCTION
7	PIRRn	pending interrupt for UARTn in reception
6 to 4	IPLRn.2 to IPLRn.0	interrupt priority level for UARTn in reception
3	PIRTn	pending interrupt for UARTn in transmission
2 to 0	IPLTn.2 to IPLTn.0	interrupt priority level for UARTn in transmission

10.1.3 I^2C and ADC Interrupt Register (PICR3)

The I^2C and the ADC can each generate one interrupt.

Table 35 I^2C and ADC Interrupt Register (address FFFF 8707H)

7	6	5	4	3	2	1	0
PIRI	IPLI2	IPLI1	IPLI0	PIRA	IPLA2	IPLA1	IPLA0

Table 36 Description of PICR3 bits

BIT	SYMBOL	FUNCTION
7	PIRI	pending interrupt for I^2C
6 to 4	IPLI2 to IPLI0	interrupt priority level for I^2C
3	PIRA	pending interrupt for ADC
2 to 0	IPLA2 to IPLA0	interrupt priority level for ADC

11 TIMERS

11.1 Timer array

Two identical 16-bit timer blocks are provided:

- Timer 0 (T0)
- Timer 1 (T1).

Each timer block consists of:

- a timebase,
- three capture/compare channels,
- a Control Register and
- a Status Register.

11.2 Timebase

The timebase contains an 8-bit prescaler with a write only reload register, and a 16-bit counter register. This counter register can only be read by software. The prescaler is clocked either by the peripheral clock FCLK or by an external clock enabled by the flag C/TN in the timer control register TnCR (T0CT for timer T0 and T1CR for timer T1). On prescaler overflow the prescaler reload value is loaded into the prescaler, which starts incrementing.

The 16-bit counter register is incremented at each prescaler overflow. When the counter reaches FFFFh, the status flag TOV is set and on the next clock the counter reload value is loaded into the counter. By resetting the control bit RUN in the timer control register the timebase is stopped, and by setting this bit, the prescaler and counter are reloaded and incremented on the next external or internal clock.

11.3 Channel function

Each channel consists of a register and an equality comparator. For each of the three channels two modes can be selected:

- **Compare mode:** sets the status flag CFn in TnSR when there is a match between the counter register and the channel register value.
- **Capture mode:** stores the counter register value into the channel register and sets the status flag CF when a transition occurs at the corresponding input pin CPn.

In both modes, each channel can generate a global interrupt request if the corresponding enable bit in the Control Register TnCR is set.

11.4 Pin parallel functions for the timer

In order to use the multiplexed pins for the timer, the other functions using these pins as output pins should be forced HIGH via a weak pull-up, enabling an external source to drive them LOW.

Table 37 Parallel functions

PIN	SETTING	PARALLEL FUNCTION
SP1/TX1/$\overline{\text{INT1}}$	if SPCON.1 = 0, SPR.1 = 1; else UART1 should not be used	CLK0
SP2/RX0/$\overline{\text{INT2}}$	if SPCON.2 = 0, SPR.2 = 1; else UART0 should not be used	CP2
SP3/TX0/$\overline{\text{INT3}}$	if SPCON.3 = 0, SPR.3 = 1; else UART0 should not be used	CP3
SP4/$\overline{\text{INT4}}$	if SPCON.4 = 0, SPR.4 = 1	CP4
SP5/$\overline{\text{INT5}}$	if SPCON.5 = 0, SPR.5 = 1	CP5

PIN	SETTING	PARALLEL FUNCTION
SP6/$\overline{INT6}$	if SPCON.6 = 0, SPR.6 = 1	CLK1
P8/PWM0	if PCON.0 = 0, PWM0 should output a logic 1 (write 00H to register PWM0)	CP0
P9/PWM1	if PCON.1 = 0, PWM1 should output a logic 1 (write 00H to register PWM1)	CP1

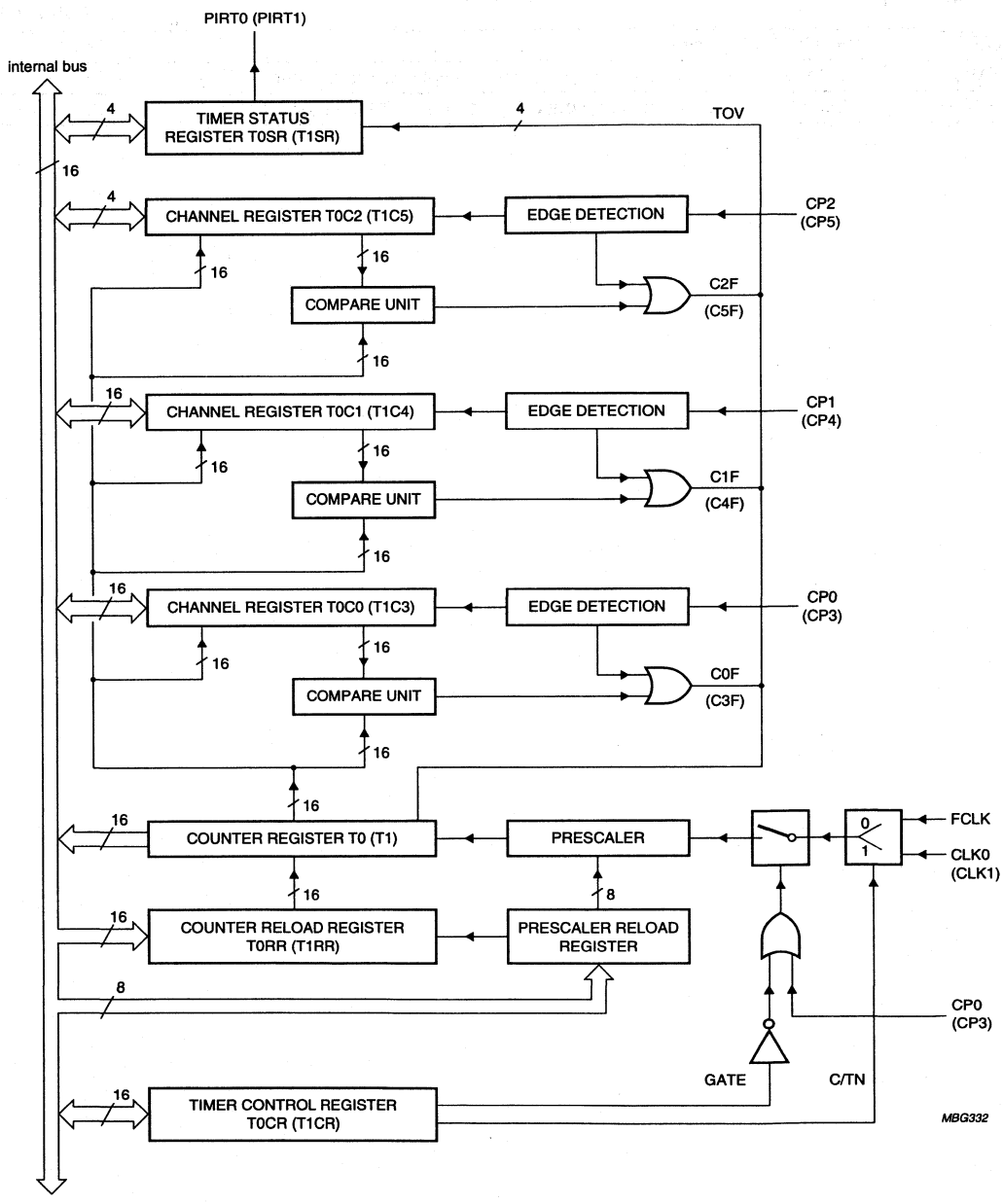


Fig.8 Timer block diagram T0 (identical with timer block T1, corresponding names indicated within brackets).

11.5 Timer Control Registers

The Timer 0 (T0) is controlled via Timer 0 Control Registers (T0CRH and T0CRL), and Timer 1 (T1) via Timer 1 Control Registers (T1CRH and T1CRL); see Fig.8 and Tables 38 to 41.

Table 38 Timer Control Registers T0CRH and T1CRH; see note 1

ADDRESS	REGISTER	15	14	13	12	11	10	9	8
FFFF 8300H	T0CRH	ECM2	C2M2	C2M1	C2M0	ECM1	C1M2	C1M1	C1M0
FFFF 8310H	T1CRH								

Table 39 Timer Control Registers T0CRL and T1CRL; see note 1

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
FFFF 8301H	T0CRL	ECM0	C0M2	C0M1	C0M0	ETOV	GATE	C/TN	RUN
FFFF 8311H	T1CRL								

Note to Tables 38 and 39

1. The default value after a CPU-reset for all bits is a logic 0.

Table 40 Description of T0CRH; T1CRH; T0CRL and T1CRL bits

BIT	SYMBOL	DESCRIPTION
15, 11 and 7	ECM2 to ECM0	Channel n interrupt enable (n = 0 to 2); ECMn = 0[1], the channel n interrupt is disabled; ECMn = 1, the channel n interrupt is enabled.
14 to 12	C2M2 to C2M0	Channel mode; see Table 41.
10 to 8	C1M2 to C1M0	
6 to 4	C0M2 to C0M0	
3	ETOV	Timer overflow interrupt enable; ETOV = 0[1], the timer overflow interrupt is disabled; ETOV = 1, the timer overflow interrupt is enabled.
2	GATE	Gated external clock; GATE = 0[1], disable gate function; GATE = 1, the prescaler increments only if the CP0 pin is HIGH for each rising edge transition of CLK0 if C/TN = 1 or with FCLK if C/TN = 0.
1	C/TN	Counter/timer mode; C/TN = 0[1], timer mode; the prescaler is incremented on the rising edge of the peripheral clock (FCLK); C/TN = 1, counter mode; the prescaler increments on the rising edge of CLK0 for Timer 0 (CLK1 for Timer 1).
0	RUN	Timer run enable; RUN = 0[1], timer prescaler stopped and registers value held; RUN = 1, when set the prescaler and counter are loaded and the prescaler is then incremented.

Note

1. The default value after a CPU-reset.

Table 41 Description of channel mode; n = 0 to 5; X = don't care

CnM2	CnM1	CnM0	DESCRIPTION
0	0	0	Channel n inhibited
0	0	1	Channel n capture on LOW-to-HIGH transition of pin CPn
0	1	0	Channel n capture on HIGH-to-LOW transition of pin CPn
0	1	1	Channel n capture on any transitions of pin CPn
1	X	X	Channel compare mode

11.6 Timer Status Register

Four events can occur: a timer overflow or three channel matches/captures. These event flags are stored in the 4-bit Timer 0 Status Register (T0SR for T0) and Timer 0 Status Register (T1SR for T1). They can be cleared by software but cannot be set. By writing a logic 1 the flags stay unchanged. In order to clear a particular flag one has to write a logic 0 to the corresponding position and logic 1s to the others. One should avoid to use the instruction BCLR, which can reset accidentally several flags.

Table 42 Timer Status Registers T0SR and T1SR

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
FFFF 830DH	T0SR	–	–	–	–	C2F	C1F	C0F	TOV
FFFF 831DH	T1SR	–	–	–	–	C5F	C4F	C3F	TOV

Table 43 Description of T0SR and T1SR bits

BIT	SYMBOL	DESCRIPTION
7 to 4	–	Reserved.
3 to 1	T0SR: C2F to C0F T1SR: C5F to C3F	Channel n event flag (note 1); CnF = 0[2], no event; CnF = 1, capture mode: a capture occurred.
0	TOV	Timer Overflow Flag; TOV = 0[2], no overflow; TOV = 1, timer overflow occurred.

Notes

1. n = 0 to 2 for T0; n = 3 to 5 for T1.
2. The default value after a CPU-reset.

11.7 Watchdog timer

The P90CL301 contains a watchdog timer consisting of a 13-bit prescaler and an 8-bit timer WDTIM. The prescaler is incremented by the peripheral clock. The 8-bit timer is incremented every 8192 cycles of the peripheral clock FCLK.

If the FCLK frequency is 2 MHz, the Watchdog timer can operate in the range of 4.1 ms up to 1 s. The Watchdog timer is disabled after reset. It can be enabled by writing any value to the WDCON register. The only way to disable a running Watchdog timer is to reset the P90CL301.

When a timer overflow occurs the microcontroller will be reset (except registers SYSCON, PCON, PRL and PRH which will not be reset). To prevent an overflow of the Watchdog timer, the User Program must reload the Watchdog register within a period shorter than the programmed timer interval.

This timer interval is determined by the 8-bit timer value written to the register WDTIM. For FCLK in MHz, the:

$$\text{Watchdog period} = (256 - \text{WDTIM}) \times \frac{8192}{\text{FCLK}}\ \mu\text{'s}$$

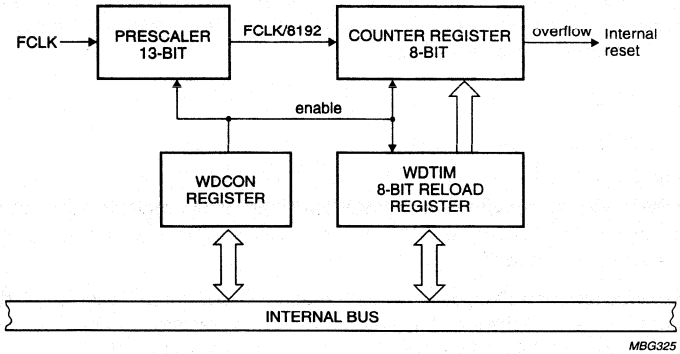


Fig.9 Watchdog timer block diagram.

The Watchdog timer is controlled by the register WDCON. A value of A5H in WDCON clears both the prescaler and timer WDTIM. After reset, WDCON contains A5H.

Every value other than A5H in WDCON enables the Watchdog timer. Since the bit 0 of the WDCON input is tied to a logic 0 by hardware during write operations on WDCON, the reset value A5H can not be programmed again and can only be restored by a reset.

Timer WDTIM can be written only if WDCON has previously been loaded with 5AH, otherwise WDTIM and the prescaler are not affected. A successful write operation to WDTIM also clears the prescaler and clears WDCON.

Only the values A5H or 5AH are stored, all other values are stored with a dummy value 00H.

12 SERIAL INTERFACES

12.1 UART interface

The UART can operate in 4 modes. The baud rate for receive and transmit can be generated internally or by the baud rate generator. The UART is full duplex, meaning it can receive and transmit simultaneously. The receive and transmit registers are both accessed as a unique register SBUF. Writing to SBUF loads the transmit register, and reading from SBUF accesses a physically separate receive register.

12.1.1 UART OPERATING MODES

The serial port can operate in one of the four modes:

Mode 0 Serial data enters and exits through RXD. TXD pin delivers the synchronous shift clock. 8 bits are transmitted/received (LSB first). When the bit PCLK3 in the SYSCON register is reset, the baud rate is equal to $1/6 \times$ CLK. When the bit PCLK3 in register SYSCON is set, the baud rate is equal to $1/12 \times$ CLK. The UART baud rate should not exceeds 4.5 Mbaud.

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a start bit at logic 0, 8 data bits (LSB first) and a stop bit at logic 1. On receive the stop bit goes into RB8 in the register SCON. The baud rate is given by the baud rate generator output BGCLK0 for the UART0 and BGCLK1 for the UART1.

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): a start bit at logic 0, 8 data bits (LSB first) a programmable 9th data bit, and a stop bit at logic 1. On transmit the 9th bit is taken from the bit TB8 from the SCON register. On receive the 9th bit goes into RB8 of SCON, while the stop bit is ignored. The baud rate is equal to $1/6 \times$ CLK. The UART clock should not exceed 4.5 Mbaud.

Mode 3 Same as mode 2 except for the baud rate, which is given by the baud rate generator output BGCLK0 for the UART0 and BGCLK1 for the UART1.

In all four modes, transmission is initiated by any instruction loading SBUF. In Mode 0, reception is initiated by the condition RI = 0 and REN = 1. In the remaining modes reception is initiated by the incoming start bit if REN = 1.

12.1.2 UART CONTROL REGISTER SCONn

The SCONn register controls the UARTn (n = 0 to 1) modes and contains the interrupt flags.

Table 44 UART Control Registers SCON0 and SCON1

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
FFFF 8603H	SCON0	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
FFFF 8607H	SCON1								

Table 45 Description of register SCON0 and SCON1 bits

BIT	SYMBOL	DESCRIPTION
7 to 6	SM0 to SM1	Mode bits; see Table 46.
5	SM2	Multiprocessor; enable the multiprocessor communication feature in Modes 2 and 3. If SM2 is set the RI will not be activated if the received 9th data bit RB8 = 0. In Mode 1, if SM2 is set the RI will not be activated if a valid stop bit is not received. In Mode 0, SM2 should be a logic 0.
4	REN	Receive enable; enables serial reception; set and cleared by software.
3	TB8	Transmit extra bit; 9th data bit that will be transmitted in Modes 2 and 3; set and cleared by software.

BIT	SYMBOL	DESCRIPTION
2	RB8	Receive extra bit; in Modes 2 and 3, RB8 is the 9th bit received. In Mode 1, if SM2 = 0, RB8 is the stop bit which is received.
1	TI	Transmit interrupt; it is set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit in the other modes (except: see bit SM2). TI must be cleared by software (cannot be set by software). By writing a logic 1 the flags stay unchanged. In order to clear a particular flag one has to write a logic 0 to the corresponding position and a logic 1 to the others. One should avoid to use the instruction BCLR, which can reset accidentally several flags.
0	RI	Receive interrupt; set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit in the other modes (except: see SM2). RI must be cleared by software (cannot be set by software). By writing a logic 1 the flags stay unchanged. In order to clear a particular flag one has to write a logic 0 to the corresponding position and a logic 1 to the others. One should avoid to use the instruction BCLR, which can reset accidentally several flags.

Table 46 Mode defined by bits SM0 and SM1

SM0	SM1	MODE	DESCRIPTION
0	0	0	shift register; $1/6 \times$ CLK
0	1	1	8-bit UART; BGCLK0 and BGCLK1
1	0	2	9-bit UART; $1/16 \times$ CLK
1	1	3	9-bit UART; BGCLK0 and BGCLK1

12.2 Baud rate generator

A dedicated baud rate generator is directly connected to the UART0. For the UART1 this clock can be divided by 1 or 4 as a function of the bit BDIV in the BCON control register.

The baud rate generator consists of a 16-bit timer, two 8-bit registers BREGL and BREGH (LSB and MSB) to store the 16-bit reload value, and a control register BCON.

When an overflow occurs the timer is reloaded with the contents of the registers BREGH, BREGL. The timer is clocked by the peripheral clock.

The baud rates for UART0 and UART1 in Mode 1 and 3 are determined by the timer overflow rate as follows (FCLK is in Hz):

$$\text{BGCLK0} = \frac{\text{FCLK}}{(16 \times (65536 - \text{BREG}))}$$

$$\text{BGCLK1} = \frac{\text{FCLK}}{\left(16 \times (65536 - \text{BREG}) \times 4^{\text{BDIV}}\right)}$$

12.2.1 UART Baud Rate Control Register (BCON)

Table 47 UART Baud Rate Control Register (address FFFF 860FH)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	BST	BDIV

Table 48 Description of BCON bits; see note 1

BIT	SYMBOL	DESCRIPTION
7 to 2	–	Reserved.
1	BST	BST = 0, stop timer; BST = 1, start timer increment after loading of timer register with the reload register value.
0	BDIV	BDIV = 0, UART1 baud rate not divided; BDIV = 1, UART1 baud rate divided by 4.

Note

1. The default value after a CPU-reset for all bits is a logic 0.

12.3 UART queue

The UART queue performs the sending and receiving of a frame of bytes of variable length through the UART without the support of the CPU. Only the UART0 has a frame buffer located at the lower 256 bytes section of the internal RAM. A controller ensurs the sequencing of the transfers between the RAM and the UART and generates interrupts to the CPU. This UART queue can be used for transmission and reception simultaneously or for only one of the two modes.

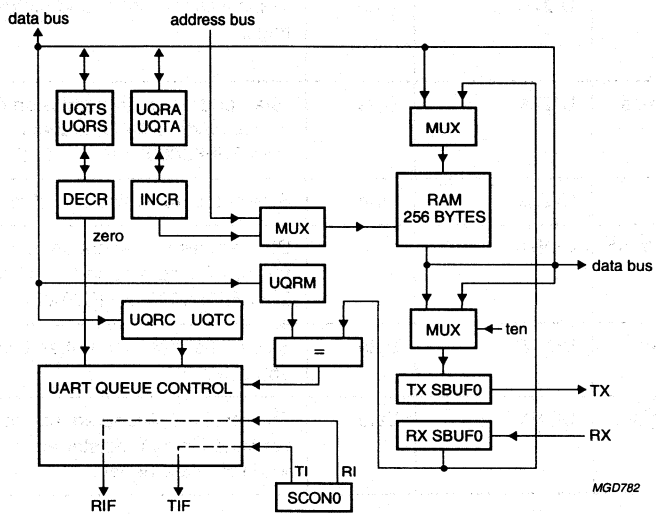


Fig.10 UART queue Block Diagram

The RAM can be accessed by the CPU anytime. The queue controller accesses the RAM either in read mode for the transmission or in write mode for the reception. When the queue controller accesses the RAM, the CPU waits for the end of the access cycle (maximum 4 CLK clocks). The RAM space can be partitioned in one or several buffers for transmission or reception or for normal data storage. The maximum size of a buffer is limited to 256 bytes. In addition to these buffers the queue consists of a set of control and data registers:

Table 49 Function of UART queue registers.

Function	Name	Size	Description
Reception Control register	UQRC	Byte	Reception control and status flags.
Transmission Control register and interrupt flags.	UQTC	Byte	Transmission control and status flags and interrupt flags.
Transmit buffer address	UQTA	Byte	Start address of transmission buffer from 00h to FFh, corresponds to CPU address from FFFF9000 to FFFF90FF.
Transmit buffer size	UQTS	Byte	Size of the transmission buffer. Limited to 256 bytes.
Reception buffer address	UQRA	Byte	Start address of reception buffer from 00h to FFh, corresponds to CPU address from FFFF9000 to FFFF90FF.
Reception buffer size	UQRS	Byte	Size of the reception buffer. Limited to 256 bytes.
Reception match register	UQRM	Byte	The received characters are compared with the value contained in this register and an interrupt is generated when they are equal.

UQRC and UQTC can be accessed together as a word or as two bytes. For each byte transmitted the UQTA is incremented, the UQTS is decremented.

For each byte received the UQRA is incremented, the UQRS is decremented.The CPU can read this register on the fly, but in this case the accuracy is not guaranted so it is recommended to halt the queue and read the values.

Table 50 Register UQRC (address FFFF 8B00):

Action of	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	REN	RME	RIE	ROE	ROF	RAR	RHLT	RSTF
CPU	S/R	S/R	S/R	S/R	R	S/R	S/R	S
QUEUE	-	-	-	-	S	-	-	R

Action of:

- CPU: R: The CPU can reset this bit, S:The CPU can set this bit.

- QUEUE: R: The queue controller can reset this bit, S: The queue controller can set this bit.

In order to keep the bit unchanged when writing to the control register, it is recommended to write a 1 when it can only by reset, and to write a 0 when it can only be set.

Table 51 Description of UQRC bits. The character * means state after peripheral reset

BIT	SYMBOL	DESCRIPTION
7	REN	Receive queue enable: This bit enables the queue controller. It connects the reception data buffer SBUF0 to the queue controller. It should be set before activating the RSTF bit. When it is reset SBUF0 can be accessed directly by the CPU. REN=0* means receive queue disable. Received byte can be read directly from SBUF0. REN=1 means receive queue enable: The transfers from the SBUF0 to the RAM can be activated by setting the bit RSTF.
6	RME	Reception match enable: If it is set each received byte is compared with the content of the register Uart Queue Receive Match UQRM and if their value match the receive interrupt flag RIF is set. RME=0* means match function disabled. RME=1 means match function enabled.
5	RIE	Reception interrupt enable: When this bit is set, each time a byte is received the receive interrupt flag RIF is set. If it is not set, an interrupt is only generated at the end of the frame. RIE=0* means no interrupt after the reception of each byte, only at the end of the frame. RIE=1 means interrupt after the reception of each byte.
4	ROE	Reception overflow enable: When this bit is set, the RSTF bit is not reset when the reception buffer size reached 0, setting the RIF flag, so the reception of further bytes is allowed. The bit ROF is not set because RSTF stays set. This bit can be set in conjunction of RAR to implement a circular buffer. ROE=0* means no overflow enable. ROE=1 means overflow enable.
3	ROF	Reception overflow flag. This flag is set by the queue controller, when a character is received with the RSTF flag reset and REN set. This event can occur after the end of reception of a frame, and if the CPU had no time to un-load the RAM and set RSTF.ROF=0* mean no overflow detection. ROF=1means overflow.
2	RAR	Reception address reset. If this flag is set, when the buffer size has been decremented to zero, the reception address is reset. This way a circular reception buffer can be located at address 0. RAR=0* means no reset of reception address. RAR=1 means reset of reception address.
1	RHLT	Reception halt : This bit is set by the CPU to interrupt the reception of the frame. The byte currently received by the UART will be stored in the buffer, but the next bytes will be lost until the CPU reset the bit RHLT. In order to stop all activity in the UART it is preferable to reset the bit REN reception enable of the register SCON0. RHLT= 0* means reception not halted. RHLT=1 means reception halted.
0	RSTF	Reception start flag: This bit is set by the CPU to enable the reception of a frame through the UART and it is reset automatically by the queue controller at the end of reception. When RHLT is set this bit stays set. When REN is reset, this bit is reset. RSTF=0* means reception not started or ended. RSTF=1 means reception started and in progress.

Table 52 Register UQTC (address FFFF 8B01)

Action of	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TIF	RIF	reserved	TIWF	TEN	TIE	THLT	TSTF
CPU	R	R	-	-	S/R	S/R	S/R	S
QUEUE	S	S	-	S/R	-	-	-	R

Table 53 Description of UQTC bits. The character * means state after peripheral reset

BIT	SYMBOL	DESCRIPTION
7	TIF	Transmission interrupt flag: This flag is set either at the end of the transmission buffer or at the transmission of each byte if TIE is set. The TIF flag should be reset by the CPU in the exception routine in order to detect further interrupts as they are edge detected for low to high transitions.
6	RIF	Reception interrupt flag: This flag is set either at the end of the reception buffer or during a character match if RME is set or at the reception of each byte if RIE is set. The RIF flag should be reset by the CPU in the exception routine in order to detect further interrupts as they are edge detected for low to high transitions.
5	Reserved	-
4	TIWF	Transmission interrupt waiting. TIWF=0* means queue controller is not waiting for UART transmit interrupt. TIWF=1 means queue controller is waiting for UART transmit interrupt.
3	TEN	Transmission queue enable. TEN=0* means transmission queue disable. Transmitted byte can be written directly into SBUF0. TEN=1 means transmission queue enable: The transfers from the RAM to SBUF0 can be activated by setting the bit TSTF.
2	TIE	Transmission interrupt enable: If it is set, each time a byte is transmitted the transmit interrupt flag TIF is set. If it is not set, an interrupt is only generated at the end of the frame.TIE=0* means no interrupt after the reception of each byte. TIE=1 means interrupt after the reception of each byte.
1	THLT	Halt transmission: This bit is set by the CPU to interrupt the transmission of the frame. The byte currently loaded in the UART will be transmitted entirely, but the next byte will wait until the CPU reset the bit HLTT. THLT=0* means transmission not halted. THLT=1 means transmission halted.
0	TSTF	Start transmission: This bit is set by the CPU to start the transmission of a frame through the UART and it is reset automatically by the queue controller at the end of transmission. TSTF=0* means transmission not started or ended. TSTF=1 means transmission started and in progress.

Table 54 UART queue registers

Register	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UQTA	FFFF 8B03	A7	A6	A5	A4	A3	A2	A1	A0
UQTS	FFFF 8B05	S7	S6	S5	S4	S3	S2	S1	S0
UQRA	FFFF 8B0	A7	A6	A5	A4	A3	A2	A1	A0
UQRS	FFFF 8B09	S7	S6	S5	S4	S3	S2	S1	S0
UQRM	FFFF 8B0B	M7	M6	M5	M4	M3	M2	M1	M0

12.3.1 UART QUEUE OPERATION:

12.3.1.1 TRANSMISSION:

The UART queue transmit operation is as follows:

The UART control register is initialized for a certain transmission mode (0, 1, 2, 3) and the baud rate generator loaded for a defined baud rate.

The CPU loads the data to be transmitted (for example 80 characters) at successive addresses of the internal RAM starting at a certain base address (for example FFFF 9010h). Then it writes the buffer start address and the buffer size in the pointer registers, and initializes the control register.

```
move.b   #$50,UQTS          ; buffer size
move.b   #$10,UQTA          ; buffer start adress
bset     TEN,UQTC ;         ; Enable transmission queue
bset     STF,UQTC;          ; Start transmission.
```

The queue controller reads the byte at the address pointed by the address register and writes it to the transmit data buffer of the UART and the buffer size register is decremented, the address register is incremented pointing to the next byte in the buffer. The transmission starts. The controller waits for the end of transmission, then compares the buffer size value to zero, if they are not equal the same operation is repeated automatically.

If the buffer size is zero the transmit interrupt flag TIF is set issuing an interrupt to the CPU.The interrupt routine should reset TIF and can reload the buffer with other values.

Before checking the buffer size value, the halt bit THLT is tested and if it is set the controller enters a transmission wait state.

12.3.1.2 RECEPTION:

The UART queue reception operation is as follows:

The UART control register is initialized for a certain reception mode (0, 1, 2, 3) and the baud rate generator loaded for a defined baud rate.

The CPU writes the buffer start address and the buffer size in the data registers, and the control register. Several modes can be used:

1. Normal reception buffer:

   We want to receive 80 characters, store then in a buffer starting at the address FFFF9020 and generate an interrupt. The CPU is able to down-load the 80 characters, before the reception of any further character.

```
move.b   #$50,UQRS        ; set buffer size
move.    #$20,UQRA        ; set buffer start address
bset     REN,UQRC         ; enable queue controller
bset     RSTF,UQRC        ; start reception
```

   After reception of the first character the queue controller reads the data reception register SBUF0 and transfers it's contents into the buffer at the address of the UQRA register, at the same time the buffer size register UQRS is decremented, the address register UQRA is incremented to point to the next byte. If the buffer size is not equal to zero the same operation is repeated automatically for the next byte to be transmitted.

   If the buffer size is zero the receive interrupt flag RIF is set issuing an interrupt to the CPU. The interrupt routine should reset RIF and can read the content of the buffer and re-initialize the control registers.

```
     andi.b    #$BE,UQTC          ; reset RIF bit
     move.b    #$28,d0            ; buffer size in words
     move.l    #$FFFF9020,a0      ; buffer start address
     move.l    #$00008000,a1      ; extern memory start address
L1   move.w    (a0)+,(a1)+        ; transfer to extern memory
     dbne      d0,L1              ; loop
```

2. Special termination character match:

   Suppose that we want to generate an interrupt after the reception of a Carriage Return character, we load in the reception match register the value ODh, to guarantee that the buffer does not overflow if the buffer size is limited to 80 characters. The buffer is located in RAM at the address FFFF 9050h.

```
move.b   #$50,UQRS        ; buffer size
move.b   #$50,UQRA        ; buffer start address
move.b   #$0d,UQRM        ; set match character
bset     REN,UQRC         ; enable queue
bset     RME,UQRC         ; reception match enable
bset     RSTF,UQRC        ; start reception,
```

   (all these control bits can be set at the same time)

   The same operations as decribed before are performed but in addition each received characters compared with the character Carriage Return and if they match the receive interrupt flag RIF is set, RSTF is reset and the reception queue is stopped.

3. Linear buffer with continuous reception.

   If we want to continue to receive characters in the buffer after the end of the buffer and the setting of RIF:

```
move.b   #$50,UQRS        ; buffer size
move.b   #$50,UQRA        ; buffer start address
bset     REN,UQRC         ; enable queue
bset     ROE,UQRC         ; reception overflow enable
bset     RSTF,UQRC        ; start reception,
(all these control bits can be set at the same time)
```

In this case RSTF is not reset at the end of the buffer, but the CPU will receive an interrupt (RIF=1) when the size register UQRS equals zero.

4. Circular buffer with interrupt.

   If we want to implement a circular buffer which generates an interrupt each time the size register is equal to 0, the UQRA address register is reset and points to the beginning of the RAM.

```
move.b   #$50,UQRS        ; buffer size
move.b   #$00,UQRA        ; buffer start address
bset     REN,UQRC         ; enable queue
bset     RAR,UQRC         ; reception reset address
bset     RSTF,UQRC        ; start reception,
(all these control bits can be set at the same time)
```

12.3.1.3 Reception halt:

Before to check the buffer size value, the halt bit HLTR0 is tested and if it is set the controller enters a reception wait state.

12.3.1.4 Emulation:

When the pin PHALTN (on the emulation package) is asserted low, the queue is halted the same way as when THLT and RHLT are set . The queue operation is continued when the pin PHALTN is released high.

12.4 I²C-bus interface

The serial port supports the twin line I²C-bus. The I²C-bus consists of a data line SDA and a clock line SCL. These lines also function as I/O port lines P11 and P10 respectively (always open drain). The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware. The I²C-bus serial I/O has complete autonomy in byte handling and operates in four modes:

- Master transmitter mode
- Master receiver mode
- Slave transmitter mode
- Slave receiver mode.

These functions are controlled by the SCON register. SSTA is the Status Register whose contents may be used as a vector to various service routines. SDAT is the data shift register and SADR the slave address register. Slave address recognition is performed by hardware.

For more details on the I²C-bus functions, see user manual *"The I²C-bus and how to use it (including specifications)"*; order number 9398 393 40011.

12.5 Serial Control Register (SCON)

Table 55 Serial Control Register (address FFFF 8207H)

7	6	5	4	3	2	1	0
CR2	ENS	STA	STO	SI	AA	CR1	CR0

Table 56 Serial Control Register SCON bits

BIT	SYMBOL	DESCRIPTION
7, 1 and 0	CR2 to CR0	These three bits determine the serial clock frequency when SIO is in a master mode function of the peripheral clock FCLK (see Tables 57 and 58).
6	ENS	Enable serial I/O; If ENS = 0, the serial interface I/O is disabled and reset; if ENS = 1, the serial interface is enabled.
5	STA	Start flag; when this bit is set in slave mode, the hardware checks the I²C-bus and generates a START condition if the bus is free or after the bus becomes free. If the device operates in master mode it will generate a repeated START condition.
4	STO	Stop flag; if this bit is set in the master mode a STOP condition is generated. A STOP condition detected on the I²C-bus clears this bit. The STOP bit may also be set in slave mode in order to recover from an error condition. In this case no STOP condition is generated to the I²C-bus, but the hardware releases the SDA and SCL lines and switches to the not selected slave receiver mode. The STOP flag is cleared by the hardware.

BIT	SYMBOL	DESCRIPTION
3	SI	Serial Interrupt flag; this flag is set, and an interrupt is generated, after any of the following events occur: • A START condition is generated in master mode. • The own slave address has been received during AA = 1. • The general call address has been received while bit SADR.0 = 1 and AA = 1. • A data byte has been received or transmitted in master mode. • A data byte has been received or transmitted as selected slave. • A STOP or START condition is received as selected slave receiver or transmitter. While the SI flag is set, SCL remains LOW and the serial transfer is suspended. SI must be reset by software.
2	AA	Assert Acknowledge; when this bit is set, an acknowledge is returned after any one of the following conditions: • Slave address is received. • The general call address is received (bit SADR.0 = 1). • A data byte is received, while the device is programmed to be a master receiver. • A data byte is received, while the device is a selected slave receiver. When bit AA is reset, no acknowledgement is returned. Consequently, no interrupt is requested when the own slave address or general call address is received.

Table 57 CLK/SCL divide factor

Values greater than 100 kbits are outside the specified frequency range.

CR2	CR1	CR0	CLK/SCL DIVIDE FACTOR						
			D = 2 (1)	D = 3	D = 4	D = 5	D=6	D=8	D=10
0	0	0	128	192	256	320	384	512	640
0	0	1	112	168	224	280	336	448	560
0	1	0	96	144	192	240	288	384	480
0	1	1	80	120	160	200	240	320	400
1	0	0	480	720	960	1200	1440	1920	2400
1	0	1	60	90	120	150	180	240	300
1	1	0	30	45	60	75	90	120	150

Table 58 I^2C-bus serial clock rates

Values greater than 100 kbits are outside the specified frequency range.

CR2	CR1	CR0	BIT FREQUENCY (kHz) AT CLK = 26 MHz						
			D = 2(1)	D = 3	D = 4	D = 5	D = 6	D = 8	D = 10
0	0	0	–	-	101	81	68	51	41
0	0	1	–	-	-	93	77	58	46
0	1	0	–		-	-	90	68	54
0	1	1	–	–	-	-	–	81	65

CR2	CR1	CR0	BIT FREQUENCY (kHz) AT CLK = 26 MHz						
			D = 2[1]	D = 3	D = 4	D = 5	D = 6	D = 8	D = 10
1	0	0	54	36	27	22	18	13	10
1	0	1	–	-	-	-	-	–	87
1	1	0	–	-	-	-	-	–	–

Note to Tables 57 and 58

1. D = divisor = $^{CLK}/_{FCLK}$; see Table 15.

12.5.1 I²C STATUS REGISTER (SSTA)

SSTA is an 8-bit read only Special Function Register. The contents of SSTA may be used as a vector to a service routine. This optimizes response time of the software and consequently that of the I²C-bus. Tables 62 to 66 show the list of the status codes defined by the contents of register SSTA.

Table 59 I²C Status Register (address FFFF 8205H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	–	–	–

Table 60 Description of SSTA bits

BIT	SYMBOL	DESCRIPTION
7 to 3	SC4 to SC0	The bits SC4 to SC0 hold a status code.
2 to 0	–	Reserved; held LOW.

Table 61 Used abbreviations in the mode descriptions; see Tables 62 to 66

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	read bit
W	write bit
ACK	acknowledgement (acknowledge bit = 0)
ACKNOT	not acknowledge (acknowledge bit = 1)
DATA	8-bit (byte) to or from the I^2C-bus
MST	master
SLV	slave
TRX	transmitter
REC	receiver

Table 62 Master transmitter (MST/TRX) mode

SSTA VALUE	DESCRIPTION
08H	A START condition has been transmitted
10H	A repeated START condition has been transmitted
18H	SLA and W have been transmitted, ACK has been received
20H	SLA and W have been transmitted, ACKNOT received
28H	DATA of S1DAT has been transmitted, ACK received
30H	DATA of S1DAT has been transmitted, ACKNOT received
38H	Arbitration lost in SLA, R/$\overline{W}$ or DATA

Table 63 Master receiver (MST/REC) mode

SSTA VALUE	DESCRIPTION
38H	Arbitration lost while returning ACKNOT
40H	SLA and R have been transmitted, ACK received
48H	SLA and R have been transmitted, ACKNOT received
50H	DATA has been received, ACK returned
58H	DATA has been received, ACKNOT returned

Table 64 Slave transmitter (SLV/TRX) mode

S1STA VALUE	DESCRIPTION
A8H	Own SLA and R received, ACK returned
B0H	Arbitration lost in SLA, R/$\overline{W}$ as MST. Own SLA and R received, ACK returned
B8H	DATA byte has been transmitted, ACK received
C0H	DATA byte has been transmitted, ACK received
C8H	Last DATA byte has been transmitted, ACKNOT received

Table 65 Slave receiver (SLV/REC) mode

SSTA VALUE	DESCRIPTION
60H	Own SLA and W have been received, ACK returned
68H	Arbitration lost in SLA, R/$\overline{W}$ as MST. Own SLA and W have been received, ACK returned
70H	General call has been received, ACK returned
78H	Arbitration lost in SLA, R/$\overline{W}$ as MST. General call received, ACK returned
80H	Previously addressed with own SLA. DATA byte received, ACK returned
88H	Previously addressed with own SLA. DATA byte received, ACKNOT returned
90H	Previously addressed with general call. DATA byte received, ACK has been returned
98H	Previously addressed with general call. DATA byte received, ACKNOT has been returned
A0H	A STOP condition or repeated START condition received while still addressed as SLV/REC or SLV/TRX

Table 66 Miscellaneous

S1STA VALUE	DESCRIPTION
00H	Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition

12.5.2 I²C Data Shift Register (SDAT)

Table 67 I²C Data Shift Register (address FFFF 8201H)

7	6	5	4	3	2	1	0
DATA.7	DATA.6	DATA.5	DATA.4	DATA.3	DATA.2	DATA.1	DATA.0

Table 68 Description of SDAT bits

BIT	SYMBOL	DESCRIPTION
7 to 0	DATA.7 to DATA.0	The serial data to be transmitted or data that has just been received. Bit 7 is transmitted or received first; i.e. data is shifted from right to left.

12.5.3 I²C Address Register (SADR)

This 8-bit register may be loaded with the 7-bit address to which the controller will respond when programmed as a slave receiver/transmitter.

Table 69 I²C Address Register (address FFFF 8203H)

7	6	5	4	3	2	1	0
SADR.7	SADR.6	SADR.5	SADR.4	SADR.3	SADR.2	SADR.1	SADR.0

Table 70 Description of the register SADR bits

BIT	SYMBOL	DESCRIPTION
7 to 1	SADR.7 to SADR.1	Slave address.
0	SADR.0	SADR.0 = GC, is used to determine whether the general CALL address is recognized: If GC = 0, general CALL address is not recognized (default value after a CPU-reset). If GC = 1, general CALL address is recognized.

13 PULSE WIDTH MODULATION OUTPUTS (PWM)

Two Pulse Width Modulation outputs are provided on the P90CL301. These channels output pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler PWMP, which generates the clock for the counter. The 8-bit counter counts modulo 255 (from 0 to 254 inclusive).

The prescaler and counter are used for the two channel outputs. The value of the 8-bit counter is compared to the content of the registers PWM0 (resp. PWM1) for the channel output PWM0 (resp. PWM1). Provided the content of this register is greater than the counter value, the output of PWM0 (resp. PWM1) is set LOW. If the content of this register is equal to, or less than the counter value, the output will stay high. The pulse width ratio is therefore defined by the content of the register PWM0 (resp. PWM1). The pulse width ratio is in the range of 0 to $^{255}/_{255}$ and may be programmed in increments of $^{1}/_{255}$.

The repetition frequency: $f_{PWM} = \frac{FCLK}{(1 + PWMP) \times 255}$ Hz; for FCLK in Hz.

When using a peripheral clock of 6 MHz for example, the above formula gives a repetition frequency range of 23 kHz to 91 Hz.

By loading the PWM0 (resp. PWM1) with either 00H or FFH, the PWM0 output can be retained at a constant HIGH or LOW level respectively. When loading FFH to the PWM0 (resp. PWM1) register, the 8-bit counter will never actually reach this value.

13.1 Prescaler PWM Register (PWMP)

Table 71 Prescaler PWM Register (address FFFF 8801H)

7	6	5	4	3	2	1	0
PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Table 72 Description of PWMP bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PWMP.7 to PWMP.0	Prescaler division factor = (PWMP + 1).

13.2 PWM Data Registers (PWM0 and PWM1)

Table 73 PWM Data Registers PWM0 and PWM1

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
FFFF 8803H	PWM0	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0
FFFF 8805H	PWM1	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Table 74 Description of PWM0 and PWM1 bits; n = 0 to 1

BIT	SYMBOL	DESCRIPTION
7 to 0	PWMn.7 to PWMn.0	Pulse width ratio. LOW/HIGH ratio of PWMn signals = $\frac{(PWMn)}{255 - (PWMn)}$

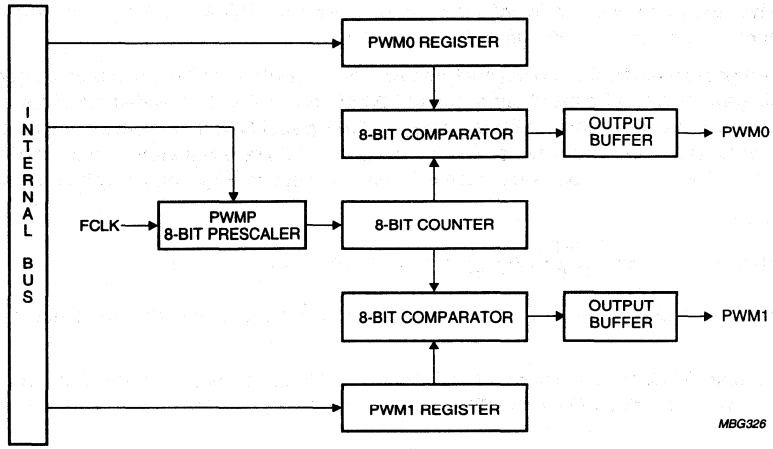


Fig.11 PWM block diagram

14 ANALOG-TO-DIGITAL CONVERTER (ADC)

The analog input circuitry consist of a 4 input analog multiplexer and an analog-to-digital converter (ADC) with 8-bit resolution. The analog reference voltage V_{refA} and the analog supplies V_{DDA}, V_{SSA} are connected via separate input pins.

The conversion time takes 24 periods of the secondary peripheral clock FCLK2 (see Section 6.6). The maximum value of the FCLK2 clock is dependant on the supply voltage (see Section 20).

As the ADC is based on a successive approximation algorithm using a resistor scale connected to V_{refA} and V_{SSA}, a continuous current flows in this resistor.

By resetting the EADC bit in the control register ADCON or by entering Power-down it is possible to switch off this current to reduce the static power consumption.

The ADC is controlled using the ADCON control register. Input channels are selected by the analog multiplexer function of register bits ADCON.0 and ADCON.1. The completion of the 8-bit ADC conversion is flagged by ADCI in the ADCON register and the result is stored in the register ADCDAT (address FFFF 8809H).The result of a completed conversion remains unaffected provided ADCI is HIGH. While ADCS or ADCI are HIGH, a new ADC start will be blocked and consequently lost. An ADC conversion already in progress is aborted when Power-down mode is entered.

14.1 ADC Control Register (ADCON)

Table 75 ADC Control Register (address FFFF 8807H)

7	6	5	4	3	2	1	0
0	EADC	0	ADCI	ADCS	0	A1	A0

Table 76 Description of the ADCON bits

BIT	SYMBOL	DESCRIPTION
7	–	Reserved; set to LOW.
6	EADC	ADC enable. If EADC = 1, then ADC is enabled. If EADC = 0, then ADC is disabled; the resistor reference is switched off to save power even while the CPU is operating.
5	–	Reserved; set to LOW.
4	ADCI	ADC interrupt flag. This flag is set when an ADC conversion result is ready to be read. An interrupt is invoked if the level IPLA is different from '0'. The flag must be cleared by software (it cannot be set by software). The ADCI bit must be cleared before a new conversion is started.
3	ADCS	ADC start and status; setting this bit starts a conversion. The logic ensures that this signal is HIGH while the conversion is in progress. On completion, ADCS is reset at the same time the interrupt flag ADCI is set. ADCS cannot be reset by software.
2	–	Reserved; set to LOW.
1, 0	A1, A0	Analog input select; this binary coded address selects one of the four analog inputs ADC0 to ADC3. It can only be changed when ADCI and ADCS are both LOW. A1 is the MSB; e.g. '11' selects analog input channel ADC3.

Table 77 Operation of ADCI and ADCS

ADCI	ADCS	OPERATION
0	0	ADC not busy, a conversion can be started.
0	1	ADC busy, start of a new conversion is blocked.
1	0	Conversion completed, start of a new conversion is blocked.
1	1	Intermediate status for a maximum of one machine cycle before conversion is completed (ADCI = 1, ADCS = 0).

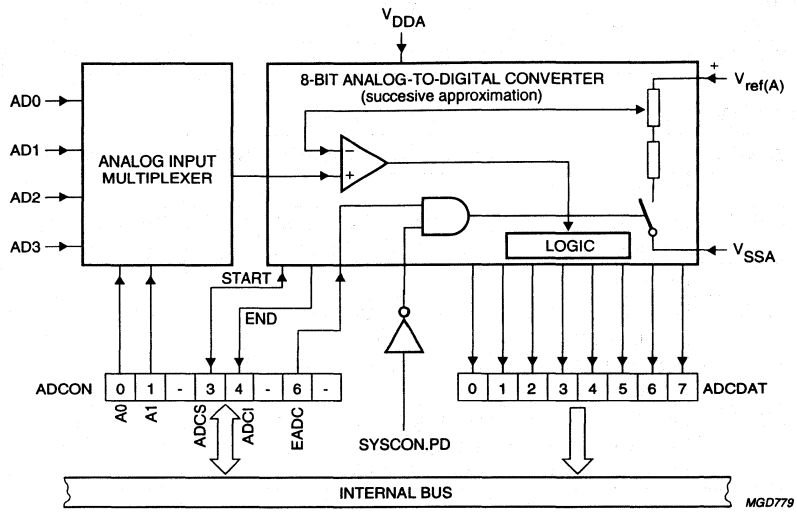


Fig.12 Functional diagram of the ADC.

15 ON-BOARD TEST CONCEPT

To improve the on-board debugging two functions are implemented, the ON-Circuit Emulation (ONCE) mode and the on-chip test ROM.

15.1 ONCE mode

The ON-Circuit Emulation (ONCE) mode eases the testing of an application without having to remove the controller from the board. The ONCE mode is entered by pulling $\overline{CSBT}$ LOW during reset. In this mode the address bus, data bus and bus control signals are in tri-state mode, all other output or bidirectional pins are weakly pulled HIGH. In this mode an emulator probe can be hooked-up to the circuit. Normal operation is restored with a normal reset.

15.2 Test ROM

A second on-board debugging function is introduced for the case were no extra connector can be placed on the PCB. It consists of an internal test-ROM of 256 bytes which is used as boot ROM after a special test mode is activated during reset. The CPU will execute the code placed in the test-ROM and initialize the UART0 and its baud rate generator and wait for commands to be sent to UART0. The internal access time is in this case 3 cycles long. It can only be accessed in supervisor mode.

The purpose of the test ROM is to offer the user a simple software interface to load programs for testing its own application and to transmit back the test result.

The program can be loaded from the host into either the on-chip RAM or the external memory. The test ROM mode is entered by pulling LOW the R/$\overline{W}$ / TROM pin during reset.

Just after the RESET initialization, the user should send a character of 9 bits with all bits being zero (1 stop bit plus 8 data bits = 0) on the RX0 line.

Using the timer, the character length is captured and then the baud rate is automatically calculated and the baud rate generator is initialized. The UART0 is then initialized in Mode 3 with SM2 multiprocessor bit set, REN and TB8 bit set (SCON = F8H). The hardware is now ready to handle the protocol using the following 4 commands (Code 00 to 11).

Table 78 Command format

7	6	5	4	3	2	1	0
Code		NB byte – 1					

Table 79 Command description

BIT	SYMBOL	DESCRIPTION
7, 6	Code	Pointer commands; see Table 80.
5 to 0	NB byte – 1	Indicates the length of the transfer; e.g. (NB byte – 1) = 0 means a 1 byte transfer, (NB byte – 1) = 63 means a 64 byte transfer.

Table 80 Pointer commands

CODE		DESCRIPTION
BIT 7	BIT 6	
0	0	The pointer (A0 register) is initialized with a value depending of the number of transferred bytes. The most significant byte should be transferred first. Protocol: To start a data transfer, the pointer should be initialized first. It is incremented by one at each byte transfer between the memory and the host. The following registers are reserved for the protocol and should not be used by the user: D0, D1, D2, D3, A0, A1 and A2.
0	1	Read command. Read 1 to 64 bytes (load to the host). The pointer is incremented at each transfer.
1	0	Write command. Write 1 to 64 bytes (load from the host). The pointer is incremented at each transfer.
1	1	Jump command. If the NB field is 0 then a jump to the pointer address (A0) is done to start code execution. If the NB field ≠ 0, the complete protocol initialization is restarted (same effect as reset and R/$\overline{W}$ / TROM = 0).

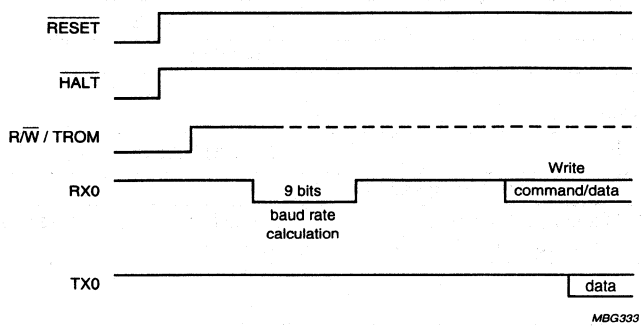


Fig.13 Test-ROM: Timing data transfer.

16 ON-CHIP RAM

The P90CL301 contains a 512 bytes RAM which can be used to store program code or data. As this memory does not need wait states, it can speed up some time consuming tasks like stack operation, table references, or small program loops, compared with slow external memory or when using the 8-bit data bus. For a read or write access, 3 CPU clocks are used. The memory content is kept even when the supply voltage is lowered down to 1.8 V after entering Power-down mode. The base address is FFFF 9000H. It can be accessed in long word, word or bytes.

17 REGISTER MAPPING

The internal register map of the P90CL301 is summarized in Table 81.

Note: Version P90CL301BFH-3/4: The internal registers can only be accessed in Supervisor mode.
Version P90CL301BFH-5 : The internal registers can be accessed in Supervisor and User mode.

Table 81 Register map

ADDRESS (HEX)	SYMBOL	WIDTH (1)	RESET STATE	REGISTER	ACCESS (2)
System register					
FFFF 8000	SYSCON	W	00C0	System Control Register	R/W
Interrupt registers					
FFFF 8101	LIR0	B	00	Latched Interrupt 0/1 Register	R/W
FFFF 8103	LIR1	B	00	Latched Interrupt 2/3 Register	R/W
FFFF 8105	LIR2	B	00	Latched Interrupt 4/5 Register	R/W
FFFF 8107	LIR3	B	00	Latched Interrupt 6/7 Register	R/W
FFFF 810F	PIFR	B	00	Pending Interrupt Flag Register	R/C
I²C registers					
FFFF 8201	SDAT	B	00	I²C Data Register	R/W
FFFF 8203	SADR	B	00	I²C Address Register	R/W
FFFF 8205	SSTA	B	F8	I²C Status Register	R
FFFF 8207	SCON	B	00	I²C Control Register	R/W
Timers registers					
FFFF 8300	T0CRH	B/W	0000	Timer 0 Control Register (high byte)	R/W
FFFF 8301	T0CRL	B	00	Timer 0 Control Register (low byte)	R/W
FFFF 8302	T0RR	W	0000	Timer 0 Reload Register	W
FFFF 8304	T0	W	0000	Timer 0 Register	R
FFFF 8306	T0C0	W	xxxx	Timer 0 Channel 0 Register	R/W
FFFF 8308	T0C1	W	xxxx	Timer 0 Channel 1 Register	R/W
FFFF 830A	T0C2	W	xxxx	Timer 0 Channel 2 Register	R/W
FFFF 830D	T0SR	B	x0	Timer 0 Status Register	R/C
FFFF 830F	T0PR	B	00	Timer 0 Prescaler Reload Register	W
FFFF 8310	T1CRH	B/W	0000	Timer 1 Control Register (high byte)	R/W
FFFF 8311	T1CRL	B	00	Timer 1 Control Register (low byte)	R/W
FFFF 8312	T1RR	W	0000	Timer 1 Reload Register	W
FFFF 8314	T1	W	0000	Timer 1 Register	R
FFFF 8316	T1C0	W	xxxx	Timer 1 Channel 0 Register	R/W
FFFF 8318	T1C1	W	xxxx	Timer 1 Channel 1 Register	R/W
FFFF 831A	T1C2	W	xxxx	Timer 1 Channel 2 Register	R/W
FFFF 831D	T1SR	B	x0	Timer 1 Status Register	R/C
FFFF 831F	T1PR	B	00	Timer 1 Prescaler Reload Register	W

ADDRESS (HEX)	SYMBOL	WIDTH (1)	RESET STATE	REGISTER	ACCESS (2)
FFFF 8401	WDTIM	B	00	Watchdog Timer Register	R/W
FFFF 8403	WDCON	B	A5	Watchdog Control Register (only A5H or 5AH)	S
Port registers					
FFFF 8503	PCON	B	00	Port Control Register	R/W
FFFF 8505	PRL	B	FF	P Port Latch (least significant byte)	R/W
FFFF 8507	PPL	B	FF	P Port Pin (least significant byte)	R
FFFF 8509	PRH	B	FF	P Port Latch (most significant byte)	R/W
FFFF 850B	PPH	B	FF	P Port Pin (most significant byte)	R
FFFF 8109	SPCON	B	80	SP Port Control Register	R/W
FFFF 810B	SPR	B	FF	SP Port Latch	R/W
FFFF 810D	SPP	B	FF	SP Port Pin	R
UART registers					
FFFF 8601	SBUF0	B	xx	UART0 Transmit/Receive Register	R/W
FFFF 8603	SCON0	B	00	UART0 Control Register	R/W
FFFF 8605	SBUF1	B	xx	UART1 Transmit/Receive Register	R/W
FFFF 8607	SCON1	B	00	UART1 Control Register	R/W
Baud rate generator registers					
FFFF 860B	BREGL	B	00	UART Baud Rate Register (least significant byte)	R/W
FFFF 860D	BREGH	B	00	UART Baud Rate Register (most significant byte)	R/W
FFFF 860F	BCON	B	00	UART Baud Rate Control Register	R/W
Peripheral interrupt registers					
FFFF 8701	PICR0	B	00	Timer Interrupt Register	R/W
FFFF 8703	PICR1	B	00	UART0 Interrupt Register	R/W
FFFF 8705	PICR2	B	00	UART1 Interrupt Register	R/W
FFFF 8707	PICR3	B	00	I^2C and ADC Interrupt Register	R/W
Pulse Width Modulation registers					
FFFF 8801	PWMP	B	00	PWM Prescaler Register	W
FFFF 8803	PWM0	B	00	PWM0 Data Register	R/W
FFFF 8805	PWM1	B	00	PWM1 Data Register	R/W
ADC registers					
FFFF 8807	ADCON	B	00	ADC Control Register	R/W
FFFF 8809	ADCDAT	B	FF	ADC Data Register	R
Chip-select registers					
FFFF 8A00	CS0N	W	FFFF	Chip-select 0 Control Register	R/W
FFFF 8A02	CS1N	W	FFFF	Chip-select 1 Control Register	R/W
FFFF 8A04	CS2N	W	FFFF	Chip-select 2 Control Register	R/W

ADDRESS (HEX)	SYMBOL	WIDTH (1)	RESET STATE	REGISTER	ACCESS (2)
FFFF 8A06	CS3N	W	FFFF	Chip-select 3 Control Register	R/W
FFFF 8A08	CS4N	W	FFFF	Chip-select 4 Control Register	R/W
FFFF 8A0A	CS5N	W	FFFF	Chip-select 5 Control Register	R/W
FFFF 8A0C	CS6N	W	FFFF	Chip-select 6 Control Register	R/W
FFFF 8A0E	$\overline{\text{CSBT}}$	W	F306	Chip-select Boot Control Register	R/W
FFFF 8A11	BSREG	B	00	Bus Size Register	R/W
UART queue registers					
FFFF 8B00	UQRC	B	00	UART Queue Receive Control Register	R/W
FFFF 8B01	UQTC	B	00	UART Queue Transmit Control Register	R/W
FFFF 8B03	UQTA	B	00	UART Queue Transmit Address Register	R/W
FFFF 8B05	UQTS	B	00	UART Queue Transmit Status Register	R/C
FFFF 8B07	UQRA	B	00	UART Queue Receive Address Register	R/W
FFFF 8B09	UQRS	B	00	UART Queue Receive Status Register	R/C
FFFF 8B0B	UQRM	B	00	UART Queue Receive Match Register	R/W

Notes

1. Width when specified is in byte (B) or word (W).
2. Access when specified is in read (R) write (W) or clear (C) only. The Watchdog Control Register is special (S).

18 LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+3.6	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
I_I, I_O	DC current into any input or output	–	5	mA
P_{tot}	total power dissipation	–	300	mW
T_{stg}	storage temperature range	–65	+150	°C
T_{amb}	operating ambient temperature range	–40	+ 85	°C
T_j	operating junction temperature range	–	+ 125	°C

19 DC CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	–	3.6	V
I_{DD}	supply current operating; note 1	V_{DD} = 3 V; CLK = 13.8 MHz	–	16	22	mA
		V_{DD} = 3 V; CLK = 27 MHz	–	32	40	mA
$I_{DD(ID)}$	supply current Idle mode; note 2a	V_{DD} = 3 V; CLK = 13.8 MHz	–	400	500	µA
		V_{DD} = 3 V; CLK = 27 MHz	–	800	1000	µA
$I_{DD(STAND)}$	supply current Standby mode; note 2b	VDD = 3 V; CLK = 13.8 MHz	-	9	15	mA
		VDD = 3 V; CLK = 27 MHz	-	18	25	mA
$I_{DD(PD)}$	supply current Power-down mode; note 3	V_{DD} = 3 V	–	2	40	µA
Inputs						
V_{IL}	LOW level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IL}	LOW level input voltage; D15 to D8, XTAL1, $\overline{HALT}$, $\overline{RESET}$, RESETIN		V_{SS}	–	$0.1V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	LOW level input current	V_{DD} = 3 V; V_{IN} = 0.4 V	–	13	50	µA
I_{TL}	input current HIGH-to-LOW transition	V_{DD} = 3 V; V_{IN} = $0.5V_{DD}$	–	140	500	µA
I_{TSI}	tri-state input current		–	1	10	µA
Outputs						
I_{OH4}	HIGH level output current; TS4 and OD4; note 4	V_{DD} = 3 V; V_{OH} = V_{DD} - 0.4 V	4	13	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{OH2}	HIGH level output current; WP2; note 4	V_{DD} = 3 V; V_{OH} = V_{DD} - 0.4 V	2	7	–	mA
I_{OL8}	LOW level output current; OD8 and S8; note 4	V_{DD} = 3 V; V_{OL} = 0.4 V	8	24	–	mA
I_{OL4}	LOW level output current; TS4 and OD4; note 4	V_{DD} = 3 V; V_{OL} = 0.4 V	4	15	–	mA
I_{OL2}	LOW level output current; WP2; note 4	V_{DD} = 3 V; V_{OL} = 0.4 V	2	8	–	mA
C_{IN}	input capacitance ; note 6		–	–	10	pF
R_{UP}	pull-up resistor UP; note 5c		16	26	60	kΩ
R_{UP2}	pull-up resistor UP2; note 5a		8	15	30	kΩ
R_{UP3}	pull-up resistor UP3; note 5b		70	100	500	kΩ
R_{STIN}	RESETIN resistor		15	31	120	kΩ

Notes

1. The operating supply current through V_{DD1}, V_{DD2} and V_{DD3} is measured with all output pins disconnected; RESETIN = $\overline{RESET}$ = $\overline{HALT}$ = 0; A23 to A0 = V_{DD}; D15 to D0 = V_{DD}.
2. Idle and standby current:
   a) The Idle supply current through V_{DD1}, V_{DD2} and V_{DD3} is measured with all port pins disconnected; A23 to A0 = V_{DD}; D15 to D0 = V_{DD}; the circuit is executing NOP instructions from an external memory.
   b) The standby current through VDD1, VDD2 and VDD3 is measured with all port pins disconnected; A23 to A0 = VDD; D15 to D0 = VDD;
3. The Power-down current through V_{DD1}, V_{DD2} and V_{DD3} is measured with all output pins disconnected; XTAL1 = $\overline{RESET}$ = HALTN = V_{DD}; A23 to A0 = V_{DD}; D15 to D0 = V_{DD}; RESETIN = V_{SS}.
4. See Table 84 for the different types.
5. Pull-ups:
   a) These active pull-ups are active on all WP2 WP4 port pins for output voltages greater than Vdd/2. They are only active during the reset sequence on the pins CS0N, CS1N, R/WN, CSBTN and FETCHN for test purpose.
   b) These active pull-ups are only active on D15-0 and A23-0 pins when BPE is set in the SYSCON register.
   c) These pull-ups are only present on the emulation pins PHALTN and NMINE.
6. Not tested in production.

20 ADC CHARACTERISTICS

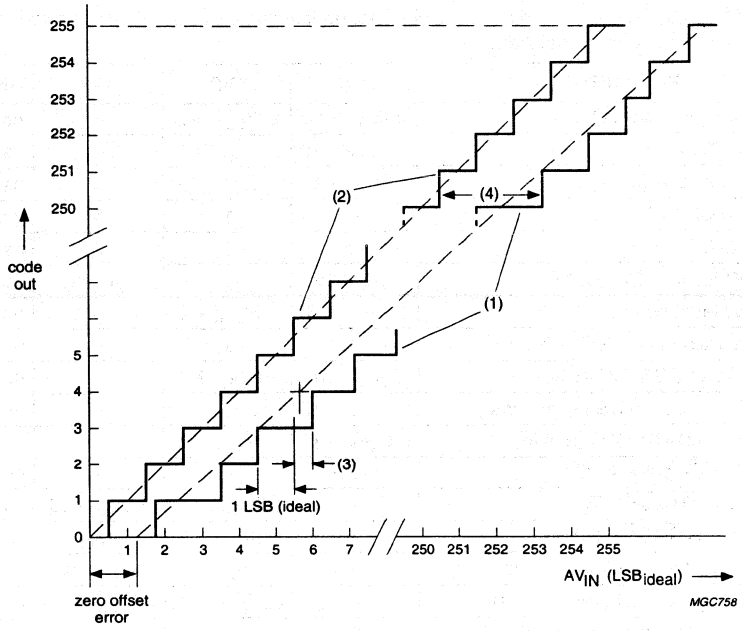
V_{DD} = 2.7 to 3.6 V; V_{refA} = V_{DDA} = V_{DD}; V_{SSA} = V_{SS}; V_{SS} = 0 V; FCLK2 = 250 kHz to 2 MHz; T_{amb} = –40 to +85 °C; for ADC test conditions see note 1; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		V_{DD} – 0.2	–	V_{DD} + 0.2	V
V_{refA}	analog reference voltage		V_{DD} – 0.2	–	V_{DD} + 0.2	V
V_{SSA}	analog ground		V_{SS} – 0.2	–	V_{SS} + 0.2	V
AV_{IN}	analog input voltage		0	–	V_{refA}	V
AI_{DD}	supply current operating	V_{DDA} = 3.0 V	–	150	250	µA
$AI_{DD(PD)}$	analog supply current Power-down mode	V_{DDA} = 3.0 V	–	0.1	5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{Vref}	resistor between V_{refA} and V_{SSA}	note 2	20	34	150	kΩ
C_{IA}	analog input capacitance	note 9	–	–	12	pF
I_{IA}	input leakage current	V_{DDA} = 3.0 V	–	–	1	µA
FCLK2	ADC clock frequency;	V_{DDA} = 2.7 V note 4	0.25	–	2	MHz
t_{ADS}	sampling time		–	6 × t_{FCLK2}	–	µs
t_{ADC}	total conversion time		–	24 × t_{FCLK2}	–	µs
A_e	absolute voltage error	note 1;5	–	–	1	LSB
OS_e	offset error	note 1; 6	–	–	1	LSB
IL_e	integral non-linearity	note 1;7	–	–	1	LSB
DL_e	differential non-linearity	note 1;8	–	–	1	LSB
M_{ctc}	channel-to-channel matching	note 3; 9	–	–	1	LSB

Notes

1. ADC test conditions: V_{DD} = 2.7 V, V_{refA} = 2.7 V, CLK = 20 MHz, FCLK2 = 2 MHz.
2. This resistor is switched off during Power-down mode and when the ADC is switched off (EADC = 0).
3. Channel-to-channel matching: The difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.
4. See Fig.15 for specific FCLK2 range as function of V_{DD}.
5. Absolute voltage error: the maximum difference between actual and ideal code transitions. Absolute voltage error accounts for all deviations of an actual converter from an ideal converter.
6. Offset error: the difference between the actual and ideal input voltage corresponding to the first actual code transition.
7. Integral non-linearity: the maximum deviation between the edges of the steps of the transfer curve and the edges of the steps of the ideal curve. The ideal step curve follows the line of least squares.
8. Differential non-linearity: the maximum deviation of the actual code width from the average code width.
9. Parameter not measured in production, only verified on sampling basis.



(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential non-linearity.
(4) Absolute voltage error.

$$1\ LSB = \frac{V_{REFA} - V_{SSA}}{256}$$

Fig.14 ADC conversion characteristics.

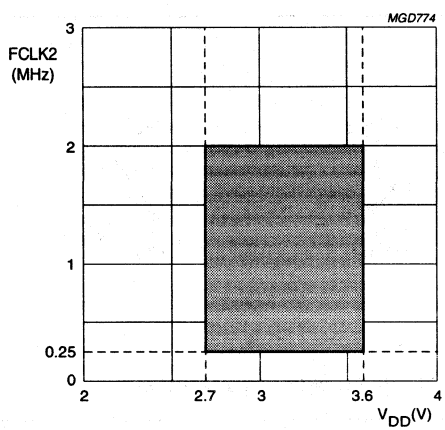


Fig.15 ADC clock (FCLK2) frequency range as a function of V_{DD}.

21 AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = –40 to +85 °C; t_{CLK} = CPU clock cycle time; no fast bus cycle (FBC = 0); no wait status; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{AVSL}	address valid to $\overline{AS}$ LOW	$0.5t_{CLK}$ - 10	$0.5t_{CLK}$ + 2	–	ns
t_{SL}	$\overline{AS}/\overline{DS}$ LOW level	$2.5t_{CLK}$ – 10	$2.5t_{CLK}$ + 2	–	ns
t_{SHAZ}	$\overline{AS}$ HIGH to address invalid	$0.5t_{CLK}$ – 10	$0.5t_{CLK}$	–	ns
t_{ASCSL}	$\overline{AS}/\overline{DS}$ to $\overline{CS}$ LOW	–5	1	5	ns
t_{ASCSH}	$\overline{AS}/\overline{DS}$ to $\overline{CS}$ HIGH	–5	1	5	ns
t_{SLSH}	$\overline{AS}$ LOW to $\overline{DS}$ LOW (write)	t_{CLK} – 15	t_{CLK}	t_{CLK} + 15	ns
t_{DSL}	$\overline{DS}$ LOW level (write)	$1.5t_{CLK}$ – 10	$1.5t_{CLK}$ + 2	–	ns
t_{AVRL}	address valid to R/$\overline{W}$ LOW (write)	t_{CLK} - 5	t_{CLK}	–	ns
t_{CLSL}	R/$\overline{W}$ LOW to $\overline{DS}$ LOW (write)	t_{CLK} – 10	t_{CLK} – 2	–	ns
t_{DOSL}	DATA-OUT valid to $\overline{DS}$ LOW (write)	$0.5t_{CLK}$ – 10	$0.5t_{CLK}$ - 1	–	ns
t_{SHDO}	$\overline{AS}$ HIGH to DATA-OUT invalid	$0.5t_{CLK}$ – 10	$0.5t_{CLK}$ – 3	–	ns
t_{HRPW}	$\overline{HALT}/\overline{RESET}$ pulse width	$24t_{CLK}$	–	–	ns
t_{ASLDTA}	$\overline{AS}$ LOW to $\overline{DTACK}$ LOW	–	$1.5t_{CLK}$ – 28	$1.5t_{clk}$ - 10	ns
t_{ASHDTA}	$\overline{AS}$ HIGH to $\overline{DTACK}$ HIGH	–	$2.5t_{CLK}$ – 25	$2.5t_{clk}$	ns
t_{DCLDI}	$\overline{DTACK}$ LOW to DATA-IN (set-up time)	–	t_{CLK}	t_{CLK} + 10	ns
$t_{DATSETUP}$	$\overline{AS}$ LOW to DATA-IN (set-up time)	-	$2.5t_{CLK}$ – 25	$2.5t_{CLK}$ – 20	ns
t_{SHDI}	$\overline{AS}$ HIGH to DATA invalid (hold time)	0	0	–	ns
t_{SHRH}	$\overline{AS}$ HIGH to R/$\overline{W}$ HIGH (write)	$0.5t_{CLK}$ – 5	$0.5t_{CLK}$ – 2	–	ns
t_{SHAH}	$\overline{AS}$ HIGH to A0 HIGH	t_{CLK} – 10	t_{CLK} + 3	t_{CLK} + 10	ns
t_{SHAWH}	$\overline{AS}$ HIGH to A0 (first byte of word cycle in 8-bit mode)	$0.5t_{CLK}$ – 10	–	$0.5t_{CLK}$ +10	ns
t_{SHW}	LDS HIGH level before write	$2.5t_{CLK}$ - 5	$2.5t_{CLK}$ - 2	-	ns

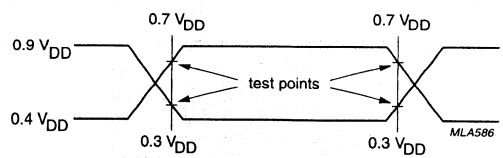


Fig.16 AC testing input waveform.

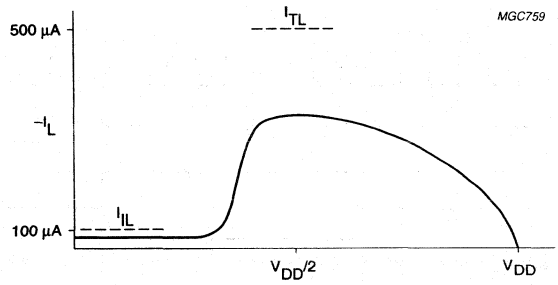


Fig.17 Input current.

22 8051 BUS TIMING

V_{DD} = 2.7 V to 3.6 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; t_{CLK} = CPU clock cycle time; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RR}	read pulse duration	$4.5t_{CLK} - 10$	$4.5t_{CLK} + 10$	ns
t_{WW}	write pulse duration	$4.5t_{CLK} - 10$	$4.5t_{CLK} + 10$	ns
t_{AL}	address set-up time	$1.5t_{CLK} - 20$	–	ns
t_{LA}	address hold time	$t_{CLK} - 5$	–	ns
t_{RD}	RD to valid data input	–	$3.5t_{CLK} - 15$	ns
t_{DFR}	data float after read	–	$2t_{CLK} - 10$	ns
t_{LD}	ALE to valid data input	–	$6t_{CLK} - 20$	ns
t_{LW}	ALE to $\overline{RD}$ $\overline{WR}$	$3t_{CLK} - 20$	$3t_{CLK} + 20$	ns
t_{DW}	data set-up time before $\overline{WR}$	$6.5t_{CLK} - 20$	–	ns
t_{WD}	data hold time after $\overline{WR}$	$0.5t_{CLK} - 10$	–	ns
t_{WHLH}	$\overline{RD}$ $\overline{WR}$ HIGH to ALE HIGH	$t_{CLK} - 10$	$t_{CLK} + 10$	ns

Note

1. These AC parameters are not tested in production.

23 TIMING DIAGRAMS

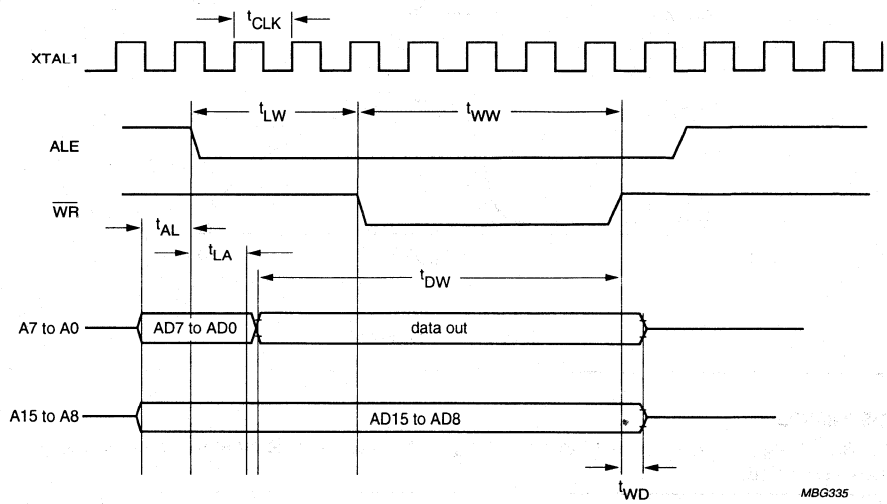


Fig.18 Write to 8051-compatible peripheral circuits.

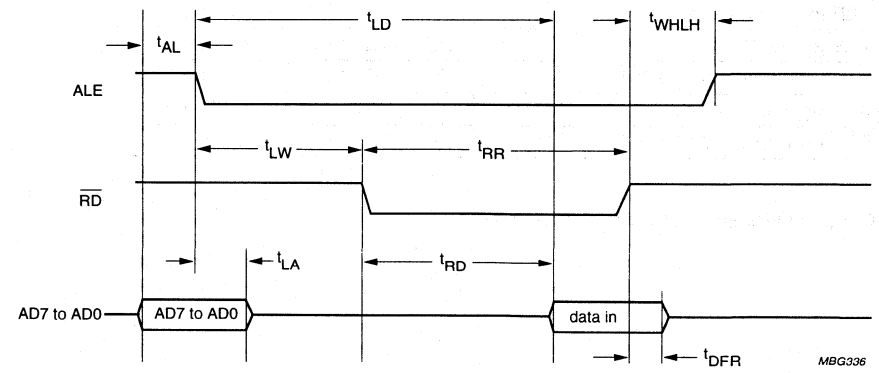


Fig.19 Read from 8051-compatible peripheral circuits.

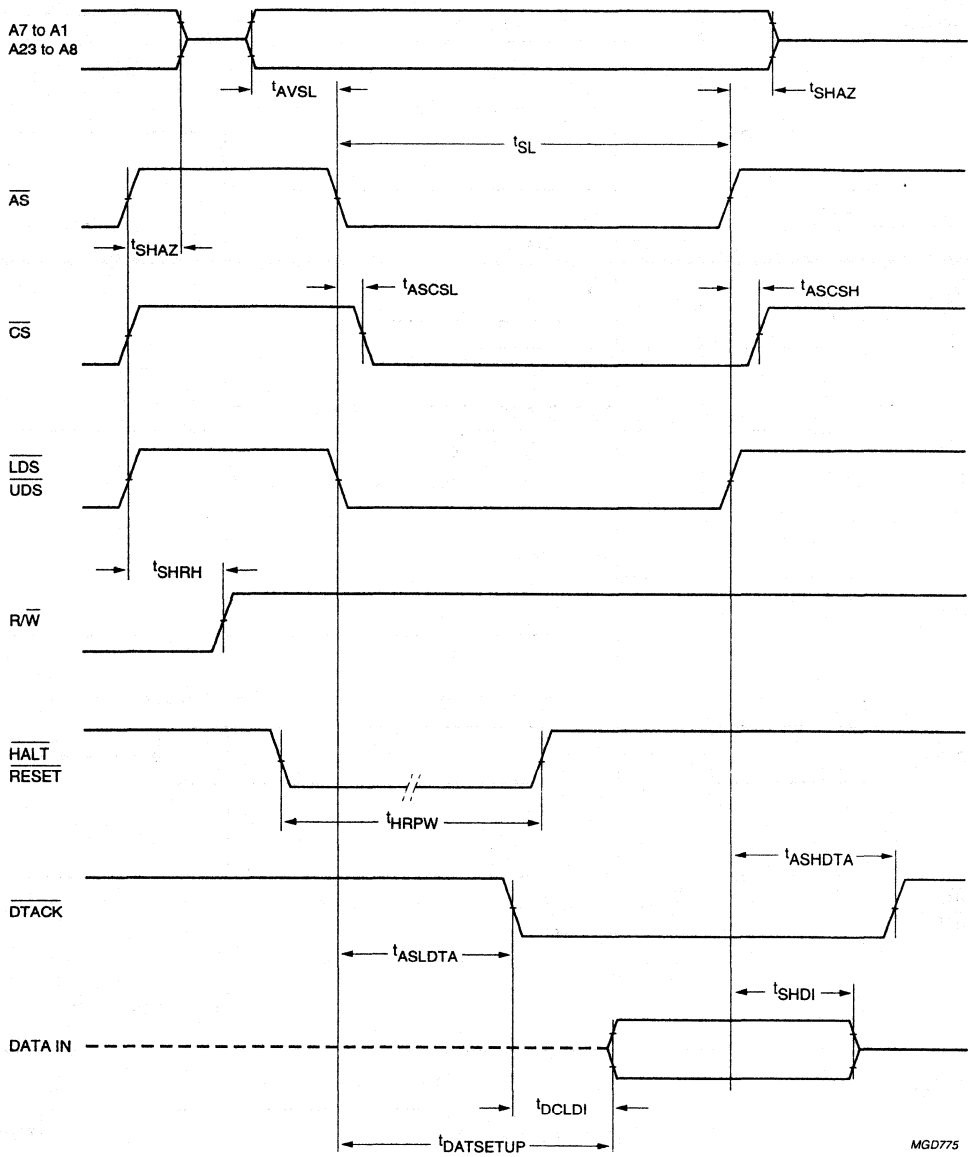


Fig.20 Read cycle timing 16-bit mode.

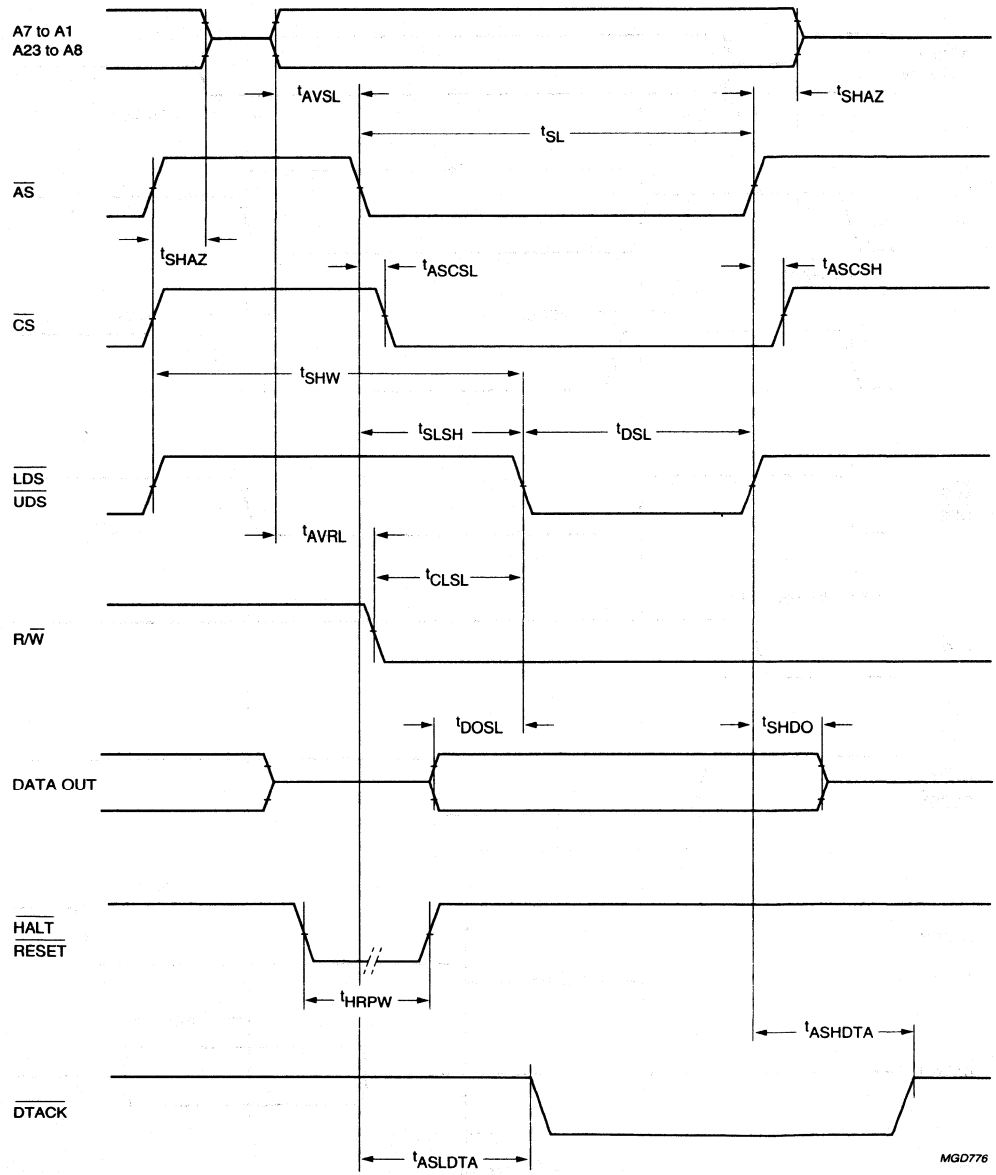
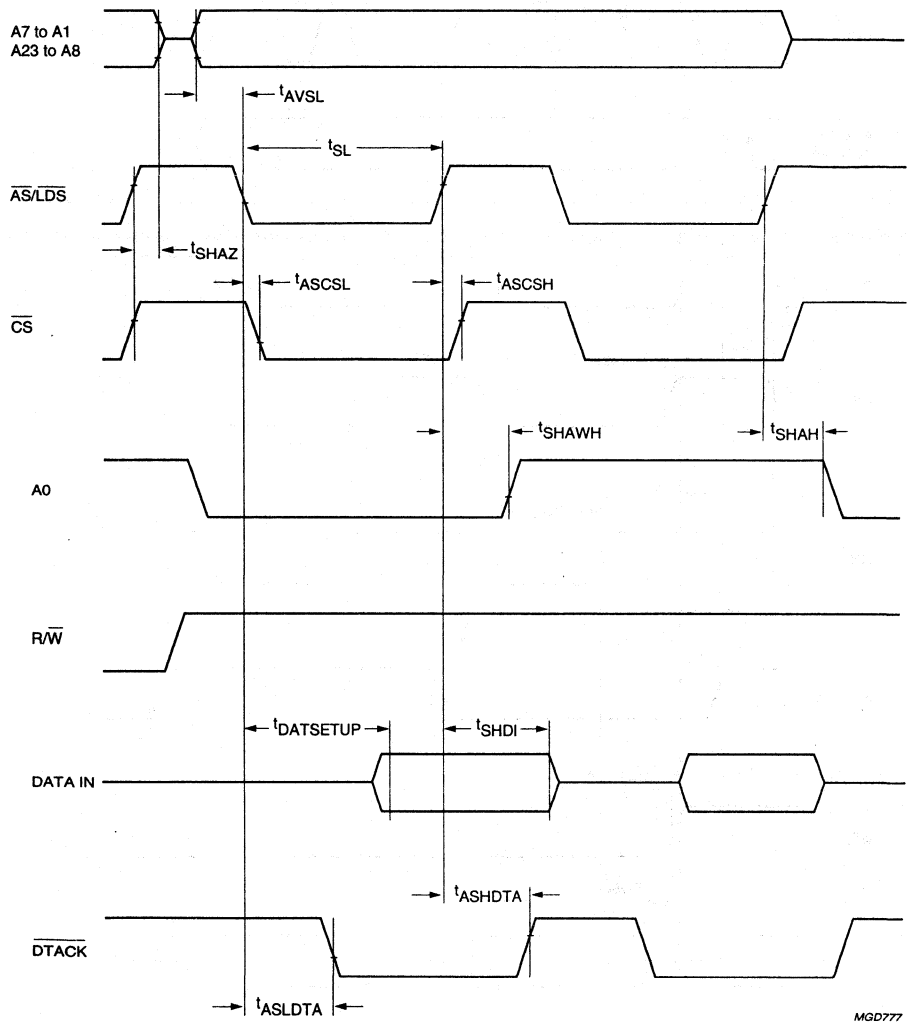


Fig.21 Write cycle timing 16-bit mode.



(no fast bus cycle, FBC = 0)

Fig.22 Read cycle timing 8-bit mode.

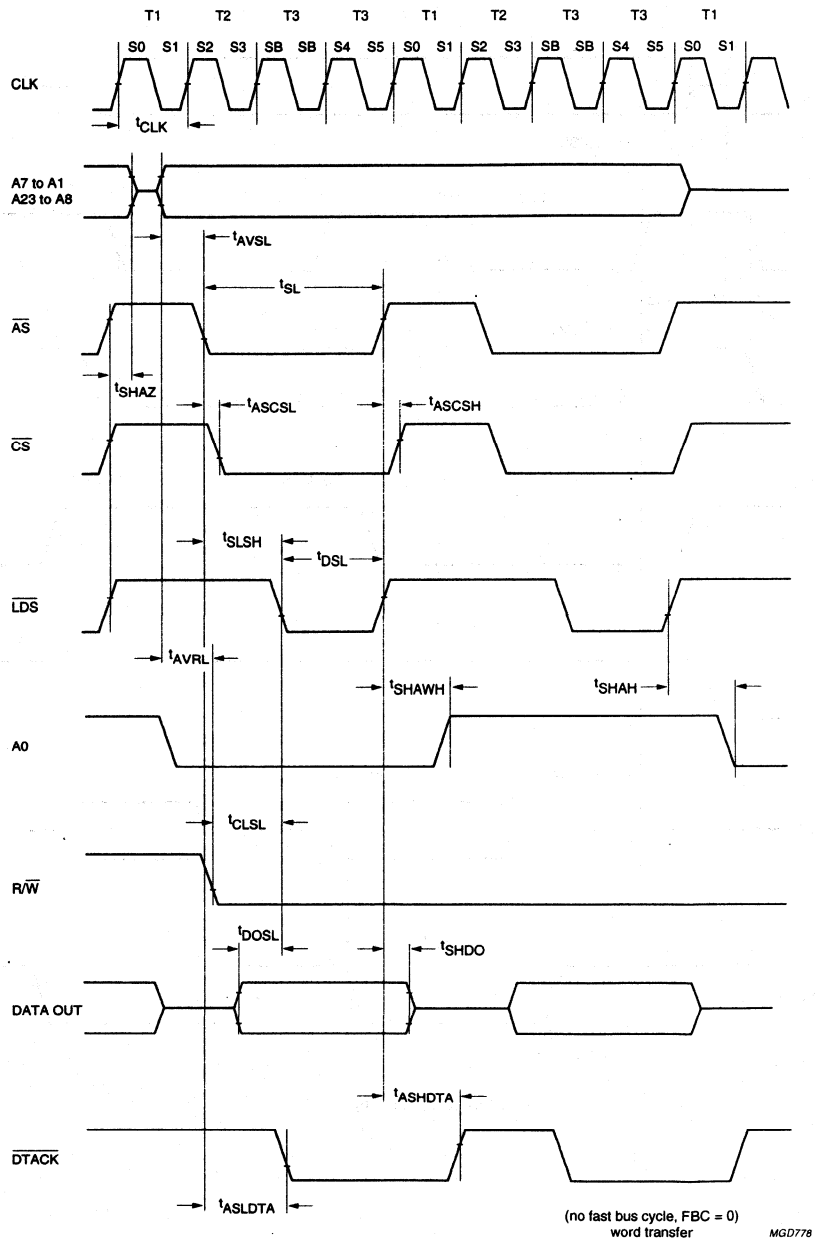


Fig.23 Write cycle timing 8-bit mode clock timing.

24 CLOCK TIMING

Table 82 P90CL301 clock timing

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
		at V_{DD} = 2.7 V		
f_{XTAL1}	input frequency	0	27	MHz
t_{CLK}	cycle time	37	–	ns
t_{CL}	pulse width	13	–	ns
t_{CH}	pulse width	13	–	ns
t_{CR}	rise time	–	5	ns
t_{CF}	fall time	–	5	ns
$\frac{t_{CH}}{t_{CLK}}$	duty cycle	45	55	%

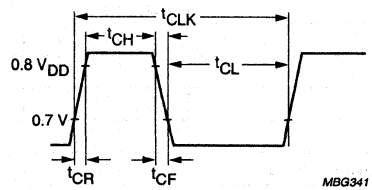


Fig.24 P90CL301 clock timing.

25 PIN STATES IN VARIOUS MODES

Table 83 describes the function, I/O, type and state in various modes - $\overline{\text{RESET}}$, Power-down, $\overline{\text{HALT}}$, $\overline{\text{ONCE}}$ and BPE Bus Pull-up Enable) of the pins.

Table 83 Pin states in various modes

PIN	FUNCTION	I/O[1]	TYPE[2]	STATE[3]				BPE ON
				$\overline{\text{RESET}}$	PD	$\overline{\text{HALT}}$	$\overline{\text{ONCE}}$	
A22 to A19	address bus	O	TSW4	Z	Z	Z	Z	W
$\overline{\text{PCS0}}$ to $\overline{\text{PCS3}}$	8051 chip-select	O	TS4	–	H	Z	–	W
A18 to A1	address bus	O	TSW4	Z	Z	Z	Z	W
AD7 to AD1	8051 data bus	I/O	TSW4	–	Z	Z	–	W
D7 to D0	lower 8-bits of data bus	I/O	TSW4	Z	Z	Z	Z	W
D15 to D8	upper 8-bits of data bus	I/O	TSW4	Z	W	Z	Z	W
PL7 to PL0	port PL	I/O	WP4	–	S	W	W	W
$\overline{\text{AS}}$	address strobe	O	TS4	H	H	Z	Z	-
$\overline{\text{LDS}}$	low data strobe	O	TS4	H	H	Z	Z	-
$\overline{\text{UDS}}$	upper data strobe	O	TS4	H	H	Z	Z	W
A0	address 0	O	TSW4	H	H	Z	Z	W
AD0	8051 address/data 0	I/O	TSW4	–	–	Z	Z	W
R/$\overline{\text{W}}$	read write strobe	O	TS4	Z	H	Z	Z	-
TROM	test ROM mode	I	UP2	–	–	–	–	-
$\overline{\text{DTACK}}$	data transfer acknowledgement	I	N	–	–	–	–	-
$\overline{\text{RESET}}$	CPU peripheral reset	I	N	–	–	–	–	-
	peripheral reset output	OD	OD8	L	Z	Z	Z	-
RESETIN	external power-on-reset	I	RS	–	–	–	–	-
$\overline{\text{HALT}}$	reset input; HALT input	I	N	–	–	–	–	-
	peripheral reset; fault output	OD	OD8	L	Z	Z	Z	-
BSIZE	data bus size	I	N	–	–	–	–	-
NMIACK	emulation NMIN acknowledgement	OD	OD8	Z	Z	Z	Z	-
SP0	second port pin 0	I/O	WP2	W	S	W	W	-
RX1	UART1 receive	I/O	WP2	–	S	W	W	-
$\overline{\text{INT0}}$	interrupt input 0	I	N	–	–	–	–	-
SP1	second port pin 1	I/O	WP2	W	S	W	W	-
TX1	UART1 transmit	O	WP2	–	S	W	W	-
$\overline{\text{INT1}}$	interrupt input 1	I	N	–	–	–	–	-
CLK0	external clock Timer 0	I	N	–	–	–	–	-
SP2	second port pin 2	I/O	WP2	W	S	W	W	-
RX0	UART0 receive	I/O	N	–	–	–	–	-
$\overline{\text{INT2}}$	interrupt input 2	I	N	–	–	–	–	-
CP2	timer capture 2	I	N	–	–	–	–	-
SP3	second port pin 3	I/O	WP2	W	S	W	W	-
TX0	UART0 transmit	I/O	WP2	–	S	W	W	-

PIN	FUNCTION	I/O[1]	TYPE[2]	STATE[3]				BPE ON
				$\overline{\text{RESET}}$	PD	$\overline{\text{HALT}}$	$\overline{\text{ONCE}}$	
$\overline{\text{INT3}}$	interrupt input 3	I	N	–	–	–	–	-
CP3	timer capture 3	I	N	–	–	–	–	-
SP4	second port pin 4	I/O	WP2	W	S	W	W	-
$\overline{\text{INT4}}$	interrupt input 4	I	N	–	–	–	–	-
CP4	timer capture 4	I	N	–	–	–	–	-
SP5	second port pin 5	I/O	WP2	W	S	W	W	-
$\overline{\text{INT5}}$	interrupt input 5	I	N	–	–	–	–	-
CP5	timer capture 5	I	N	–	–	–	–	-
SP6	second port pin 6	I/O	WP2	W	S	W	W	-
$\overline{\text{INT6}}$	interrupt input 6	I	N	–	–	–	–	-
CLK1	external clock Timer 1	I	N	–	–	–	–	-
NMIN	non-maskable interrupt	I	N	–	–	–	–	-
SP7	second port pin 7	I/O	WP2	W	S	W	W	-
P8	port PH pin 8	I/O	WP2	W	S	W	W	-
PWM0	PWM output 0	O	WP2	–	H	W	W	-
CP0	timer capture 0	I	N	–	–	–	–	-
P9	port PH pin 9	I/O	WP2	W	S	W	W	-
PWM1	PWM output 1	O	WP2	–	H	W	W	-
CP1	timer capture 1	I	N	–	–	–	–	-
XTAL1	external crystal input	I	XI	–	–	–	–	-
$\overline{\text{CS1}}$ to $\overline{\text{CS0}}$	chip-select 1 to 0	O	TS4	W	H	Z	Z	-
FC1 to FC0	function code	O	TS4	–	S	Z	Z	-
TSM1 to TSM0	test mode inputs multiplexed with CS1N/0N for test purpose only.	I	UP2	–	–	–	–	-
$\overline{\text{CS2}}$	chip-select 2	O	TS4	H	H	Z	Z	-
$\overline{\text{CS3}}$	chip-select 3	O	TS4	H	H	Z	Z	-
ALE	8051 address strobe	O	TS4	–	H	Z	Z	-
$\overline{\text{CS4}}$	chip-select 4	O	TS4	H	H	Z	Z	-
$\overline{\text{RD}}$	8051 read strobe	O	TS4	–	H	Z	Z	-
$\overline{\text{CS5}}$	chip-select 5	O	TS4	H	H	Z	Z	-
$\overline{\text{WR}}$	8051 write strobe	O	TS4	–	H	Z	Z	-
P10	port PH pin 10	I/O	OD8	Z	Z	Z	Z	-
SCL	I^2C-bus clock	OD	OD8	–	Z	Z	Z	-
P11	port PH pin 11	I/O	OD8	Z	Z	Z	Z	-
SDA	I^2C-bus data	OD	OD8	–	Z	Z	Z	-
$\overline{\text{CS6}}$	chip-select 6	O	TS4	–	H	Z	Z	-
A23	address pin 23	O	TS4	H	S	Z	Z	-
$\overline{\text{CSBT}}$	chip-select boot	O	TS4	W	H	Z	Z	-
$\overline{\text{ONCE}}$	ONCE mode	I	UP2	–	–	–	–	-
P15 to P12	port PH pins 15 to 12	I/O	WP2	W	W	Z	Z	-

PIN	FUNCTION	I/O[1]	TYPE[2]	STATE[3]				BPE ON
				$\overline{\text{RESET}}$	PD	$\overline{\text{HALT}}$	$\overline{\text{ONCE}}$	
ADC3 to ADC0	analog inputs 3 to 0	I	AN	–	–	–	–	-
V_{refA}	ADC reference voltage	I	AREF	Z	Z	R	R	-
$\overline{\text{FETCH}}$[4]	fetch output	O	TS4	W	Z	Z	Z	-
$\overline{\text{EMUL}}$[4]	emulation mode	I	UP2	–	–	–	–	-
$\overline{\text{NMINE}}$[4]	emulation NMIN	I	UP	–	–	–	–	-
CLKOUT[4]	emulation clock output	O	S4	S	S	S	S	-
$\overline{\text{PHALT}}$[4]	emulation HALT	I	UP	–	–	–	–	-

Notes to the pin states in various modes

1. I = input; O = output; I/O = bidirectional.
2. See Table 84 for pin type description.
3. State of the pin in different modes $\overline{\text{RESET}}$, PD (Power-down), $\overline{\text{HALT}}$, $\overline{\text{ONCE}}$ and BPE (Bus Pull-up Enable).
   a) – = not available.
   b) Z = tri-state.
   c) W = weak pull-up.
   d) S = state logic 0 or logic 1.
   e) R = resistive
   f) H = HIGH state.
   g) L = LOW state.
4. Emulation version only.

Table 84 Pin type description

PIN TYPE	DESCRIPTION	MAXIMUM LOAD (pF)
TS4	tri-state output, normal input	100
TSW4	tri-state output, normal input with internal pull-up	100
WP2	weak pull-up output, normal input	80
WP4	weak pull-up output, normal input	80
N	normal input	–
UP	input with internal pull-up	–
UP2	input with internal pull-up	–
OD8	open drain	400
AN	analog input	–
S4	strong output	100
RS	Schmitt trigger input	-
AREF	analog reference input	–

26 PORTS SCHEMATICS.

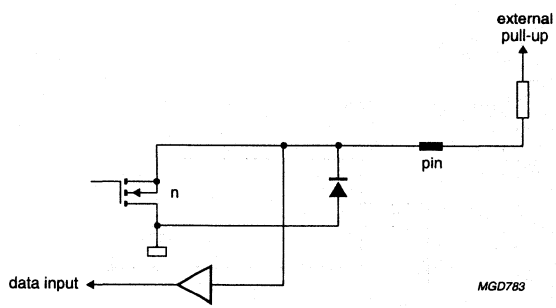


Fig.25 Open-drain port

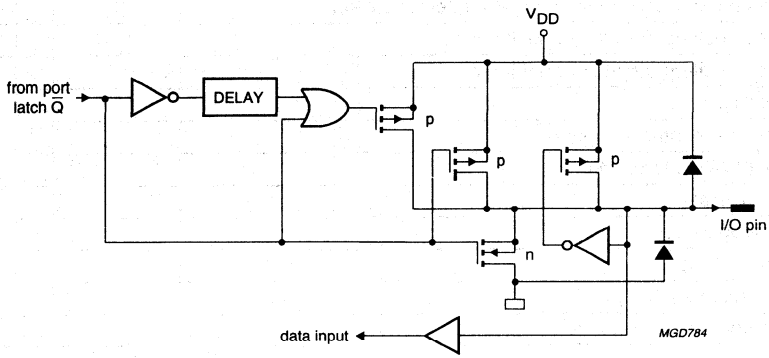


Fig.26 WP2+WP4 port

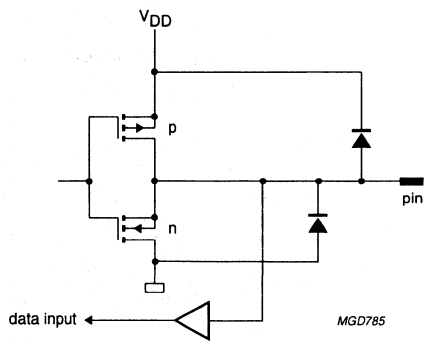


Fig.27 Tri-state port

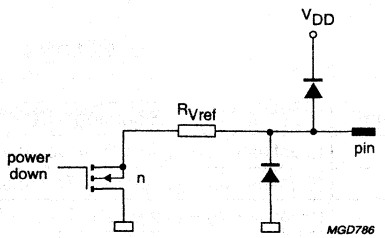


Fig.28 AREF input

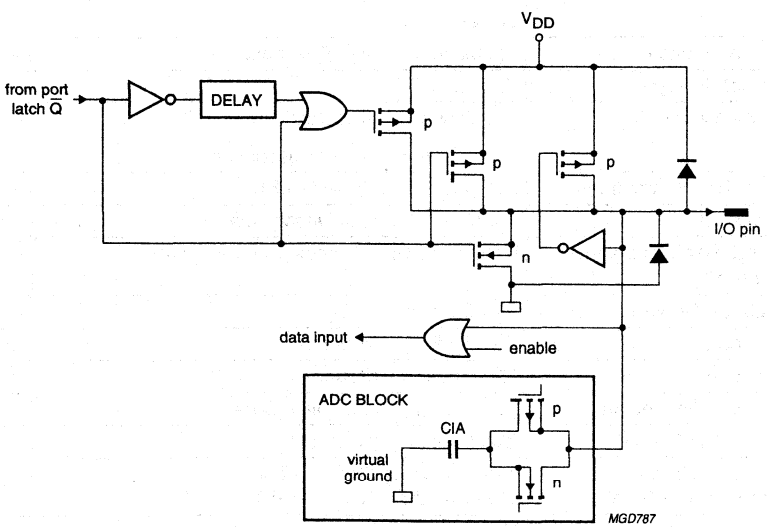


Fig.29 AN +WP2 (P[15-12]) port

27 INSTRUCTION SET AND ADDRESSING MODES

The P90CL301 is completely code compatible with the 68000, which means that programs developed for the 68000 will run on the P90CL301. This applies to both the source and object codes. The instruction set was designed to minimize the number of mnemonics that the programmer has to remember. Following tables give an overview of the instruction set and the different addressing modes.

Table 85 Instruction set; for Condition codes see notes 1 to 7

MNEMONIC	DESCRIPTION	OPERATION	CONDITION CODES				
			X	N	Z	V	C
ABCD	Add Decimal with Extend	$(Destination)_{10} + (Source)_{10} + X \rightarrow Destination$	*	U	*	U	*
ADD	Add Binary	(Destination) + (Source) → Destination	*	*	*	*	*
ADDA	Add Address	(Destination) + (Source) → Destination	–	–	–	–	–
ADDI	Add Immediate	(Destination) + Immediate Data → Destination	*	*	*	*	*
ADDQ	Add Quick	(Destination) + Immediate Data → Destination	*	*	*	*	*
ADDX	Add Extended	(Destination) + (Source) + X → Destination	*	*	*	*	*
AND	AND Logical	(Destination) ∧ (Source) → Destination	–	*	*	0	0
ANDI	AND Immediate	(Destination) ∧ Immediate Data → Destination	–	*	*	0	0
ASL, ASR	Arithmetic Shift	(Destination) Shifted by <count > → Destination	*	*	*	*	*
B_{CC}	Branch Conditionally	If CC then PC + d → PC	–	–	–	–	–
BCHG	Test a Bit and Change	~(< bit number >) of Destination → Z ~(< bit number >) of Destination → < bit number > of Destination	–	–	*	–	–
BCLR	Test a Bit and Clear	~(< bit number >) of Destination → Z	–	–	*	–	–
BRA	Branch Always	PC + d → PC	–	–	–	–	–
BSET	Test a Bit and Set	~(< bit number >) of Destination → Z 1 → < bit number > of Destination	–	–	*	–	–
BSR	Branch to Subroutine	PC → SP @ –; PC + d → PC	–	–	–	–	–
BTST	Test a Bit	~(< bit number >) of Destination → Z	–	–	*	–	–
CHK	Check Register against Bounds	If Dn < 0 or Dn > (< source >) then TRAP	–	*	U	U	U
CLR	Clear an Operand	0 → Destination	–	0	1	0	0
CMP	Compare	(Destination) – (Source)	–	*	*	*	*
CMPA	Compare Address	(Destination) – (Source)	–	*	*	*	*
CMPI	Compare Immediate	(Destination) – Immediate Data	–	*	*	*	*
CMPM	Compare Memory	(Destination) – (Source)	–	*	*	*	*
DB_{cc}	Test Condition, Decrement & Branch	If (not CC) then Dn –1 → Dn; if Dn ≠ –1 then PC + d → PC	–	–	–	–	–
DIVS	Signed Divide	(Destination) / (Source) → Destination	–	*	*	*	0
DIVU	Unsigned Divide	(Destination) / (Source) → Destination	–	*	*	*	0
EOR	Exclusive OR Logical	(Destination) ⊕ (Source) → Destination	–	*	*	0	0
EORI	Exclusive OR Immediate	(Destination) ⊕ Immediate Data → Destination	–	*	*	0	0
EXG	Exchange Register	Rx ↔ Ry	–	–	–	–	–

MNEMONIC	DESCRIPTION	OPERATION	CONDITION CODES				
			X	N	Z	V	C
EXT	Sign Extend	(Destination) Sign – extended → Destination	–	*	*	0	0
JMP	Jump	Destination → PC	–	–	–	–	–
JSR	Jump to Subroutine	PC → SP @ –; Destination → PC	–	–	–	–	–
LEA	Load Effective Address	Destination → An	–	–	–	–	–
LINK	Link and Allocate	An → SP @ –; SP → An; SP + d → SP	–	–	–	–	–
LSL, LSR	Logical Shift	(Destination) Shifted by < count > → Destination	*	*	*	0	*
MOVE	Move Data from Source to Destination	(Source) → Destination	–	*	*	0	0
MOVE to CCR	Move to Condition Code	(Source) → CCR	*	*	*	*	*
MOVE to SR	Move to the Status Register	(Source) → SR	*	*	*	*	*
MOVE from SR	Move from the Status Register	SR → Destination	–	–	–	–	–
MOVE USP	Move User Stack Pointer	USP → An; An → USP	–	–	–	–	–
MOVEA	Move Address	(Source) → Destination	–	–	–	–	–
MOVEM	Move Multiple Registers	Registers → Destination; (Source) → Registers	–	–	–	–	–
MOVEP	Move Peripheral Data	(Source) → Destination	–	–	–	–	–
MOVEQ	Move Quick	Immediate Data → Destination	–	*	*	0	0
MULS	Signed Multiply	(Destination) * (Source) → Destination	–	*	*	*	0
MULU	Unsigned Multiply	(Destination) * (Source) → Destination	–	*	*	*	0
NBCD	Negate Decimal with Extend	$0 - (\text{Destination})_{10} - X \rightarrow$ Destination	*	U	*	U	*
NEG	Negate	0 – (Destination) → Destination	*	*	*	*	*
NEGX	Negate with Extend	0 – (Destination) – X → Destination	*	*	*	*	*
NOP	No Operation	–	–	–	–	–	–
NOT	Logical Complement	~(Destination) → Destination	–	*	*	0	0
OR	Inclusive OR Logical	(Destination) ∨ (Source) → Destination	–	*	*	0	0
ORI	Inclusive OR Immediate	(Destination) ∨ Immediate Data → Destination	–	*	*	0	0
PEA	Push Effective Address	Destination → SP @ –	–	–	–	–	–
RESET	Reset External Devices	–	–	–	–	–	–
ROL, ROR	Rotate (Without Extend)	(Destination) Rotated by < count > → Destination	–	*	*	0	*
ROXL, ROXR	Rotate with Extend	(Destination) Rotated by < count > → Destination	*	*	*	0	*
RTE	Return from Exception	SP @ + → SR; SP @ + → PC	*	*	*	*	*
RTR	Return and Restore Condition Codes	SP @ + → CC; SP @ + → PC	*	*	*	*	*
RTS	Return from Subroutine	SP @ + → PC	–	–	–	–	–
SBCD	Subtract Decimal with Extend	$(\text{Destination})_{10} - (\text{Source})_{10} - X \rightarrow$ Destination	*	U	*	U	*
S_{CC}	Set According to Condition	if CC then 1 → Destination; else 0 → Destination	–	–	–	–	–

MNEMONIC	DESCRIPTION	OPERATION	CONDITION CODES				
			X	N	Z	V	C
STOP	Load Status Register and Stop	Immediate Data → SR; STOP	*	*	*	*	*
SUB	Subtract Binary	(Destination) – (Source) → Destination	*	*	*	*	*
SUBA	Subtract Address	(Destination) – (Source) → Destination	–	–	–	–	–
SUBI	Subtract Immediate	(Destination) – Immediate Data → Destination	*	*	*	*	*
SUBQ	Subtract Quick	(Destination) – Immediate Data → Destination	*	*	*	*	*
SUBX	Subtract with Extend	(Destination) – (Source) – X → Destination	*	*	*	*	*
SWAP	Swap Register Halves	Register [31:16] ↔ Register [15:0]	–	*	*	0	0
TAS	Test and Set an Operand	(Destination) Tested → CC; 1 → [7] of Destination	–	*	*	0	0
TRAP	Trap	PC → SSP @ –; SR → SSP @ –; (Vector) → PC	–	–	–	–	–
TRAPV	Trap on Overflow	If V then TRAP	–	–	–	–	–
TST	Test and Operand	(Destination) Tested → CC	–	*	*	0	0
UNLK	Unlink	An → SP; SP @ + → An	–	–	–	–	–

Notes

1. [ ] = bit number.
2. * = affected.
3. – = unaffected.
4. 0 = cleared.
5. 1 = set.
6. U = defined.
7. @ = location addressed by.

27.1 Addressing modes

Table 86 Data addressing modes; see notes 1 to 14

MODE	GENERATION
Register Direct Addressing	
Data Register Direct	EA = Dn
Address Register Direct	EA = An
Absolute Data Addressing	
Absolute Short	EA = (Next Words)
Absolute Long	EA = (Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA = (PC) + d_{16}
Relative with Index and Offset	EA = (PC) + (Xn) + d_8
Register Indirect Addressing	
Register Indirect	EA = (An)
Postincrement Register Indirect	EA = (An), An ← An + N

MODE	GENERATION
Predecrement Register Indirect	An ← An – N, EA = (An)
Register Indirect with Offset	EA = (An) + d_{16}
Indexed Register Indirect with Offset	EA = (An) + (Xn) + d_8
Immediate Data Addressing	
Immediate	DATA = Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA = SR, USP, SSP, PC, SP

Notes

1. EA = Effective Address.
2. An = Address Register.
3. Dn = Data Register.
4. Xn = Address or Data Register used as Index Register.
5. N = 1 for bytes; 2 for words; 4 for long words.
6. ← = Replaces.
7. SR = Status Register.
8. PC = Program Counter.
9. () = Contents of.
10. d_8 = 8-bit offset (displacement).
11. d_{16} = 16-bit offset (displacement).
12. SP = Stack Pointer.
13. SSP = System Stack Pointer.
14. USP = User Stack Pointer.

28 INSTRUCTION TIMING

In the Tables 87 to 99 the number of bus read and write cycles are shown in parentheses as (R/W). The timing is given for operation in 16-bit mode. For operation in 8-bit mode the numbers shown in parentheses should be multiplied by a factor 2.

Table 87 Effective address calculation times

INSTRUCTION	ADDRESSING MODE	BYTE; WORD	LONG
Rn	Data or Address Register Direct	0 (0/0)	0 (0/0)
(An)	Address Register Indirect	4 (1/0)	8 (2/0)
(An)+	Address Register Indirect postincrement	4 (1/0)	8 (2/0)
–(An)	Address Register Indirect predecrement	7 (1/0)	11 (2/0)
d(An)	Address Register Indirect Displacement	11 (2/0)	12 (3/0)
d(An, Xi)	Address Register Indirect with Index	14 (2/0)	8 (3/0)
xxx.S	Absolute Short	8 (2/0)	12 (3/0)
xxx.L	Absolute Long	12 (3/0)	16 (4/0)
d(PC)	Program Counter with Displacement	11 (2/0)	15 (3/0)
d(PC, Xi)	Program Counter with Index	14 (2/0)	16 (4/0)
#xxx	Immediate	4 (1/0)	8 (2/0)

Table 88 MOVE Byte and MOVE Word Instruction clock periods

INSTR.	Rn	(An)	(An)+	–(An)	d(An)	d(An, Xi)	xxx.S	xxx.L
Rn	7 (1/0)	11 (1/1)	11 (1/1)	14 (1/1)	18 (1/1)	21 (1/1)	15 (1/1)	19 (1/1)
(An)	11 (2/0)	15 (2/1)	15 (2/1)	18 (2/1)	22 (2/1)	25 (2/1)	19 (2/1)	23 (2/1)
(An)+	11 (2/0)	15 (2/1)	15 (2/1)	18 (2/1)	22 (2/1)	25 (2/1)	19 (2/1)	23 (2/1)
–(An)	14 (2/0)	18 (2/1)	18 (2/1)	22 (2/1)	25 (2/1)	28 (2/1)	22 (2/1)	26 (2/1)
d(An)	18 (3/0)	22 (3/1)	22 (3/1)	25 (2/1)	29 (2/1)	32 (2/1)	26 (2/1)	30 (2/1)
d(An, Xi)	21 (3/0)	25 (3/1)	25 (3/1)	28 (3/1)	32 (3/1)	35 (3/1)	29 (3/1)	33 (3/1)
xxx.S	15 (3/0)	19 (3/1)	19 (3/1)	22 (3/1)	26 (3/1)	29 (3/1)	23 (3/1)	27 (3/1)
xxx.L	19 (4/0)	23 (4/1)	23 (4/1)	26 (4/1)	30 (4/1)	33 (4/1)	27 (4/1)	31 (4/1)
d(PC)	18 (3/0)	22 (3/1)	22 (3/1)	25 (3/1)	29 (3/1)	32 (3/1)	26 (3/1)	30 (3/1)
d(PC, Xi)	21 (3/0)	25 (3/1)	25 (3/1)	28 (3/1)	32 (3/1)	35 (3/1)	29 (3/1)	33 (3/1)
#xxx	11 (3/0)	15 (2/1)	15 (2/1)	18 (2/1)	22 (2/1)	25 (2/1)	19 (2/1)	23 (2/1)

Table 89 MOVE long instruction clock periods

INSTR.	Rn	(An)	(An)+	–(An)	d(An)	d(An, Xi)	xxx.S	xxx.L
Rn	7 (1/0)	15 (1/2)	15 (1/2)	18 (1/2)	22 (2/2)	25 (2/2)	19 (2/2)	23 (3/2)
(An)	15 (2/0)	23 (2/2)	23 (2/2)	26 (2/2)	30 (4/2)	33 (4/2)	27 (4/2)	31 (5/2)
(An)+	15 (3/0)	23 (3/2)	23 (3/2)	26 (3/2)	30 (4/2)	33 (4/2)	27 (4/2)	31 (5/2)
–(An)	18 (3/0)	26 (3/2)	26 (3/2)	29 (3/2)	33 (4/2)	36 (4/2)	30 (4/2)	34 (5/2)
d(An)	22 (4/0)	30 (4/2)	30 (4/2)	33 (4/2)	37 (5/2)	40 (5/2)	34 (5/2)	38 (6/2)
d(An, Xi)	25 (4/0)	33 (4/2)	33 (4/2)	36 (4/2)	40 (5/2)	43 (5/2)	37 (5/2)	41 (6/2)
xxx.S	19 (4/0)	27 (4/2)	27 (4/2)	30 (4/2)	34 (5/2)	37 (5/2)	31 (5/2)	35 (6/2)
xxx.L	23 (5/0)	31 (5/2)	31 (5/2)	34 (5/2)	38 (6/2)	41 (6/2)	35 (6/2)	39 (7/2)
d(PC)	22 (4/0)	30 (4/2)	30 (4/2)	33 (4/2)	37 (5/2)	40 (5/2)	34 (5/2)	38 (6/2))
d(PC, Xi)	25 (4/0)	33 (4/2)	33 (4/2)	36 (4/2)	40 (5/2)	43 (5/2)	37 (5/2)	41 (6/2)
#xxx	15 (3/0)	23 (3/2)	23 (3/2)	26 (3/2)	30 (4/2)	33 (4/2)	27 (4/2)	31 (5/2)

Table 90 Standard Instruction clock periods

INSTRUCTION	SIZE	op<ea>, An	op<ea>, Dn	op<ea>, M
ADD	Byte, Word	7(1) (1/0)	7(1) (1/0)	11(1) (1/1)
	Long	7(1) (1/0)	7(1) (1/0)	15(1) (1/2)
AND	Byte, Word	–	7(1) (1/0)	11(1) (1/1)
	Long	–	7(1) (1/0)	15(1) (1/2)
CMP	Byte, Word	7(1) (1/0)	7(1) (1/0)	–
	Long	7(1) (1/0)	7(1) (1/0)	–
DIVS	–	–	169(1)(2) (1/0)	–
DIVU	–	–	130(1)(3) (1/0)	–
EOR	Byte, Word	–	7(1) (1/0)	11(1) (1/1)
	Long	–	7(1) (1/0)	15(1) (1/2)
MULS	–	–	76(1)(3) (1/0)	–
MULU	–	–	76(1)(3) (1/0)	–
OR	Byte, Word	–	7(1) (1/0)	11(1) (1/1)
	Long	–	7(1) (1/0)	15(1) (1/2)
SUB	Byte, Word	7(1) (1/0)	7(1) (1/0)	11(1) (1/1)
	Long	7(1) (1/0)	7(1) (1/0)	15(1) (1/2)

Notes

1. Add effective address calculation time.
2. Indicates maximum value.
3. The duration of the instruction is constant.

Table 91 Immediate instruction clock periods

INSTRUCTION	SIZE	op<#>, Dn	op<#>, An	op<#>, M
ADDI	Byte, Word	14 (2/0)	–	18[1] (2/1)
	Long	18 (3/0)	–	26[1] (3/2)
ADDQ	Byte, Word	7[1] (1/0)	7[1] (1/0)	11[1] (1/1)
	Long	7[1] (1/0)	7[1] (1/0)	15[1] (1/2)
ANDI	Byte, Word	14 (2/0)	–	18[1] (2/1)
	Long	18 (3/0)	–	26[1] (3/2)
CMPI	Byte, Word	14 (2/0)	–	14 (2/0)
	Long	18 (3/0)	–	18 (3/0)
EORI	Byte, Word	14 (2/0)	–	18[1] (2/1)
	Long	–	–	26[1] (3/2)
MOVEQ	Long	7 (1/0)	–	–
ORI	Byte, Word	14 (2/0)	–	18[1] (2/1)
	Long	18 (3/0)	–	26[1] (3/2)
SUBI	Byte, Word	14 (2/0)	–	18[1] (2/1)
	Long	18 (3/0)	–	26[1] (3/2)
SUBQ	Byte, Word	7[1] (1/0)	7 (1/0)	11[1] (1/1)
	Long	7[1] (1/0)	7 (1/0)	15[1] (1/2)

Note

1. Add effective address calculation time.

Table 92 Shift/rotate instruction clock periods

INSTRUCTION	SIZE	REGISTER	MEMORY
ASR, ASL	Byte	13 + 3n (1/0)	14 (1/1)[1]
	Word	13 + 3n (1/0)	–
LSR, LSL	Byte, Word	13 + 3n (1/0)	14 (1/1)[1]
	Long	13 + 3n (1/0)	–
ROR, ROL	Byte, Word	13 + 3n (1/0)	14 (1/1)[1]
	Long	13 + 3n (1/0)	–
ROXR, ROXL	Byte, Word	13 + 3n (1/0)	14 (1/1)[1]
	Long	13 + 3n (1/0)	–

Note

1. Add effective address calculation time.

Table 93 Single operand instruction clock periods

INSTRUCTION	SIZE	REGISTER	MEMORY
CLR	Byte, Word	7 (1/0)	11 (1/1)[1][2]
	Long	7 (1/0)	15 (1/2)[1][3]
NBCD	Byte, Word	10 (1/0)	14 (1/1)[1]
NEG	Byte, Word	7 (1/0)	11 (1/1)[1]
	Long	7 (1/0)	15 (1/2)[1]
NEGX	Byte, Word	7 (1/0)	11 (1/1)[1]
	Long	7 (1/0)	15 (1/2)[1]
NOT	Byte, Word	7 (1/0)	11 (1/1)[1]
	Long	7 (1/0)	15 (1/2)[1]
Scc	Byte, Word	13 (1/0)	17 (1/1)[1]
	Long	13 (1/0)	14 (1/1)[1]
TAS	Byte	10 (1/0)	15 (2/1)[1][2]
TST	Byte, Word	7 (1/0)	7 (1/0)[1]
	Long	7 (1/0)	7 (1/0)[1]

Notes

1. Add effective address calculation time.
2. Subtract one read cycle (–4(1/0)) from effective address calculation.
3. Subtract two read cycles (–8(2/0)) from effective address calculation.

Table 94 Bit manipulation instruction clock periods

INSTRUCTION	SIZE	DYNAMIC		STATIC	
		REGISTER	MEMORY	REGISTER	MEMORY
BCHG	Byte	–	14 (1/1)[1]	–	21 (2/1)[1]
	Long	10 (1/0)	–	17 (2/0)	–
BCLR	Byte	–	14 (1/1)[1]	–	21 (2/1)[1]
	Long	10 (1/0)	–	17 (2/0)	–
BSET	Byte	–	14 (1/1)[1]	–	21 (2/1)[1]
	Long	10 (1/0)	–	17 (2/0)	–
BTST	Byte	–	7 (1/0)[1]	–	14 (2/0)[1]
	Long	7 (1/0)	–	14 (2/0)	–

Note

1. Add effective address calculation time.

Table 95 Conditional instruction clock periods

INSTRUCTION	DISPLAY	TRAP OR BRANCH	
		TAKEN	NOT TAKEN
Bcc	Byte	13 (1/0)	13 (1/0)
	Word	14 (2/0)	14 (2/0)
BRA	Byte	13 (1/0)	–
	Word	14 (2/0)	–
BSR	Byte	21 (1/2)	–
	Word	22 (2/2)	–
DBcc	cc True	–	14 (2/0)
	cc False	17 (2/0)	17 (3/2)
CHK	–	70 (3/4)(1)	19 (1/0)(1)
TRAPV	–	55 (3/4)	10 (1/0)

Note

1. Add effective address calculation time.

Table 96 JMP, JSR, LEA, PEA, MOVEM instruction clock periods
n = number of registers to move.

INSTRUCTION	SIZE	(An)	(An)+	–(An)	d(An)	d(An, Xi)	xxx.S	xxx.L	d(PC)	d(PC, Xi)
JMP	–	7 (1/0)	–	–	14 (2/0)	17 (2/0)	14 (2/0)	18 (3/0)	14 (2/0)	17 (2/0)
JSR	–	18 (1/2)	–	–	25 (2/2)	28 (2/2)	25 (2/2)	28 (2/2)	25 (2/2)	28 (2/2)
LEA	–	7 (1/0)	–	–	14 (2/0)	17 (2/0)	14 (2/0)	18 (3/0)	14 (2/0)	17 (2/0)
PEA	–	18 (1/2)	–	–	25 (2/2)	28 (2/2)	25 (2/2)	28 (2/2)	25 (2/2)	28 (2/2)
MOVEM M → R	Word	26+7n (2+n/0)	26+7n (2+n/0)	–	30+7n (3+n/0)	33+7n (3+n/0)	30+7n (3+n/0)	34+7n (4+n/0)	30+7n (3+n/0)	33+7n (3+n/0)
	Long	26+11n (2+2n/0)	26+11n (2+2n/0)	–	30+11n (3+2n/0)	33+11n (3+2n/0)	30+11n (3+2n/0)	34+11n (4+2n/0)	30+11n (3+2n/0)	33+11n (3+2n/0)
MOVEM R → M	Word	23+7n (2/n)	–	23+7n (2/n)	27+7n (3/n)	30+7n (3/n)	27+7n (3/n)	31+7n (4/n)	–	–
	Long	23+11n (2/2n)	–	23+11n (2/2n)	27+11n (3/2n)	30+11n (3/2n)	27+11n (3/2n)	31+11n (4/2n)	–	–

Table 97 Multi-precision Instruction Clock Periods

INSTRUCTION	SIZE	op Dn, An	op M, M
ADDX	Byte, Word	7 (1/0)	28 (3/1)
	Long	7 (1/0)	40 (5/2)
CMPM	Byte, Word	–	18 (3/0)
	Long	–	26 (5/0)
SUBX	Byte, Word	7 (1/0)	28 (3/1)
	Long	7 (1/0)	40 (5/2)
ABCD	Byte	10 (1/0)	31 (3/1)
SBCD	Byte	10 (1/0)	31 (3/1)

Table 98 Miscellaneous Clock Periods

INSTRUCTION	SIZE	REGISTER	MEMORY	REGISTER TO MEMORY	MEMORY TO REGISTER
ANDI to CCR	–	14 (2/0)	–	–	–
ANDI to SR	–	14 (2/0)	–	–	–
EORI to CCR	–	14 (2/0)	–	–	–
EORI to SR	–	14 (2/0)	–	–	–
EXG	–	13 (2/0)	–	–	–
EXT	Word	7 (1/0)	–	–	–
	Long	7 (1/0)	–	–	–
LINK	–	25 (2/2)	–	–	–
MOVE from SR	–	7 (1/0)	11 (1/1)[1]	–	–
MOVE to CCR	–	10 (1/0)	10 (1/0)[1]	–	–
MOVE to SR	–	10 (1/0)	10 (1/0)[1]	–	–
MOVE from USP	–	7 (1/0)	–	–	–
MOVE to USP	–	7 (1/0)	–	–	–
MOVEP	Word	–	–	25 (2/2)	22 (4/0)
	Long	–	–	39 (2/4)	36 (6/0)
NOP	–	7 (1/0)	–	–	–
ORI to CCR	–	14 (2/0)	–	–	–
ORI to SR	–	14 (2/0)	–	–	–
RESET	–	154 (1/0)	–	–	–
RTE short format	–	–	–	–	–
RTE long format					–
no rerun	–	140 (18/0)	–	–	–
with rerun	–	146 (18/0)	–	–	–
return of TAS	–	151 (19/0)	–	–	–
RTR	–	22 (4/0)	–	–	–
RTS	–	15 (3/0)	–	–	–
STOP	–	17 (2/0)	–	–	–
SWAP	–	7 (1/0)	–	–	–
UNLK	–	15 (3/0)	–	–	–

Note

1. Add effective address calculation time.

Table 99 Exception processing clock periods

EXCEPTION	NUMBER OF CLOCK PERIODS
Address error	158 (3/17)
Bus error	158 (3/17)
Interrupt	65 (4/4)[1]
Illegal instruction	55 (3/4)
Privilege instruction	55 (3/4)
Trace	55 (3/4)
Trap	52 (3/4)
Divide by zero	64 (3/4)[2]
RESET[3]	43 (4/0)

Notes

1. The interrupt acknowledge bus cycle is assumed to take four external clock periods.
2. Add effective address calculation time.
3. Indicates the maximum time from when $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ are first sampled as negated to first instruction fetch.

NOTES

Section 13
Clock/Calendar

CONTENTS

PCF8593 Low power clock calendar; 12C–bus 13–3

Low power clock calendar PCF8593

FEATURES

- I²C-bus interface operating supply voltage: 2.5 to 6.0 V
- Clock operating supply voltage (T_{amb} = 0 to +70 °C): 1.0 to 6.0 V
- Data retention voltage: 1.0 to 6.0 V
- External $\overline{RESET}$ input pin
- Operating current (f_{scl} = 0 Hz, 32 kHz time base, V_{DD} = 2.0 V): typ. 1 µA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C-bus)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Space-saving SO8 package
- Slave address:
  - READ A3H
  - WRITE A2H.

GENERAL DESCRIPTION

The PCF8593 is a CMOS Real-time clock/calendar optimized for low power consumption. Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. The built-in 32.768 kHz oscillator circuit and the first 8 registers are used for the clock/calendar and counter functions. The next 8 registers may be programmed as alarm registers or used as free RAM space.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	6.0	V
		I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz	–	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	4.0	15.0	µA
		f_{scl} = 0 Hz; V_{DD} = 2 V	1.0	8.0	µA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8593P	8	DIL	plastic	SOT97-1
PCF8593T	8	SO8	plastic	SOT96-1

BLOCK DIAGRAM

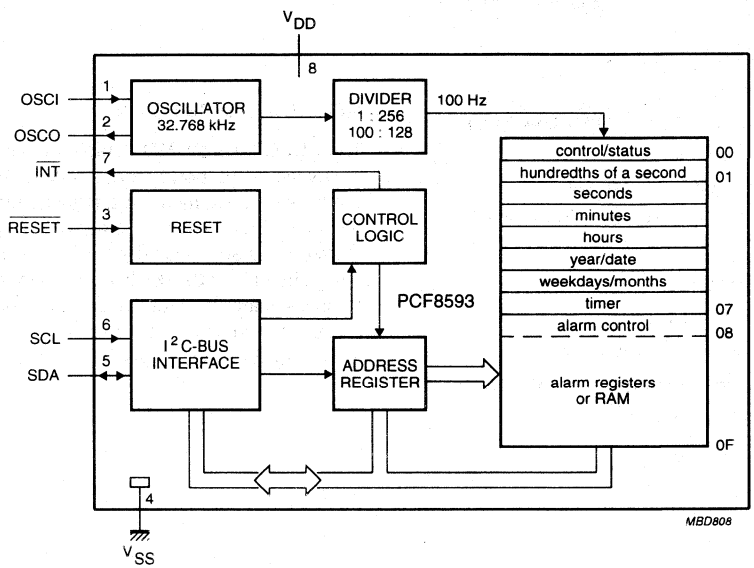


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
$\overline{\text{RESET}}$	3	reset input (active LOW)
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
$\overline{\text{INT}}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

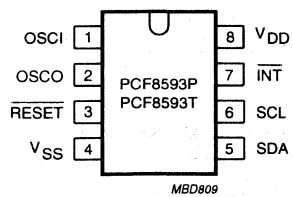


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The PCF8593 contains sixteen 8-bit registers with an 8-bit auto-incrementing address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider and a serial two-line bidirectional I²C-bus interface.

The first 8 registers (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F may be programmed as alarm registers or used as free RAM locations.

Counter function modes

When the control/status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and week day are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a week day alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open-drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When a timer function without any function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I²C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

Counter registers

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig 6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

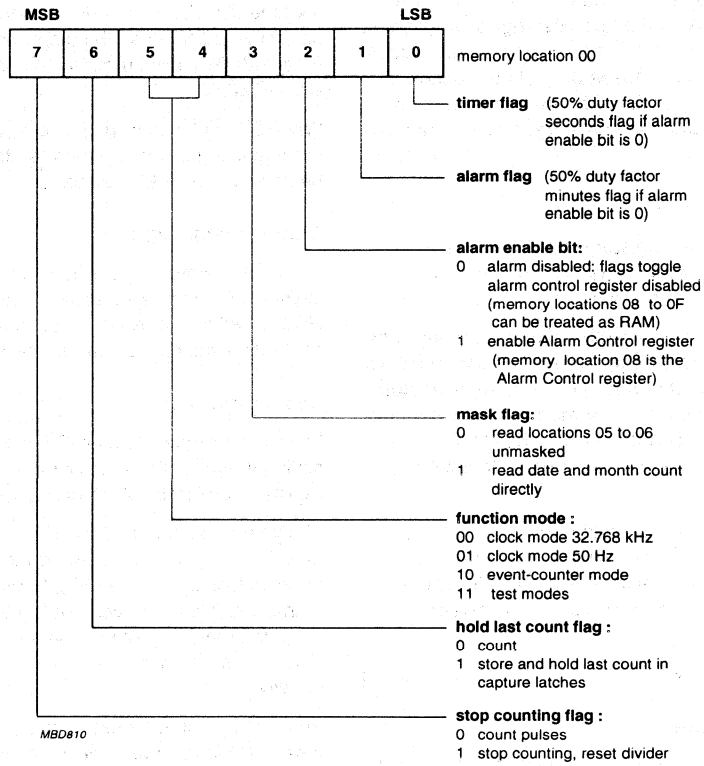


Fig.3 Control/status register.

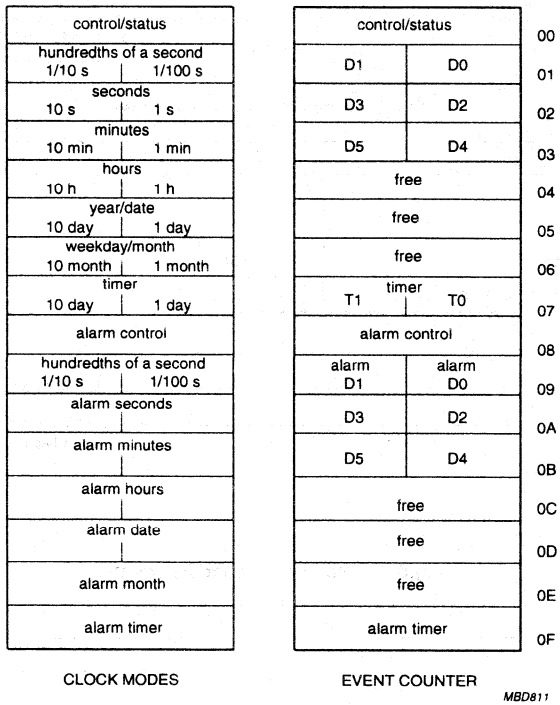


Fig.4 Register arrangement.

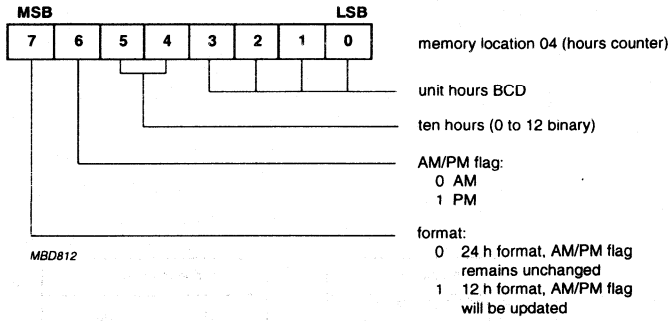


Fig.5 Format of the hours counter.

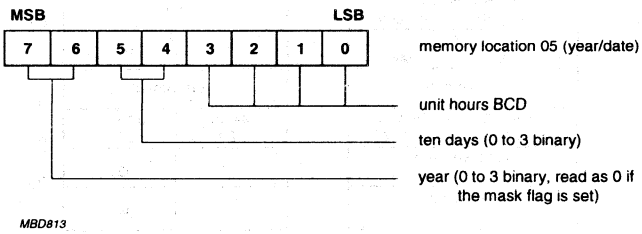


Fig.6 Format of the year/date counter.

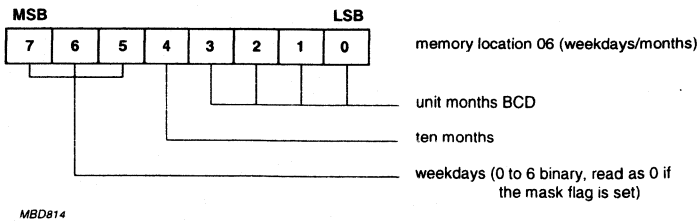


Fig.7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes.

UNIT	COUNTING CYCLE	CARRY TO NEXT UNIT	CONTENTS OF THE MONTH COUNTER
Hundredths of a second	00 to 99	99 to 00	–
Seconds	00 to 59	59 to 00	–
Minutes	00 to 59	59 to 00	–
Hours (24 h)	00 to 23	23 to 00	–
Hours (12 h)	12 AM	–	–
	01 AM to 11 AM	–	–
	12 PM	–	–
	01 PM to 11 PM	11 PM to 12 AM	–
Date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10 and 12
	01 to 30	30 to 01	4, 6, 9 and 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2 and 3
Months	01 to 12	12 to 01	–
Year	0 to 3	–	–
Weekdays	0 to 6	6 to 0	–
Timer	00 to 99	no carry	–

Alarm control register

When the alarm enable bit of the control/status register is set (address 00, bit 2) the alarm control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Fig.8).

Alarm registers

All alarm registers are allocated with a constant address offset of hexadecimal 08 to the corresponding counter registers (see Fig.4; Register arrangement).

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Remark: in the 12 h mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

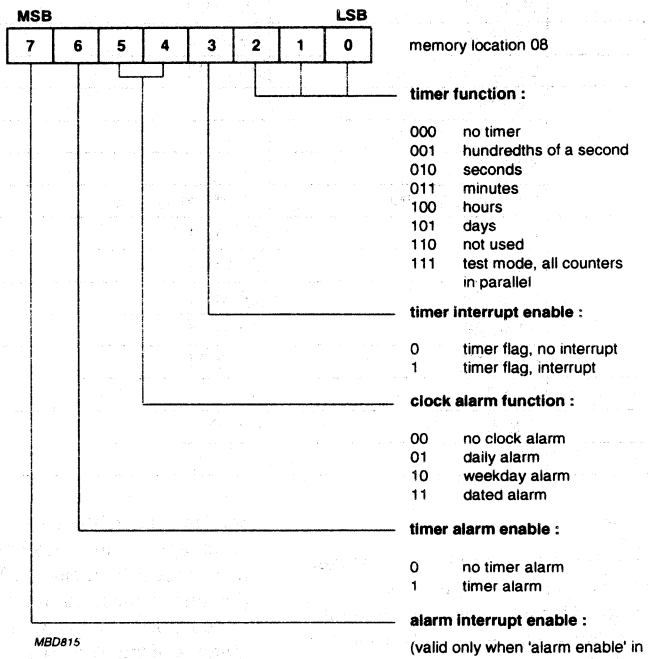


Fig.8 Alarm control register; clock mode.

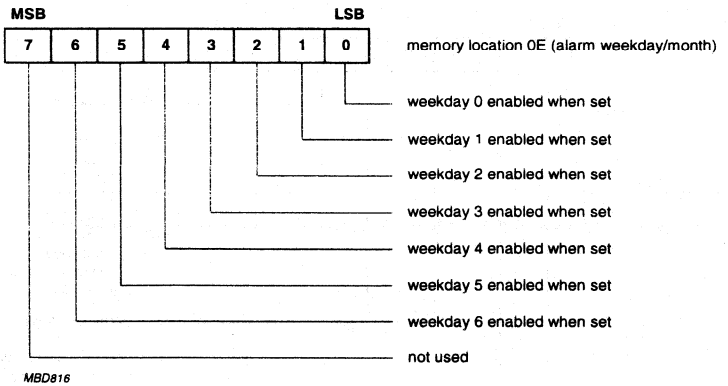


Fig.9 Selection of alarm weekdays.

Timer

The timer (location 07) is enabled by setting the control/status register = XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The timer flag (LSB of control/status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the alarm control register.

Additionally, a timer alarm can be programmed by setting the timer alarm enable (bit 6 of the alarm control register). When the value of the timer equals a pre-programmed value in the alarm timer register (location 0F), the alarm flag is set (bit 1 of the control/status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the alarm interrupt (bit 6 of the alarm control register).

Resolution of the timer is programmed via the 3 LSBs of the alarm control register (see Fig.11; Alarm and timer Interrupt logic diagram).

Event counter mode

Event counter mode is selected by bits 4 and 5 which are logic 1, 0 in the control/status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in locations 1, 2, and 3. Thus, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in locations 9, A, and B, and the event alarm is enabled (bits 4 and 5 which are logic 0, 1 in the alarm control register). In this event, the alarm flag (bit 1 of the control/status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the alarm interrupt enable in the alarm control register. In this mode, the timer (location 07) increments once for every one, one-hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0,1 and 2 of the alarm control register. In all other events, the timer functions are as in the clock mode.

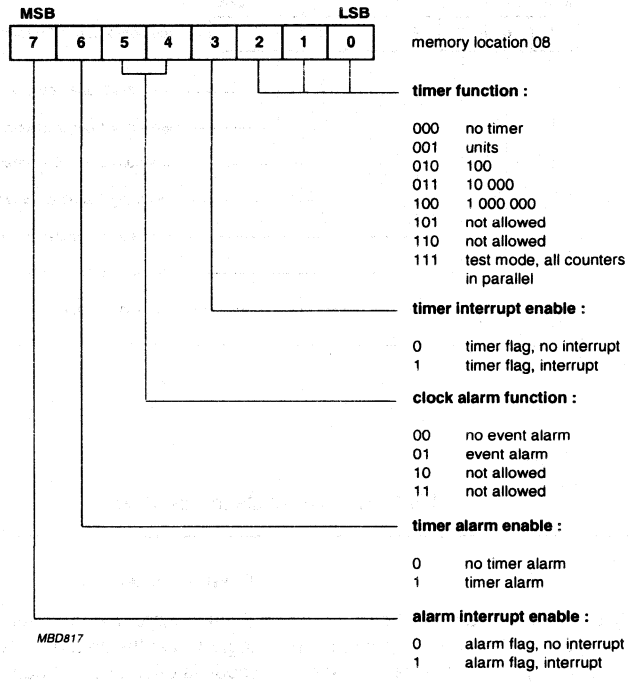
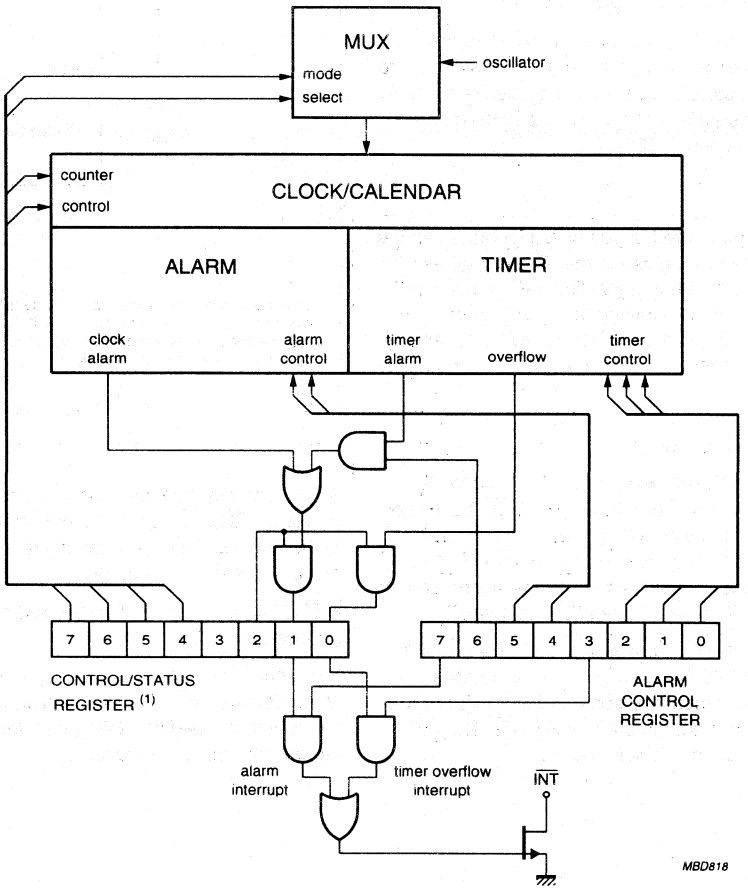


Fig.10 Alarm control register; event-counter mode.

Interrupt output

The conditions for activating the open-drain n-channel interrupt output $\overline{INT}$ (active LOW) are determined by appropriate programming of the alarm control register. These conditions are clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all events, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

In the clock mode, if the alarm enable is not activated (alarm enable bit of control/status register is logic 0), the interrupt output toggles at 1 Hz with a 50% duty cycle (may be used for calibration). The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Fig.11.



(1) If the alarm enable bit of the control/status register is reset (logic 0), a 1 Hz signal can be observed on the interrupt pin $\overline{INT}$.

Fig.11 Alarm and timer interrupt logic diagram.

Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see Chapter "Application information" ; Section "Quartz frequency adjustment"). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high-impedance state. This allows the user to feed the 50 Hz reference frequency or an external high-speed event signal into the input OSCI.

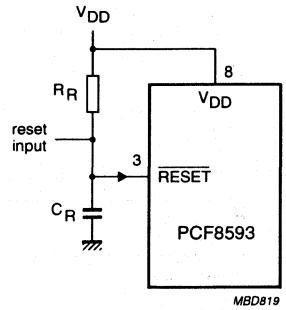
DESIGNING

When designing the printed-circuit board layout, keep the oscillator components as close to the IC package as possible, and keep all other signal lines as far away as possible. In applications involving tight packing of components, shielding of the oscillator may be necessary. AC coupling of extraneous signals can introduce oscillator inaccuracy.

Initialization (see Fig.12)

Note that immediately following power-on, all internal registers are undefined and, following a $\overline{\text{RESET}}$ pulse on pin 3, must be defined via software. Attention should be paid to the possibility that the device may be initially in event-counter mode, in which event the oscillator will not operate. Over-ride can be achieved via software.

Reset is accomplished by applying an external $\overline{\text{RESET}}$ pulse (active LOW) at pin 3. When reset occurs the I^2C-bus interface is reset. The control/status register and all clock counters are not affected by $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ must return HIGH during device operation.



To avoid overload of the internal diode by falling V_{DD}, an external diode should be added in parallel to R_R if $C_R \geq 0.2$ µF. Note that RC must be evaluated with the actual V_{DD} of the application, as their value will be V_{DD} rise-time dependent.

Fig.12 RC reset.

An RC combination can also be utilized to provide a power-on $\overline{\text{RESET}}$ signal at pin 3. In this event, the values of the RC must fulfil the following relationship to guarantee power-on reset (see Fig.12).

$\overline{\text{RESET}}$ input must be $\leq 0.3V_{DD}$ when V_{DD} reaches V_{DDmin} (or higher).

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

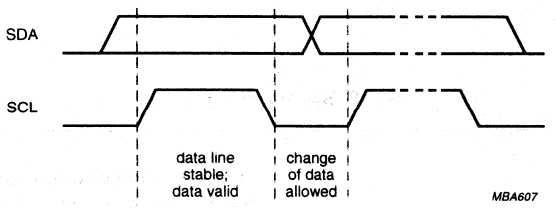


Fig.13 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

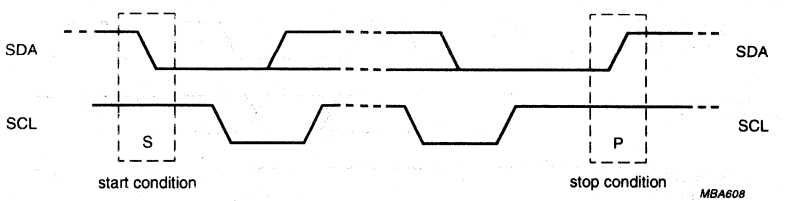


Fig.14 Definition of start and stop conditions.

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

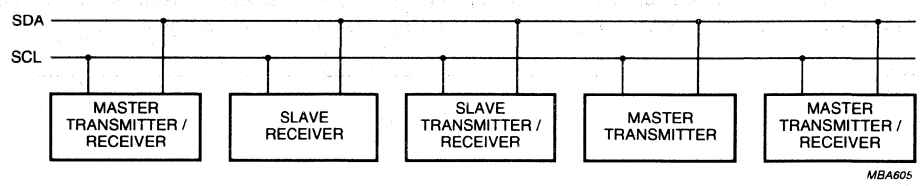


Fig.15 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

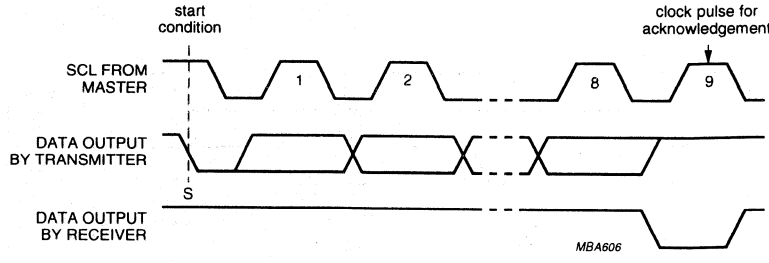


Fig.16 Acknowledgement on the I^2C-bus.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8593 READ and WRITE cycles is shown in Figs 17, 18 and 19.

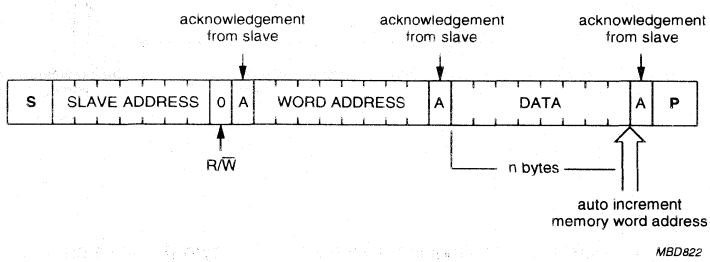


Fig.17 Master transmits to slave receiver (WRITE) mode.

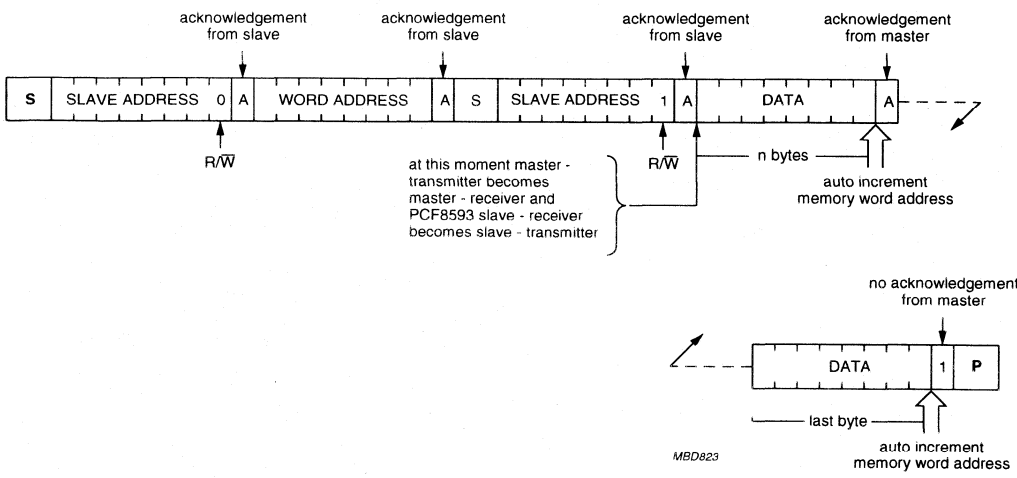


Fig.18 Master reads after setting word address (write word address; READ data).

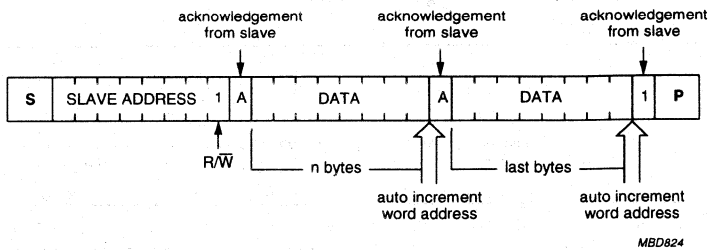


Fig.19 Master reads slave immediately after first byte (READ mode).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.8	+7.0	V
I_{DD}	supply current (pin 8)	−	50	mA
I_{SS}	supply current (pin 4)	−	50	mA
V_I	input voltage	−0.8	V_{DD} + 0.8	V
I_I	DC input current	−	10	mA
I_O	DC output current	−	10	mA
P_{tot}	total power dissipation per package	−	300	mW
P_O	power dissipation per output	−	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

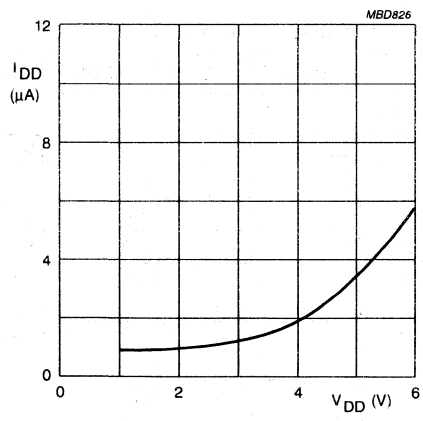
V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; f_{osc} = 32 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Supply						
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	−	6.0	V
		I²C-bus inactive	1.0	−	6.0	V
V_{DDosc}	quartz oscillator supply voltage	T_{amb} = 0 to 70 °C; note 2	1.0	−	6.0	V
		T_{amb} = −40 to 85 °C; note 2	1.2	−	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz; clock mode; note 3	−	−	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 2 V; inputs at V_{DD} or V_{SS}	−	1.0	8.0	µA
		f_{scl} = 0 Hz; V_{DD} = 5 V; inputs at V_{DD} or V_{SS}	−	4.0	15	µA
SDA, SCL, $\overline{INT}$ and RESET						
V_{IL}	LOW level input voltage		0	−	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	−	V_{DD}	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	−	−	mA
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	−1	−	+1	µA
C_I	input capacitance	note 4	−	−	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
OSCI and $\overline{\text{RESET}}$						
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−250	–	+250	nA
$\overline{\text{INT}}$						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1	–	–	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
SCL						
C_I	input capacitance	note 4	–	–	7	pF
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA

Notes

1. Typical values measured at 25 °C.
2. When powering up the device, V_{DD} must exceed the specified minimum value by 300 mV to guarantee correct start-up of the oscillator.
3. Event counter mode; supply current dependent upon input frequency.
4. Tested on sample basis.



f_{SCL} = 32 kHz; T_{amb} = 25 °C.

Fig.20 Typical supply current in clock mode as a function of supply voltage.

AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_{osc}	integrated oscillator capacitance		20	25	30	pF
Δf_{osc}	oscillator stability	for ΔV_{DD} = 100 mV; T_{amb} = 25 °C; V_{DD} = 1.5 V	–	2×10^{-7}	–	
f_i	input frequency	note 1	–	–	1	MHz
Quartz crystal parameters (f = 32.768 kHz)						
R_S	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
I²C-bus timing (see Fig.21; notes 2 and 3)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SP}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	start condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid		–	–	3.4	µs
$t_{SU;STO}$	stop condition set-up time		4.0	–	–	µs

Notes

1. Event counter mode only.
2. All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

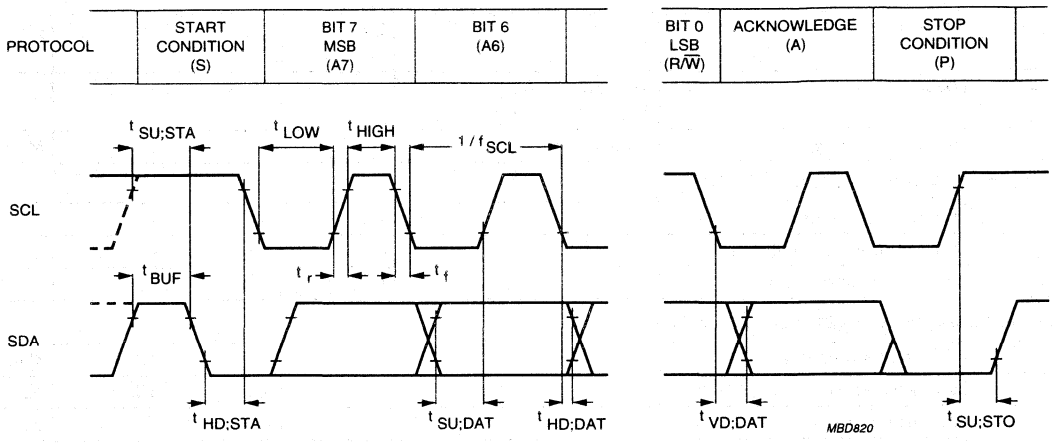


Fig.21 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

Quartz frequency adjustment

METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal which can be programmed to occur at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be achieved.

METHOD 2: OSCI TRIMMER

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

- Power-on
- Apply $\overline{\text{RESET}}$
- Initialization (alarm functions).

Routine:

- Set clock to time T and set alarm to time T + ΔT
- At time T + ΔT (interrupt) repeat routine.

METHOD 3: DIRECT OUTPUT

Direct measurement of oscillator output (accounting for test probe capacitance).

Slave address

The PCF8593 has an internally fixed I²C-bus slave address.

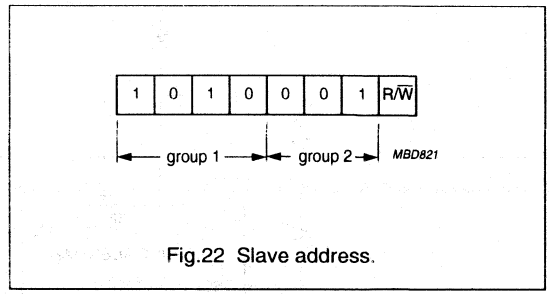
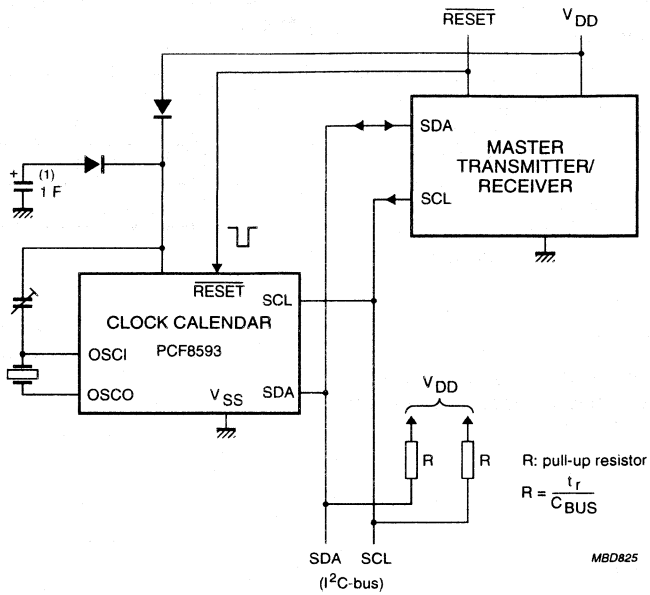


Fig.22 Slave address.



(1) Example Philips DLC 196 Double-Layer Capacitor family.

Fig.23 Application diagram.

Section 14
Battery Management

CONTENTS

SAA1501T	Battery charge level indicator	14–3
TEA1102; TEA1102T	Fast charge IC for NICd, NiMH, SLA and Lilon	14–19
TEA1104; TEA1104T	Cost effective battery monitor and fast charge IC for NICd and NiMH chargers	14–39
PCF1252–X family	Threshold detector and reset generator	14–49

Battery charge level indicator SAA1501T

FEATURES

- High level of integration to allow assembly in intelligent battery packs
- Accurate charge and discharge account
- Large dynamic range of charge and discharge currents
- Independent settings of charge and discharge efficiency
- 2 V minimum supply voltage (2 cell operation)
- Temperature protection of batteries during charging
- Temperature controlled self-discharge
- Accurate charge current regulation
- Two charge amount display modes, LCD and LED.

GENERAL DESCRIPTION

The SAA1501T is intended to be used as a battery monitor and charge current control circuit in rechargeable battery systems.

The SAA1501T is processed in BiCMOS technology where the benefits of mixed bipolar and CMOS technology is fully utilized to achieve high accuracy measurements and digital signal processing in the same device. The general function of the integrated circuit is a Coulomb counter. During battery charging, the charge current and charge time are registered in a Coulomb counter. During discharge, the discharge current and time are recorded. The momentary charge amount of the batteries can be displayed either on an LCD screen or on an LED bargraph. Using the SAA1501T, intelligent batteries or intelligent battery powered systems can be easily designed with only a few external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.0	3.0	4.3	V
I_{CC}	supply current	V_{CC} = 3 V; $I_c = I_d$ = 60 µA	–	1.2	1.7	mA
I_{CCstb}	supply current in standby mode	V_{CC} = 3 V; $V_{CSI} = V_{DSI}$ = 0 V	–	–	100	µA
f_{osc}	fixed oscillator frequency	C_{osc} = 820 pF; R_{ref} = 51.5 kΩ	–	4.2	–	kHz
$V_{i(s)}$	input sense voltage (pins 9 and 10)		0	–	V_{CC} – 1.6	V
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA1501T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

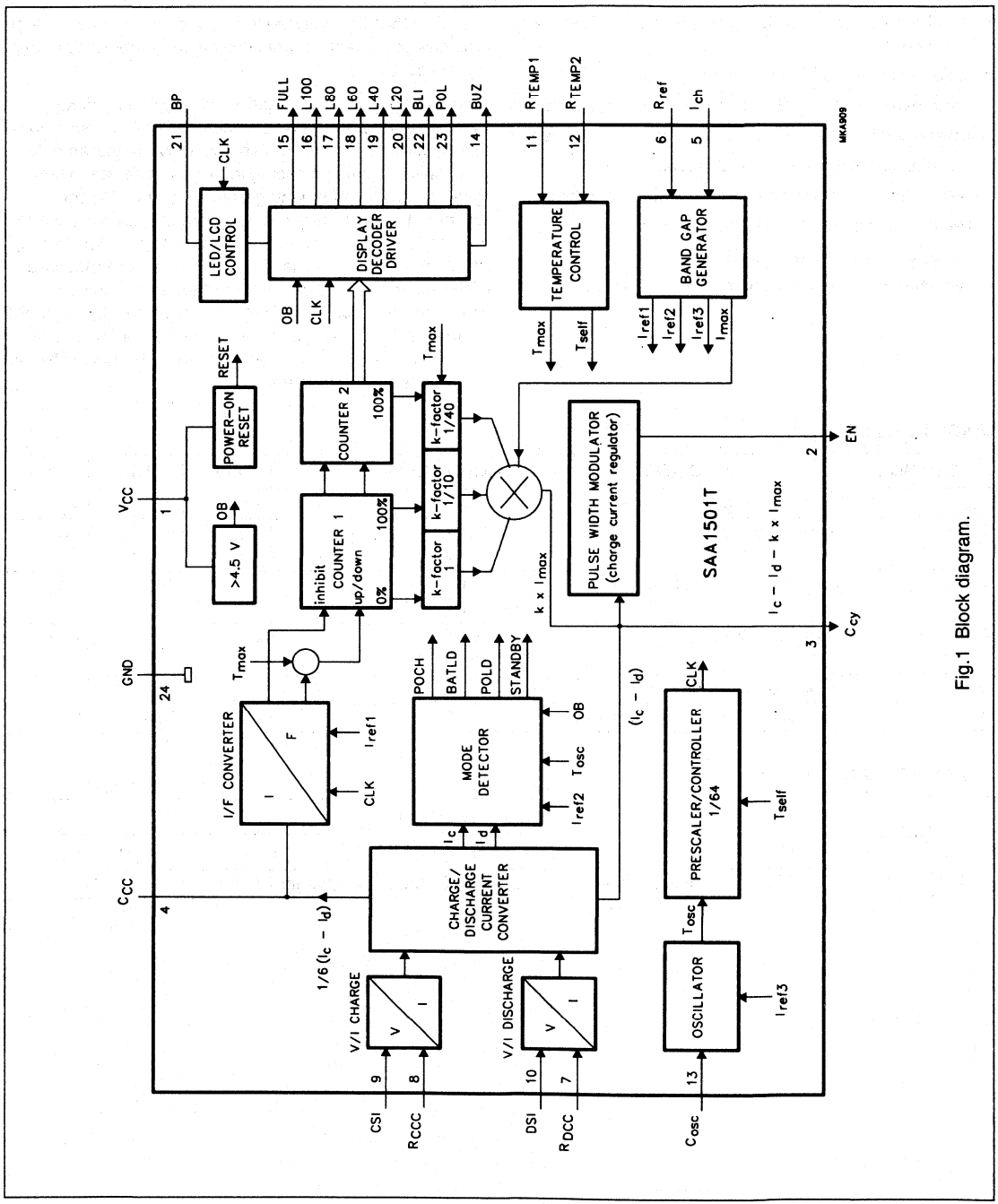


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CC}	1	supply voltage
EN	2	enable output
C_{cy}	3	duty cycle capacitor output
C_{CC}	4	charge counter capacitor output
I_{ch}	5	maximum average charge current setting input
R_{ref}	6	current reference resistor input
R_{DCC}	7	discharge current conversion resistor input
R_{CCC}	8	charge current conversion resistor input
CSI	9	charge sense input
DSI	10	discharge sense input
R_{TEMP1}	11	temperature sensing resistor 1 input
R_{TEMP2}	12	temperature sensing resistor 2 input
C_{osc}	13	oscillator capacitor input
BUZ	14	buzzer output
FULL	15	battery full indication output
L100	16	100% segment indication output
L80	17	80% segment indication output
L60	18	60% segment indication output
L40	19	40% segment indication output
L20	20	20% segment indication output
BP	21	LCD back plane drive
BLI	22	battery low indicator LED output
POL	23	power-on LED output
GND	24	power ground

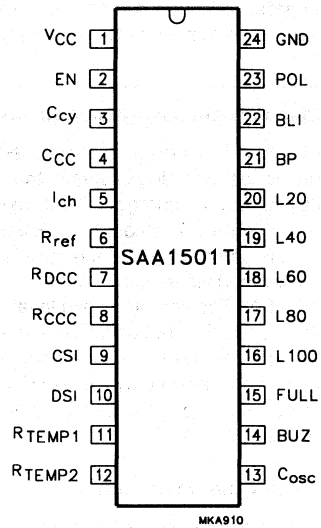


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The most important function of the SAA1501T is the charge account in rechargeable battery systems. Both NiCd and NiMH batteries in all sizes can be used. The system can operate alone as a charge monitor with a charge amount display function or, can operate in conjunction with a charger. If the SAA1501T operates together with a charger, it delivers a control signal at output EN, for charge current regulation or for battery voltage regulation.

Fast charging systems and charge current regulation

The SAA1501T is especially designed to be used in fast charging systems. In fast charging systems, the charge time is lowered by raising the charge current. Signal EN controls the charger current. The counters register the state of charge of the batteries and at the 80% level the charge current is reduced via a smaller duty cycle regulation of signal EN. The second (slow) level fully charges the batteries which is not possible with the first (fast) level. After the slow charge mode the counter switches over to an even smaller duty cycle of EN and thus enters the third (trickle) charge mode, to overcome the self-discharge of the batteries.

Current sensing and charge account

The charge current is sensed by means of a very low resistance (e.g. 70 mΩ) sense resistor R_{sc} (see Fig.8) to save power at high charge rates. Via the V/I charge converter and external resistor R_{CCC} (see Fig.8), the sensed voltage is converted into a charge current I_c (the same is applicable for the discharge current). In the I/F converter the charge current is converted into a frequency for up-counting the counter. For the discharge current (I_d) the converted frequency is used for down-counting. The up and down counting is registered in counters CNT1 and CNT2, depending on the actual charge and discharge current levels of the batteries. This is called dynamic charge account.

Charge display

The charge amount represented by the Coulomb counter can be displayed via an LCD screen or via an LED bargraph. If the charge amount is reduced to 0%, the battery low indicator (BLI) LED is turned on at the end of a battery discharge session. A flashing BLI, in combination with a repeating buzzer alarm, informs the user about the low charge state. A new charge session should then be started.

Protections

In the temperature control block, the absolute temperature is used as a protection to end the fast charge cycle. Fast charging at high temperature is not permitted because of degradation of the battery cells. If the batteries are disconnected, an open-battery condition is recognized and the SAA1501T enters the standby mode.

Mode detection

The mode detector detects whether there are any charge or discharge currents, whether the system is powered, whether loads are connected or whether the system is in the standby mode. If power is connected, the power-on LED (POL) is on. In the standby mode, the Coulomb counter will count down in accordance with the self-discharge speed of the batteries, which is temperature controlled. The following subsections describe the various blocks of the block diagram in more detail.

Supply and reference

During the period when V_{CC} rises from 0 V to the internal reset level, all counters are reset. The internal reset is released before V_{CC} reaches 1.7 V. The operating supply voltage ranges from 2 V to the open battery level of 4.3 V (min). The characteristics are guaranteed at V_{CC} = 3 V. In order to protect the SAA1501T against high supply voltages during open battery in a flyback converter, a voltage clamp circuit is made active at 6.35 V (typ). The clamping current must not exceed 80 mA. A band gap reference block is included to generate accurate voltages i.e. for the oscillator. Moreover, together with R_{ref}, accurate currents are generated which are used in the I/F and V/I converters and the oscillator block. In the standby mode only the oscillator and the digital parts are active to limit the discharge current of the batteries to a current level of less than 100 mA. The circuits that are needed temporarily are switched on and off during standby (see "Timing characteristics" t_{som}).

Voltage-to-current charge and discharge

In the V/I converter, the input charge current is translated into acceptable levels for the circuit. The conversion formula is:

$$I_c = \frac{(I_{charge} \times R_{sc})}{R_{CCC}}$$; where $R_{CCC} > R_{sc}$ (see Fig.7)

With R_{CCC}, the charge efficiency can be manipulated depending on the charge level. The restriction of the SAA1501T is a maximum average charge current of 60 μA and a minimum momentary charge current of 0.6 μA. The same formula is applicable for the discharge current. The discharge efficiency can now also be changed by R_{DCC} depending on the discharge current levels, but independent of the charge current. As both sense levels are referenced to ground, the sensing elements could be combined into one. The outputs are used combined as $\frac{1}{6} \times (I_c - I_d)$ in the I/F converter and combined as $(I_c - I_d)$ in the pulse width modulator block and made separately available in the mode detector. The conversion is made lower by a factor of 6 in the I/F converter block, thereby enabling the use of poor leakage capacitors on pin 4. All V/I converter pins are sensitive to capacitive loading ($C_{out} \times R_{conv} < 1$ ms), the conversion resistors should be mounted as close as possible to the output pins.

I/F converter

This block produces up-counts while charging and down-counts while discharging. The I/F converter translates the charge/discharge currents into a frequency. This frequency is determined by

$$f = \frac{(I_{c(d)} \times R_{sense} \times 6)}{(C_{CC} \times \Delta V_{osc} \times R_{CCC(RDCC)})}$$

During the time period 't', the charge current, expressed as a 'Charge Parcel', will be counted in the Coulomb counters (CNT1 and CNT2). During discharge the 'Charge Parcel' is the product of the discharge current and the 't' from the I/F converter generated frequency. The momentary contents of the Coulomb counter is a multiple of the 'Charge Parcels'.

Coulomb counters CNT1 and CNT2

The SAA1501T has been designed for average maximum charge and discharge current levels of 5 C and minimum charge and discharge current levels of 0.05 C. This means that counter CNT1 will be full, or empty, after a minimum time period of 12 minutes at maximum charge and discharge currents at the recommended oscillator frequency. Higher charge and discharge rates than 5 C are possible, but only by changing the oscillator frequency. It should be noted that the self-discharge time and the display functions are influenced by a higher oscillator frequency. The SAA1501T enables top-up charging in order to account for the decrease of charge efficiency at high charge rates. The SAA1501T switches to the slow charge mode at full recognition when CNT1 is at its maximum. As soon as the batteries are completely full (when CNT2 is at its maximum), the SAA1501T switches to the trickle charge mode to overcome the self-discharge of the batteries. The top-up charge volume of CNT2 = 0.2 × CNT1 = 0.2 C (where Q is rated as Ampere hours of the battery). The slow and trickle charge current levels are dependent on the k-factor. Signal EN controls the external charger e.g. TEA1400 (see Fig.8). When an LED bargraph display is used, the LED currents are also considered as a battery discharge current, and therefore influence the duty cycle of the charge current regulation signal EN. The SAA1501T also enables temperature protection. In the event that the battery temperature exceeds a certain maximum temperature level ($T_{battery} > T_{max}$), which can be set by an external NTC resistor, the SAA1501T switches to the slow charge mode. In the standby mode (self-discharge mode), which is recognized by the SAA1501T in the mode detector when both the charge and discharge currents are zero ($I_c = I_d = 0$), the self-discharge of the batteries is registered by counting down in 200 days (based on f_{osc} = 4 kHz) if $T_{battery} < T_{self}$ or in 100 days (based on f_{osc} = 4 kHz) if $T_{battery} > T_{self}$. T_{self} is also set by means of an external NTC resistor.

Band gap generation

From the band gap voltage block, two reference voltages are derived V_{ref} and V_{max}. Voltage V_{ref} at pin R_{ref} sets the reference currents, I_{ref1} (I/F converter); I_{ref2} (mode detector) and I_{ref3} (oscillator). Voltage V_{max} sets the current I_{max} which is used in the pulse width modulation block to accurately control the charge current.

Charge current regulation

While charging, the SAA1501T produces a charge current regulation signal EN in the pulse width modulation block which is used for controlling an external charger. This digital signal EN is derived from the signal produced at pin C_{cy}. The duty cycle is determined by

$$\delta = \frac{k \times I_{max}}{I_c - I_d}$$

in which the value of k depends on the state of the counters CNT1 and CNT2:

CNT1 is not full; k = 1 (fast charging).

CNT1 is full; CNT2 is not full; k = 0.1 (slow charging).

CNT1 and CNT2 are full; k = 0.025 (trickle charging).

Mode detector

This block differentiates between the available modes of operation. The modes are given below:

Charge mode; power charge (POCH).

Discharge mode; battery load (BATLD).

Power load mode (POLD); the batteries are charged while the load is also active.

Self discharge mode; (STANDBY).

To detect power in a regulated system (see Fig.8) the EN signal is used for sensing. The POCH mode is recognized when the converted charge current $I_c > I_{ref2}$ (when in the power mode, change of mode can only be recognised if EN is HIGH). The BATLD mode is recognized when $I_d > I_{ref2}$; the POLD mode is recognized when $I_c > I_{ref2}$ and $I_d > I_{ref2}$; the standby mode is recognized when $I_c < I_{ref2}$ and $I_d < I_{ref2}$. In the standby mode, if the advised frequency (4 kHz) is applied, it takes 0.5 s to determine another mode (in all other modes, a change of mode is sensed continuously). In all other modes an eventual change of mode is done continuously. To save supply current during standby, the V/I converters are switched off. With the specific fixed intervals, the SAA1501T checks whether power or load is connected again. This checking is synchronized by the sensing signal of the V/I converters. The SAA1501T can handle a DC charge current as well as a discontinuous charge current (SMSP charger). The load current can also be DC or interrupted, e.g. produced by a motor. The digital filtering of both signals, to overcome faulty mode detections, restricts the conditions in which power and load are recognized. Because of the very sensitive input detection level of the mode detector for a charge current (power) in combination with the high interference levels of motor driving, the detection level for power ($I_c > I_{ref2}$) is raised by a factor of 25 when the batteries are loaded.

Oscillator

As the oscillator has to operate in all modes, including the standby mode, the current consumption of the oscillator must be very low. The same applies for the band gap generator block, because the band gap delivers accurate reference voltages and currents to the oscillator block. Apart from the low current consumption, the accuracy of the period time is important. The period time of the oscillator is:

$$t_{osc} = 2 \times C_{osc} \times \frac{(V_H - V_L)}{I_{ref3}} = 5.6 \times C_{osc} \times R_{ref}$$

Prescaler/controller

In the prescaler, a new system clock is created (CLK) which is used for all timing blocks. Many frequencies are derived from the basic oscillator at the standard frequency of 4 kHz ($1/T_{osc}$), such as the self-discharge times and the modulation frequency for the buzzer, the drive voltage frequency for the LCD screen and the pulse trains for temperature measurements and power/load sensing measurements in the mode detector.

Temperature

In the temperature control block two temperature measurements are performed. In order to switch off fast charging when the battery temperature exceeds an adjustable maximum temperature (T_{max}), a maximum temperature measurement is performed. A second temperature measurement is performed in the standby mode. This temperature measurement is input to the temperature control block to switch over the self-discharge rate from a count down of 200 days (based on f_{osc} = 4 kHz) if $T_{battery} < T_{self}$, to a count down rate of 100 days (based on f_{osc} = 4 kHz) if $T_{battery} > T_{self}$. In all modes the temperature is measured periodical. The temperature circuit which controls the above mentioned functions is a bridge configuration synthesis, as illustrated in Fig.3.

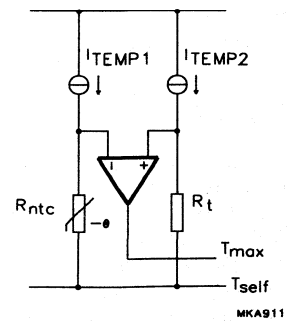


Fig.3 Temperature circuit.

Display decoder driver

The counters are used to output the battery charge amount via a decoder and driver stage to the display outputs L100, L80, L60, L40 and L20 to drive an LCD screen or an LED bargraph. A 64 Hz (based on f_{osc} = 4 kHz) block signal at output BP (back plane) must be connected to the back plane of the LCD bar. If pin BP is connected to ground, the display outputs L20 to L100 will produce signals for an LED bargraph. Output signal POL (power-on LED) indicates when the batteries are in the charge mode. When the counter is not at its maximum state, POL is on and flickers at 2 Hz (based on f_{osc} = 4 kHz) when the counter is at its maximum. The waveforms illustrated in Fig.4 depict operation of the monitor display. The outputs BLI (battery low indication), BUZ (buzzer) and FULL indicate the extreme status (empty or full) of the counters and the batteries. The waveforms of the signals BLI and BUZ if one switches over from BATLD to standby when BLI is active, are given in Fig.4.

The BLI sequence is as follows. If during discharge the charge state falls below 0%, the red BLI LED is turned on. Changing mode from discharge to standby means that the BLI LED and the buzzer (BUZ) are activated as indicated in Fig.4. If after a 0% passing recharge is activated, the red BLI LED is turned on again for as long as the counter remains below 10%. Switch-over in the 0 to 10% range to standby will activate BLI and BUZ again.

The LEDs of the LED bargraph are activated as a result of each operational mode change, starting with a step-up pattern. Step-up means that LEDs are activated successively one after the other, in accordance with the charge status each $\frac{1}{8}$ s (based on f_{osc} = 4 kHz). After the step-up, the LEDs will be on for 8 s (based on f_{osc} = 4 kHz), except for the POCH mode, where the LEDs will be on continuously to inform the user about the charge state of the batteries. The LCD display is, apart from the LED mode, always visible.

Figure 5 shows the legend for Fig.6. Figure 6 shows the operation of the monitor display.

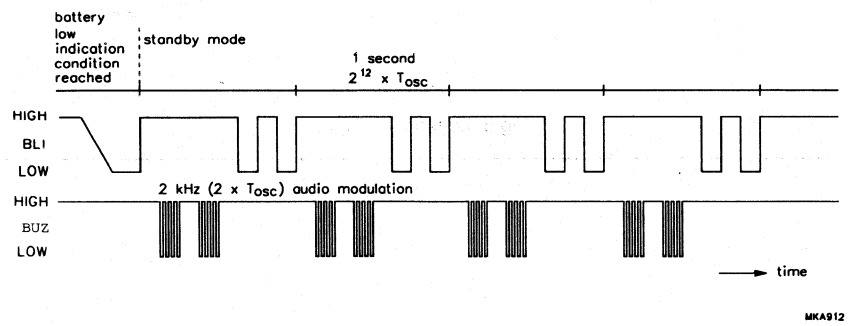


Fig.4 BLI and buzzer timing.

Open battery protection

Open battery protection is active when V_{CC} = 4.5 V (typ.). The SAA1501T will then react as if the system is in the standby mode. This means that the LEDs are turned off in the LED mode, in the LCD mode the flickering is stopped and the enable pin (EN) is switched to floating.

Testing

A user test facility is built-in for checking if the LCD and/or LED displays are mounted correctly. Pin R_{CCC} is used as a test pin. Raising the voltage above 1 V during the set-up time will activate the test. The test mode can only be started in the standby mode. In the test mode all counters are reset and will be active successively in the sequence BLI, L20, L40, L60, L80, L100 and FULL with an interval period determined by T_{osc}. The test mode can be exited via the following methods:

Power-on; the Coulomb counter retains the latest data displayed.

Automatically after the test cycle time; the Coulomb counter is reset.

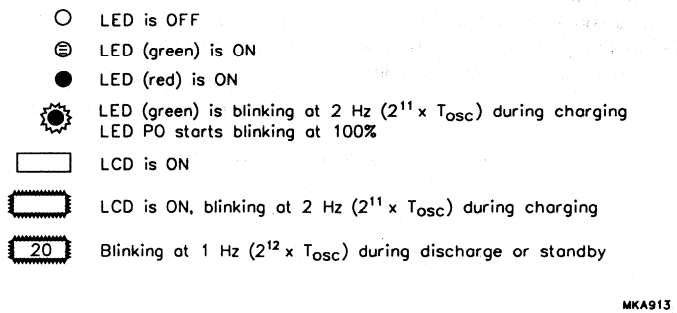
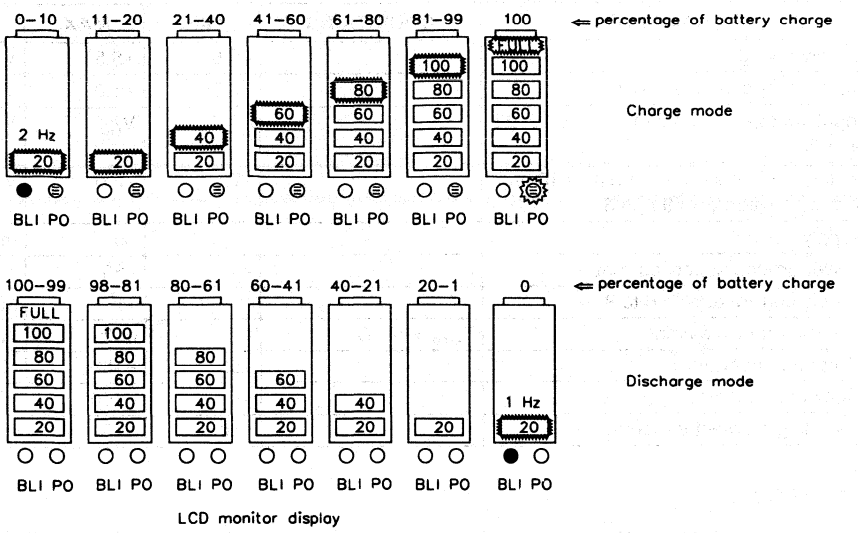


Fig.5 Legend for Fig.6.



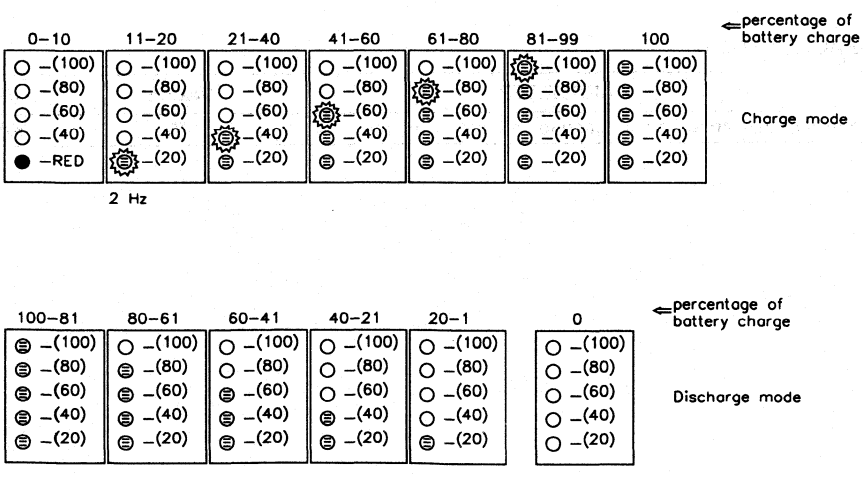


Fig.6 Charge state of counter shown by LCD or LED display.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All voltages with respect to GND (pin 24); input currents are positive; pins 5, 6 and 21 are not allowed to be voltage driven; the voltage ratings are valid provided other ratings are not being violated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.5	+5.5	V
V_{n1}	input voltage at pins 9 to 12		−0.5	+1.0	V
V_{n2}	input voltage at pins 2 to 4, 13 to 20, 22 and 23		−0.5	V_{CC}	V
ΔV	voltage difference between pins 10 and 7 and between pins 9 and 8		−2.0	+2.0	V
I_{CC}	supply current		–	80	mA
I_{GND}	power ground supply current		–	−80	mA
I_n	supply current at pins 5 to 8		–	−1	mA
P_{tot}	total power dissipation	T_{amb} = 70 °C	–	0.75	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		–	+150	°C
T_{amb}	operating ambient temperature		−10	+75	°C

QUALITY SPECIFICATION

In accordance with SNW-FQ-611 part E. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The Handbook can be ordered using the code 9398 510 63011.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

CHARACTERISTICS

V_{CC} = 3 V; T_{amb} = 25 °C; R_{ref} = 51.5 kΩ (0.1%); C_{osc} = 820 pF (0.1%); R_{CCC} = R_{DCC} = 3.65 kΩ (0.1%); R_{max} = 3.48 kΩ (0.1%); $I_{ref} = V_{ref}/R_{ref}$; $I_{max} = V_{max}/R_{max}$; the minimum and maximum values are 4 sigma limits; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage	note 1	2.0	3.0	4.3	V
$V_{CC(ir)}$	supply voltage internal reset		–	1.2	1.7	V
I_{CC}	supply current	$I_c = I_d$ = 60 µA	0.6	–	1.7	mA
I_{CCstb}	supply current in standby mode	$V_{CSI} = V_{DSI}$ = 0 V	–	–	100	mA
V_{ref}	reference voltage	note 2	204	211	217	mV
I_{ref}	reference current	notes 1 and 2	3.5	–	8	µA
V_{max}	maximum voltage	note 2	204	211	217	mV
TC	temperature coefficient of reference voltage	T = 0 to 100 °C	0	25×10^{-6}	100×10^{-6}	°C
V_{clamp}	clamping level voltage	I_{CC} = 50 mA	5.8	6.3	6.8	V
Voltage-to-current charge/discharge						
I_4	voltage-to-current charge/discharge current accuracy	V_9 = 7 mV; V_4 = 1.5 V	–259	–324	–389	nA
		V_{10} = 7 mV; V_4 = 1.5 V	262	328	394	nA
		V_9 = 200 mV; V_4 = 1.5 V	–8.93	–9.13	–9.32	µA
		V_{10} = 200 mV; V_4 = 1.5 V	8.93	9.13	9.32	µA
I_3	voltage-to-current charge/discharge current accuracy	V_9 = 7 mV; R_{max} = 400 kΩ; k = 0.025	–1.55	–1.94	–2.32	µA
		V_{10} = 7 mV; R_{max} = 400 kΩ; k = 0.025	1.57	1.97	2.36	µA
		V_9 = 200 mV; R_{max} = 400 kΩ; k = 0.025	–53.5	–54.7	–56	µA
		V_{10} = 200 mV; R_{max} = 400 kΩ; k = 0.025	53.5	54.7	56	µA
I_4/I_3	relative current accuracy of voltage-to-current in charge counter capacitor	$V_9 = V_{10}$ = 200 mV	–	1.0	2.5	%
$V_{i(s)}$	input sense voltage at pins 9 and 10	$V_{CC(max)}$ = 3.7 V; note 1	0	–	V_{CC} – 1.6	V
		3.7 < V_{CC} < 4.4 V; note 1	–	–	2.1	V
$I_{o(s)}$	DC output sense current (pins 8 and 7)		0.6	–	60	µA
V_{os}	offset voltage		–	–	1.8	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I/F converter						
a	multiplication factor for I_{ref1}	$I_{ref1} = a \times I_{ref}$ (where a is constant); V_4 = 1.26 V; idle mode	2.35	2.5	2.65	
V_{clamp}	clamping voltage (pin 4)	$I_c = 0$; I_d = 60 μA; I_4 = 10 μA	0.7	0.9	1.1	V
$V_{CCC(H)}$	HIGH level reference voltage (pin 4)		1.58	1.66	1.74	V
$V_{CCC(L)}$	LOW level reference voltage (pin 4)		1.26	1.33	1.4	V
Pulse width modulator						
ACC	accuracy for I_{max} at C_{cy}	15 < I_{max} < 60 μA	–	–	±3	%
I_{max}	maximum DC current	$I_{max} = V_{max}/R_{max}$; note 1	0.6	–	60	mA
I_d/I_{max}	k factor	k = 1; V_d = 1.5 V; idle mode	0.95	0.98	1.01	
		k = 0.1; V_d = 1.5 V; idle mode	0.094	0.099	0.104	
		k = 0.025; V_d = 1.5 V; idle mode	0.023	0.025	0.027	
V_{CCY}	start up-clamping voltage (pin 3)	I_d = 10 μA; $I_c = 0$	0.7	0.9	1.1	V
V_{CCY}	clamping voltage (pin 3)	open-circuit at pin 3; pin 5 = V_{CC}; $\pm(I_c - I_d)$ = 60 μA	–	–	V_{CC} – 0.6	V
$V_{CCY(H)}$	HIGH level switching voltage		1.60	1.77	1.86	V
$V_{CCY(L)}$	LOW level switching voltage		1.28	1.32	1.37	V
I_Z	3-state enable current	V_2 = 1.5 V	–	–	1	μA
Mode detector						
I_{ref2}	mode detection level at pins 7 and 8	$I_{ref2} \geq e \times I_{ref}$ (where e is constant)	–	$0.15I_{ref}$	–	
I_{ref4}	mode detection level at pin 7	$I_{ref4} \geq I_{ref2}$; in modes POLD and BATLD	–	$25I_{ref2}$	–	
Oscillator (pin 13)						
Q_c	charge amount	$I_{ref1(sink)} \times T_{clk}$	142	150	158	nC
Q_d	discharge amount	$I_{ref1(source)} \times T_{clk}$	142	150	158	nC
ΔQ	difference between charge and discharge charge amount		0.95	1.0	1.05	
b	multiplication factor for I_{ref3}	$I_{ref3} = b \times I_{ref}$ (where b is constant)	–	0.75	–	
ΔV_{osc}	voltage swing HIGH-to-LOW transition		–	440	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{osc}	oscillator frequency		3.9	4.3	4.7	kHz
Temperature control (pins 11 and 12)						
V_i	input voltage		0	–	900	mV
I_{TEMP2}/I_{TEMP1}	detection at T_{max}	$V_{11} = V_{12} = 300$ mV	9.7	10.0	10.3	
I_{TEMP2}/I_{TEMP1}	detection at T_{self}	$V_{11} = V_{12} = 300$ mV	15	16	17	
c	multiplication factor for I_{TEMP1}	$I_{TEMP1} = c \times I_{ref}$ (where c is constant); $V_{TEMP1} = V_{TEMP2} = 300$ mV	0.45	0.54	0.63	
d	multiplication factor for I_{TEMP2}	$I_{TEMP2} = d \times I_{ref}$ (where d is constant); $V_{TEMP1} = V_{TEMP2} = 300$ mV	4.5	5.4	6.3	
Open battery protection						
$V_{CC(ob)}$	open-battery level voltage		4.3	4.5	4.65	V
Testing						
V_{test}	test level voltage		1.0	–	2.0	V
Display decoder driver						
I_{OL1}	LOW level output current (pin 20 LED), (LED 20 is on)	$V_{OL} = 0.6$ V; L40 to L100 off; $V_{CC} = 2.4$ V	7	10	12	mA
I_{OBP}	output LED sense current (pin 21 LED), (LED 20 is on)	$V_{OBP} = 0.1$ V; L40 to L100 off; $V_{CC} = 2.4$ V	63	82	100	µA
$I_{LED(CF)}$	LED current compensation factor	I_{OL1}/I_{OBP}; $V_{CC} = 2.4$ V	110	121	132	
I_{OL2}	LOW level output current (pins 20 to 16 LED), (all LEDs are on)	all LEDs on; $V_{OL} = 0.7$ V; $V_{CC} = 2.8$ V	7.5	11	14	mA
$I_{OBP(tot)}$	total output sense current (pins 21)	$V_{OBP} = 0.1$ V; $V_{CC} = 2.8$ V; L20 to L100 on	350	452	560	µA
$I_{LED(CF)}$	LED current compensation factor	$5I_{OL2}/I_{OBP(tot)}$	115	125	135	
I_{OL}	output current (pins 20 to 16 LCD)	$V_{OL} = 0.5$ V; $V_{CC} = 2.8$ V	350	480	640	µA
$I_{OL(14,15)}$	LOW level output current (pins 14 and 15)	$V_{OL} = 0.4$ V; $V_{CC} = 2.4$ V	0.9	1.2	1.7	mA
$I_{OL(22,23)}$	LOW level output current (pins 22 and 23 LED)	$V_{OL} = 0.4$ V; $V_{CC} = 2.1$ V	7	10	12	mA
$I_{OL(21)}$	LOW level output current (pin 21 LCD)	$V_{OL} = 0.4$ V; $V_{CC} = 2.8$ V	572	849	1214	µA
I_{OH}	HIGH level output current (pins 20 to 16 LED)	$V_{OH} = 2.4$ V; $V_{CC} = 2.8$ V	261	378	526	µA
$I_{OH(21)}$	HIGH level output current (pin 21 LED)	$V_{OH} = 2.4$ V; $V_{CC} = 2.8$ V	239	378	565	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{OH(14)}$	HIGH level output current (pin 14)	V_{OH} = 2 V; V_{CC} = 2.4 V	0.7	1.6	2.5	µA
$I_{OH(15)}$	HIGH level output current (pin 15)	V_{OH} = 2 V; V_{CC} = 2.4 V	0.99	1.67	2.69	mA
$I_{OH(22,23)}$	HIGH level output current (pins 22 and 23)	V_{OH} = 2.4 V; V_{CC} = 2.4 V	260	450	708	µA
I_{LO}	output leakage current (pin 21)	V_{OH} = 0 to V_{CC}	–	–	±1	µA

Notes

1. Not measured by the industrial measuring program, but guaranteed by design.
2. Internally detected from band gap generator.

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE
T_{osc}	oscillator cycle time	note 1	$T_{osc} = 2C_{osc} \times V_{osc}/I_{ref3}$
T_{clk}	clock cycle time		$64t_{osc}$
t_{som}	sense operation mode time	note 2	$1.5 \times 2^{7}T_{osc}$
$t_{som(p)}$	sense operation mode period time	note 2	$2^{12}T_{osc}$
t_{rec}	recognition time	power; note 3	$>32t_{osc}$
		load; note 4	$>20t_{osc}$
t_{self}	self discharge counter time	$T_{battery} > T_{self}$ (100 days at f_{osc} = 4 kHz)	$2^{35}T_{osc}$
		$T_{battery} > T_{self}$ (200 days at f_{osc} = 4 kHz)	$2^{36}T_{osc}$
$t_{battery(s)}$	battery temperature measurement sense time		$2^{7}T_{osc}$
$t_{battery(p)}$	battery temperature measurement period time		$2^{16}T_{osc}$
t_{su}	display test set-up time		$2^{11}T_{osc} < t < 1.5 \times 2^{18}T_{osc}$
t_{id}	interval display test time		$2^{10}T_{osc}$
t_{pd}	period display test time		$1.5 \times 2^{18}T_{osc}$
$t_{su:LED}$	LED set-up time		$2^{9}T_{osc}$
$t_{LED(ON)}$	LEDs-on time	after change of mode (except POCH mode)	$2^{15}T_{osc}$
f_{BP}	drive voltage frequency for back plane		$2^{-4}T_{osc}$
f_{BUZ}	modulation frequency for auto buzzer		$\frac{1}{2}T_{osc}$

Notes

1. $t_{osc} = 2C_{osc} \times \frac{V_{osc}}{I_{ref3}}$; where V_{osc} = 440 mV and I_{ref3} = 0.75.
2. Applies to all converters and enable signal.
3. For charge current AC or DC: $f > \frac{1}{2}f_{osc}$.
4. For discharge current AC: $f > \frac{1}{4}f_{osc}$.

APPLICATION INFORMATION

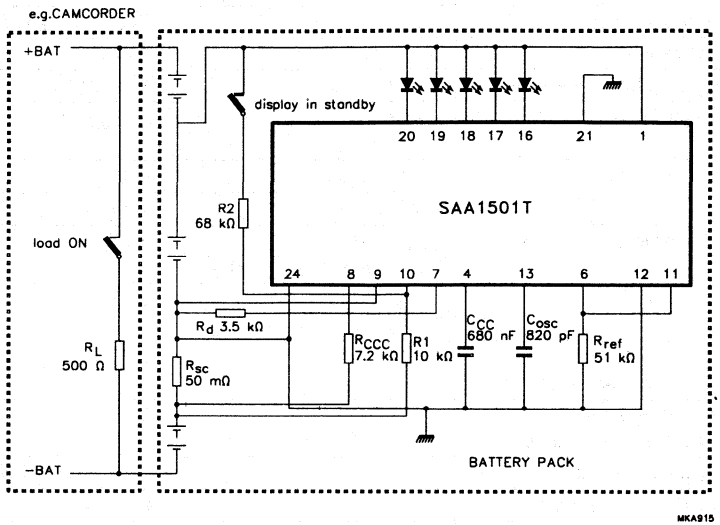


Fig.7 Battery pack application diagram; with camcorder.

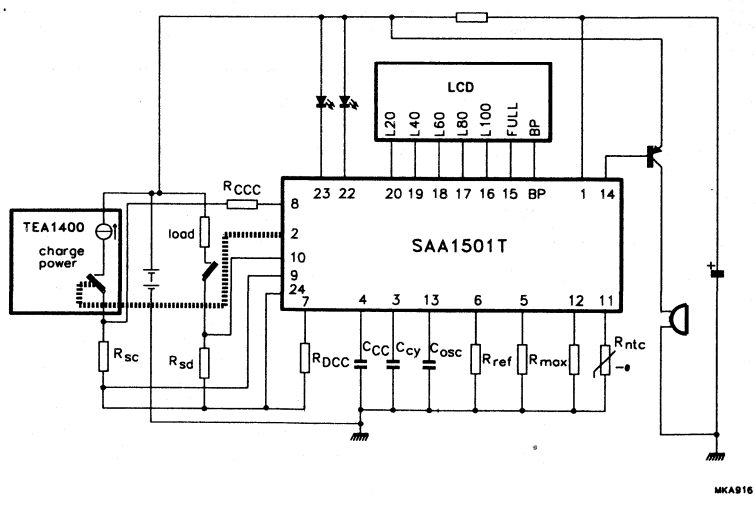


Fig.8 State-of-charge indicator and charge current regulation.

Fast charge IC for NiCd, NiMH, SLA and Lilon

TEA1102; TEA1102T

FEATURES

- Safe and fast charging of Nickel Cadmium (NiCd), Nickel Metal Hydride (NiMH), Lithium Ion (Lilon), and Sealed Lead Acid (SLA) batteries
- Three charge states for NiCd or NiMH; fast, top-off and trickle or voltage regulation (optional)
- Two charge states for Lilon or SLA; current and voltage limited
- Adjustable fast charge current [0.5CA to 5CA nominal (CA = Capacity Amperes)]
- DC top-off and pulsating trickle charge current (NiCd and NiMH)
- Temperature dependent $\Delta T/\Delta t$ battery full detection
- Automatic switch-over to accurate peak voltage detection ($-1/4$%) if no NTC is applied
- Possibility to use both $\Delta T/\Delta t$ and peak voltage detection as main fast charge termination
- Support of inhibit during all charging states
- Manual refresh with regulated adjustable discharge current (NiCd and NiMH)
- Voltage regulation in the event of no battery
- Support of battery voltage based charge indication and buzzer signalling at battery insertion, end of refresh and at full detection
- Single, dual and separate LED outputs for indication of charge status state
- Minimum and maximum temperature protection
- Time-out protection
- Short-circuit battery voltage protection
- Can be applied with few low-cost external components.

GENERAL DESCRIPTION

The TEA1102; TEA1102T are fast charge ICs which are able fast charge NiCd and NiMH, SLA and Lilon batteries.

The main fast charge termination for NiCd and NiMH batteries are $\Delta T/\Delta t$ and peak voltage detection, both of which are well proven techniques. The TEA1102; TEA1102T automatically switches over from $\Delta T/\Delta t$ to peak voltage detection if the thermistor fails or is not present. The $\Delta T/\Delta t$ detection sensitivity is temperature dependent, thus avoiding false charge termination. Three charge states can be distinguished; fast, top-off and trickle.

Charging Lilon and SLA batteries is completely different. When the batteries reach their maximum voltage (adjustable), the TEA1102; TEA1102T switches over from current regulation to voltage regulation. After a defined time period, which is dependent on battery capacity and charge current, charge is terminated. Due to small self discharge rates of Lilon and SLA batteries, trickle charge can be omitted.

Several LEDs, as well as a buzzer, can be connected to the TEA1102; TEA1102T for indicating battery insertion, charge states, battery full condition and protection mode.

The TEA1102; TEA1102T are contained in a 20-pin package and are manufactured in a BiCMOS process, essentially for integrating the complex mix of requirements in a single chip solution. Only a few external low cost components are required in order to build a state of the art charger.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1102	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT 146-1
TEA1102T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		5.45	–	11.5	V
I_P	supply current	outputs off	–	4	–	mA
$\Delta V_{NTC}/V_{NTC}$	temperature rate dependent ($\Delta T/\Delta t$) detection level	V_{NTC} = 2 V T_j = 0 to 50 °C	–	–0.25	–	%
$\Delta V_{bat}/V_{bat}$	voltage peak detection level with respect to top value	V_{bat} = 2 V T_j = 0 to 50 °C	–	–0.25	–	%
I_{Vbat}	input current battery monitor	V_{bat} = 0.3 to 1.9 V	–	1	–	nA
$V_{bat(l)}$	voltage at pin 19 for detecting low battery voltage		–	0.30	–	V
I_{IB}	battery charge current	fast charge	10	–	100	µA
		top-off mode	–	3	–	µA
$I_{IB(max)}$	maximum battery charge current	voltage regulation full NiCd and NiMH battery	–	10	–	µA
$I_{IB(Lmax)}$	maximum load current	no battery	–	40	–	µA
f_{osc}	oscillator frequency		10	–	200	kHz
V_{reg}	regulating voltage	LiIon	–	1.37	–	V
		SLA	–	1.63	–	V
		NiCd and NiMH (pin V_{stb} open-circuit)	–	1.325 or V_{stb}	–	V
		open battery	–	1.9	–	V

BLOCK DIAGRAM

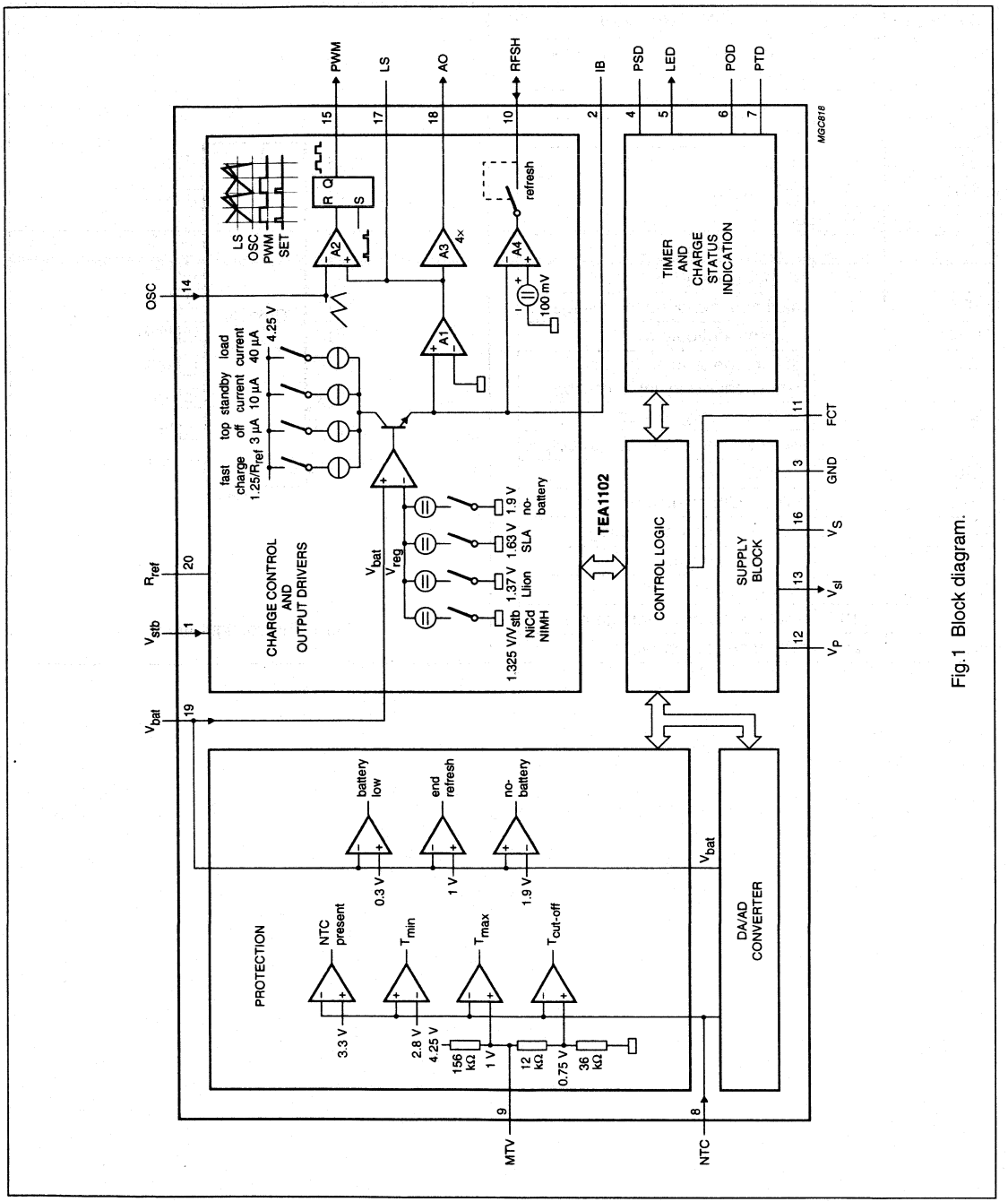


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{stb}	1	standby regulation voltage input (NiCd and NiMH)
IB	2	charge current setting
GND	3	ground
PSD	4	program pin sample divider
LED	5	LED output
POD	6	program pin oscillator divider
PTD	7	program pin time-out divider
NTC	8	temperature sensing input
MTV	9	maximum temperature voltage
RFSH	10	refresh input/output
FCT	11	fast charge termination and battery chemistry identification
V_P	12	positive supply voltage
V_{sl}	13	switched reference voltage output
OSC	14	oscillator input
PWM	15	pulse width modulator output
V_S	16	stabilized reference voltage
LS	17	loop stability pin
AO	18	analog output
V_{bat}	19	single-cell battery voltage input
R_{ref}	20	reference resistor pin

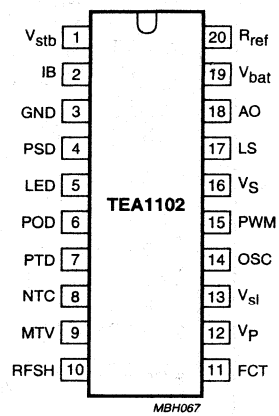


Fig.2 Pin configuration.

INTRODUCTION

All battery types are initially fast charged with an adjustable high current. Fast charge termination depends upon the battery type. With NiCd and NiMH batteries the main fast charge termination will be the $\Delta T/\Delta t$ (temperature detection) and/or peak voltage detection and with SLA and LiIon batteries when the battery voltage reaches 2.45 or 4.1 V respectively.

The fast charge period is followed by a top-off period for NiCd and NiMH batteries and by a fill-up period for SLA and LiIon batteries. During the top-off period the NiCd and NiMH batteries are charged to maximum capacity by reduced adjustable charge current.

During the fill-up period the SLA and LiIon batteries are charged to maximum capacity by a constant voltage and a gradually decreasing current. The fill-up and top-off period ends after time-out or one hour respectively.

After the fill-up or top-off period, the TEA1102 switches over to the standby mode. For NiCd and NiMH batteries either the voltage regulation or trickle charge mode can be selected. The voltage regulation mode is selected when the battery includes a fixed load. Trickle charge prevents a discharge of the battery over a long period of time. For SLA and LiIon batteries the charge current is disabled during standby. The fast charge mode is entered again when the battery voltage reaches 1.5 V (SLA) or 3 V (LiIon).

Charging principles

CHARGING NiCd/NiMH BATTERIES

Fast charging of the battery begins when the power supply voltage is applied and at battery insertion.

During fast charge of NiCd and NiMH batteries, the battery temperature and voltage are monitored. Outside the initialized temperature and voltage window, the system switches over to the top-off charge current.

The TEA1102 supports detection of fully charged NiCd and NiMH batteries by either of the following criteria:

- $\Delta T/\Delta t$
- Voltage peak detection.

If the system is programmed with $\Delta T/\Delta t$ and V_{peak} or, $\Delta T/\Delta t$ or V_{peak} as the main fast charge termination, it automatically switches to voltage peak detection if the battery pack is not provided with a temperature sensing input (NTC). In this way both packages, with and without temperature sensor, can be used randomly independent of the applied full detection method. Besides $\Delta T/\Delta t$ and/or voltage peak detection, fast charging is also protected by temperature cut-off and time-out.

To avoid false fast charge termination by peak voltage detection or $\Delta T/\Delta t$, full detection is disabled during a short hold-off period at the start of a fast charge session. After fast charge termination, the battery is extra charged by a top-off period. During this period of approximately one hour, the charge current is lowered thus allowing the battery to be charged to nearly 100% before the system switches over to standby.

After the battery has been charged to nearly 100% by the top-off period, discharge of the battery (caused by a load or by the self-discharge) can be avoided by voltage regulation or by trickle charge.

If batteries are charged in combination with a load, the TEA1102 can be programmed to apply voltage regulation during the standby mode. In this way, discharge of the battery caused by self-discharge or by an eventual load is avoided. The regulating voltage is adjustable to the voltage characteristic of the battery. For battery safety the charge current is limited and the temperature is monitored during voltage regulation. If a trickle charge is applied, the self-discharge of the battery will be compensated by a pulsating charge current.

To avoid the so called 'memory effect' in NiCd batteries, a refresh can be manually activated.The discharge current is regulated by the IC in combination with an external power transistor. After discharging the battery to 1 V per cell, the system automatically switches over to fast charge.

CHARGING LiION/SLA BATTERIES

Charging these types of batteries differs considerably from charging NiCd and NiMH batteries. The batteries will be charged with a charge current of 0.15 CA if their cell voltage is below the minimum voltage of 0.9 V for LiIon or 0.45 V for SLA. With batteries in good condition the battery voltage will rise above 0.9 V in a short period of time. When the batteries are short-circuited the voltage will not rise above 0.9 V within one hour and the system will change over to cut-off, which means that the output drivers AO and PWM are fixed to zero and that battery charge can only be started again after a power-on reset. If the battery voltage of a good condition battery is above the minimum level of 0.9 V the battery will be charged with the programmed fast charge current.

If LiIon or SLA batteries are used, 'full' is detected when the battery voltage reaches 4.1 and 2.45 V respectively. At this point the TEA1102 switches from current regulation to voltage regulation (fill-up mode).

After the 'fill-up' period the charge current is not regulated, which means that the output drivers AO and PWM are fixed to zero. When the battery voltage becomes less than 3 V for Lilon and 1.5 V for SLA, the IC enters the fast charge mode again.

FUNCTIONAL DESCRIPTION

Control logic

The main function of the control logic is to support the communication between several blocks. It also controls the charge method, initialization and battery full detection. The block diagram of the TEA1102 is illustrated in Fig.1.

Conditioning charge method and initializations

At system switch-on, or at battery insertion, the control logic sets the initialization mode in the timer block. After the initialization time the timer program pins can be used to indicate the charging state using several LEDs.
The charge method is defined at the same time by the following methods:

- If the FCT pin is 0 or 1.25 V, indicating that SLA or Lilon batteries have to be charged, the battery will be charged by limit current and limit voltage regulation. Without identification (FCT pin floating), the system will charge the battery according to the charge characteristic of NiCd and NiMH batteries.
- The standby charge method (NiCd and NiMH), trickle charge or voltage regulation, is defined by the input pin V_{stb}. By biasing this voltage with a set voltage, the output voltage will be regulated to the V_{stb} set voltage. If this pin is connected to V_S, or no NTC is connected the system applies trickle charge.

If pin RFSH is connected to ground by depressing the switch, the TEA1102 discharges the battery via an external transistor connected to pin RFSH. The discharge current is regulated with respect to the external (charge) sense resistor (R_{sense}). End-of-discharge is reached when the battery is discharged to 1 V per cell. Refreshing the battery can only be activated during charging of NiCd and NiMH batteries. When charging Lilon and SLA batteries, discharge before charge is disabled.

The inhibit mode has the main priority. This mode is activated when the V_{stb} input pin is connected to ground. Inhibit can be activated at any charge/discharge state, whereby the output control signals will be zero, all LEDs will be disabled and the charger timings will be set on hold. Table 1 gives an operational summary.

Table 1 Functionality of program pins

FUNCTION	FCT	NTC	RFSH	V_{stb}
Inhibit	X(5)	X(5)	X(5)	low
Lilon and SLA detection	low	X(5)	X(5)	X(5)
Refresh (NiCd and NiMH)	not low(3)	X(5)	low	not low
$\Delta T/\Delta t$ detection	floating	note 1	not low	not low
$\Delta T/\Delta t$ and voltage peak detection	high	note 1	not low	not low
Voltage peak detection	not low	note 2	not low	not low
Trickle charge at standby	not low	X(5)	not low	high
	not low	note 2	not low	not low
Voltage regulation at standby	not low	note 1	not low	floating(4)

Notes

1. The NTC voltage has been to be less than 3.3 V, which indicates the presence of an NTC.
2. The NTC voltage is outside the window for NTC detection.
3. Not low means floating or high.
4. V_{stb} has to be floating or set to a battery regulating voltage in accordance with the specification.
5. Where X = don't care.

Supply block

The supply block delivers the following outputs:

- A power-on reset pulse to reset all digital circuitry at battery insertion or supply switch-on. After a general reset the system will start fast charging the battery.
- A 4.25 V stabilized voltage source (V_S) is externally available. This source can be used to set the thermistor biasing, to initialize the programs, to supply the external circuitry for battery voltage based charge indication and to supply other external circuitry.
- A 4.25 V bias voltage (V_{sl}) is available for use for more indication LEDs. This output pin will be zero during the initialization period at start-up, thus avoiding any interference of the extra LEDs when initializing.

Charge control

The charge current is sensed via a low-ohmic resistor (R_{sense}), see Fig.8. A positive voltage is created across resistor R_b by means of a current source I_{ref} which is set by R_{ref} in the event of fast charge and by an internal bias current source in the event of top-off and trickle charge (I_{IB}), see Fig.1. The positive node of R_b will be regulated to zero via error amplifier A1, which means that the voltage across R_b and R_{sense} will be the same. The fast charge current is defined by the following equation:

$$I_{fast} \times R_{sense} = R_b \times I_{ref} \quad (1)$$

The output of amplifier A1 is available at the loop stability pin LS, consequently the time constant of the current loop can be set. When V_{peak} (NiCD and NiMH) is applied, the current sensing for the battery voltage will be reduced, implying that the charge current will be regulated to zero during:

$$t_{sense} = 2^{10} \times POD \times t_{osc} \quad (2)$$

Actually battery voltage sensing takes place in the last oscillator cycle of this period.

To avoid modulation on the output voltage, the top-off charge current is DC regulated, defined by the following equation:

$$I_{top-off} \times R_{sense} = R_b \times 3 \times 10^{-6} \quad (3)$$

where:

$$t_{top-off} = 2^{27} \times TOD \times t_{osc} \quad (4)$$

The top-off charge current will be approximately 0.15 CA, which maximizes the charge in the battery under safe and slow charging conditions. The top-off charge period will be approximately one hour, so the battery will be extra charged with approximately 0.15 Q. In this way the battery is fully charged before the system switches over to standby.

When pin 1 (V_{stb}) is connected to V_S, or no NTC is connected the system compensates the (self) discharge of the battery by trickle charge. The trickle charge current will be pulsating, defined by the following equation:

$$I_{trickle} \times R_{sense} = R_b \times \frac{15}{16} \times 10^{-6} \quad (5)$$

During the non current periods at trickle charge the charge current is regulated to zero, so that the current for a load connected in series across the battery with the sense resistor will be supplied by the power supply and not by the battery.

If at pin 1 (V_{stb}) a reference voltage is set in accordance with the specification, and no NTC is connected the charge mode will switch over from current to voltage regulation after top-off. The reference regulating voltage can be adjusted to the battery characteristic by external resistors connected to pin V_{stb}.

This reference voltage has to be selected in such a way that it equals the rest voltage of the battery. By using voltage regulation, the battery will not be discharged at a load occurrence. If the V_{stb} input pin is floating, the TEA1102 will apply voltage regulation at 1.325 V during the standby mode (NiCd and NiMH). The current during voltage regulation is limited to 0.5 CA. If the battery charge current is maximized to 0.5 CA for more than 2 hours charging will be stopped. Moreover, if the temperature exceeds T_{max}, charging will be stopped completely. As voltage regulation is referred to one cell, the voltage on the V_{bat} pin must be the battery voltage divided by the number of cells (NiCd and NiMH).

For Lilon or SLA batteries, the battery is extra charged after full detection by constant voltage regulation during a certain fill-up period. Lilon and SLA batteries have to identify themselves by an extra pin on the battery pack to ground, which is connected via a resistor to pin 11 (FCT). As the battery voltage sense (V_{bat}) has to be normalized to a one cell voltage of NiCd and NiMH packages, the V_{bat} input pin will be regulated to 1.367 and 1.633 V during fill-up for Lilon and SLA respectively. In this way this system can accept a mixture of one Lilon, two SLA and three NiCd or NiMH packages.

After fill-up, charging of Lilon or SLA batteries is disabled. The battery charge is then fixed to zero, ensuring maximum life-cycle of the battery.

Because of a fixed zero charge current, the battery will be discharged if a load is applied.

To ensure an eventual load during all charging states, the fast charge mode will be entered again if the battery voltage drops below 15 V for SLA or 3 V for Lilon.

When charging, the standby mode (Lilon and SLA) can only be entered after a certain period of time depending on time-out. The same applies for charging NiCd or NiMH batteries. To support full test of the TEA1102 at application, the standby mode is also entered when $V_{bat} < V_{bat(l)}$ at fill-up or top-off respectively.

Timer

The timing of the circuit is controlled by the oscillator frequency.

The timer block defines the maximum charging time by 'time-out'. At a fixed oscillator frequency, the time-out time can be adapted by the Programmable Time-out Divider (PTD) using the following equation.

$$t_{time-out} = 2^{26} \times POD \times PTD \times t_{osc} \quad (6)$$

The time-out timer is put on hold by low voltage, temperature protection and during the inhibit mode. The Programmable Oscillator Divider (POD) enables the oscillator frequency to be increased without affecting the sampling time and time-out. Raising the oscillator frequency will reduce the size of the inductive components that are used.

At fast charging, after battery insertion, after refresh or supply interruption, the full detector will be disabled for a period of time to allow a proper start with flat or inverse polarized batteries. This hold-off period is disabled at fast charging by raising pin V_{stb} to above ±5 V (once). So for test options it is possible to slip the hold-off period. The hold-off time is defined by the following equation:

$$t_{hold-off} = 2^{-5} \times t_{time-out} \quad (7)$$

Table 2 gives an overview of the settings of timing and discharge/charge currents.

Table 2 Timing and current formulae

SYMBOL	DESCRIPTION	FORMULAE
t_{osc}	timing	see Fig.3
$T_{sampling}$ ($\Delta T/\Delta t$)	NTC voltage sampling frequency	$2^{17} \times POD \times PSD \times t_{osc}$
$T_{sampling}$ (V_{peak})	battery voltage sampling frequency	$2^{16} \times POD \times t_{osc}$
$t_{top-off}$		$2^{27} \times POD \times t_{osc}$
$t_{time-out}$		$2^{26} \times POD \times PTD \times t_{osc}$
$t_{hold-off}$		$2^{-5} \times t_{time-out}$
t_{LED}	inhibit or protection	$2^{14} \times POD \times t_{osc}$
t_{sense}		$2^{10} \times POD \times t_{osc}$
t_{switch}		$2^{21} \times POD \times PTD \times t_{osc}$
I_{fast}	charge/discharge currents	$\frac{R_b}{R_{sense}} \times \frac{V_{ref}}{R_{ref}}$
$I_{top-off}$		$\frac{R_b}{R_{sense}} \times 3 \times 10^{-6}$
$I_{trickle}$		$\frac{R_b}{R_{sense}} \times \frac{15}{16} \times 10^{-6}$
$I_{load-max}$		$\frac{R_b}{R_{sense}} \times 40 \times 10^{-6}$
I_{RFSH}		$\frac{100\ mV}{R_{sense}}$

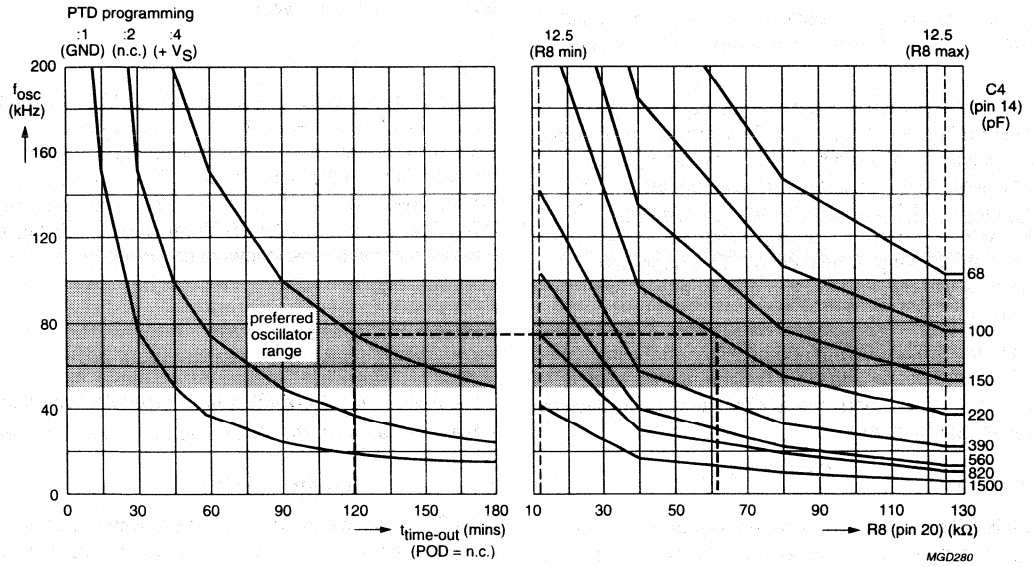


Fig.3 $t_{time-out}$ as a function of R8 and PTD with C4 as parameter.

LED indication

With few external components, indication LEDs can be connected to the program pins and the LED pin of the TEA1102. These program pins change their function from an input to an output pin after a short initialization time at system switch-on or battery insertion. Output pin V_{sl} enables the external LEDs to be driven and avoids interaction with the programming of the dividers during the initialization period.

The applied LEDs indicate:

- Protection
- Refresh
- Fast charge
- 100%
- No-battery.

The LED output pin can also indicate the charging state by one single LED. The indication LED can be connected directly to the LED output. This single LED indicates:

- Fast charge (LED on)
- 100% or refresh (LED off)
- Protection or inhibit (LED floating).

The refresh can be indicated by an extra LED connected to pin 4 (PSD). A buzzer can also be driven from the TEA1102 to indicate battery insertion end of refresh or full battery.

AD/DA converter

When battery full is determined by peak voltage detection, the V_{bat} voltage is sampled at a rate given by the following equation:

$$t_{sampling}(V_{peak}) = 2^{16} \times POD \times t_{osc} \quad (8)$$

The analog value of a V_{bat} sample is then digitized and stored in a register. On the following sample, the digitized value is converted back to the analog value of V_{bat} and compared with the 'new' V_{bat} sample.

At an increase of the battery voltage the 14-bit analog-to-digital convertor (ADC) is refreshed with this new value. Therefore, the digitized value always represents the maximum battery voltage. A decreased V_{bat} voltage is not stored, but is compared to the stored value.

Full is detected when the voltage decrease of V_{bat} is $\frac{1}{4}$% of the stored peak battery value. To avoid interference due to the resistance of the battery contacts during battery voltage sensing, the charge current is regulated to zero during $t = 2^{10} \times POD \times t_{osc}$, via the regulation pins AO and PWM. At the last period, the V_{bat} voltage is sensed and stored in a sample-and-hold circuit. This approach ensures very accurate detection of the battery full condition (minus $\frac{1}{4}$%).

When battery full is determined by $\Delta T/\Delta t$, the voltage on the NTC pin is used as the input voltage to the AD/DA convertor. The sampling time at $\Delta T/\Delta t$ sensing is given by the following equation:

$$t_{sampling}\left(\frac{\Delta T}{\Delta t}\right) = 2^{17} \times POD \times PSD \times t_{osc} \quad (9)$$

After this initialized sample time the new temperature voltage is compared to the preceding AD/DA voltage and the AD/DA is refreshed with this new value. A certain increase of the temperature is detected as full battery, depending on the initialization settings. The decision of full detection by $\Delta T/\Delta t$ or V_{peak} is digitally filtered thus avoiding false battery full detection.

Output drivers

The charge current regulation signal is available at two output pins, AO and PWM.

ANALOG OUTPUT

The analog control voltage output at pin 18 (AO) can be used to drive an opto-coupler in mains separated applications when an external resistor is connected between AO and the opto-coupler. The maximum current through the opto-coupler diode is 2 mA. The voltage gain of amplifier A2 is typical 11 dB (times 3.5). The DC voltage transfer is given by the following equation:

$$V_{ao} = 3.5 \times (V_{LS} - 1.35).$$

The AO output can be used for:

- Linear (DC) applications
- Not mains isolated SMPS with a separate controller
- Mains isolated SMPS, controlled by an opto-coupler.

PULSE WIDTH MODULATOR (PWM)

The LS voltage is compared internally with the oscillator voltage to deliver a pulse width modulated output at PWM (pin 15) to drive an output switching device in a SMPS converter application via a driver stage. The PWM output is latched to prevent multi-pulsing. The maximum duty factor is internally fixed to 79% (typ.). The PWM output can be used for synchronization and duty factor control of a primary SMPS via a pulse transformer.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltages						
V_P	positive supply voltage		−0.5	–	11.5	V
V_{oLED}	output voltage at pin 5		−0.5	–	15	V
V_n	voltage at pins PWM, LS and NTC		−0.5	–	$+V_S$	V
V_{IB}	voltage at pin 2		−0.5	–	1.0	V
Currents						
I_{VS}	current at pin 16		−3	–	+0.01	mA
I_{Vsl}	current at pin 13		−1	–	+0.3	mA
I_{oLED}	output current at pin 5		–	–	12	mA
I_{AO}	output current at pin 18		−10	–	+0.05	mA
I_{oPWM}	output current at pin 15		−15	–	+14	mA
I_{Rref}	current at pin 20		−1	–	+0.01	mA
I_P	positive supply current	$T_j < 100$ °C	–	–	30	mA
$I_{P(stb)}$	supply standby current	$V_P = 4$ V	–	35	45	µA
Dissipation						
P_{tot}	total power dissipation	$T_{amb} = +85$ °C				
	SOT146-1		–	–	1.2	W
	SOT163-1		–	–	0.6	W
Temperatures						
T_{amb}	operating ambient temperature		−20	–	+85	°C
T_j	junction temperature		–	–	+150	°C
T_{stg}	storage temperature		−55	–	+150	°C

Note

1. All voltages are measured with respect to ground; positive currents flow into the IC; all pins not mentioned in the voltage list are not allowed to be voltage driven. The voltage ratings are valid provided that other ratings are not violated; current ratings are valid provided that the power rating is not violated.

QUALITY SPECIFICATION

General quality specification for integrated circuits: SNW-FQ-611E.

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °C; R_{ref} = 62 kΩ; unless otherwise specified.

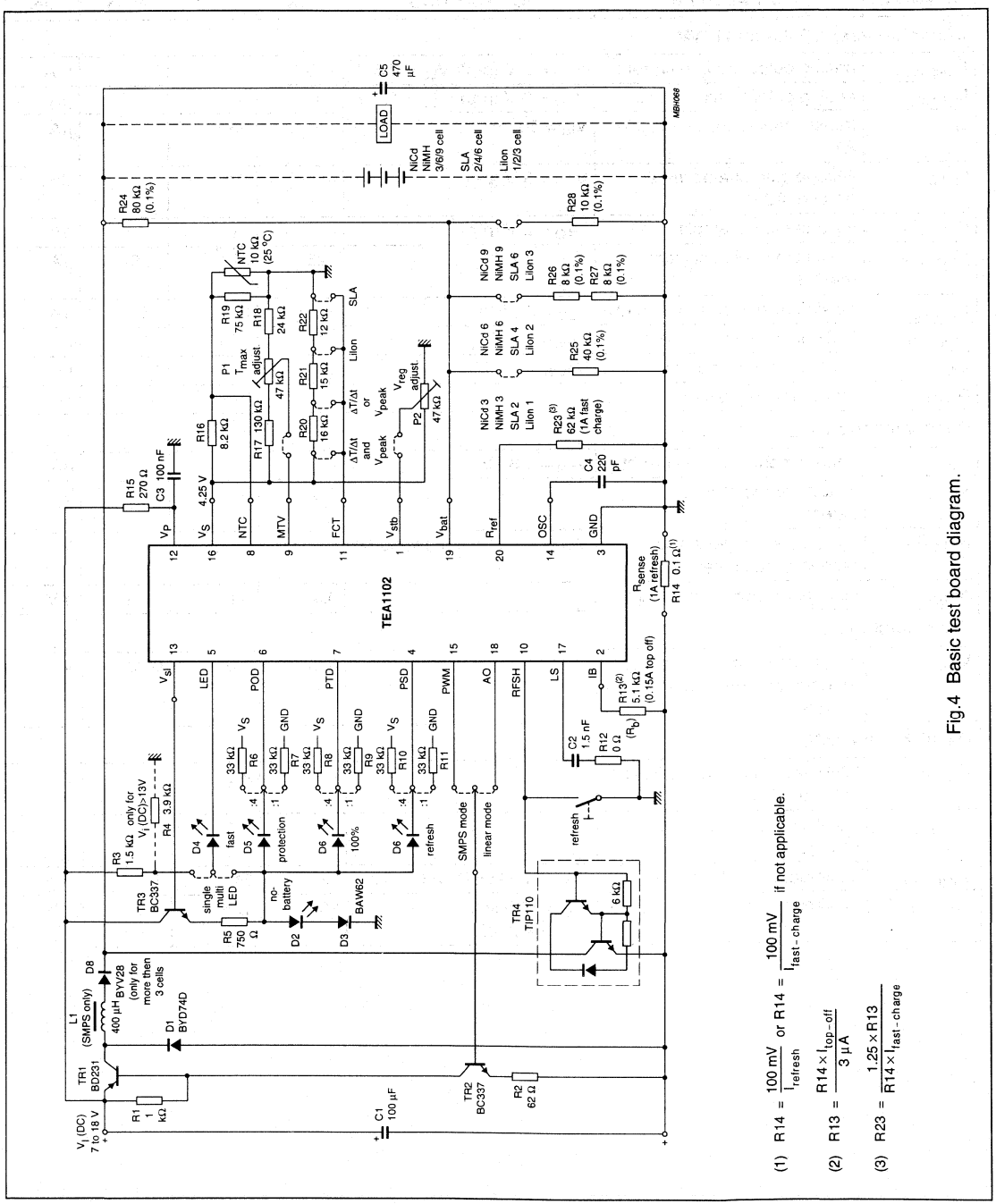
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; pins V_P, V_S, R_{ref} and V_{sl}						
V_P	supply voltage		5.45	–	11.5	V
I_P	supply current	outputs off; V_P = 11.5 V	–	4	6	mA
V_{clamp}	clamping voltage (pin 12)	I_{clamp} = 30 mA	11.5	–	12.8	V
V_{start}	start voltage		6.1	6.4	6.7	V
V_{LSP}	low supply protection level		4.65	5.05	5.45	V
V_S	source voltage (stabilized)	I_S = 2 mA	4.14	4.25	4.36	V
V_{SL}	LED source voltage	I_{LED} = 50 µA	4.05	4.25	4.45	V
V_{ref}	reference voltage	I_{ref} = 20 µA; V_P = 10 V	1.21	1.25	1.29	V
TC_{Vref}	temperature coefficient of the reference voltage	T_{amb} = 0 to 45 °C; I_{ref} = 20 µA; V_{ref} = 1.25 V	0	±60	±120	ppm/K
$\Delta V_{ref}/\Delta V_P$	power supply rejection ratio of the reference voltage	f = 100 Hz; V_P = 8 V; ΔV_P = 2 V (p-p)	–46	–	–	dB
ΔV_{ref}	load rejection of source voltage	ΔI_S = 20 mA; V_P = 10 V	–	–	5	mV
I_{Rref}	current range of reference resistor		10	–	100	µA
Charge current regulation; pins IB and R_{ref}						
I_{IB}/I_{ref}	fast charge	V_{IB} = 0	0.85	1.0	1.15	V
V_{thIB}	threshold voltage at pin IB	T_{amb} = 25 °C	–2	–	+2	mV
		T_{amb} = 0 to 45 °C	–3	–	+3	mV
I_{IB}	charge current	top-off mode; V_{IB} = 0	2.5	3	3.5	µA
$I_{IB(max)}$	maximum charge current	voltage regulation full NiCd/NiMH battery; V_{IB} = 0	8.4	10	11.6	µA
$I_{IB(Lmax)}$	maximum load current	open battery; V_{IB} = 0	33	40	47	µA
$I_{IB(LI)}$	input leakage current	currentless mode	–	–	150	nA
Refresh; pin RFSH						
V_{Rsense}	sense resistor voltage	$I_{refresh} = V_{IB}/R_{sense}$; refresh mode; $I_{refresh}$ = 18 mA	85	100	115	mV
V_{RFSH}	refresh voltage for programming start of refresh	NiCd/NiMH	0	–	250	mV
V_{bat}	voltage at pin V_{bat} for detecting end of refresh	NiCd/NiMH	0.9	1.0	1.1	V
$I_{source(max)}$	maximum source current	V_{IB} = 85 mV; V_P = 10 V V_{RFSH} = 2.7 V; T_{amb} = 25 °C	1.8	2	2.2	mA
$V_{RFSH(max)}$	maximum refresh voltage	I_{RFSH} = 1 mA	2.7	–	–	V
$V_{RFSH(off)}$	voltage at pin RFSH when refresh is off		700	770	840	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Temperature related inputs; pins NTC and MTV						
V_{NTCh}	input voltage at pin NTC for detecting high temperature	pin MTV open-circuit	0.95	1	1.05	V
		MTV setting	0.9MTV	MTV	1.1MTV	V
$V_{NTCh(hy)}$	hysteresis of V_{NTCh}		60	90	120	mV
V_{NTCl}	input voltage at pin NTC, detecting low temperature		2.7	2.8	2.9	V
$V_{NTCl(hy)}$	hysteresis of V_{NTCl}		65	100	135	mV
$V_{NTC(co)}$	input voltage at pin NTC for detecting temperature cut-off		0.7MTV	0.75MTV	0.8MTV	V
$V_{NTC(bat)}$	maximum input voltage at pin NTC for detecting battery with NTC		3.15	3.3	3.45	V
I_{NTC}	input current at pin NTC	V_{NTC} = 2 V	−5	–	+5	µA
V_{MTV}	voltage level at pin MTV	default (open-circuit)	0.95	1	1.05	V
			0.5	–	2.5	V
$\Delta V_{NTC}/V_{NTC}$	$\Delta T/\Delta t$ detection level	V_{NTC} = 2 V; T_j = 0 to 50 °C	–	−0.25	–	%
Voltage regulation						
V_{reg}	regulation voltage	LiIon; I_{ref} = 20 µA	1.33	1.37	1.41	V
		SLA; I_{ref} = 20 µA	1.58	1.63	1.68	V
		NiCd and NiMH; pin V_{stb} open-circuit	1.30	1.325	1.35	V
		NiCd and NiMH; V_{stb} = 1.5 V	0.99V_{stb}	V_{stb}	1.01V_{stb}	V
		open battery	1.85	1.9	1.95	V
TC_{Vreg}	temperature coefficient of regulation voltage	V_{reg} = 1.37 V; T_{amb} = 0 to 45 °C	0	–	±120	ppm/K
g_m	transconductance of amplifier A3	V_{bat} = 1.9 V; no battery mode	–	2.8	–	mA/V
Program pin V_{stb}						
V_{stb}	open voltage at pin V_{stb}		1.30	1.325	1.35	V
$V_{stb(im)}$	voltage at pin V_{stb} for programming inhibit mode		0	–	0.8	V
$V_{stb(st)}$	voltage at pin V_{stb} for programming voltage regulation at standby	NiCd and NiMH	1.0	–	2.2	V
$V_{stb(tc)}$	voltage at pin V_{stb} for programming trickle charge at standby	NiCd and NiMH	2.6	–	V_S	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Program pins; PSD, POD and PTD						
$V_{4,6,7}$	voltage level at pins PSD, POD or PTD	default (open-circuit)	1.9	2.1	2.3	V
$V_{4,6,7(1)}$	voltage level at pins PSD, POD or PTD for programming the divider = 1		0	–	1.2	V
$V_{4,6,7(2)}$	voltage level at pins PSD, POD or PTD for programming the divider = 2		1.6	–	2.5	V
$V_{4,6,7(4)}$	voltage level at pins PSD, POD or PTD for programming the divider = 4		3.1	–	V_S	V
$I_{PODsink}$	protection current for multi-LED indication	V_{POD} = 1.5 V	8	10	12	mA
$I_{PTDsink}$	full battery current for multi-LED indication	V_{PTD} = 1.5 V	8	10	12	mA
$I_{PSDsink}$	refresh current for multi-LED indication	V_{PSD} = 1.5 V	8	10	12	mA
I_{LI}	input leakage current	V_{POD} = 4.25 V; V_{PTD} = 4.25 V; V_{PSD} = 4.25 V	0	–	50	µA
Program pin FCT						
$V_{FCT(SLA)}$	voltage level for detecting an SLA battery		0	–	0.7	V
$V_{FCT(Lilon)}$	voltage level for detecting a Lilon battery		0.9	–	1.6	V
$V_{FCT(or)}$	voltage level for programming $\Delta T/\Delta t$ or V_{peak} as fast charge termination	NiCd and NiMH	2.0	–	3.3	V
$V_{FCT(and)}$	voltage level for programming $\Delta T/\Delta t$ and V_{peak} as fast charge termination	NiCd and NiMH	3.7	–	V_S	V
V_{FCT}	voltage level at pin FCT	default (open-circuit)	2.3	2.6	2.9	V
Program pin LED						
$V_{LED(m)}$	output voltage level for programming multi-LED indication		0	–	2.5	V
$V_{LED(s)}$	output voltage level for programming single LED indication		3.1	–	V_P	V
$I_{sink(max)}$	maximum sink current	V_{LED} = 1.5 V	8	10	12	mA
$I_{LI(LED)}$	input leakage current	V_{LED} = 10 V	0	–	70	µA
		V_{LED} = 0.6 V	0	–	5	µA
$V_{o(max)}$	maximum output voltage		–	–	15	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output drivers; AO, LS and PWM						
$I_{AO(source)}$	analog output source current	V_{AO} = 3 V (p-p); V_{LS} = 2.8 V	−10	–	0	mA
$I_{AO(sink)}$	analog output sink current	V_{AO} = 3 V (p-p); V_{LS} = 1.2 V	50	–	–	µA
g_{m1}	transconductance of amplifier A1	V_{IB} = 50 mV	–	250	–	µA/V
$G_{v1,2}$	voltage gain of amplifiers A1 and A2	V_{AO} = 3 V (p-p)	–	72	–	dB
G_{v2}	voltage gain of amplifier A2	V_{AO} = 2 V (p-p)	–	11	–	dB
$I_{LS(source)}$	maximum source current (pin LS)	V_{LS} = 2.25 V	−25	−21	−16	µA
$I_{LS(sink)}$	maximum sink current (pin LS)	V_{LS} = 2.25 V	16	21	25	µA
$I_{OH(PWM)}$	HIGH level output current	V_{PWM} = 3 V	−19	−15	−11	mA
$I_{OL(PWM)}$	LOW level output current	V_{PWM} = 0.7 V	10	14	18	mA
δ_{PWM}	maximum duty factor		–	79	–	%
Battery monitor; V_{bat}						
I_{Vbat}	battery monitor input current	V_{bat} = 1.85 V	–	1	–	nA
V_{bat}	voltage range of V_{peak} detection		0.3	–	2	V
$\Delta V_{bat}/V_{bat}$	V_{peak} detection level with respect to top level	V_{bat} = 1.85 V; T_j = 0 to 50 °C	–	−0.25	–	%
ΔV_{bat}	voltage resolution for V_{peak}		0.42	0.6	0.78	mV
Protections; V_{bat}						
$V_{bat(l)}$	maximum voltage at pin V_{bat} for detecting low battery voltage		0.27	0.30	0.33	V
Oscillator; pin OSC						
$V_{osc(H)}$	HIGH level oscillator switching voltage		–	2.5	–	V
$V_{osc(L)}$	LOW level oscillator switching voltage		–	1.5	–	V
$f_{osc(min)}$	minimum oscillator frequency	R_{ref} = 125 kΩ; C_{osc} = 400 pF	19	21	23	kHz
$f_{osc(max)}$	maximum oscillator frequency	R_{ref} = 12.5 kΩ; C_{osc} = 400 pF	130	165	200	kHz

APPLICATION INFORMATION



(1) $R14 = \frac{100\ mV}{I_{refresh}}$ or $R14 = \frac{100\ mV}{I_{fast-charge}}$ if not applicable.

(2) $R13 = \frac{R14 \times I_{top-off}}{3\ \mu A}$

(3) $R23 = \frac{1.25 \times R13}{R14 \times I_{fast-charge}}$

Fig.4 Basic test board diagram.

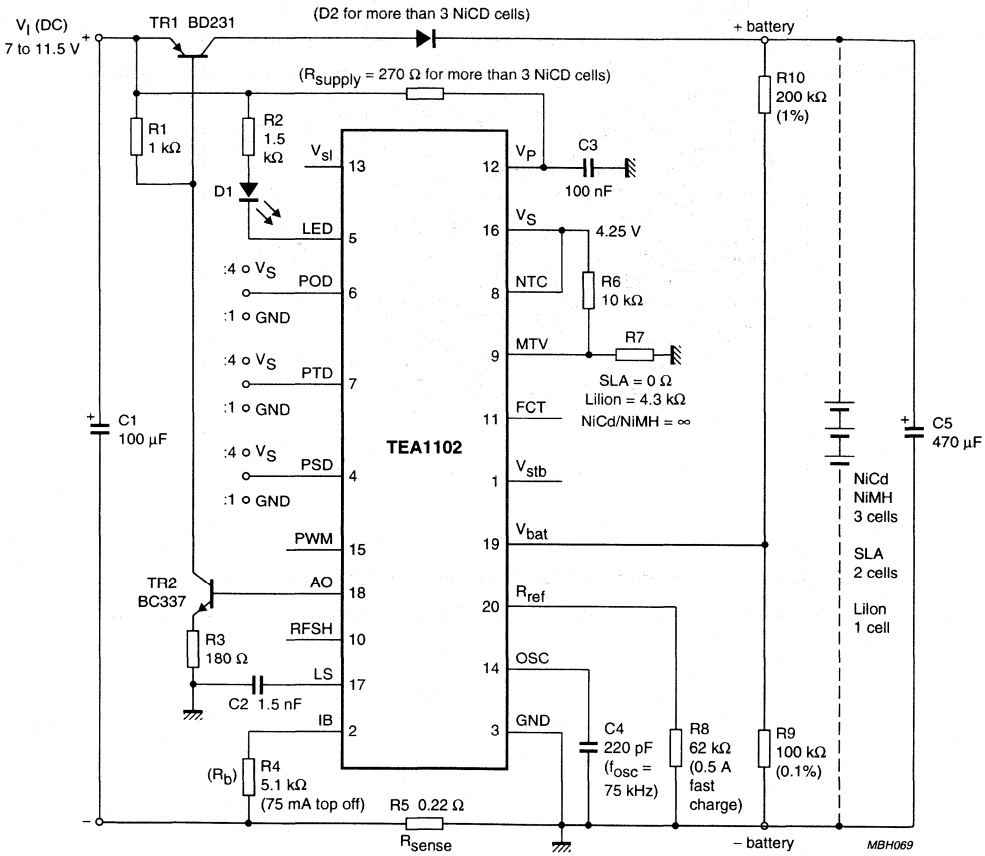


Fig.5 Linear application diagram.

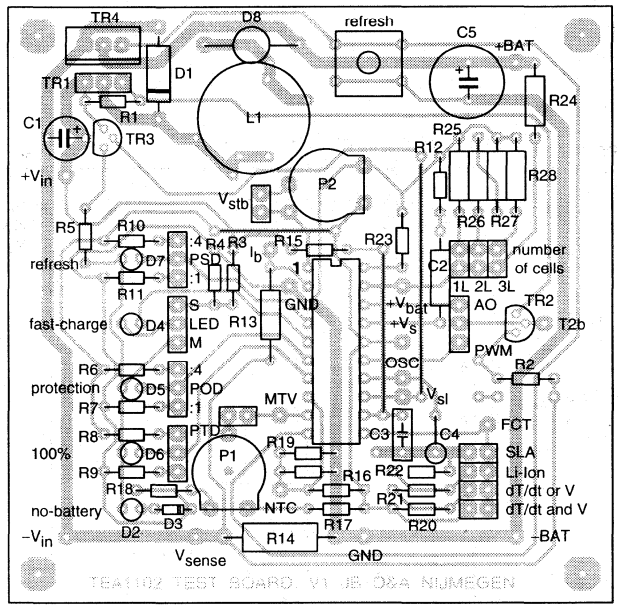


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Fig.6 Component side of printed-circuit board (test board) scale 1 : 1.

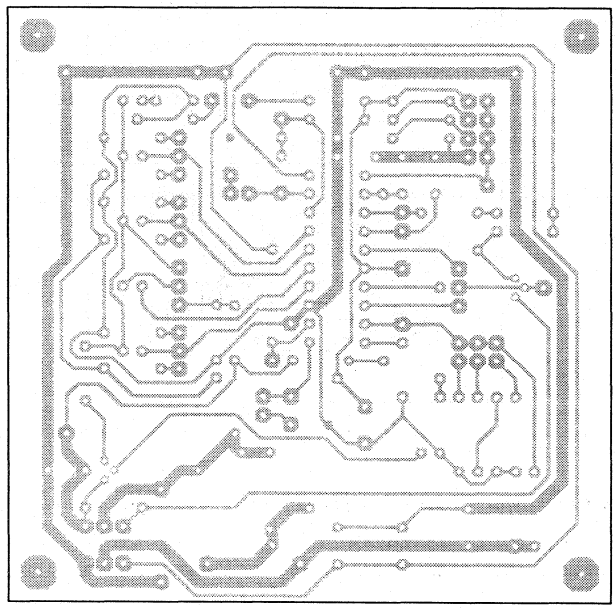


Fig.7 Track side of printed-circuit board (test board) scale 1 : 1.

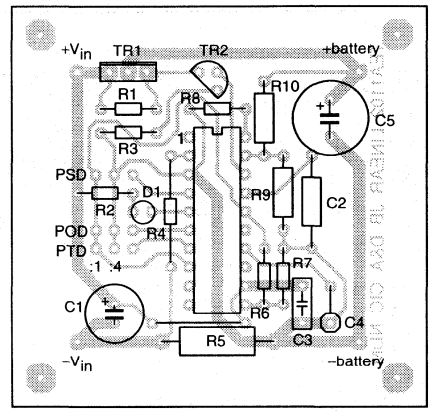


Fig.8 Component side of printed-circuit board (linear application) scale 1 : 1.

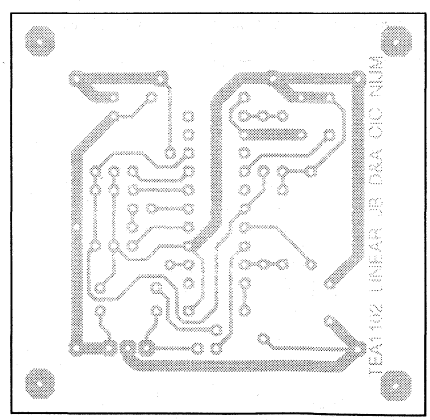


Fig.9 Track side of printed-circuit board (linear application) scale 1 : 1.

Cost effective battery monitor and fast charge IC for NiCd and NiMH chargers

TEA1104; TEA1104T

FEATURES

- Accurate detection of fully charged batteries by currentless peak voltage sensing
- Switch-over from fast to safe trickle charge current at battery full detection
- Fast charge termination back-up by maximum time and maximum temperature detection
- Several trickle charge drive possibilities for mains isolated and non-mains isolated systems
- Battery checking to protect against short-circuited and open batteries
- Battery monitor allows recharging of different battery packs in the same charger
- Dual LED indicator provision
- External regulator not required because of large input voltage range
- Few low cost external components required.

APPLICATIONS

- Portable telephone
- Portable computer
- Portable audio
- Portable video.

GENERAL DESCRIPTION

The TEA1104 is manufactured in a BiCMOS process intended to be used as a battery monitor circuit in charge systems for NiCd and NiMH batteries. It is especially designed for cost effective compact consumer applications.

The circuit is able to detect fully charged batteries by currentless battery voltage sensing. Several output drive functions are available to control the (reduced) trickle charge current to keep the batteries full with maximum life expectations.

The battery full detection is backed up by two independent mechanisms to make the system fail safe; maximum time and maximum temperature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		5.45	–	11.5	V
I_P	supply current	outputs off	–	–	3	mA
V_{bat}	voltage range of battery full detection		0.81	–	3.6	V
$\Delta V_{bat}/V_{bat}$	voltage peak detection level with respect to top value		–	0.25	–	%
I_{bat}	battery monitor input current		–	–	1	nA
$V_{bat(l)}$	battery voltage protection low		–	0.81	0.91	V
$V_{bat(h)}$	battery voltage protection high		3.5	3.6	–	V
f_{osc}	oscillator frequency		10	–	100	kHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1104	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TEA1104T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

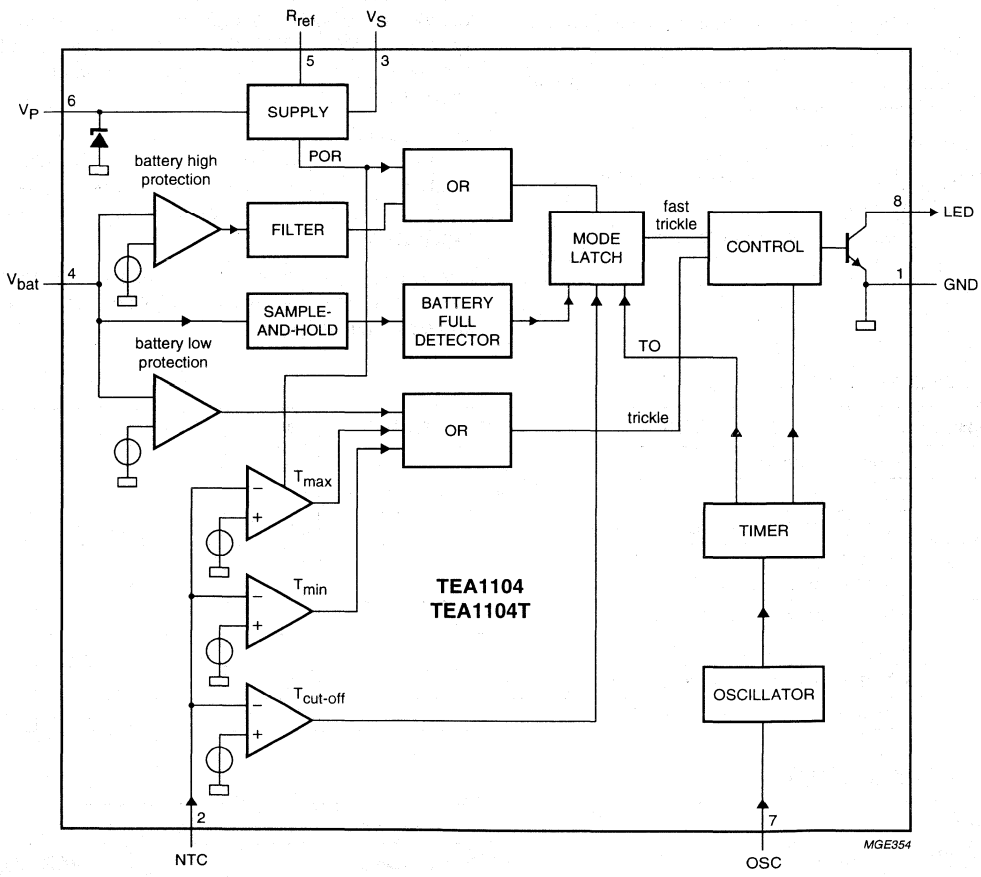


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
NTC	2	negative temperature coefficient resistor input
V_S	3	stabilized supply voltage
V_{bat}	4	battery voltage sensing
R_{ref}	5	reference resistor
V_P	6	positive supply voltage
OSC	7	oscillator input
LED	8	LED output

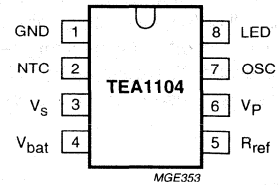


Fig.2 Pin configuration.

INTRODUCTION

The operation of the TEA1104; TEA1104T is explained with the aid of the application diagram illustrated in Fig.7.

An application note (AN95085) is available describing the versatility of the TEA1104; TEA1104T.

An external power current source charges the batteries via an electronic switch which is controlled by the TEA1104. The TEA1104 monitors the battery voltage. Fully charged batteries are detected when the battery voltage peaks. In fact, a voltage drop of 0.25% with respect to the top value is detected. Fast charging is initiated at 'power on' or at 'replaced batteries'. The switch is continuously on, providing that all protection levels are met. At battery full detection, the charge current is duty cycled to reduce the average charge current to a lower level, keeping the batteries fully charged but at he same time assuring long battery life. In Fig.3 the battery voltage during fast charge is plotted.

FUNCTIONAL DESCRIPTION

A block diagram of the TEA1104; TEA1104T is illustrated in Fig.1

Mode latch

The Mode latch determines if the system is in the fast or in the slow charge mode.

- Fast charge is active at:
  - power switch-on and battery connected
  - temperature between minimum and maximum value
  - battery insert
- Trickle charge is active if:
  - battery full is detected
  - maximum time is exceeded
  - maximum cut-off temperature is exceeded after the initial phase.

Supply block

For correct start-up, the IC supply current is limited to 35 µA (typ.) until the start-up voltage of 6.4 V is reached (standby mode). Thereafter, the operating supply voltage V_P has to be within the window of 5.45 to 11.5 V, meaning that there is no need for an external voltage regulator to supply the IC.

The supply block delivers the following outputs:

- With the help of an external resistor (pin R_{ref}), a reference current is obtained which defines the accuracy of all IC timing characteristics
- Externally available 4.25 V stabilized voltage source (V_{source}). This source is used internally to supply a large part of the circuit and can be used to set the NTC biasing and to supply other external circuitry with a maximum current of 1 mA. Protection information is provided via V_S, to design a dual LED indicator
- Power-on reset pulse resets all digital circuitry after a start or restart, due to an interrupted V_S.

Open battery protection

When the rechargeable battery is removed, the output voltage V_{bat} will rise to a high level. The 'open battery protection' block will detect this voltage and the charge current will be switched off. A digital filter prevents false open battery protection. The open battery signal (V_{bat} > 3.6 V) must be present for a duration of at least 4 clock pulses.

Battery monitor

One or two cell packs can be connected directly to V_{bat} (battery connection) without an external resistor divider. At larger cell packs the battery voltage must be scaled down to a voltage range of 0.81 to 3.6 V. It is also possible to take a tap on the chain of batteries. Battery full is recognized by voltage peak detection (V_{peak}), meaning a decrease of 0.25% (typ.) with respect to the top value. Keeping in mind a battery voltage range of 0.81 to 3.6 V and an accuracy of 10% at V_{bat} = 2.4 V for battery full detection, means that the internal ADC has to be 13 bits. Several filters are included to prevent false full detection. The series resistance of the battery and battery connection can cause battery voltage fluctuations and therefore it is necessary to stop the charging before sensing; this is called the 'inhibit time'. This will be performed automatically via the regulation output pin LED. The charging is stopped for ten oscillator periods at the end of which sampling is performed. The battery voltage will now be sensed in a currentless way.

Timer/oscillator

The oscillator has a sawtooth shape.

The period time is defined by: $t_{osc} = K \times R_{ref} \times C_{osc}$

The oscillator frequency is used in the timer block. In this block several important signals are created.

- Time-out for protecting the fast charge process in time. Time-out is normally chosen to be 25% longer than the associated fast charge time. So for a one hour charge time, time-out = 1.25 hours. The relationship with the oscillator period time is:
  - Time-out = 2 exp28 $\times$ t_{osc}
- The duty factor in the trickle charge mode: The duty factor is fixed to $1/40$, meaning that the average:
  - $I_{trickle} = 1/40 \times I_{fast}$
  - $t_{on} = 3/4 \times 2$ exp9 $\times$ t_{osc}
  - $t_{off} = 2$ exp14 $\times$ t_{osc}.
- The battery voltage is sensed each 'cycle time'. The cycle time is defined as:
  - $T_{cycle} = 2$ exp16 $\times$ t_{osc}
- The 'inhibit time' is the time that the charger current is disabled, after which the battery voltage is sensed in a currentless way.
  - $t_{inhibit} = 10 \times t_{osc}$

  Battery sampling takes one oscillator period for each cycle interval.
  - $t_{sample} = t_{osc}$
- The 'disable time' is present to correct start-up with flat or polarized batteries. During the disable time, the battery full detection is not active.
  - $t_{disable} = 2$ exp $-5 \times$ time-out

The timer is reset by battery full detection, but is on hold during the temperature and battery-low protection modes.

Temperature protection block

Temperature sensing is achieved by using a cheap thermistor. Two temperature windows are built in:

- If the temperature at power-on reset is above the maximum temperature protection level, the trickle charge current is active. The same applies for temperatures below the minimum temperature. Fast charging starts when the temperature is in between the minimum and the maximum temperature levels.
- If the temperature is between the maximum and minimum temperature at power-on reset, the fast charge current level is active. If the temperature sinks below the minimum temperature level, again the trickle charge level is active. At rising temperature, the fast charge current is latched off at the 'cut off' temperature level.

To avoid switching on and off with temperature, a hysteresis is built in for low temperature level. If the temperature protection is not necessary, pin 'Negative Temperature Coefficient resistor' (NTC) must be connected to pin R_{ref}.

Battery low protections

When the battery voltage is less than 0.81 V, the circuit assumes that there are short circuited batteries and the charge current is reduced to the trickle charge level. If the batteries are flat, the trickle charge current is able to raise the battery voltage within an acceptable period of time, after which fast charging starts.

Output drivers

Several output drive possibilities are supported by the TEA1104, to limit the fast charge current and to indicate the mode that the charge is in.

In mains isolated systems, output drive current is available for a bipolar or MOS switching device. Moreover, current regulators can be driven (see Fig.4).

In non mains isolated systems, the current source can be switched via the auxiliary winding (see Fig.6) using the TEA140X power plugs.

In the application section, an example is shown driving two LEDs that are indicating fast charging, protection during fast charging, full status and removed batteries. It is also possible to output the same information via one LED only.

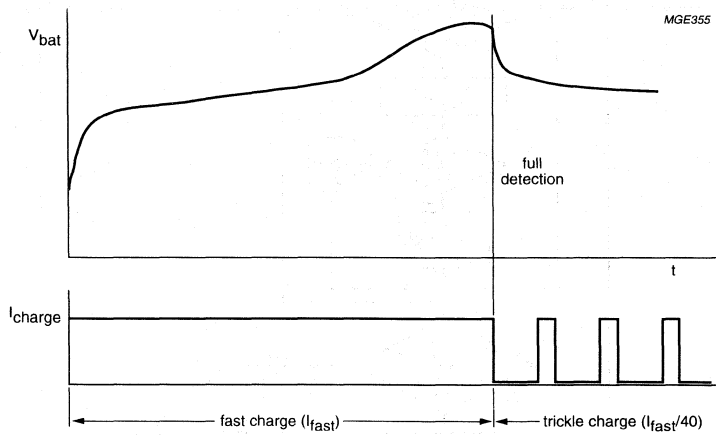


Fig.3 NiCd battery characteristics during a 1.25C charge cycle.

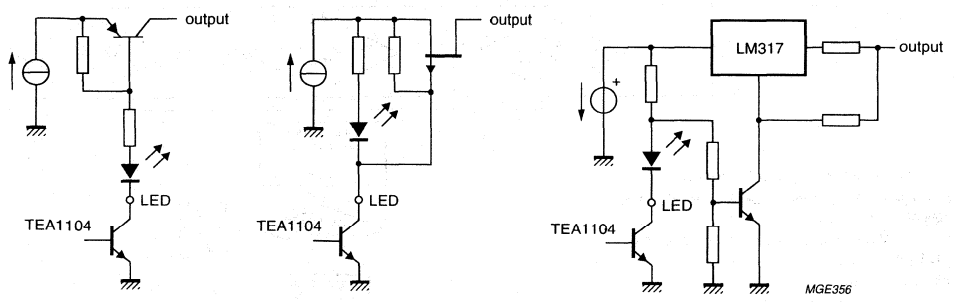
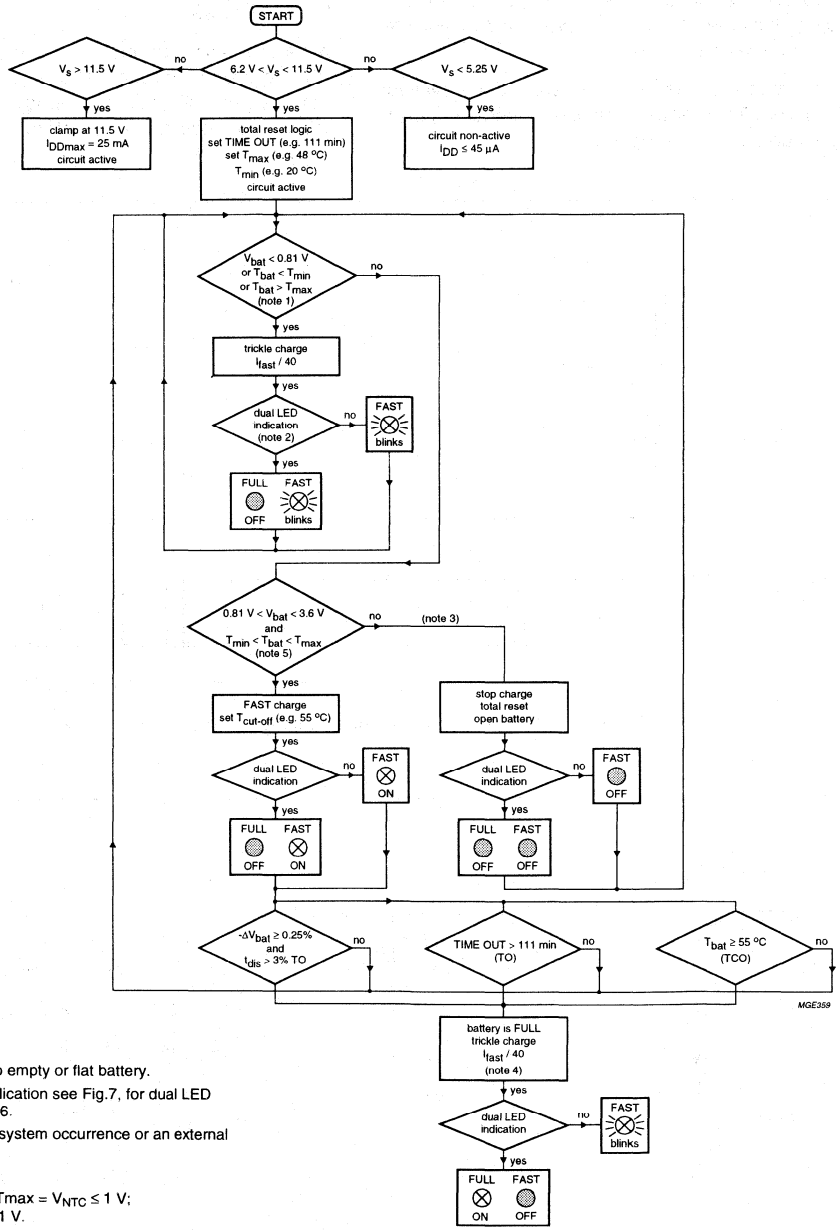


Fig.4 Output drivers.



(1) V_{bat} < 0.81 V due to empty or flat battery.

(2) For single LED application see Fig.7, for dual LED application see Fig.6.

(3) V_{bat} > 3.6 V due to system occurrence or an external inhibit via pin V_{bat}.

(4) Release via reset.

(5) T_{min} = V_{NTC} ≥ 2 V; Tmax = V_{NTC} ≤ 1 V; $T_{cut-off}$ = V_{NTC} ≤ 0.81 V.

Fig.5 Flow chart of the TEA1104.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		−0.5	+13.2	V
V_{oLED}	LED output voltage (pin 8)		−0.5	V_P	V
V_{iNTC}	negative temperature coefficient resistor input voltage (pin 2)		−0.5	+5	V
$V_{i(OSC)}$	oscillator input voltage (pin 7)		−0.5	+5	V
$V_{i(bat)}$	battery input voltage (pin 4)		−0.5	+5	V
V_{Rref}	reference resistor voltage (pin 5)		−0.5	+5	V
I_{source}	output source current		−3	+0.01	mA
I_{oLED}	LED output current		−	25	mA
I_{Rref}	reference resistor current		−1	+0.01	mA
I_{bat}	battery current		−1	+1	mA
V_P	supply current		−	25	mA
P_{tot}	total power dissipation	T_{amb} = 70 °C			
		TEA1104	−	0.5	W
		TEA1104T	−	0.35	W
T_{amb}	operating ambient temperature		−20	+70	°C
$T_{j(max)}$	maximum operating junction temperature		−	+150	°C
T_{stg}	storage temperature		−55	+150	°C

Note

1. All voltages are measured with respect to ground; positive currents flow into the IC. The voltage ratings are valid provided that other ratings are not violated; current ratings are valid provided that the power rating is not violated.

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611 part E"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °C; R_{ref} = 33 kΩ; C_{OSC} = 1 nF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		5.45	–	11.5	V
$\Delta V_P/\Delta t$	supply voltage start rate		–	–	0.5	V/µs
V_{clamp}	clamping voltage	I_{clamp} = 25 mA	11.5	–	12.8	V
V_{start}	start-up voltage		6.1	6.4	6.7	V
V_{pd}	power-down voltage level		4.65	5.05	5.45	V
I_P	supply current	outputs off	–	–	3	mA
I_{start}	start-up current	V_P = 4 V	–	45	50	µA
V_S	stabilized voltage	I_S = 1 mA	4.03	4.25	4.46	V
V_{Rref}	voltage range at reference resistor	I_{Rref} = 20 µA	1.18	1.25	1.31	V
TC_{Vref}	temperature coefficient of the reference voltage	T_{amb} = 0 to 45 °C	–	±60	±120	ppm/K
I_{Rref}	current range of the reference resistor		10	–	100	µA
Temperature related input; NTC						
$V_{i(co)}$	input voltage level for detecting temperature cut-off		0.75	0.81	0.87	V
$V_{i(co;\ max)}$	maximum input voltage level for detecting temperature cut-off		0.92	1.0	1.08	V
$V_{i(co;\ min)}$	minimum input voltage level for detecting temperature cut-off		1.85	2.0	2.15	V
I_{NTC}	input current	V_{NTC} = 1.5 V	−5	–	+5	µA
Output drivers						
δ_{LED}	LED pulse duty factor		2.4	2.5	2.6	%
$V_{LED(sat)}$	LED saturation voltage	$I_{LED(sat)}$ = 15 mA	–	–	600	mV
$I_{LI(LED)}$	LED input leakage current	V_{LED} = 15 V	–	–	5	µA
Battery monitor						
$I_{i(bat)}$	input battery current	V_{bat} = 2.4 V	–	1	–	nA
V_{bat}	voltage range for peak detection		0.81	–	3.6	V
$\Delta V_{bat}/V_{bat}$	peak detection level with respect to top level	V_{bat} = 2 V	–	0.25	–	%
T_j	temperature range of peak detection		0	–	50	°C
Protections; BAT						
$V_{bat(l)}$	low level battery protection voltage		–	0.81	0.91	V
$V_{bat(h)}$	high level battery protection voltage		3.5	3.6	4.5	V
Oscillator						
k	correction factor		0.84	0.93	1.02	
f_{osc}	frequency range		10	–	100	kHz

APPLICATION INFORMATION

A guideline for the settings of TEA1104 and its external components selection is given based on an example of a 1 hour charger for a 4 cell NiCd or NiMH battery pack. The basic application diagram as illustrated in Fig.6 which is based on the application diagram illustrated in Fig.7 with some additional components; a 2 LED charge status indication has been provided.

For charging a battery within one hour the charge current rating should be as follows:

Required minimum charge current = battery capacity × 1.2/charge time.

Therefore, for a 1 Ah battery the external charge current supply has to deliver at least 1.2 A.

TEA1104 settings

The fast charge back-up timer period, time-out, has to be set in relation to the expected maximum charge time. Normally, a safety back-up time is chosen approximately 25% longer than the maximum expected fast charge time. For a one hour charger the time-out period can be set to 1.25 h.

Time-out relationship with the oscillator repetition time is as follows;

t_{osc} = time-out (h) × 3600/2 exp28

t_{osc} = 17μs for time-out = 1.25 h

t_{osc} is set with the combination of C_{osc} and R_{ref}; where $t_{osc} = 0.93 \times R_{ref} \times C_{osc}$.

R_{ref} can be chosen between 13 and 120 kΩ, but a 27 kΩ resistor is recommended. The oscillator capacitor can be calculated which is 668 pF; the nearest higher practical value is 680 pF.

In the trickle charge mode the LED output will pulsate with a repetition time; $t_{trickle} = 2\ exp14 \times t_{osc} = 0.28$ s.

The duty factor of the pulse is 2.5% of $t_{trickle}$. This duty factor also applies to the charge current as the charge current switch is driven by the LED output. Therefore, the average trickle charge current is I_{fast} /40. The V_{bat} input can be adapted to the battery voltage via the resistor dividers R1 and R2. When an NTC thermistor has been incorporated into the battery, the minimum, maximum and cut-off temperature levels can be set with the resistors R3 and R4. For an NTC with a common sensitivity of 3965 and adjustment resistor values R3 = 13 kΩ, R4 = 20 kΩ the minimum, maximum and cut-off temperatures will be 5, 42 and 50 °C respectively.

The flow chart of the TEA1104; TEA1104A is given in Fig.5. The load state of the batteries can be displayed by one or two LEDs. The flow chart is not to be regarded as sequential. Each mode of operation is a purely separate continuous process.

Table 1 Dual LED indication

CHARGER MODE	V_{LED}	V_S	LED 1	LED 2
Fast charging	low	high	on	off
Fast charging protection	low/high	high	on/off	off
Full (trickle charging)	low/high	low	off	on
Battery open	high	high	off	off

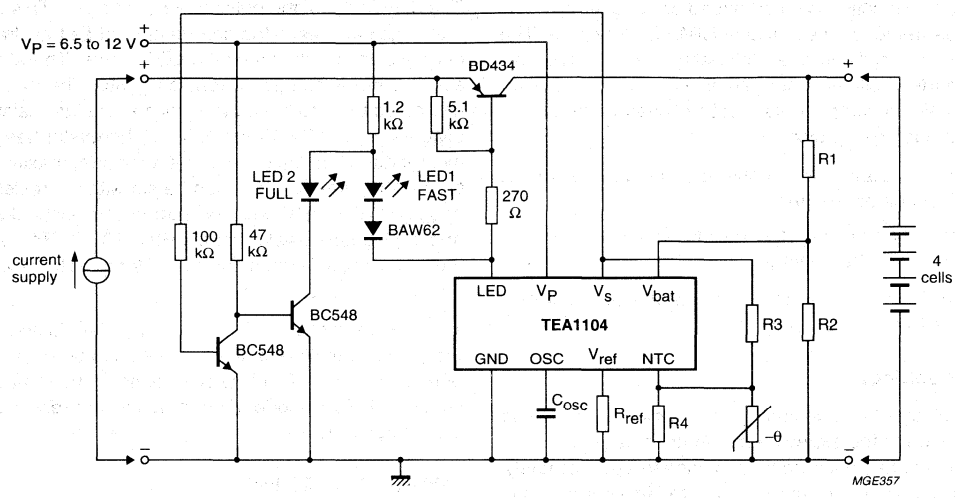


Fig.6 Basic application diagram.

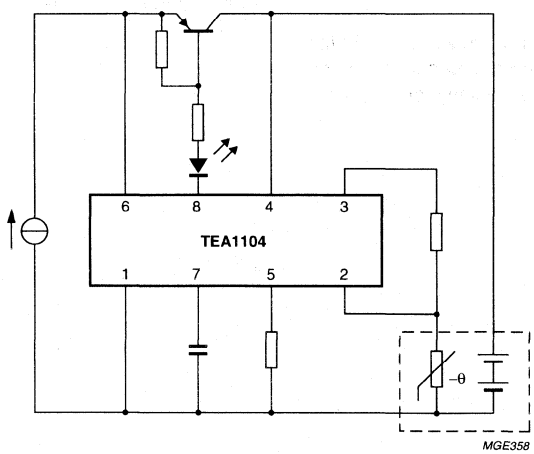


Fig.7 Application diagram.

Threshold detector and reset generator PCF1252-X family

FEATURES

- Very low current consumption, typically 10 μA
- 10 factory programmed threshold voltages available covering trip voltages from 4.75 to 2.55 V
- ±50 mV trip point accuracy over full temperature range
- Variable RESET delay
- RESET pulse polarity selection
- Defined outputs at 0.6 V (typ.)
- Comparator for second level detection (e.g. overvoltage detection)
- Advance warning of power fail
- Operating temperature range –40 to +85 °C.

GENERAL DESCRIPTION

The PCF1252-Xs are low-power CMOS voltage threshold detectors designed especially for supervision of microcontroller/microprocessor systems for detection of power-on/off conditions and generation of a system reset pulse. The PCF1252-X also provides a $\overline{\text{POWF}}$ (power fail) output which is activated at a precise factory-programmed trip point. A system RESET output has a built-in delay with duration determined by an external capacitor (C_{CT}).

A second comparator (comparator 2) has been included to enable the possibility of a second monitoring point in the system.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1252-XP(1)	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF1252-XT(1)	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Note

1. X = 0 to 9; depending on threshold voltage.

BLOCK DIAGRAM

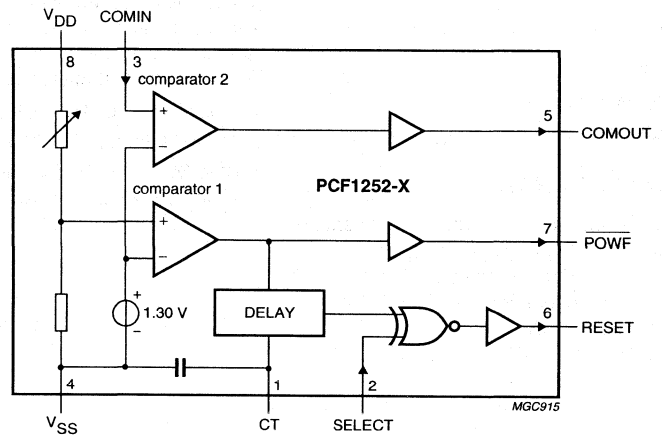


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CT	1	connection for the external capacitor
SELECT	2	select polarity or external reset input
COMIN	3	comparator input
V_{SS}	4	ground (0 V)
COMOUT	5	comparator output
RESET	6	reset output
$\overline{POWF}$	7	power failure signal output
V_{DD}	8	supply voltage

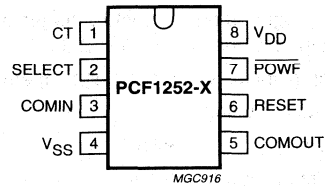


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION (see Fig.1)

The PCF1252-X contains:

- A precise factory-programmed voltage reference
- Two comparators
- A delay circuit.

The PCF1252-X family is comprised of 10 versions with different factory-programmed voltage trip-points (V_{TRIP}), see Chapter "Characteristics".

Supply

The supply voltage (V_{DD}) is internally divided before being compared, via comparator 1, with the internal reference voltage.

$\overline{POWF}$ (see Fig.3)

The $\overline{POWF}$ output is:

- LOW, if V_{DD} is below V_{TRIP}
- HIGH, if V_{DD} is above V_{TRIP}.

Power-on reset (SELECT = LOW)

As V_{DD} rises past V_{TRIP}, a positive reset pulse is generated at RESET. The duration of the reset pulse (t_R) is determined by the value of the external capacitor (C_{CT}; maximum 1 µF, see Fig.8) connected to CT. With no external capacitor connected, C_{CT} assumes a minimum value of 100 pF. If SELECT is HIGH, the reset pulse is inverted.

Power failure

During a power-off condition ($V_{DD} < V_{TRIP}$), $\overline{POWF}$ goes LOW. After a time delay (t_S), also determined by C_{CT}, RESET goes HIGH. Any $\overline{POWF}$ assertion ($V_{DD} < V_{TRIP}$) will result in a subsequent RESET pulse.

Voltage trip-point

By selecting the voltage trip-point slightly higher than the minimum operating voltage of the microcontroller/microprocessor, there is sufficient time for data storage before the power actually fails.

In order to prevent oscillations around the voltage trip-point, a small hysteresis has been included, resulting in a power-on switching point that is higher than the voltage trip-point (minimum of 15 mV). The voltage trip-point refers to the value at which power-off is signalled.

COMIN

Input to the second comparator (comparator 2). When used in conjunction with an external voltage divider, this allows a second point in the system to be monitored. This input has no built-in hysteresis. When not in use connect to V_{DD}. COMOUT will be LOW or HIGH depending on the voltage at COMIN:

- COMOUT = HIGH, if voltage at COMIN is above the switch point V_{SP} (typically 1.30 V).
- COMOUT = LOW, if voltage at COMIN is below the switch point V_{SP} (typically 1.30 V).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+7.0	V
V_I	input voltage		−0.5	V_{DD} + 0.5	V
I_I	DC clamp-diode current	all pins: $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	–	20	mA
I_O	output current		–	20	mA
P_{tot}	total power dissipation		–	150	mW
T_{stg}	storage temperature		−65	+100	°C
T_{amb}	operating ambient temperature		−40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal handling precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

CHARACTERISTICS

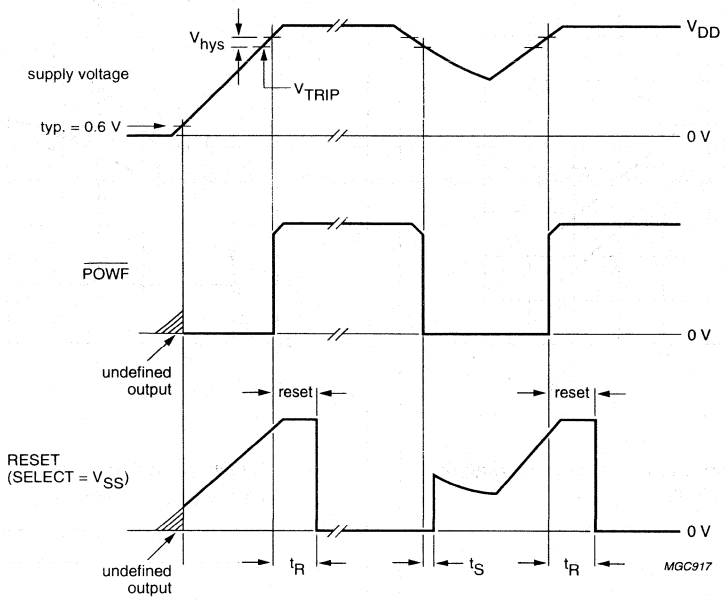
V_{DD} = 2.4 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; (see Fig.3); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.4	–	6.0	V
V_{TRIP}	Voltage trip-point:	T_{amb} = 25 °C				
	PCF1252-0		4.70	4.75	4.80	V
	PCF1252-1		4.50	4.55	4.60	V
	PCF1252-2		4.20	4.25	4.30	V
	PCF1252-3		4.00	4.05	4.10	V
	PCF1252-4		3.70	3.75	3.80	V
	PCF1252-5		3.50	3.55	3.60	V
	PCF1252-6		3.20	3.25	3.30	V
	PCF1252-7		3.00	3.05	3.10	V
	PCF1252-8		2.70	2.75	2.80	V
	PCF1252-9		2.50	2.55	2.60	V
I_{DD}	supply current	T_{amb} = 25 °C; $V_{DD} = V_{TRIP} + 0.5$ V; COMIN = V_{DD}; see Figs. 4 and 5	–	10	15	µA
ΔV_{TRIP}	voltage trip-point temperature coefficient	note 1	–	$\pm 100 \times 10^{-6}$	$\pm 400 \times 10^{-6}$	mV/K
V_{hys}	voltage trip-point hysteresis		15	30	50	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
COMIN						
V_{SP}	COMIN switch point	T_{amb} = 25 °C	1.28	1.30	1.32	V
ΔV_{SP}	COMIN switch point temperature coefficient	note 1	–	±0.1	±0.5	mV/K
SELECT						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
SELECT and COMIN						
I_{LI}	LOW level leakage input current		–	–	–1.0	µA
I_{LI}	HIGH level leakage input current		–	–	1.0	µA
$\overline{\text{POWF}}$, RESET and COMOUT						
I_O	output sink current	V_O = 0.4 V; V_{DD} = 2.4 V; see Fig.6	1	3	–	mA
I_O	output source current	V_O = 2.0 V; V_{DD} = 2.4 V; see Fig.7	–0.75	–2	–	mA
t_R	reset time	C_{CT} = 1 nF; note 2	400	1000	2000	µs
t_S	save time	C_{CT} = 1 nF; note 2	40	100	200	µs
t_R/t_S	reset to save time ratio		–	10	–	
C_{int}	CT internal capacitance		–	100	–	pF

Notes

1. Values given per degree Kelvin; tested on a sample basis.
2. Conformance to these specifications is only guaranteed if the slew rate of V_{DD} is less than 25 V/ms.



t_R = reset time (duration of reset pulse).

t_S = save time (time between assertion of $\overline{POWF}$ and assertion of the reset output). This time can be used for storing of critical data and orderly system shut-down.

V_{hys} = hysteresis voltage (prevents oscillation around V_{TRIP}).

Fig.3 Timing diagram.

Typical performance characteristics

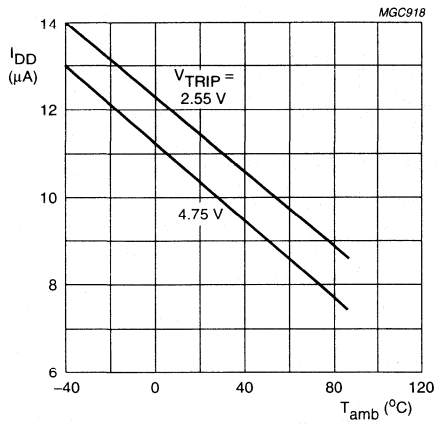


Fig.4 Supply current as a function of temperature; V_{DD} = 5 V; COMIN = V_{DD}.

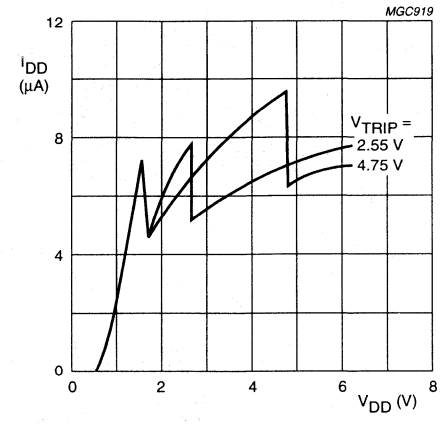


Fig.5 Supply current as a function of the supply voltage; T_{amb} = +25 °C.

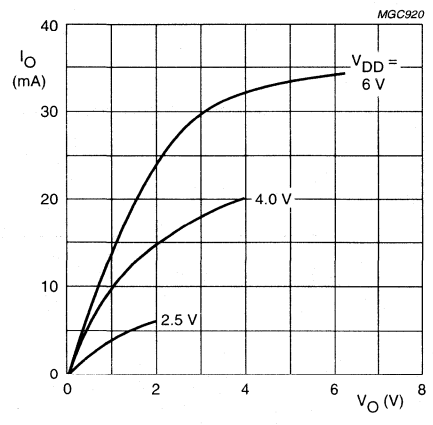


Fig.6 Output sink current as a function of the output voltage.

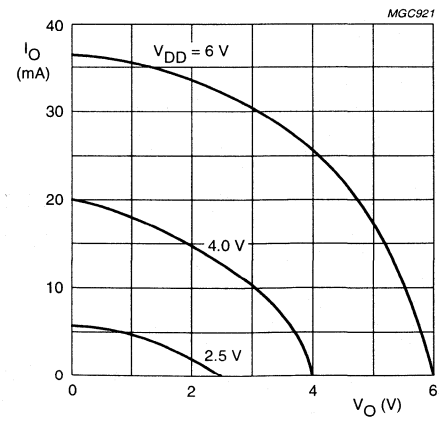
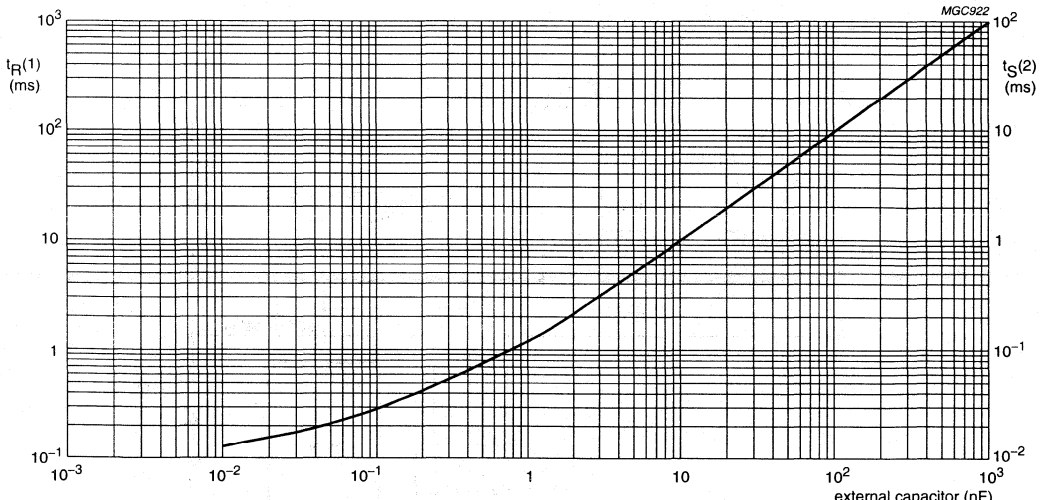


Fig.7 Output source current as a function of the output voltage.



(1) t_R (typ.) = (0.1 + C_{CT}) ms.
(2) t_S (typ.) = (0.01 + 0.1 C_{CT}) ms.

Fig.8 Reset and save times as a function of the external capacitor (C_{CT}).

APPLICATION INFORMATION

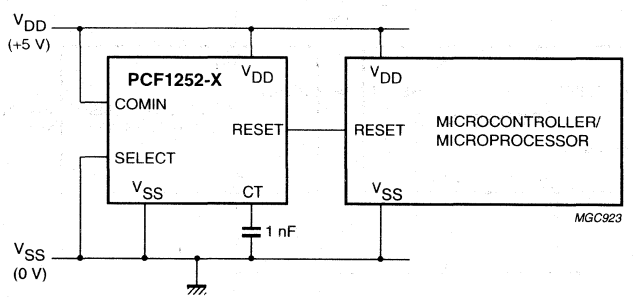


Fig.9 Typical power-on reset circuit for a microcontroller/microprocessor system; (when not used, COMIN must be connected to V_{DD}).

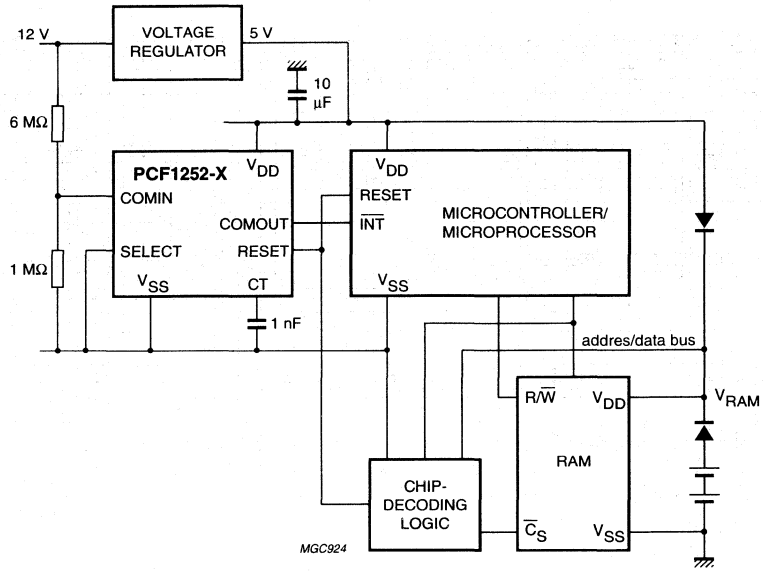
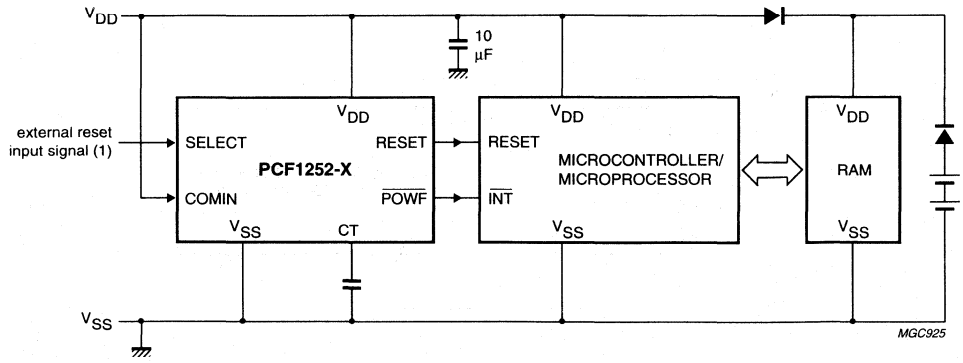


Fig.10 Data retention circuit for memory back-up systems.



(1) For external reset application, the SELECT input must be debounced.

Fig.11 Data retention circuit with external switchable reset for systems with a single voltage supply.

Section 15
Discrete Transistors and Power Modules

CONTENTS

Discrete Front End Selector Guide 15–2
RF Power Modules for Portable Equipment 15–3
RF Power Transistors for Portable Equipment 15–4
RF Wideband Transistors Selector Guide 15–6
MOSFETS Selector Guide 15–21

Discrete Front End Selector Guide

FUNCTION	SYSTEM FREQUENCY (MHZ)	SOT23	SOT323	SOT143(1)	SOT343(1)	SOT353(2)	SOT363(2)
LNA	900;1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505
	900:1900	BFR520	BFS520	BFG520	BFG520W	BFC520	BFM520
MIXER	900	BFR93A	BFR93AW	BFG83A	BFG83AW		
	900;1900	BFR505	BFS505	BFG505	BFG505W	BFE505	BFM505
	900;1900	BFR520	BFS520	BFG520	BFG520W	BFE520	BFM520
BUFFER AND VCO	900	BFR92A	BFR92AW	BFG92A	BFG92AW		
	900	BFR93A	BFR93AW	BFG93A	BFG93AW		
	900	BFQ67	BFQ67W	BFG87	BFG87W		
	900;1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505
	900;1900	BFR520	BFS520	BFG520	BFG520W	BFC520	BFM520
IF	40 TO 100	BF547	BF547W				
		BFS17	BFS17W	BFG17A			
		BFR92A	BFR92AW	BFG92A	BFG92AW		

1. Also available in /X and /XR versions.
2. Under development.

RF Power Modules for Portable Equipment

TYPE NUMBER	APPLICATION	FREQUENCY BAND (MHZ)	SUPPLY VOLTAGE (V)	LOAD POWER (W) MIN.	DRIVE POWER (inW)	POWER GAIN (DB) MIN.	EFFICIENCY (%) MIN.	EFFICIENCY (%) TYP.	PACKAGE	PACKAGE THICKNESS (min)
ANALOG CELLULAR										
BGY115A	AMPS	824–849	6.0	1.2	2	27.8	45	50	SOT321	4
BGY115B	(E) TACS	872–905	6.0	1.2	2	27.8	45	50	SOT321	4
BGY115D	Spread Spectrum	902–928	6.0	1.2	2	27.8	45	50	SOT321	4
BGY118A	AMPS	824–849	4.8	1.2	2	27.8	50	55	SOT321	4
BGY118B	(E)TACS	872–905	4.8	1.2	2	27.8	50	55	SOT321	4
BGY118D	SPREAD SPEC-TRUM	898–928	4.8	1.2	2	27.8	50	55	SOT321	4
BGY119A	AMPS	824–849	4.8	1.2	2	27.8	50	55	SOT359	3
BGY119B	(E)TACS	872–905	4.8	1.2	2	27.8	50	55	SOT359	3
BGY119D	Spread Spectrum	902–928	4.8	1.2	2	27.8	50	55	SOT359	3
BGY122A	AMPS	824–849	4.8	1.2	2	27.8	50	55	SOT388	2
BGY122B[1]	(E)TACS	872–905	4.8	1.2	2	27.8	50	55	SOT388	2
BGY122D[1]	Spread Spectrum	898–928	4.8	1.2	2	27.8	50	55	SOT388	2
BGY120A	AMPS	824–829	3.6	1.2	2	27.8	50	55	SOT388	2
BGY120B[2]	(E)TACS	872–905	3.6	1.2	2	27.8	50	55	SOT388	2
BGY120D[2]	Spread Spectrum	898–928	3.6	1.2	2	27.8	50	55	SOT388	2
DIGITAL CELLULAR										
BGY201	GSM	880–915	12.5	14	1	41.5	33	35	SOT278A	7
BGY202	GSM	890–915	6.0	1.4	2	28.5	45	50	SOT321	4
BGY203	GSM	880–915	6.0	3.5	1	35.5	40	–	SOT342	4
BGY205	GSM	880–915	6.0	3.5	2	32.5	–	45	SOT321B	3
BGY204[1]	GSM	880–915	4.8	3.2	2	32.5	–	45	SOT321B	3
BGY206[1]	GSM	880–915	4.8	3.0	5	27.8	–	45	SOT308	2
BGY207[1]	GSM	880–915	4.8	1.2	2	27.8	50	55	SOT359	3
BGY208[1]	GSM	880–915	6.8	3.5	10	30.7	–	45	SOT388	2

1. Preliminary specification
2. Objective specification

RF Power Transistors for Portable Equipment

TYPE NUMBER	FREQUENCY (MHZ)	SUPPLY VOLTAGE (V)	LOAD POWER (W)	POWER GAIN (DB) MIN.	EFFICIENCY (%) MIN.	EFFICIENCY (%) TYP.	RESISTANCE$_3$ (K/W)	THERMAL PACKAGE
ANALOG CELLULAR								
BLT80	900	7.5	0.8	6	60	67	22[4]	SOT223
BLT81	900	7.5	1.2	6	60	70	32[5]	SOT223
BLT80	900	6.0	0.8	6		70	22[4]	SOT223
BLT81	900	6.0	1.2	6		70	32[5]	SOT223
BLT70	900	4.8	0.6	6	60		38[6]	SOT223
BLT71	900	4.8	1.2	6	60		24[7]	SOT223
BLT71/81	900	4.8	1.2	10	55	63	50[11]	SOT86 (SO8pl)
BLT61	900	3.8	1.2	6	50	60	30[8]	SOT86 (SO8pl)
DIGITAL CELLULAR								
BFG540W	900	8.0	18 dBM	6	60	67	22[4]	SOT433
BFG540W	1900	3.6	14 dBm	6	60	67	22[4]	SOT433
BFG10W/x	900	6.0	28 dBm	6	60	67	22[4]	SOT433
BFG10W/x	1900	3.6	20 dBm	6	60	67	22[4]	SOT433
BFG11W/x	1900	3.6	26 dBm	6	60	67	22[4]	SOT433
BLT82	900	6.0	3.5	6	50	65	32[17]	SOT96 (S08pl)

APPLICATION	SUPPLY VOLTAGE	LOAD POWER	1ST STAGE	2ND STAGE	3RD STAGE
ANALOG	6.0	1.2	BFG540W/x	BLT80	BLT81*
	4.8	1.2	BFG540W/x	BLT70	BLT71
	4.8	1.2	BFG510W/x	BLT7118	–
	3.8	1.2	BFG540W/x	BFG10W/x	BLT61
GSM	6.0	3.5	BFG540W/x	BFG10W/x	BLT82
	4.8	3.0	BFG540W/x	BFG10W/x	
	3.6	3.0	BFG540W/x	BFG10W/x	
PCN/DCS1800	6.0	2.0	BFG540W/x	BFG10W/x	
	4.8	1.6	BFG540W/x	BFG10W/x	
DECT	3.6	0.4	BFG540/x	BFG10x	BFG11/x
			BFG540W/x	BFG10W/x	BFG11W/x

NOTES:

T_0 is the temperature at the soldering pointof the collector tab

1. Preliminary specification
2. Objective specification
3. Junction to soldering point
4. P_{tot} =2W, T_G=131°C
5. P_{tot} =2W, T_G=110°C
6. P_{tot} =2W, T_G=95°C
7. P_{tot} =3.5W, T_G=90°C
8. P_{tot} =2W, T_G=115°C
9. P_{tot} =2W, T_G=115°C
10. P_{tot} =1W, T_G=130°C
11. P_{tot} =1.7W, T_G=90°C
12. P_{tot} =1.9W, T_G=115°1

FIRST GENERATION NPN WIDEBAND TRANSISTORS (f_T up to 3.5 GHz)

f_T / I_C CURVE (see Fig.1)	PACKAGE					
	PLASTIC, LEADED	SURFACE-MOUNT				
	TO-92	SOT23	SOT89	SOT143	SOT223	SOT323
(1)		BFT25				
(2)		BF747 BF547				BF547W
(3)	BF689K BF763	BFS17				BFS17W
(4)		BFS17A		BFG17A		
(5)		BFR53				
(6)			BFQ17		BFG16A	

SECOND GENERATION WIDEBAND TRANSISTORS (f_T up to 6 GHz)

f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE							
		CERAMIC		SURFACE-MOUNT					
		SOT122	SOT173 (note 1)	SOT23	SOT89	SOT143 (note 2)	SOT223	SOT323	SOT343 (note 2)
(7)	NPN			BFR92(A)		BFG92A (/X) (/XR)		BFR92AW	BFG92AW (/X) (/XR)
	PNP			BFT92				BFT92W	
(8)	NPN		BFP91A	BFR93(A)		BFG93A (/X) (/XR)	BFG94	BFR93AW	BFG93AW (/X) (/XR)
(9)	PNP			BFT93				BFT93W	
(10)	NPN		BFP96	BFR106	BFQ19		BFG97		
	PNP				BFQ149		BFG31		
(11)	NPN				BFQ18A		BFG35		
(11)	NPN	BFQ34							
(12)	NPN	BFQ68							
(13)	NPN	BFQ136							

Notes

1. Short-lead version (SOT173X) also available.
2. SOT143 and SOT343 packages are available with alternative pinning.
   European pinning - no type number suffix; USA pinning - suffix /X; Japanese pinning - suffix /XR.
   Brackets around the suffixes (/X) and (/XR) denote pinning options. No brackets means no options,
   (e.g. BFG10W/X: available only with USA pinning).

THIRD GENERATION NPN WIDEBAND TRANSISTORS (f_T up to 12 GHz)

f_T / I_C CURVE (see Fig.1)	PACKAGE						
	CERAMIC		SURFACE-MOUNT				
	SOT172	SOT173 (note 1)	SOT23	SOT143 (note 2)	SOT223	SOT323	SOT343 (note 2)
(14)		BFQ66	BFQ67	BFG67 (/X) (/XR)		BFQ67W	BFG67W (/X) (/XR)
(15)				BFG197 (/X) (/XR)	BFG198		BFG197W (/X) (/XR)
(16)	BFQ135				BFG135		
(17)	BFQ270						

FOURTH GENERATION NPN WIDEBAND TRANSISTORS (f_T up to 10 GHz)

f_T / I_C CURVE (see Fig.1)	PACKAGE							
	CERAMIC	SURFACE-MOUNT						
	SOT172	SOT23	SOT143 (note 2)	SOT223	SOT323	SOT343 (note 2)	SOT353 (note 3)	SOT363 (note 3)
(18)		BFT25A	BFG25A/X		BFS25A	BFG25AW (/X) (/XR)		
(19)		BFR505	BFG505 (/X) (/XR)		BFS505	BFG505W (/X) (/XR)	BFC505 BFE505	BFM505
(20)		BFR520	BFG520 (/X) (/XR)		BFS520	BFG520W (/X) (/XR)	BFC520 BFE520	BFM520
(21)		BFR540	BFG540 (/X) (/XR)	BFG541	BFS540	BFG540W (/X) (/XR)	BFC540 BFE540	BFM540
(22)			BFG590 (/X) (/XR)	BFG591		BFG590W (/X) (/XR)		
(23)	BFQ621		BFG10 (/X)			BFG10W/X		
(24)			BFG11 (/X)			BFG11W/X (note 3)		

Notes

1. Short-lead version (SOT173X) also available.
2. SOT143 and SOT343 packages are available with alternative pinning.
   European pinning - no type number suffix; USA pinning - suffix /X; Japanese pinning - suffix /XR.
   Brackets around the suffixes (/X) and (/XR) denote pinning options. No brackets means no options,
   (e.g. BFG10W/X: available only with USA pinning).
3. Development types.

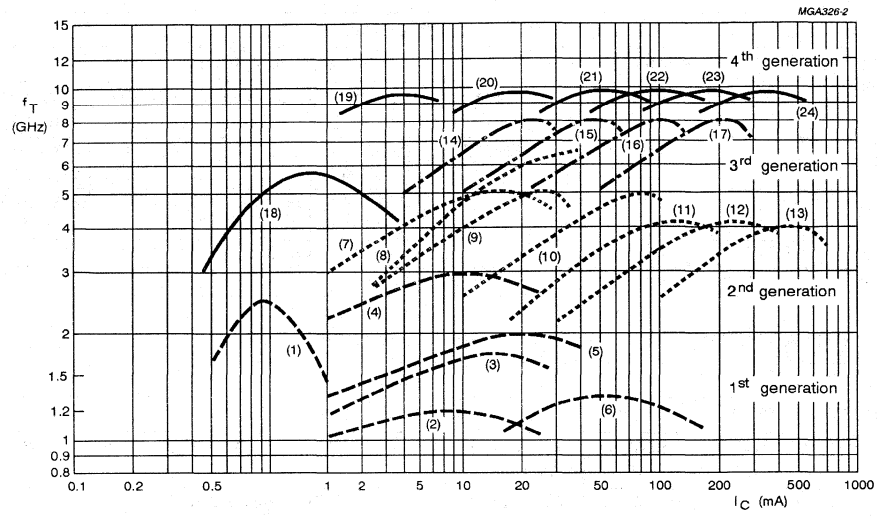


Fig.1 Transition frequency (f_T) characteristics as a function of collector current (I_C) for the four generations of RF bipolar wideband transistors.

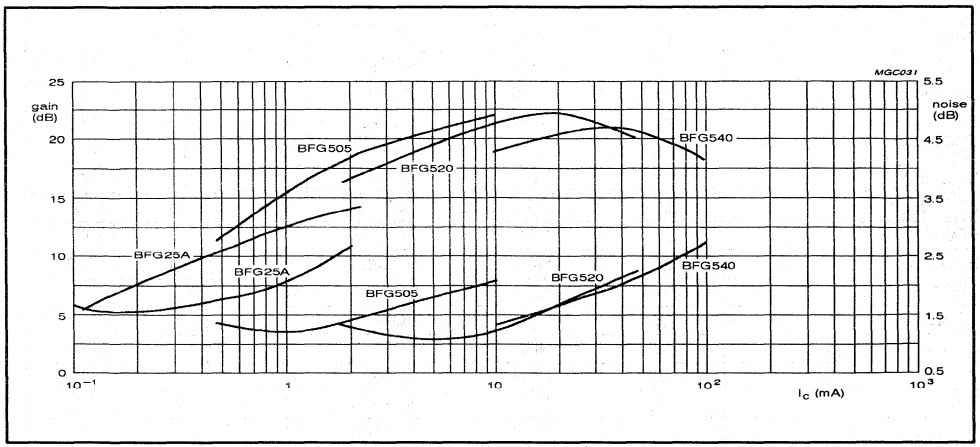


Figure 2. Gain and Noise as a Function of Collector Current

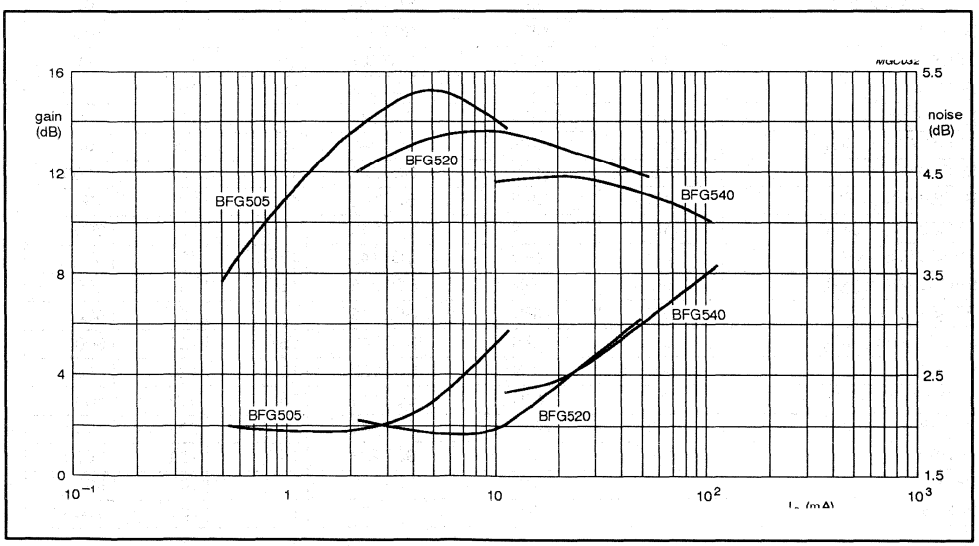


Figure 3. Gain and Noise as a Funcation of Collector Current

PRODUCT DATA

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BF547	(2)	NPN	SOT23	20	50	300
BF547W	(2)	NPN	SOT323	20	50	300
BF689K	(3)	NPN	TO-92	15	25	360
BF747	(2)	NPN	SOT23	20	50	300
BF763	(3)	NPN	TO-92	25	25	360
BFG10(/X)	(23)	NPN	SOT143	8	250	250
BFG10W/X	(23)	NPN	SOT343	10	250	400
BFG11(/X)	(24)	NPN	SOT143	8	500	400
BFG16A	(6)	NPN	SOT223	25	150	1000
BFG17A	(4)	NPN	SOT143	15	50	300
BFG25A/X	(18)	NPN	SOT143	5	6.5	32
BFG25AW(/X)(/XR)	(18)	NPN	SOT343	5	6.5	500
BFG31	(10)	PNP	SOT223	15	100	1000
BFG35	(11)	NPN	SOT223	18	150	1000
BFG67(/X)(/XR)	(14)	NPN	SOT143	10	50	380
BFG67W(/X)(/XR)	(14)	NPN	SOT343	10	50	500
BFG92A(/X)(/XR)	(7)	NPN	SOT143	15	25	400
BFG92AW(/X)(/XR)	(7)	NPN	SOT343	15	25	500
BFG93A(/X)(/XR)	(8)	NPN	SOT143	12	35	300
BFG93AW(/X)(/XR)	(8)	NPN	SOT343	12	35	500
BFG94	(8)	NPN	SOT223	12	60	700
BFG97	(10)	NPN	SOT223	15	100	1000
BFG135	(16)	NPN	SOT223	15	150	1000
BFG197(/X)(/XR)	(15)	NPN	SOT143	10	100	350
BFG197W(/X)(/XR)	(15)	NPN	SOT343	10	100	500
BFG198	(15)	NPN	SOT223	10	100	1000
BFG505(/X)(/XR)	(19)	NPN	SOT143	15[2]	18	150
BFG505W(/X)(/XR)	(19)	NPN	SOT343	15[2]	18	500
BFG520(/X)(/XR)	(20)	NPN	SOT143	15[2]	70	300
BFG520W(/X)(/XR)	(20)	NPN	SOT343	15[2]	70	500
BFG540(/X)(/XR)	(21)	NPN	SOT143	15[2]	120	500
BFG540W(/X)(/XR)	(21)	NPN	SOT343	15[2]	120	500
BFG541	(21)	NPN	SOT223	15[2]	120	650
BFG590(/X)(/XR)	(22)	NPN	SOT143	15	200	400
BFG590W(/X)(/XR)	(22)	NPN	SOT343	15	200	500
BFG591	(22)	NPN	SOT223	15	200	2000
BFP91A	(8)	NPN	SOT173	12	50	600
BFP96	(10)	NPN	SOT173	15	100	1000

PRODUCT DATA

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BF547	1.2		20	100								
BF547W	1.2		20	100								
BF689K	1.8	4		100	3	16[4]	200					
BF747	1.2		20	100								
BF763	1.8	5		800								
BFG10(/X)			7[4]	1900								
BFG10W/X			10[4]	900		7[4]	1900					
BFG11(/X)			5[4]	1900								
BFG16A	1.5		10	500								
BFG17A	2.8	2.5	15	800								
BFG25A/X	5	1.8	18	1000								
BFG25AW(/X)(/XR)	5	2	16	1000								
BFG31	5		16	500		12	800	550			70	10
BFG35	4		15	500		11	800	750			100	10
BFG67(/X)(/XR)	8	1.7	17	1000	2.5	10	2000					
BFG67W(/X)(/XR)	7.5	1.7	15.5	1000	2.2	10	2000					
BFG92A(/X)(/XR)	5	2	16	1000	3	11	2000					
BFG92AW(/X)(/XR)	6	2.1	15.5	1000	3	10	2000					
BFG93A(/X)(/XR)	6	1.7	16	1000	2.3	10	2000					
BFG93AW(/X)(/XR)	7	2	14.5	1000	3	9	2000					
BFG94	6	2.7		500	3	13.5	1000	500	21.5	34	45	10
BFG97	5.5	2	16	500		12	800	700			70	10
BFG135	7		16	500		12	800	850			100	10
BFG197(/X)(/XR)	7.5	2.3	16	1000		10	2000					
BFG197W(/X)(/XR)	7.5	2.4	14	1000	3.5	9	2000	700			30	8
BFG198	8		18	500		15	800	700			70	8
BFG505(/X)(/XR)	9	1.6	20	900	1.9	13	2000		4	10	5	6
BFG505W(/X)(/XR)	9	1.6	19	900	1.9	12	2000		4	10	5	6
BFG520(/X)(/XR)	9	1.6	19	900	1.9	13	2000	275	17	26	20	6
BFG520W(/X)(/XR)	9	1.6	17	900	1.85	11	2000	275	17	26	20	6
BFG540(/X)(/XR)	9	1.9	18	900	2.1	11	2000	500	21	34	40	8
BFG540W(/X)(/XR)	9	1.9	16	900	2.1	10	2000	500	21	34	40	8
BFG541	9	1.9	15	900	2.1	9	2000	500	21	34	40	8
BFG590(/X)(/XR)	5		13	900		7.5	2000					
BFG590W(/X)(/XR)	5		13	900		7.5	2000		21		80	5
BFG591	7		13	900		7.5	2000					
BFP91A	6		22.5	500	2.3	18.5	800					
BFP96	5		19	500	3.7	15	800					

PRODUCT DATA

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BFQ17	(6)	NPN	SOT89	25	150	1000
BFQ18A	(11)	NPN	SOT89	18	150	1000
BFQ19	(10)	NPN	SOT89	15	100	1000
BFQ34	(11)	NPN	SOT122	18	150	2700
BFQ66	(14)	NPN	SOT173	10	50	350
BFQ67	(14)	NPN	SOT23	10	50	300
BFQ67W	(14)	NPN	SOT323	10	50	300
BFQ68	(12)	NPN	SOT122	18	300	4500
BFQ135	(16)	NPN	SOT172	19	150	2700
BFQ136	(13)	NPN	SOT122	18	600	9000
BFQ149	(10)	PNP	SOT89	15	100	1000
BFQ270	(17)	NPN	SOT172	19	500	10000
BFQ540	(21)	NPN	SOT89	15[3]	120	950
BFQ621	(23)	NPN	SOT172	16	150	800
BFR53	(5)	NPN	SOT23	10	50	250
BFR92	(7)	NPN	SOT23	15	25	300
BFR92A	(7)	NPN	SOT23	15	25	300
BFR92AW	(7)	NPN	SOT323	15	25	300
BFR93	(8)	NPN	SOT23	12	35	300
BFR93A	(8)	NPN	SOT23	12	35	300
BFR93AW	(8)	NPN	SOT323	12	35	300
BFR94A	(8)	NPN	SOT122	25	150	3500
BFR106	(10)	NPN	SOT23	15	100	500
BFR505	(19)	NPN	SOT23	15[2]	18	150
BFR520	(20)	NPN	SOT23	15[2]	70	300
BFR540	(21)	NPN	SOT23	15[2]	120	480
BFS17	(3)	NPN	SOT23	15	25	300
BFS17A	(4)	NPN	SOT23	15	25	300
BFS17W	(3)	NPN	SOT323	15	50	300
BFS25A	(18)	NPN	SOT323	5	6.5	32
BFS505	(19)	NPN	SOT323	15[2]	18	150
BFS520	(20)	NPN	SOT323	15[2]	70	300
BFS540	(21)	NPN	SOT323	15[2]	120	500
BFT25	(1)	NPN	SOT23	5	6.5	30
BFT25A	(18)	NPN	SOT23	5	6.5	32
BFT92	(7)	PNP	SOT23	15	25	300
BFT92W	(7)	PNP	SOT323	15	35	300
BFT93	(9)	PNP	SOT23	12	35	300

PRODUCT DATA

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BFQ17	1.5		16	200		6.5	800					
BFQ18A	4											
BFQ19	5.5	3.3	11.5	500		7.5	800					
BFQ34	4	8	16.3	500				1200	26	45	120	15
BFQ66	8	2.7	11.5	2000								
BFQ67	8	1.7	14	1000	8	2.7	2000					
BFQ67W	8	2	13	1000	2.7	8	2000					
BFQ68	4		13	800				1600	28	47	240	15
BFQ135	6.5		17	500		13.5	800	1200			120	18
BFQ136	4		12.5	800				2500			500	15
BFQ149	5	3.75	12	500								
BFQ270	6		16	500		10	1000	1600			240	18
BFQ540	9	1.3		900				450			40	8
BFQ621	7		18.5	500				1200			120	18
BFR53	2	5		500		10.5	800					
BFR92	5	2.4	18	500				150			14	10
BFR92A	5	2.1	14	1000	3	8	2000	150			14	10
BFR92AW	5	2	14	1000	3	8	2000					
BFR93	6	1.9	16.5	500								
BFR93A	6	1.9	13	1000	3	7	2000	425			30	8
BFR93AW	6	1.5	13	1000	2.1	8	2000					
BFR94A	3.5	8		200								
BFR106	5	3.5	11.5	800				350			50	9
BFR505	9	1.6	17	900	1.9	10	2000		4	10	5	6
BFR520	9	1.6	15	900	1.9	9	2000		17	26	20	6
BFR540	9	1.9	14	900	2.1	7	2000	550	21	34	40	8
BFS17	1	4.5		500								
BFS17A	2.8	2.5	13.5	800				150			14	10
BFS17W	1.6	4.5		500								
BFS25A	5	1.8	13	1000								
BFS505	9	1.6	17	900	1.9	10	2000		4	10	5	6
BFS520	9	1.6	15	900	1.9	9	2000		17	26	20	6
BFS540	9	1.9	14	900	2.1	8	2000		21	34	40	8
BFT25	2.3	3.8	18	500		12	800					
BFT25A	5	1.8	15	1000								
BFT92	5	2.5	18	500				150			14	10
BFT92W	5	2.5	17	500	3	11	1000					
BFT93	5	2.4	16.5	500				300			30	5

PRODUCT DATA

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BFT93W	(9)	PNP	SOT323	12	50	300
MPSH10		NPN	TO-92	25	40	1000
PMBT3640		PNP	SOT23	12	80	350
PMBTH10		NPN	SOT23	25	40	400
PMBTH81		PNP	SOT23	20	40	400

DEVELOPMENT TYPES

TYPE NUMBER	POLARITY	PACKAGE	RATINGS		
			V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BFC505	NPN	SOT353	15[2]	18	500
BFC520	NPN	SOT353	15[2]	70	1000
BFC540	NPN	SOT353	15[2]	120	1000
BFE505	NPN	SOT353	15[2]	18	500
BFE520	NPN	SOT353	15[2]	70	1000
BFE540	NPN	SOT353	15[2]	120	1000
BFG11W/X	NPN	SOT343	8	500	630
BFM505	NPN	SOT363	15[2]	18	500
BFM520	NPN	SOT363	15[2]	70	1000
BFM540	NPN	SOT363	15[2]	120	1000

Notes

1. Typical values at d_{im} = −60 dB, measured according to DIN45004B, para. 6.3: 3-tone test.
2. V_{CES}.
3. Minimum value.
4. Power gain G_p.

PRODUCT DATA

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BFT93W	5	2.4	15.5	500	3	10	1000					
MPSH10	0.65[3]											
PMBT3640	0.5[3]											
PMBTH10	0.65[3]											
PMBTH81	0.6[3]											

DEVELOPMENT TYPES

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BFC505	6	1.6		900	2.4		2000					
BFC520	7	1.3		900	2.4		2000					
BFC540	9	1.6		900	2.9		2000					
BFE505	9	1.2		900	1.9		2000					
BFE520	9	1.1		900	1.9		2000					
BFE540	9	1.3		900	1.9		2000					
BFG11W/X			6[4]	1900								
BFM505	9	1.2	17	900	1.9	10	2000					
BFM520	9	1.6	15	900	1.9	9	2000					
BFM540	9	1.9	14	900	2.1	7	2000					

Notes

1. Typical values at d_{im} = −60 dB, measured according to DIN45004B, para. 6.3: 3-tone test.
2. V_{CES}.
3. Minimum value.
4. Power gain G_p.

LINE-UPS

Analog cellular (AMPS, (E)TACS, NMT) 900 MHz

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
Bipolar					
1	BFG540/X	BLT80	BLT81	1.2	6.0
1	BFG540/X	BLT70	BLT71	1.2	4.8
1	BFG520W/X	BFG10W/X	BLT61	1.2	3.6

Digital cellular (GSM) 900 MHz

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
Bipolar					
1	BFG540W/X	BFG10W/X		3.0 pulsed	4.8
1	BFG540W/X	BFG10W/X	BLT82	3.5 pulsed	6.0

Portable transmitters (860 MHz to 960 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
Bipolar					
1	BFG540	BLT80	BLT81	1.2	6.0
15	BFG91A	BLT80	BLT92/SL	3.0	7.5

Digital cellular (GSM) 1800 MHz

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
Bipolar					
4	BFG540W/X	BFG10W/X		2.0	6.0

RF wideband transmitters for pager front-end (see Fig.2)

FUNCTION	TYPE NUMBER [1]	REMARKS
RF amplifier	BFT25A	lowest current (0.2 mA)
	BFR505	higher gain, lower noise (1 mA)
	BFC505	higher gain, lower noise, high isolation (0.3 mA)
Oscillator, mixer or buffer	BFR92A	choice of the transistor is determined by the available current and the required performance
	BFQ67	
	BFT25A	
	BFR505	

Note

1. Equivalent types are available in SOT23, SOT143, SOT323, or SOT343 packages.

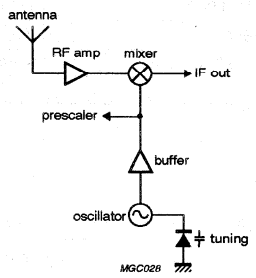


Fig.2 Typical front-end section for pagers.

RF wideband transistors for the receiver section in cordless/cellular phones (see Fig.3)

FUNCTION	TYPE NUMBER	SYSTEM FREQUENCY (MHz)	FEATURES
LNA	BFC505	1900	high isolation gain, low noise current
	BFR505	900; 1900	good performance at low current (1 mA)
	BFR520	900; 1900	higher gain, lower noise (10 mA)
Mixer	BFR93A	900	low cost, acceptable performance
	BFG505	900; 1900	good performance, low current
	BFG520	900; 1900	higher power to IF (10 mA)
	BFE505	900; 1900	balanced mixer in a single SOT353 package
Buffer and VCO	BFR92A	900	excellent VCO, good buffer, low-cost
	BFR93A	900	excellent VCO, good buffer, low-cost
	BFQ67	900	third generation, good performance
	BFR 505	900; 1900	good VCO, high-gain buffer, low current
	BFR520	900; 1900	good VCO, higher output power
	BFG505	1900	buffer and VCO in a single SOT353 package
IF	BFS17A	40 to 100	any first or second generation transistor

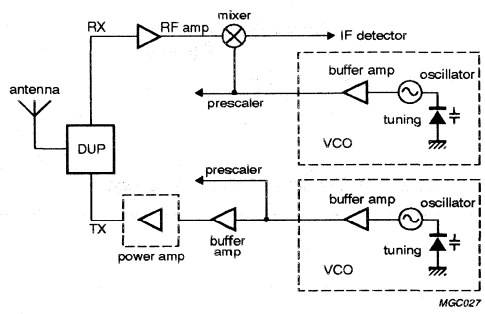


Fig.3 Typical RF section for cordless and cellular phones.

RF wideband transistors for the receiver section in cordless/cellular phones (see Fig.3)

FUNCTION	SYSTEM FREQUENCY (MHz)	SOT23	SOT323	SOT143 (1)	SOT343 (1)	SOT353 (2)	SOT363 (2)
LNA	900; 1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505
	900; 1900	BFR 520	BFS520	BFG520	BFG520W	BFC520	BFM520
Mixer	900	BFR93A	BFR93AW	BFG93A	BFG93AW		
	900; 1900	BFR505	BFS505	BFG505	BFG505W	BFE505	BFM505
	900; 1900	BFR520	BFS520	BFG520	BFG520W	BFE520	BFM520
Buffer and VCO	900	BFR92A	BFR92AW	BFG92A	BFG92AW		
	900	BFR93A	BFR93AW	BFG93A	BFG93AW		
	900	BFQ67	BFQ67W	BFG67	BFG67W		
	900; 1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505
	900; 1900	BFR520	BFS520	BFG520	BFG520W	BFC520	BFM520
IF	40 to 100	BF547	BF547W				
		BFS17	BFS17W	BFG17A			
		BFR92A	BFR92AW	BFG92A	BFG92AW		

Note

1. Also available in /X and /XR versions.
2. Under development.

RF wideband transistors for the power amplifier section in cordless/cellular phones (see Fig.4)

SYSTEM	SUPPLY VOLTAGE (V)	P_{out} (mW)	SOT143	SOT343
CT1, CT1+, CT2, CT2+ CT3	3.3	driver for PA2	BFG67	BFG67W
			BFG505	BFG505W
			BFG520	BFG520W
		15	BFG67	BFG67W
		20	BFG520	BFG520W
		40	BFG540	BFG540W
DECT, PHP	3.3	400	BFG540/X	BFG540W/X
			BFG10/X	BFG10W/X
			BFG11/X	BFG11W/X (1)

Note

1. Under development.

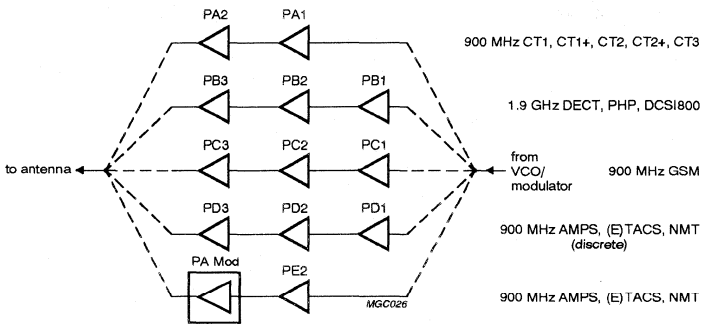


Fig.4 Typical power amplifier section for cordless and cellular phones.

MOSFETS Selector Guide

WIRELESS COMMUNICATIONS

TYPE	DESCRIPTION	CHANNEL	GATE(S)	SUPPLY VOLTAGE (V_{DS})	PACKAGE
PHN205	Low ohmic battery switch	N&N	Dual	25	S08 (SOT96)
PHP212	Low ohmic battery switch	P&P	Dual	25	S08 (SOT96)
PHC20512	Low ohmic battery switch	N&P	Dual	25	S08 (SOT96)
PHN103	Low ohmic battery switch	N	Single	30	S08 (SOT96)
PHP109	Low ohmic battery switch	P	Single	30	S08 (SOT96)
BSP030	Low ohmic battery switch	N	Single	30	S08 (SOT96)
BSP090	Low ohmic battery switch	P	Single	30	S08 (SOT96)

TYPE	DESCRIPTION	CHANNEL	GATE(S)	SUPPLY VOLTAGE (V_{DS})	PACKAGE
BF904	Mixer/oscillator	N&P	Dual	3 to 7	SOT143
BF904WR	Mixer/oscillator	N&P	Dual	3 to 7	SOT343
BF909	Mixer/oscillator	N&P	Dual	3 to 7	SOT143
BF909WR	Mixer/oscillator	N&P	Dual	3 to 7	SOT343

TYPE	DESCRIPTION	CHANNEL	GATE(S)	SUPPLY VOLTAGE (V_{DS})	PACKAGE
BSN254	Line interrupter/ground switch	N	Single	250	SOT54
BSN304	Line interrupter/ground switch	N	Single	300	SOT54
BSP126	Line interrupter/ground switch	N	Single	250	SOT223
BSP130	Line interrupter/ground switch	N	Single	300	SOT223
VN2406L	Line interrupter/ground switch	N	Single	240	SOT54
BSP92	Line interrupter/ground switch	P	Single	240	SOT54
BSP225	Line interrupter/ground switch	P	Single	250	SOT223
BSP224	Line interrupter/ground switch	P	Single	250	SOT54
BSP304	Line interrupter/ground switch	P	Single	250	SOT223

Section 16
Package Information

Wireless Communications

Soldering 16–3

Ceramic dual in-line package

0580A 8-Pin (300 mils wide) ceramic dual in-line (F) package 16–5

0582B 16-Pin (300 mils wide) ceramic dual in-line (F) package 16–6

Plastic dual in-line package

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1 16–7

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1 16–8

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4 16–9

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1 16–10

DIP24: plastic dual in-line package; 24 leads (400 mil) SOT248-1 16–11

DIP24: plastic dual in-line package; 24 leads (600 mil) SOT101-1 16–12

DIP28: plastic dual in–line package; 28 leads (600 mil) SOT117–1 16–13

DIP40: plastic dual in–line package; 40 leads (600 mil) SOT129–1 16–14

Plastic small outline package SO (Small Outline) and SOL (Small Outline Large)

SO8: plastic small outline package; 8 leads; body width 3.9mm SOT96-1 16–15

SO14: plastic small outline package; 14 leads; body width 3.9 mm SOT108-1 16–16

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1 16–17

SOL16: plastic small outline package; 16 leads; body width 7.5 mm SOT162-1 16–18

SOL20: plastic small outline package; 20 leads; body width 7.5 mm SOT163-1 16–19

SOL24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1 16–20

SOL28: plastic small outline package large; 28 leads; body width 7.5 mm SOT136-1 16–21

Plastic small outline package (SSOP), plastic thin shrink small outline (TSSOP), and very small outline (VSO)

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm SOT369-1 16–22

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm SOT266–1 16–23

SSOP24 plastic shrink small outline package; 24 leads; body width 5.3 mm SOT340–1 16–24

TSSOP24 plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355–1 16–25

VSO56 plastic very small outline package; 56 leads SOT190–1 16–26

Quad flat package(QFP)

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307–2 16–27

QFP64: plastic quad flat package; 64 leads; body 14 x 20 x 2.8 mm SOT319–2 16–28

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm SOT317-2 16–29

Low profile quad flat package (LQFP)

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm SOT401-1 16–30

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm SOT358-1 16–31

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm SOT313-2 16–32

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.75 mm SOT314–2 16–33

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm SOT315–2 16–34

LQFP100: plastic low profile quad flat package 100 leads; body 14 x 14 x 1.4 mm SOT407–1 16–35

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 14 x 1.4 mm SOT420-1 16–36

Thin quad flat package (TQFP)

TQFP32: plastic thin quad flat package; 32 leads; body 7 x 7 x 1.4mm SOT358–2 16–37

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when though-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1. Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260°C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24V) to the lead(s) of the package, below the seating plane or not more than 2mm above it. If the temperature of the soldering iron bit is less than 300°C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400°C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2. Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be indluenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapor phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Manual"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250°C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45°C.

Table 3. Suitability of surface mounted packages for various soldering methods

Rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder theives at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at and angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, only consider wave soldering for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4mm**, e.g., SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2 and SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260°C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150°C within 6 seconds. Typical dwell time is 4 seconds at 250°C.

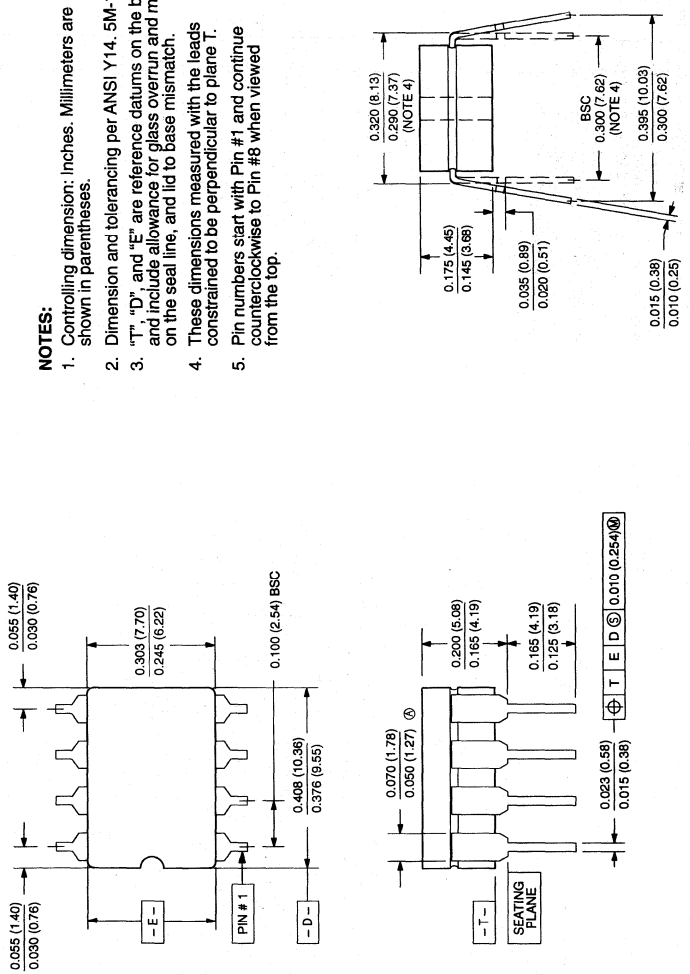
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320°C.

Package outlines

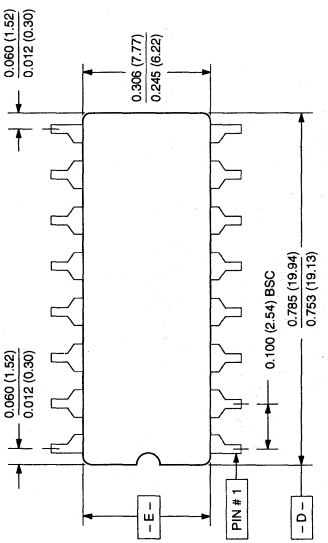
0580A 8-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE

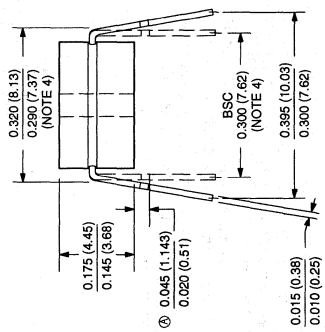


853–0580A 006688

Package outlines

0582B 16-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE





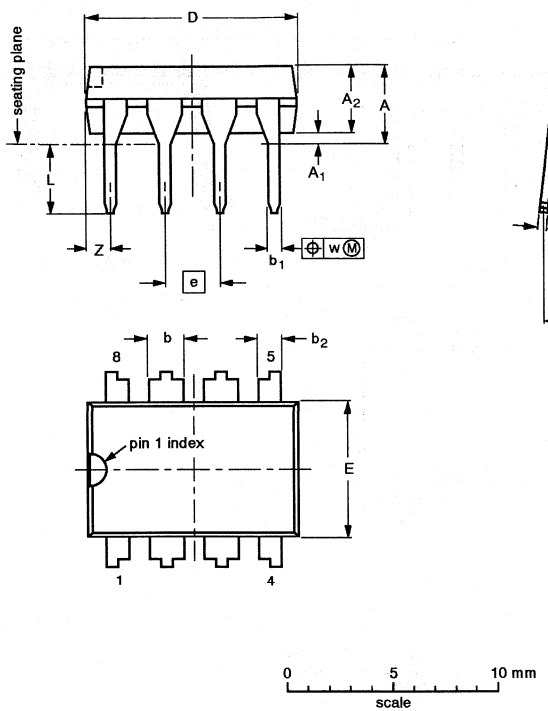
NOTES:

1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14. 5M-1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from the top.

853-0582B 06688

Package outlines

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

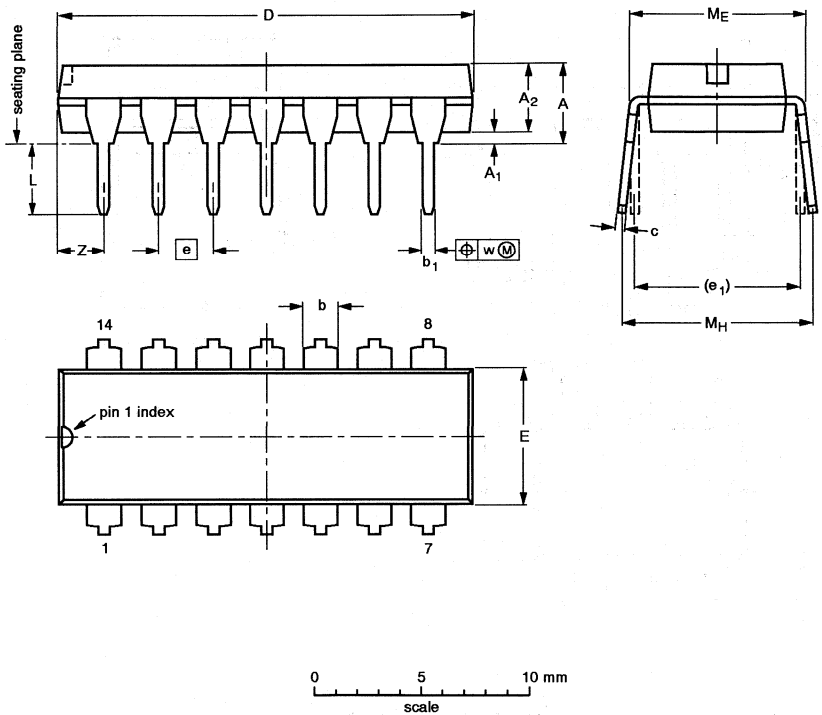
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

Package outlines

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

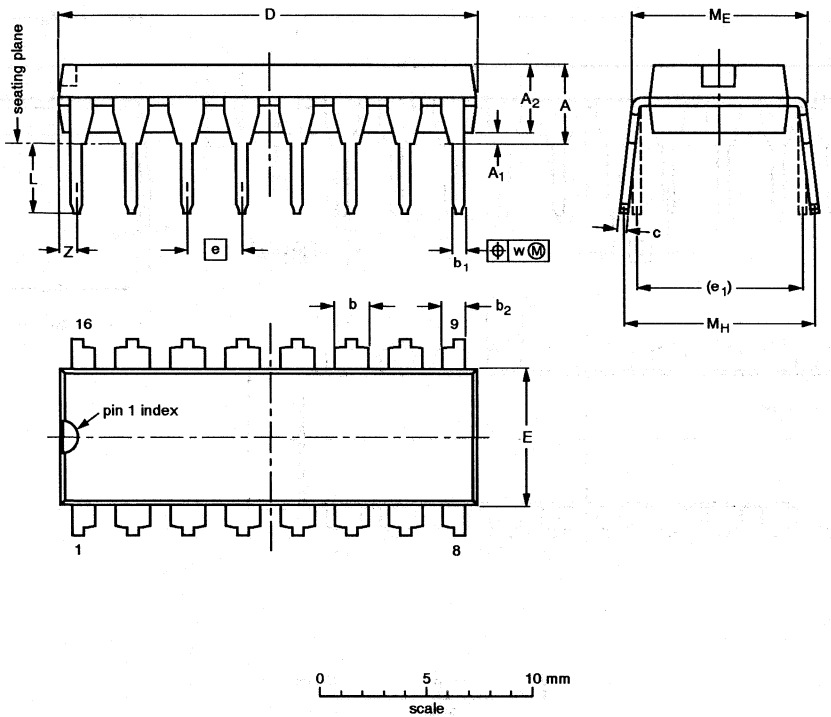
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

Package outlines

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

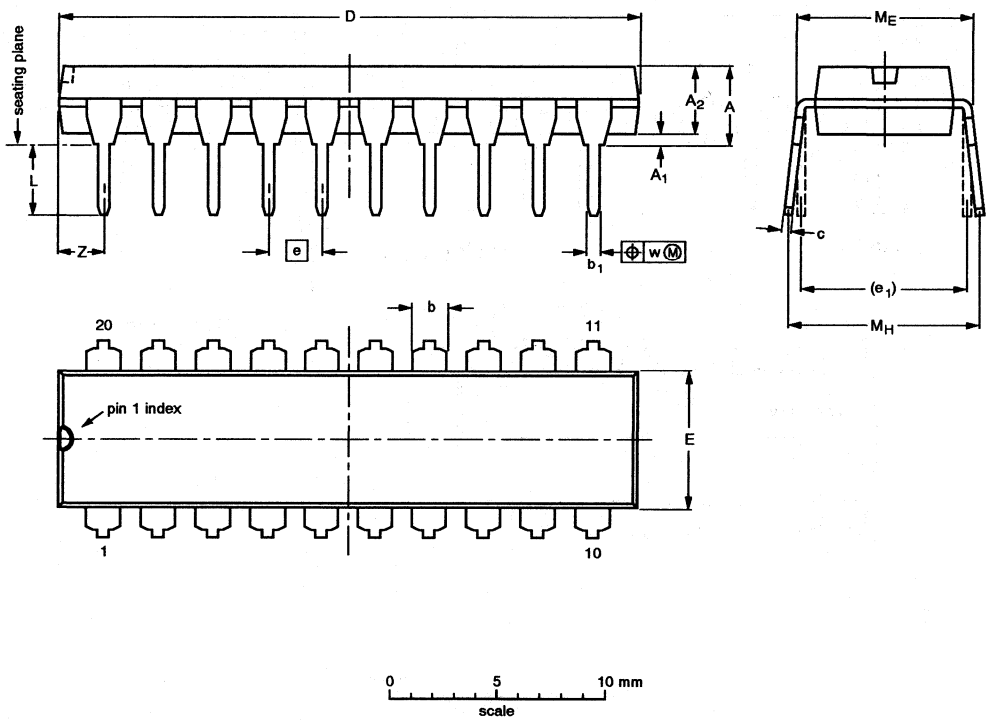
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

Package outlines

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

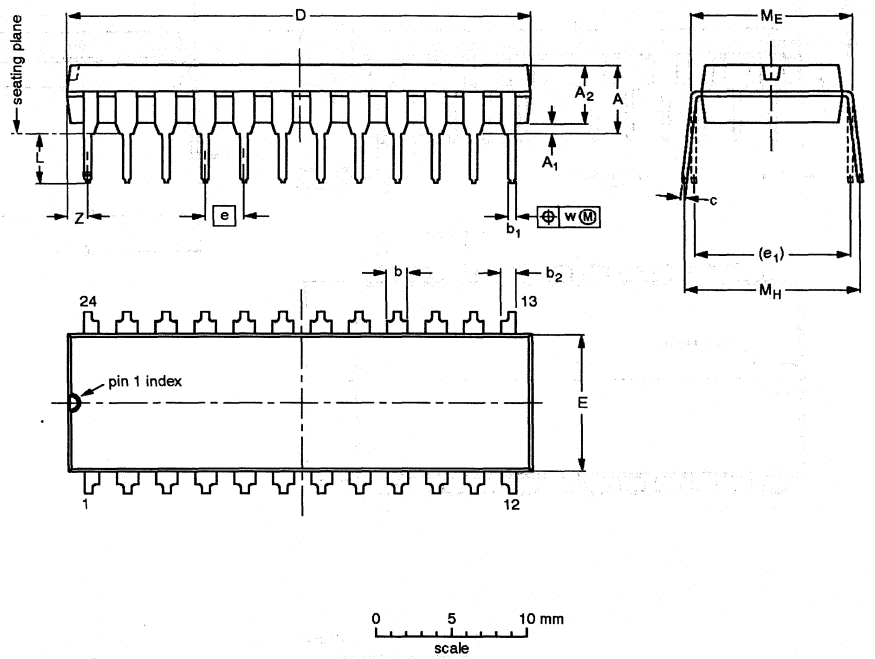
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

Package outlines

DIP24: plastic dual in-line package; 24 leads (400 mil) SOT248-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.83	0.51	3.94	1.63 1.14	0.56 0.43	1.07 0.86	0.36 0.25	30.61 30.23	9.40 8.76	2.54	10.16	3.51 3.05	10.72 10.16	12.57 10.16	0.25	1.40
inches	0.190	0.020	0.155	0.064 0.045	0.022 0.017	0.042 0.034	0.014 0.010	1.205 1.190	0.370 0.345	0.100	0.400	0.138 0.120	0.422 0.400	0.495 0.400	0.01	0.055

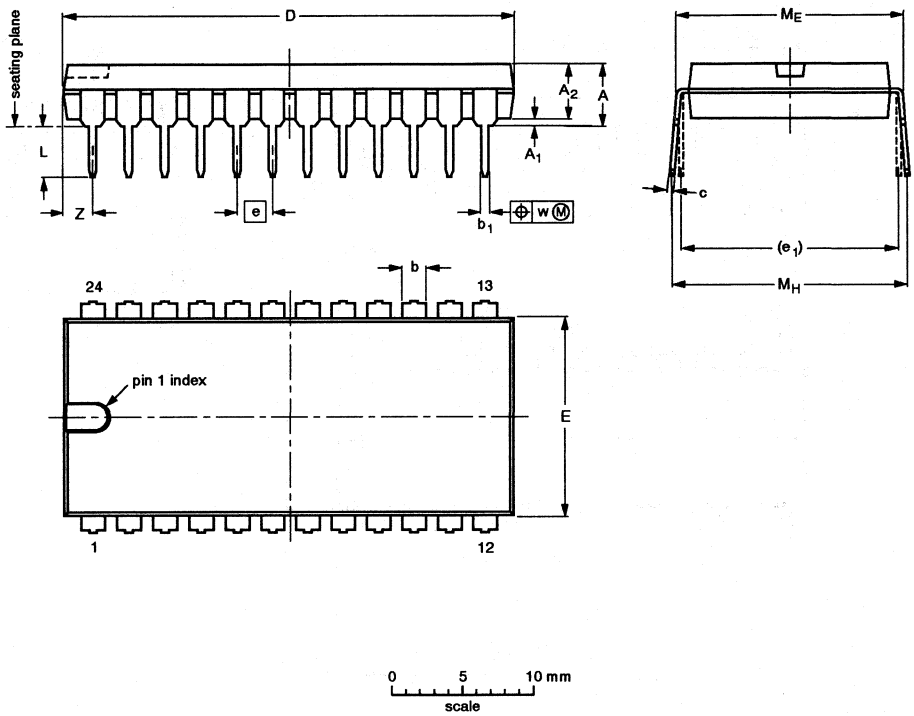
Note

1. Plastic or metal protrusions of 0.01 inch maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT248-1						95-03-11

Package outlines

DIP24: plastic dual in-line package; 24 leads (600 mil) SOT101-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

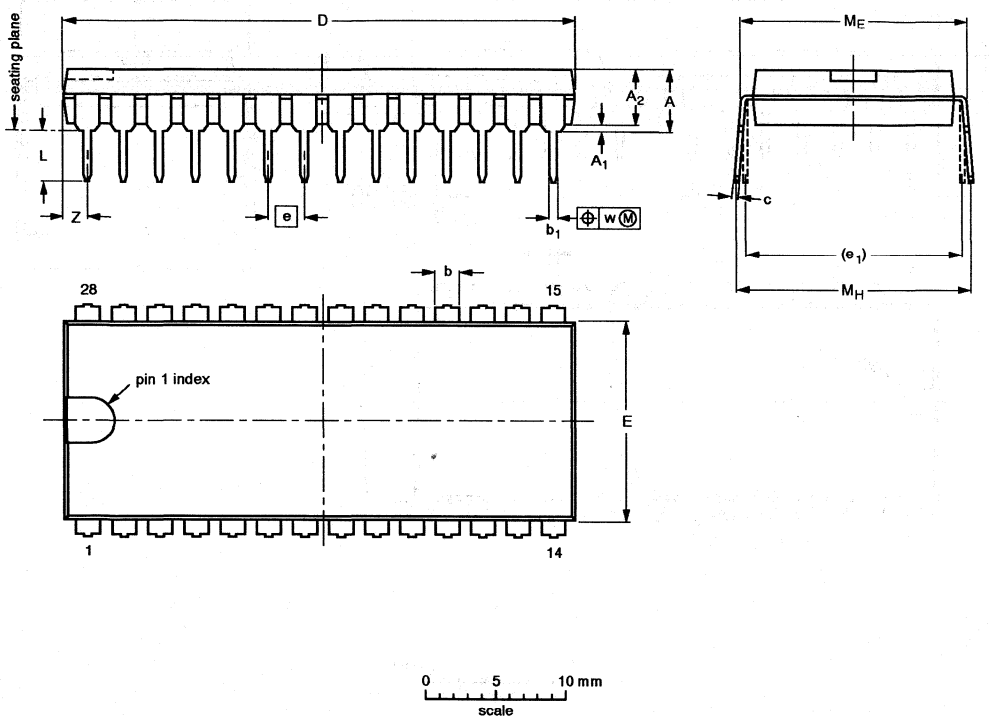
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

Package outlines

DIP28: plastic dual in-line package; 28 leads (600 mil) SOT117-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

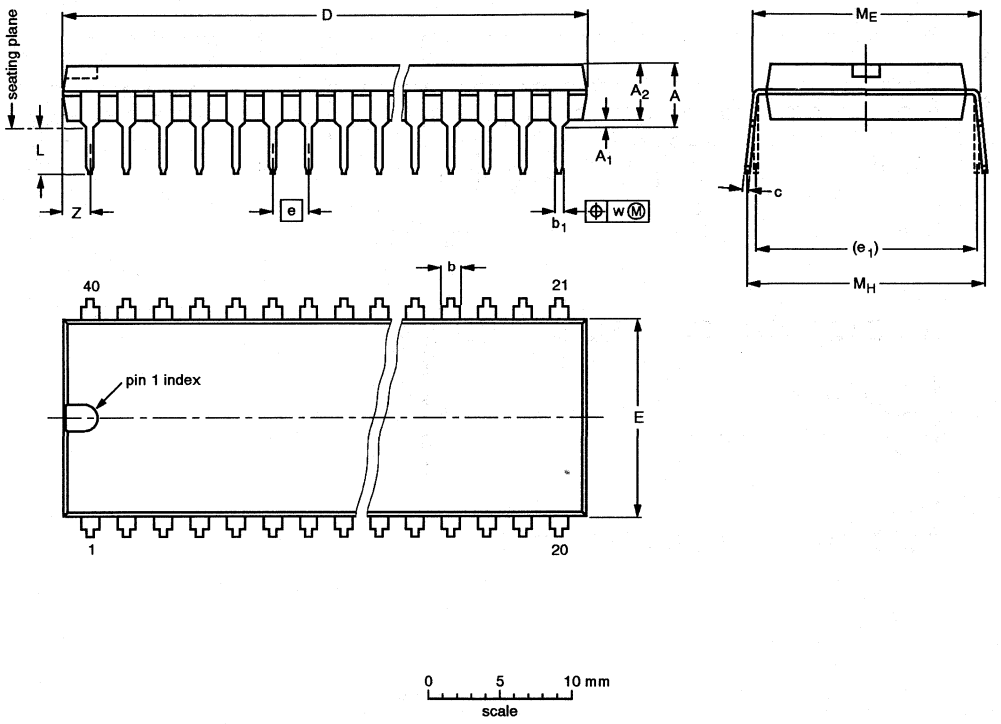
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

Package outlines

DIP40: plastic dual in-line package; 40 leads (600 mil) SOT129-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

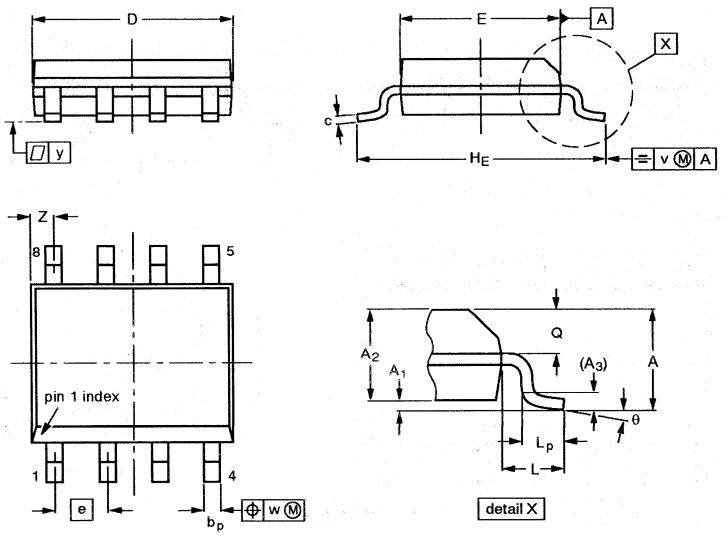
Note

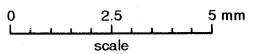
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

Package outlines

SO8: plastic small outline package; 8 leads; body width 3.9mm — SOT96-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

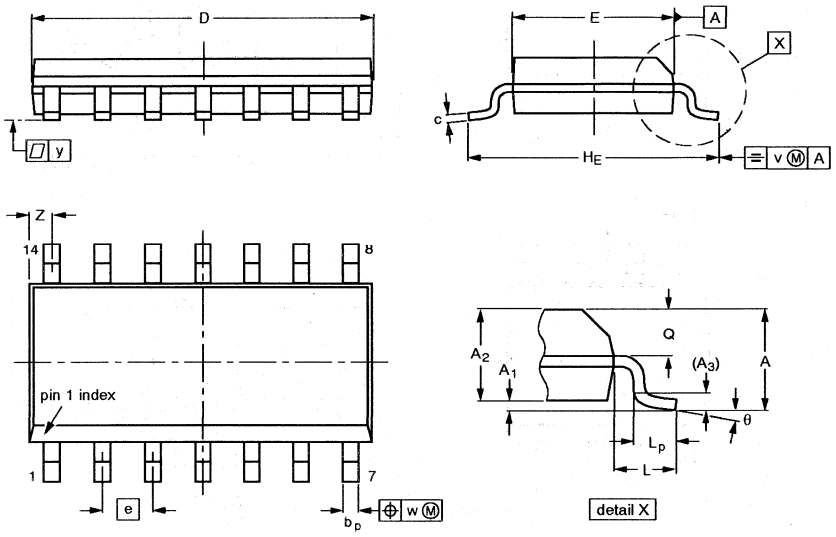
Notes

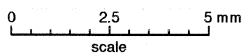
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

Package outlines

SO14: plastic small outline package; 14 leads; body width 3.9 mm — SOT108-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

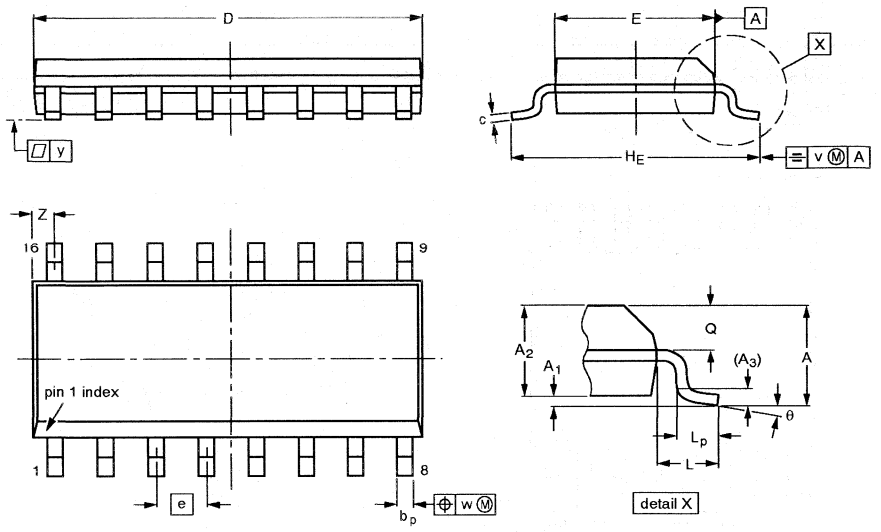
Note

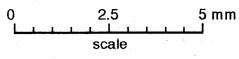
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~91-08-13~~ 95-01-23

Package outlines

SO16: plastic small outline package; 16 leads; body width 3.9 mm — SOT109-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

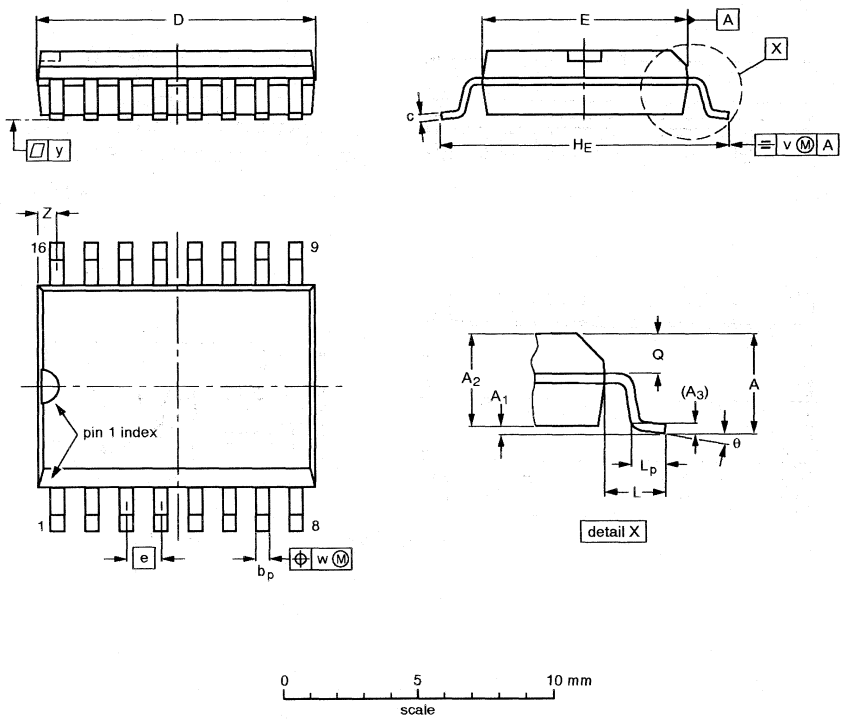
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

Package outlines

SO16: plastic small outline package; 16 leads; body width 7.5 mm — SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

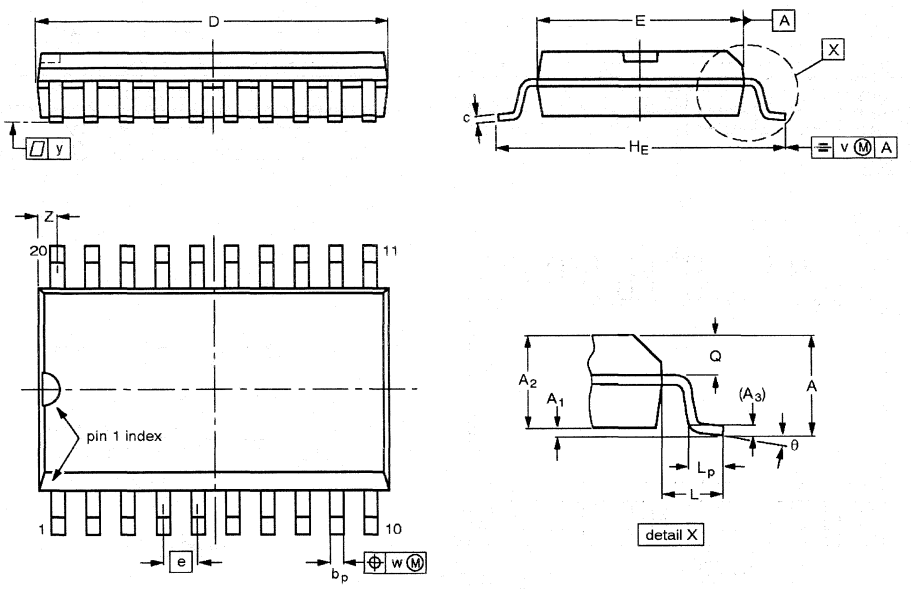
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

Package outlines

SO20: plastic small outline package; 20 leads; body width 7.5 mm — SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

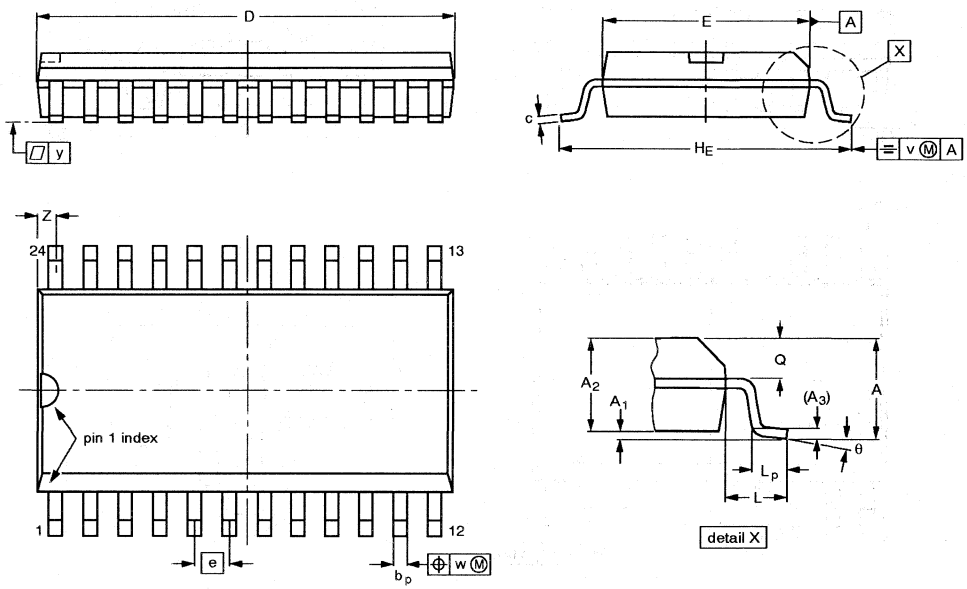
Note

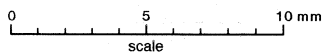
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

Package outlines

SO24: plastic small outline package; 24 leads; body width 7.5 mm — SOT137-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

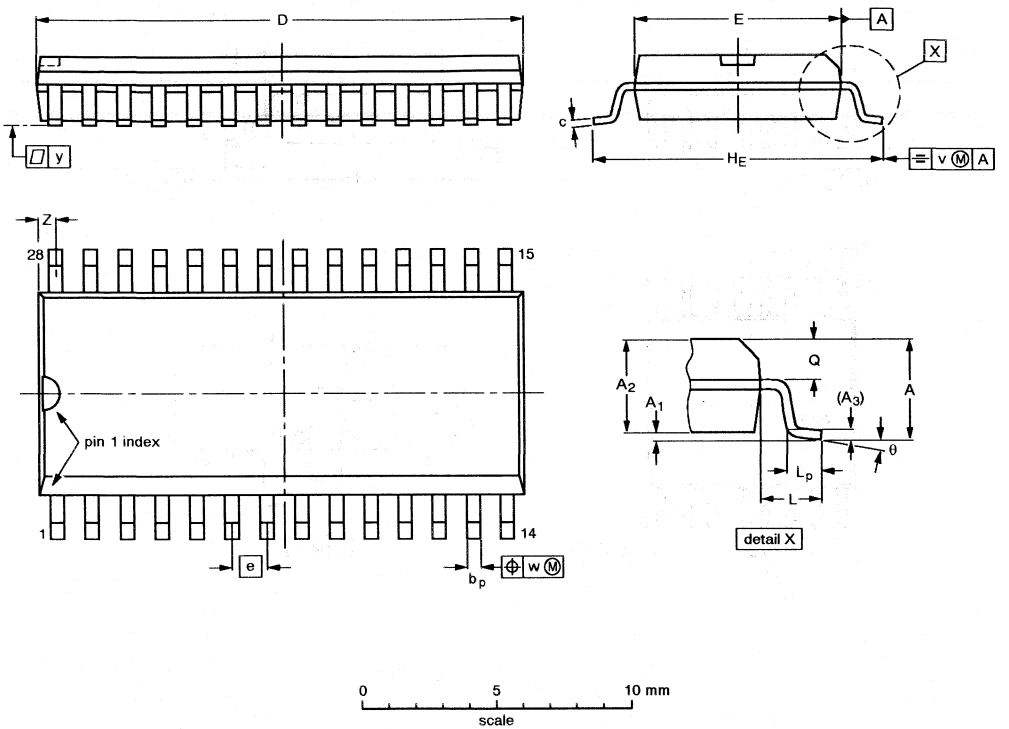
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

Package outlines

SO28: plastic small outline package; 28 leads; body width 7.5mm — SOT136-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

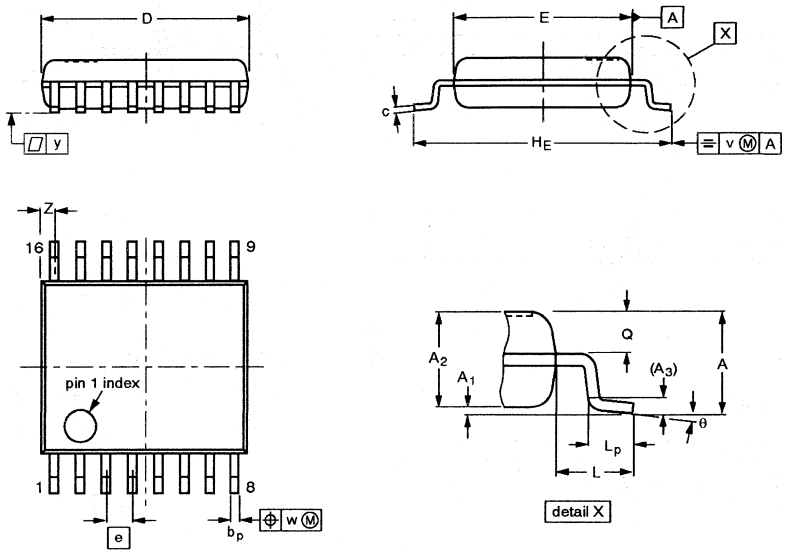
Note

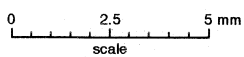
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

Package outlines

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm — SOT369-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

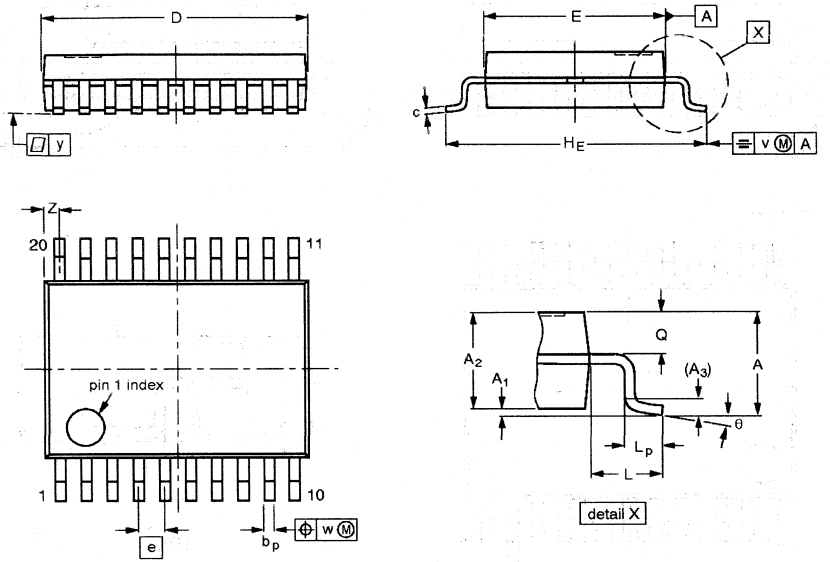
Note

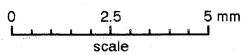
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1						~~94-04-20~~ 95-02-04

Package outlines

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm — SOT266-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

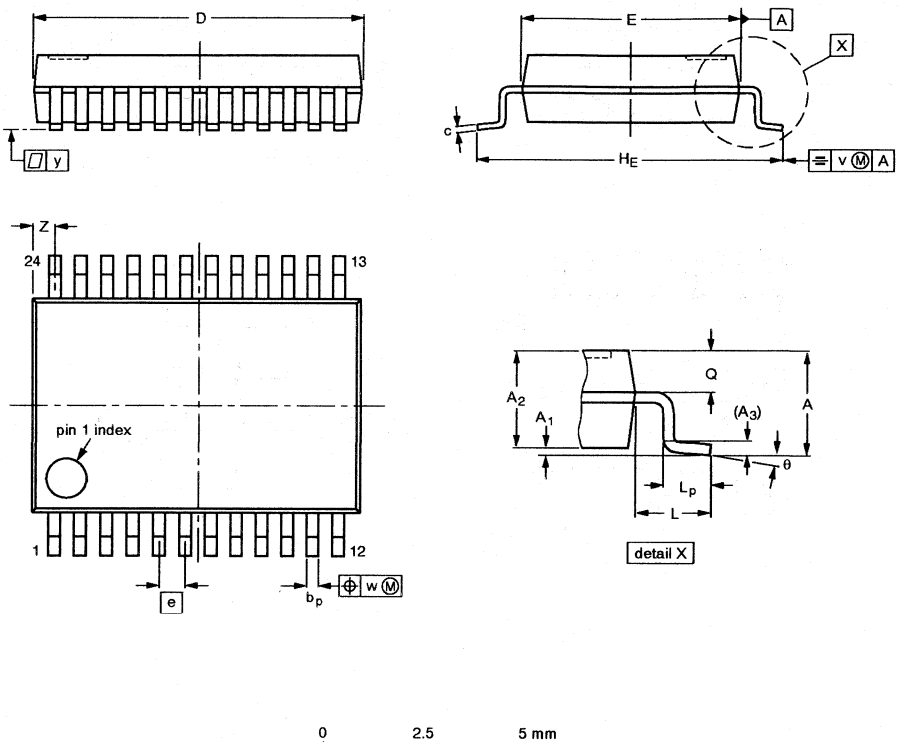
Note

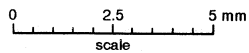
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

Package outlines

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm — SOT340-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

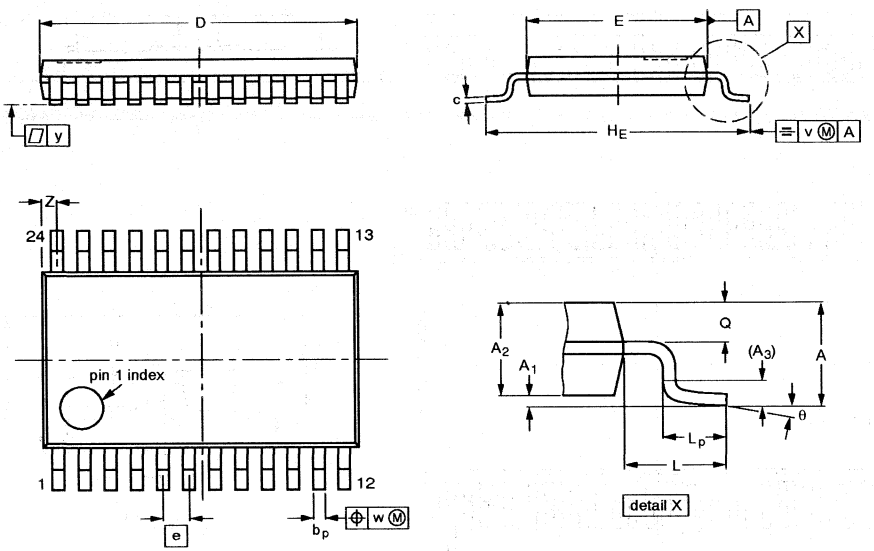
Note

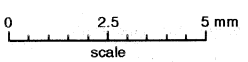
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

Package outlines

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm — SOT355-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

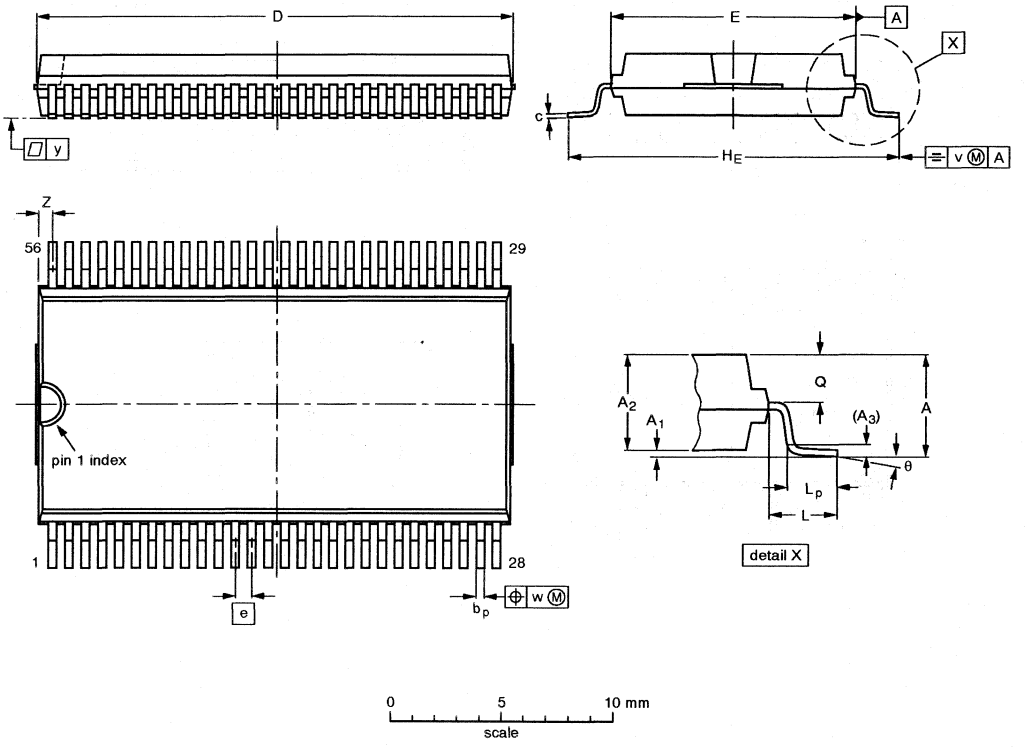
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

Package outlines

VSO56: plastic very small outline package; 56 leads — SOT190-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7° 0°
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.03	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

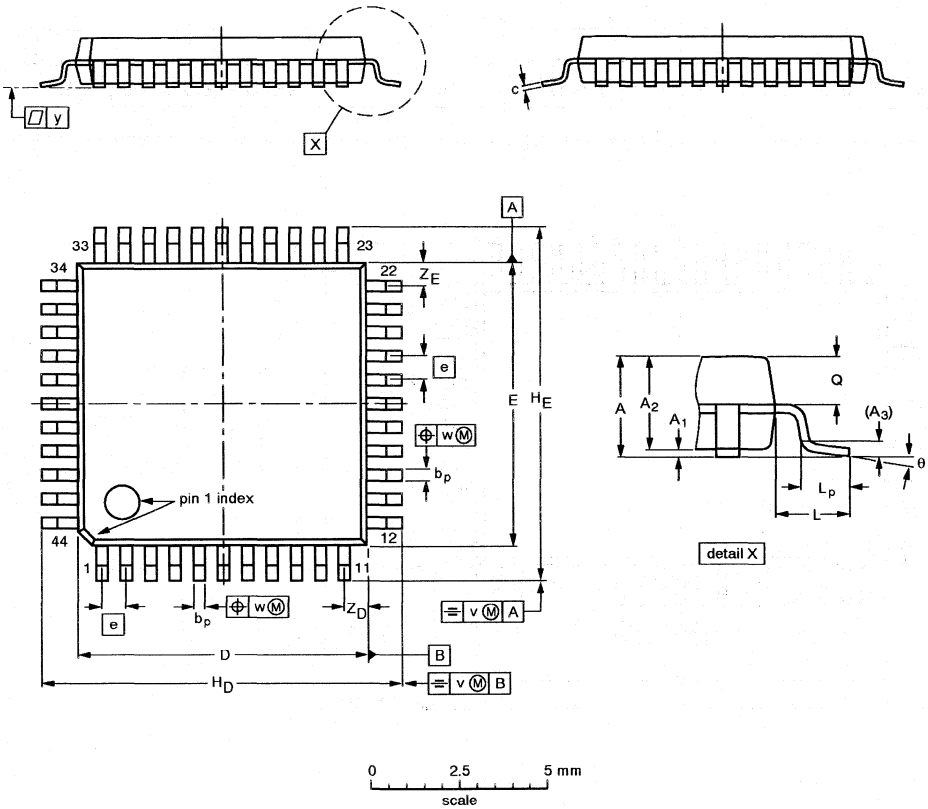
Note

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT190-1						~~92-11-17~~ 96-04-02

Package outlines

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

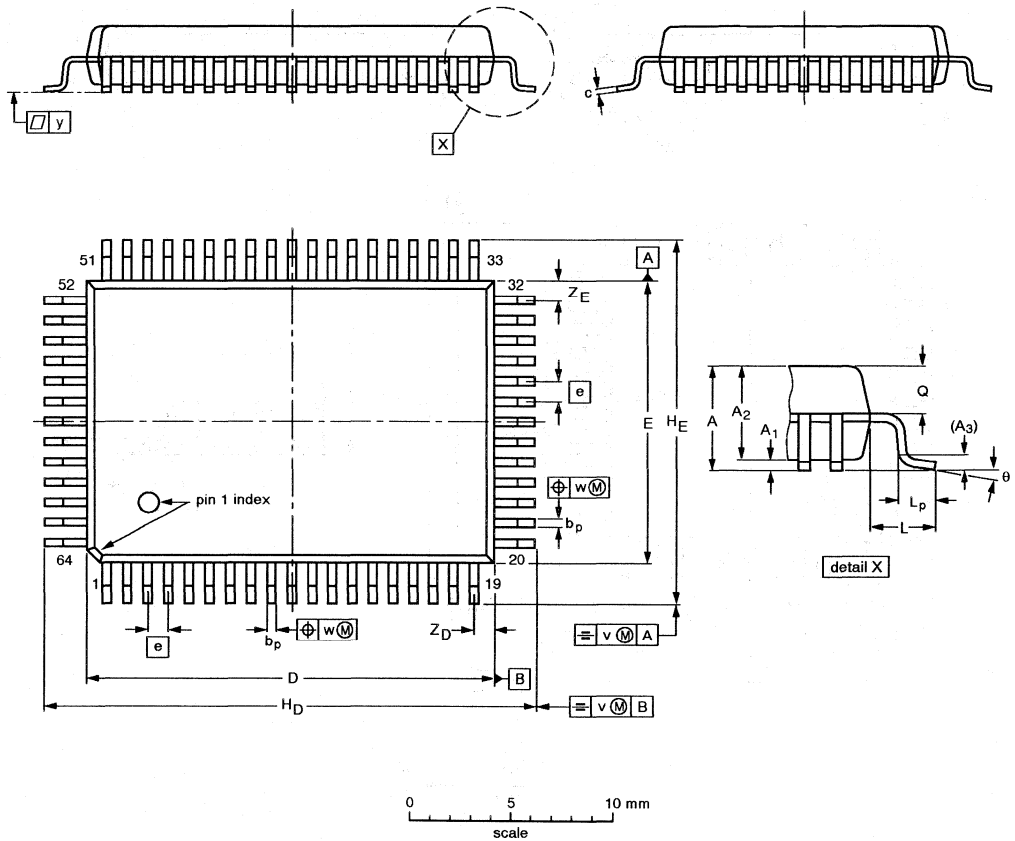
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

Package outlines

QFP64: plastic quad flat package; 64 leads (lead length 1.95mm); body 14 x 20 x 2.8 mm SOT319-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7° 0°

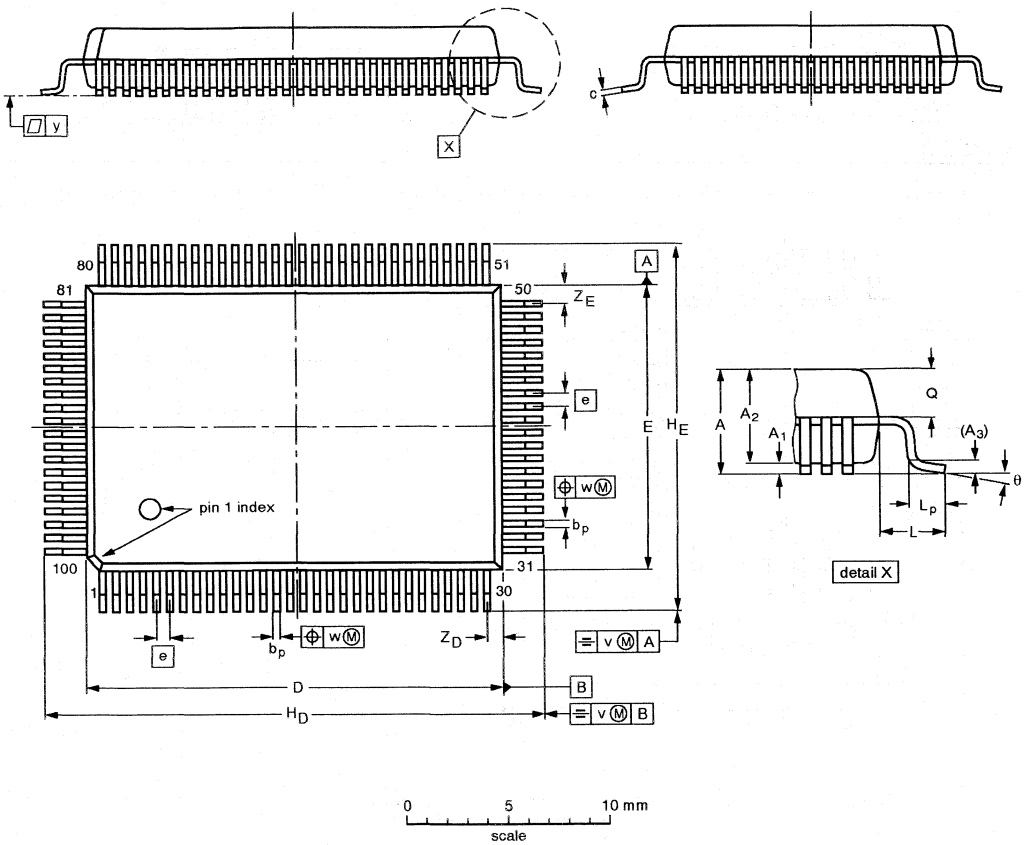
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~92-11-17~~ 95-02-04

Package outlines

QFP100: plastic quad flat package; 100 leads (lead length 1.95mm); body 14 x 20 x 2.8 mm SOT317-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7° 0°

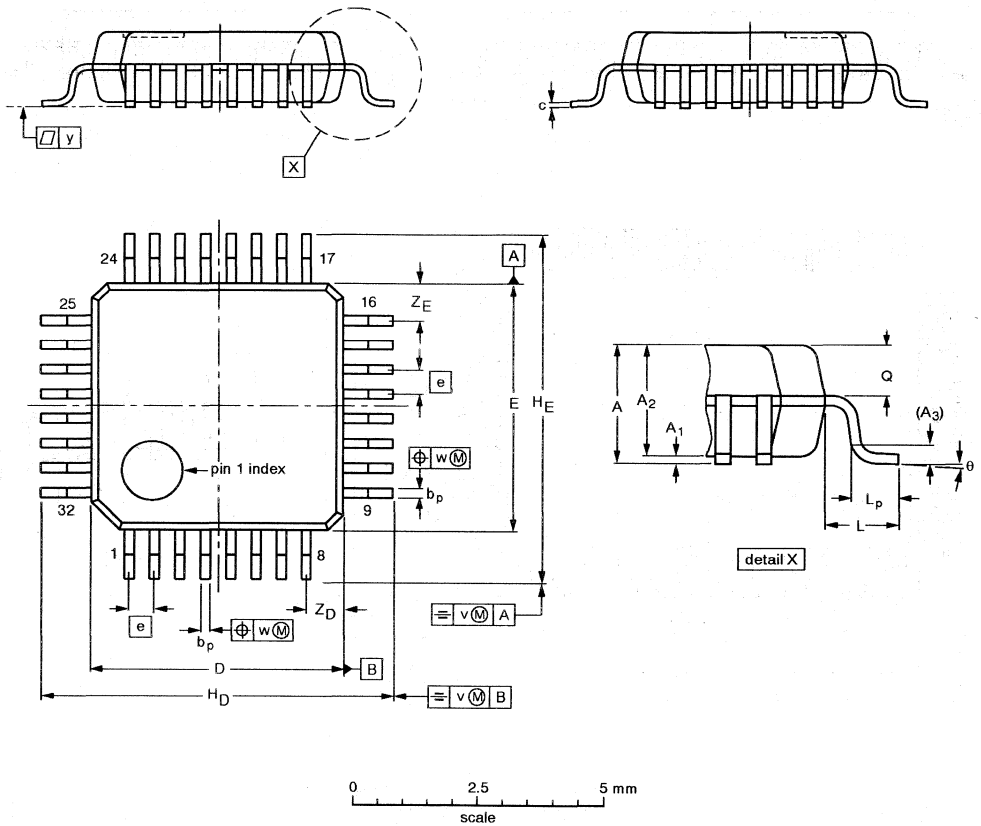
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~92-11-17~~ 95-02-04

Package outlines

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm — SOT401-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.70 0.57	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

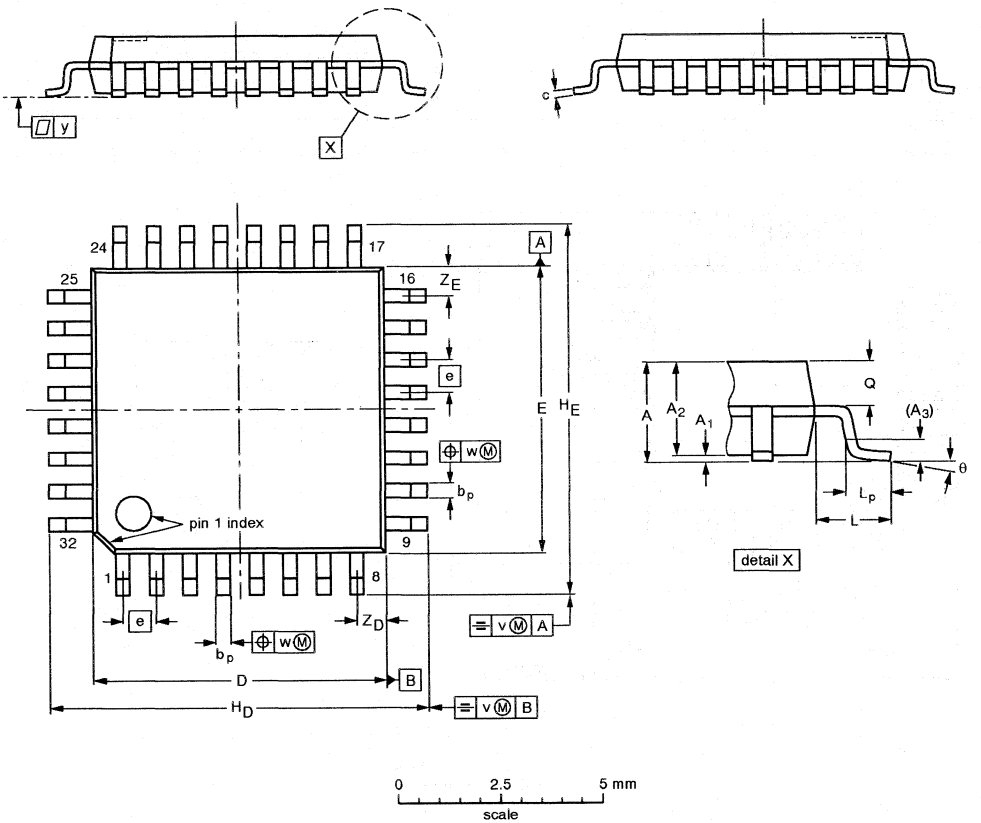
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~94-04-25~~ 95-12-19

Package outlines

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm — SOT358-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7° 0°

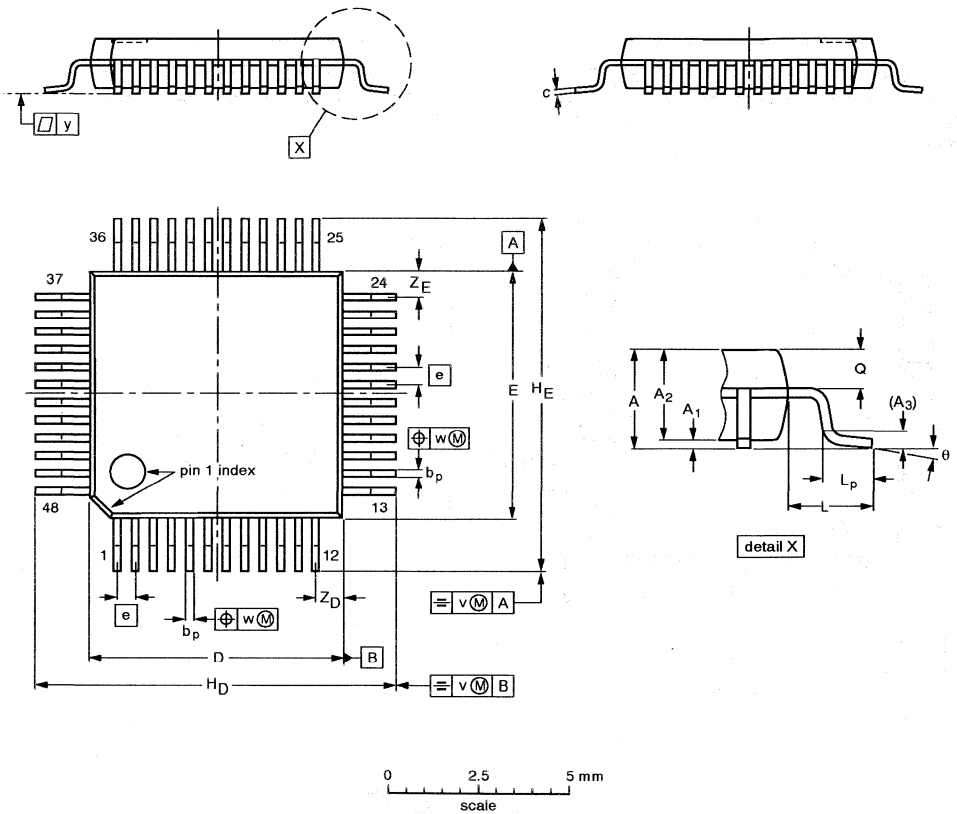
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1						~~93-06-29~~ 95-12-19

Package outlines

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm — SOT313-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

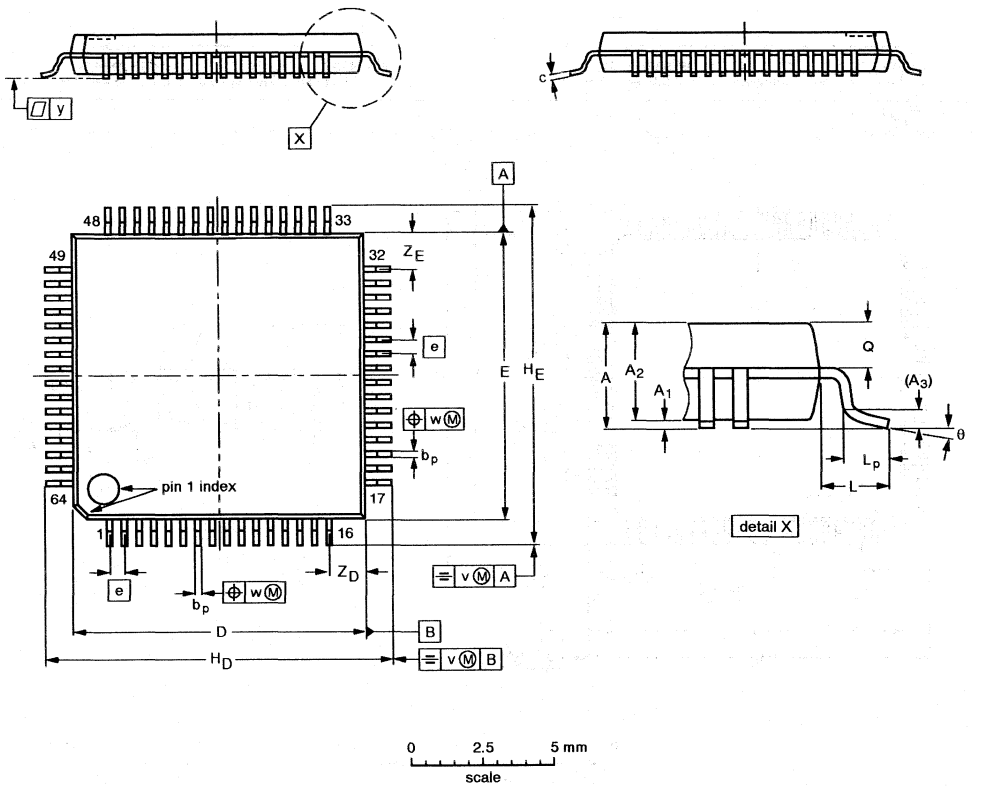
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~93-06-15~~ 94-12-19

Package outlines

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm — SOT314-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

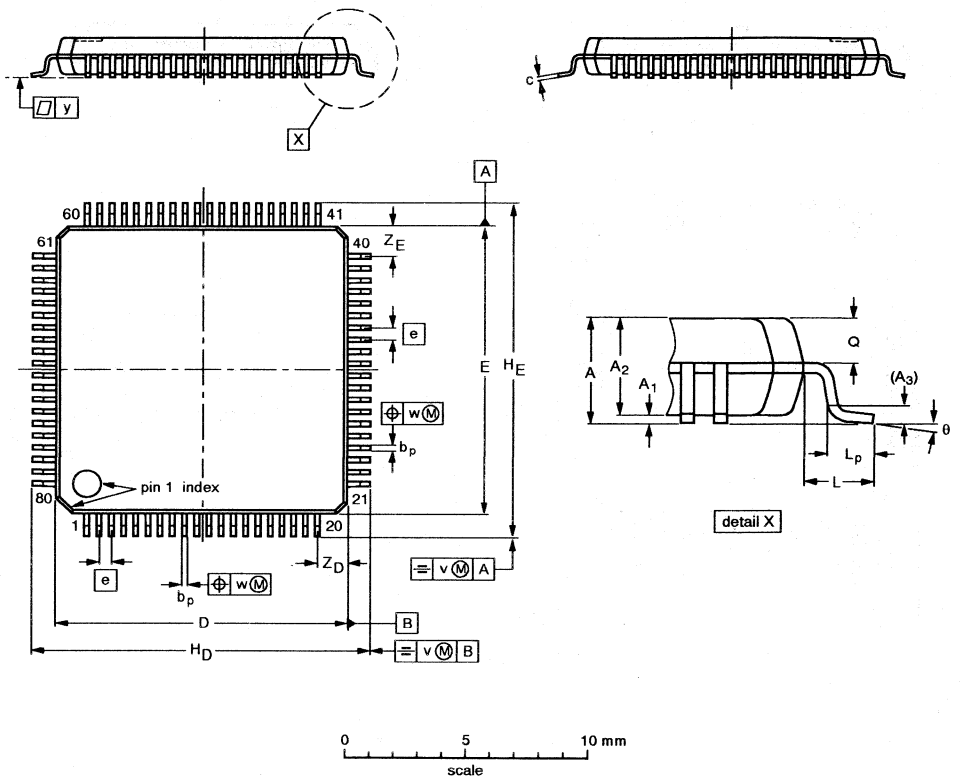
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~94-01-07~~ 95-12-19

Package outlines

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm — SOT315-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.25 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1.0	0.7 0.3	0.70 0.58	0.2	0.15	0.1	1.45 1.05	1.45 1.05	4° 0°

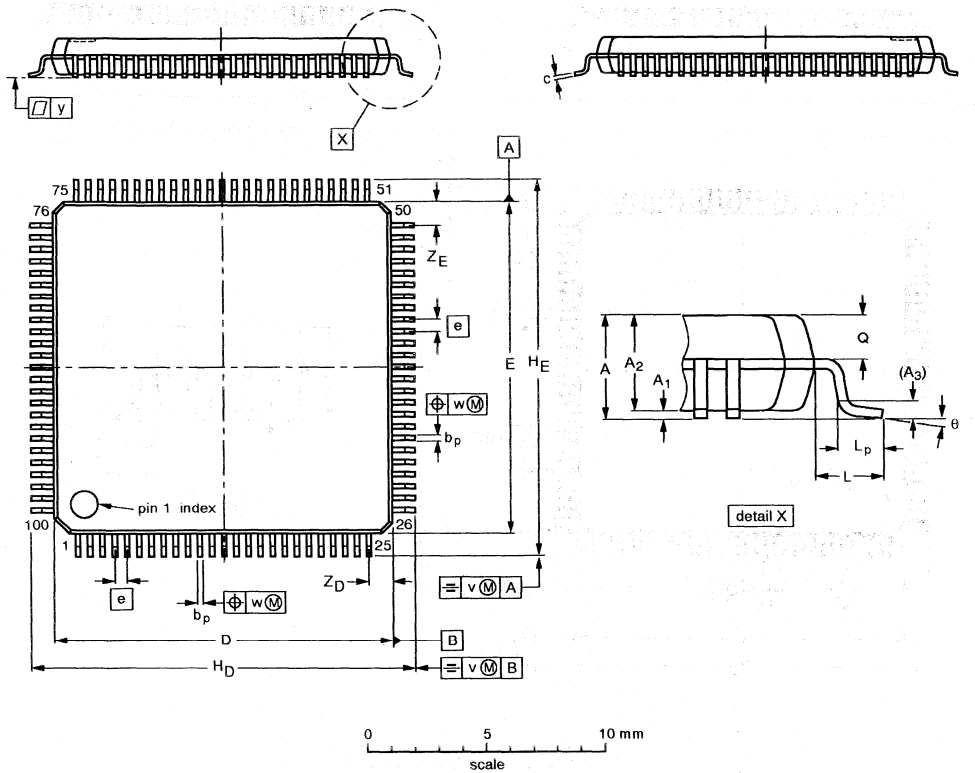
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT315-1						~~92-03-24~~ 95-12-19

Package outlines

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm — SOT407-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.70 0.57	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7° 0°

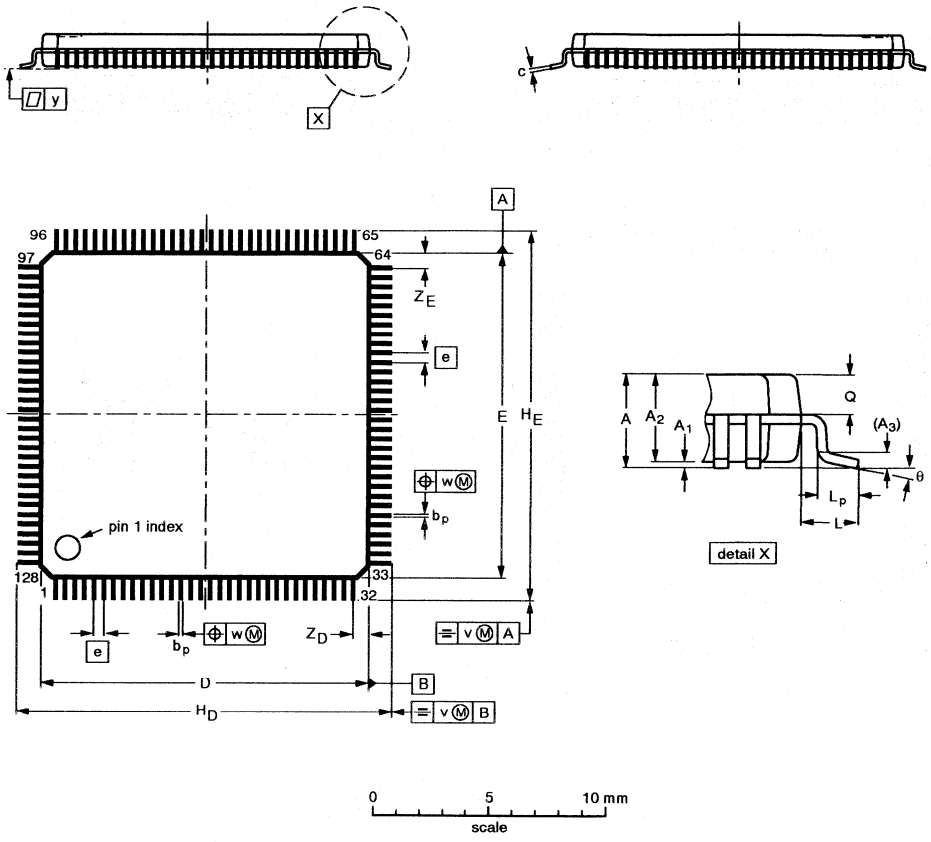
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						95-12-19

Package outlines

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 14 x 1.4 mm — SOT420-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.23 0.13	0.20 0.09	14.1 13.9	14.1 13.9	0.4	16.15 15.85	16.15 15.85	1.0	0.75 0.45	0.70 0.58	0.2	0.08	0.1	0.95 0.65	0.95 0.65	7° 0°

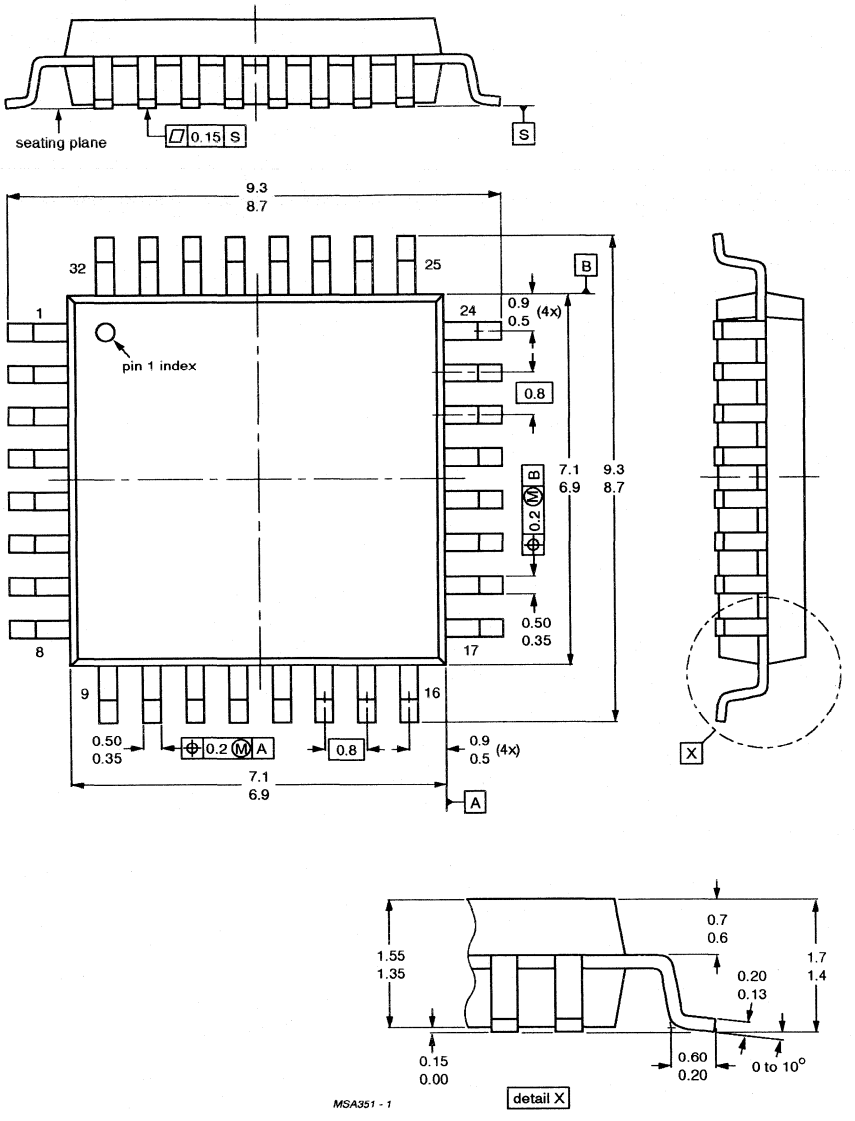
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT420-1						96-02-07

Package outlines

TQFP32: plastic thin quad flat package; 32 leads; body 7x7x1.4 mm **SOT358-2**



Dimensions in mm.

DATA HANDBOOK SYSTEM

1997 Jan

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